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Modulating the Filamentary-Based Resistive Switching Properties of HfO_2 Memristive Devices by Adding Al_2O_3 Layers

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Abstract: The resistive switching properties of HfO_2 based 1T-1R memristive devices are electrically modified by adding ultra-thin layers of Al_2O_3 into the memristive device. Three different types of memristive stacks are fabricated in the 130 nm CMOS technology of IHP. The switching properties of the memristive devices are discussed with respect to forming voltages, low resistance state and high resistance state characteristics and their variabilities. The experimental I–V characteristics of set and reset operations are evaluated by using the quantum point contact model. The properties of the conduction filament in the on and off states of the memristive devices are discussed with respect to the model parameters obtained from the QPC fit.

Keywords: bi-layers; quantum point contact model; memristive device; embedded applications; variability; conductive filament; CMOS compatibility

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1. Introduction

Novel applications, such as edge computing [1], big-data processing [2,3], image recognition [4] etc., demand efficient computing techniques and advancements in memory storage technologies [5]. CMOS compatibility, low power consumption, low cost, good endurance, fast switching, etc., are among the other features which are expected from the new memory technologies [6]. Besides the fact that the oxide-based memristive devices can exhibit all the above-mentioned features, it is also possible to monolithically integrate them with the CMOS logic on the same process nodes [7]. This adds to an advantage of using the memristive devices for embedded storage applications [8].

The memristive devices fabricated on silicon substrates are mainly used for memory storage [9], embedded [8] and neuromorphic computing applications [10]. Apart from silicon substrates, the memristive devices are also realized on polymer substrates for applications in the field of flexible electronics [11]. Oxides such as TiO_2 [12], NiO [13], ZnO [14], etc., among many others, are used as a physically flexible switching material in memristive devices. Further, the memristive devices are fabricated on glass substrates, which have low thermal conductivities, compared to silicon substrates [15]. The glass substrates favor the diffusion of oxygen vacancies [16]. An improved resisting switching performance in terms of higher memory window (MW), better endurance characteristics and lower value of reset voltages are reported in various oxides, such as HfO_x [15], SnO_2 [16], TaO_x [17] and MoO_3 [18]. This work mainly focuses on the memristive devices which are fabricated on the silicon substrates.

Among other memristive device types, the filamentary-based memristive devices have the advantages of good retention, fast switching and CMOS compatibility [19]. Resistive switching in the filamentary-based memristive devices is due to the redox reactions taking place at the switching layer, under the influence of electric fields [20]. Hafnium oxide (HfO_2), acting as a memristive switching layer, is one of the most extensively studied material in the literature [21,22]. The availability of the deposition processes and its CMOS compatibility are the main reasons for the wide usage of the material [23]. However, HfO_2 memristive devices integrated in back-end-of-line (BEOL) CMOS technology exhibit increased intrinsic device variabilities [24]. This challenge of reducing the variability in HfO_2-based memristive devices led to the investigations on further CMOS compatible materials [25]. Various oxides, such as Al_2O_3, TiO_2, Ta_2O_5, SiO_2, etc., among many others, have been used in combination with HfO_2 layers [26]. The material combinations are used either as ionic doping or in the form of stacked memristive layers, i.e., bi-layer, tri-layer and multi-layer memristive devices [27–29].

Due to their diverse potential applications, Al_2O_3 | HfO_2 bi-layers have been widely investigated in the literature [30,31]. The type of process and the precursors used for the deposition of Al_2O_3 layers plays a vital role for the performance of the memristive bi-layer devices [30–33]. Further, the aluminum oxide layer is widely used as a tunnel barrier in various kinds of memristive devices [34,35]. Various improvements of the resistive switching properties are reported in terms of uniform switching voltages and reduced dispersions of the high resistance state (HRS) [31], analog switching properties [33], etc.

The conduction filament (CF) properties in single layer memristive devices are discussed frequently with respect to the quantum point contact (QPC) model by various research groups [36–38]. Memristive switching oxides, such as HfO_2 [38] and TaO_x [39], are mainly used for the study. However, in the case of memristive bi-layers, in particular, Al_2O_3 | HfO_2 based devices, the resistive switching properties of the devices are discussed quite often, but the properties of their CF with respect to QPC are very seldomly discussed. Hence, in this work, the filamentary-based resistive switching properties of memristive HfO_2 devices are altered by adding the Al_2O_3 layers, which are deposited by using atomic layer deposition (ALD). Three different memristive layer stacks are compared in terms of their resistive switching behaviors. Further, the modulation in their conductive filament properties is analyzed within the frame work of the quantum point contact (QPC) model. The experimental I-V curves of the memristive devices from the set and reset operations are fitted using the QPC model for the low-resistance state (LRS) and the high-resistance state (HRS), respectively. Finally, the CF properties are discussed with respect to the model parameters obtained by fitting the experimental I–V characteristics to the QPC model.

2. Experimental

The integrated 1T–1R memristor devices are fabricated using the standard 130 nm CMOS technology of IHP. The CMOS transistor of gate length 130 nm and gate width 150 nm has its drain terminal connected to the bottom electrode (BE) of the memristor device. This forms a series connection between the memristive module and the CMOS transistor. Figure 1 shows the EDX with TEM cross section of the integrated 1T-1R memristive device. The integration of the memristor module into BEOL CMOS technology reduces the parasitic RC.

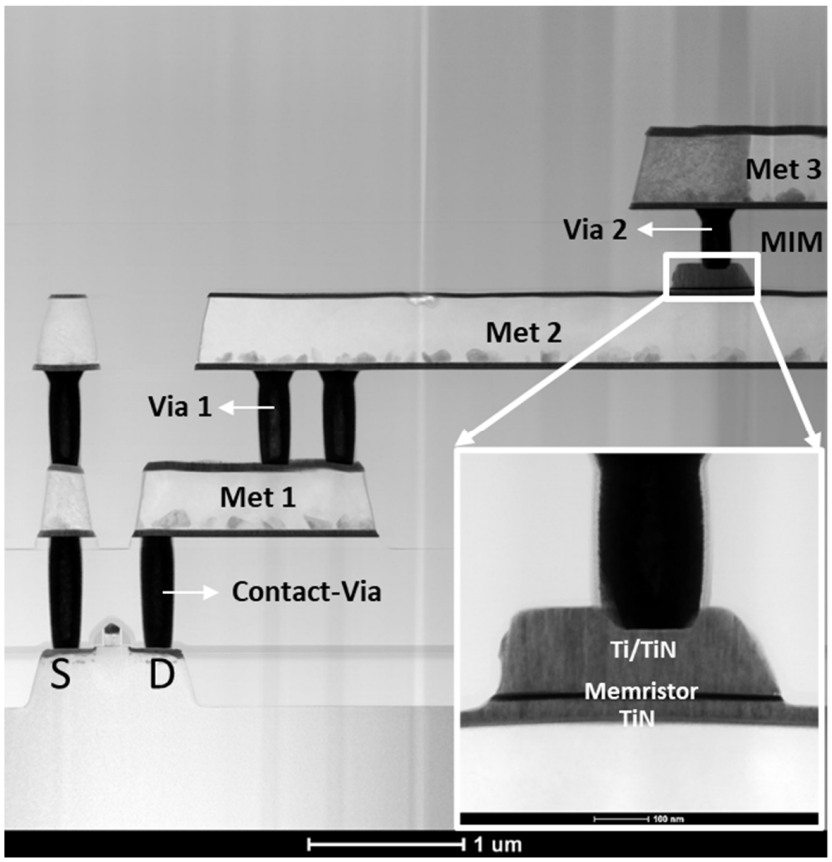

Figure 1. TEM cross-section of an integrated 1T–1R memristor device, fabricated in 130 nm CMOS technology. The inset micrograph illustrates the memristor module.

The memristor module, which is essentially a metal–insulator–metal (MIM) structure, is placed between metals 2 and 3 in the AlCu BEOL interconnects as shown in Figure 1. The BE of the memristor module consists of sputter deposited TiN of 150 nm thickness. The switching layers are deposited on top of the BE, using a CMOS compatible thermal ALD process at 300 °C. Aluminum oxide (Al_2O_3) layers are deposited by alternate pulsing of trimethylaluminum ($Al_2(CH_3)_6$) as a precursor and water (H_2O) as a reactant. Further, the deposition of HfO_2 takes place by the alternate pulsing of hafniumtetrachloride ($HfCl_4$) as a precursor and water (H_2O) as a reactant. In order to avoid gas phase reactions, an inert gas purge is performed after every pulse, which removes the unreacted precursor and reactants, and the byproducts of the self-termination reactions from the deposition chamber. The switching layers are deposited in three different types of stacks, namely, V1, V2 and V3, as illustrated in Table 1. The V1 variant is the reference sample, which consists of a single layer HfO_2 of 8 nm thickness. The V2 and V3 variants consists of thin Al_2O_3 layers of 1 and 2 nm thickness, respectively deposited on top of the TiN BE, in addition to the HfO_2 layer of 8 nm thickness, which is deposited successively without vacuum breakage. Eventually, V1, V2 and V3 device types comprise total dielectric layer thicknesses of 8, 9 and 10 nm, respectively. The presence of the thin Al_2O_3 layers is verified by the TEM cross section with EDX analysis as shown in Figure 2. The top electrode (TE) deposition of 7 nm thick Ti and 150 nm thick TiN above the dielectric switching layers prepares the MIM stack for subsequent process steps. The patterning of the MIM stack is one of the crucial steps in the memristor module fabrication and was realized by standard MIM module fabrication of a qualified SiGe–BiCMOS technology. The approach consists of an improved fabrication technique with a spacer and encapsulation process steps. Further details can be found in [40].

Table 1. Variants of memristive devices with respective layer thicknesses.

Description	V1 (nm)	V2 (nm)	V3 (nm)
TiN TE	150	150	150
Ti	7	7	7
HfO_2	8	8	8
Al_2O_3	-	1	2
TiN BE	150	150	150

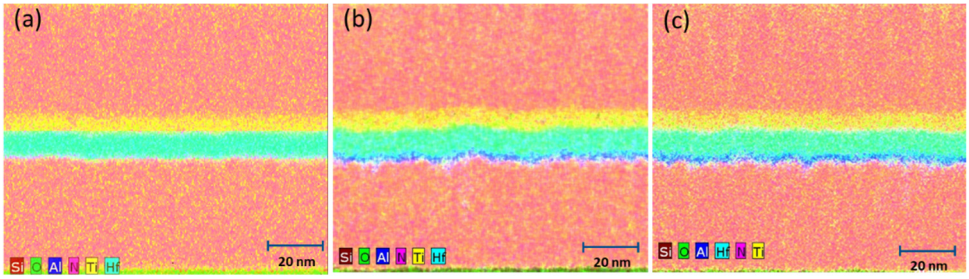

Figure 2. Cross-sectional TEM images with EDX elemental mapping of memristor modules in (**a**) V1 (**b**) V2 and (**c**) V3 variants.

The TEM and the energy dispersive X-ray (EDX) images were prepared using the Tecnai Osiris tool, which was operated at 200 kV. EDX analysis was performed in the scanning TEM mode using the software Esprit from Brucker. Further, the EDX measurements were quantified using the Cliff–Lormier method. The TEM lamella of samples were prepared by using the NVision 40 focused ion beam (FIB) tool from Zeiss. The surface of the samples was protected by using a carbon layer deposited through ion beam deposition technique. The prepared lamellas were lifted out using a micromanipulator. X-ray photoelectron spectroscopy (XPS) depth profile measurements were carried on a PHI5000 Versaprobe II tool with an Al Kα X-ray source (1486.6 eV) at 89.7 W.

The presence of thin Al_2O_3 layers was verified by using TEM and EDX analyses as shown in Figure 2. However, the stoichiometry of them was not determined using the EDX technique due to the limitation of their depth resolution. Further, the Al_2O_3 films were deposited using an industry standard TALD process with negligible nucleation delay with respect to their growth cycles [41]. The films were grown layer by layer using a self-terminated surface reaction process; they are reported widely in the literature to be stoichiometric [42,43]. Additionally, the Al_2O_3 layers grown on silicon substrates were analyzed using X-ray photoelectron spectroscopy (XPS) depth profile analysis for their stoichiometry as shown in Figure 3. The ratio of O/Al atomic concentrations was determined to be ~1.5, indicating the Al_2O_3 layers as being stoichiometric.

Electrical measurements of 1T-1R V1, V2 and V3 devices were performed under identical DC conditions at room temperature. The resistive switching performance of the memristive devices was tested with a Keithley 4200-SCS semiconductor parameter analyzer connected to a FormFactor PMV200 manual probe station. The characterization of the memristive devices begins with a crucial and onetime operation step called forming. During forming, the drain voltage (V_D) is double swept from 0 to 4 V while grounding the source terminal (S) and biasing the gate terminal (G) to 1.5 V. The forming operation is followed by reset and set operations. The reset operation was performed at a gate bias (V_G) of 2.9 V and, the source voltage (V_S) was double swept from 0 to 2 V while grounding the drain terminal (D). The set operation was performed similar to forming, except that the V_D was double swept from 0 to 2 V while grounding S. Finally, 10 devices of each variant were programmed by 50 subsequent cycles of set and reset operations.

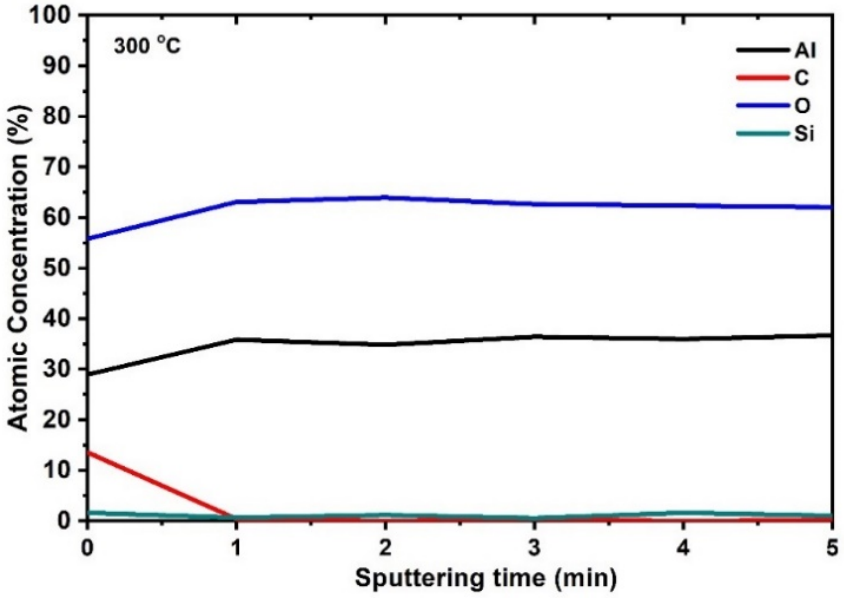

Figure 3. XPS depth profile analysis of Al_2O_3 layers deposited using TALD process at 300 °C.

3. Quantum Point Contact (QPC) Modelling

The conduction filament (CF) properties of V1, V2 and V3 memristive devices were analyzed using the QPC model. The reset and set I–V characteristics were used to model the conduction properties of the CF in HRS and LRS states of the memristive devices, respectively. The HRS I–V characteristics are modeled as [36]

$$\mathrm{I} = \frac{2e}{h}\frac{G}{G_O}\left(eV + \frac{1}{\alpha}Ln\left[\frac{1+e^{\alpha(\phi-\beta eV)}}{1+e^{\alpha[\phi+(1-\beta)eV]}}\right]\right) \quad (1)$$

where I is the measured current, V is the applied voltage, β is the potential drop at the cathode and anode interfaces, e is the elementary charge of an electron, h is the plank's constant, G/G_o is the conductance parameter which is also equal to number of CFs at very low voltages, φ is the potential barrier height, and α is the parameter related to the potential barrier thickness (T_B). Due to the asymmetry of the potential drop at the two ends of the CF, the β value is estimated to be 1. The presence of a potential barrier disrupting the CF is assumed in the HRS for all the three different types of devices V1, V2 and V3. A value of G/G_o equal to 1 is assumed. According to Lian et al., in the case of low voltages and high enough potential barriers, Equation (1) converges as below [37]:

$$\mathrm{I} = \frac{2e}{h}Ne^{(-\alpha\phi)}\left[V + \frac{\alpha\beta}{2}V^2\right] \quad (2)$$

where N is the number of CFs at HRS, which is assumed to be 1. The current limiting transistor is connected in series with the memristor device in a 1T–1R test structure. Considering the real case scenario of testing the memristive devices in the form of arrays, the read operation of the HRS takes place in the linear region of the transistor [44]. The resistance of the transistor at this point is negligible compared to the resistance of the memristive device [44]. Hence, the resistance of the select transistor is not taken into account for the HRS simulation using the QPC model.

Due to the metallic-like conductivity of the CF in the LRS of the memristive devices, the barrier confinement parameter α collapses to zero, resulting in a linear I–V relation. The resistance of the transistor in this case is comparable to the memristive device and hence cannot be neglected [45]. The value of R is determined from the simulations and electrical

characterization of the transistor. Finally, the LRS currents equation within the frame work of QPC model is illustrated as [38]

$$\mathrm{I} = \frac{NG_o}{1 + NG_oR}V \tag{3}$$

where $G_o = 2e^2/h = (12.9\ k\Omega)^{-1}$ is the quantum conductance unit, N is the number of CFs and, and $R = 3\ k\Omega$ is the series resistance extracted from the transistor output characteristics.

The expression for the width of the potential barrier (T_B) in the HRS state of the memristive device is illustrated as [36]

$$\mathrm{T_B} = \frac{h\alpha}{2\pi^2}\sqrt{\frac{2\Phi}{m^*}} \tag{4}$$

where m^* is the effective mass of the electron within the CF.

The radius of constriction (R_B) of the CF in the HRS state of the memristive device is expressed as [36]

$$\mathrm{R_B} = \frac{hz_o}{2\pi\sqrt{2\Phi m^*}} \tag{5}$$

where z_o is the first zero of the Bessel function J_o [36]. The value of z_o is equal to 2.404.

4. Results and Discussion

The mean values of the forming voltages with their dispersions versus the total dielectric thickness of V1, V2 and V3 memristive devices are as shown in Figure 4. Furthermore, the corresponding I–V characteristics of the forming operations are illustrated in Figure 5. The forming voltages increase with the addition of the Al_2O_3 layers in the V2 and V3 devices. According to the literature, the forming voltage of the memristive devices is directly proportional to the thickness of the dielectric and inversely proportional to the square root of the dielectric constant $\left(\sqrt{k}\right)$ [46,47]. The effective thicknesses of the memristive layers in V1, V2 and V3 devices are 8, 9 and 10 nm, respectively. Additionally, the measured dielectric constants of Al_2O_3 and HfO_2 are ~8.5 and ~22, respectively. The increase in the effective dielectric thickness with the addition of Al_2O_3 layers, which also has lower dielectric constant, plays a major role in the increase in the forming voltages observed in Figure 4.

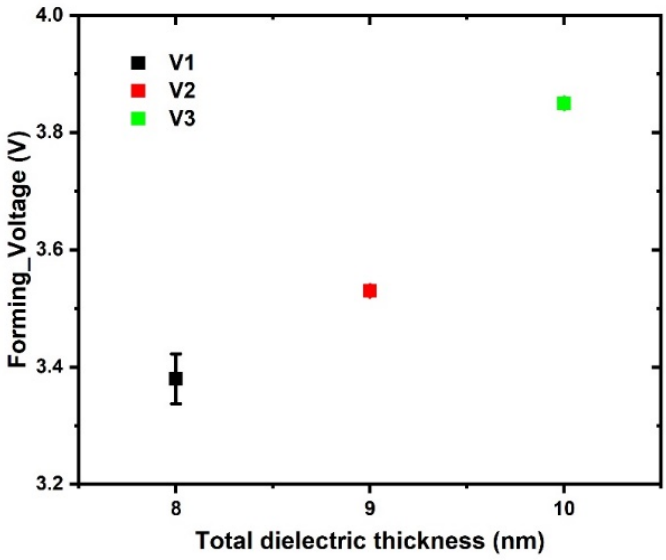

Figure 4. Mean values of forming voltages with error bars versus the total dielectric thickness of memristive device variants fabricated in 130 nm CMOS technology of IHP.

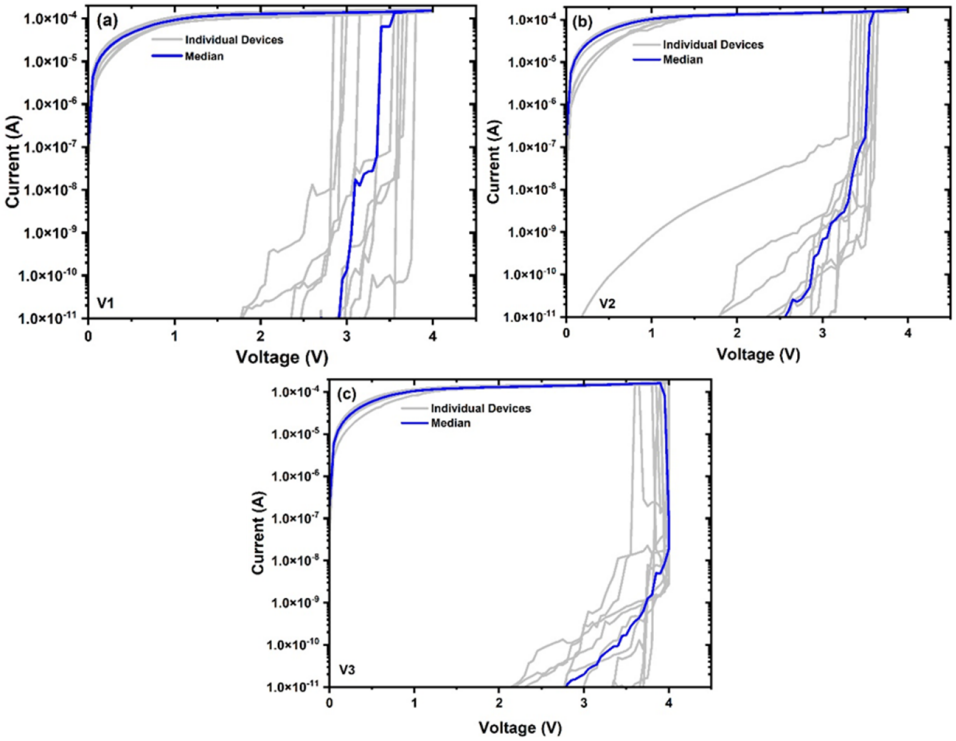

Figure 5. Forming I–V characteristics of (**a**) V1, (**b**) V2 and (**c**) V3 device variants. The characteristics of individual devices from each variant are represented in grey, and the computed median curves are represented in blue.

Further, the breakdown voltages of pure Al_2O_3 layers are investigated in MIM devices without CMOS transistors as shown in Figure 6a, and their corresponding schematic of the layer stacks are illustrated in the inset images. Figure 6b illustrates the TEM images with EDX analysis of single layer Al_2O_3 (6 nm) MIM devices with and without Ti. The images are included to verify the thickness of the Al_2O_3 dielectric layer under study. Due to the oxygen scavenging properties of Ti, the devices with 7 nm Ti layer exhibit lower breakdown voltages compared to the devices without the Ti layer. However, the single layer Al_2O_3-based MIM devices with and without the Ti layer exhibit higher breakdown voltages compared to V1, V2 and V3 devices. This clearly demonstrates the higher strength of Al_2O_3 layers for breakdown.

The variability in the LRS and HRS currents are analyzed with respect to the DC set operations. The values of the LRS and HRS currents of V1, V2 and V3 devices are extracted at a V_D value of 0.2 V. The box plots of LRS and HRS currents illustrated in Figures 7 and 8 are determined from 10 devices of each variant type. Figure 7 provides the summary of LRS currents distribution of all the three memristive device types. The mean values of the LRS currents increase with the thickness of the Al_2O_3 layers in the memristive stack. Furthermore, the addition of the Al_2O_3 layers reduces the variability of the LRS currents. The HRS currents extracted from 10 devices of V1, V2 and V3 devices are as shown in Figure 8. The mean values of the HRS currents increase with the thickness of the Al_2O_3 layers. The memory window (MW), which is essentially the on/off ratio of the memristive devices, is determined from the ratio of the LRS current values to the HRS current values. Both the LRS and HRS current values increase with the addition of the Al_2O_3 layers. As illustrated in Table 2, the mean values of the on/off ratios are determined to be, 86, 73, and 62 for V1, V2, and V3 devices, respectively. The increase in the LRS and HRS currents are discussed later in the same section, with respect to the QPC modeling. Although the values of the on/off ratios are reduced in V2 and V3 memristive devices, the variability in the on and off state currents of the resistive switching operations are also considerably reduced as shown in Figures 7 and 8. This reduction in variability is one of the basic

requirements of the memristive devices to utilize them for multi-level operation [48]. The memristive devices with a capability of multi-level operation are suitable for neuromorphic computing applications [49]. Although V3 devices exhibited higher forming voltage and lower memory window compared to V1 and V2 devices, the reduction in their LRS and HRS current variabilities makes them suitable for multi-level operation. The lower formation energy of oxygen vacancies in Al_2O_3 layers compared to HfO_2 layers may be responsible for the reduction in the LRS and HRS current variability [50,51].

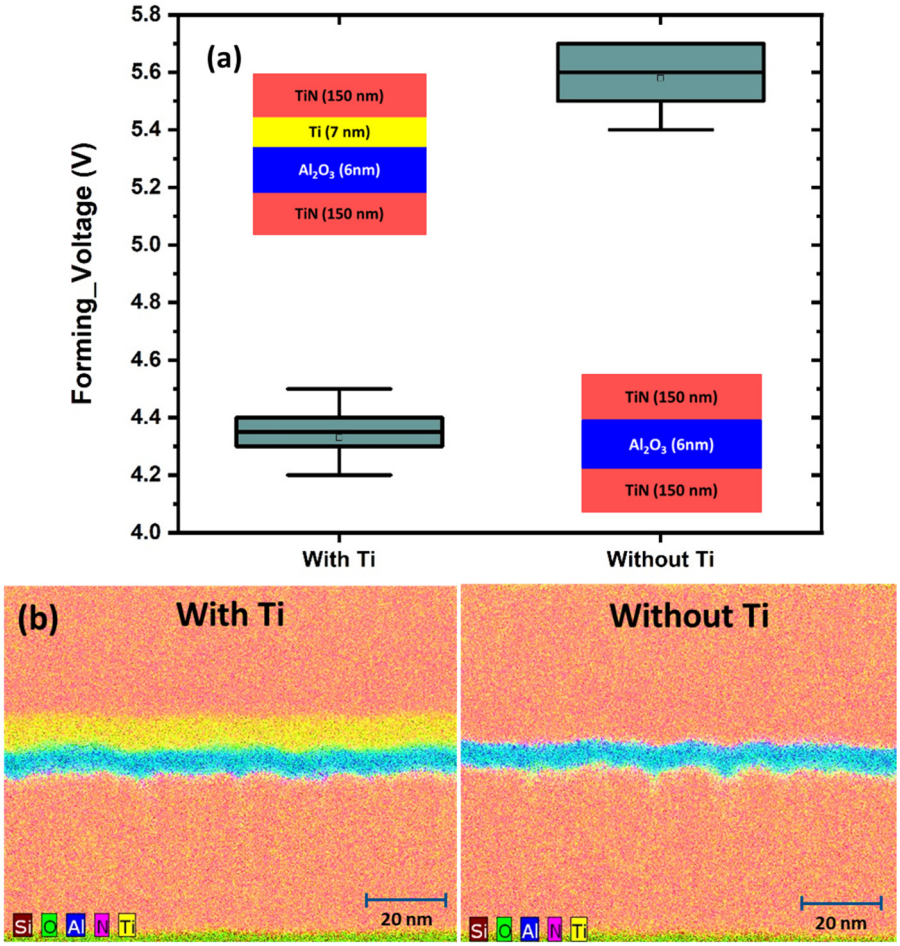

Figure 6. The single layer Al_2O_3−based MIM devices with and without Ti layer are (**a**) electrically characterized for their breakdown voltages (the inset images illustrate the schematic of the layer stack) and (**b**) material characterized by using cross-sectional TEM images with EDX elemental mapping.

Table 2. The mean values of memory window (MW) of V1, V2 and V3 devices determined from the respective mean values of LRS and HRS currents.

Description	V1	V2	V3
Mean LRS (A)	1.61×10^{-5}	2.35×10^{-5}	2.63×10^{-5}
Mean HRS (A)	1.88×10^{-7}	3.2×10^{-7}	4.23×10^{-7}
MW (Mean LRS/Mean HRS)	~86	~73	~62

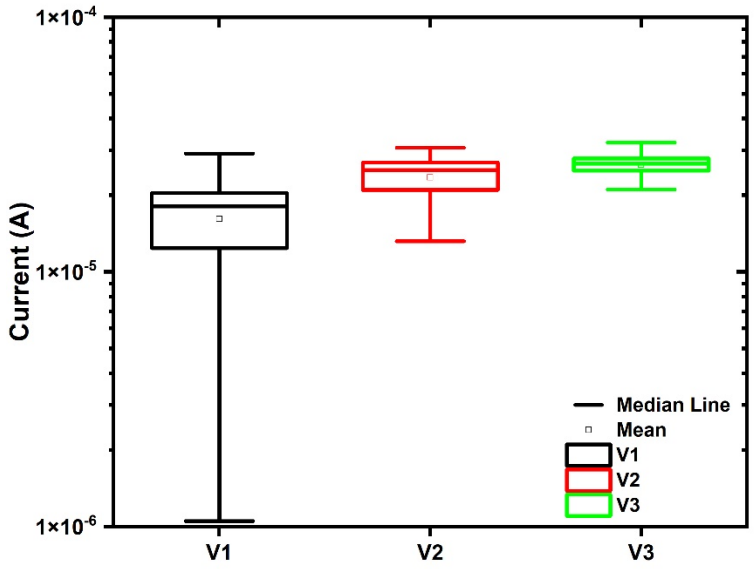

Figure 7. LRS currents extracted from DC set operations of V1, V2 and V3 memristive devices.

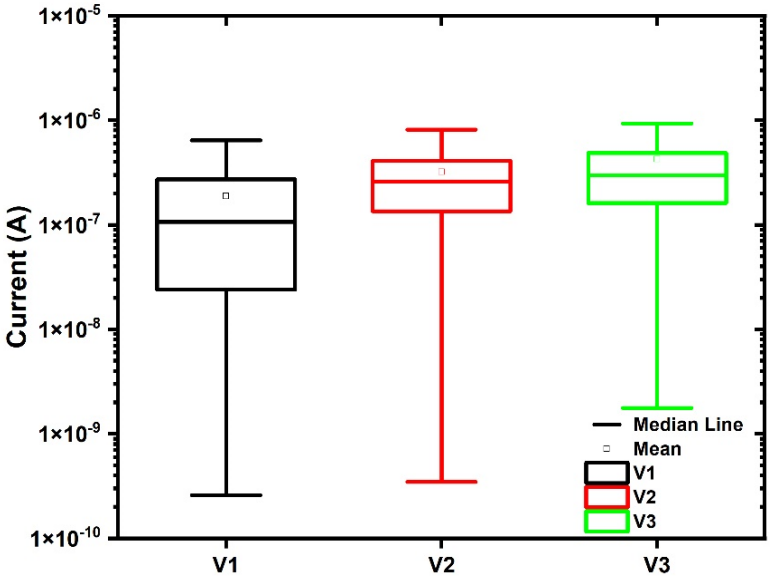

Figure 8. HRS currents extracted from DC set operations of V1, V2 and V3 memristive devices.

Figure 9 illustrates the QPC model fit for the experimental I−V characteristics of the mean values of the LRS currents from DC set operations of V1, V2 and V3 devices in the V_D range of 0 to 0.5 V. The LRS curves are fitted using Equation 3, and the model parameter N, which is the number of CFs in the memristive device, is extracted. It can be clearly seen that the LRS current values increase with the addition of Al_2O_3 layers. Additionally, the value of N increases as well with the thickness of the Al_2O_3 layer as illustrated in Table 3. The increase in the conduction values and the value of N with the addition of Al_2O_3 layers signifies the growth of stronger conduction filaments [52].

Table 3. The fitting parameter N extracted from the QPC model fit for LRS curves.

Description	N
V1	1.43
V2	2.33
V3	2.73

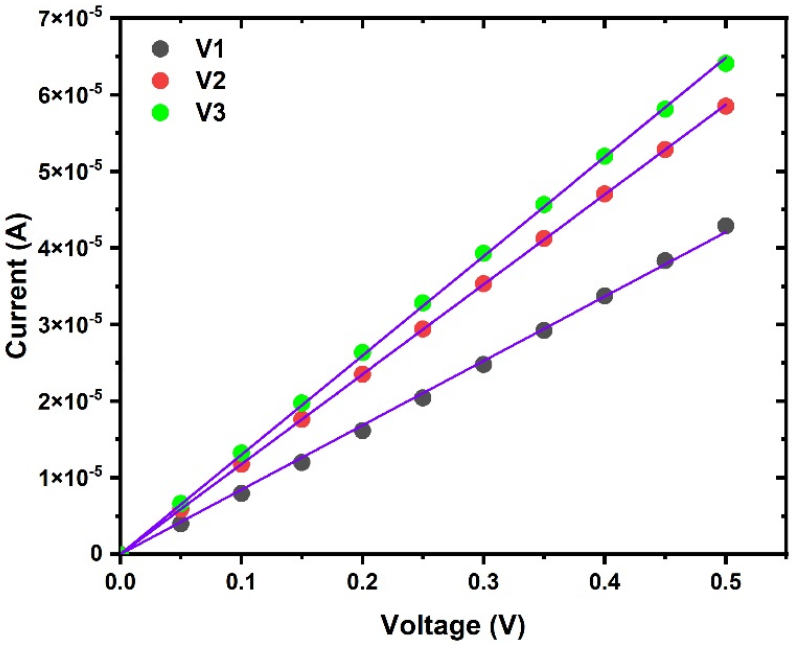

Figure 9. Experimental I–V characteristics (symbols) associated with the mean LRS currents extracted from DC set operations of V1, V2 and V3 memristive devices. The solid lines are simulated characteristics using the QPC model for LRS (Equation (3)).

The experimental I–V characteristics of the mean values of the HRS currents from DC reset operations of V1, V2 and V3 devices in the vs. range of 0 to 0.5 V are fitted using the QPC model as shown in Figure 10. Equation (2) is used for the fit, and the parameters α and φ are extracted. The values of the extracted model parameters are as illustrated in Table 4. The corresponding parabolic potential barriers of V1, V2 and V3 devices are schematically represented as shown in Figure 11. The values of α and φ obtained for V1 devices are comparable with the results from Grossi et al. [53]. The potential barrier height (φ) increases with the addition of Al_2O_3 layers. However, the HRS current levels increase as well with the addition of Al_2O_3 layers. During reset, the oxygen vacancies start to move toward the Ti layer due to which the CF gets partially re-oxidized and the constriction of the filament takes place near the BE interface [54]. Additionally, the dissolution of the CF is restricted in the Al_2O_3 layers due to the lower mobility of the oxygen vacancies compared to that of HfO_2 layers [33]. Hence, the constriction point becomes more localized with the addition of Al_2O_3 layers. Further, the claim is supported by the decrease in the shape parameter (α) and the T_B/R_B ratio as illustrated in Table 4. The ratios of T_B/R_B are determined from Equations (4) and (5). Additionally, the ratios are calculated instead of their individual values in order to omit the complex estimations and calculations related to the effective mass of the electron in the CF of the bi-layer memristive devices.

Table 4. The fitting parameters α and φ extracted from the QPC model fit for HRS curves and the determined ratios of T_B/R_B.

Description	α	φ	T_B/R_B
V1	17.61	0.29	1.35
V2	8.37	0.53	1.17
V3	6.75	0.6	1.07

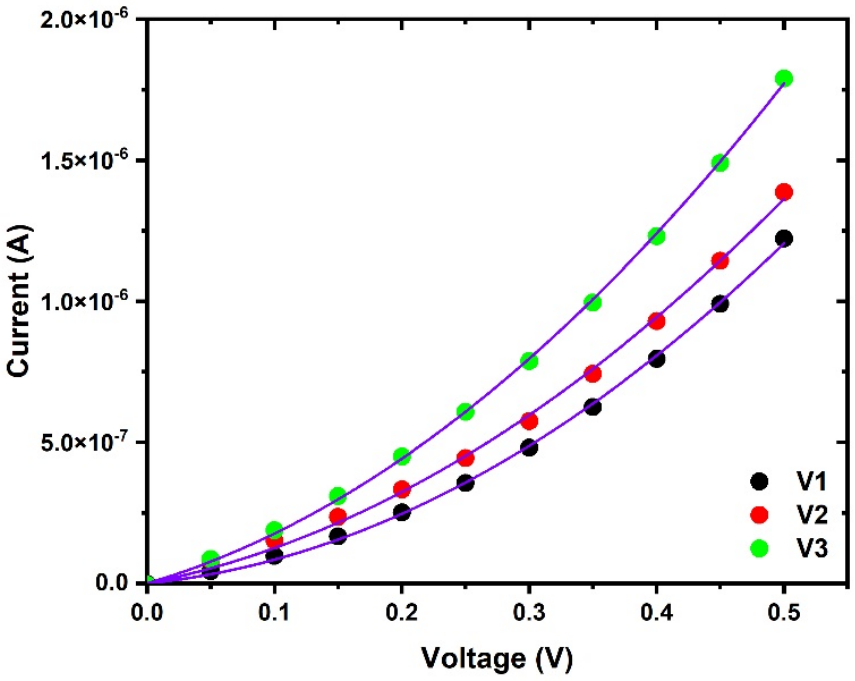

Figure 10. Experimental I–V characteristics (symbols) associated with the mean HRS currents extracted from DC reset operations of V1, V2 and V3 memristive devices. The solid lines are simulated characteristics using the QPC model for HRS (Equation (2)).

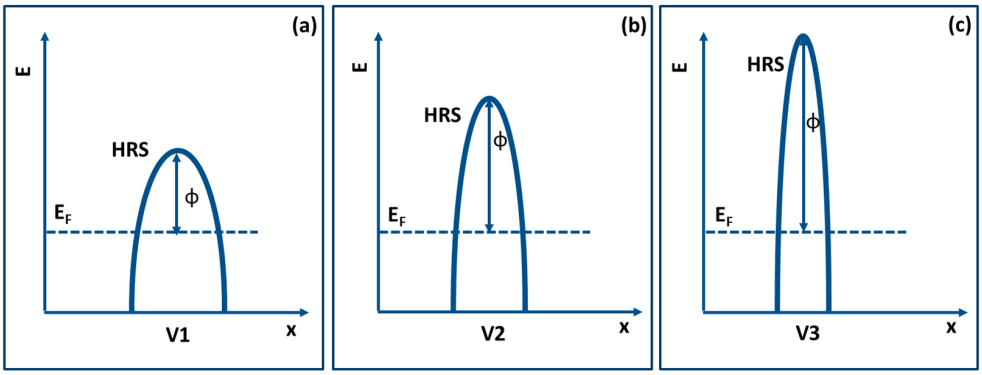

Figure 11. Schematic representation of the energy band diagram of the conductive filament potential barrier in (**a**) V1, (**b**) V2 and (**c**) V3 memristive devices. E is the energy of electrons, x is the direction of current flow in the filament, E_F is the Fermi level and φ is the potential barrier height with respect to the Fermi level.

5. Conclusions

The resistive switching behavior of hafnium oxide (HfO_2) based single-layer memristive devices are compared with Al_2O_3 | HfO_2 based bi-layer memristive devices. With the addition of Al_2O_3 layers, the LRS as well as HRS currents are increased, and the resistive on/off ratio is slightly decreased from 86 to 62, but finally the variabilities of read-out currents are strongly reduced. Furthermore, the CF properties are analyzed and discussed with respect to QPC modeling. The experimental I–V curves fit accurately with the QPC model. The addition of thin Al_2O_3 layers result in increasing the diameter of the conduction filaments in LRS and increasing the potential barrier height in HRS combined with reduced barrier thickness, resulting in localized constriction points of filaments. These results provide a promising platform for multi-level switching with high performance.

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