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# Optical Proximity Correction for 0.13 $\mu\text{m}$ SiGe:C BiCMOS

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## ABSTRACT

We present results for a rule based optical proximity (RB-OPC) and a model based optical proximity correction (MB-OPC) for 0.13  $\mu\text{m}$  SiGe:C BiCMOS technology. The technology provides integrated high performance heterojunction bipolar transistors (HBTs) with cut-off frequencies up to 300 GHz. This requires an optical proximity correction of critical layers with an excellent mask quality. This paper provides results of the MB-OPC and RB-OPC using the Mentor Calibre software in comparison to uncorrected structures (NO-OPC). We show RB- and MB-OPC methods for the shallow trench and gate layer, and the RB-OPC for the emitter window-, contact- and metal layers. We will discuss the impact of the RB- and MB-OPC rules on the process margin and yield in the 0.13  $\mu\text{m}$  SiGe:C BiCMOS technology, based on CD-SEM data obtained from the evaluation of the RB- and MB-OPC corrected SRAM cells.

**Keywords:** optical proximity correction, 0.13 $\mu\text{m}$  SiGe:C BiCMOS

## INTRODUCTION

Structures below 0.25  $\mu\text{m}$  require an OPC to guaranty well pattern printability and quality. The distortion of feature details increases significantly with smaller dimensions of the features due to the diffraction and the low-pass filter characteristics of the lithographic lens. The impact of the distortion on pattern quality can lead to complete failure of integrated circuits. Some of the main distortions are the line-end shortening (LES), bridging and corner rounding, for example. LES and bridging are most critical because of their high negative impact on pattern quality. Corner rounding and other effects, like line edge roughness (LER) and line width roughness (LWR) may not lead to failure, but they can have an impact on the transistor performance [1, 2]. A large LWR or LER of a transistor, for example, can be seen as several transistors with a different width and therefore with a different speed. In addition a larger area of the gate layer outside of the active shallow trench layer has a larger capacity which needs more time to load. This can be caused by e.g. corner rounding.

We study a RB-OPC and MB-OPC approach for 0.13  $\mu\text{m}$  SiGe:C BiCMOS technology at the IHP. The MB-OPC approach is made with relaxed settings in respect to LES to avoid bridging and less aggressive to reduce the mask writing time and costs. The technology provides integrated HBTs with cut-off frequencies up to 300 GHz [3, 4, 5]. The innovative device design and the OPC of the critical layers in the bipolar part is the key for increasing the performance, like increasing the speed of HBTs. The CMOS process was optimized for low-power applications. The device performance is highly associated with the patterning quality on the wafer. This requires an OPC of critical layers with an excellent mask quality e.g. CD (critical dimension), CD uniformity, CD linearity, registration and the transfer of the OPC corrections on the mask.

## METHODOLOGY

The shown results of the MB-OPC and RB-OPC are created with the Mentor Calibre software /6, 7/. The optical model for the MB-OPC was built with the vectorial TCCcalc model for high NA. The MB-OPC corrections were obtained from SEM measurements of test structures from Mentor Graphics. The applied RB-OPC was developed and tested in several steps for the 0.25  $\mu\text{m}$  and 0.13  $\mu\text{m}$  technology at the IHP. The RB-OPC is based on CD-SEM measurements on several test structures to study the distortions e.g. edge placement error (EPE) (line end – shortening, CD) and corner rounding. The coherence  $\sigma = 0.85$  of the KrF lithography tool for the gate and shallow trench layers is optimized for a low OPC effect vs. the pitch and for the correction of plasma etch bias differences between single and dens lines for the RB-OPC approach. The two OPC approaches and the uncorrected structures were applied on one mask set and exposed with the same illumination settings. We use the chemical amplified positive resist SL4800 and UV210 (Rohm&Haas) and a bottom anti-reflective coating (BARC). For the gate layer an antireflective hard mask of 33 nm PECVD  $\text{Si}_x\text{N}_y\text{O}_z$  /8/ and for the shallow trench layer 70 nm AR10L (Rohm&Haas) as BARC were applied. The exposure was carried out with high NA KrF-Scanner Nikon S207D with  $\text{NA}=0.75$  and  $\sigma = 0.85$ .

For the mask fabrication the layer data have to be fractured to get the mask data for e-beam exposure. This is done with the MGS (mask data generating system) by FhG IPMS /9, 10/. The fracturing is realized with a 10 nm grid. For high-end masks the e-beam proximity effect has to be compensated. Forward-scattered electrons within the resist (effective range about 0.1  $\mu\text{m}$ ) and back-scattered electrons from the substrate back into the resist (range about a few microns) cause a distorted dose distribution different from the nominal dose. This leads to dose losses at edges and small structures. The nominal dose has to be corrected to get the intended dose in the resist. The proximity correction is calculated within MGS using a set of input parameters. This set is unique for a certain manufacturing process and was determined in several tests.

The OPC generated masks were manufactured at Photronics Dresden using the variable shape e-beam writer ZBA320 from VISTEC. For high accuracy the resist development was done on a Steag ASE5000 and the etching on a Unaxis GenIII. For CD measurement  $\mu\text{-Tec}$  LWM 250 UV tool in I-line mode was used. CD values below 0.5  $\mu\text{m}$  were measured by a CD-SEM KLA 8100 XPR. The registration measurements were done by a Vistec LMS IPRO. The defect inspection tools are Orbot RT 8000 for Die-to-Database inspection, a Lasertec MD 2000 for Die-to-Die inspection (I-line), and a KLA-Starlight for contamination measurement.

## DATA

In table 1 we present RB- and MB-OPC methods for the critical layers shallow trench, gate, and the RB-OPC for the emitter window-, contact- and metal layers.

Table 1: OPC of the 0.13  $\mu\text{m}$  SiGe:C BiCMOS technology. The rule based OPC was carried out by CD- or edge placement error (EPE)-, line end shortening (LES)- correction and using of inner and outer serifs. In addition the model based OPC was applied.

Layer	CD		OPC				
	Type	nm	EPE / CD	LES	Inner Serif	Outer Serif	Model
Shallow trench	Clear bar	150	-	-	x	x	x
Gate	Chrome bar	130	-	-	x	x	x
Emitter window	Clear bar	180	x	x	x		-
Emitter poly	Chrome bar	340	x	x	-	-	-
Contact	Clear hole	160	-	-	-	-	-
	Clear bar	160	x	x	-	-	-
Metal 1	Chrome bar	160	-	-	-	x	-
Metal 2 -6	Chrome bar	200	-	-	-	x	-

The line end shortening (LES) and CD or edge placement error (EPE) of emitter window have been determined with test windows of different length, widths (in a 120 nm - 220 nm range) and serif sizes. An example is given in Fig 1. The exposure was carried out by using  $\text{NA}_{\text{lens}} = 0.75$  and  $\text{NA}_{\text{ill}} = 0.52$  with 320 nm UV210 (Rohm&Haas) on 70 nm bottom anti-reflective coating (AR10L, Rohm&Haas). For the emitter window OPC we use 80 nm serifs to correct the LES and EPE for clear bars.

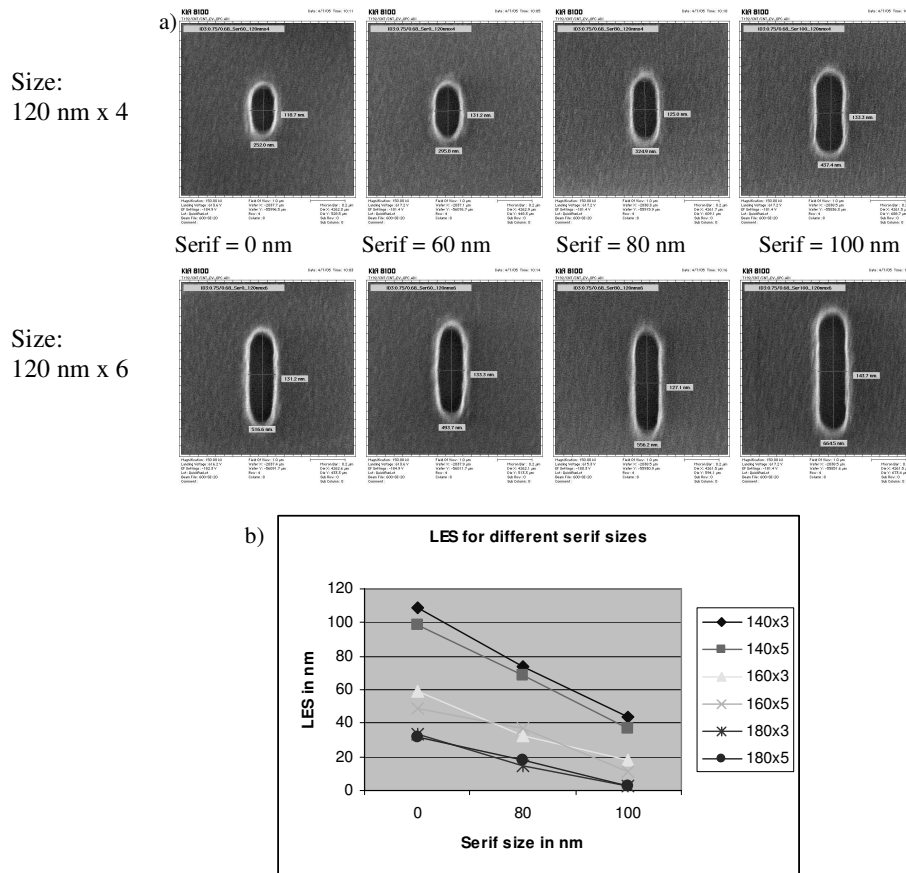


Figure 1: a) SEM images show test emitter windows of 120 nm width and length of 4x and 6x times the width with different serif sizes. The structures are used to determine the RB-OPC for the different emitter windows. b) LES with different serif sizes for different emitter window lengths

For the contact clear bars we use the same algorithm for the OPC like the emitter window RB-OPC for EPE and LES corrections. A serif OPC is not necessary due to the fixed window dimension of the contact clear bars. To determinate the RB-OPC for the shallow trench and gate layer we tested several serif sizes for the inner and outer serifs. In addition we shift the inner serifs out of the center position. After evaluation of different serif sizes and placing, we apply 70 nm outer serifs and 100 nm inner serifs to the 0.13  $\mu\text{m}$  technology. The inner serifs for the gate layer are shifted by 10nm out of the center placement, so the serif is shifted by 40 nm into the corner. In the 0.25  $\mu\text{m}$  SiGe:C BiCMOS technology we achieved a contact resistance decrease of 35% and 10% yield increase with the serif RB-OPC. Due to those results we use the serif RB-OPC in the 0.13  $\mu\text{m}$  BiCMOS technology changing the serif dimension to 60 nm for Metal 1 and 80 nm for Metal 2-6. The OPC was electrical tested using contact chains by measurement of contact resistance yield.

For the MB-OPC we exposed and measured 216 test structures created by Mentor Calibre for the shallow trench and gate layer. The test structure set consists of several structure types e.g. lines, grids at different pitches /6, 7/. The models are based on CD measurements of test structures. The edge placement error (EPE) is calculated based on the measured CD values. The fitted OPC-models were tested with verification structures to control the predictability of the build MB-OPC models.

Furthermore we use the simulation software SOLID-E /11/ for further investigation.

## RESULTS

For the evaluation of the effect of the different OPC approaches we use a 4 MBit SRAM cell. On the mask set we applied a NO-OPC, a RB-OPC and a MB-OPC corrected version of the SRAM. As shown in table 1, we applied the MB-OPC only to the shallow trench and gate layer. At first we compare the layout for the gate layer with the structures on the masks. Therefore the fabricated masks were inspected with a KLA-Tencor 8100XPR SEM CD. An example for every OPC approach for the gate layer is shown in Fig. 2.

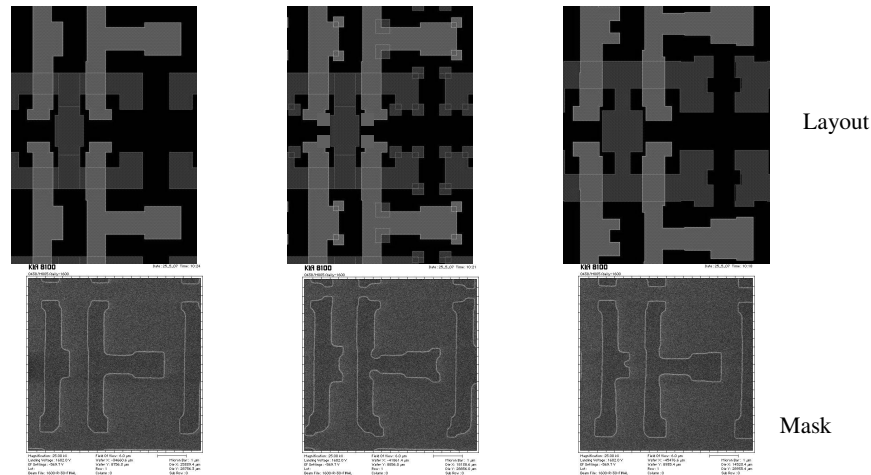


Figure 2: SRAM layout (STR and Gate layer) and the mask images (Gate layer) for the uncorrected, the RB-OPC and MB-OPC approach (left to right).

The images (Fig. 2) show a very good transfer of the layout to the mask. For the RB-OPC approach the inner and outer serifs are well printed. Because of the plasma-etch a rounding at the edges is to be seen, especially for the inner serifs. The mask image of the MB-OPC approach shows a good printing of the small details, but also the same rounding at the edges. All in all we see a good transfer of the RB-OPC and the calculated MB-OPC features to the mask.

Second we investigate the resist pattern, especially the LES and corner rounding for the three versions. We use KLA Tencor eCD 2 and the CD2D offline software /12/ for the measurements on top-down SEM images.

For the uncorrected gates (NO-OPC) we see a LES of 60 nm. The applied MB-OPC corrects the LES down to 46 nm, owing to a relaxed minimum structure space of 130 nm to prevent bridging. The RB-OPC improves the LES to 27 nm and shows the best result. The RB-OPC places a serif at the edge of the gates. The minimum distance between the serifs is only 90 nm. An example of the layout differences is given in Fig. 2. For the uncorrected structures the space between the gates is 160 nm. For the RB-OPC approach we have the same distance except for the serifs, where the minimum space is 90 nm. With the used settings for the MB-OPC we get a minimum space of 130 nm. The structures for the LES and corner rounding investigation are shown in Fig. 3 and the results in table 2.

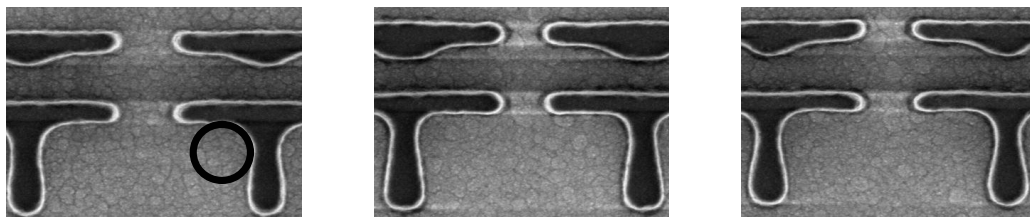


Figure 3: SEM images of the gate layer resist structures for the uncorrected, RB-OPC and MB-OPC approach are shown (left to right). The corner rounding is measured at the marked spot on the left and right side of the feature.

Table 2: Remaining line-end shortening and the corner rounding for the three OPC variants.

	LES in nm	Corner radius in nm (left / right)
NO-OPC	60	158 / 153
RB-OPC	27	124 / 130
MB-OPC	46	140 / 141

In table 2 we show the results of the corner rounding measurement for the uncorrected, the RB-OPC and the MB-OPC. The RB-OPC shows the smallest corner rounding, but we measure differences for the left and right side of the structure. The corner rounding of MB-OPC is between the uncorrected and the RB-OPC, but shows the same results for the left and right side of the structure. The differences results form the different corner correction. For the RB-OPC the inner serifs have a size of 100 nm and are shifted by 10 nm out of the center of the concave corners. The MB-OPC corrects the concave corners over a length of 135 nm and cuts 5 nm on the left and 15 nm on the right side of the structure.

After the evaluation of LES and the corner rounding, we investigate the process window for gate layer structures. For this investigation we expose the gate layer at different focus settings and compare the SEM images. Fig. 4 shows the top-down SEM images with the best focus point (focus = -0.05) and a defocus in + 0.25 / -0.2 direction.

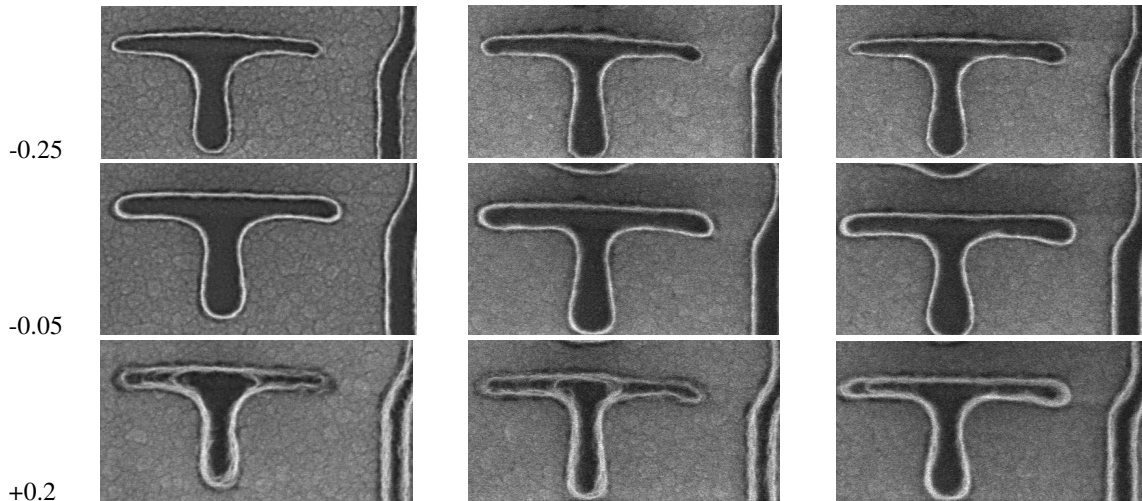


Figure 4: The images show the gate layer resist structures for the uncorrected, RB-OPC and MB-OPC version (left to right).

If we compare the resist structures at defocus points (-0.25 and +0.2) we see noticeable differences in the pattern quality. The distortion of the uncorrected and RB-OPC structures is higher than for the MB-OPC structures, especially for positive defocus.

In addition, we compare top-down SEM images after the gate layer etch step. The images for the NO-OPC, RB-OPC and MB-OPC corrected structures are shown in Fig. 5. The images are very enlightening, because the overlay of the gate structure to the shallow trench layer is visible. This allows a very good comparison of the three versions for both layers.

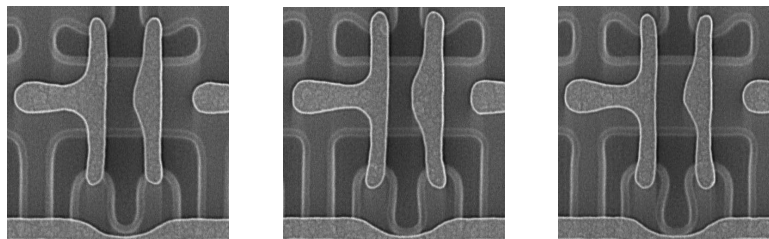


Figure 5: SEM top-down images for the uncorrected, the RB-OPC and the MB-OPC version after gate poly etch (left to right). The pictures show the shallow trench and gate layer.

As to be in Fig. 5, even the version without any OPC correction, show good pattern fidelity. In comparison with the RB-OPC and the MB-OPC significant differences are visible. The transistor gates, for example, are much longer and less sensitive to process fluctuations e.g. defocus. As already mentioned, the uncorrected structures show a higher distortion at defocus in comparison to the RB- and MB-OPC.

## CONCLUSION

In summary, we successfully apply and test a RB-OPC and MB-OPC approach for the critical layers in the 0.13  $\mu\text{m}$  BiCMOS technology. In comparison between the RB-OPC and MB-OPC to uncorrected structures we see improvements in respect of LES, corner rounding and the process window. Furthermore we see that the relaxed settings for the MB-OPC can be tightened for better LES control. The developed OPC approaches were applied to 0.13  $\mu\text{m}$  BiCMOS technology with excellent RF performance of  $f_T = 255$  GHz and  $f_{\text{max}} = 315$  GHz ( $BV_{\text{CEO}} = 1.8\text{V}/5/$ ).

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