

Studierende/r

Name

Wendt

Vorname

Thilo

Semester

M-APR 3

Studiengang

Applied Research in Engineering Sciences

Abschlussarbeit

Titel

Inference and Training of a Multilayer Perceptron in a Deep Reinforcement Learning Context on a FPGA

Erstkorrektor/in in der Technischen Hochschule

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Abgabedatum

09.05.2022

Durchgeführt in (Firma/Behörde/Hochschule)

Institut ELSYS

Betreuer/in in Firma/Behörde

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Zusammenfassung

This thesis addresses the design and verification of a multilayer perceptron (MLP) and the corresponding optimization algorithm, the batch gradient descent (BGD), on a FPGA using high level synthesis (HLS) for Xilinx devices. The solutions developed in this project are used in a reinforcement learning environment for the control of power electronic systems. The thesis briefly presents the principle of reinforcement learning, a mathematical description of the MLP and the BGD as well as programming techniques for HLS. The structure of the solutions and performance examinations are presented in the results part of the thesis. The project delivers functionally verified solutions for the execution on a FPGA. The solutions are able to process a three layer MLP with 16 inputs and outputs and 128 neurons in the hidden layer in 2,361 clock cycles at 100 MHz clock frequency which results in a runtime of 23.6 μ s. The corresponding BGD for one training example features a minimum runtime of 13,141 clock cycles or 1,314 μ s. However, performance is expected to further improve after resolving several issues described in the thesis.

Schlüsselworte

FPGA, Artificial Neural Network, Batch Gradient Descent, High Level Synthesis

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