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Decay mechanisms in CdS-buffered Cu(In,Ga)Se$_2$ thin-film solar cells after exposure to thermal stress: Understanding the role of Na

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Abstract

Due to their tunable bandgap energy, Cu(In,Ga)Se$_2$ (CIGSe) thin-film solar cells are an attractive option for use as bottom devices in tandem configurations. In monolithic tandem devices, the thermal stability of the bottom device is paramount for reliable application. Ideally, it will permit the processing of a top device at the required optimum process temperature. Here, we investigate the degradation behavior of chemical bath deposited (CBD) CdS-buffered CIGSe thin-film solar cells with and without Na incorporation under thermal stress in ambient air and vacuum with the aim to gain a more detailed understanding of their degradation mechanisms. For the devices studied, we observe severe degradation after annealing at 300°C independent of the atmosphere. The electrical and compositional properties of the samples before and after a defined application of thermal stress are studied. In good agreement with literature reports, we find pronounced Cd diffusion into the CIGS absorber layer. In addition, for Na-containing samples, the observed degradation can be mainly explained by the formation of Na-induced acceptor states in the TCO front contact and a back contact barrier formation due to the out-diffusion of Na. Supported by numerical device simulation using SCAPS-1D, various possible degradation models are discussed and correlated with our findings.

KEYWORDS
CdS buffer layer, CIGSe, degradation mechanism, elemental interdiffusion, Na, SCAPS, simulation, thermal stress

1 | INTRODUCTION

Recently, Cu(In,Ga)Se$_2$ (CIGSe) thin-film solar cells have shown an efficiency boost up to 23.35% by alkali post-deposition treatments

(PDTs).[1] According to the theoretical limit of about 33% at a bandgap energy of 1.15 eV[2] for single junction devices, there is still open room to further increase their efficiency. One approach to achieve this could be to decrease the absorption losses in the transparent conductive

[Correction added on 11 June 2021 after first online publication: Tables 1 and 2 have been corrected in this version.]

oxide (TCO) used as front contact material by increasing its transparency. For this, it would be of great advantage to be able to work at elevated deposition temperatures and/or to apply a post-deposition annealing.[3–5] Another possibility to increase device efficiencies even past the single junction Shockley–Queisser limit is to fabricate multi-junction solar cells by utilizing different wavelength ranges of the incident light spectrum in a stack of two or more solar cells with different bandgap energies. Recently, an efficiency of 24.1% for a perovskite/CIGSe tandem solar cell has been reported.[6] Here, a CdS-buffered CIGSe device was used as a bottom device with the deposition temperature of the perovskite device not exceeding 100°C. However, to broaden the choice of absorber materials that can potentially be used as top devices in such tandem stacks, the thermal stability of the bottom device is paramount for reliable application. Ideally, it will permit processing of the top device at the required optimum process temperature. For a chalcopyrite-based top device, this would have to exceed 400°C.[7]

The impact of thermal exposure on CIGSe solar cells under different environmental conditions was formerly investigated by several groups. Ramanathan et al. have demonstrated that heat treatments in air ("aging") at 250°C of CIGSe/CdS/i-ZnO junctions led to the formation of a wide bandgap secondary phase as seen in the corresponding external quantum efficiency (EQE).[8] Kijima and Nakada have conducted vacuum annealing for 30 min on CdS and ZnS(O,OH)-buffered CIGSe solar cells. They found that excess Cd and Zn diffuse into the CIGSe absorber layer leading to degradation of the device performance.[9] Similar observations were confirmed by other groups.[10–12] They have however not reported the effect of Na on the cell degradation. Besides this, Kazmerski et al. have observed Cu_2S formation at the CIGSe/CdS interface using X-ray photoelectron spectroscopy (XPS) analysis leading to 50–75% loss in photovoltaic cell performance.[10] Looking at potential-induced degradation (PID) of CIGSe solar cells and modules, it has been shown that also alkali elements play a crucial role in the deterioration of the investigated device performance.[13–16] In our study here, the CIGSe solar cell devices with and without Na incorporation are used to investigate decay mechanisms of those devices after thermal stress. Accordingly, a comprehensive model is presented, which describes the degradation mechanisms in place, and it will be seen that it is indeed Na that plays a key role in the observed, thermally induced degradation. For the sake of possible guidance, Figure 11 might be seen while reading Sections 3 and 5.

2 | EXPERIMENTAL PROCEDURES AND NUMERICAL SIMULATION

For device fabrication, an 800-nm-thick molybdenum layer is deposited by DC sputtering on top of $50 \times 50 \times 2\text{-mm}^3$-sized soda lime glass substrates as a back contact. Na-free samples contain a 150-nm-thick SiO_xN_y diffusion barrier that is deposited before the Mo back contact. The ~2.1-μm-thick CIGSe absorber layer is co-evaporated in a three-stage-like process at a maximum nominal substrate temperature of 530°C, showing a compositional in-depth Ga gradient and a final molar fraction ratio Cu/(Ga + In) (CGI) of 0.90. Details of the

adapted three-stage process can be found in Heinemann et al.[17] After washing the CIGSe absorber layer in 10% NH_3 (aq), a CdS buffer layer is applied by chemical bath deposition (CBD). On top of the CdS, a bilayer consisting of intrinsic ZnO (i-ZnO) and a doped ZnO:Al (AZO) with a total thickness of approximately 190 nm is sputter deposited at room temperature (RT) and at 150°C, respectively. Finally, using a shadow mask, Ni/Al/Ni contact grids are deposited by e-beam evaporation in order to facilitate current collection. It should be noted that one dedicated reference sample ("as-deposited") will be shown for each set of samples together with the respective results in order to be able to compare the obtained results, since the sets were deposited at different points in time. Particularly for the sets of samples used in Section 3.2, we term the respective reference devices as, for example, "as-deposited with Na for air annealing" or "as-deposited with Na for vacuum annealing."

Concerning the annealing procedures, the systems (a simple hot plate for air annealing and a heater in a vacuum chamber for vacuum annealing) are preheated to the desired annealing temperature. After the temperature has stabilized, the samples are exposed to the desired thermal stress. The temperature of the hot plate was measured with a temperature sensor showing a variation of $\Delta T = \pm 2°C$. With regard to the vacuum annealing, a $5 \times 5\text{-cm}^2$ sample holder is used to handle the samples inside the vacuum system. Temperature calibration in the vacuum system is achieved using temperature stickers. Nevertheless, a comparatively slow heat-up rate that is caused by the sample holder increasing the thermal mass and a possibly laterally inhomogeneous heat distribution must be taken into account. Therefore, the accuracy of the annealing temperature in vacuum is estimated to be in the range of $\Delta T = \pm 5°C$, even though nominally identical annealing procedures have been used.

The annealing procedures are applied either to complete devices or separately after individual layer deposition steps, as depicted in Figure 1. Hence, annealing in air or under vacuum is carried out after CIGSe (just before CdS deposition), CdS, i-ZnO, and AZO deposition. After annealing, unfinished devices are completed with the remaining layers. In the course of this study, the front contact layers might be seen as a main reason for the observed degradations. We therefore employed etching procedures to selectively remove the front contact layers and to rebuild them freshly for the purpose to reveal the effect of front contact layers on the observed degradation. To that end, some of the completed samples that had been annealed after CdS and AZO during preparation are separately etched (1) for 5 min in 10% citric acid in order to remove the ZnO bilayer or (2) for 2 min in 10% HCl or in 10% HCl and 10% KCN (complementary experiment) in order to remove the CdS and ZnO bilayer. Afterwards, respectively, either the ZnO bilayer or both the CdS and the ZnO bilayer are freshly redeposited. The KCN etch is performed in an experiment, which investigated the possible presence of $Cu_2(S,Se)$ phases at the absorber/buffer interface as indicated by the work of Bér et al.[18] Their presence can, however, be excluded here (see Figure S5). KCN etching did not further affect the properties of the device completed with the HCl-etched CIGS surface. Therefore, the KCN etch is not mentioned further below; it was however performed on all the samples from
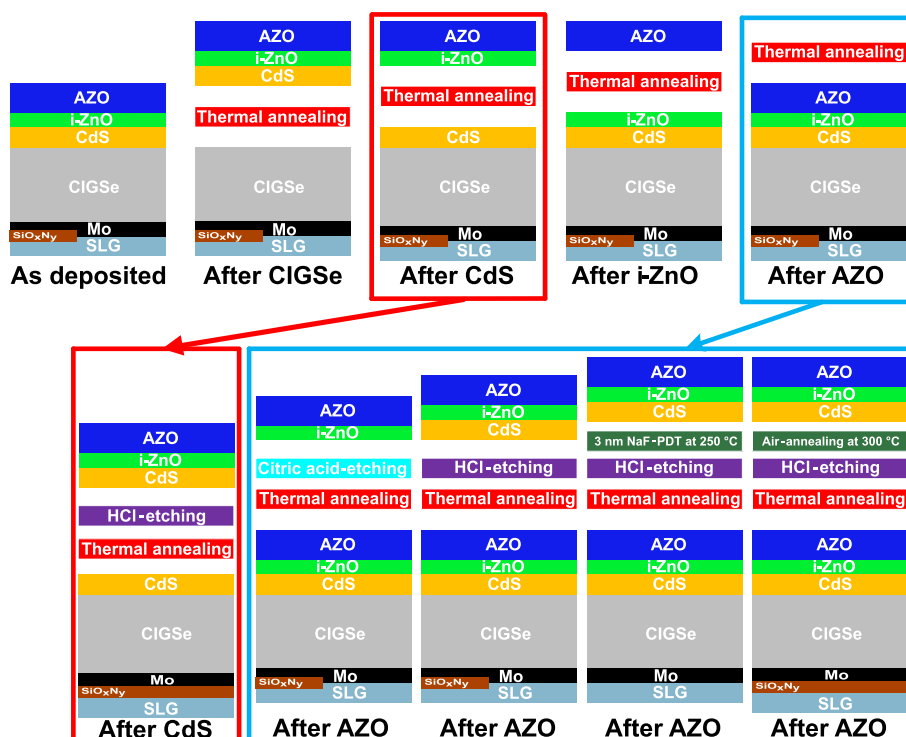
FIGURE 1 Schematic illustration of the sample processing—thermal annealing after each deposition step and etching with citric acid, HCl, or HCl + NaF PDT as well as HCl + AA. It should be noted that since there are two types of devices, that is, those with and those without Na, a glass substrate only covered in half by a SiO_xN_y barrier indicates that BOTH, devices with AND without barrier, have been processed. The colored frames refer to the etching procedures. For instance, the red frame indicates that a device without Na that is annealed directly after CdS deposition is etched with HCl and rebuilt. In this case, a complete SiO_xN_y barrier is indicated, because this is applied only to the device without Na

vacuum annealing experiments. An NaF PDT consisting of the evaporation of nominally 3-nm NaF at 250°C was implemented for Na-containing samples after HCl etching prior to the redeposition of CdS/i-ZnO/AZO. For one sample without Na, air annealing at 300°C for 20 min was performed on the HCl-etched sample as well. Note that all the samples were stored in N_2-filled desiccator before and after the deposition, annealing, and analysis. After the completion of the annealing treatments, the analysis of the samples was performed mostly in the first 6–8 weeks. However, it should be noted that the temperature-dependent current density–voltage measurement in some cases has been carried out after up to ~9 months. In this case, however, it was ensured that the current density–voltage measurements of these samples did not show any instability after the long storage time.

Current density–voltage (JV) measurements were conducted under standard test conditions (AM1.5, 1000 W m^{-2}, 25°C) using a WACOM A+ solar simulator. In this study, each sample contains at least seven, mostly 15 solar cells with a nominal area of 0.97 cm^2. Therefore, we use box plots to visualize the JV measurements, where 25% of the data above and below the median are located within the box. Temperature- and illumination-dependent current–voltage (JV–T) measurements were conducted under vacuum in order to avoid condensation of water on the sample in a liquid N_2-cooled cryostat (CryoVac) using a Keithley 2601A source measurement unit in 4-point contact configuration and a LED solar simulator (Oriel VeraSol) simulating an AM1.5 solar spectrum with a light intensity of 1000 W m^{-2}. The temperature ranges from 320 up to 90 K with a step size of 10 K. Measurements of the EQE with light bias at 0 voltage bias and the capacitance–voltage (CV) in dark were performed using in-house built setups. Elemental depth profiles are determined by glow discharge optical emission spectrometry (GD-OES) using a Spectruma GDA

650 tool.[19] For better comparison, the Na and Cd depth profiles are aligned at the respective Cd onset. Please note that the Na depth profiles are smoothed in order to ease viewability. Sheet resistance measurements are done by 4-point measurement on the AZO layers incorporated in the solar cell structure.

The 1D-Solar Cell Capacitance Simulator Software (SCAPS-1D 3.3.07) was used to simulate the obtained experimental results.[20] The bandgap energy (E_g), electron affinity (χ), and thickness of the CIGSe absorber are determined according to the Ga/(Ga + In) (GGI) ratio measured by GD-OES and integrated into the SCAPS simulation program using optical absorption parameters of experimentally deposited $CuInSe_2$ and $CuGaSe_2$ and further employing a corresponding interpolation algorithm within SCAPS based on Burgelman and Marlein.[21] The optical absorption parameters of the other layers, except for CdS, were experimentally determined. In order to implement parasitic absorption losses within the CdS layer and ensure that light absorption in the CdS layer does not contribute to photocurrent, we used neutral midgap defects in the CdS layer along with the embedded absorption model in SCAPS. Note that the carrier concentration extracted from the CV measurement is called as N_{CV}, whereas the corresponding input parameter for the simulation is referred to as N_A^{CIGSe}.

3 | EXPERIMENTAL RESULTS

3.1 | Determining typically harmful thermal stress conditions

As a starting point, we compared the JV measurements of complete solar cells with and without Na incorporation obtained before and

after thermal annealing in air for 20 min to be able to define an overall critical annealing temperature. Figure 2 displays box plots of the *JV* parameters, recorded on devices, which have been annealed at the given temperature. Clearly, the efficiency decreases with increasing annealing temperature. Even for relatively low temperatures ≤250°C, slight deteriorations in V_{OC} and *FF* yielding lower efficiencies for the devices with and without Na are evident. In the case of solar cells with Na incorporation, the losses in open-circuit voltage (V_{OC}), fill factor (*FF*), and efficiency (η) are more pronounced for temperatures >250°C. At the highest annealing temperature of 300°C for 20 min, the V_{OC} and *FF* decreased considerably resulting in an efficiency below 4%. In the case of the solar cells without Na incorporation, similar trends are observed, except for overall lower V_{OC} and *FF* values, which are due to the absence of Na in the CIGSe absorber. Again, solar cells degraded considerably after annealing at 300°C for 20 min.

Figure 3 shows illuminated (left) and dark (right) *JV* curves of complete solar cells with Na subjected to air annealing at 300°C with an annealing duration increasing from 30 s to 20 min. Within the first 2 min of annealing, very little changes in V_{OC} and *FF* can be seen. There are also no relevant changes in J_{SC}. From then on, V_{OC} and *FF* continue to decrease significantly, along with increasing current losses. In addition, the formation of a mixture of kink and rollover anomalies in the illuminated *JV* curves becomes apparent. The current densities measured in the dark are increasingly blocked with longer annealing duration. In the light of the results presented in Figures 2 and 3, the total heating flux that the device is exposed to seems more relevant than the annealing temperature, but only once the annealing temperature is higher than the critical threshold temperature. For the devices investigated in this study this threshold lies ∼250°C, as can be seen in Figure 2. Above the critical annealing temperature, the
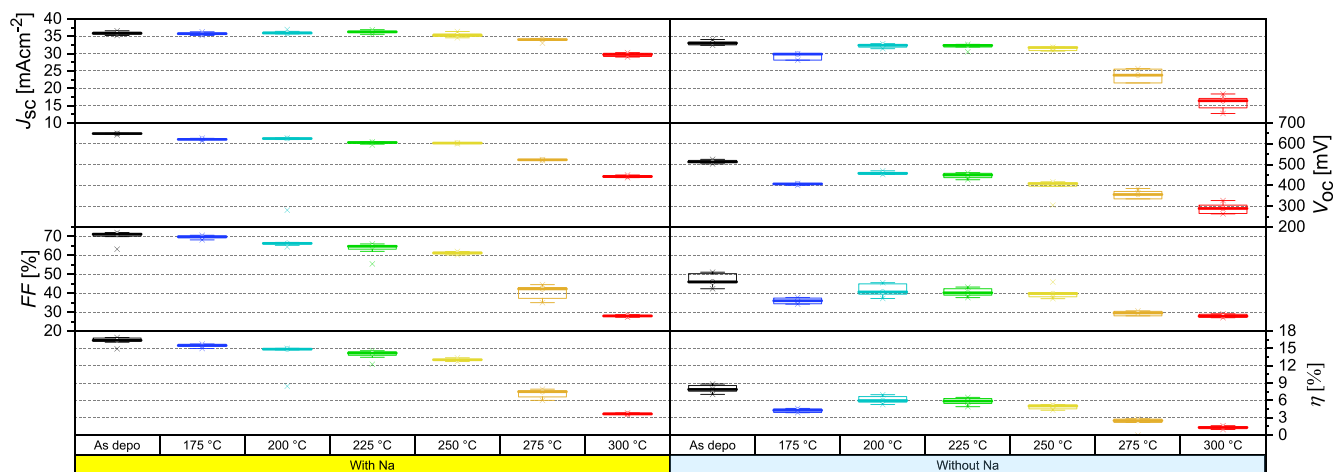

FIGURE 2 Results of *JV* measurements of solar cells with (left) and without (right) Na incorporation air annealed at up to 300°C for 20 min; a fresh device was used for each annealing temperature
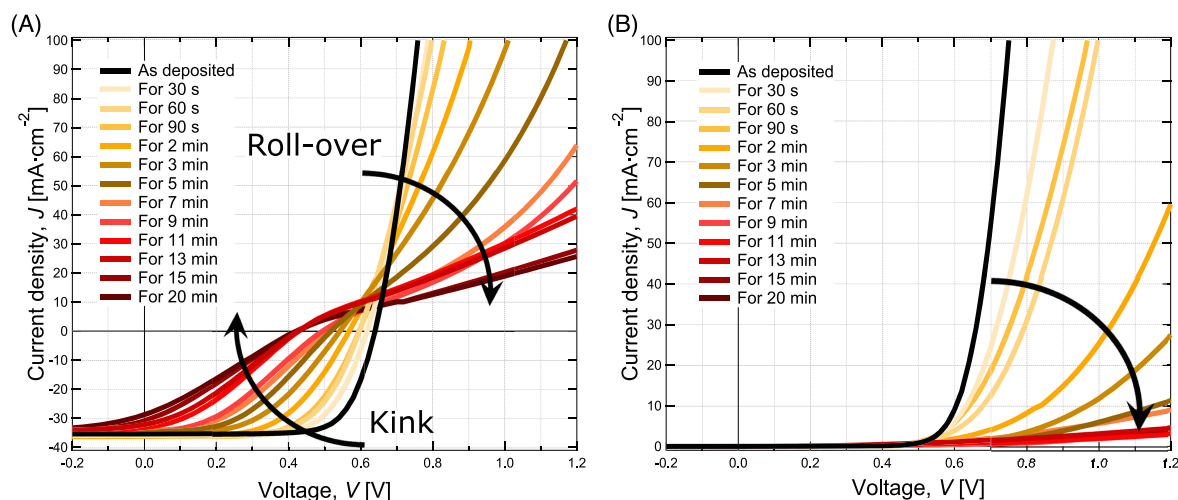

FIGURE 3 Illuminated (left) and dark (right) *JV* curves for the time-resolved annealed solar cells with Na incorporation at 300°C in air

degradation of the devices hinges on the total heating flux (see Figure 3). This observation is in line with the results shown by Flammini et al.[22] It is obvious that annealing at 300°C for 20 min is extremely damaging for the complete solar cells of both kinds. Therefore, for this study, these experimental stress conditions were chosen, to study and determine the causes why the various devices degrade under thermal stress.

3.2 | Comparing thermal stress in air and vacuum on CIGSe devices with and without Na incorporation

In order to identify the degradation mechanisms in the solar cells after exposure to thermal stress in more detail, we administered the annealing procedures as presented in Figure 1. Annealing at 300°C was carried out for 20 min in air or under vacuum after CIGSe (just before CdS deposition), CdS, i-ZnO, and AZO deposition individually. For better understanding, the samples are named as shown in Table 1. The corresponding JV results for each type of sample are shown in Figure 4.

Again the as-deposited samples with and without Na for air and vacuum annealing demonstrate different PV parameters, especially V_{OC} and FF. We attribute the variation in V_{OC} and FF, which is seen for nominally identical samples, to the general variability often seen in our CIGSe devices over longer time periods, due to slight variations in one of the deposited components. In case of solar cells with Na incorporation, air annealing after CIGSe (AA-CIGSe-wNa) results in slightly decreased V_{OC} and FF, whereas vacuum annealing (VA-CIGSe-wNa) only leads to a slight V_{OC} decrease. Air and vacuum annealing after CdS, i-ZnO, and AZO deposition show a similarly detrimental effect on V_{OC}. However, in addition, air annealing leads to a significantly enhanced decrease in FF, accompanied by a small drop of around 2 mA cm^{-2} in J_{SC}, all in all resulting in a strongly degraded solar cell performance. Vacuum annealing leads to less deterioration in FF and no observable change in J_{SC}.

Without Na present, air annealing of the CIGSe absorber layer (AA-CIGSe-w/oNa) facilitates an increased V_{OC} and FF compared to the as-deposited sample (AA-Asdepo-w/oNa). Apart from this, similar trends to the case with Na present can be observed in the deterioration of the JV parameters for air and vacuum annealing. As also seen in Figure 5a,c for the air-annealed devices with and without Na, a drop in J_{SC} when annealing after CdS, i-ZnO, and strongest after AZO is noted.

We conclude that the overall degradation behaviors are—in principle—independent of the annealing atmosphere, noting that this is not true when annealing bare as-deposited CIGSe absorber layers. Figure 5a–d displays the JV curves of the air- and vacuum-annealed solar cells with and without Na that showed the best efficiencies each. The air-annealed samples after CdS, i-ZnO, and AZO exhibit strong rollover and kink anomalies, especially in the case of devices with Na incorporation. On the other hand, only slight rollover behavior can be seen in case of vacuum-annealed samples after CdS and i-ZnO. Further, EQE data are given in Figure 5e–h. There are no relevant changes in the EQE when annealing after CIGSe in any case. Once CdS has been deposited prior to air or vacuum annealing of the devices both with and without Na incorporation, the EQE decreases in the blue portion of the spectrum, with stronger deterioration visible when annealing samples without Na and more so when annealing after i-ZnO deposition (AA-i-ZnO-w/oNa). Annealing after AZO (AA-AZO-wNa and AA-AZO-w/oNa) only shows a detrimental effect on the EQE when done in air, independent of the Na content. In particular, sample AA-AZO-wNa exhibits a pathological behavior by giving an $EQE > 1$ at around 400 nm. We attribute this to a light-sensitive behavior in the window and absorber layers, which causes an

TABLE 1 List of the individual sample investigated in this study

	Air annealing		Vacuum annealing	
	With Na	**Without Na**	**With Na**	**Without Na**
As-deposited	AA-Asdepo-wNa	AA-Asdepo-w/oNa	VA-Asdepo-wNa	VA-Asdepo-w/oNa
Annealed after				
CIGSe	AA-CIGSe-wNa	AA-CIGSe-w/oNa	VA-CIGSe-wNa	VA-CIGSe-w/oNa
CdS	AA-CdS-wNa	AA-CdS-w/oNa	VA-CdS-wNa	VA-CdS-w/oNa
CdS, then HCl etched	—	AA-CdS-HCl-w/oNa	—	—
i-ZnO	AA-i-ZnO-wNa	AA-i-ZnO-w/oNa	VA-i-ZnO-wNa	VA-i-ZnO-w/oNa
AZO	AA-AZO-wNa	AA-AZO-w/oNa	VA-AZO-wNa	VA-AZO-w/oNa
AZO, then citric acid etched	AA-AZO-citric-wNa	—	VA-AZO-citric-wNa	VA-AZO-citric-w/oNa
AZO, then HCl etched	AA-AZO-HCl-wNa	—	VA-AZO-HCl-wNa	VA-AZO-HCl-w/oNa
AZO, then HCl + NaF PDT	AA-AZO-HCl-NaF-wNa	—	VA-AZO-HCl-wNa	—
AZO, then HCl + air annealing	—	—	—	VA-AZO-HCl-AA-w/oNa

Note: It should be noted that there are four different types of experiments: (1) air annealing (AA) with Na (wNa), (2) air annealing (AA) without Na (w/oNa), (3) vacuum annealing (VA) with Na (wNa), and (4) vacuum annealing (VA) without Na (w/oNa). For each annealing experiment, there is one reference sample named here "as-deposited." Accordingly, as-deposited references are identified by, for example, AA-Asdepo-wNa and VA-Asdepo-wNa. The remaining of the experiment details are indicated between the prefix "AA or VA" and suffix "wNa or w/oNa."
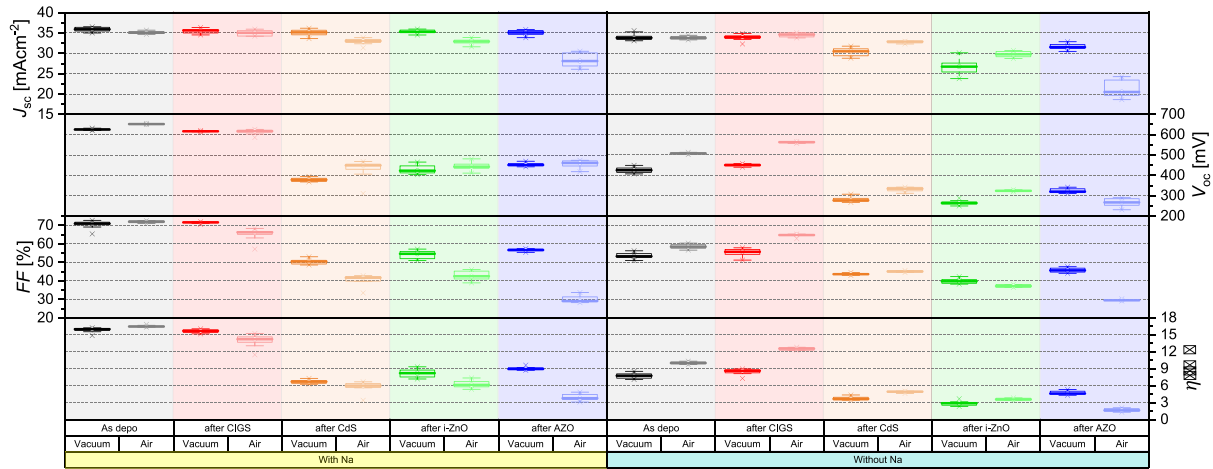
FIGURE 4 Effect of air and vacuum annealing on the *JV* parameters of solar cells with (left) and without (right) Na incorporation. Please note that in total, there are four different as-deposited samples (one for each set of air- and vacuum-annealed samples with and without Na, since the sets were processed at different times)
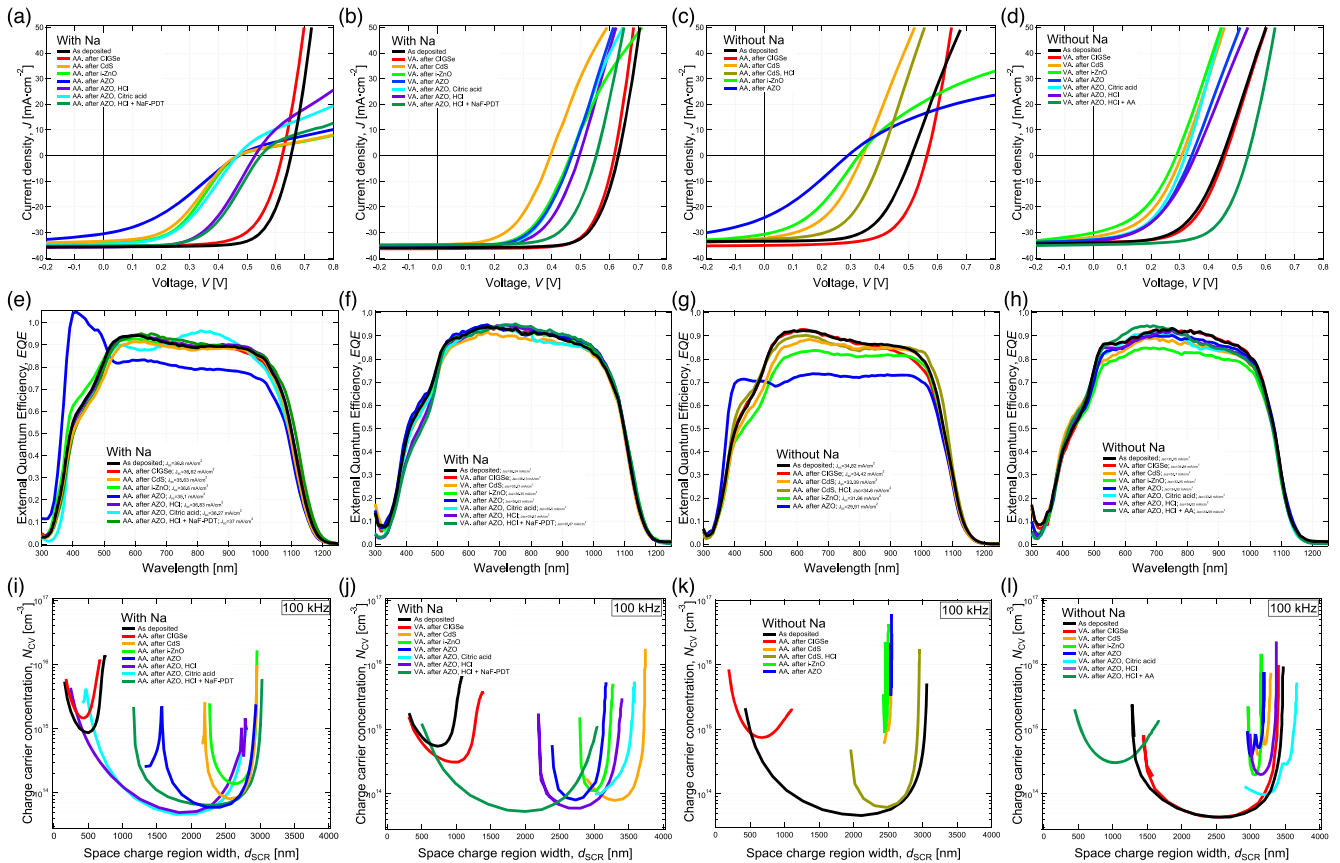
FIGURE 5 *JV* (a–d), *EQE* (e–h), and N_{CV} (i–l) of the best solar cells with and without Na incorporation exposed to air annealing (AA) and vacuum annealing (VA) after each layer deposition at 300°C for 20 min

additional flow of injected charge carriers towards the front contact during *EQE* measurement similar to an apparent quantum efficiency as suggested by Scheer and Schock[23] or photoconductivity effects as described by Phillips and Roy.[24]

Figure 5i–l provides information about the charge carrier distributions within the absorber after the various treatments. Air annealing of the bare CIGSe absorbers with and without Na (AA-CIGSe-wNa and AA-CIGSe-w/oNa) brings about an increase in N_{CV} , more

pronounced for the sample without Na. Vacuum annealing either leads to a slight decrease in N_{CV} in the case with Na (VA-CIGSe-wNa sample) or does not affect the N_{CV} for the sample without Na (VA-CIGSe-w/oNa sample). However, the annealing procedures applied after CdS, i-ZnO, and AZO regardless of the environment have striking repercussions on the N_{CV} profiles for both cases with and without Na. The common observation for all of these samples is a shift of their N_{CV} profiles to larger d_{SCR}. While the samples with Na demonstrate decreased N_{CV}, the samples without Na exhibit even increased N_{CV} along with the entire shift of their N_{CV} profiles. These observations therefore stress that although the annealing atmosphere did hardly alter the trend observed in the PV parameters (see Figure 4), it does crucially affect the manifestation of the degradation mechanisms in place. To reveal the underlying degradation mechanisms individually, further electrical characterization of all devices and elemental in-depth profiles measured on the as-deposited and annealed devices will be analyzed below.

Table 2 shows the correlation between V_{OC} and N_{CV} as determined by CV for the best devices as observed when annealing after the various processing steps. The absorber layers for each set of samples (with and without Na for air and vacuum annealing) are deposited in separate, nominally equal co-evaporation processes. Na supply is varied simply by the use of substrates with and without Na diffusion barrier. The as-deposited samples with Na generally show higher V_{OC}, which is attributed to the presence of Na during CIGSe deposition. In Table 2, the section ΔV_{OC} compares experimentally observed values with those derived from the relation

$$\Delta V_{OC}^{CV} \approx \frac{k_B T}{q} \ln \frac{N_{CV}}{N_{CV}^*}, \tag{1}$$

with k_B denoting the Boltzmann constant, temperature T, the elemental charge q, and the charge carrier concentration N_{CV}^* of the reference device.[23] It should be noted that this relation is only true, if the dominant recombination pathway is in the absorber bulk. Hence, values for ΔV_{OC}^{CV} are only shown for those devices, for which—as will be indicated below via $JV-T$ analysis—the main recombination pathway is assumed within the absorber bulk. All other values for devices that—according to the $JV-T$ analysis—exhibit the main recombination taken place at the interface are not calculated (denoted as not applicable [n.a.]). The value shown for ΔV_{OC}^{JV} for the as-deposited reference device for vacuum-annealed set demonstrates that the observed differences in V_{OC} can be explained by the difference in N_{CV} when Na is present. Without Na present during growth, this is not the case.

TABLE 2 V_{OC}, N_{CV}, ΔV_{OC}, and R_{Sheet} values of the best solar cells with and without Na before and after annealing at 300°C for 20 min

| | Na | As-deposited | Annealed in | Annealed after | | | | Annealed after AZO, then etched and rebuilt | | |
				CIGSe	CdS	i-ZnO	AZO	Citric acid	HCl	HCl + NaF PDT
V_{OC}(mV)	Yes	652	Air	626	468	481	471	467	528	548
	Yes	632	Vacuum	616	395	465	469	467	495	554
	No	511	Air	564	342	328	290	—	407[a]	—
	No	449	Vacuum	458	307	288	342	320	354	537 (AA)
N_{CV} ($\times 10^{13}$ cm^{-3})	Yes	110	Air	160	4.5	4.1	7.8	4.6	5.0	6.5
	Yes	55	Vacuum	31	7.9	11.3	8	9.9	6.0	5.4
	No	5.4	Air	74	90	100	340	—	6.2[a]	—
	No	4.3	Vacuum	4.3	39.6	19.7	37.9	9.8	19.9	30.5 (AA)
ΔV_{OC}^{JV} / ΔV_{OC}^{CV}	Yes	0/0	Air	−26/+10	−184/n.a.	−171/n.a.	−181/n.a.	−4/n.a.	+57/n.a.	+77/n.a.
(mV)	Yes	−20/−18	Vacuum	−36/−33	−257/n.a.	−187/n.a.	−183/n.a.	−2/n.a.	+26/n.a.	+85/n.a.
	No	−141/n.a.	Air	−88/−10	−310/n.a.	−324/n.a.	−362/n.a.	—	+65/n.a.[a]	—
	No	−203/n.a.	Vacuum	−194/n.a.	−345/n.a.	−364/n.a.	−310/n.a.	−22/n.a.	+12/n.a.	+95/n.a. (AA)
R_{Sheet} ($\Omega/\square$)	Yes	94	Air	107	94	85	959	107	115	101
	Yes	65	Vacuum	64	74	73	113	76	76	66
	No	95	Air	87	78	80	420	—	95[a]	—
	No	61	Vacuum	60	71	68	91	70	71	70 (AA)

Note: ΔV_{OC}: for comparability, the values for the "as-deposited and annealed after" devices refer to the "as-deposited" device in the "air-annealed" sample set with Na, and the values in the section "etched and rebuilt" refer to the "annealed after AZO" in their individual sample set; AA notifies "air annealing." The "from JV" values are calculated using $\Delta V_{OC}^{JV} = V_{OC}^* - V_{OC}$, while the "from N_{CV}" values, ΔV_{OC}^{CV}, are calculated according to Equation (1). AA: after etching, this sample was only air annealed at 300°C for 20 min as alternative to a NaF PDT.

[a]This sample has been air annealed after CdS deposition. After annealing, it was etched with HCl and rebuilt with the respective layers.

Only part of ΔV_{OC}^{JV} can be attributed to a doping effect of the CIGSe absorber.

The JV–T measurements that were performed on the various devices with and without Na are shown in Figure 6a–d. From this measurement, the difference at the linear extrapolation of V_{OC} to 0 K from high T (gives activation energy [E_a]) and from low T (V_{OC} saturation) can be interpreted as barrier height at the back contact.[25] Samples grown on substrates with and without Na differ in the determined values for the E_a and the back-contact barrier height (Φ_{BC}). The AA-Asdepo-wNa and VA-Asdepo-wNa samples show a good agreement of E_a and the bandgap energy extracted from EQE measurement (E_g^{EQE}), while a Φ_{BC} of about 0.14 eV initially appears for these samples. On the other hand, the AA-Asdepo-w/oNa and VA-Asdepo-w/oNa samples indicate $E_a < E_g$ along with a higher Φ_{BC} of about 0.20 eV. Interestingly, air annealing of the sample without Na after CIGSe (AA-CIGSe-w/oNa) raises the E_a to a value that is

equal to its E_g^{EQE}. Apart from this, any annealing after CdS deposition leads to severe decrease in E_a smaller than E_g^{EQE}. Furthermore, both air annealing and vacuum annealing also increase Φ_{BC} of the Na-containing sample to the level of the back barrier height in the samples without Na. In contrast to these findings, however, the latter is not significantly altered by annealing of the samples in any atmosphere.

Table 2 also lists values for the sheet resistance R_{sheet} of the TCO front contact as measured on the as-deposited and annealed devices. Due to maintenance that was performed on the TCO deposition tool during the experiments of this work, there is some variability in the values for the various sets of samples that is well reproduced on glass references. Due to the roughness of the surface of the CIGSe compared to the glass surface, the TCO resistance measured on the devices front contact is slightly higher than the reference values on glass. The one notable effect of the annealing steps on R_{sheet} is a clear

(a)

	As-depo	AA CIGSe	AA AZO	Air-annealed after AZO		
				Citric	HCl	HCl+NaF
E_g^{EQE}	1.11 eV (± 0.01)	1.09 eV (± 0.01)	1.11 eV (± 0.01)	1.09 eV (± 0.01)	1.10 eV (± 0.01)	1.09 eV (± 0.01)
E_a	1.11 eV (± 0.02)	1.09 eV (± 0.02)	0.78 eV (± 0.01)	0.78 eV (± 0.01)	0.84 eV (± 0.01)	0.85 eV (± 0.02)
Φ_{BC}	0.14 eV (± 0.02)	0.21 eV (± 0.02)	0.18 eV (± 0.02)	0.19 eV (± 0.02)	0.14 eV (± 0.02)	0.13 eV (± 0.03)

(b)

	As-depo	VA AZO	VA. after AZO	
			Citric	HCl+NaF
E_g^{EQE}	1.11 eV (± 0.01)	1.11 eV (± 0.01)	1.10 eV (± 0.01)	1.11 eV (± 0.01)
E_a	1.11 eV (± 0.01)	0.84 eV (± 0.03)	0.81 eV (± 0.01)	0.95 eV (± 0.01)
Φ_{BC}	0.14 eV (± 0.02)	0.20 eV (± 0.04)	0.17 eV (± 0.01)	0.19 eV (± 0.01)

(c)

	As-depo	AA CIGSe	AA CdS	AA AZO
E_g^{EQE}	1.12 eV (± 0.01)	1.13 eV (± 0.01)	1.13 eV (± 0.01)	1.13 eV (± 0.01)
E_a	0.86 eV (± 0.02)	1.13 eV (± 0.02)	0.72 eV (± 0.01)	0.58 eV (± 0.01)
Φ_{BC}	0.20 eV (± 0.02)	0.17 eV (± 0.02)	0.19 eV (± 0.01)	0.21 eV (± 0.01)

(d)

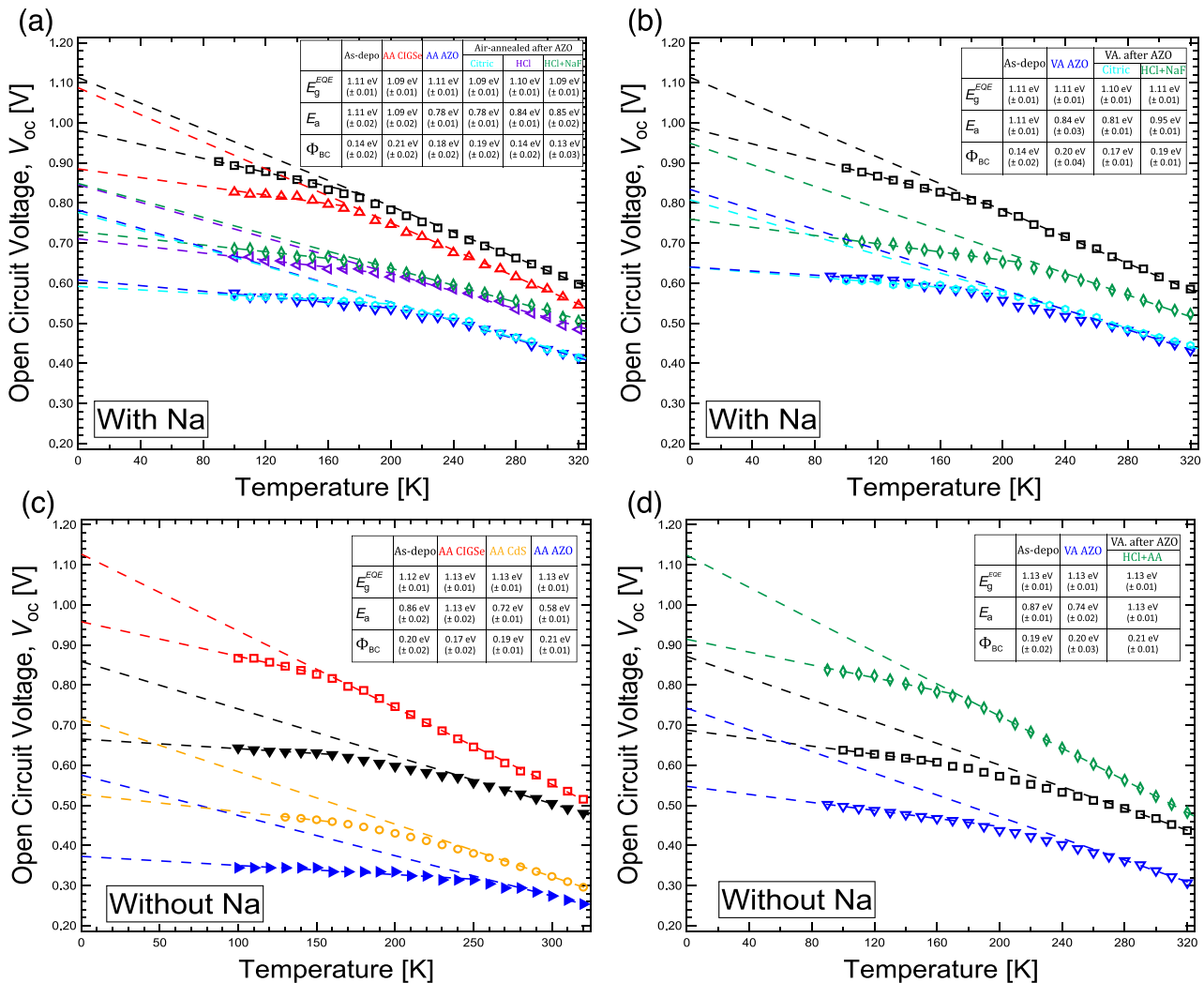|	As-depo	VA AZO	VA. after AZO
			HCl+AA
E_g^{EQE}	1.13 eV (± 0.01)	1.13 eV (± 0.01)	1.13 eV (± 0.01)
E_a	0.87 eV (± 0.01)	0.74 eV (± 0.02)	1.13 eV (± 0.01)
Φ_{BC}	0.19 eV (± 0.02)	0.20 eV (± 0.03)	0.21 eV (± 0.01)

FIGURE 6 The $V_{OC}(T)$ characteristics under one sun illumination at temperatures from 90 to 320 K for the respective CIGSe solar cells with and without Na. Each set of sample is separately shown for with Na in (a), for vacuum annealing with Na in (b), for air annealing without Na in (c), and for vacuum annealing without Na in (d). It should be noted that the table shown in each graph includes the bandgap energy extracted from EQE measurement air annealing (E_g^{EQE}), activation energy (E_a), and resulting back-contact barrier height (Φ_{BC})

increase when the complete device is annealed in air (AA-AZO-wNa and AA-AZO-w/oNa), while there is only a slight increase in R_{sheet} after vacuum annealing.

Finally, Figure 7 shows the Cd and Na depth profiles (for ease of comparison aligned at the point of Cd onset in all devices) of the air- and vacuum-annealed solar cells with and without Na as measured by GD-OES. The as-deposited Na profiles in Figure 7b,d display an accumulation of Na mainly at the Mo/CIGSe and less so at the CIGSe/CdS interface. The VA-Asdepo-wNa sample—even though nominally identical to sample AA-Asdepo-wNa—exhibits a lower Na content at both interfaces and in the entire absorber layer compared to the AA-Asdepo-wNa sample. The lower Na content of the VA-Asdepo-wNa might substantiate the lower V_{OC}. The main effect of air annealing after CIGSe on Na is a flattening of the Na depth profile towards the back contact (see Figure 7b), while the vacuum annealing after CIGSe only gives rise to a rather slight decrease of the Na signal in the absorber layer. Annealing after CdS, i-ZnO, and AZO leads to significant changes in the Na depth profiles of all Na-containing samples. Na
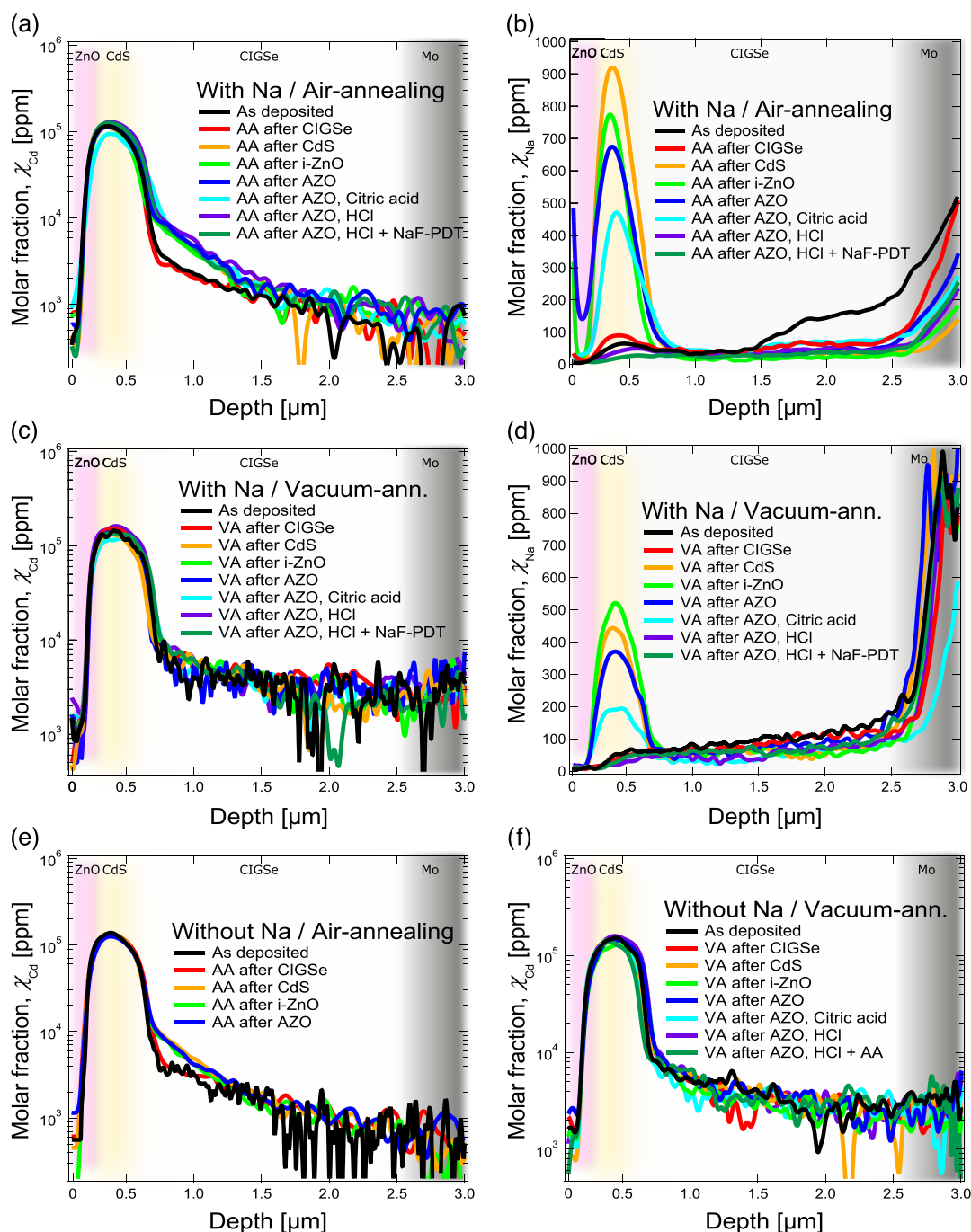

FIGURE 7 GD-OES Cd depth profiles of the solar cells with (a, c) and without (e, f) Na as well as the Na depth profiles of the solar cells with Na (b, d) annealed in air and under vacuum at 300°C for 20 min

diffuses into the CdS and ZnO bilayer and with air annealing after AZO also towards the surface of the AZO layer (see Figure 7b). On the other hand, vacuum annealing only provokes Na out-diffusion into the CdS layer, not into the ZnO bilayer as seen in Figure 7d. Additionally, air annealing after CdS, i-ZnO, and AZO leads to significant Cd diffusion into the CIGSe absorber with and without Na up to a depth of 200–400 nm (see Figure 7a,e). In contrast, Cd diffusion into the CIGSe can hardly be seen after vacuum annealing in either case (see Figure 7c,f).

3.3 | Partial mitigation of annealing damage

In order to test a possible way to mitigate damage and for closer investigation of the effects of thermal stress on the window layers, those samples that were annealed after AZO were etched by HCl (as indicated in Table 2) to completely remove all layers from the CIGSe absorber or alternatively by citric acid in order to selectively remove the ZnO bilayer only (see also Figure 1). In addition to the HCl etch, a NaF PDT was carried out for both the air- and vacuum-annealed Na-containing samples, and an air-annealing step at 300°C for 20 min for the Na-free sample directly after the etching process instead of the NaF PDT.

The corresponding JV curves are displayed in Figure 5a–d. As it was described above, the JV curves of the air-annealed solar cells exhibit a mixture of strong rollover and kink anomalies (see Section 4 for more details). After etching of the window layers and rebuilding them, these anomalies are partially recovered. Also, etching and redeposition of the TCO restore R_{sheet} to values in the range of the original values seen in Table 2. In particular, the following effects occur: (1) removing only the TCO (not the CdS) of the Na-containing sample (AA-AZO-citric-wNa) gives rise to a partial recovery of the current loss, while the V_{OC} is hardly affected. For the corresponding vacuum-annealed samples (VA-AZO-citric-wNa and VA-AZO-citric-w/oNa), the citric acid etch shows no recovery effect. (2) HCl etching and rebuilding the air-annealed solar cells with Na (AA-AZO-HCl-wNa) with new CdS and TCO leads to a disappearance of the kink anomaly along with the complete recovery of the J_{SC} loss, while the rollover is hardly affected. Additionally, removal and rebuilding of the complete window layer improves the V_{OC} of the device by more than 60 mV compared to the AA-AZO-wNa sample. A similar observation is made for the sample that was vacuum annealed after AZO, then HCl etched (VA-AZO-HCl-wNa) and rebuilt. Without Na, sample AA-CdS-HCl-w/oNa, which was air annealed after CdS, then HCl etched and rebuilt also shows a partial improvement in V_{OC} by 65 mV, while the sample that was vacuum annealed after AZO, then HCl etched and rebuilt (VA-AZO-HCl-w/oNa) only shows a rather weak gain in V_{OC}. (3) When the HCl-etched air-annealed sample, AA-AZO-HCl-NaF-wNa, is exposed to NaF PDT prior to CdS redeposition, an additional increase in V_{OC} is notable in conjunction with a remaining strongly pronounced rollover. (4) Exposing the HCl-etched, vacuum-annealed sample to a NaF PDT (VA-AZO-HCl-NaF-wNa) improves its V_{OC} by more than 80 mV and reduces the slight rollover behavior

present before etching. (5) A general observation concerning the $JV–T$ results from Figure 6a–d is that an HCl etch and NaF PDT raise E_a, while citric acid etch does not further change the corresponding E_a. (6) The air-annealing treatment for the sample without Na that was vacuum annealed after AZO (VA-AZO-HCl-AA-w/oNa) instead of the NaF PDT leads to an increase in V_{OC} by almost 200 mV along with a remarkable increase in N_{CV} and fully alleviates the slight rollover behavior seen in the JV characteristic of its as-deposited reference (VA-Asdepo-w/oNa). With respect to the $JV–T$-result in Figure 6d, it strikingly brings the E_a to the same level of E_g^{EQE}.

In summary, this indicates that there is a loss in J_{SC} that can be mitigated when "rebuilding" the AZO after air annealing. An almost complete recovery of the J_{SC} loss can only be realized when the CdS layer is etched off together with the TCO and rebuilt. The annealing-induced V_{OC} loss can also be partially recovered by rebuilding the n side of the junction. However, a large part of the total V_{OC} loss remains in the CIGSe absorber, even though the rebuilding of the CIGSe/CdS improves the V_{OC}. This again coincides with the observed evident diffusion of Na through the window layers during annealing, if present.

4 | PRINCIPLE SCAPS-1D MODELS FOR POSSIBLE DEGRADATION

To establish an understanding for the degradation mechanisms that may be caused by exposure of the CIGSe solar cell to thermal stress, some principle models for experimentally observed degradation mechanisms including compositional changes near the interfaces are introduced. First, a basic model of the as-deposited CIGSe devices, which reproduces the JV and CV measurements is presented using SCAPS-1D.[20]

The device properties that are utilized for the basic model for an as-deposited, Na-containing device are listed in the first section of Table S1 and are based on Gloeckler et al.[26] In Figure 8, the measured and simulated JV, CV, and EQE curves as well as the corresponding energy band diagram of the as-deposited CIGSe solar cell with Na (AA-Asdepo-wNa) are displayed. The conduction band offset between CIGSe and CdS as well as CdS and ZnO are assumed to be $\Delta E_C^{CIGSe/CdS} = 0.1$ eV (Spike) and $\Delta E_C^{CdS/ZnO} = -0.2$ eV (cliff), respectively, as proposed by Sozzi et al.[27] The minority carrier lifetime is set to $\tau_e = 23$ ns with bulk recombination via neutral defects placed at 0.6 eV above the valence band maximum (VBM). Note that this neutral defect level is used to represent the overall bulk recombination in the devices. The real distribution of the bulk defects is known to be more complicated.[28] An acceptor defect is placed at the CIGSe/CdS interface at 0.47 eV above the VBM of CIGSe absorber. This is motivated by the exposure of samples after CIGSe deposition to air and daylight prior to the CdS processing step[29] and enables the simultaneous simulations of the JV and CV characteristics, which under absence of these defects could not be achieved. In our model, they show rather weak influence on the corresponding JV results revealing that the largely dominant recombination mechanism
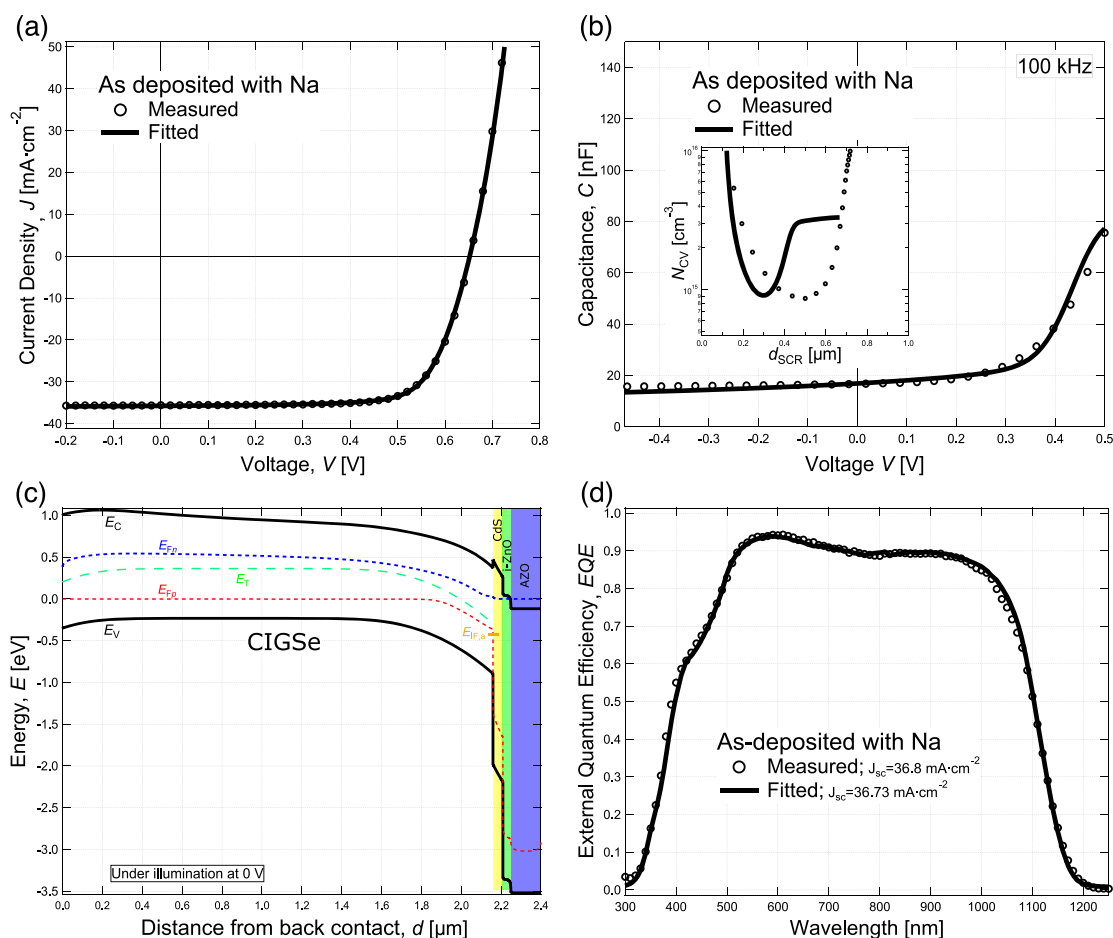
FIGURE 8 The measured (a) *JV* and (b) *CV* curves of the as-deposited CIGSe solar cell with Na for air annealing (AA-Asdepo-wNa) shown in Section 3.2 (open circles) and the corresponding simulated *JV* and *CV* curves (solid line). (c) Corresponding simulated energy band diagram of the device under illumination at 0 V including the energy defect levels in the absorber bulk and at the CIGSe/CdS interface. (d) The measured and fitted *EQE* curves of the as-deposited CIGSe solar cell with Na incorporation

is present within the absorber, not at the interfaces (see Figure S1a), depending on the chosen energetic position and defect density. Moreover, based on the *JV–T* measurement (see Figure 6a), a back-contact barrier with a height of 140 meV is added to the basic model.

Characteristic phenomena that are observed in the experimental *JV* curves (Figure 5) are mostly the kink (I) and rollover (II) anomalies. In the literature, these anomalies are often connected with experimental findings, which will be shortly reviewed here. With this, numerical models will be tailored to fit the experimental findings observed after the CIGSe solar cells have been exposed to thermal stress.

4.1 | Kink anomaly

The kink anomaly is generally due to a charge carrier extraction barrier for the photocurrent resulting in a voltage-dependent photocurrent collection.[23] Possible causes for this anomaly are formation of a thin p^+ layer in the near CIGSe absorber surface close to the CdS buffer,[23] a highly positive conduction band offset (spike)

at the CIGSe/CdS interface,[23] or deep acceptor trap states in the CdS layer.[30,31] Here, for our devices that are exposed to thermal annealing, as based on the *JV–T* measurement results, an increased spike formation seems unlikely.

4.2 | Rollover anomaly

The rollover anomaly is described to be a current saturation in the first quadrant of the *JV* curve, that is, under forward bias, revealing a charge carrier injection barrier.[23,32] The first possible cause for that behavior is the presence of a back-contact barrier representing a hole injection barrier at the CIGSe/Mo interface.[23,32–38] Another possible cause is acceptor states at the CdS/ZnO front interface.[23] However, it should be noted that these types of defects at the CdS/ZnO interface can also induce a kink anomaly resulting in lower photocurrent under forward bias and *FF* as suggested by Nguyen et al. and Urbaniak and Igalson.[39,40] In addition to these, Villanueva-Tovar et al. have proposed that a strong cliff at the CdS/ZnO interface can also cause an injection barrier leading to a rollover anomaly.[41]

Regarding the integration of the experimentally observed findings from Section 3.2 into the device simulation, these can be related to the following possible effects:

- Back contact barrier: the presence of Na during CIGSe absorber deposition is crucial to catalyze $MoSe_2$ formation creating an ohmic contact between the Mo and the CIGSe layer.[42,43] The experimentally observed flattening of the Na depth profiles after all annealing procedures could be a sign for an increased back-contact barrier. Therefore, in the case of Na-free solar cells, a higher back-contact barrier is initially assumed. Figure 6a–d reveals the back-contact barrier height for the corresponding devices.

- Acceptor states in the CdS and at the CdS/i-ZnO interface: annealing after CdS, i-ZnO, and AZO leads to Na diffusion especially into the CdS and the ZnO, as seen in Figure 7b,d. Na atoms are known to create deep acceptor states in CdS and ZnO at an energy of around 0.3 eV above the VBM of each layer.[44–46] Since Na accumulation in the vicinity of the CIGSe absorber surface is not detected, the formation of a p^+ layer can be excluded. Furthermore, a high positive conduction band offset (increased spike formation) at CIGSe/CdS can be excluded for the devices annealed after CdS, i-ZnO, and AZO as based on the JV–T measurement results (see Figure 6). Accordingly, such deep acceptor states are included into the SCAPS model and used to fit the Na-containing devices. If no Na is present in the solar cells, no acceptor trap states are implemented in the corresponding simulations.

- n-type surface: another experimental observation is strong Cd diffusion into the CIGSe absorber layer after air annealing. This can modify the absorber material close to the junction from p type to n type via the formation of Cd_{Cu} defects.[12,47–50] As it was seen in Figure 7a, air annealing-induced Cd diffusion into CIGSe cannot be removed by HCl etching. Therefore, in all cases that the samples were annealed together with CdS layer on top of CIGSe, the effect of the Cd diffusion as an n-type surface layer without changing the whole absorber bandgap grading is used.

- Negative band offset at the CIGSe/CdS interface (cliff formation): based on JV–T measurements (see Figure 6a–d), a cliff-like energy band alignment at the CIGSe/CdS interface is assumed when annealing devices with CdS layer present on top of the CIGSe absorber, since the conditions $E_a < E_g^{EQE}$ are interpreted as dominant recombination to occur at the interface. This is considered true also after etching since—as mentioned above—once it has taken place, Cd diffusion is permanent and the CIGSe absorber layers are Na poor. For simulation, the magnitude of the cliff-like band alignment at CIGSe/CdS is adjusted by changing the electron affinity of the CdS layer.

Figure 9 exemplarily displays how the above mentioned possible degradation mechanisms individually influence the simulated JV and EQE curves of the basic device model. The corresponding simulated energy band diagrams are shown as well. If a back-contact barrier of $\Phi_{BC} = 0.4$ eV is present at the CIGSe/Mo interface while keeping carrier concentration of the CIGSe (N_A^{CIGSe}) constant in the simulation, a rollover anomaly forms (see Figure 9a,b). However, this manifestation of the back-contact barrier depends strongly on the carrier concentration in the absorber layer: for example, decreasing the N_A^{CIGSe} in the example gives rise to an increased V_{OC} loss rather than a rollover due to increased back-contact recombination. This can be clearly seen in the related band diagram as well.

The effect of acceptor states in the CdS layer is shown in Figure 9c,d indicating the formation of a kink anomaly. It is apparent that this leads to reduced FF and J_{SC}. With increasing acceptor defect density, the severity of the kink anomaly becomes more visible, since the extraction barrier for generated electrons is more pronounced due to the compensation of the n-type conductivity within CdS layer by acceptor states accounting for a reduced FF. Furthermore, the slight drop in J_{SC} most likely arises from the reduced d_{SCR} as shown in the respective energy band diagram in Figure 9d. Even though acceptor states at the CdS/i-ZnO interface show virtually the same effect, even more pronounced, they additionally lead to the formation of an injection barrier and therefore of a rollover (see Figure 9e,f). This behavior is rather similar to the case of above mentioned possible cause of strong cliff at CdS/ZnO interface for a rollover, as proposed by Villanueva-Tovar et al.[41]

Finally, in Figure 9g,h, the effect of an n-type layer at the CIGSe surface is shown. Since it is mainly affecting the J_{SC}, we show the simulated EQE curves instead of the JV curves. A 50-nm-thick n-type layer decreases the EQE in the short wavelength region depending highly on the magnitude of the n-type doping (N_D^{n-type}), thereby reducing J_{SC}. Regarding the impact of increasing the thickness of n-type layer at constant N_D^{n-type}, the decrease in EQE is further amplified, while V_{OC} is slightly increased due to decreased interface recombination. Consequently, such an n-type layer at the CIGSe surface can lead to poor blue response seen in EQE curves.

If no Na is present during growth, the basic device model, as introduced above, has to be adjusted to be able to represent the measured JV and CV characteristics. As seen from Table 2, in Na-free devices, N_{CV} is lower, and—as was argued above—a higher back-contact barrier needs to be introduced. Further, JV–T measurements imply that a cliff-like band alignment is present at the CIGSe/CdS interface. It should also be noted that due to the fact that Na decreases the In–Ga interdiffusion during CIGSe growth, Na-free devices are expected to exhibit a slightly larger minimum bandgap E_g when compared to Na-containing devices as also suggested by Caballero et al.[51] In our numerical simulation routine, this, however, is of no concern, as for each device the experimentally measured in-depth Ga gradient is used. Finally, in order to be able to fit the measured data, the minority carrier lifetime of the AA-Asdepo-w/oNa sample has to be decreased from 23 ns in the basic model with Na to 12 ns when no Na is present to account for an additional V_{OC} and FF loss, as proposed by Zakay et al.[52] This is done by increasing the capture cross section of the neutral defects in the absorber layer. It should also be noted that within this work, a "good" or "bad" quality of the absorber layer, as judged by the minority carrier lifetime in the bulk, is tuned by
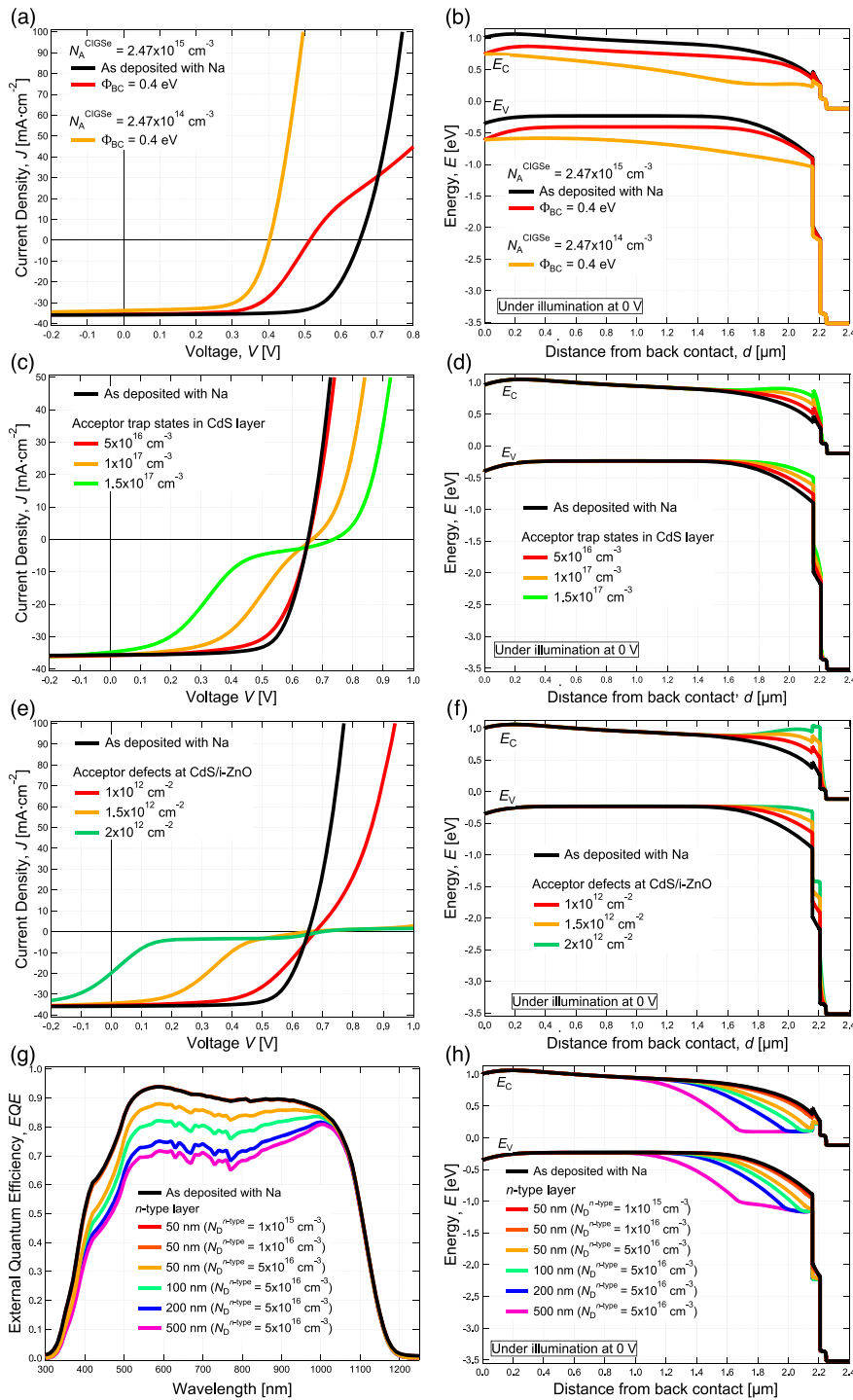
FIGURE 9 The effects of the various principle causes individually applied to the basic device model with Na present as simulated in SCAPS-1D. The effect of integration of (a, b) the back-contact barrier along with N_A^{CIGSe}, (c, d) acceptor trap states in the CdS layer, (e, f) acceptor states at the CdS/i-ZnO interface, and (g, h) n-type surface along with the increasing thickness and N_D^{n-type} into the basic device model on the JV characteristic (EQE for the n-type surface) and energy band diagram

an adjustment of only the capture cross section of the neutral defects in the absorber layer rather than by an increase of the neutral defect density. Taken as a whole, this device (AA-Asdepo-w/oNa) accordingly suffers mostly by interface recombination, which is justified by its $JV-T$ result, as simulated by SCAPS (see Figure S1b). The simulation parameters for all solar cells with and without Na can be found in Tables S3, S2, S5, and S4.

5 | DISCUSSION—DEGRADATION MECHANISMS IN CIGSE SOLAR CELLS UNDER THERMAL STRESS

Obviously, thermal stress—regardless of the atmosphere—results in severe degradation of the investigated CIGSe solar cells causing degeneration of electrical and optoelectronic characteristics. Distinct

possible causes as reasons behind these losses have been defined. Some losses can be recovered to a certain extent after removing the front contact by the use of citric acid or HCl. Using the observed trends and their associated effects on the annealed devices, we now attempt to draw up a more general model for the origins of these losses.

5.1 | Annealing after CIGSe

In the case of air annealing after CIGSe, the solar cell with Na shows a lower V_{OC} compared to the AA-Asdepo-wNa device, while N_{CV} does not show a corresponding decrease but even increases slightly. This is attributed to both an increased bulk recombination and an increased back-contact barrier height, as confirmed by $JV–T$ in Figure 6a, due to the reduced Na content in the CIGSe absorber and near the CIGSe/

Mo back interface that was clearly seen in Figure 7b. Taken together, using those effects along with the experimentally determined higher value for N_A^{CIGSe} in the simulation, the experimental device characteristics of both JV and CV of the sample AA-CIGSe-wNa can be reproduced well (see Figures 10a and S4a, respectively). In contrast, vacuum annealing after CIGSe with Na leads to a decreased V_{OC}. Here, however, a lower N_{CV} is determined. GD-OES depth profiles also only show a minor effect on the Na in-depth profile. The ΔV_{OC} values from JV and CV measurements shown in Table 2 reveal that most of the V_{OC} loss arises from the decreased N_{CV} for this device. Correspondingly, the device characteristics can again be reproduced in SCAPS using decreased N_A^{CIGSe} along with a slightly increased Φ_{BC} (see Figure 10b).

Sample AA-CIGSe-w/oNa without Na that was air annealed after CIGSe, on the other hand, exhibits a relatively high V_{OC} increase accompanied by an N_{CV} increase in contrast to the AA-Asdepo-w/oNa
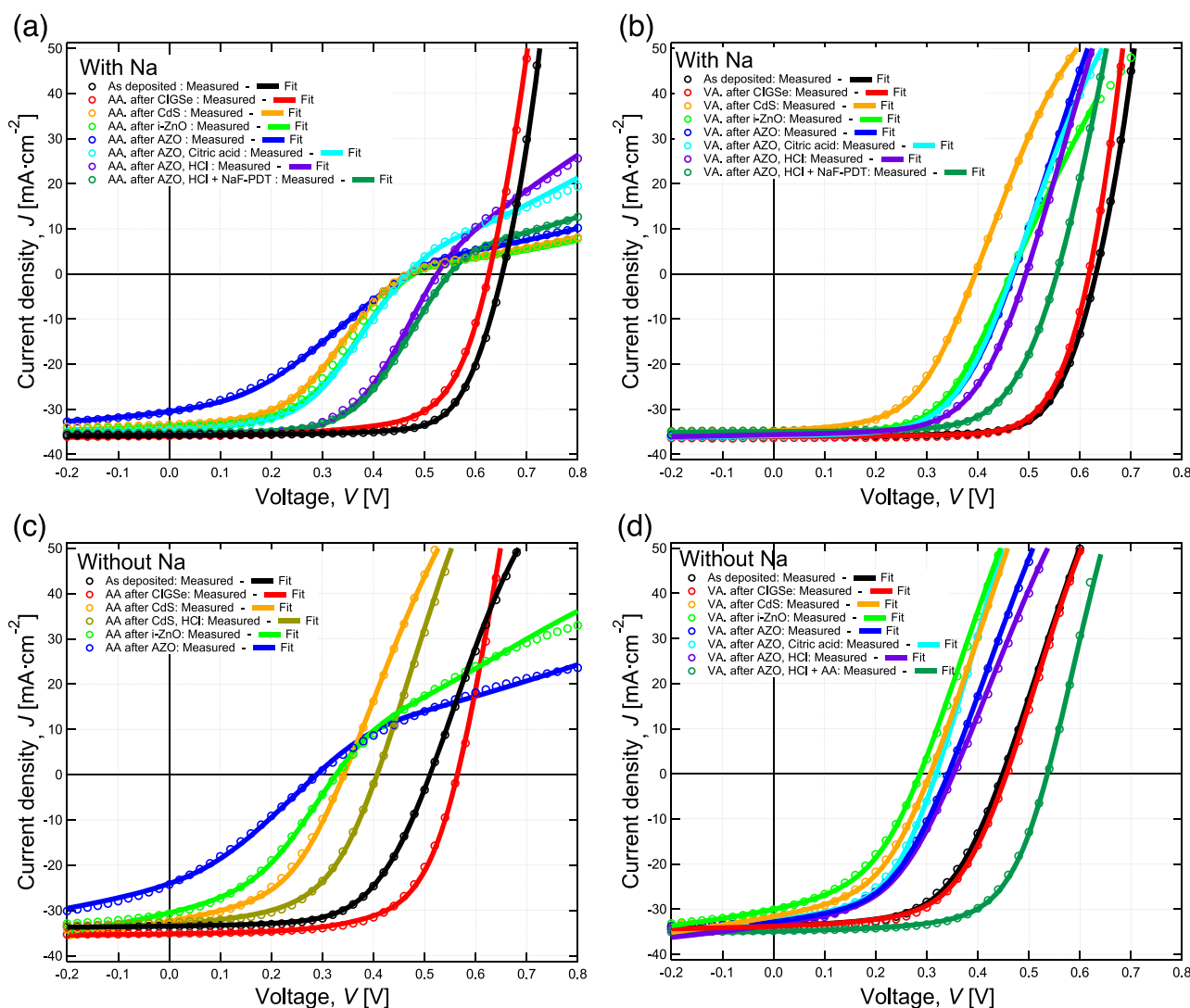

FIGURE 10 Simulated JV characteristics of the degraded solar cells in comparison with the experimentally derived JV curves after air (a, c) and vacuum annealing (b, d) as well as with and without Na, respectively

sample. Perhaps the most significant finding is that air annealing of the CIGSe absorber without Na leads to the change of the main recombination mechanism from the interface (AA-Asdepo-w/oNa) to the absorber bulk (AA-CIGSe-w/oNa) according to the JV–T results seen in Figure 6c. With $\Delta V_{OC} = -88/-10$ mV from Table 2, the V_{OC} calculated according to Equation (1) for the AA-CIGSe-w/oNa sample, much of the V_{OC} loss due to the absence of Na can be mitigated by air annealing of the bare CIGSe absorber. In spite of the absence of Na in the absorber, oxygen atoms seem able to passivate Se vacancies leading to a reduction in the donor concentration as suggested by several studies.[53–55] This may hold for both solar cells air annealed after CIGSe with and without Na incorporation, but only for N_{CV}. However, the air annealing of the Na-free CIGSe cannot completely make up the lack of Na as can be seen by the fact that the V_{OC} of this device (564 mV) is still substantially lower than the one of the Na-containing AA-Asdepo-wNa reference (652 mV). It would seem to imply that oxygen-induced passivation of the CIGSe absorber is not exclusively enough to make the cells as efficient as Na despite the interface passivation and N_{CV} increase. Comparing the simulated devices of the AA-Asdepo-wNa and AA-Asdepo-w/oNa, the low V_{OC} and efficiency are associated with four reasons: the lack of Na leads to more severe defect-assisted recombination in the absorber bulk (leading to a lower τ_e), a rather low N_{CV}, a higher Φ_{BC}, and a cliff forms at the CIGSe/CdS interface as is also implied by JV–T characterization in Figure 6a,c. According to the model proposed here for the AA-CIGSe-w/oNa sample, a spike at the CIGSe/CdS interface is set to act as interface passivation due to the increased interface energy bandgap; the absence of Na on the other hand still results in severe recombination in the absorber bulk and a higher back-contact barrier. Implementing all of the above mentioned implications into the basic device model, a good agreement between the measurements and simulations of the corresponding JV and CV results (see Figure S4) could be realized as seen in Figure 10c. We conclude that in the investigated devices, Na, beside its doping effect, plays a crucial role reducing the severity of the bulk defects (higher τ_e), limiting the back-contact barrier height, and providing the prominent spike-like band lineup at the CIGSe/CdS interface. Similarly, the dopant and passivation effects of Na have been reported by Zakay et al. and Cojocaru-Mirédin.[52,56] Here, a question for further basic research is posed with respect to the reason for the formation of the spike-like band lineup at the CIGSe/CdS interface. Does it rather depend on the band bending at the CIGSe surface or the electron affinity? In conclusion, annealing of the bare CIGSe absorber layers seems to be less critical in terms of the degradation mechanisms.

5.2 | Annealing after CdS, i-ZnO, and AZO

It is generally observed for Na-containing devices that only about one third of the V_{OC} decrease of the samples that are air and vacuum annealed after CdS, i-ZnO, and AZO can be accounted for by an N_{CV} decrease, except for the VA-CdS-wNa sample matching only one fifth of the V_{OC} decrease. According to the model proposed here, the rest

of the V_{OC} losses arise from a combination of a decreased N_A^{CIGSe} and τ_e in the CIGSe absorber due to Na out-diffusion from CIGSe, an increased Φ_{BC} due to Na depletion at the CIGSe/Mo interface, and a cliff formation at the CIGSe/CdS interface. On the other hand, a V_{OC} decrease by a decreased N_{CV} does not directly hold for the Na-free devices annealed after CdS deposition, which experimentally show even higher N_{CV}. However, the measured charge carrier profiles of these devices could contain defect contributions arising from the front contact layers, since the AA-CdS-HCl-w/oNa device shows still shifted, however reduced N_{CV} as seen in Figure 5k. This might be a reason for the defect contribution that leads to the observed additional increase in N_{CV}, when annealing is applied to the devices after CdS deposition. This effect can consistently be observed for the etched and rebuilt devices with and without Na as well (see Figure 5i–l). Additionally, the presence of a higher Φ_{BC} can also cause a decrease in the N_{CV} profile along with the shift to larger d_{SCR}, as revealed by SCAPS simulations (see Figure S2). However, a decreased N_A^{CIGSe} as an input parameter in the simulation with increasing Φ_{BC} results in the entire shift of the N_{CV} profile to the right along with significantly narrower d_{SCR} at an elevated value of N_{CV}. This should also be taken into account when interpreting the experimentally determined N_{CV} profiles. Consequently, the shift of the experimentally determined N_{CV} profiles to the right can be a strong indicator for an increased Φ_{BC}, which has been proven by the JV–T measurements in Figure 6a–d.

Looking at the Na depth profiles of the samples with Na that were air and vacuum annealed after CdS deposition in Figure 7b,d, a high amount of Na is obviously located at the CdS layer coming from the CIGSe absorber regardless of the annealing environment. A comparison of the Na depth profiles of the air- and vacuum-annealed devices reveals that the nature of the CBD–CdS, which contains a considerable amount of water and OH$^-$ ions,[57] attracts mobile Na ions from the CIGSe absorber due to its rather low electronegativity.[58] These results clearly unveil that the wet nature of the CBD–CdS buffer layer or water containing air environments poses a major problem in terms of the Na out-diffusion from the CIGSe absorber layer. Thereby for simulation, it is generally assumed that all the samples that are annealed with a CdS layer present on the CIGSe absorber have reduced τ_e, caused by the absence of Na. In the same vein, comparing the Na depth profiles of the AA-AZO-wNa and VA-AZO-wNa samples, it is possible to identify additional Na diffusion towards to the AZO surface in case of air annealing. This also confirms the triggering mechanism of Na diffusion by water and/or oxygen in air environment. Furthermore, Table 2 compares the sheet resistance value R_{Sheet} of the AZO layer of each solar cell, showing that R_{Sheet} rapidly increases upon annealing under presence of either Na or air (and strongest in case of both). Air annealing-induced additional Na diffusion into the AZO layer correlates to the strongest increase in R_{Sheet} considerably increasing the overall series resistance of the device AA-AZO-wNa. Interestingly, in view of the Na depth profiles and sheet resistance values from Table 2, a comparison of the AA-AZO-wNa, AA-AZO-w/oNa, and VA-AZO-wNa samples provides strong evidence that Na and humid air have a detrimental effect on the TCO
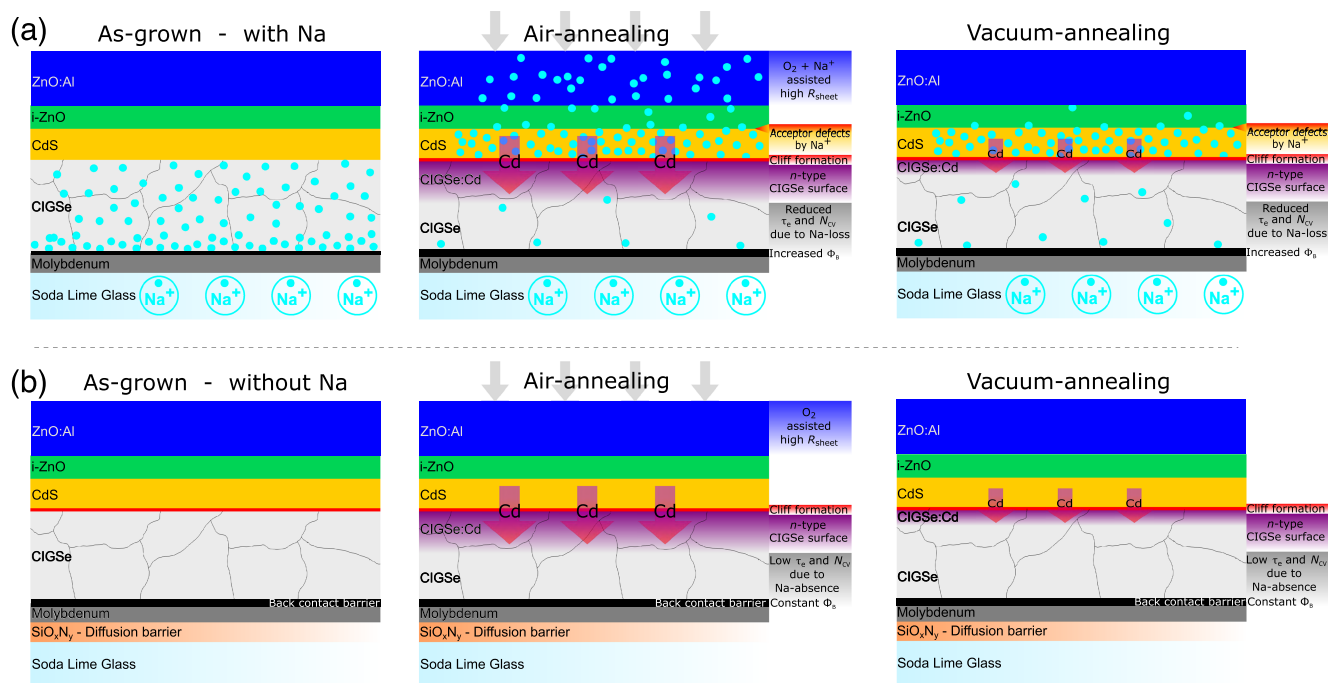
FIGURE 11 Schematic representation of the suggested thermal stress-induced degradation mechanisms of the CdS-buffered CIGSe thin-film solar cells with (a) and without Na (b) in air and under vacuum along with the initial states of the solar cells (as-grown)

conductivity or that Na enhances a detrimental effect of humid air on the TCO, as a catalytic effect of Na was described in several studies before.[16,59]

It is stressed that if any of the Na-containing samples is exposed to thermal stress, they exhibit almost the same $\Phi_{BC} \approx 0.20$ eV as in the case of the Na-free solar cells, which also show a higher Φ_{BC} even after annealing (see Figure 6a–d). The integration of the above mentioned observations into the simulations has generated a good correlation between measurement and simulation for annealed devices after CdS deposition (see Figure 10a–d). Besides this, the measured JV curves of the air-annealed devices exhibit a stronger rollover anomaly than the vacuum-annealed devices. As discussed in Section 4, the severity of the rollover anomaly hinges on N_A^{CIGSe} and the Φ_{BC} (see Figure 9a,b). Accordingly, the strong rollover behavior of the air-annealed samples with and without Na could only be simulated with further increased Φ_{BC} and N_A^{CIGSe} (see Tables S3, S2, S5, and S4), even though their measured N_{CV} is lower.

All the devices annealed after CdS deposition exhibit a clear kink behavior (voltage-dependent current loss) in the JV characteristics, which is also discussed in Section 4. As mentioned above, after the annealing treatment, Na atoms are mainly located within the CdS layer and also its surroundings, that is, CdS/i-ZnO interface. Na is known to generate deep acceptor defects in the CdS[44] and ZnO.[45,46] Considering the experimental observations and possible reasons for a kink behavior as well as accordingly integrating the deep acceptor defects into the CdS layer and at the CdS/i-ZnO interface, the established SCAPS model shows only modest correlation between measured and simulated JV characteristics for kink behavior. In the

case of the samples without Na, however, there is inconsistency with this argument, since no interdiffusion apart from Cd diffusion into CIGSe is detectable from GD-OES in-depth profiles. Therefore, kink behavior of the annealed samples after CdS deposition without Na is simulated in SCAPS model by an additional light-dependent shunt resistance, which reproduces well their measured JV characteristics along with the other observations as seen in Figure 10c,d.

Another significant aspect we assume is the formation of a cliff at the CIGSe/CdS interface that is inferred from the difference between E_a and E_g^{EQE} as determined via JV–T measurements on the devices, which were annealed after CdS deposition, as shown in Figure 6a–d. Accordingly, Na-containing devices that are annealed after CdS deposition suffer highly from recombination at the CIGSe/CdS interface. In the case of Na-free devices, even the as-deposited case shows intrinsically high interface recombination at the CIGSe/CdS interface, again interpreted as a cliff formation. Annealing of this junction with the presence of CdS on top of CIGSe leads to increased cliff formation. With these findings integrated into the simulations for all the samples with and without Na that are annealed after CdS deposition, the experimentally observed V_{OC} losses could be well simulated.

5.3 | Current loss analysis

For current loss analysis, EQE results are consulted. There is a small decrease in J_{SC} due to reduced collection in the long-wavelength region for the samples that are air annealed after CIGSe with and without Na (AA-CIGSe-wNa and AA-CIGSe-w/oNa). Taking into

account that an increased charge carrier density observed for these devices (see Table 2) will cause a reduced width of the space charge region, a smaller effective collection length is suggested to be the reason for this observation.[60,61]

Additionally, the *EQE* curves of the solar cells that are annealed after CdS deposition with and without Na are inclined in the wavelength range between 400 and 1000 nm, which is interpreted as a confirmation of an *n*-type layer formation on top of the absorber (cf. Figure 9g,h) due to the Cd diffusion into CIGSe via the formation of Cd_{Cu} defects that can be clearly seen in Figure 7a,e. Without Na in the devices, this effect is stronger visible. By the aid of the measured Cd in-depth profiles as seen in Figure 7a,b,e,f, the thickness of the *n*-type surface on top of the CIGSe is subsequently chosen 200 and 50 nm for air-annealed and vacuum-annealed devices in the simulations, respectively. There is no indication that the etching and rebuilding of the window layers affected the *n*-type surface layers, which is why they are still present in the simulations for those devices as well. With the presence of the accordingly chosen *n*-type surface layer and tailoring the N_D^{n-type} in order to be able to reproduce the experimentally observed effect in their *EQE* curves, the simulated device performances correlate well with the experiment. However, it should also be noted that—even though an HCl etch could not remove once diffused Cd from the CIGSe surface region—the effectiveness of a possible *n*-type surface is also reduced by redeposition of fresh window layers.

According to the *EQE* result for the device with Na that was air annealed after i-ZnO, the response of the short wavelength region that is characterized by absorption losses in the CdS may suggest the formation of a layer with a higher bandgap than that of CdS, such as maybe CdZnS as suggested by Ramanathan et al.[8] However, we tend to suppose that it is rather the same pathologic trend as when annealing after AZO with Na (exhibiting an *EQE* > 1) that is already in effect and which we attribute to a light-sensitive behavior in the window layers causing an additional flow of injected charge carriers towards the front contact during measurement of the spectral response. It has been argued that this behavior (*EQE* > 1) happens only when applying a voltage bias.[23] In contrast, Figure S3 implies that here it is the application of a light bias that induces this pathologic behavior of the spectral response, similarly proposed by Phillips and Roy,[24] while applying voltage bias seems not to have an effect.

Additional current loss is observed in the *JV* characteristics (see Figure 10a,c) for the devices that are air annealed after AZO with and without Na compared to the samples that are air annealed before AZO deposition. This clearly indicates that this additional drop in J_{SC} is driven by the increased AZO resistivity (see Table 2) in those devices resulting in higher series resistance, as also discussed above. These increases in AZO resistivity were translated into the SCAPS simulations as an overall increase in series resistance, resulting in a good agreement with the experimental data, since an increase of the resistivity of the TCO cannot directly be integrated into the AZO layer in SCAPS due to the fact that this is a two-dimensional effect, which is not applicable to SCAPS-1D.

5.4 | Etching procedures

After removing the ZnO bilayer by etching with citric acid, there is no significant change seen in V_{OC} and N_{CV} as well as in the shape of the *JV* curve in any of the samples with and without Na (AA-AZO-citric-wNa, VA-AZO-citric-wNa, and VA-AZO-citric-w/oNa) as compared to the corresponding samples (AA-AZO-wNa, VA-AZO-wNa, and VA-AZO-w/oNa). On the other hand, the removal of the CdS layers along with the ZnO bilayers by HCl etching leads to an increase in V_{OC} of more than 60 mV for the sample AA-AZO-HCl-wNa and 25 mV for the VA-AZO-HCl-wNa sample. The reader is reminded that citric acid does not and HCl does remove the CdS together with the TCO front contact during etching and that in annealed devices, the CdS layer is extremely Na rich, as seen in Figure 7b. Additionally, we infer from the *JV–T* measurements that the HCl-etched sample (AA-AZO-HCl-wNa) exhibits a smaller cliff-like CBM offset than the AA-AZO-wNa and AA-AZO-citric-wNa samples (see Figure 6a), indicating that the Na accumulation in the CdS might be the origin of the magnitude of the cliff formation at the CIGSe/CdS interface. This would indeed explain the more pronounced cliff formation at the CIGSe/CdS interface, since Na is known to raise the electron affinity of the CdS layer.[62] Applying this to our SCAPS model, we ascribe up to one third of the annealing-induced V_{OC} loss to the Na diffusion into the CdS layer regardless of the annealing environment. With reduced electron affinity of the CdS layer, HCl-etched samples can be fitted well to the measured characteristics in both cases of air and vacuum annealing (see Figure 10a–d).

Applying a NaF PDT after the HCl etch on the CIGSe absorber of the air-annealed sample with Na (AA-AZO-HCl-NaF-wNa) recovers the V_{OC} by an additional 20 mV. It could nevertheless be argued that the NaF PDT itself does not contribute to a carrier concentration increase (see Figure 5i) and seems to be ineffective for the CIGSe bulk as seen from its Na depth profile in Figure 7b. The effectiveness of the NaF PDT could be attenuated by the presence of a secondary phase such as $Cu_2(S,Se)$ which is well known to be detrimental for CIGSe thin-film solar cells.[10,63,64] This was investigated in a separate experiment, for which the reader may refer to Figure S5. The experiment shows that secondary-phase formation can be excluded in our case. The relative increase in V_{OC} seen for the sample VA-AZO-HCl-NaF-wNa is higher than for the sample AA-AZO-HCl-NaF-wNa; however, both of them have comparable V_{OC}. Applying the NaF PDT to the vacuum-annealed and HCl-etched sample (VA-AZO-HCl-NaF-wNa) shows a subtle increase in its Na depth profile in the whole absorber as can be seen in Figure 7d. Consequently, there are two main effects of the NaF PDT in terms of the recovery of the degraded devices: a surface or interface effect and a bulk effect. With respect to the NaF PDT-treated sample AA-AZO-HCl-NaF-wNa, the fact that the negative band offset (cliff) at the CIGSe/CdS interface is reduced results in a good correlation of simulated and experimental device characteristics as seen in Figure 10a. Hence, here the effectiveness of the NaF PDT remains at the CdS/*n*-type CIGSe interface and cannot reach the CIGSe absorber bulk possibly due to the formation of a rather thick *n*-type CIGSe surface, which the Na diffusion is unable to

overcome, as indicated above. As a result, it can be concluded that a NaF PDT supports better junction properties at the CIGSe/CdS interface. On the other hand, the presence of both a decreased negative band offset (cliff) and an increased τ_e of the CIGSe absorber due to the slightly increased Na content in the CIGSe (bulk effect) for the NaF PDT-treated sample VA-AZO-HCl-NaF-wNa reproduces the experimentally determined curves well (see Figure 10b). This coincides with the fact that the assumed thickness of the n-type CIGSe surface for vacuum-annealed devices is rather thin, which presumably allows the NaF PDT on this device to be more effective.

Applying an air-annealing treatment to the sample without Na that was vacuum annealed after AZO and etched with HCl instead of application of a NaF PDT (VA-AZO-HCl-AA-w/oNa) has led to a similarly improved V_{OC} as the NaF PDT treatment on the samples with Na and even better diode behaviors (without rollover anomaly). Along with the remarkable increase in N_{CV}, this again suggests the previously mentioned oxygen-induced passivation. Its JV–T characteristic shown in Figure 6d reveals that this device is not limited at the CIGSe/CdS interface. Therefore, the JV and CV characteristics of this device are well simulated by employing a positive band offset (spike) at the CIGSe/CdS, as in the case of as-deposited devices with Na. This motivates further investigations of a combination of an air-annealing treatment and a NaF PDT in order to make more efficient and possibly more thermally stable devices. In conclusion, the latter approach for the Na-free CIGSe devices illustrates that overall degraded devices can be recovered or even improved. However, the complete recovery of this device might be dependent on the thickness of the n-type CIGSe surface, as stated above. Further investigation should be carried out in order to better understand whether severity of the formation of n-type CIGSe surface prevents the complete recovery of the degraded solar cells.

A summary of the main findings and of the principal issues for the general representation of the degradation mechanisms of the CdS-buffered CIGSe solar cells is schematically illustrated in Figure 11. It is suggested that the degradation mechanisms of the CdS-buffered CIGSe solar cells are in principle independent of the thermal stress environment in terms of the overall device performances. However, this does not hold for the AZO degeneration and rollover anomaly. It was found that the solar cell performances decrease markedly when the devices are annealed after CdS, i-ZnO, and AZO deposition. Air annealing leads to severe Cd diffusion into CIGSe, populating the CIGSe surface with n-type doping, while vacuum annealing does not bring about severe Cd diffusion. The major issue is Na out-diffusion from CIGSe absorber into CdS and TCO layers regardless of the environment, leading to an increased Φ_{BC}, reduced N_{CV} and τ_e, cliff-like formation at the CIGSe/CdS interface, and acceptor defects in CdS layer and at CdS/i-ZnO interface, since the presence of water and OH⁻ bonds in the CBD-deposited CdS layer attracts Na ions due to their low electronegativity.[58] Moreover, Na also expedites the degradation of the AZO conductivity, when annealing takes place in air together with AZO layer. All things considered, it is alluded by help of the etching procedures and annealing directly after CIGSe deposition that the CIGSe absorber material is thermally stable. It is worth noting

that the conclusions and decay mechanisms for the CBD–CdS-buffered CIGSe solar cells that are presented here can only be argued to apply for the composition $CGI \sim 0.9$, which is used here, as it represents a commonly used composition in the field of CIGSe solar cells and modules. Most of the degradation mechanism we discussed depend on the diffusivity of Na within the CIGSe, which, for example, is known to be different in Cu-poor materials from stoichiometric or Cu-rich compositions as proposed by Nishinaga et al.[65] Therefore, the device's degradation mechanisms are likely to also show a dependence of the Cu content of the CIGSe absorber.

6 | CONCLUSION

The degradation mechanisms of the CdS-buffered CIGSe solar cells with and without Na incorporation under thermal stress were investigated. To distinguish degradation effects, annealing was performed on unfinished layer stacks after CIGSe, CdS, i-ZnO, and AZO deposition. In addition, the etching processes—removing degraded window components from the annealed devices—has been performed as a mitigation strategy. In all cases, the electrical, optoelectronic, and compositional properties of the CIGSe devices have been characterized before and after thermal stress was applied in air and under vacuum conditions. It is proposed that the degradation mechanisms of the CdS-buffered CIGSe solar cells are in principle independent of the thermal stress environment. This does however not hold for the AZO degradation and the rollover anomaly. It was found that the solar cell performance drops severely when the devices are annealed after CdS, i-ZnO, or AZO layer deposition. Na diffusion from the CIGSe absorber into the CdS and TCO layers is the main cause for the observed degradations, since the movement of the Na ions is primarily triggered by the presence of water and OH⁻ bonds in the CBD-deposited CdS layer, which both attract Na due to its low electronegativity. By the same token, Na accelerates the degradation of the AZO conductivity resulting in an increased device series resistance when annealing takes place in an air environment. Na may also cause acceptor-like defects in the CdS, TCO layers, and the respective interfaces. As JV–T measurements have shown, any annealing procedure carried out after CdS deposition seems to give rise to a cliff formation in the band lineup at the CIGSe/CdS interface resulting in a severe V_{OC} drop. Consequently, Na out-diffusion has a very deleterious effect on the device performance. In addition, Cd diffusion into the CIGSe absorber is also observed after annealing, particularly when the devices are exposed to air annealing. This may cause the formation of an n-type surface via the formation of Cd_{Cu} defects. By means of the etching processes, it is proposed that mitigation of the observed loss seems to be possible at least in part when redepositing fresh front contact layers such as CdS and TCO layers. The absence of Na in CIGSe in Na-free devices and in devices with Na after annealing, who have suffered Na loss by out-diffusion from CIGSe, seems to induce a decreased τ_e and N_{CV}, an increased back-contact barrier height, and a lower quality junction at the CIGSe/CdS interface due to cliff formation. Towards increased thermally stable CIGSe devices, no Na or at

least no Na diffusion from the CIGSe absorber into the buffer/TCO layers, no Cd diffusion into the absorber, and stable back-contact properties have to be achieved. Future research should further develop new thermally and chemically suitable materials or material combinations for use as buffer layers in CIGSe thin-film solar cells.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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SUPPORTING INFORMATION

Additional supporting information may be found online in the Supporting Information section at the end of this article.