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Printed circuit board embedded power semiconductors: A technology review

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ABSTRACT

Embedding power semiconductor devices into printed circuit boards (PCB) provides several benefits compared to conventional packaging technologies. Integrating the semiconductor dies into the circuit board reduces the converter size. This results in short current loops, enabling low interconnection resistances and parasitic inductances. Both contribute to a higher system-level efficiency, as conduction and switching losses are reduced. Moreover, the use of thick Cu substrates allows efficient heat removal, due to a low thermal resistance. Therefore, PCB embedding has received a lot of attention in the power electronics community for more than a decade. This article aims to provide a comprehensive review of the scientific literature on the topic ranging from basic fabrication technology over module or system-level demonstrators for electrical and thermal testing to reliability studies. Performance indicators, such as the commutation loop inductance L_σ, the chip area independent thermal resistance $R_{th} \times A_{chip}$, allow a comparison of different approaches and benchmarking with conventional power modules. Several publications report stray inductances below 1 nH and chip area independent thermal resistances in the range of 20…30 mm^{2}K/W.

1. Introduction

Printed circuit boards (PCB) are essential components of almost any electronic system. They provide electrical interconnection of the active and passive components, which are assembled on the surface of the PCB by soldering, adhesive bonding, or press-fit technology. Driven by the demand for more compact electronic devices, engineers started to build passive components inside the multilayer structure of the circuit boards (Jillek & Yung, 2005). Resistors are generated using resistive layers, such as NiP-based *Omegaply (Ohmega Technologies Inc. USA)*, which are laminated in the circuit board stack-up. Dielectrics with high relative permittivity enable embedded capacitors and magnetic materials allow the fabrication of integrated inductors (Waffenschmidt et al., 2005). Attaching SMD-components on internal layers and burying them in the subsequent lamination steps provides an alternative approach to fabricating PCB-embedded passives (Hofmann, 1996). In the same way, active components, either with an SMD package or as a bare die, can be integrated into the PCB multilayer (Jung, Ostmann, & Landsberger, 2000; Manessis et al., 2017; Ostmann et al., 2002; Palm et al., 2005; Waris et al., 2001). At first, these technologies were developed with focus on mobile communication applications (Kujala et al., 1999). In view of a higher degree of miniaturization, *Fraunhofer IZM* developed PCB-embedded 2-chip modules, 3D System-in-Package (SiP), and Quad-Flat Non-Lead (QFN) packages (Ostmann et al., 2009). The miniaturization came along with a drastic reduction of parasitic resistances and inductances, which is of special interest for power electronic circuits. Soon, low-power converter SiP using PCB embedding technologies were commercialized. An example is *Texas Instruments MicroSiP*™ technology, which was introduced in 2010 (Texas Instruments, 2017). Here, a low-power DC/DC converter contains a substrate-embedded MOSFET bare die and surface-mounted passive components, see Fig. 1. Comparable technologies are available from several companies, such as *DrBlade*™ by *Infineon* or *Semiconductor Embedded in Substrate (SESUB)* by *TDK* (Infineon Technologies, 2014; TDK, 2022). Typically, these embedded SiPs have power levels in the range of several watts and operating voltages below 50 V.

More recently, researchers and engineers have investigated the use of PCB embedding for higher power applications covering voltage ratings up to 1200 V and power levels up to 100 kW. One of the main drivers of this development has been the electrification of passenger vehicles, which demands highly efficient power converters with high volumetric and gravimetric power density at low costs (Grubl et al., 2018; Ostmann et al., 2002). Due to the possibility to minimize the package parasitics, PCB embedding is particularly beneficial in combination with

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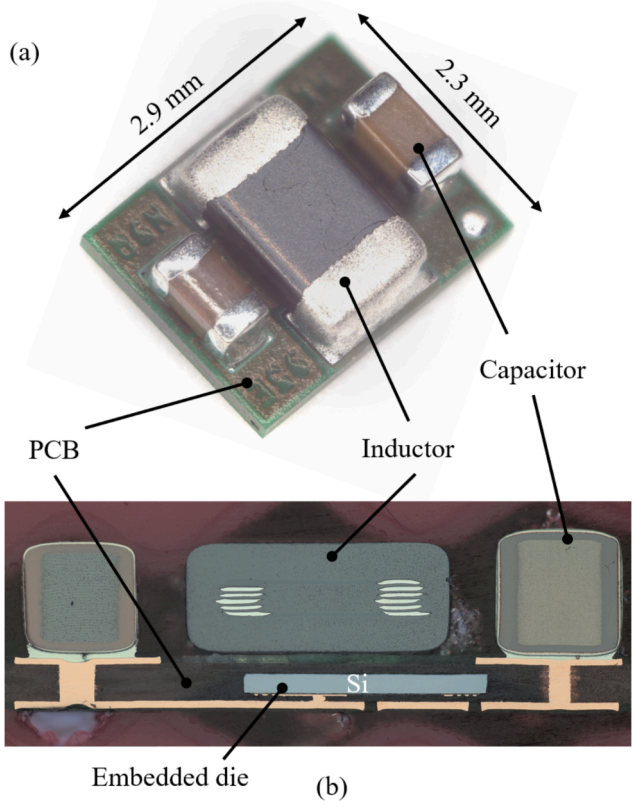

Fig. 1. Texas Instruments μSIP DC/DC converter (a) optical micrograph and (b) cross section. A silicon die is embedded in the PCB.

fast-switching wide-bandgap power semiconductors, such as silicon carbide (SiC) MOSFET or gallium nitride (GaN) HEMT. These devices demand low commutation loop inductances for clean and efficient switching (Kaminski, 2017).

This article reviews the scientific literature on PCB embedding of power semiconductors for mid-power applications (herein defined as ~1…100 kW, voltages up to 1200 V). It does not cover low-power applications, embedding of passive components, sensors, or thermal management. Another recent review on embedding technologies with a broader scope covers these topics (Buttay et al., 2018).

The paper is structured as follows: The first section briefly introduces the power semiconductor devices which are embedded into circuit board. Next, the fabrication technology is presented with focus on mainstream industrial processes. Moreover, the paper covers unconventional approaches, often investigated by academic researchers. Common challenges in fabrication are reviewed and discussed. Section 3 presents the requirements for the selection of embedding materials and presents some selected examples. Technology demonstrators that have been used for thermal and electrical performance testing are discussed in Section 4. With reference to the performance numbers, benefits of the technology will be worked out. Next, the challenges and limitations of embedding are described. Section 5 focuses on the reliability of PCB-embedded power semiconductors, addressing thermomechanical issues and electrical isolation. A brief discussion and outlook on future developments conclude the paper.

2. PCB embedding technology

This section presents the fundamentals of PCB embedding. First, the active power semiconductor devices, which are embedded into the circuit board, are briefly presented. Subsequently, conventional packaging technologies are briefly introduced before presenting different established approaches for PCB embedding. There are some common challenges, such as the necessity of Cu chip metallization, microvia drilling and plating, and thermomechanical stresses. More unconventional embedding technologies are presented in the last subsection.

2.1. Power semiconductors and conventional packaging

Power electronic converters are based on switch-mode operation and, therefore, require semiconductor transistors as switching elements. Silicon metal-oxide-semiconductor field-effect transistors (MOSFET) are typically used for low-voltage applications of up to about 600 V. For higher voltages insulated-gate bipolar transistors (IGBT) present the standard solution (Wintrich et al., 2015). However, they require a separate antiparallel freewheeling diode in most applications. New semiconductor devices based on wide band gap materials are becoming increasingly popular, due to their higher efficiency, especially in fast-switching applications. Prominent examples are gallium nitride (GaN) high-electron-mobility transistors (HEMT) and silicon carbide (SiC) MOSFET. GaN HEMT serve applications with voltages up to 650 V, whereas SiC MOSFET are applied for higher voltages. In contrast to microelectronics, where usually millions of transistors are integrated into a single semiconductor chip, these power devices contain one single transistor per chip only. The current rating of the device scales with its footprint area A_{chip}. For MOSFET and IGBT, a vertical structure is used, with gate and source (or emitter in case of the IGBT) on the top side of the chip and the drain (or collector) on the bottom side (ABB, 2013). GaN HEMT are horizontal devices, with all functional contacts on the chip top side. However, its substrate requires a defined potential and therefore contains a separate contact on the chip bottom side. Consequently, any packaging technology for power semiconductors needs to establish electrical connections on the top and the bottom side of the semiconductor chip. In conventional packages, the semiconductor is attached bottom down to a conductive substrate, either a metal lead frame in case of discrete packages or a copper cladded ceramic substrate in case of multi-chip power modules. To enable solder die-attach, a silver surface is used for the bottom metallization of the die. The top side contacts are formed with thick aluminum bond wires and require an aluminum-based metallization. For protection and to provide sufficient isolation, the devices are encapsulated in epoxy molding compound or by potting in silicone gel. In conventional power circuits, the packaged semiconductors are electrically connected to other components of the circuit by printed circuit boards or bus bars. PCB embedding provides an alternative approach—that of embedding the power semiconductor chip into the circuit board. The following sections present the fabrication technology of such embedded power devices.

2.2. Mainstream embedding processes

Fabrication of PCB-embedded power devices essentially means building a circuit board around the semiconductor die. This section presents the three most common fabrication processes, which are commercially available from various PCB manufacturers. Fig. 2 schematically illustrates the basic process steps, showing (a) the “Chip-on-Substrate” process, (b) the “Chip-in-Cavity” process, and (c) “Double-side Microvia” process. The Chip-on-Substrate process was invented by *Fraunhofer IZM* in 1999 (Jung, et al., 2000). In a first step, the semiconductor die is attached to a “PCB bottom layer”. This bottom layer is either a Cu substrate (Link et al., 2021), an insulated metal substrate (IMS) (Ostmann et al., 2012), or a copper-cladded ceramic substrate such as direct copper bonded (DCB) (Hoene et al., 2013; Huesgen et al., 2021). Several prepregs (a glass fiber fabric, pre-impregnated with partially cured resin, known as FR4 in PCB industry) are stacked on top. The first prepreg layers have cutouts, to accommodate the semiconductor chip, while upper layers cover the full area. A copper foil covers the stack. The thickness and resin content of the prepregs requires careful consideration, as the free volume of the geometry is filled by a resin flow from the prepregs (Munding et al., 2017). The stack is

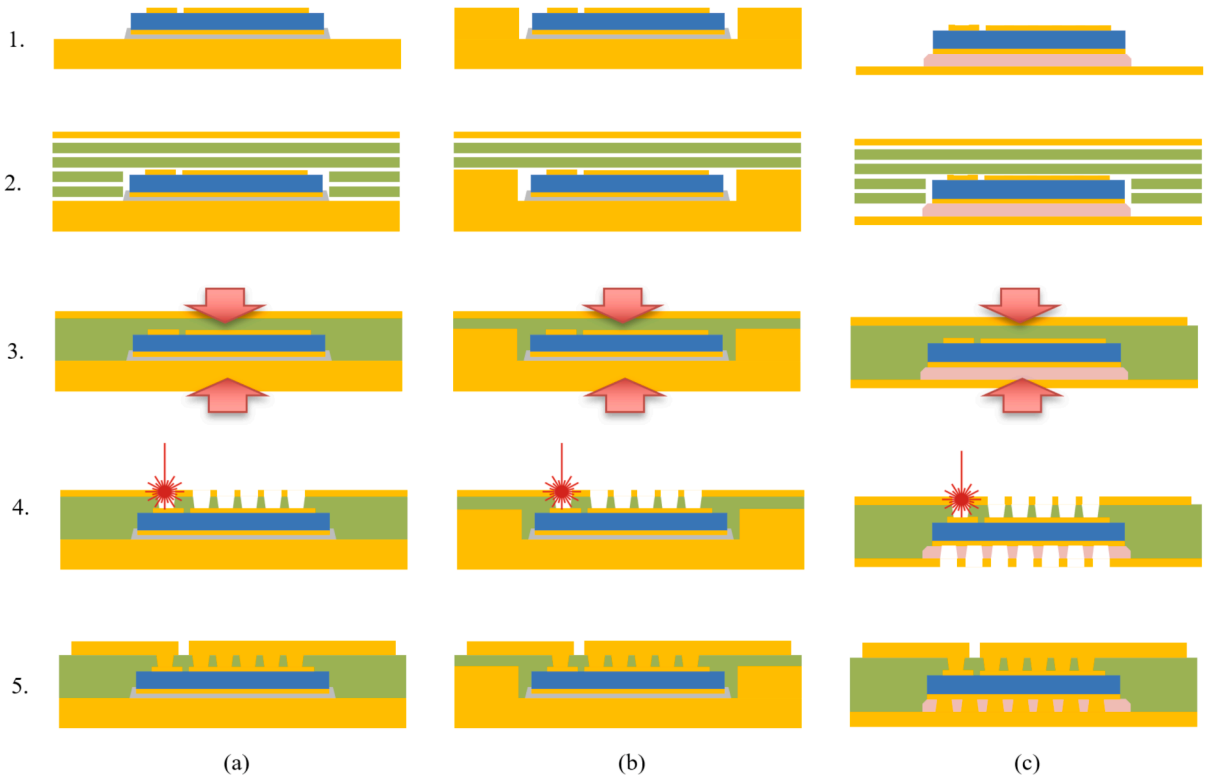

Fig. 2. Illustration of the PCB embedding process flows: (a) Chip-on-Substrate, (b) Chip-in-Cavity, and (c) Double-side Microvia.

laminated in a vacuum press at a temperature in the range of 180…200°C and a pressure of 1…3 MPa for 60…180 min. The exact process conditions depend on the resin type and exact geometry. Microvias are drilled using a laser process, stopping on the top side chip metallization. The top side contacts are established by Cu electroplating and subsequent structuring of the top side trace. The plating process requires a copper metallization on the chip, which is uncommon today, as most semiconductor chips have an Al-based metallization for wire bonding. This issue will be discussed in more detail in Section 2.3. An optical micrograph of a cross-section through an Si diode that has been embedded by the Chip-on-Substrate process is shown Fig. 3 (a).

The Chip-in-cavity process is outlined in Fig. 2 (b). The substrate, typically a thick Cu plate, features a cavity, where the semiconductor die is placed. The cavity depth equals the chip and die-attach bond line thickness, so that the top metallization of the chip is level with the substrate surface. Subsequently, unstructured prepregs and a Cu foil are stacked on top. There is no need to work with structured prepregs, which facilitates stacking of the laminate. The subsequent steps of the process are identical to those of the Chip-on-Substrate process and require vacuum lamination, laser drilling, Cu plating and structuring of the top trace. This technology is available from PCB suppliers, such as *Schweizer Electronic AG*, Germany (known as p^2 *Pack*® technology) (Gottwald & Roessle, 2014; Gottwald & Roessle, 2018) or *Advanced Semiconductor Engineering ASE Inc* (here known as *embedded active system integration eASI*) (Essig et al., 2016; Essig et al., 2017). Fig. 3 (b) shows a cross-sectional view of an embedded package fabricated with the p^2 Pack technology

Double-side Microvia embedding is shown in Fig. 2 (c). Here, the chip is attached by a (non-conductive) adhesive to a thin Cu foil. Multiple layers of prepreg, with and without cutout, and a final Cu foil are stacked on top. The stack is vacuum laminated before microvia are laser drilled on the top and bottom side of the device. That way all electrical connections are established by Cu plating, avoiding any potentially critical die-attach layer. This process is known as *Embedded Component Package ECP*® from *AT&S*, Austria (Stahr, 2021), or *MICROVIA*.

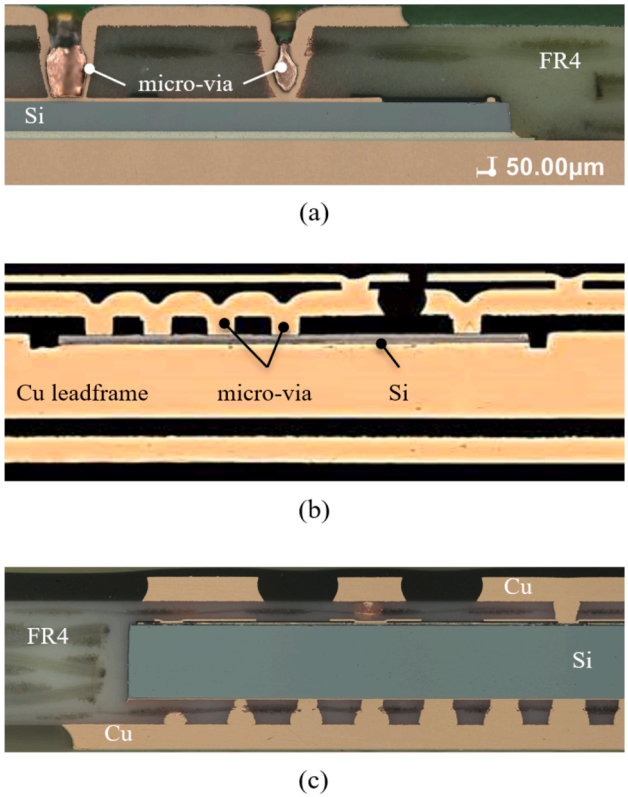

Fig. 3. Microscopic cross section of different PCB embedding approaches (a) Chip-on-Substrate, (b) Chip-in-Cavity [courtsey of Schweizer Electronic AG], and (c) Double-side Microvia.

embedding technology from *Würth Electronic*, Germany (Wolf, 2021). A cross-sectional micrograph of a *GaN Systems GS61008T* package, which is fabricated by ECP technology, is shown in Fig. 3 (c). The basic Double-side Microvia process can be modified by introducing a full area plating on the chip backside, to improve heat removal from the embedded component. *AT&S* labels this process variation *PARSEC (PlAnaR Surface Embedded Components)* technology (Stahr & Morianz, 2019).

The embedding technologies described above can be applied for two different integration concepts, as illustrated in Fig. 4. In the first concept, embedding is used as device-level fabrication technology to generate PCB power packages. These are attached as surface mount device SMD components to the main circuit board. Embedding provides an alternative solution to the classical leadframe-based discrete packages. The *GaN Systems GaN PX* package is a good example of such a PCB power package (GaN Systems, 2022). It is fabricated using the ECP technology from AT&S. Some publications use the term "prepackage", which was first introduced by researchers at Fraunhofer IZM (Ostmann, 2017). In contrast to a PCB power package, a prepackage does contain a heat spreader and does not provide sufficient clearance and creepage. A second assembly step, for example by PCB embedding, is required to obtain a functional power module. Sharma et. al. present a good example for this approach (Sharma et al., 2020).

The second concept utilizes PCB embedding for both, device level packaging and board-level packaging. This requires additional lamination steps after embedding, to add more routing layers and to provide electrical insulation on the bottom side of the package where the heat sink is attached. To enable efficient heat removal, thermally conductive, electrically insulating prepreg materials are required. More details on the materials are given in Section 3. A printed circuit board with multiple embedded power semiconductors and internal electrical isolation will be labeled as PCB power module. Additional components, such as gate drivers, decoupling capacitors, and temperature or current sensors are attached as SMD to the PCB power module to generate an embedded "intelligent" power module (IPM). In an extreme case, the entire power circuit is integrated on the embedded PCB to form a complete System-in-Board (SiB).

2.3. Fabrication technology challenges

This section details important challenges, which need to be addressed in almost any embedding process. As discussed earlier, power semiconductors are typically available with Ag surface on the backside and Al surface on the frontside. Embedding requires a Cu surface for subsequent microvia plating. The first subsection presents ways to generate Cu surfaces, either on wafer-level or on chip level. Laser-drilling is another critical process step closely linked to the Cu metallization and is covered in the second subsection. The last subsection concerns thermomechanical stresses, that are intrinsically present in packages with heterogeneous materials having different coefficient of thermal expansion (CTE).

2.3.1. Copper plating

As detailed above, a Cu metallization is required for most embedding processes, either on the front-side only (Chip-on-Substrate and Chip-in-Cavity) or on both sides of the chip (Double-side-Microvia). However, front side Cu is also of interest for conventional packages, where a replacement of Al bond wires by Cu bond wires leads to a significant improvement of the power cycling (Heuck et al., 2014; Rittner et al., 2014) . Within the publicly-funded research project *ProPower*, wafer-level electroplating has been investigated. First, a seed layer is deposited on top of the original chip metallization and structured by photolithography. Subsequently, Cu is electroplated in the chip pads which are defined by the photoresist. Stripping of the photoresist and etching of the seed layer follows. Last, the chips are diced and removed from the carrier. Plating process parameters were optimized to enable plating of up to 50 µm thick Cu. However, chip bending of more than 100 µm was observed for Cu thickness in the range of 30…50 µm. Bending of the die can be reduced by a double side plating of Cu. Special tools have been developed for this purpose and allow low stress Cu on thin power semiconductor wafers (Melvin & Roelfs, 2017).

As these plating processes are not yet widely integrated into commercial fabrication lines, many users have to deal with standard metallization. Therefore, researchers developed chip-level solutions for deposition of Cu on native Al metallization. Randoll et al. describe a chip-level electroplating process, similar to the wafer-level process described above (Randoll, 2018; Randoll et al., 2016). Another option is to use physical vapor deposition (PVD). Here, the Cu geometry is defined by a shadow mask, which avoids photolithography at chip level. Such a process was used by Kearney et al. to sputter Cr/Cu (5 nm / 8 µm) on the Al top side metallization of IGBTs and Diode (Kearney et al., 2017). Le Leslé et al. compared e-beam and thermal evaporation of Cu (Le Lesle et al., 2020). Both approaches proved to be impractical. Thermal evaporation did not yield a good adhesion between the original metallization and to Cu layer, leading to a significant increase in losses during device operation. The e-beam process, however, introduced a negative shift in threshold voltage, due to trapped charges in the gate oxide.

2.3.2. Microvia formation

After lamination of the PCB stack, the electrical contacts are

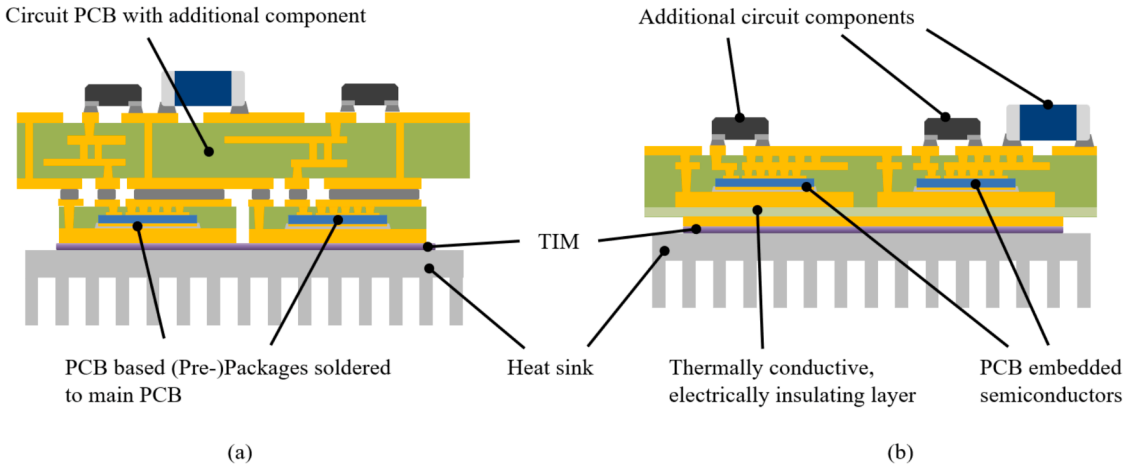

Fig. 4. Illustration of integration concepts for PCB embedding (a) PCB power packages are used as SMD, and (b) an embedded intelligent power module (IPM) or System-in-Board is fabricated by additional embedding steps after prepackage fabrication.

established by microvias. Microvias are formed by laser processing, using either ultraviolet (UV) radiation or infrared (IR) radiation (Liu, 2021). Both can remove the glass fabric/resin composite material. Cu is only removed by UV laser, which is a benefit as the microvia formation starts with drilling through the top Cu layer. When using an IR-laser, the top copper layer needs to be removed by photolithography and etching beforehand. On the other side, the drilling process needs to stop on the chip metallization without causing any damage. Here, the IR laser is beneficial, as it provides a lower energy input to the metallization (Ostmann et al., 2013). A deeper study of the laser process is presented by Munding et al. (2017). In their study, they used an IR laser with 9.4 μm wavelength. A PVD process with subsequent photolithographic structuring was used for Cu deposition on the native Al metallization of the chip. A wide range of process parameters was investigated. In case of high energy input, blisters were observed in the metallization. The blisters are caused by eutectic formed at the Al-Cu interface. This eutectic phase has a melting point of only 547°C compared to 660°C for pure aluminum. Hence, the eutectic melts first, when reached by the heat-affected zone of the laser process. In the worst case, the entire metallization is removed in this location and might even trigger chip cracking. To overcome this issue, the authors recommend to plate copper with a thickness of more than 11 μm to keep the Al-Cu interface out of the heat affected zone (Munding et al., 2017). Additionally, a diffusion barrier can be placed between the Al and the plated Cu to avoid formation of the eutectic phase.

Other researchers have optimized the geometry of the via structure to achieve low electrical contact resistance and low thermal resistance. Yu et al. investigated the influence of via size and via count on the contact resistance (Yu et al., 2016). As uncommon geometries (square well with 1 mm^2 through a 400 μm thick FR4 layer and a Cu plating thickness of 7 μm) were investigated, an unrealistically high resistance of 1.13 mΩ was theoretically obtained. The experiment showed even higher values, due to delamination of the less than 500 nm thick Cu metallization, which had been plated by PVD on chip level.

Reiner et al. investigated the impact of the via diameter on the thermal resistance of a GaN power IC that was embedded by the Double-side-Microvia process (Reiner et al., 2018). At fixed pitch, an increasing via diameter reduces the thermal resistance. Vias with 50 μm diameter showed a thermal resistance of 3.7 K/W, which decreased to 1.1 K/W with a via diameter of 100 μm.

A further improvement of the microvia density was proposed by Perrin et al. (2021). After drilling and plating a first set of vias, a second set was placed in the unplated regions between the already established vias. A complete bulk contact, generated in four iterations, helped to reduce the thermal resistance of the package by 32%, compared to a conventional structure with only one set of microvias.

2.3.3. Thermomechanical stresses

Heterogenous materials with dissimilar CTE introduce thermomechanical stresses in any kind of package. These stresses can cause yield issues in fabrication, e.g. due to chip fracture (Bohm et al., 2004), or limit the lifetime due to fatigue. In conventional packages, bond wire lift-off and die-attach delamination are the predominant failure modes caused by thermomechanical stresses (Lutz et al., 2018).

PCB-embedded packages contain either Si or SiC semiconductor chips, which are often attached to a Cu layer and encapsulated by a dielectric laminate, such as FR4. The relevant material properties are listed in Table 1. As the circuit board materials FR4 and Cu have closely matched CTE, however, the semiconductor materials are strongly mismatched. Mechanical stresses are introduced during assembly of the components at elevated temperatures (Pletz et al., 2011). Die-attach is usually performed either by adhesive bonding (Tang et al., 2021), soldering (Guyenot et al., 2017), Ag sintering (Kearney et al., 2017), or transient liquid phase bonding (Gottwald & Roessle, 2018). Except for adhesive bonding, which is a low-temperature process, all other die-attach techniques require process temperatures in the range of

Table 1
Material properties relevant for thermomechanical stresses in PCB embedded packages.

Material	E GPa	CTE ppm/K	k W/mK	Reference
Semiconductor				(Pavliček et al., 2022)
Si	170	2.6	130	
SiC	410	4.0	450	
Die attach				(Duch et al., 2017)
Ag-sinter (pressure assisted)	50	19	200	
Ag-sinter (pressureless)	25	19	100	
SnAg3.5 Solder	30	25-30	20-50	
Circuit board				
FR4 (Isola 370H)	25.8/21.9*	13/14* (45)**	0.4	(Isola Group, 2022)
Cu-EPT	127	17.7	390	(Wieland, 2021)

* lengthwise / crosswise direction.
** z-direction.

230°C to 260°C. Cooling down to room temperature will introduce significant stresses. Subsequent lamination of the dielectrics, performed at 180°C to 200°C, contributes to the overall stress profile in the package. These stresses can cause spontaneous chip fracture. Several authors report horizontal cracks, either after die-attach (Otto et al., 2018) or after embedding (Randoll et al., 2015; Zhang et al., 2013). Crack formation is explained as follows: Due to its lower CTE, the semiconductor die experiences in-plane compressive stress. Transverse contraction (Poisson's ratio) induces tensile stress in the z-direction (Kasem & Feinstein, 1987). Surface flaws on the chip edge, which are caused by the dicing process, trigger the formation of horizontal cracks (Ranjan et al., 1998). Prediction of the fracture probability requires statistical methods (Bohm et al., 2004; Bohm et al., 2004; Hauck et al., 2005). The result is strongly influenced by the chip geometry, the surface quality (Zhao et al., 2008), and the structure of the metallization (Deluca et al., 2011).

2.4. Unconventional embedding processes

Besides the mainstream PCB embedding process, the scientific literature discusses different alternative approaches, often developed by academia.

One example is the SiC half-bridge power module developed by Feix et al. (Feix et al., 2015). The process technology is based on the Chip-on-Substrate process using an Aluminum-Nitride DCB. However, the high-side switch of the half-bridge is attached as flip-chip face down to the substrate, while the low-side switch is attached face up, see Fig. 5 (a). That way, the commutation loop inductance can be minimized by placing primary DC link capacitors directly on top. Moreover, the output capacitance is significantly reduced, as the output potential is located only on the first PCB layer and cannot form a parasitic capacitance to ground potential.

Regnat et al. developed the power chip on chip (PCOC) module, where the embedded high side and low side switches are stacked on top of each other (Regnat et al., 2015; Regnat et al., 2018). The concept is based on the Double-side Microvia embedding process. Additional layers for routing of the Kelvin contacts, gate and power contacts are added by sequential lamination steps. That way, two quasi-identical submodules are generated. As illustrated in Fig. 5 (b), both parts are laminated using a thermally and electrically conductive prepreg to generate the stacked half-bridge. As each switch contains 4 SiC MOSFET in parallel, special care is taken to symmetrize the impedance of all switches. Therefore, SMD decoupling capacitors are attached on the sidewall of the module between DC+ and DC- potential. The main advantage of this concept is

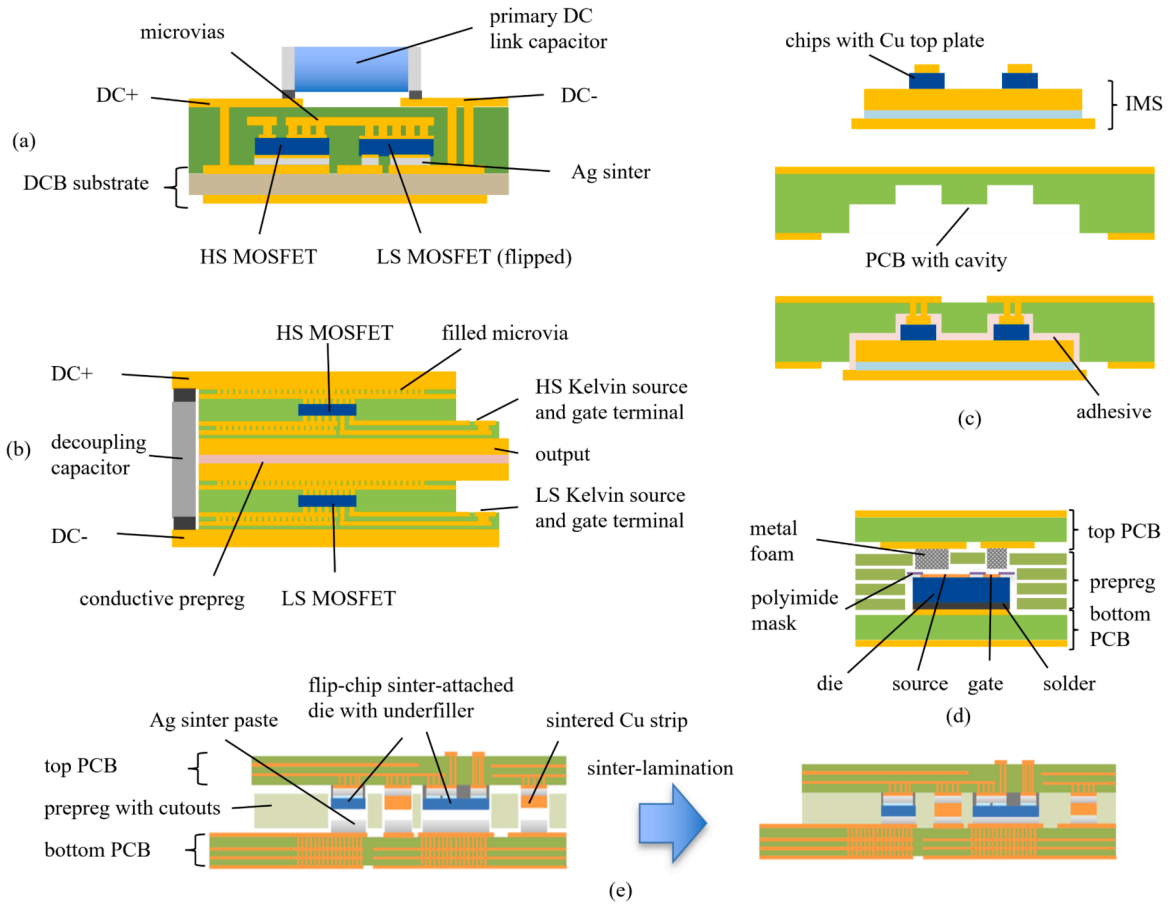

Fig. 5. Illustration of alternative embedding concepts: (a) half-bridge module with one semiconductor is attached face up, the second face down on a DBC substrate, adopted from (Feix et al., 2015), (b) 3D stacked half bridge adopted from (Regnat et al., 2015), (c) embedding by adhesive bonding, adopted from (Sharma et al., 2018), (d) metal foam top side contacts, adopted from (Pascal et al., 2018), (e) double side sinter contacts, adopted from (Polezhaev et al., 2019) .

the extremely low stray inductance. A mock-up, where the semiconductors have been replaced with vias to create a short circuit, has been used for an impedance measurement. Based on this measurement, a power loop inductance of 0.23 nH was estimated.

To avoid handling of bare dies in the PCB production line, Sharma et al. developed a special process where embedding is performed by adhesive bonding (Sharma et al., 2016; Sharma et al., 2018). The concept is outlined in Fig. 5 (c). In a first step, the PCB supplier fabricates a semi-ready circuit board with machined cavities. The semiconductor supplier assembles the chips to an IMS substrate. To embed the semiconductors both parts are bonded together with a silicone adhesive. The board is sent back to the PCB line, where the chips are contacted by plated microvia and the top trace is structured. Another unique feature of this approach is the top side contact of the semiconductor. First, the standard Al metallization is modified by electroless plating of a Ni/Au layer. This surface finish allows soldering or sintering of a Cu plate on the chip metallization, similar to the *Danfoss Bond Buffer* (Rudzki et al., 2014) or the *Hereaus Die Top System* (Heraeus Electronics, 2022). Due to the thickness of the Cu interposer, mechanical drilling is applied for the fabrication of the plated contact via.

As discussed above, mainstream PCB embedding processes require a copper metallization on the chip, which is not standard. To enable embedding of power devices with standard Al metallization, top contacts based on pressed metal foam have been developed by Pascal et al. (Bensebaa et al., 2020; Pascal et al., 2017; Pascal et al., 2018). Fig. 5 (d) shows the fabrication process: First, the chip is soldered to a PCB substrate. Then, prepregs with cutouts for the chip are placed on top, followed by a polyimide mask with openings for the chip contact pads. Additional prepreg layers, with cutouts are stacked on top. Metal foam pads are inserted into these cutouts. Last a second PCB is placed on top and the entire stack is vacuum laminated. The electrical contact between chip and top PCB is established by the pressed nickel foam, which is kept in place by the resin from the prepregs. The reliability of the contact was tested by passive thermal cycles, current surges, and repetitive short-circuits. Some of the samples performed as good as wire-bonded contacts, indicating the potential of the technology.

Another novel interconnection technology for top and bottom side interconnection was investigated by Djuric et al. (2019). The interconnection is based on Cu nano-wires which are generated on an electroplated Cu mesa structure. The assembly of the die in the PCB stack is performed in a single lamination step, where a permanent contact between the nano-wires and the chip metallization is formed by thermocompression bonding. The authors report an electrical resistance in the range of 200 μΩ to 400 μΩ, depending on the temperature.

Polezhaev et al. investigated an embedding process, where the semiconductors are sandwiched between two PCB (Polezhaev et al., 2019). As shown in Fig. 5 (e), the semiconductors and Cu strips are flip-chip attached by Ag sintering to the top board. An underfill is applied for mechanical support of the chips. Sinter paste is stencil-printed to the chip land pad on the bottom PCB. The top PCB is placed face down on the bottom PCB with a prepreg in between. Bonding is performed by combined Ag sintering of the chip contacts and lamination of the prepreg on the remaining area. The key challenge was to find a process window acceptable for lamination and sintering. An Ag paste for pressure-less sintering and special prepreg based on benzoxazine resin were required. The authors report successful operation of a

demonstrator in double-pulse testing.

A similar fabrication concept with IMS instead of PCBs for the top and bottom substrate has been investigated by Tablati et al. (2020). A MOSFET with 1.75 mΩ on-state resistance was used for a technology demonstrator. However, an increased resistance of 6.7 mΩ was observed after assembly, which, according to the authors, may indicate a poor sinter contact.

3. Materials

The dielectric materials play a crucial role for PCB embedding and are available in various forms, such as a core, resin-coated copper RCC, sheet material, or pre-impregnated glass-fiber fabrics (prepregs). Core materials are copper cladded laminates with fully cured dielectrics and are used as a basis for most circuit boards. Multilayer boards are fabricated by adding more copper layers with RCC, sheet material, or prepreg, which all contain partially cured resin that acts as adhesive and dielectric. Sheet materials contain resin and filler particles, while prepregs additionally contain a glass fiber fabric. RCC are sheet materials applied to a Cu foil. Material suppliers provide a large range of products, which differ in resin formulation and filler composition. To choose the right material for PCB embedding, an understanding of the material properties and the requirements is indispensable. The next subsections detail the material requirements and present some selected materials.

3.1. Material requirement

Thermal, mechanical, electrical, and fabrication-related properties need to be considered when selecting any embedding material (Kröner, 2021).

Material datasheets specify the glass transition temperature, the decomposition temperature, and the time to delamination at 260°C and 288°C as specified in IPC-TM-650 (IPC TM-650). The glass transition temperature of a resin is typically considered as the upper limit and should not be exceeded during the operation of the device. In embedded packages, the material is in direct contact with the semiconductor die, which may be operated with a junction temperature of 175°C, in case of state-of-the-art devices, and may exceed 200°C with the future SiC devices (Schuderer et al., 2014). The heat losses are transferred to a heat sink through an electrically insulating material on the bottom side, see Fig. 4 (b). These materials need to provide a high thermal conductivity, combined with good electrical insulation. Typically, different materials, optimized for each purpose, are chosen for embedding on the top side and for isolation on the bottom side.

The breakdown voltage and dielectric strength are material properties relevant for the insulation performance. Typical organic isolators have a dielectric strength in the range of 40…50 kV/mm. However, long-term stability over the entire lifetime of the system is of concern. Conductive anodic filament (CAF) growth is a known issue that might lead to insulation failure in PCB materials (Randoll, 2018). Under temperature, humidity, and voltage bias, electrochemical reactions generate a conductive Cu path along glass fibers and can ultimately cause a short circuit. CAF depends on many factors, which are hard to quantify. Therefore, material suppliers simply grade the materials as "CAF resistant" after passing a standardized test procedure according to IPC-TM 650 method 2.6.25 (IPC TM-650).

Important mechanical properties are the coefficient of thermal expansion and the Young's modulus. These are responsible for mechanical stresses in the package as described in Section 2.3.3. The x and y-direction CTE (in-plane) causes stresses on the semiconductor die. The z-axis CTE (cross-plane) should match Cu (17.7 ppm/K) to limit axial stresses on the microvia.

Materials properties related to processing are also of concern. The resin must fill voids in the embedding stack. This requires a good resin flow during the lamination process. Generally, filler particles have a negative impact on the flow properties but are required to enhance thermal conductivity and to reduce the CTE. Moreover, a high filler content may have a negative impact on machining of vias by means of mechanical tools or laser. Although important for material selection, these properties are not quantified in datasheets and therefore material selection requires some experience.

3.2. Selected materials

Although many scientific publications deal with PCB embedding, detailed information on material choice is rare. Only few publications explicitly mention the manufacturer and material type that was used in the study. Table 2 lists materials that have been explicitly named in publications. The respective references are cited in the table, together with the data source for the material properties. The list includes epoxy-based materials with a glass transition temperature of 175°C and 180°C. These materials have an in-plane CTE in the range of 13…15 ppm/K and a low thermal conductivity, which indicates a low filler content and good flowability during processing. The adhesion to Cu is larger than 1 N/mm and the moisture absorption is below 0.2%. Higher glass transition temperatures are found in materials based on benzoxazine (200°C), polyimide-blend (280°C), and bismaleimide-triazine (300°C). The latter two are materials used as substrates in microelectronics packaging, and therefore have an extremely low CTE (3…5 ppm/K). Compared to the standard epoxy-based materials, they show a higher moisture absorption and a lower peel strength.

Table 3 lists thermally conductive dielectrics for the bottom-side isolation of the embedded package, as indicated in Fig. 4 (b). The list includes a standard epoxy-based prepreg material with thermal conductivity of 0.4 W/mK and an epoxy-based prepreg with enhanced thermal conductivity of 1.3 W/mK. To improve the thermal conductivity, ceramic filler particles are added to the resin. However, a high filler content has a negative impact on the flowability of the resin during processing. Therefore, the use of these materials is limited to geometries that have a low free volume. Materials with a thermal conductivity exceeding 2 W/mK are available from isolated metal substrate (IMS) technology. These are highly filled resin sheet materials without glass fiber fabric.

4. Demonstrators

PCB embedded power semiconductors have been described in many scientific papers over the past decade. Table 4 shows a brief but comprehensive list of various research demonstrators in chronological order. The list includes both, simple technology demonstrators that have only been used for switch-level testing and converter-level demonstrators for dedicated application scenarios. They cover all types of integration concepts, such as PCB-embedded power modules, intelligent power modules, and System-in-Board solutions. In some cases, a rigorous classification was difficult and additional information was added to the integration concept. The next columns give details on the embedding process technology. Information on the substrate, bottom-side chip connection (die-attach) and top-side connection, and electrical isolation are shown in the subsequent section of the table. The last two columns list the application cases, where communicated by the authors, and comments on unique features or further details on the demonstrator.

Table 5 lists the same demonstrators and provides technical details, such as topology, chip type and ratings, number of parallel chips in the demonstrator, and the key performance indicators stray inductance and thermal resistance. The table includes 22 demonstrators (12 × half-bridge topology, 6 × B6 bridge, 2 × Full-bridge, 2 × 3-level T-type phase legs). All common types of power semiconductors, Si IGBT, Diodes and MOSFET, SiC MOSFET, and GaN HEMT, have been applied. The rated blocking voltages are mostly 650 V or 1200 V with only two exceptions in the 100 V range. The stray inductance L_σ of the commutation loop has been disclosed for 11 demonstrators. The lowest inductance (0.23 nH)

Table 2
Selected dielectric materials for PCB embedding and their relevant material properties.

	Manufacturer			Isola	Panasonic	Isola	Showa Denko (Hitachi)	Mitsubishi
	Material			PCL370HR	R1566S / R1551S	IS550H	MCL-E-795G	CCL-HL832NSF
General	References			(Stahr et al., 2016)	(Sharma et al., 2018; Stahr et al., 2016)	(Guyenot et al., 2017; Polezhaev et al., 2019; Guyenot et al., 2018)	(Kröner, 2021)	(Hou et al., 2019; Zhang et al., 2013)
	Data source			(Isola , 2022)	(Panasonic, 2022)	(Isola, 2021)	(Showa Denko Materials, 2021)	(Mitsubishi, 2022)
	Chemistry			Epoxy	Epoxy	Benzoxazine	Polyimid-blend	Bismaleimide-triazine
Thermal	Glass Transition Temperature (T_g)	DSC	°C	180	175	200	280	300
	Decomposition Temperature (T_d)	weight loss	°C	340	355	400	480	
	Z-Axis CTE	below T_g	ppm/K	45	40	38	10…15	
		above T_g	ppm/K	230	180	210	70…100	
	X/Y-Axis CTE	below T_g	ppm/K	13/14	11-13/13-15	13-17	4	5/3
	Thermal Conductivity		W/mK	0.4		0.7	0.65	0.7
Electrical	Permittivity (D_k)	1 GHz		4.17	4.7	4.5	4.4	4.4
	Loss tangent (D_f)	1 GHz		0.0161	0.011	0.014	0.006	0.008
	Dielectric Breakdown		kV	>50		60		
	Electric strength		kV/mm	54		46,9		
	Comparative Tracking Index (CTI)		Class (Volts)	3 (175-249)		3		
Physical	Peel strength		N/mm	1.25	1.6	1.45	0.8	0.8
	Flexural strength	length direction	MPa	620		419		510
	Flexural modulus	length direction	GPa				36	32
	Moisture absorption		%	0.15	0.18	0.25	0.5	0.35

Table 3
Selected thermally conductive dielectric materials for PCB embedding.

	Manufacturer			Isola	Panasonic	Laird	Aismalibar
	Material			PCL370HR	E-Cool R14-T1	TLAM SS HTD	COBRITHERM HTC
General	References			(Stahr et al., 2016)	(Sharma et al., 2018; Stahr et al., 2016)	(Stahr et al., 2016)	(Stahr et al., 2016)
	Data source			(Isola, 2022)	(Panasonic E-Cool, 2022)	(Laird technologies, 2011)	(Aismalibar, 2021)
	Chemistry			Epoxy	Epoxy	Proprietary	Proprietary
Thermal	Glass Transition Temperature (T_g)	DSC	°C	180	148	168	120
	Decomposition Temperature (T_d)	weight loss	°C	340	350		
	Z-Axis CTE	below T_g	ppm/K	45	24		
		above T_g	ppm/K	230	150		
	X/Y-Axis CTE	below T_g	ppm/K	13/14	19-21		
	Thermal Conductivity		W/mK	0.4	1.3	2.2	3.2
Electrical	Permittivity (D_k)	1 GHz		4.17	5.7		5.2
	Loss tangent (D_f)	1 GHz		0.0161	0.018		0.015
	Dielectric Breakdown		kV	>50			
	Electric Strength		kV/mm	54	57	39.3	54
	Comparative Tracking Index (CTI)		Class (Volts)	3 (175-249)	(>600)	(>600)	(>600)
Physical	Peel Strength		N/mm	1.25	1.1	1.25	2.8
	Flexural Strength	length direction	MPa	620	230	142	
	Flexural Modulus	length direction	GPa				
	Moisture Absorption		%	0.15	0.2		

was reported for the 3-dimensionally stacked PCOC concept, as detailed in Section 2.4 (Regnat et al., 2015). For half-bridges with GaN HEMT, stray inductances in the range of 0.5 nH have been reported (Dechant et al., 2019; Qi et al., 2022; Savulak et al., 2018). To achieve such values, a primary DC link capacitor must be placed directly on top of the embedded semiconductors. The GaN devices profit from their lateral structure, as the vertical current loop can be minimized. Vertical devices lead to higher stray inductance values, typically in the range of 1 nH to 2 nH. (Klein et al., 2019; Knoll et al., 2021; Marczok et al., 2020; Neeb et al., 2014).

In real-world applications, the current-carrying capability of power semiconductors is limited by the thermal performance of the package and the cooling system. A performance indicator is the thermal resistance, which is proportional to the temperature difference between the

Table 4
List of lab scale demonstrators with details on the embedding technology.

Publication	Year	Institution / Project	Integration concept	Technology				Application	Comment
				Substrate	Die attach	Isolation	top side contact		
(Hoene et al., 2013; Hoene et al., 2014)	2013	Fraunhofer - IZM	Power module with primary DC link	Al_2O_3 DBC	Ag sinter	Al_2O_3	Au stud bump + plating		Pick-up coil current sensor with tube shunt
(Neeb et al., 2014; Neeb, 2018)	2014	RWTH / HiLEVEL-Project	Power module	Cu leadframe	Ag sinter	TC prepreg	microvia	50 kW automotive power module	
(Feix et al., 2015)	2015	Fraunhofer - IZM	Power module with integrated gate booster and primary DC link	AlN DBC	Ag sinter	AlN	microvia		One chip attached face up, second chip attached face down on substrate
(Regnat et al., 2015)	2015	Uni. Grenoble / Mitsubishi	Power module with primary DC link	none	microvia	none	microvia	1200V / 80 A power module	Power Chip on Chip - 4 dies parallel, decoupling capacitors soldered to board edges
(Sharma et al., 2016)	2016	UAS Kempten	Power module	Cu-IMS	solder	TC prepreg	soldered Cu top plate + microvia		Embedding by adhesive bonding
(Wyss & Biela, 2016)	2016	ETHZ	Intelligent power module (IPM)	Cu leadframe with cavity	Ag sinter	TC prepreg	microvia	30 kW boost PFC converter	Schweizer Smart p^2 Pack technology
(Stahr et al., 2016; Nicolics et al., 2017)	2016	AT&S EmPower Project	Power module with primary DC link	none	plated CU	dielectric 8W/mK	microvia	500 W, 48 V, 20 A MOSFET B6 bridge for BLDC motor	unisolated power core with ims sinterlaminated to top and bottom side
(Loher et al., 2016)	2016	Fraunhofer - IZM	Power module	Cu-IMS	Ag sinter	TC prepreg 3.2W/mK	microvia	2.3 kW PV inverter	
(Loher et al., 2016)	2016	Fraunhofer - IZM	Power module	Cu-IMS	Ag sinter	TC prepreg 3.2W/mK	microvia	10 kW inverter for motor drive	
(Hensler et al., 2017)	2017	Siemens	System-in-Board					Industrial motor drive dual 3-level (t-type) topology	2 × 27 kW, power density 17.2 kW/l, efficiency 99.2%
(Kearney et al., 2017)	2017	ABB	Power module	Cu leadframe with cavity	Ag sinter	TC prepreg	microvia	B6 Bridge module	Schweizer Smart p^2 Pack technology Cr/Cu 5nm/8µm sputtered on chip
(Sharma et al., 2018)	2018	UAS Kempten	Intelligent power module (IPM)	IMS	Ag sinter	TC prepreg	sintered Cu top plate + microvia		Embedding by adhesive bonding
(Savulak et al., 2018)	2018	United Technologies Research Center	System-in-board	none	microvia plating		microvia	5 kW inverter	AT&S ECP fabrication
(Caillaud et al., 2019)	2019	Uni Lyon / Mitsubishi	System-in-board	thin Cu	adhesive bonding + microvia and plating	TIM	microvia	EV onboard charger	Converter fully embedded (including gate drivers and passive components) Three layers (power, gate driver, Inductor) stacked
(Dechant et al., 2019)	2019	TH Rosenheim	Intelligent power module (IPM)	thin Cu	adhesive bonding + microvia and plating	external isolation with AlN plate	microvia		Würth Electronic *MICROVIA.embedding*
(Polezhaev et al., 2019)	2019	UAS Kempten	Power module	PCB	Ag sinter	TIM	sinter-lamination		Assembly by sinter-lamination
(Klein et al., 2019)	2019	Fraunhofer - IZM	Intelligent power module (IPM)	Cu	Ag sinter	dielectic 1.4W/mK	microvia	industrial inverter 100 kW	
(Marczok et al., 100, 2020)	2020	SiC-Modul project	Intelligent power module (IPM)	Cu leadframe with cavity	Ag sinter	TC prepreg 4,3W/mK	microvia	90 kW 6-phase integrated motor drive	Schweizer Smart p^2 Pack technology
(Sharma et al., 2020)	2020	UAS Kempten	Intelligent power module (IPM)	Cu leadframe	Ag sinter	dielectric coolant	sintered Cu top plate + microvia		Module isolation by dielectric liquid coolant
(Hou et al., 2018; Hou et al., 2020)	2020	TU Delft / Chinese Academy of Science	Power module	none	none	TIM	PVD + Cu plating		No Cu metallization required
	2021					TIM	microvia		

(*continued on next page*)

Table 4 (*continued*)

Publication	Year	Institution / Project	Integration concept	Technology				Application	Comment
				Substrate	Die attach	Isolation	top side contact		
(Sharma et al., 2021; Koch et al., 2021, Ghebreslassie et al., 2022)		UAS Kempten / Uni Stuttgart	Intelligent power module (IPM)	Cu leadframe	pressureless Ag sintering			48 V DC/DC converter	PCB based prepackages attached to system board
(Knoll et al., 2021)	2021	CPES	Intelligent power module (IPM)	none	microvia	TIM	microvia	22 kW AC-DC converter for EV On-board-charger	AT&S PARSEC technology
(Qi et al., 2022)	2022	Xi'an Jiaton University	Intelligent power module (IPM)	none	microvia	TIM	microvia		

chip junction and the package case ($R_{th,jc}$), the heat sink ($R_{th,jhs}$), the ambient temperature ($R_{th,ja}$), or cooling fluid temperature ($R_{th,jf}$). Moreover, the heat flow density, and hence the chip footprint area has a strong impact on the thermal resistance. To compare the thermal performance of packaging technologies with different chip sizes, the area-independent thermal resistance $R_{th} \times A_{chip}$ provides a good measure. This property is listed in the last column of Table 5. Typical values for the area-independent junction to heat sink thermal resistance are in the range of 20…30 mm^{2}K/W (Hensler et al., 2017; Kearney et al., 2017; Klein et al., 2019; Wyss & Biela, 2016). Lower values were achieved by double side cooling (18.6 mm^{2}K/W) (Nicolics et al., 2017), direct liquid cooling (9.6mm^{2}K/W) (Birkhold et al.). The lowest reported values (3.3 mm^{2}K/W and 5.3 mm^{2}K/W) do not include electrical insulation (Knoll et al., 2021; Qi et al., 2022).

5. Reliability

Reliability is mandatory for any electronics packaging technology. To verify reliability, endurance tests according to application-specific standards must be performed and passed. The automotive qualification guideline AQG324, formally known as LV324, is an example of such a standard, relevant for power modules in automotive drivetrains (ECPE 2021). The standard describes test methods that qualify the power module for the application environment and for lifetime testing. The individual test methods aim to trigger certain well-known failure modes and require passing a defined minimum acceptance criterium. As e-mobility presents a target application for PCB embedding, AQG324 provides a good basis for initial reliability testing. However, new failure modes might be more relevant in PCB-embedded packages and may require additional test methods (Randoll, 2018). The following subsections cover investigations on the thermomechanically induced failures and on the insulation behavior.

5.1. Thermomechanical reliability

A numerical study on the reliability of an embedded MOSFET package was carried out by Yang et al. (Yang et al., 2009). Based on finite element method (FEM) simulations, the authors located critical thermomechanical stresses in an embedded MOSFET package. These stresses could trigger the following failure modes:

(1) Chip cracking during fabrication, as discussed in Section 2.3.3.
(2) Cracking or delamination of the Cu vias
(3) Delamination of the Cu chip metallization

A graphical representation of the failure modes in a schematic cross-section is shown in Fig. 6. Additionally, laminate fracture and die-attach delamination are included.

Experimental testing requires either passive temperature cycles, using temperature-shock-chambers, or active load cycles, where the semiconductor is periodically heated by current pulses (Lutz et al., 2018).

Laminate cracking was observed by Munding et al. after passive temperature cycling (-55 to 150°C) on samples with RCC as embedding material (Munding et al., 2017). However, no cracks occurred when prepregs were used for embedding instead. The prepreg glass fibers improved the mechanical strength of the dielectric material. Pavliček et al. observed delamination of the sinter die-attach in a PCB-prepackage with SiC die after 500 thermocycles (-50 to 150°C) (Pavliček et al., 2022). Similar observations were made by Birkhold et. al. after 1000 cycles at -40 to 200°C (Birkhold et al., 2020). In the same study, delamination of vias and fracture of the metallization were reported. The via delamination results from axial stresses caused by the difference in CTE between the embedding materials and the plated Cu via. FR4 materials have a z-axis CTE in the range of 40 ppm/K, compared to 17.7 ppm/K for Cu, see Table 1. Due to the conical shape of the microvia, the fracture occurs at the foot, where the cross-sectional area is minimal. Cracking in the chip metallization results from the CTE difference between the metal and the semiconductor die. Often, Cu is plated on top of the native Al metallization. The tensile strength of Al is significantly lower than Cu. Therefore, cracks are found predominantly in the Al layer.

The results of active load cycling tests are summarized in Fig. 7. The graph shows the temperature amplitude versus the number of cycles to failure. For benchmarking, the results of a conventional DBC-based, wire-bonded power module are indicated by a blue line. Kearney et al. performed tests with one set of embedded IGBT modules, which were first cycled with a temperature difference of 42 K for 1 million cycles. Then the same samples were cycled at 62 K for almost 2 million more cycles before increasing the temperature difference. The test was aborted after 400.000 cycles at 90 K without any failure (Kearney et al., 2017). Therefore, the results in the diagram represent a lower limit, which is indicated with an arrow and question mark above the horizontal bar. Randoll et al. performed a power cycling test on an IGBT module with ΔT=80 K, which was aborted after 370.000 cycles without failure (Randoll, 2018; Randoll et al., 2015). Stahr et. al. did not observe any failure of a MOSFET module in up to 300.000 cycles at ΔT=125 K (Stahr, 2021; Stahr & Morianz, 2019). A critical increase in thermal resistance was observed by Guyenot on a MOSFET module after 600.000 cycles at ΔT=120 K (Guyenot et al., 2017). Solder die-attach delamination was the root cause for the failure. Dechnat et. al. report via delamination on a GaN HEMT after 220.000 cycles at 120°C (Dechant et al., 2019). Gottwald et. al. report a test campaign with a larger (not quantified) number of samples of SiC modules (Gottwald et al., 2022). To highlight the potential of the technology, they show in their publication the highest number of cycles to failure. These values represent an upper boundary in that case. Compared to conventional wire-bonded power modules, all reported results for embedded modules indicate a

Table 5
Key performance numbers of lab-scale demonstrators.

Reference	Year	Institution / Project	Topology	Semiconductor		dies parallel	Voltage (V)	Current (A)	Foot-print (mm^2)	L_σ (nH)	Thermal resistance Rth		$R_{th} \times A_{chip}$ (mm^2K/W)
(Hoene et al., 2013; Hoene et al., 2014)	2013	Fraunhofer - IZM	Half-Bridge	SiC	JFET	1	1200			0.57[a]			
(Neeb et al., 2014; Neeb, 2018)	2014	RWTH / HiLEVEL-Project	B6 bridge	Si	IGBT/ Diode	3	600	200	99.5	1.5[b]	j-a	0.45[e]	44.8
(Feix et al., 2015)	2015	Fraunhofer - IZM	Half-Bridge	SiC									
(Regnat et al., 2015)	2015	Uni. Grenoble / Mitsubishi	Half-Bridge	SiC	MOSFET	4	1200	36	10.4	0.23[c]			
(Sharma et al., 2016)	2016	UAS Kempten	Half-Bridge	Si	IGBT	1	1200	25	42.9		j-c	0.87[e]	37.3
(Wyss & Biela, 2016)	2016	ETHZ	3-level T-type	IGBT	IGBT/ Diode	1	1200	50	49.6	4.5[b]	j-hs	0.4[e]	19.8
(Stahr et al., 2016; Nicolics et al., 2017)	2016	AT&S EmPower Project	B6 Bridge	Si	MOSFET	1	100	110	12.6		j-hs	1.48[e,f]	18.6
(Loher et al., 2016)	2016	Fraunhofer - IZM		SiC	JFET		650						
(Loher et al., 2016)	2016	Fraunhofer - IZM	Half-Bridge	Si	IGBT/ Diode								
(Hensler et al., 2017)	2017	Siemens	3-level T-type	SiC	MOSFET	1	1200	75	24.0		j-hs	0.95[e]	22.8
(Kearney et al., 2017)	2017	ABB	B6 Bridge	Si	IGBT/ Diode	1	1200	25	42.9		j-hs	0.56[e]	24.0
(Sharma et al., 2018)	2018	UAS Kempten	B6 Bridge	Si	IGBT	1	1200	50	82.8		j-c	0.21[e]	17.1
(Savulak et al., 2018)	2018	United Technologies Research Center	2x B6 Bridge	GaN	HEMT	1	650	30		0.43[d]			
(Caillaud et al., 2019)	2019	Uni Lyon / Mitsubishi	Full-Bridge	SiC	MOSFET	1	1200	32	10.4				
(Dechant et al., 2019)	2019	TH Rosenheim	Half-Bridge	GaN	HEMT	1	650	30	12.8	0.55[a]	j-hs	1.32[e]	16.8
(Polezhaev et al., 2019)	2019	UAS Kempten	Half-Bridge	Si	IGBT	1	650	50	14.0		j-c	2.06[d]	28.9
(Klein et al., 2019)	2019	Fraunhofer - IZM	Half-Bridge	SiC	MOSFET	1	1200	81	26.0	0.97	j-hs	1.15[d]	29.9
(Marczok et al., 100, 2020)	2020	SiC-Modul project	Half-Bridge	SiC	MOSFET	2	1200	80	12.0	1.7[a]	j-f	0.8[d]	9.6
(Sharma et al., 2020)	2020	UAS Kempten	B6 Bridge	Si	IGBT	1	1200	50	82.8		j-f	0.43[e,g]	35.6
(Hou et al., 2018; Hou et al., 2020)	2020	TU Delft / Chinese Academy of Science	Half-Bridge	SiC	MOSFET	1	1200	36	10.4				
(Sharma et al., 2021; Koch et al., 2021, Ghebreslassie et al., 2022)	2021	UAS Kempten / Uni Stuttgart	Half-Bridge	GaN	HEMT	2	100	100	11.2	1.7[d]	j-a	1.7[e]	19.1
(Knoll et al., 2021)	2021	CPES Virginia Tech	Half-Bridge	SiC	MOSFET	1	1200	60	27.1	2.3[d]	j-c	0.12[e,f,j]	3.3
(Qi et al., 2022)	2022	Xi'an Jiaton Univeristy	Full-Bridge	GaN	HEMT	1	650	30	12.7	0.55[a]	j-c	0.42[d,j]	5.3

[a] calculated from measured resonance frequency.
[b] calculated by turn-on voltage in dip.
[c] impedance measurement on mock-up.
[d] simulation.
[e] measurement.
[f] double-side cooling.
[g] transformer oil coolant.
[j] non-isolated.

clear improvement of the load cycling capability.

5.2. Isolation behavior

Fig. 8 illustrates the cross section of a generic PCB-embedded power module. Dielectric breakdown may occur in locations with high electric field strength. These are found on the chip top side, where the full operation voltage is applied between central contact pads and the guard ring. A second critical location is the bottom side isolation, as the thermal contact pad is typically connected to GND potential.

5.2.1. Bottom side insulation

The isolation behavior of thermally conductive prepreg materials was investigated by Randoll (Randoll, 2018; Randoll et al., 2014). Material samples with square electrodes on the top and the bottom were used for partial discharge testing. The thesis reports the partial discharge extinction voltage (PDEV) in the temperature range of 25°C to 175°C. A PDEV in the range of 4.0 to 7.0 V is obtained up to the glass transition temperature of 150°C. At 175°C PDEV decreases to 1.5 kV. Therefore, embedding materials should not exceed Tg during operation, when high voltages are applied.

Kearney et al. used a 1200 V IGBT module with 130μm thick

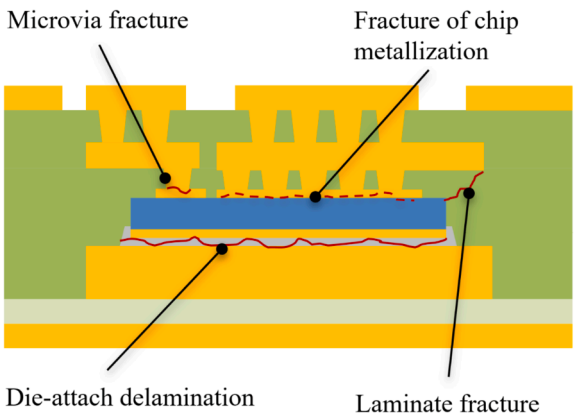

Fig. 6. Illustration of failure modes in PCB embedded packages under thermomechanical stresses.

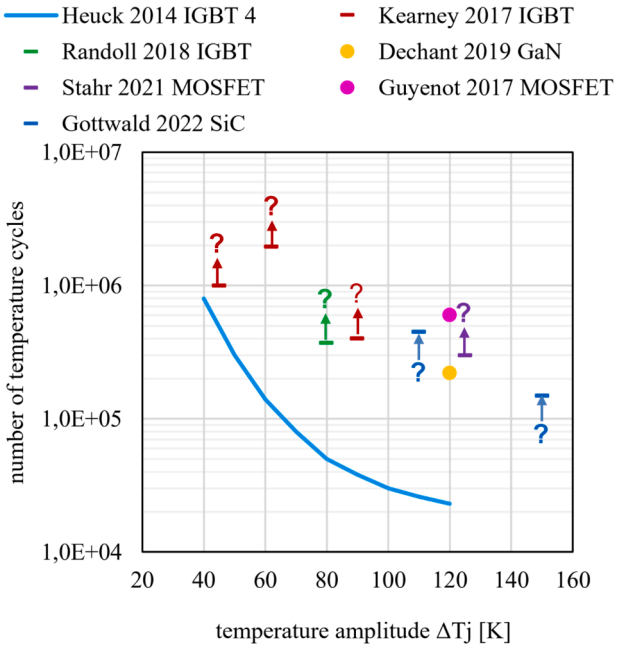

Fig. 7. Active load cycling results of PCB embedded power semiconductors taken from literature (Stahr, 2021; Randoll, 2018; Guyenot et al., 2017; Kearney et al., 2017; Dechant et al., 2019; Gottwald et al., 2022). A round mark indicates a failure. The horizontal bar with an arrow above indicates that the test was aborted before a failure occurred and presents a lower limit. The horizontal bar with arrow below indicates that several samples have failed, and the highest number of cycles is reported, which presents an upper limit. The blue line indicates the power cycling capability of a conventional wire-bonded power module, data taken from (Heuck et al., 2014).

insulation layer for evaluation of the bottom side insulation (Kearney et al., 2017). Dielectric strength and partial discharge inception voltage (PDIV) were measured in initial state and after ageing by 500 thermocycles -40°C to 150°C. The initial samples showed a breakdown voltage between 5.3 kV and 6.5 kV, and a PDIV in the range of 4.7 kV. After ageing, the breakdown voltage decreased to 4.2 kV to 4.7 kV, and the PDIV to 3.5*V* to 4.1 kV. Long term ageing experiments were conducted with a test voltage of 2.5kV at 90°C. From the results, a useful lifetime of 15 to 30 years is extrapolated.

5.2.1. Top side insulation

Dechant et al. studied the dielectric strength of an embedded 650 V GaN HEMT (Dechant et al., 2019). Both the source and the drain contact

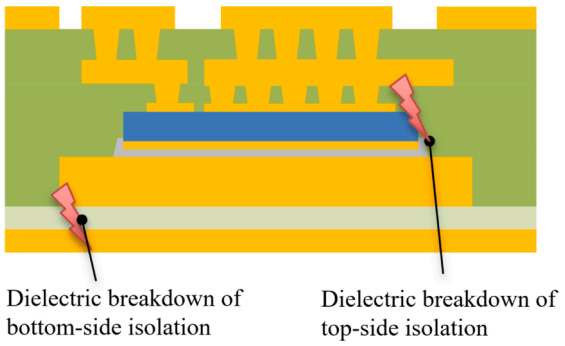

Fig. 8. Illustration of locations of dielectric breakdown in PCB embedded packages.

were located on the top side of the chip and formed an interdigital structure. A first package routing layer was placed on top, separated by a 100 μm thick dielectric, which needed to withstand the full blocking voltage of the chip. A characteristic breakdown voltage of 14.7 kV was reported, when tested at 25°C. However, this value strongly degraded at higher temperatures. A decrease of 77% was measured at 125°C. In contrast to that, high-temperature storage leads to an increase in room-temperature breakdown voltage. This effect can be explained by a densification process in the resin, which leads to recovery of initial flaws. The densification process ends after about 2000 h of high temperature storage. Further high temperature exposure is expected to degrade the breakdown strength, due to ageing of the resin.

Link et al. performed high-humidity-high-temperature-reverse-bias (H3TRB) tests on embedded 1200 V diodes. The samples were exposed for 1000 h to 85°C temperature, 85% relative humidity and a voltage bias of 960 V, which equals 80% of the nominal blocking voltage. This procedure is a standard test for power modules and aims to stress the chip passivation (ECPE 2021; Lutz et al., 2018). However, test conditions were comparable to CAF tests according to IPC-TM-650 (IPC TM-650), albeit at higher voltage. An initial set of samples failed the test, showing increased leakage current. A lift-off of the chip's polyimide passivation was identified as a root cause. In a second, improved set of samples, three out of four passed the test.

Frühauf et al. combined TST and HRTRB testing, to investigate a cross-correlation between thermomechanical damage and loss of electrical insulation (Fruehauf et al., 2018). The test was conducted on a low-voltage system-in-package with PCB embedded logic chip and power MOSFET. The samples were first exposed to 100 thermo-shock cycles to trigger a mechanical ageing. Then, the samples were exposed to H3TRB conditions for 100 h. The bias voltage was not reported, however, the input voltage of SiP was specified with 18 V, so that a low voltage bias may be assumed. The sequence was repeated five times and a steady increase in leakage current was observed in intermediate measurements. However, even after the end of test, the maximum leakage current remained well below the specifications of the device.

6. Conclusion and outlook

In this paper, we have reviewed the scientific literature on embedding of active power semiconductor devices into circuit boards. The fabrication technology can be classified into three basic processes, the Chip-on-Substrate, the Chip-in-Cavity, and the Double-side Microvia process. Today, PCB suppliers use these processes, sometimes with minor modifications. All require semiconductor dies with Cu metallization, which is still a challenge, as power semiconductors typically have Al metallization on the top side, and Ag on the bottom side. Several methods to apply a Cu metallization on the top have been presented and the requirements for subsequent laser drilling for contact formation have been discussed in the literature. Academic research has proposed some alternative approaches for electrical connections of embedded

dies, such as sintered Cu plates, metal-foam contacts, or thermo-compression bonding of Cu nanowires. All these methods are still at research stage.

The selection of the laminate material is another important topic. Circuit boards in most cases rely on epoxy-based laminates. Other resin materials such as benzoxazine, polyimide-blend, or bismaleimide-triazine offer higher glass transition temperatures and might enable semiconductor junction temperatures of up to 200°C in operation. Moreover, they offer lower CTE values, which reduces the intrinsic thermomechanical stresses in the heterogenous material stack.

Many examples of PCB-embedded power packages are disclosed in the scientific literature. These demonstrators include all common types of power semiconductors with nominal blocking voltages up to 1200 V. A key benefit of PCB embedding is the planar structure, which enables low-inductive designs. By integration of primary DC link capacitors, the commutation loop inductance of the switching cell can be reduced to well below 1 nH, which is required for fast and clean switching of wide-bandgap semiconductors. This number is more than one order of magnitude below the stray inductance of an off-the-shelf power module, e.g. *Infineon FS50R12W2T7* with $L_{sCE,typ} = 40$ nH (Infineon, 2020). On the other hand, the planar structures with large area traces generate parasitic capacitances. It is known that these parasitic capacitances cause ground currents and EMI issues (Domurat-Linde & Hoene, 2012). Up to now, this topic has received little attention in the PCB embedding literature.

The use of thick Cu substrates allows efficient heat removal from the semiconductor. Typical chip area independent thermal resistances are in the range of 20…40 mm^2K/W. This number compares to 40 mm^2W for a conventional power module with Al_2O_3 DBC substrate (*Infineon FS50R12W2T7* $R_{th,jhs} = 0.955$, $A_{chip} = 41mm^2$) (Infineon, 2020). A further reduction of the thermal resistance was achieved by double side cooling or integrated liquid cooling.

When discussing PCB embedding, the use of organic insulation materials is typically a point of concern. Several studies report breakdown voltages of more than 5.0 kV, even for dielectrics as thin as 100 μm. However, the dielectric strength decreases at elevated temperatures and due to temperature cycles. Moreover, the growth of copper traces, known as CAF in the PCB industry, is still of concern and requires further research. The combination of thermomechanical stresses and high-temperature high-humidity voltage bias could prove critical for high-voltage applicatons (Munding et al., 2017; Randoll, 2018).

According to some researchers, fabrication of embedded structures on panel level might provide cost benefits. However, there are no scientific studies that support this claim. Apparently, the cost structure of commercial PCB suppliers is highly confidential and therefore will not be discussed in publications. Nevertheless, various SiP with embedded dies in the cost-sensitive low power segment prove successful commercial implementation of the technology. For higher power applications, there are only a few commercial products, such as GaN Systems's GaN PX embedded package (GaN Systems, 2022). First System-in-Board converters for application in 48 V mild-hybrid drivetrains have been announced with start of production scheduled for 2021 (Infineon, 2019; Reichhardt, 2019). Higher voltage applications, such as EV-traction inverters, on-board chargers, and DC/DC converters are on the roadmap of major technology suppliers (Gottwald et al., 2022). Dedicated development and production capacities are currently being built up, both in Europe and Asia (AT&S, 2022; Zühlke, 2020). It seems that, after more than a decade of research, the technology is finally ready to move out of the laboratory and turn into real-world products.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

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References

Jillek, W., & Yung, W. (2005). Embedded components in printed circuit boards: A processing technology review. *The International Journal of Advanced Manufacturing Technology, 25*, 350–360. https://doi.org/10.1007/s00170-003-1872-y

Waffenschmidt, E., Ackermann, B., & Ferreira, J. A. (2005). Design method and material technologies for passives in printed circuit board embedded circuits. *IEEE Transactions on Power Electronics, 20*, 576–584. https://doi.org/10.1109/TPEL.2005.846530

Hofmann, T. (1996). Multi-Layer-Substrat sowie Verfahren zu seiner Herstellung, German Patent DE19627543B9.

Palm, P., Moisala, J., Kivikero, A., Tuominen, R., & Iihola, A. (2005). Embedding active components inside printed circuit board (PCB) - A solution for miniaturization of electronics. In *Proceedings of the international symposium on advanced packaging materials: Processes, properties and interfaces*. IEEE. March 16-18, 2005.

Manessis, D., Pawlikowski, J., Ostmann, A., Schischke, K., Aschenbrenner, R., Schneider-Ramelow, M., … Lang, K.-D. (2017). Embedding technologies for heterogeneous integration of components in PCBs-an innovative modularisation approach with environmental impact. In *Proceedings of the 21st European microelectronics and packaging conference (EMPC) exhibition* (pp. 1–8). IEEE.

Waris, T. F., Tuominen, R., & Kivilahti, J. K. (2001). Panel-sized integrated module board manufacturing. In *Proceedings of the international conference on polymers and adhesives in microelectronics and photonics* (pp. 218–223). IEEE.

Ostmann, A., Neumann, A., Auersperg, J., Ghahremani, C., Sommer, G., Aschenbrenner, R., & Reichl, H. (2002). Integration of passive and active components into build-up layers. In *Proceedings of the 4th electronics packaging technology conference* (pp. 223–228). IEEE.

Kujala, A., Tuominen, R., & Kivilahti, J. K. (1999). Solderless interconnection and packaging technique for embedded active components. In *Proceedings of the 49th electronic components and technology conference ECTC* (pp. 155–159). IEEE.

Ostmann, A., Manessis, D., Boettcher, L., Karaszkiewicz, S., & Reichl, H. (2009). Realisation of embedded-chip QFN packages - technological challenges and achievements. In *Proceedings of the European microelectronics and packaging conference EMPC*. IEEE.

Infineon Technologies (2014). Press release June 16th https://www.infineon.com/cms/de/about-infineon/press/market-news/2014/INFPMM201406-045.html, accessed 23 April 2022.

Grubl, W., Gross, S., & Schuch, B. (2018). Embedded components for high temperature automotive applications. In *Proceedings of the 68th electronic components and technology conference ECTC* (pp. 1233–1237). IEEE.

Jung, E., Ostmann, A., & Landsberger, C. (2000). Verfahren zum Integrieren eines Chips innerhalb einer Leiterplatte und Integrierte Schaltung. *European Patent, EP1230680B1*.

Kaminski, N. (2017). The ideal chip is not enough: Issues retarding the success of wide band-gap devices. *Japanese Journal of Applied Physics, 56*, 04CA03. https://doi.org/10.7567/JJAP.56.04CA03

Buttay, C., Martin, C., Morel, F., Caillaud, R., Le-Lesle, J., Mrad, R., … Mollov, S. (2018). Application of the PCB-embedding technology in power electronics – state of the art and proposed development. In *Proceedings of the international symposium on 3D power electronics integration and manufacturing (3D-PEIM)*. IEEE.

Wintrich, A., Nicolai, U., Tursky, W., & Reimann, T. (2015). *Application manual power semiconductors* (2nd Ed.). Ilmenau: ISLE Verlag.

Link, L., Sharma, A. B., Polezhaev, V., Huesgen, T., Vaas, M., Stohrer, G., & Koch, F. (2021). Top side isolation investigation of PCB embedded 1.2kV dies. In *Proceedings of the 23rd European microelectronics and packaging conference & exhibition EMPC*. IEEE.

Ostmann, A., Hofmann, T., Neeb, C., Boettcher, L., Manessis, D., & Lang, K.-D. (2012). Embedded power electronics for automotive applications. In *Proceedings of the 7th international microsystems, packaging, assembly and circuits technology conference IMPACT* (pp. 163–166). IEEE.

Huesgen, T., Polezhaev, V., Sharma, A. B., Liu, C., Montazerian, M., Stadler, P., … Salvatore, G. (2021). Reliability Screening of a Hybrid DBC/PCB power semiconductor prepackage. In *Proceedings of the 23rd European microelectronics and packaging conference EMPC*. IEEE.

Hoene, E., Ostmann, A., Lai, B. T., Marczok, C., Müsing, A., & Kolar, J. W. (2013). Ultra-low-inductance power module for fast switching seminconductors. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion, renewable energy and energy management PCIM*. IEEE.

Munding, A., Kessler, A., Scharf, T., Plikat, B., & Pressel, K. (2017). Laminate chip embedding technology — impact of material choice and processing for very thin die packaging. In *Proceedings of the 67th electronic components and technology conference (ECTC)* (pp. 711–718). IEEE.

Gottwald, T., & Roessle, C. (2014). p2 Pack - the paradigm shift in interconnect technology. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion, renewable energy and energy management PCI*. IEEE.

Gottwald, T., & Roessle, C. (2018). Minimizing form factor and parasitic inductances of power electronic modules: The p2 Pack Technology. In *Proceedings of the 7th electronic system-integration technology conference ESTC*. IEEE.
Essig, K. S., Chiu, C. T., Kuo, J., Chen, P., & Yannou, J.-M. (2016). Higher efficiency Power Module solutions by chip embedding. In *Proceedings of the 6th electronic system-integration technology conference ESTC*. IEEE.
Essig, K. S., Yannou, J.-M., Chiu, C. T., Kuo, J., & Chen, P. (2017). High efficient mid power modules by next generation chip embedding technology. In *Proceedings of the 21st European microelectronics and packaging conference EMPC*. IEEE.
Stahr, J. (2021). ECP-Technology for Packaging. In *Leiterplatten-Einbetttechnologien für die Leistungselektronik. Cluster Online Seminar*. Cluster Leistungselektronik im ECPE e.V.
Stahr, J., & Morianz, M. (2019). Powering up electronics—latest developments and concepts for packaging of electronics in automotive systems. *Electronic components and systems for automotive applications* (pp. 107–115). Springer.
ABB, (2013). Applying IGBT and diode dies: Application note 5SYA 2059-04.
TDK, (2022). Micro Module Substrat mit Built-in ICs, Produkte mit SESUB Technologie, https://product.tdk.com/de/products/sesub/index.html, accessed 23 April 2022.
Texas Instruments, (2017). MicroSiP Power Modules Construction Overview,, https://training.ti.com/microsip-power-modules-construction-overview, accessed 23 April 2022.
Ostmann, A. (2017). Einbetten von Pre-Packages statt Bare-Die - Modulare Leistungselektronik. In *Schaltungsträger und Substrattechnologien für die Leistungselektronik*. Cluster Leistungselektronik im ECPE e.V.
Sharma, A. B., Schnur, J., Haag, N., Polezhaev, V., & Huesgen, T. (2020). PCB embedding using single-switch-pre-packages as modular building blocks. In *Proceedings of the 11th international conference on integrated power electronics systems CIPS*. IEEE.
Rittner, M., Gross, D., Guyenot, M., Guenther, M., Haag, S., Kaden, T., … Kock, M. (2014). Robust top side contact technology on power semiconductors. In *Proceedings of the 8th international conference on integrated power electronics systems CIPS*. IEEE.
Hensler, A., Bigl, T., Neugebauer, S., & Pfefferlein, S. (2017). Air Cooled SiC three level inverter with high power density for industrial applications, International Exhibition and Conference for Power Electronics, Intelligent Motion. *Renewable Energy and Energy Management PCIM Europe, IEEE*.
Heuck, N., Guth, K., Thoben, M., Mueller, A., Oeschler, N., Boewer -, L., … Ciliox, A. (2014). Aging of new interconnect-technologies of power-modules during power-cycling. In *Proceedings of the 8th international conference on integrated power electronics systems* (pp. 1–6). IEEE.
Melvin, C., & Roelfs, B. (2017). Simultaneous front and back side Cu metallization on power chips: DP: Discrete and power devices or ET/ID: Enabling technologies and innovative devices. In *Proceedings of the 28th advanced semiconductor manufacturing conference ASMC* (pp. 189–191). IEEE.
Randoll, R. G. (2018). Investigations on a Packaging Technology for PCB Integrated Power Electronics. *Doctoral thesis*.
Randoll, R., Wondrak, W., & Schletz, A. (2016). Lifetime and manufacturability of integrated power electronics. *Microelectronics Reliability, 64*, 513–518. https://doi.org/10.1016/j.microrel.2016.07.032
Laird technologies. (2011). TlamTM SS HTD Thermally Conductive PCB Substrate. *Datasheet*.
Le Lesle, J., Quemener, V., Morrand, J., Perrin, R., Mrad, R., & Mollov, S. (2020). Design, manufacturing and evaluation of a highly integrated low-voltage high-current inverter. In *Proceedings of the 11th international conference on integrated power electronics systems CIPS*. IEEE.
Ostmann, A., Boettcher, L., Manessis, D., Karaszkiewicz, S., & Lang, K. D. (2013). Power modules with embedded components. In *Proceedings of the Eurpoean microelectronics packaging conference EMPC*. IEEE.
Yu, C., Buttay, C., Labouré, É., Bley, V., Combettes, C., & Brillat, G. (2016). Comparison of topside contact layouts for power dies embedded in PCB. In *Proceedings of the 6th electronic system-integration technology conference (ESTC)*. IEEE.
Reichhardt, M. (2019). Mild-Hybrid: Continental nutzt Leiterplatten mit Embedded Chips. *Automobil Industrie*.
Reiner, R., Weiss, B., Meder, D., Waltereit, P., Gerrer, T., Quay, R., … Ambacher, O. (2018). PCB-embedding for GaN-on-Si power devices and ics. In *Proceedings of the 10th international conference on integrated power electronics systems CIPS*. IEEE.
Perrin, R., Le Lesle, J., Morand, J., & Lefevre, G. (2021). A PCB based package with thermal resistance improvement. In *Proceedings of the 23rd European conference on power electronics and applications (EPE'21 ECCE Europe)*. IEEE.
Bohm, C., Hauck, T., Muller, W. H., & Juritza, A. (2004). Probability of silicon fracture in molded packages [ICs]. In *Proceedings of the 5th international conference on thermal and mechanical simulation and experiments in microelectronics and microsystems EuroSimE* (pp. 75–81). IEEE.
Lutz, J., Schlangenotto, H., Scheuermann, U., & de Doncker, R. (2018). *Semiconductor power devices*. Springer International Publishing.
Pletz, M., Bermejo, R., Supancic, P., Stahr, J., & Morianz, M. (2011). Numerical investigation of the process of embedding components into Printed Circuit Boards. In *Proceedings of the 12th international conference on thermal, mechanical & multi-physics simulation and experiments in microelectronics and microsystems*. IEEE.
Tang, Q., Dchar, I., & Then, N. K. (2021). Die Attach effect on electrical performance and reliability of embedded die package. In *Proceedings of the 23rd electronics packaging technology conference EPTC* (pp. 374–377). IEEE.
Guyenot, M., Mager, C., Birkhold, A., Ratchev, R., Khoshamouz, A., Gottwald, T., & Kreuer, S. (2017). New resin materials for high power embedding. In *Proceedings of the 67th electronic components and technology Conference ECTC* (pp. 690–695). IEEE.
Kearney, D. J., Kicin, S., Bianda, E., & Krivda, A. (2017). PCB embedded semiconductors for low-voltage power electronic applications. *IEEE Transactions on Components, Packaging and Manufacturing Technology, 7*, 387–395. https://doi.org/10.1109/TCPMT.2017.2651646
Otto, A., Schroeder, T., Dudek, R., Wang, W.-S., Baum, M., Wiemer, M., … Rzepka, S. (2018). Evaluation of Ag-sinter and CuSn-TLP based joining technologies on lead frame. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion, renewable energy and energy management PCIM* (pp. 1–8). IEEE.
Zhang, X., Chan, J., Cao, L., Hou, F., He, H., & Wan, L. (2013). Thermal-mechanical simulation of embedded module based on organic substrate. In *Proceedings of the IEEE international symposium on advanced packaging materials* (pp. 126–136). IEEE.
Randoll, R., Asef, M., Wondrak, W., Böttcher, L., & Schletz, A. (2015). Characteristics and aging of PCB embedded power electronics. *Microelectronics Reliability, 55*, 1634–1639. https://doi.org/10.1016/j.microrel.2015.06.072
Kasem, Y., & Feinstein, L. (1987). Horizontal die cracking as a yield and reliability problem in integrated circuit devices. *IEEE Transactions on Components Hybrids and Manufacturing Technology, 10*, 654–661. https://doi.org/10.1109/TCHMT.1987.1134789
Ranjan, M., Gopalakrishnan, L., Srihari, K., & Woychik, C. (1998). Die cracking in flip chip assemblies. In *Proceedings of the IEEE electronic components and technology conference ECTC* (pp. 729–733). IEEE.
Bohm, C., Hauck, T., Juritza, A., & Muller, W. H. (2004). Weibull statistics of silicon die fracture. In *Proceedings of the 6th electronics packaging technology conference EPTC* (pp. 782–786). IEEE.
Hauck, T., Bohm, C., & Muller, W. H. (2005). Weibull statistics for multiple flaw distributions and its application in silicon fracture prediction. In *Proceedings of the 6th international conference on thermal, mechanical and multi-physics simulation and experiments in micro-electronics and micro-systems EuroSimE* (pp. 242–247). IEEE.
Zhao, J.-H., Tellkamp, J., Gupta, V., & Edwards, D. (2008). Experimental evaluations of the strength of silicon die by 3-point-bend versus Ball-on-Ring tests. In *Proceedings of the 11th intersociety conference on thermal and thermomechanical phenomena in electronic systems* (pp. 687–694). IEEE.
Deluca, M., Bermejo, R., Pletz, M., Supancic, P., & Danzer, R. (2011). Strength and fracture analysis of silicon-based components for embedding. *Journal of the European Ceramic Society, 31*, 549–558. https://doi.org/10.1016/j.jeurceramsoc.2010.10.029
Pavliček, N., Liu, C., Stalder, P., Salvatore, G., Mohn, F., Huesgen, T., & Thoma, T. (2022). Patterning and CTE-matching of contacts to optimize thermomechanical stress in power semiconductor pre-packages. In *Proceedings of the 12th international conference on integrated power electronics systems CIPS*. IEEE.
GaN Systems, (2022)., https://gansystems.com/, accessed 26 April 2022.
Isola Group, (2022). 370HR thermally robust epoxy laminate and Prepreg Isola, https://www.isola-group.com/pcb-laminates-prepreg/370hr-laminate-prepreg/, accessed 25 April 2022.
Duch, S., Schmitt, W., Chew, L. M., Nachreiner, J., & Gunst, S. (2017). HERAEUS mAgic SINTER MATERIALs: Product presentation.
Regnat, G., Jeannin, P. O., Lefevre, G., Ewanchuk, J., Frey, D., Mollov, S., & Ferrieux, J. P. (2015). Silicon carbide power chip on chip module based on embedded die technology with paralleled dies. In *Proceedings of the energy conversion congress and exposition ECCE* (pp. 4913–4919). IEEE.
Regnat, G., Jeannin, P. O., Frey, D., Ewanchuk, J., Mollov, S. V., & Ferrieux, J.-P. (2018). Optimized power modules for silicon carbide mosfet. *IEEE Transactions on Industry Applications, 54*, 1634–1644. https://doi.org/10.1109/TIA.2017.2784802
Sharma, A. B., Paul, D., Kreck, M., Rahmoun, Y., Anders, P., Gruber, M., & Huesgen, T. (2016). PCB embedded power package with reinforced top-side chip contacts. In *Proceedings of the 6th electronic system-integration technology conference ESTC*. IEEE.
Sharma, A. B., Schnur, J., Haag, N., Kuwan, T., Stogel, A., & Huesgen, T. (2018). Fabrication of PCB embedded 1200V/50A power module and benchmarking with commercial DBC-based package. In *Proceedings of the 10th international conference on integrated power electronics systems CIPS*. IEEE.
Rudzki, J., Becker, M., Eisele, R., Poech, M., & Osterwald, F. (2014). Power modules with increased power density and reliability using Cu wire bonds on sintered metal buffer layers. In *Proceedings of the 8th international conference on integrated power electronics systems CIPS* (pp. 1–6). IEEE.
Pascal, Y., Labrousse, D., Petit, M., Lefebvre, S., & Costa, F. (2018). Experimental investigation of the reliability of Printed Circuit Board (PCB)-embedded power dies with pressed contact made of metal foam. *Microelectronics Reliability, 88*, 707–714. https://doi.org/10.1016/j.microrel.2018.06.064. -90.
Pascal, Y., Abdedaim, A., Labrousse, D., Petit, M., Lefebvre, S., & Costa, F. (2017). Using laminated metal foam as the top-side contact of a PCB-embedded power die. *IEEE Electron Device Letters, 38*, 1453–1456. https://doi.org/10.1109/LED.2017.2748223
Bensebaa, S., Berkani, M., Lefebvre, S., & Petit, M. (2020). Design and characterization of PCB-embedded power dies using solderless pressed metal foam. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion PCIM Europe digital days* (pp. 1–7). IEEE.
Heraeus Electronics, (2022). - Die Top System (DTS®), https://www.heraeus.com/en/het/products_and_solutions_het/material_systems/die_top_system/dts_page.html, accessed 30 April 2022.
Wieland (2021). Datasheet Wieland K32: Cu-ETP C11000 CW004A.
Djuric, B., Bley, V., Morand, J., Dagut, O., Cambronne, J. P., & Mollov, S. (2019). Double side interconnection for vertical power components based on macro and nano structured copper interfaces and printed circuit board technologies, MiNaPAD.
Polezhaev, V., Sharma, A. B., Schiffmacher, A., Litzenberger, L., Wilde, J., & Huesgen, T. (2019). Development of a novel 600V/50A power package with semiconductor chips sandwiched between PCB substrates using double-side Ag-sintering. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion PCIM Europe*. IEEE.
Tablati, A., Alayli, N., Youssef, T., Belnoue, O., Theolier, L., & Woirgard, E. (2020). New power module concept in PCB-embedded technology with silver sintering die attach. *Microelectronics Reliability, 114*, Article 113891. https://doi.org/10.1016/j.microrel.2020.113891

Feix, G., Hoene, E., Zeiter, O., & Pedersen, K. (2015). Embedded very fast switching module for SiC power MOSFETs. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion PCIM*. IEEE.

Kröner, H. (2021). Advanced packaging materials for packaging and chip embedding technology, in: Clusterseminar Leiterplatten-Einbetttechnologie für die Leistungselektronik.

IPC TM-650 Test methods manual, IPC International,Inc.

Schuderer, J., Vemulapati, U., & Traub, F. (2014). Packaging SiC power semiconductors Challenges, technologies and strategies. In *Proceedings of the workshop on wide bandgap power devices and applications* (pp. 18–23). IEEE.

Stahr, H., Morianz, M., Gross, S., Unger, M., Nicolics, J., & Boettcher, L. (2016). Investigation of a power module with double sided cooling using a new concept for chip embedding. In *Proceedings of the 9th international conference on integrated power electronics systems CIPS*. IEEE.

Guyenot, M., Maas, D., Ratchev, R., Khoshamouz, A., Gottwald, T., & Kreuer, S. (2018). New failure mechanism in high temperature resin materials. In *Proceedings of the 68th electronic components and technology conference ECTC* (pp. 1238–1244). IEEE.

Hou, F., Wang, W., Lin, T., Cao, L., Zhang, G. Q., & Ferreira, J. A. (2019). Characterization of PCB embedded package materials for SiC MOSFETs. *IEEE Transactions on Components, Packaging and Manufacturing Technology, 9*, 1054–1061. https://doi.org/10.1109/TCPMT.2019.2904533

Panasonic Industrial Devices & Solutions. (2022). Highly heat resistant Halogen-free Multi-layer circuit board materials | R-1566S https://industrial.panasonic.com/ww/products/pt/halogen-free/hfreer1566s, accessed 25 April 2022.

Isola. (2021). IS550H very high thermally reliability Laminate and Prepreg | Isola Group,, https://www.isola-group.com/pcb-laminates-prepreg/is550h-laminate-prepreg/, accessed 25 April 2022.

Showa Denko Materials Co. Ltd. (2021), MCL-E-795G Halogen Free, High Tg, High Elastic Modulus and Low CTE material, https://www.mc.showadenko.com/english/products/bm/005.html, accessed 25 April 2022.

Mitsubishi Gas Chemical Company, (2022). Non-haloganated Low CTE BT Resin Laminate for IC Plastic Packages https://www.mgc.co.jp/eng/products/sc/btprint/lineup/hfbt.html, accessed 25 April 2022.

Aismalibar, (2021). COBRITHERM HTC 3,2W: Datasheet DS_21.

Savulak, S., Guo, B., & Krishnamurthy, S. (2018). Three-phase inverter employing PCB embedded GaN FETs. In *Proceedings of the applied power electronics conference and exposition APEC* (pp. 1256–1260). IEEE.

Qi, Z., Pei, Y., Wang, L., Yang, Q., & Wang, K. (2022). A highly integrated PCB embedded GaN full-bridge module with ultralow parasitic inductance. *IEEE Transactions on Power Electronics, 37*, 4161–4173. https://doi.org/10.1109/TPEL.2021.3128694

Klein, K., Hoene, E., & Lang, K. D. (2019). Power module design for utilizing of WBG switching performance. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion PCIM Europe*. IEEE.

Marczok, C., Martina, M., Laumen, M., Richter, S., Birkhold, A., Flieger, B., … Paesler, T. (2020). SiCmodul - modular high-temperature SiC power electronics for fail-safe power control in electrical drive engineering. In *Proceedings of the 11th international conference on integrated power electronics systems CIPS*. IEEE.

Knoll, J., Son, G., DiMarino, C., Li, Q., Stahr, H., & Morianz, M. (2021). Design and analysis of a PCB-embedded 1.2 kV SiC half-bridge module. In *Proceedings of the energy conversion congress and exposition ECCE* (pp. 5240–5246). IEEE, 10/10/2021 - 10/14/.

Neeb, C., Teichrib, J., de Doncker, R. W., Boettcher, L., & Ostmann, A. (2014). A 50 kW IGBT power module for automotive applications with extremely low DC-link inductance. In *Proceedings of the 16th European conference on power electronics and applications EPE*. IEEE.

Wolf, J. (2021). Leistungsbauteile integriert in Leiterplattenmaterial Eine Übersicht zu Aufbauten und Herausforderungen. In *Leiterplatten-Einbetttechnologien für die Leistungselektronik. Cluster Online Seminar*. Cluster Leistungselektronik im ECPE e.V.

Wyss, J., & Biela, J. (2016). Analysis of PCB embedded power semiconductors for a 30 kW boost PFC converter. In *Proceedings of the 18th European conference on power electronics and applications EPE'16 ECCE Europe*. IEEE.

Panasonic Industrial Devices & Solutions. (2022). High thermal conductive Bonding sheet R-14,, https://industrial.panasonic.com/ww/products/pt/ecool/ecoolm, accessed 25 April 2022.

Nicolics, J., Unger, M., Groß, S., Morianz, M., & Stahr, H. (2017). Thermal characterization of a 500W motor driver module with embedded power transistors. In *Proceedings of the 40th international spring seminar on electronics technology (ISSE)*. ISSE.

Birkhold, A., & Martina, M. (2020). PCB Embedding von SiC MOSFET für automotive Leistungselektronikmodule. In *Elektronische Baugruppen und Leiterplatten EBL*. VDE Verlag.

Hoene, E., Ostmann, A., & Marczok, C. (2014). Packaging Very Fast Switching Semiconductors. In *Proceedings of the 8th International conference on integrated power electronics systems CIPS*. IEEE.

Neeb, C. (2018).Aufbau- und Verbindungstechnik für Leistungselektronik in Automotiveanwendungen, PhD Thesis, RWTH Aachen.

Liu, L. (2021). Laser processing technologies in the PCB industry. *Laser Focus World*. Endeavor Business Media.

Loher, T., Karaszkiewicz, S., Bottcher, L., & Ostmann, A. (2016). Compact power electronic modules realized by PCB embedding technology. In *Proceedings of the 2016 IEEE CPMT symposium Japan (ICSJ)* (pp. 259–262). IEEE.

Caillaud, R., Le Lesle, J., Buttay, C., Morel, F., Mrad, R., Degrenne, N., & Mollov, S. (2019). Evaluation of the PCB-embedding technology for a 3.3 kW converter. In *Proceedings of the international workshop on integrated power packaging IWIPP*. IEEE, 4/24/2019 - 4/26/.

Hou, F., Guo, X., Wang, Q., Wang, W., Lin, T., Cao, L., … Ferreira, J. A. (2018). High Power-Density 3D integrated power supply module based on panel-level PCB embedded technology. In *Proceedings of the 68th electronic components and technology conference ECTC* (pp. 1365–1370). IEEE.

Hou, F., Wang, W., Ma, R., Li, Y., Han, Z., Su, M., Li, J., Yu, Z., Song, Y., Wang, Q., Chen, M., Cao, L., Zhang, G., & Ferreira, B. (2020). Fan-out panel-level PCB-embedded SiC power MOSFETs packaging. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 8*, 367–380. https://doi.org/10.1109/JESTPE.2019.2952238

Sharma, A. B., Weimer, J., Koch, D., Kallfass, I., & Huesgen, T. (2021). Asymmetric packages for optimal performance of GaN-HEMT using PCB fabrication technology. In *Proceedings of the international exhibition and conference for power electronics, intelligent motion, renewable energy and energy management PCIM Europe digital days*. IEEE.

Koch, D., Sharma, A., Weimer, J., Weiser, M., Huesgen, T., & Kallfass, I. (2021). A 48 V, 300 kHz, High Current DC/DC-converter based on paralleled, asymmetrical & thermally optimized PCB embedded GaN packages with integrated temperature sensor. In *Proceedings of the 33rd International symposium on power semiconductor devices and ICs ISPSD* (pp. 383–386). IEEE.

ECPE. (2021). *ECPE guideline AQG 324: Qualification of power modules for use in power electronics converter units in motor vehicles* (3th ed.).

Yang, D., Kengen, M., Peels, W., Heyes, D., & van Driel, W. D. (2009). Reliability modeling on a MOSFET power package based on embedded die technology. In *Proceedings of the 10th international conference on thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems EuroSimE*. IEEE.

Dechant, E., Seliger, N., & Kennel, R. (2019). Performance of a GaN Half Bridge Switching Cell with Substrate Integrated Chips. *PCIM Europe*.

Dechant, E., Seliger, N., & Kennel, R. (2019). Power cycling and temperature endurance test of a GaN switching cell with substrate integrated chips. *Microelectronics Reliability, 100*, Article 113372. https://doi.org/10.1016/j.microrel.2019.06.064. -101.

Ghebreslassie, M., Sharma, A. B., & Huesgen, T. (2022). Thermal impedance evaluation of optimized PCB-based GaN HEMT single-chip- Prepackage using VGS Method. In *Elektronische Baugruppen und Leiterplatten EBL*. VDE Verlag.

Gottwald, T., Martina, M., Marczok, C., Laumen, M., Flieger, B., & Wendt, O. (2022). Power embedding. In *2th International conference on integrated power electronics systems CIPS*. IEEE.

Randoll, R., Wondrak, W., & Schletz, A. (2014). Dielectric strength and thermal performance of PCB-embedded power electronics. *Microelectronics Reliability, 54*, 1872–1876. https://doi.org/10.1016/j.microrel.2014.07.139

Dechant, E., Seliger, N., & Kennel, R. (2019). A study of dielectric breakdown of a half-bridge switching cell with substrate integrated 650V GaN dies. In *Proceedings of the international workshop on integrated power packaging IWIPP* (pp. 18–23). IEEE.

Fruehauf, P., Munding, A., Pressel, K., Vogt, M., & Schwarz, P. (2018). Chip-package-board reliability of System-in-Package using laminate chip embedding technology based on Cu leadframe. In *Proceedings of the 7th electronic system-integration technology conference ESTC*. IEEE.

Domurat-Linde, A., & Hoene, E. (2012). Analysis and reduction of radiated EMI of power modules. In *Proceedings of the 7th international conference on integrated power electronics systems CIPS* (pp. 1–6). IEEE.

Infineon Technologies. (2019), Press release, https://www.infineon.com/cms/de/about-infineon/press/market-news/2019/INFATV201905-068.html, accessed 29 April 2022.

Infineon Technologies. (2020). Datasheet FS50R12W2T7.

Zühlke, K. (2020). Neues Werk in Betrieb: Schweizer startet Produktion in China,, https://www.elektroniknet.de/elektronikfertigung/leiterplatten/schweizer-startet-produktion-in-china.176796.html, accessed 29 April 2022.

AT&S (2022). Press release March, 3rd, https://ats.net/de/2022/03/03/baubeginn-fuer-neues-ats-forschungszentrum-in-leoben/, accessed 29 April 2022.