

Investigations on High-Power LEDs and Solder Interconnects in Automotive Application: Part II—Reliability

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Abstract—Thermo-mechanical reliability is one major challenge in solid-state lighting for automotive applications. Mismatches in the coefficients of thermal expansion (CTE) between high-power LED packages and substrates paired with temperature changes induce mechanical stress. This leads to thermal degradation by crack formation in the solder interconnect and/or delamination in the substrate, which in turn increases junction temperature, thus decreasing light output and reducing the lifetime. A reliability study with a total of 1,800 samples - segmented in nine LED types and five solder pastes - is performed to investigate degradation and understand the influence of solder material and LED package design. The results are presented in two papers. Initial characterization of the LEDs was handled in the first paper. This second paper focuses on degradation and lifetime. Overall, more than 40,000 transient thermal analysis (TTA) and 9,000 scanning acoustic microscopy (SAM) measurements were taken to evaluate degradation during accelerated aging of 1,500 thermal shock cycles. Six different failure modes were observed, which were distinguishable by only using TTA data. For the reliability evaluation, crack ratio was determined by SAM images while thermal degradation as well as mean lifetime were determined using TTA data. Multiple observations were made within this study. **First: SAM and TTA data correlated very well; Second: Higher silver content and additives in the solder paste reduce crack growth and increases lifetime; Third: Thick film ceramic LEDs reach significant longer lifetimes than thin film ceramic LEDs, and copper lead-frame LEDs reached by far the longest lifetimes; Fourth: A pad design with a greater pad size, smaller gaps and balanced size ratio between electrical and thermal pad is advantageous; Fifth: Voiding (below 10%) has no significant influence on the reliability.**

Index Terms—LED, non-destructive testing, reliability, solder, scanning acoustic microscopy (SAM), thermal impedance (Zth), thermal resistant (Rth), transient thermal analysis (TTA), X-ray.

I. INTRODUCTION

LEDs have replaced conventional light sources (e.g., filament and discharge lamps) for illumination in nearly all fields because of better optical, mechanical, electrical, and environmental properties [2], [3] as well as regulation [4]. In today's lighting industry, the most common light source is the white LED based on a blue light emitting GaN die with phosphor light conversion [5].

Independent of LED color or type, the most critical parameter is the junction temperature T_J . An increase in T_J results in a decrease in light output - i.e., a reduction of efficiency - a color shift and a lifetime reduction [6]. To limit T_J to a non-critical range during operation, the generated heat must be conducted from the LED junction through the LED package and substrate to the heat sink. Thermal and mechanical properties of this path determine the initial thermal performance as well as the degradation due to environmental conditions [7].

Initial performance and degradation both depend strongly on the chosen component dimensions and materials for the LED, solder interconnect and substrate. Finding the best combination is not trivial and valuable data is mostly not publicly accessible. To reveal influences, we performed a full factorial reliability study with nine LED types and five lead-free solder pastes, resulting in a total sample count of 1800 high-power LEDs. Thermal shock cycling between -40°C and $+125^\circ\text{C}$ until 1500 cycles was used for accelerated aging and the degradation progress investigated at multiple intermediate aging stages.

Initial characterization of the LEDs by X-Ray, scanning acoustic microscopy (SAM) and transient thermal analysis (TTA) was published in [1]. This second part focuses on reliability and lifetime. Here, crack growth during aging was determined from SAM images while thermal degradation was evaluated based on TTA data. Both data sets correlate very well. Based on the results, design rules for solder paste and LED package design are formalized.

II. DESIGN OF EXPERIMENT

In total, 1800 LEDs were part of this reliability study. The LEDs were separated in nine LED types and five lead-free

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
















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TABLE I
SUMMARY OF RELEVANT MECHANICAL, ELECTRICAL AND THERMAL PARAMETERS OF THE LEDs

Name in this paper	FC-SP1	FC-SP2	FC-SP3	FC-SP4	FC-GB1	FC-GB2	FC-GB3	VTF1	VTF2
Classification	Automotive	General	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive
Image									
Submount	Lead frame	thick-film AlN ceramic	thick-film AlN ceramic	thick-film AlN ceramic	thick-film AlN ceramic	thin-film AlN ceramic	thin-film AlN ceramic	Lead frame	thick-film AlN ceramic
Die size ⁽¹⁾ [mm ²]	0.6	1.9	1.3	1.0	1.0	0.9	1.0	1.0	1.0
Size [mm ²]	1.6 x 1.2	1.6 x 1.6	2.5 x 2.0	1.61 x 1.88	2.3 x 1.9	1.8 x 1.45	1.8 x 1.45	3.75 x 3.75	1.9 x 1.5
Pad count	2	2	3	3	3	3	2	3	3
Elec. Pads [mm ²]	1.3 x 0.31	1.5 x 0.6	0.9 x 0.7	0.59 x 0.57	0.9 x 0.7	0.49 x 0.47	1.6 x 0.47	2.7 x 0.5	0.87 x 0.54
Therm. Pad [mm ²]	Non	Non	0.9 x 1.7	0.84 x 1.41	0.9 x 1.65	0.815 x 1.23	Non	2.7 x 1.0	0.6 x 1.34
Σ Pad-Size [mm ²]	0.81	1.80	2.79	1.86	2.75	1.45	1.49	5.40	1.77
Pad-Gap [mm]	0.28	0.30	0.45	0.25	0.25	0.30	0.30	0.35	0.25
Pad-Ratio	1 : 1	1 : 1	1 : 2.43	1 : 3.52	1 : 2.36	1 : 4.44	1 : 1	1 : 2	1 : 1.67
I_{Nom} [A]	0.35	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
$R_{th-JC-el.}$ ⁽²⁾ [K/W]	4.75	6.0	3.0	3.5	4.2	3.3	3.0	3.0	3.3
Pad-Design (scaled)									

⁽¹⁾ Measured after mechanical phosphor removal.

⁽²⁾ R_{th} from junction to case of the LED related to the electrical power. If the datasheet included no typical value, the mean value of the specified range is used.

⁽³⁾ Downscaled by factor 2.

solder pastes for a full factorial design of experiment. Each combination has a sample count of 40 LEDs. Thermal shock cycling until 1500 cycles was used for accelerated aging. The degradation progress was inspected at several intermediate aging stages.

This section briefly recapitulates most relevant properties of LEDs, solder pastes and substrate regarding reliability. More detailed information can be found in [1]. The thermal shock parameters and intermediate measurement stages are also described in this section.

A. LEDs

The mechanical, electrical and thermal specifications of the nine LED types from seven different manufactures are listed in Table I including images and pad design. The LEDs are named and numbered according to their internal die/die attach structure: FC-SP (Flip Chip with solder pads), FC-GB (Flip Chip with gold bumps) and VTF (Vertical thin film). For detailed information see [1]. All are packaged white high-power LEDs, based on a blue LED with a phosphor conversion layer [8]. Except FC-SP2, all are specified for automotive usage. All LEDs are classified for $I_{Nom} = 1.0$ A, except FC-SP1 with $I_{Nom} = 0.35$ A due to smaller die size.

To relieve thermo-mechanical stress on the LED die and for improved heat spreading, all LED types use submount technology. The LED die is therefore attached to a submount, either an AlN ceramic or a copper lead frame, which was then soldered to the substrate [9]. This setup reduces the coefficient of thermal expansion (CTE) mismatch affecting the die, since

the CTE of the die (Si: 3.2 ppm/°C) is much closer to the CTE of the submount (AlN: 5.3 ppm/°C, Cu: 16.7 ppm/°C) compared to the CTE of the substrate (Al: 23.6 ppm/°C) [10]. FC-SP2, FC-SP3, FC-SP4, FC-GB1 and VTF2 use thick film AlN submount with approx. 50 μ m Cu height. FC-GB2 and FC-GB3 use thin film AlN ceramic with <5 μ m Cu height. FC-SP1 and VTF2 use a copper lead frame.

There are three dominating solder pad designs used by the LED manufacturers for SMD soldering the LED package to the Printed Circuit Board (PCB). The scaled pad layouts of the LEDs are included in Table I. FC-SP1, FC-SP2 and FC-GB3 use a symmetrical two-pad design, with one pad for anode and one for cathode. VTF1 uses a “in-line” three-pad design, where two pads are electrical connected by the copper lead frame. The remaining LEDs use a “distributed” three-pad design, which includes an additional, electrical isolated solder pad below the die for improved heat management. This third solder pad is called thermal pad.

For later pad design evaluation, the pad ratio - defined as the ratio between biggest and smallest pad - is included in Table I. For the symmetrical two-pad designs, both pads have the same size resulting in a size ratio of 1 : 1. For three-pad designs, the thermal pad is typically bigger compared to the electrical pads. The pad ratio for these is defined as:

$$pad\ ratio = A_{Single\ Elec.\ Pad} : A_{Therm.\ Pad} \quad (1)$$

The pad ratio differs for the LED types. E.g., FC-GB2 has a pad ratio of 1 : 4.44, meaning that the thermal pad is much bigger than the electrical pads whereas for VTF2 with a pad ratio of 1 : 1.67, the pad sizes are more balanced.

TABLE II
COMPOSITION IN WEIGHT PERCENTAGE FOR THE DIFFERENT SOLDER PASTES, SORTED BY AG PARTS. REMAINING PART IS Sn

Paste	Additives material					
	Ag	Cu	Sb	Bi	Ni	In
SAC105	1.0	0.5	-	-	-	-
SAC107+BiIn	1.0	0.7	-	1.6	-	0.2
SAC305	3.0	0.5	-	-	-	-
SAC327+Sb	3.2	0.7	5.5	-	-	-
SAC387+SbBiNi	3.8	0.7	1.5	3.0	0.15	-

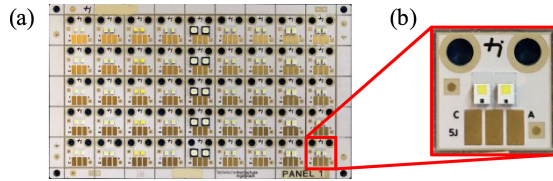


Fig. 1. (a) IMS-PCB with 90 LEDs soldered with same paste and (b) sub-PCB with two LEDs of one LED type.

B. Solder Pastes

Five commercial Sn based lead-free solder pastes were selected for this study. Their composition is listed in Table II. Two of them are pure SAC (Sn, Ag, Cu) alloys with different portions of silver. The others are SAC+ pastes with additives of Sb, Bi, Ni or In, developed for improved thermal performance and reliability [11].

All pastes were of type 4 (solder sphere diameter: 20 μm to 38 μm) and applied by a stencil-printing process using a 75 μm stencil. LEDs were placed with a semi-automatic pick-and-place machine. A batch oven was used to apply the same standardized reflow soldering profile [12] for all pastes with nitrogen protective atmosphere and vacuum during liquidus.

C. Substrate

The LEDs were soldered on an insulated metal substrate printed circuit board (IMS-PCB) with 70 μm Cu thickness, a 50 μm thick dielectric with a thermal conductivity of 4.2 W/mK and a 1.6 mm Al core (Al alloy 5052). Each IMS-PCB is assembled with 90 LEDs and can be separated into 45 sub-PCBs (each holding two LEDs of the same type). An image of an assembled IMS-PCB is shown in Fig. 1.

D. Thermal Shock Cycling

Thermal shock cycling between $-40\text{ }^\circ\text{C}$ and $+125\text{ }^\circ\text{C}$ with a dwell time of 30 min and a transfer time < 3 min was used for accelerated aging of the samples until 1500 thermal shock cycles (TSC). The quality of the samples was initially and at several intermediate aging stages checked by non-destructive test methods (TTA, SAM and X-ray) to evaluate the degradation progress. Additionally, destructive cross-sectional analysis was used to verify the non-destructive results for a number of samples. The aging process until 1500 TSC with all intermediate measurement stages is depicted in Fig. 2.

III. MEASUREMENT METHODS

This section explains the three non-destructive test methods used and recapitulates the results of the initial characterization. More detailed information can be found in [1].

A. X-Ray Inspection

X-ray is nowadays the most popular inspection method in development and production of electronics. X-ray is mostly used to detect solder bridges, voids (gas/resin inclusions in the solder joint) and non-wetted solder areas (unsoldered regions due to residues or contamination on component or substrate) [13], [14]. However, X-ray is not suited for crack detection [15].

All LEDs were initial inspected on standard 2D X-ray equipment. X-ray images are used to calculate void ratio in the solder joint by an algorithm described in [1]. Due to the vacuum soldering process, the void ratio was below a 5% average for all LED types and solder pastes except FC-GB3 (no specific reason found).

X-Ray inspection was performed on selected samples after 1000 TSC and 1500 TSC, but no usable information regarding cracks or other failures was gained by these later measurements.

B. Scanning Acoustic Microscopy

In contrast to X-Ray, SAM can also detect lateral degradation like cracks and delamination [16], [17] and is therefore used to identify crack sizes and locations. The crack ratio (cracked solder area compared to the total solder area) was determined for individual solder pads of each LED at five aging stages: Initial and after 100 TSC, 500 TSC, 1000 TSC and 1500 TSC.

For crack ratio calculation, the individual solder joints were first identified. The cracked area inside the solder joints was determined by a dynamic threshold. Areas brighter than the threshold are classified as cracked; darker areas uncracked [18], [19]. The growth of cracks during aging is shown for one FC-SP3 sample LED in Fig. 3 with raw SAM images on top and postprocessed images with marked solder joints (blue outline) and cracks (red area) below. Initial and 100 TSC SAM images show only voids. After 500 TSC, cracks growing from the right edge of the thermal pad and in the right electrical pad are observed. After 1000 TSC, cracks in thermal pad and right electrical pad have propagated further and crack growth is initiated in the left electrical pad. After 1500 TSC already 67% of the solder pad area is cracked.

C. Transient Thermal Analysis

TTA is used to determine the integrity of the thermal path from LED junction to heatsink. TTA measurements follow a standardized measurement procedure [20] and were performed on in-house developed automatized TTA equipment [21]. All LEDs were measured with heat and sense time $t_{Heat} = t_{Sense} = 3$ s. A sense current $I_{Meas} = 20$ mA and individual heating currents $I_{Heat} = I_{Nom}$ (see Table I) were used. To improve signal quality, data was averaged over ten measurement repetitions. TTA was performed initially and at eleven

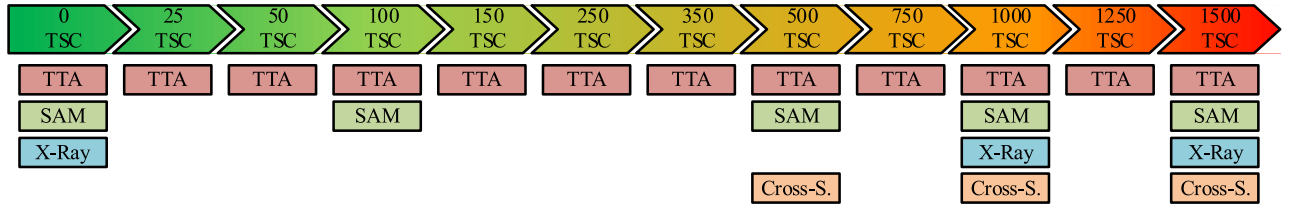


Fig. 2. Accelerated aging until 1500 temperature shock cycles with intermediate measurement stages for TTA, SAM, X-Ray and cross-sectional analysis.

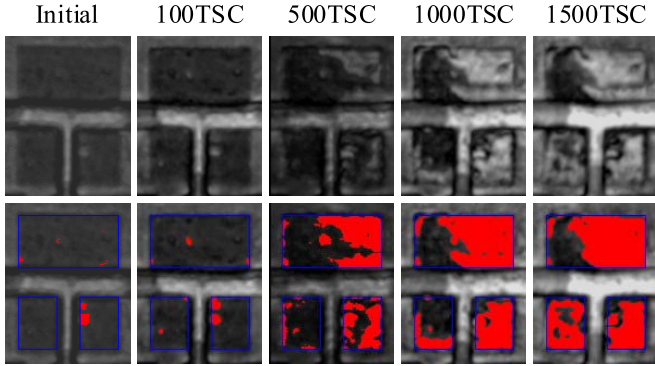


Fig. 3. Crack ratio of a FC-DA3 LED with raw SAM image on top and post-processed SAM images with marked solder joints (blue outline) and marked cracks (red areas) below. A crack ratio of 39% after 500 TSC, 56% after 1000 TSC and 67% after 1500 TSC is observed. Initial and 100 TSC image show only voids.

further aging stages (see Fig. 2). Without automatization, this high measurement effort would not be realizable.

Key parameter of the TTA is the thermal impedance $Z_{th}(t)$, representing the time resolved temperature change $\Delta T(t)$ for a change in power ΔP . $\Delta T(t)$ is measured indirectly via the temperature sensitivity SEN of the forward voltage $V_f(t)$ of the LED:

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P} = \frac{\Delta V_f(t)}{\Delta P * SEN}. \quad (2)$$

$Z_{th}(t)$ describes the thermal properties of the thermal path from LED junction to heatsink. A thermal degradation of any part of the thermal path results in an increase in $Z_{th}(t)$ [22]. A $Z_{th}(t)$ increase during aging is shown in Fig. 4 (a) for the FC-SP3 sample LED already shown in Fig. 3. The line color shifts from blue to red with rising TSC. Until 350 TSC the $Z_{th}(t)$ curves overlap, meaning that no degradation of the thermal path occurred. After 350 TSC, the steady-state values of the $Z_{th}(t)$ curves steadily rise from 7.50 K/W to 12.9 K/W, implying a continual degradation of the thermal path. The steady-state value represents the thermal resistance R_{th} and is a simple way to interpret TTA data. The results correlate with the crack ratio of the LED, where first cracks occurred at 500 TSC with a further growing afterwards.

Evaluation with R_{th} does not distinguish between degradation of different layers. This is only possible with the full $Z_{th}(t)$ curve. The degradation can be assigned to different layers depending on the separation time of the curves in $Z_{th}(t)$. The earlier the separation occurs, the closer spatially the degraded layer is to the LED junction and vice versa [6]. Hence, in [1] different time intervals were individually defined for all LED

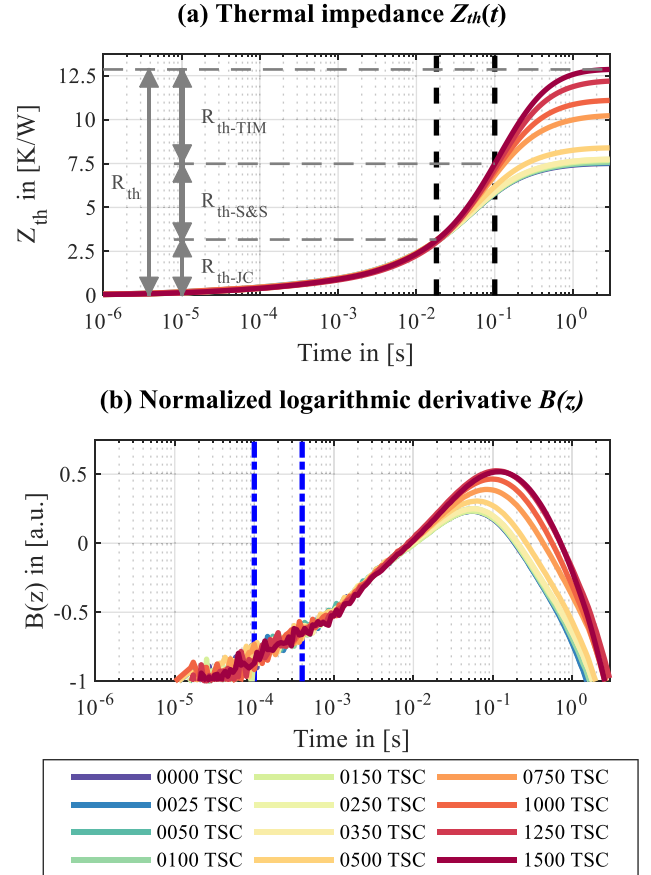


Fig. 4. Evaluation of the thermal degradation with (a) $Z_{th}(t)$ and (b) $B(z)$ while aging. Both methods show degradation after 350 TSC. $Z_{th}(t)$ is separated in three time intervals, marked by the dashed black lines. The increase inside the interval refers to the R_{th} of the section marked by gray arrows. Separation of lines occurs in the second interval due to crack in the solder joint. The normalization interval for $B(z)$ is marked with dash-dotted blue lines.

types to separate the thermal path into three main sections. The $Z_{th}(t)$ increase in these intervals is referred as R_{th} of these sections: LED package (R_{th-JC}), solder and substrate ($R_{th-S\&S}$) and thermal interface material (TIM) (R_{th-TIM}). Solder and substrate cannot be considered separately since both are too close together. The interval boundaries for FC-SP3 are included in

Fig. 4 (a) as vertical dashed black lines at 18 ms and 100 ms. The R_{th} of the intervals are marked with gray arrows at 1500 TSC. In case of the sample LED, the separation appears in the second interval at all TSC, indicating a degradation of solder or substrate. This degradation mode was verified by SAM inspection.

Besides the overall R_{th} and three sectional R_{th} , the normalized logarithmic derivative $B(z)$ is used for rating of the thermal integrity in this study. For calculation, the substitution $z = \ln(t)$ is applied to $Z_{th}(t)$. Afterwards, $Z_{th}(z)$ is differentiated by z and finally logarithmized:

$$B(z) = \log\left(\frac{1}{\Delta P * SEN}\right) + \log\left(\frac{dV_f(t)}{dz}\right). \quad (3)$$

The influence of ΔP and SEN is thereby reduced to a linear offset which can be compensated by a normalization in an appropriate time interval [23]. Especially for LEDs, this is a useful method since measurement of the actual ΔP is a complex and error-prone process using an optical sphere [24].

$B(z)$ curves for the sample LED are plotted in Fig. 4 (b). The normalization interval from 100 μs to 400 μs is marked with vertical dash-dotted blue lines and is identical for all LED types. As for qualification using $Z_{th}(t)$, the curves overlap until 350 TSC and afterward steadily increase. For quantitative comparison the peak height B_{max} and the peak position t_{max} is used, which both increase in case of degradation.

D. Electrical Analysis

A separated electrical inspection was not performed at any aging stage because $V_f(I_{Heat})$ and $V_f(I_{Sense})$ are contained in the TTA data as the last measurement point of the heating/sensing phases respectively. Both points are therefore measured in thermal equilibrium.

E. Cross-Sectional Analysis

Destructive cross-sectional analysis was performed after 500 TSC and 1000 TSC for two LEDs of each paste/LED type combination. These samples were used to verify SAM and TTA results but not for statistical evaluation.

IV. FAILURE MODES

The following section describes the six observed failure modes. Three of them are caused by cracks in the solder joint. The other three are independent of the solder joint. All failure modes can be distinguished solely with TTA data. Therefore, the relative increase (RI) in (a) R_{th} , (b) $R_{th-S\&S}$, (c) R_{th-JC} , and (d) $V_f(I_{Heat})$, and the absolute increase in (e) B_{max} are plotted for example LEDs of the failure modes in Fig. 5. SAM images and optical images are added as reference.

A. Thermal Degradation

Most common failure mode in this study was thermal degradation due to solder joint cracking. Cracks reduce the area for heat conduction and therefore increase $Z_{th}(t)$ resp. R_{th} . Thermal degradation was observed for all LED types.

TTA results of a VTF2 LED showing thermal degradation are plotted in Fig. 5 (a-e) as solid blue lines. The corresponding SAM image are included in the blue box below. (c) R_{th-JC} remains nearly constant since separation in $Z_{th}(t)$ due to solder cracks appears past the time interval for the LED package.

(a) R_{th} and (b) $R_{th-S\&S}$ both increase by approx. 120%. However, one would assume that the RI in $R_{th-S\&S}$ is stronger.

But an increase in R_{th} of a single layer not only leads to an increase in the $Z_{th}(t)$ -amplitude, but also to a time delay. This can be seen in Fig. 4 (a), where the saturation of $Z_{th}(t)$ emerges later with increased amplitude. The delay shifts parts of the thermal impact of the cracks past the fixed time interval for solder & substrate. These parts are not considered in $R_{th-S\&S}$ anymore. The delay can be explained using a Cauer RC-network to describe the thermal path [25]. An increase in R_{th} leads to a slower response of the network.

The RI in R_{th-S} & S thus does not fully represent the thermal impact of solder cracks. However, R_{th-S} & S is more stable against variations of the TIM likely to happen while performing a long-time-lasting study. A dynamic interval could solve this issue, but is not the focus of this study.

For (d) $V_f(I_{Heat})$, no changes are observed. (e) B_{max} shows a similar behavior like R_{th} and $R_{th-S\&S}$ and can be used as an alternative. SAM images of the sample verify solder joint cracking.

B. Electrical Degradation

Electrical degradation is an escalation of thermal degradation. The cracks in the electrical pads have grown so large that the electrical resistance has increased significantly. This failure mode was observed for samples of all LED types except the two lead frame LEDs FC-DA1 and VTF1. These show an overall slower crack growth as discussed later in this paper.

TTA results for a VTF2 sample LED showing electrical degradation are plotted in Fig. 5 (a-e) as red lines. SAM images are included in the red box below. Until 750 TSC, the behavior looks like thermal degradation for all TTA parameters. The electrical degradation begins after 750 TSC, and an (d) RI in $V_f(I_{Heat})$ of 18% is reached after 1500 TSC.

A higher $V_f(I_{Heat})$ results in a higher ΔP used in the $Z_{th}(t)$ calculated with (2). However, the additional electrical power is not converted in the LED die but in the solder joint below the submount. Therefore, $Z_{th}(t)$ seemingly decreases, visible particularly for (c) R_{th-JC} . For (a) R_{th} and (b) $R_{th-S\&S}$, the reduction is not observable due to overlapping thermal degradation. (e) B_{max} can compensate for changes in ΔP by normalization.

The sample SAM images show the stronger the crack growth in the electrical pads compared to the thermal degradation which causes this behavior.

C. Fall Off

The furthest escalation of solder joint cracking is fall off due to loss of mechanical connection. Only 18 LEDs of types TFFC-GB2 and TFFC-GB3 showed this damage extent.

TTA results of one FC-GB2 sample are plotted in Fig. 5 (a-e) as green lines. The behavior is like thermal resp. electrical degradation, but with a more intense increase, reaching an (a) RI in R_{th} above 120% after 1000 TSC.

D. Die Attach Degradation

A few FC-GB1 and VTF1 samples showed thermal degradation in the die-attach. TTA results of one VTF1 sample are

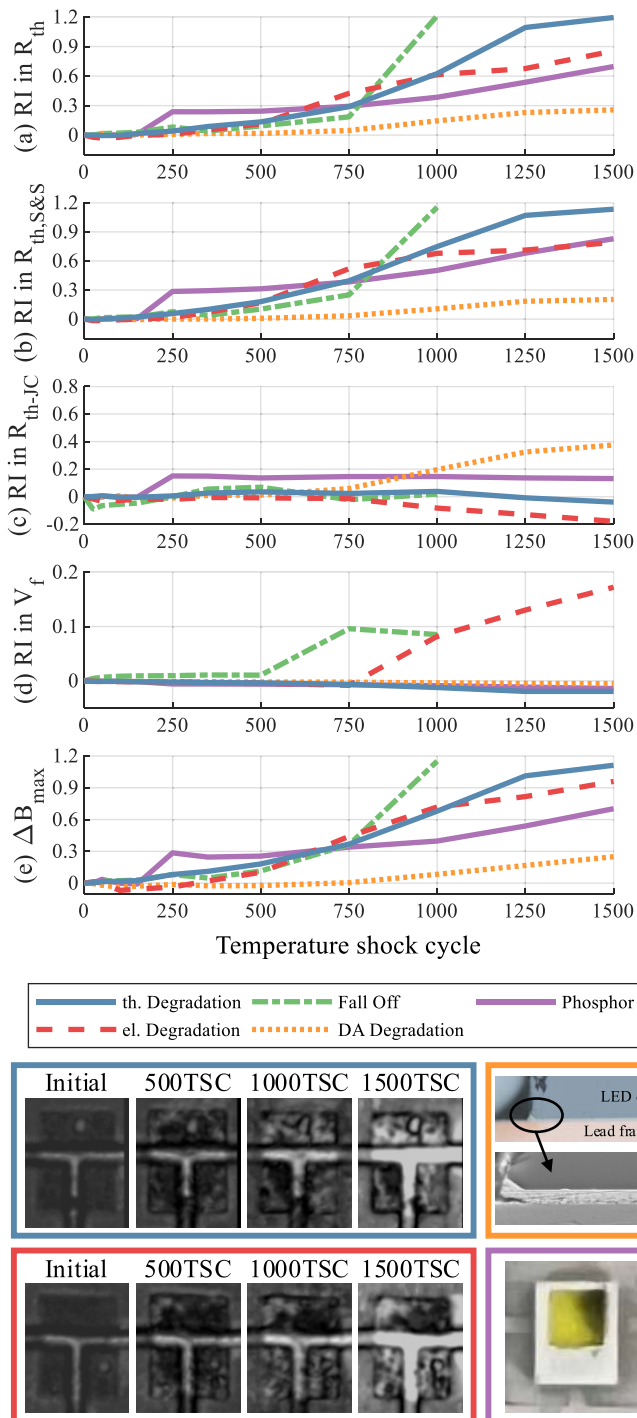


Fig. 5. Relative increase in different TTA parameters for five observed failure modes. Measurement points are not marked for reason of clarity. Below SAM, cross section and optical images are included to verify the failure mode. TTA can distinguish between the five failure modes.

plotted in Fig. 5 (a-e) as orange lines. The cross-sectional analysis with microscope and REM included in the orange box below reveals a die attach crack.

The die-attach degradation can be detected using (c) R_{th-JC} . Since the die-attach is closest to the LED die, the separation in $Z_{th}(t)$ appears earlier and inside the time interval for the LED package. The degradation starts at 750 TSC with a continuous increase to an RI of 39% after 1500 TSC. The

upstream degradation in the thermal path also affects the later time intervals producing the RI in R_{th} , $R_{th-S\&S}$ and B_{max} . The unique characteristic is the RI in R_{th-JC} . For a detailed view of $Z_{th}(t)$ see supplementary information Fig. 13.

E. Phosphor Darkening

In addition to continuous degradation, this study also revealed spontaneous degradation due to darkening of the phosphor. A specific cause for the darkening was not found. Most probably, chemical residues inside the thermal shock chamber are responsible [26]. In total, only 33 LEDs from all types except FC-GB3 and VTF1 showed phosphor darkening during two different cycling intervals. The chamber was cleaned after second observation, and the failure mode did not occur anymore.

TTA results for one VTF2 sample are plotted in Fig. 5 (a-e) as purple lines. A picture of the sample is included in the purple box. At 250 TSC, a spontaneous increase in R_{th} , $R_{th-S\&S}$, R_{th-JC} and B_{max} is observed. Due to the darkening, a greater part of the optical power is absorbed by the phosphor leading to higher losses and higher operation temperature. However, the electrical operation point is not affected and thus V_f (I_{Heat}) and ΔP remain constant. Therefore $Z_{th}(t)$ is increases.

F. Electrical Failure

Electrical failures were observed for two LEDs of type FC-GB3. One was observed at 100 TSC. This LED showed V_f (I_{Sense}) < 1.0V without any visible damage. The other one was observed at 500 TSC. This LED was electrically unstable and unable to generate light. The LED showed massive mechanical damage, maybe due to improper handling. Both LEDs were excluded from the statistical evaluation.

V. RESULTS

The following section evaluates the reliability of LED Types and solder pastes. Three different methods are described: average crack growth, average thermal degradation and lifetime estimation. This section focusses on the observations. Analysis and discussion follow in the next section.

A. Crack Growth

The average crack ratio of each group (same solder paste, same LED type) is depicted in Fig. 6 after 500, 1000 and 1500 TSC. Pastes are arranged with rising Ag content from left to right. LED Types are arranged according to the submount type. Initial and 100 TSC crack ratios are not included since no cracks were observed.

After 500 TSC, LEDs using thick film ceramic submounts already show a notable crack ratio, which correlates strongly with the Ag content of the paste. Lower Ag content leads to higher crack ratios. The thin film ceramic LEDs show a higher than average crack ratio, independent of the solder paste. Lead frame LEDs show no significant cracks after 500 TSC.

After 1000 TSC and 1500 TSC, the crack ratio further increases for thick and thin film ceramic submount LEDs. The correlation with the Ag content for thick film LEDs remains

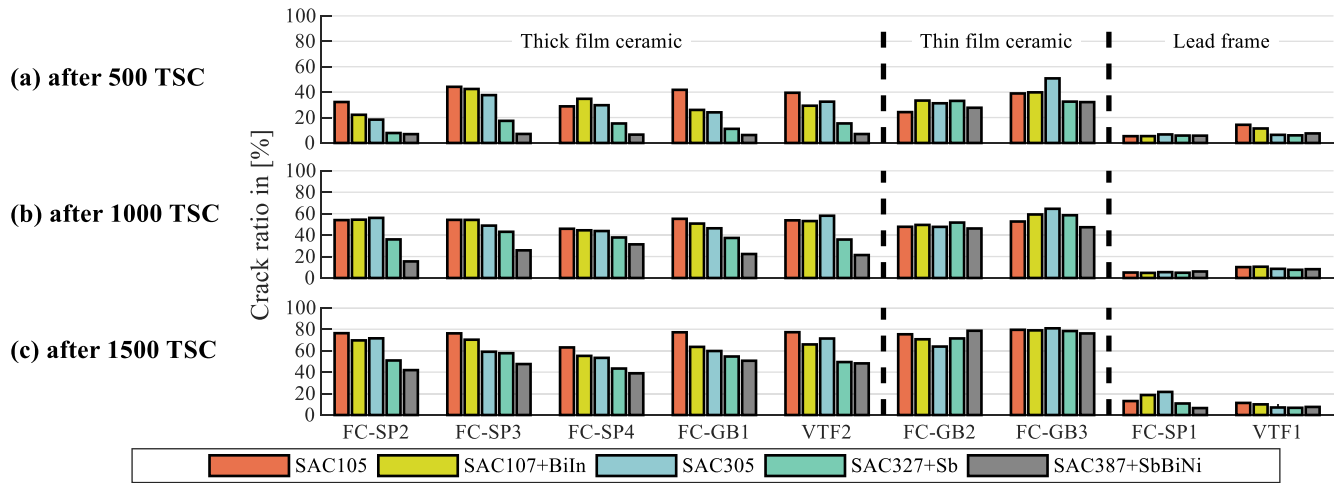


Fig. 6. Crack ratio after (a) 500 TSC, (b) 1000TSC and (c) 1500TSC for all LED types with on bar for each solder paste. The solder pastes are arranged with increasing Ag content from left to right. The LED types are sorted according to the submount technology.

valid at all aging stages. The lead frame LEDs showed only slight cracking even after 1500 TSC. This was also verified by cross-sectional analysis. Due to the smaller CTE mismatch between Al and Cu, the mechanical stress on the solder interconnect is lower.

B. Thermal Degradation

The average thermal degradation is depicted in Fig. 7 using the average RI in $R_{th-S\&S}$ during TSC for (a) VTF2 LEDs to compare pastes and (b) SAC305 to compare LED-Types. All other combination can be found the supplementary information and Fig. 14 and Fig. 15. The different submount technologies are indicated by the line style.

For VTF2 in (a), pastes with higher Ag content show a slower thermal degradation. This matches with the results from the crack growth evaluation and applies for all thick film ceramic LEDs (see supplementary information Fig. 14 and Fig. 15). Comparing the LED types for SAC305 in (b), the strongest thermal degradation was observed for the two thin film LEDs (dashed lines). The thick film LEDs (solid lines) show a smaller thermal degradation while the lead frame LEDs show no thermal degradation even after 1500 TSC. This is also consistent with the crack growth results.

C. Thermal and Electrical Lifetime Estimation

The mean thermal and electrical lifetimes τ of all groups were determined by at first defining different failure criteria (FailCT) and second fitting a Weibull distribution for failure statistic. If an individual LED exceeds a FailCT at a certain TSC, the LED is classified as failed in this FailCT starting from this TSC. Following FailCT were defined:

$$FailCT(RI \text{ in } R_{th}) \equiv 20\% \quad (F1)$$

$$FailCT(RI \text{ in } R_{th-S\&S}) \equiv 20\% \quad (F2)$$

$$FailCT(\Delta B_{max}) \equiv 0, 05 \quad (F3)$$

$$FailCT(RI \text{ in } V_f) \equiv 5\% \quad (F4)$$

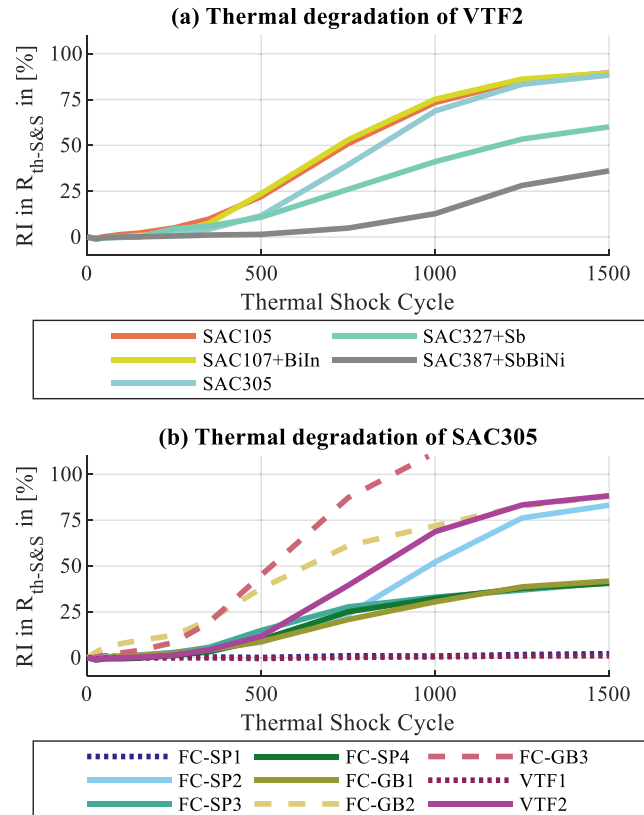


Fig. 7. Evaluation of thermal degradation during TSC using RI in $R_{th-S\&S}$ for (a) all VTF2 samples to compare the pastes and (b) all SAC305 samples to compare LED types. Different submounts are indicated by line style: Solid = Thick film; Dashed = Thin film; Dotted = lead frame.

A typical FailCT of 20% for RI in R_{th} and $R_{th-S\&S}$ was selected [27], [28]. A FailCT corresponding to a 20% RI in R_{th} was selected for ΔB_{max} as well (see [17] for details on this correspondance). Due to limitation in voltage measurement range of the TTA equipment, a FailCT of 5% instead of the typical 20% was chosen for the RI in V_f (I_{Heat}) [29].

The τ were computed from the resulting failure rates during TSC, assuming Weibull distributions for all FailCT. An

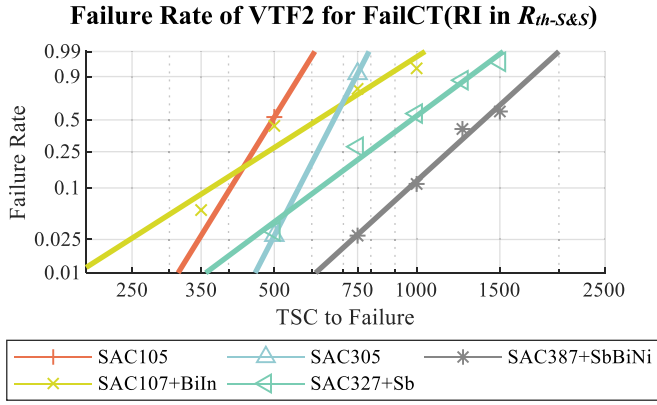


Fig. 8. Weibull plot of VTF2 for all five solder pastes for the FailCT RI in $R_{th-S\&S} = 20\%$. The markers represent the measured failure. The lines represent the fitted Weibull distribution.

exemplative Weibull plot is shown for VTF2 and FailCT (F2) in Fig. 8. Showing the Weibull plots for all LED types, solder pastes and FailCT wouldn't be practical, so the τ for all groups and all FailCT are summarized in Fig. 9. The solder pastes are sorted from left to right with increasing Ag content. LED Types are arranged according to submount types.

A determination of τ was not possible for LEDs using copper lead frame technology, as not enough LEDs exceeded one of the FailCT even after 1500 TSC. For LEDs using thin film ceramic, lower τ than for LEDs using thick film ceramic were observed for all FailCT. This corresponds to both previous evaluations. For thick film ceramic LEDs, a correlation of τ with the Ag content of the paste is observed. Higher Ag content increases τ .

Comparing the FailCT itself, the three thermal FailCT (F1-F3) result in a similar tendency for the computed τ . If a group achieves high τ for (F1), (F2) and (F3) are also high and vice versa. A slight difference in absolute value is observed between the τ of the same group for different FailCT. (F1) yields marginally higher τ than (F2) and (F3). The electrical FailCT (F4) does not fit to this relation. Some LEDs show a higher τ (e.g., FC-SP2) and some a lower τ (e.g., FC-SP4) than based on previous criteria. The reason is a higher sensitivity to electrical failure, which is discussed in more detail in the next section.

D. Correlation Between TTA and SAM

To investigate the correlation between TTA and SAM data, the RI in $R_{th-S\&S}$ is plotted against the crack ratio for each LED individually. The resulting point cloud for FC-SP3 LEDs is shown in Fig. 10 as an example. The data point color corresponds to the solder paste. Results after 500, 1000 and 1500 TSC are separated by marker shape.

Independent of solder paste, all FC-SP3 follow a common trend. Crack ratio has only a minor influence on the thermal performance below approx. 30%. Above this threshold, an increase of $R_{th-S\&S}$ with the crack ratio is observed, but with a relatively high variance. Inferring the crack ratio from the RI in $R_{th-S\&S}$ is therefore only possible to a limited extent.

The high variance is caused by different crack locations. Simulative analysis of the LEDs in the study revealed that first, cracks in the thermal pad have higher thermal impact than cracks in the electrical pads, and second, that intense cracking in a single solder pad has higher thermal impact than a homogenous crack distribution [30], [31]. However, taking crack location into account when comparing TTA and SAM data is not trivial. Detailed investigations are ongoing but not part of this paper.

The other LED types show a comparable behavior, where the threshold, after which cracks impact the thermal performance, varies between approx. 20% and 35%.

VI. ANALYSIS AND DISCUSSION

A. Influence of the Solder Paste

As mentioned in previous sections, the solder paste has a significant influence on crack growth, thermal degradation and τ . To visualize this correlation, τ is plotted against Ag content in Fig. 11. For each paste two data points are plotted in the same color. The squared shaped data point represents the average τ over all LED types using thick film ceramic. The circular data point represents the average τ over all LED types using thin film ceramic. Lead frame LEDs are not included due to lack of failed samples.

For thin film ceramic LEDs, higher Ag content results only in minor improvement in τ . Pastes only achieved a τ between 400 TSC and 620 TSC. SAC327+Sb reached the highest τ , even though it does not have the highest Ag content. This can be explained by the large stress due to CTE mismatch for those components. Apparently, the stress exceeds the yield strength of the high silver and doped SAC solders.

For thick film ceramic LEDs, the approx. 50 μm thick Cu layer reduces the CTE mismatch. The influence of paste is thus more significant. However, Ag content is not the only factor. Instead, the additives can be more decisive. SAC305 shows only a minor improvement towards SAC105, while SAC327+Sb, with only 0.2%wt more Ag than SAC305 reached a τ 42% higher. SAC387+SbBiNi achieved a 105% higher τ compared to SAC305 with 0.8%wt more Ag. However, for SAC107+BiIn no improvement was observed compared to SAC105 which has the same Ag content.

B. Influence of the LED Package Design

Besides the solder paste, LED package design also has a significant influence on the reliability. The highest τ was achieved by the lead frame LEDs, where not enough samples failed even after 1500 TSC to determine τ .

The CTE mismatch between Cu and the Al of the substrate is smaller than between AlN and Al, so the mechanical stress on the solder joint is smaller. The Cu lead frame does increase the mechanical stress on the die attach, but only two samples of VTF1 showed degradation of the die attach after 1500 TSC.

Thin film ceramic on the other hand is unfavorable for τ . FC-GB2 and FC-GB3 showed distinctly smaller τ compared to the thick film LEDs. The Cu layer acts as a buffer for the solder interconnect towards the rigid AlN. For the thin film ceramic, this buffer is missing which increases the mechanical

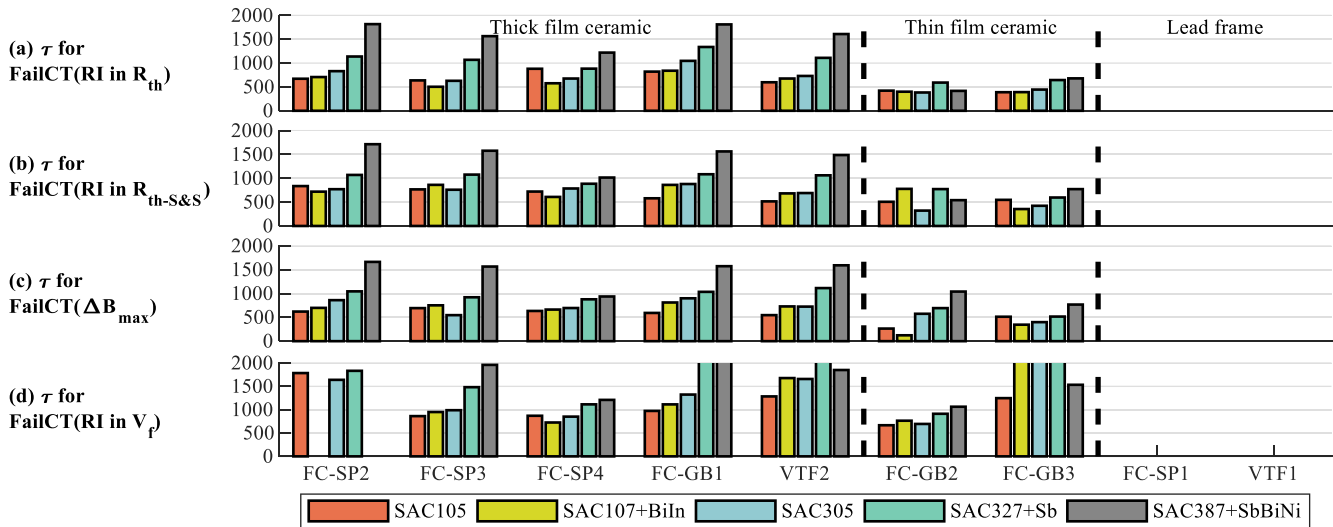


Fig. 9. Mean lifetime τ of groups (same LED type, same solder paste). τ was determined for four different limits (F1-4). Solder pastes are sorted from left to right with increasing Ag content. If τ was not determinable due to lack of failed samples, no bar is drawn. If τ is above 2000 TSC, the bar is open on the top side.

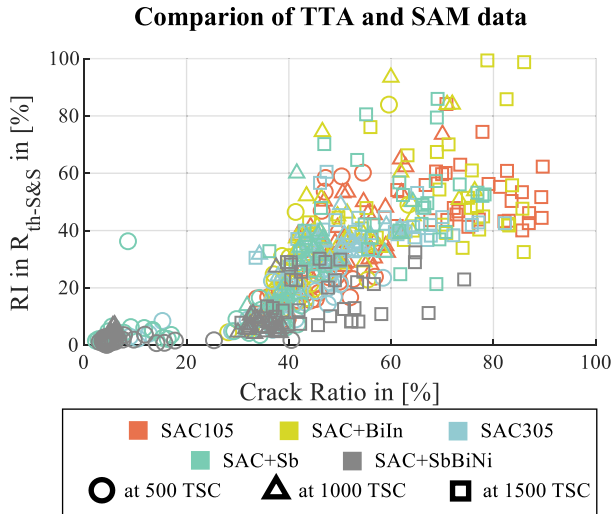


Fig. 10. Correlation of crack ratio from SAM data and relative increase in R_{th} from TTA data for all FC-SP3 LEDs at 500, 1000 and 1500TSC.

stress. Altogether thick film ceramic LEDs achieved higher τ compared to thin film ceramic LEDs.

The influence of solder pad design on τ is evaluated using the five thick film ceramic LEDs. Three influential parameters were identified. The pad area (bigger is better), the gap between the pads (smaller is better) and the pad ratio between thermal and electrical pad (smaller resp. balanced is better). All are listed in Table I. For use in the combined rating, each parameter is scaled relatively to the best value of all thick film ceramic LEDs in the particular category. Thus, all parameters are between 0 and 1, where higher values are better.

Using these three parameters, a package rating for the thermal reliability is defined for each package. A weight of 1 is used for pad area and pad gap and a weight of 0.5 for the pad ratio. The resulting package rating for thermal reliability is plotted against τ for (F1) in Fig. 12 (a). The reliability rating

Influence of the solder paste on the Lifetime

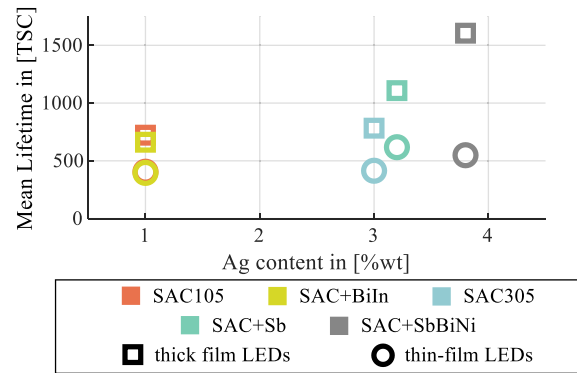


Fig. 11. Mean lifetime τ of thick film ceramic LEDs and thin film ceramic LEDs dependent on the Ag content of the solder paste.

describes the relation between pad design and lifetime quite well even though the weights were not fitted but chosen by experience. However, for a more accurate evaluation further packages and simulations are required.

Similarly, a package rating was defined for electrical reliability. Only the pad ratio is chosen here. The package rating for electrical reliability is plotted against τ for (F4) in Fig. 12 (b). The variation is described quite well. The reason why the pad ratio is particularly important for electrical reliability is the mechanical stability of the individual pads. The smaller the electrical pads are compared to the thermal pad, the lower the mechanical strength and the earlier the crack initiation in the electrical pads.

C. Influence of Voiding

To evaluate the influence of voids in the solder joint on lifetime, the void ratio was compared to the cycles-to-fail for the individual LEDs. To describe the correlation between those two parameters within each sample group (same LED type,

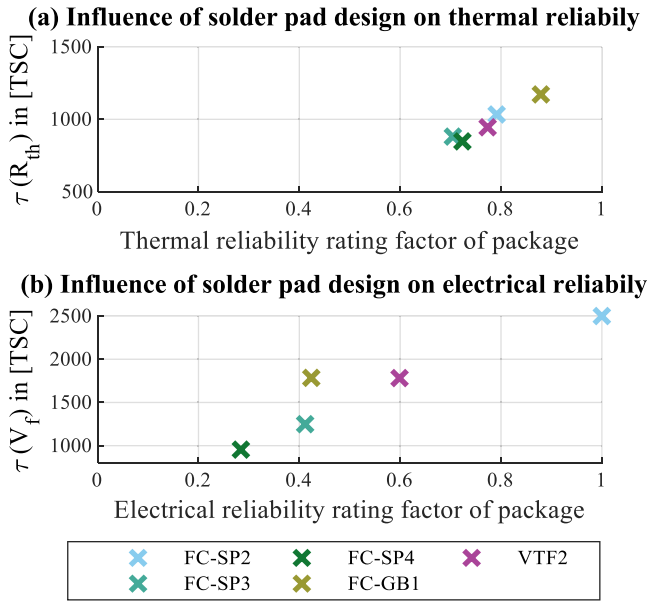


Fig. 12. Package rating for (a) thermal reliability and (b) electrical reliability against achieved lifetime according to limit (L1) resp. (L4). The packing rating is determined from the solder pad design parameters pad size, gap between pads and size ratio between thermal and electrical pad.

same paste) a linear fit was chosen. The coefficient of determination R^2 was used to assess the significance of the correlation. With 0.053 on average no significant correlation was identified, meaning that the void ratio has no influence on the lifetime in this study. A better prediction by use of other fitting functions was not productive.

It should be mentioned that due to the vacuum soldering process, a very low voiding ratio below 5% on average was achieved. A correlation between void ratio and lifetime could still exist for higher void ratios but cannot be tested for within this study.

VII. OPEN-SOURCE DATASET

The full data set of this study is published open source at www.kaggle.com under “Reliability of High-Power LEDs and Solder Pastes”.

VIII. CONCLUSION

An extensive reliability study with 1800 white high-power LEDs was carried out, investigating nine LED packages from different manufacturers and five SAC+ solder paste with different Ag content and additives. As substrate an Al-IMS-PCB was used. Thermal shock cycling (-40 °C/+125 °C/30 min) until 1500 cycles was used for accelerated aging and the thermal degradation inspected at multiple intermediate aging stages by TTA and SAM.

SAM images were used to determine the crack ratio for each LED individually. While lead frame LEDs showed nearly no cracks even after 1500 TSC, thick film ceramic LEDs showed crack growth strongly dependent on the paste composition. Thin film ceramic LEDs instead had the highest crack ratio, nearly independent of the paste indicating that the high thermomechanical stress exceeds the improved yield strength obtained by the Ag and the additives.

With R_{th} , R_{th-JC} , $R_{th-S&S}$, B_{max} and V_f (I_{Heat}) five parameters were extracted from TTA data. A comparison between TTA and SAM data showed that cracks in the solder joint only have a significant thermal impact above approx. 25% crack ratio.

TTA data was further used to evaluate failure modes. With thermal degradation, electrical degradation, fall off, die attach degradation and phosphor darkening, five failure modes were identified. All are distinguishable by TTA data alone.

TTA was also used to determine the average lifetime dependent on solder paste and LED type. By means of this average lifetime both the paste composition and the package design were rated. Overall, the thin film ceramic LEDs showed the shortest lifetimes. Even high Ag pastes can't increase the reliability. For lead frame LEDs, only a few samples failed for all pastes until 1500 TSC. Due to the lower CTE mismatch between Cu and Al, the solder joint suffers less mechanical stress, increasing the lifetime. However, lead frame LEDs feature higher mechanical stress on the die attach, but only two samples with a die attach failure were observed in this study. The thick film ceramic LEDs showed the highest dependency on solder paste and package resp. solder pad design. For solder pastes, the highest influence was assigned to the additives in the paste, far more decisive than the Ag content. For the pad design three influential parameters were identified. A larger solder area, a smaller gap between the pads and balanced pad ratio between thermal and electrical pads improve the reliability.

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