Introduction

Graphene is an interesting electronic material with ultra-high charge carrier mobilities. Therefore, it has been proposed as a transistor material with a very fast response. Due to the lack of a gap in its energy spectrum, however, its switching capabilities are poor. In this paper, we consider graphene as a metal, suited for atomically flat electrodes. The following experiment proposes a transistor testbed that can be used to evaluate any semiconducting material on graphene electrodes. Graphene has previously been used in several experiments as a contact material to organic semiconductors and to conventional semiconductors. In our case, the graphene has epitaxial quality, which brings along a well-defined work function. For the proof of principle, we use standard carbon-based semiconductors in the transistor channel: P3HT as one of the most frequently used p-type polymer semiconductors and fullerenes as an example for n-type semiconductors. This material combination has the interesting property that the all-important metal/semiconductor interface is entirely carbon based. Further, this transistor concept avoids any roughness in the electrode as well as in the channel area, as the semiconductor spreads over the atomically flat graphene electrodes and the atomically flat SiC substrate without a significant step in between.

The graphene species we use is epitaxial graphene on a SiC (0001) wafer, grown by thermal decomposition. It uses SiC both as a substrate but also as carbon source for the graphene growth. The result is large-area graphene in epitaxial registry with respect to the single-crystal wafer. As SiC is a wide-bandgap semiconductor, it can be chosen as highly insulating, but also as a well conducting material, depending on doping. In our case, we have conducted a conducting plane ~1200 nm below the surface of a semi-insulating 6H–SiC wafer by implantation of dopants. This serves as electrostatic gate with respect to the graphene plane at the wafer surface, because the SiC area in between acts as gate dielectric up to applied voltages of ~100 V.

Experimental

The bottom gate was structured and contacted in a semi-insulating 6H–SiC(0001) wafer (II-VI Inc.) either by aluminum implantation ([Al] = 2.13 × 10^{12} cm^{-2}, used for P3HT transistor in Fig. 3), or by nitrogen implantation with reduced ion dose ([N] = 1.1 × 10^{13} cm^{-2}, used for fullerene and P3HT transistors), following the strategies and recipes of ref. 16 and 17. Subsequently, the samples were heated in Ar atmosphere at 1750 °C in a cold-wall reactor. Under these conditions, high-quality monolayer graphene (MLG) is formed. It is known that this graphene species is not charge neutral, but has a charge carrier density of n = 10^{13} cm^{-2}, a work function of \( \Phi = 4.31\) eV, and charge carrier mobilities of \( \mu_{\text{graphene}} = 1000 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1} \) at room temperature. In a next step, the graphene was patterned by standard e-beam lithography, such that source and drain electrodes were defined (channel length \( l = (5–10) \mu\text{m} \), width \( w = 1000 \mu\text{m} \) or \( w = 400 \mu\text{m} \) and fitted with Ti/Au contact pads. P3HT was spin coated and subsequently patterned by an oxygen etch using an aluminum mask such that P3HT covered the source, channel and drain area. For the fullerene samples,
fullerenes were deposited by thermal evaporation through a PMMA shadow mask (thickness (70–100) nm), and immediately transferred to a cryostat (sample in vacuum). For the latter, care was taken that the freshly prepared fullerene layer was exposed to air less than 5 minutes. The device structure is sketched in Fig. 1.

Results and discussion

For the analysis of data, we use the standard MOSFET models.\textsuperscript{18} They distinguish two regimes. The first is the linear regime, when the difference between gate and threshold voltage is greater than the drain voltage ($V_{GS} - V_{T} > V_{DS}$). In this case the source current depends on the drain voltage as

$$I_{lin} = \frac{\mu C_{w} V_{DS}}{l} \left(V_{GS} - V_{T} - \frac{V_{DS}}{2}\right)$$  \hspace{1cm} (1)

with threshold voltage $V_{T}$ and the gate capacitance $C$ per area. $C = 6.9 \text{nF cm}^{-2}$ was determined from the plate capacitor formula with SiC as dielectric ($d = 1.25 \mu m$). The validity of this approximation was previously confirmed.\textsuperscript{16,17}

In the second regime, when the drain voltage is equal or greater than the difference between gate and threshold voltage ($V_{DS} \approx V_{GS} - V_{T}$), the current saturates due to the channel pinch-off and is given by:

$$I_{sat} = \frac{\mu C_{w}}{2l} (V_{GS} - V_{T})^{2}$$  \hspace{1cm} (2)

Note that eqn (1) and (2) are exemplarily given for n-channel MOSFETs. For p-channel FETs the sign of the voltages has to be changed.

Polythiophene as prototypical p-type semiconductor

A first and all-important step is to check the electrical contact properties of the graphene-semiconductor interface. For this purpose, we used bottom-gated transistor structures with various channel lengths $l$. At first, we discuss the case of P3HT.

Fig. 2a shows the normalized zero-bias resistance $R_{lin} \times w$ determined from the linear regime for voltages $V_{DS} < 2 \text{ V}$ as a function of the channel length $l$. For all gate voltages $V_{GS}$ investigated, a linear dependence is observed. The extrapolation to zero length results in a contact resistance $R_{contact} = (0.20 \pm 0.05) \Omega \text{ cm}$. This value is almost independent of the channel resistance $R_{channel}$ of each device, which is parametrically varied by $V_{GS}$. This is expected as the monolayer graphene/SiC interface screens the gate effect of the bottom gate due to Fermi level pinning,\textsuperscript{16,17} which is enforced by silicon dangling bonds underneath the graphene layer. Note that the P3HT on top of the graphene contact is consequently un gated. $R_{contact}$ therefore includes the graphene resistance (negligible), the transition from graphene to ungated P3HT and the resistive pathway in P3HT above the source and drain electrodes (see Fig. 2b). This evaluation scheme cannot be applied to fullerenes, as the zero-bias resistance is not linear (see below).

Fig. 2 (a) Normalized zero-bias resistance $R_{lin} \times w$ measured on three P3HT transistors with different channel length $l$, each evaluated for four gate voltages $V_{GS}$. The contact behaves entirely ohmic. The contact resistance $R_{contact}$ is extracted using the transfer length method (TLM). (b) Scheme of the contributions to $R_{lin} = 2R_{contact} + R_{channel}(V_{GS})$. The arrows indicate the gate electric field, which influences only $R_{channel}$ of the semiconductor in the transistor channel. The graphene/semiconductor contact areas with $R_{contact}$ are unaffected by the gate due to Fermi level pinning at dangling bond states below graphene.

For the given transistor scheme, two problems occurred, which had to be solved: (i) gate electric field screening by surface states and (ii) gate leakage.

Ad (i). In first experiments, we observed almost no gate effect as can be seen in Fig. 3a. This problem was presumably due to surface-near defects in the substrate or interface, which were
generated by the removal of the graphene in the channel area. It turned out that milder conditions (RF power: 15 W, 1 min instead of 100 W, 15 s) during the oxygen plasma etch as well as a HF dip prior to semiconductor deposition solved the problem (see Fig. 3b). We conclude that the gate effect was spoiled either by plasma-induced surface-near defects in SiC, which are avoided by milder etching conditions, or by the uncontrolled formation of a thin SiO₂ layer with high interface trap density.

Ad (ii). Despite our expectation that an aluminum-doped bottom gate is favorable for the creation of holes in p-type materials, it turned out that for the given experiment nitrogen-doping is advantageous. Under these conditions, the n-type/intrinsic junction is driven in forward direction. This limits the applicable gate voltage to approximately $-20 \text{ V}$. The advantage, however, is that less implantation-induced defects are created in the gate dielectric, which reduces the gate leakage current significantly. In the following, only nitrogen-doped bottom gates are used.

Fig. 4 shows the output and transfer characteristics taken on a P3HT transistor fabricated with optimized processing conditions. The output characteristic clearly reveals a linear regime for source–drain voltages $V_{\text{DS}} < 2 \text{ V}$ and a saturation regime at high $V_{\text{DS}}$ values (dependent on the gate voltage $V_{\text{GS}}$). The transfer characteristic measured at $V_{\text{DS}} = -20 \text{ V}$ is depicted in Fig. 4b. The left scale corresponds to the square root of $I_{\text{DS}}$. The linear curve observed at $V_{\text{GS}} < 5 \text{ V}$ proves that the transistor behaves closely to an ideal MOSFET and eqn (2) can be applied for the saturation current.

The on/off ratio of the P3HT transistor is $\approx 10^2$. From the transfer characteristic, a threshold voltage $V_t = 20 \text{ V}$ is obtained by extrapolation of the $I_{\text{DS}}^{-1/2}$-$V_{\text{GS}}$ curve (cf. Fig. 4b). Further, from the maximum slope $dI_{\text{DS}}^{-1/2}/dV_{\text{GS}}$ a field-effect mobility of $\mu_{\text{FE}} = 5 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is extracted, which is a typical value for P3HT. The effective mobility $\mu_{\text{eff}} = 5 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ can be calculated from the slope of the linear regime of the output characteristic employing eqn (1) for $V_{\text{DS}} < -5 \text{ V}$, where it is in perfect agreement with $\mu_{\text{FE}}$. We explicitly included the contact resistance $R_{\text{contact}}$ by rescaling of $V_{\text{DS}}$:

$$V_{\text{DS,channel}} = V_{\text{DS,measured}} - 2R_{\text{contact}}I_{\text{DS}}$$

This correction is relatively small ($<10\%$), which displays the high quality of the all-carbon graphene to P3HT contact.
Fullerene as prototypical n-type semiconductor

As an example for an n-type semiconductor, we used a fullerene layer deposited by thermal evaporation. On a first glance, the fullerene/graphene contact seems to be particularly homogeneous, as two pure sp\(^2\) carbon materials are in contact. However, when investigating these transistors at room temperature, very poor conduction was observed. The bad conductivity is related to rotational dynamics of the single fullerene molecules.\(^{19}\) The conduction improved substantially by three orders of magnitude when cooling down the sample to about 100 K. At this temperature, the rotational dynamics is largely frozen out.

Fig. 5a displays the output characteristics of a fullerene transistor with graphene electrodes at 100 K. As expected for an n-type semiconductor, the source-drain current \(I_{DS}\) increases with increasing gate voltage \(V_{GS}\). Although there is a significant gate effect, a linear regime at small \(V_{DS}\) is missing. Instead, a super-linear increase of \(I_{DS}\) is observed. This indicates that the fullerene/graphene contact is not ohmic, but rather Schottky-like. This observation elucidates how different both carbon allotropes are electronically. Nevertheless, the transistor is functional and reaches on/off ratios of \(3 \times 10^3\) as can be seen in the transfer characteristic (Fig. 5b). The current \(I_{DS}\) in the saturation regime depends on \(V_{GS}\). Thus, a field effect mobility according to eqn (2) can be evaluated resulting in \(\mu_{FE} = 0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}\) for \(V_{GS} > 10\text{ V}\). Note that this value is a rough estimate as the contact resistance is essentially unknown and may influence the result significantly.

Conclusions

Epitaxial graphene with implanted bottom gate in SiC (0001) can be used as a testbed to investigate the semiconducting field-effect transistor operation of new materials under extremely well-controlled conditions. The well-defined work function of epitaxial graphene (independent of applied backgate voltages) and its zero roughness provide reproducible (metallic) source and drain electrodes without any gate effect in the contact area. The zero roughness continues also in the bottom gated transistor channel area at the clean and atomically flat SiC surface with practically no step in between. The screening effect of the SiC/epitaxial graphene interface provides a spatially sharp separation of contact area and channel.

For the p-type semiconductors P3HT, perfect ohmic injection and transistor operation according to standard MOSFET models is observed. This allows an accurate determination of parameters. We expect that this analysis can be extended to many other p-type organic semiconductors electronically similar to P3HT. The testbed can be used also for fullerenes as an example for n-type semiconductors, where transistor operation was observed. The obvious Schottky-like contacts indicate work function mismatch. Consequently, a linear regime in the output characteristic is missing and the determination of parameters is less meaningful.

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Notes and references