Simulation and Modeling of Silicon-Carbide Devices

Simulation und Modellierung von Siliziumkarbid-Bauelementen

der Technischen Fakultät
der Friedrich-Alexander-Universität
Erlangen-Nürnberg
zur Erlangung des Grades

Doktor-Ingenieur

vorgelegt von

Viktoryia Uhnevionak
aus Genf
Als Dissertation genehmigt

von der Technischen Fakultät
der Friedrich-Alexander-Universität Erlangen-Nürnberg

Tag der mündlichen Prüfung: 10/03/2015

Vorsitzende des Promotionsorgans: Prof. Dr.-Ing. M. Merklein

Gutachter: PD Dr. Peter Pichler
  Prof. Dr.-Ing. Robert Weigel
Abstract

In recent years, silicon carbide (SiC) became an attractive material and opened new perspectives in power electronics due to its superior material properties. The wide bandgap, high thermal conductivity and high breakdown electric field make SiC a material of choice for power MOSFETs. The incorporation of SiC MOSFETs, for example, in power converters allows to decrease their weight and size. This can be a big advantage for many applications including electric cars. The ability of SiC devices to withstand high temperatures simplifies the thermal management of the electrical systems. However, the commercial use of MOSFETs is currently limited by technological problems which result in low channel mobility and high turn-on voltage.

The aim of this thesis was to understand and explain the mechanisms which control the channel mobility in SiC MOSFETs using numerical simulation and to develop a self-consistent simulation methodology for a description of their electrical behavior. For technological progress, development and optimization of semiconductor devices, TCAD simulation became an increasingly important tool of investigation. However, for SiC devices TCAD simulation currently is a big challenge. Most of the simulation models were developed for silicon, and, thus, can not adequately describe the transport properties of SiC devices. Moreover, because of a high density of interface traps at the SiC/SiO₂ interface, which strongly degrade the channel mobility of SiC MOSFETs, an accurate interface trap model is of primary importance for the simulation.

In the framework of the MobiSiC (Mobility Engineering for SiC Devices) project lateral n-channel 4H-SiC MOSFETs have been fabricated and electrically characterized by current-voltage and Hall-effect measurements. The effects of temperature and bulk potential engineering upon the transport properties in the channel of SiC MOSFETs have been studied. The interpretation of the electrical measurements, i.e. current-voltage characteristics $(I_D(V_G))$ as well
as sheet carrier density and channel mobility obtained from the Hall-effect measurements \( n_{inv}(V_G), \mu(V_G) \), has been performed within this work using numerical simulation with Sentaurus Device of Synopsys.

For an accurate evaluation of the Hall-effect measurements, a new method for the calculation of Hall factors was developed. It is based on the fact that both Hall factor and mobility depend on the same mechanisms by which the charge carriers are scattered. The method of calculation accounts for all electron scattering mechanisms in the active area of the device. Thus, for the first time, an accurate Hall factor has been calculated for the channel of MOSFETs and applied for the correction of the Hall-effect measurements.

Experimental data, for example from Hall-effect measurements, is often used to characterize the density of interface traps. In this work, a new method, which allows a more accurate characterization, is suggested. In the first step, the densities of the interface traps versus trap energy \( D_{IT}(E_T) \) are extracted from the Hall-effect and capacitance-voltage measurements using a conventional method. Afterwards, the extracted \( D_{IT}(E_T) \) distributions are introduced into Sentaurus Device and optimized numerically to minimize the deviations between the numerically simulated characteristics \( n_{inv}(V_G), \mu(V_G), \) and \( I_D(V_G) \) and the experimentally measured data. The numerical simulation allows to take into account, for instance, the effects of potential drop along the channel between source and drain as well as the Fermi-Dirac distribution of the electrons. These effects are neglected when the interface trap density is extracted conventionally from the experimental data. Thus, it is expected that the new method produces physically more reasonable results on the \( D_{IT}(E_T) \) distributions. Based on the experimental and simulated results, origin and nature of the interface defects are discussed.

The simulation methodology, in which the method of the Hall factor calculation and the method of the \( D_{IT}(E_T) \) extraction are accounted for, could consistently describe the temperature dependence as well as the doping dependence of the transport properties of SiC MOSFETs studied in this thesis. On the basis of a good agreement between simulations and measurements, a comprehensive interpretation of the scattering mechanisms in the channel of SiC MOSFETs with different doping concentrations and at different temperatures has been performed. One of
the main findings from this work is that a decrease of the interface trap density is not the only factor which can improve the performance of SiC MOSFETs. For example, their performance can be improved significantly by decreasing the doping concentration of the channel. It was also found that the doping concentration of the channel affects the temperature dependence of the channel mobility: At elevated temperatures for highly doped MOSFETs it increases with increasing temperature while for lowly doped ones it decreases.
Zusammenfassung


Der Zweck dieser Doktorarbeit war, durch numerische Simulationen den Mechanismus zu verstehen und zu erklären, der in SiC MOSFETs die Kanalbeweglichkeit bestimmt und eine selbstkonsistente Simulationsmethodologie zur Beschreibung der elektrischen Eigenschaften von SiC MOSFETs zu entwickeln. Für den technologischen Fortschritt, sowie für die Entwicklung und Optimierung von Halbleiterbauelementen ist der rechnergestützte Entwurf von elektronischen Bauelementen und ihrer Herstellung (TCAD – Technology Computer Aided Design) zu einem zunehmend wichtigen Untersuchungswerkzeug geworden. TCAD-Simulationen für SiC-Bauelemente sind aktuell jedoch eine große Herausforderung. Die meisten Simulationsmodelle wurden für Silizium entwickelt und können deshalb die Transporteigenschaften von SiC-Bauelementen nicht adäquat beschreiben. Darüber hinaus ist die Grenzschicht zwischen Siliziumkarbid und Gateoxid durch eine hohe Konzentration von
Haftstellen charakterisiert, die die Kanalbeweglichkeit in SiC-MOSFETs stark degradieren. Deshalb ist ein genaues Modell für die Haftstellen an der Grenzschicht von vorrangiger Bedeutung für die Simulation.

Im Rahmen des Projekts MobiSiC (Mobility Engineering for SiC Devices) wurden laterale n-Kanal 4H-SiC MOSFETs hergestellt und elektrisch durch Strom-Spannungs- und Halleffektmessungen charakterisiert. Die Effekte von Temperatur und Substratdotierung auf die Transporteigenschaften im Kanal von SiC MOSFETs wurden untersucht. Die Interpretation sowohl der Strom-Spannungskennlinien \( I_D(V_G) \) als auch der aus den Halleffektmessungen abgeleiteten Schichtladungsträgerkonzentrationen und Kanalbeweglichkeiten \( n_{inv}(V_G), \mu(V_G) \) wurden in dieser Arbeit mit Hilfe numerischer Simulationen mit Sentaurus Device von Synopsys durchgeführt.


Experimentelle Daten, z. B. von Halleffektmessungen, werden oft zur Charakterisierung der Dichte von Haftstellen an der Grenzschicht verwendet. In dieser Arbeit wird eine neue Methode vorgeschlagen, die eine genauere Charakterisierung erlaubt. In einem ersten Schritt werden Haftstellendichten als Funktion der Energie \( D_{IT}(E_T) \) von Halleffekt- und Kapazitäts-Spannungsmessungen auf konventionelle Art extrahiert. Danach werden sie in Sentaurus Device eingegeben und numerisch optimiert um die Abweichungen zwischen den simulierten Kennlinien \( I_D(V_G), n_{inv}(V_G) \) und \( \mu(V_G) \) und den Messungen zu minimieren. Die numerische Simulation erlaubt, Effekte wie z.B. die Potentialverteilung zwischen Source und Drain sowie die Fermi-Dirac-Verteilung der Elektronen zu berücksichtigen. Solche Effekte bleiben bei der konventionellen Extraktion der Haftstellendichte unberücksichtigt. Es ist deshalb zu erwarten,

Die Simulationsmethodologie, in die die Methode der Berechnung von Hallfaktoren und die Methode der Extraktion der Haftstellendichte eingingen, konnte konsistent die Temperaturabhängigkeit sowie die Konzentrationsabhängigkeit der Transporteigenschaften der in dieser Arbeit betrachteten SiC MOSFETs beschreiben. Auf der Basis der guten Übereinstimmung zwischen Simulationen und Messungen konnten die Streumechanismen im Kanal von SiC MOSFETs mit unterschiedlichen Dotieratomkonzentrationen und bei unterschiedlichen Temperaturen umfassend interpretiert werden. Eine der Haupterkenntnisse dieser Arbeit ist, dass eine Verringerung der Grenzflächenhaftstellendichte nicht der einzige Faktor zur Verbesserung der Eigenschaften von SiC MOSFETs ist. Ihre Eigenschaften können z.B. auch durch eine Verringerung der Kanaldotierung erheblich verbessert werden. Weiterhin wurde gefunden, dass die Konzentration der Kanaldotierung die Temperaturabhängigkeit der Kanalbeweglichkeit beeinflusst: Bei hochdotierten MOSFETs steigt sie mit der Temperatur während sie sich bei niedrig dotierten MOSFETs verringert.
Contents

Abstract .................................................................................................................................................. i

Zusammenfassung ....................................................................................................................................... v

Chapter 1 Introduction ................................................................................................................................... 1

1.1 SiC as a wide bandgap semiconductor .............................................................................................. 1

1.2 TCAD for the development and optimization of semiconductor devices ....................................... 4

1.3 Lateral 4H-SiC MOSFETs: Literature review .................................................................................. 6

1.4 Thesis outline ...................................................................................................................................... 8

Chapter 2 Simulation and Experimental Setup ....................................................................................... 11

2.1 Basic concept of a device simulation ............................................................................................... 11

2.2 Description of the MOSFET structures and fabrication processes ............................................... 13

2.3 Description of electrical measurements of SiC MOSFETs .............................................................. 15

Chapter 3 Physical Models ..................................................................................................................... 17

3.1 Fermi-Dirac statistics ......................................................................................................................... 17

3.2 Bandgap energy and its temperature dependence ............................................................................. 19
Thesis Publications ............................................................................................................. 131
List of Figures ....................................................................................................................... 133
List of Tables .......................................................................................................................... 139
List of Symbols ...................................................................................................................... 141
Index ....................................................................................................................................... 145
Chapter 1  Introduction

1.1  SiC as a wide bandgap semiconductor

Today, silicon (Si) is the basic material for the manufacturing of most power semiconductor devices. In many fields of application, however, Si-based power electronics has already reached its theoretical limit. An increase of the need of electric power as well as the rising costs of energy makes silicon less competitive for many applications. An efficient energy management becomes one of the utmost challenges at the present time. One of the solutions to meet high power requirements is to replace silicon by wide-bandgap (WBG) semiconductors, e.g. silicon carbide (SiC), gallium nitride (GaN), a diamond, the properties of which are very exciting [1]:

Firstly, the use of WBG semiconductors for the electronic devices has the advantage for high-temperature operation where an uncontrolled conduction of electrons is prevented due to the higher thermal energy needed for electrons to move from the valence band to the conduction.

Secondly, WBG semiconductors have a large electric breakdown field which results in higher breakdown voltages ($V_{BR}$) for power devices and allows usage of much higher doping levels for the same $V_{BR}$ in comparison with Si. As a result, WBG-semiconductor-based power devices have lower on-resistances of the drift region.

Thirdly, the electron saturation velocities of the WBG semiconductors are higher than in Si. Considering that saturation velocity is directly proportional to the high-frequency switching capability of a semiconductor, WBG semiconductor-based power devices could be switched at higher frequencies than Si-based ones.
Fourthly, SiC and diamond have higher thermal conductivities in comparison with Si. This property allows material to dissipate the heat of the device to its surroundings better, resulting in lower increase of the device temperature. As a conclusion, due to the wide bandgap, devices built with WBG materials can operate at higher temperatures, higher voltages and higher frequencies. These abilities make them interesting for use in future electronic systems under conditions where Si-based devices cannot be used.

One of the WBG candidates for the replacement of Si, which is widely investigated now, is SiC. Due to its unique physical and electronic properties it shows a great promise for the future of power electronics. SiC has a huge amount of different polytypes, however, 4H-SiC is often chosen as the most suitable for the power electronics due to its wider bandgap and higher bulk mobility. Table 1 compares the most important material properties of Si and 4H-SiC.

Table 1. Material properties of 4H-SiC and Si [1]

<table>
<thead>
<tr>
<th>Material Property</th>
<th>Si</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.12</td>
<td>3.26</td>
</tr>
<tr>
<td>Electric breakdown field ($10^6$ V/cm)</td>
<td>0.3</td>
<td>2.2</td>
</tr>
<tr>
<td>Electron mobility (cm$^2$/Vs)</td>
<td>1500</td>
<td>1000</td>
</tr>
<tr>
<td>Electron saturation velocity ($10^7$ cm/s)</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Thermal conductivity (W/K-cm)</td>
<td>1.5</td>
<td>4.9</td>
</tr>
</tbody>
</table>

From Table 1 it is obvious that for power electronics 4H-SiC surpasses Si: Three times larger bandgap, nearly ten times higher electric breakdown field and more than three times higher thermal conductivity. In comparison with other WBG semiconductors with similar material properties, SiC has a significant advantage. This advantage is related to the ability to form SiO$_2$ layers on SiC by thermal oxidation in a way similar to Si, providing a good basis for the fabrication of MOS-based electronic devices. However, the opportunity to have SiO$_2$ as its native oxide can be considered nowadays not only as a great advantage but at the same time as a critical factor for the electrical applications. The high density of imperfections encountered in thermally grown oxide as well as at the SiC/SiO$_2$ interface represents a major obstacle for the performance
1.1 SiC as a wide bandgap semiconductor

of SiC MOS-devices [2]. For power MOSFETs, where one of the main requirements is a low power loss at on-state, and, thus, a low on-resistance, the quality of the SiC/SiO₂ interface is of primary importance. For example, for Vertical Diffused MOS, where the on-resistance of the drift region is low because of the high electric breakdown field of SiC, the overall performance of the device diminishes because of the high on-resistance of the channel at the interface. Thus, to use the full potential of SiC for the development of power electronics, the quality of the SiC/SiO₂ interfaces has to be improved [3].

To understand better the mechanisms which control the mobility in the channel at the interface and, thus, to improve channel mobility, lateral SiC MOSFETs are widely used for investigations. The very low channel mobility and the corresponding low channel current are the biggest issues for lateral SiC MOSFETs. Their low performance is usually related to the presence of a large number of interface defects at the SiC/SiO₂ interface. Despite that the oxide appears to be similar to that grown on silicon, the oxidation process in the presence of carbon is different and leads to a higher defect density at the interface. For clarity, the density of interface traps at the Si/SiO₂ interface in modern CMOS technology does not exceed $10^{10}$ cm⁻² eV⁻¹. In contrast, at the SiC/SiO₂ interface, this value is about ~$10^{11}$ cm⁻² eV⁻¹ in the middle of the bandgap and ~$10^{13}$ cm⁻² eV⁻¹ or even more at the band edges in 4H-SiC [4]. The question how to reduce these defects at the SiC/SiO₂ interface has become a key issue in the development of SiC MOS technology.

The standard method to reduce the interface defects by passivation with hydrogen known from Si MOS processing is not sufficient for the SiC/SiO₂ structures. This leads to the necessity to improve the processing technology and make additional material research. Currently, one of the most used methods for the improvement of SiC/SiO₂ interfaces is nitridation [5]. It has been found that the alternative method through oxidation and post-annealing in a nitrogen-containing atmosphere can reduce the interface defects by as much as a factor of ~ 2-4 [6,7]. However, the amount of traps at the SiC/SiO₂ interface still surpasses the amount of traps at the Si/SiO₂ interface resulting in a limitation of the commercial use of SiC MOS-based devices. Thus, to
understand better the nature of defects, to find technologically feasible methods to eliminate them and to improve the channel mobility of MOSFETs are the main tasks for the future research of SiC MOS technology. On the current stage of SiC research, simulation is an important instrument of the investigations. For example, simulation of processes and devices helps to understand better effects which can have an impact upon the performance of SiC devices and, thus, to find faster the solution needed to achieve a progress in the SiC device development.

### 1.2 TCAD for the development and optimization of semiconductor devices

During the last decades the software for the Technology Computed Aided Design (TCAD) has been strongly improved with the purpose to support the development and optimization of semiconductor technologies, devices and circuits. The market for TCAD tools is currently dominated by the company Synopsys [8] which offers a variety of integrated tools for IC design. Device simulation and model development is only one of its components which allows to visualize device behavior. Considering that computer resources started to be much cheaper in comparison with costs of experimental investigations, device modeling and simulation became a more and more important tool in research environments as well as in industry [9].

One of the most important advantages of using TCAD simulation and modeling is to allow deep insight and understanding of physical processes involved in the device operation. In addition, the estimation of the International Technology Roadmap for Semiconductor (ITRS) shows that the use of TCAD can help to reduce the cost and time required for the device development by up to 35-37% [10]. To illustrate the advantages of TCAD as one of the instruments of device investigation, its abilities are summarized in Fig. 1.
1.2 TCAD for the development and optimization of semiconductor devices

Fig. 1: Schematic representation of the abilities of device simulation and modeling.

As indicated in Fig. 1, one of the branches of the TCAD abilities is the simulation of hypothetical devices, i.e. devices which have not yet been manufactured. Implementation of simulations allows industry designers to predict device behavior and understand its performance benefits before its production. These simulations may not be completely predictive because there is always some disagreement between simulations and measurements. However, the simulation of hypothetical devices can provide a good initial feeling that helps in further development. The second branch of the TCAD abilities is the simulation of real devices, i.e. devices which have been already manufactured and experimentally characterized. The main purpose of such simulations is to understand and explain the behavior of the devices. The results of the simulation can be used for further development.

All the benefits mentioned above emphasize the importance of simulation as one of the investigation techniques in the field of device research and development. In addition, TCAD simulation and modeling can be considered as an important complementary tool for the successful development of process of devices.
For SiC devices TCAD simulation currently is a big challenge. Most of the models were developed for silicon, and, thus, can not adequately describe transport properties of SiC devices. To use simulation to explain the behavior of SiC devices, numerical models have to be calibrated.

1.3 Lateral 4H-SiC MOSFETs: Literature review

The commercialization of n-channel lateral SiC MOSFETs is still limited due to their low electrical performance which is related to the high amount of defects at the SiC/SiO₂ interface. According to literature, there are two main classes of defects which contribute to the distribution of the interface trap density of states \( D_{IT}(E_T) \) across the SiC bandgap [11]: A first class of defects covers the entire SiC bandgap with a density not exceeding \( 10^{12} \text{ cm}^{-2}\text{eV}^{-1} \). A second class of defects, known as near-interface traps (NITs), consists of electron traps near the SiC conduction band. The peak density of NITs reaches \( 10^{13} \text{ cm}^{-2}\text{eV}^{-1} \) and sometimes \( 10^{14} \text{ cm}^{-2}\text{eV}^{-1} \).

Furthermore, the total \( D_{IT} \) distribution in the bandgap is not uniform over energy; by spreading across the SiC bandgap it forms four broad peaks [12]. Different theoretical and experimental studies have been performed to find out the origin of these defects and understand the difference in their densities compared with the defects at the Si/SiO₂ interface.

In one of the publications of Afanas’ev [13], to explain the defect density at the SiC/SiO₂ interface, it was suggested to consider the following aspects:

- a higher surface density of atoms per unit area in SiC than in Si which may lead to a higher density of dangling bonds at the interface (e.g., on 4H-SiC (0001), the surface density is \( 1.21 \cdot 10^{15} \text{ at/cm}^2 \), on Si (100) – \( 6.8 \cdot 10^{14} \text{ at/cm}^2 \));
- a larger width of the 4H-SiC bandgap energy in comparison with Si which may allow the oxide defects located near the interface to appear in the SiC bandgap and behave like interface traps;
• the presence of the carbon which may involve additional chemical complexity of the SiC oxidation and potentially leads to a specific defect generation in SiO$_2$.

The question of the origin of defects at the SiC/SiO$_2$ interface is quit complicated and remains so far not well understood. Using photon stimulated tunneling (PST) measurements on SiC and Si-based MOS structures, traps with an energy level 2.8 eV below the conduction band of SiO$_2$ have been found in comparable densities in both oxides grown on Si and SiC [14,15]. In the 4H-SiC bandgap, these traps are positioned 0.1 eV below the conduction band, which corresponds to the energetic location of NITs. Based on that and considering the universality of the defects in SiO$_2$ layers grown on SiC and Si, it was suggested to relate NITs to oxide defects introduced during the oxidation process. From the theoretical investigations, it was also concluded that NITs originate from oxide defects near the interface. In addition, it was mentioned that one part of the NITs can be related to defects specific to SiO$_2$ on SiC formed in the oxide phase [16]. The interface traps in the lower part of the bandgap are explained mainly by carbon-related structures at the interface [4,16,17].

The presence of a large amount of traps at the SiC/SiO$_2$ interface leads to a degradation of the mobility in the channel of SiC MOSFETs. Typical values of the field-effect electron mobility in lateral 4H-SiC MOSFETs with oxides grown by dry O$_2$ oxidation are less than 10 cm$^2$/Vs. To improve such a low channel mobility, different techniques for the reduction of the density of interface traps were introduced. One of it is the use of hydrogen annealing as a precleaning stage for gate oxidation. By this technique, Ueno et al. obtained a field-effect mobility of 20 cm$^2$/Vs for MOSFETs with a p-type channel doping of 3·10$^{16}$ cm$^{-3}$ [18]. Another method, which is the most common one nowadays, is the oxidation or post-oxidation annealing in NO or N$_2$O ambients [5,19]. As an example, Fujihira et al. got a field-effect mobility of 30 cm$^2$/Vs for a MOSFETs with p-type doping of 1·10$^{16}$ cm$^{-3}$ [20]. As an alternative technique, it was shown that phosphorus passivation decreases the interface trap density even more and increases mobility by a factor of 2 in comparison to the standard nitridation [21]. By POCl$_3$ annealing Okamoto improved the channel mobility and obtained a peak field-effect mobility of 89 cm$^2$/Vs for a
channel doping concentration of \(7 \times 10^{15} \text{ cm}^{-3}\) [22]. Another oxidation method which is more efficient in the reduction of the interface traps is the sodium-enhanced oxidation [23,24]. However, this method has a big disadvantage. Due to the presence of sodium (Na) during the oxidation process, mobile Na ions in the oxide are involved and may cause threshold voltage instabilities.

As alternative method to oxidation techniques, nitrogen implantation in the channel region is widely investigated to increase the channel mobility [25,26,27]. In the work of Strenger et al. the effect of nitrogen implantation into the MOSFET channel region prior to oxidation in \(\text{N}_2\text{O}\) atmosphere was investigated [28]. For a p-doped substrate with a concentration of \(3.5 \times 10^{17} \text{ cm}^{-3}\) the peak of the field-effect mobility after \(\text{N}_2\text{O}\) oxidation was 12 cm\(^2\)/Vs. Using implantation of nitrogen with different doses for a MOSFETs with the same p-type doping concentration, an increase in the field-effect mobility was observed. For nitrogen (N) doses of \(1 \times 10^{13} \text{ cm}^{-2}\), \(3 \times 10^{13} \text{ cm}^{-2}\) and \(5 \times 10^{13} \text{ cm}^{-2}\), the peak of the field-effect mobility was equal to 17 cm\(^2\)/Vs, 21 cm\(^2\)/Vs and 25 cm\(^2\)/Vs, respectively.

As it can be seen from this short overview, many studies have been performed already to understand and solve the problem of the low channel mobility by improving the SiC/\(\text{SiO}_2\) interface. However, there are still many unknown aspects and despite the enhancements which have been already achieved, the channel mobility in 4H-SiC MOSFETs is still far from the channel mobility in Si MOSFETs [29].

### 1.4 Thesis outline

This thesis presents a study of lateral n-channel 4H-SiC MOSFETs. The fabrication and electrical characterization of all studied structures have been carried out in the framework of the French-German cooperation project MobiSiC (Mobility engineering for SiC devices). The fabrication of the devices, except MOSFETs #E1, has been done by C. Strenger at the Fraunhofer IISB, Germany. The MOSFETs #E1 have been fabricated by Robert Bosch GmbH.
The electrical characterization of all devices has been performed by E. Bedel-Pereira and V. Mortet at LAAS-CNRS, France. A description of the studied MOSFET structures, their fabrication processes and the experiments performed for their characterization are presented in Chapter 2.

The main aim of this work was to understand the mechanisms which control the channel mobility of SiC MOSFETs using TCAD simulation. For this purpose, current-voltage and Hall-effect measurements have been interpreted in this thesis by two-dimensional numerical simulations performed with Sentaurus Device of Synopsys.

To describe the electrical measurements of MOSFETs, a simulation methodology has been developed and the following physical models with proper parameters for 4H-SiC were introduced in the simulation:

- Fermi-Dirac statistics
- Bandgap energy model
- Incomplete ionization model
- Near-Interface Trap model
- Mobility degradation model

A full description of the models with the parameters used will be given in Chapter 3.

For the characterization of the interface defects, the most crucial parameter for SiC MOSFETs, their densities versus trap energies have been extracted from the electrical measurements. The methods of the extraction of the $D_{IT}(E_T)$ distributions are described in Chapter 4.

To interpret accurately channel mobilities obtained from Hall-effect measurements, the Hall factor has been evaluated, for the first time, for the channel of SiC MOSFETs. The method developed in this work for the calculation of the Hall factor is presented in Chapter 5.

The results of the simulations in comparison with the electrical measurements are shown and discussed in Chapter 6. Therein, the simulation methodology developed to interpret the electrical
characteristics of MOSFETs will be presented. In addition, the effects of temperature and bulk potential engineering upon the transport properties in the channel of SiC MOSFETs will be discussed.

In Chapter 7 the main conclusions and an outlook will be given.
Chapter 2  Simulation and Experimental Setup

2.1 Basic concept of a device simulation

Sentaurus Device of Synopsys is a device simulator that provides the ability to simulate the electrical behavior of semiconductor devices. In the current work a lateral SiC MOSFET is represented in the simulator software as a “virtual device whose physical properties are discretized onto a nonuniform mesh” [30]. A diagram with a description of the setup of device simulation is shown in Fig. 2.

Fig. 2: Diagram with the setup of device simulation.
Chapter 2 Simulation and Experimental Setup

As it can be seen in Fig. 2, the implementation of a simulation with Sentaurus Device starts with the design of the device structure. Such information as device dimensions, material of the device regions, location of electrical contacts and doping distributions have to be properly described in the simulator. To achieve accurate simulation of real MOSFETs, in addition to the description of the device structure, it is very important to define appropriate physical models in the simulation. After defining the device structure and the physical models, simulation continues with solving the equations that describe the carrier transport in the active region of the device. The equations to be solved are

the Poisson equation,

\[ \nabla \cdot (\varepsilon_S \nabla \psi) = -q(p - n + N_D^+ - N_A^-) - \rho_{\text{trap}} \]  

(1)

the electron and hole continuity equations,

\[ \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n - R_{\text{net}} \]  

(2)

\[ \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{J}_p - R_{\text{net}} \]  

(3)

and the electron and hole current density equations

\[ \vec{J}_n = q \mu_n n \mathcal{E} + q D_n \nabla n \]  

(4)

\[ \vec{J}_p = q \mu_p p \mathcal{E} - q D_p \nabla p \]  

(5)

Therein, \( \varepsilon_S \) is the dielectric constant of the semiconductor, \( \psi \) the electrostatic potential, \( q \) the elementary charge, \( n \) and \( p \) are the electron and hole concentrations, \( N_D^+ \) and \( N_A^- \) the concentrations of ionized donor and acceptor impurities, \( \rho_{\text{trap}} \) is the surface charge density which may be present due to the interface trap charges, \( J_n \) and \( J_p \) are the electron and hole current densities, \( R_{\text{net}} \) is the net recombination rate, \( \mathcal{E} \) is the electric field, \( \mu_n \) and \( \mu_p \) are the electron and
2.2 Description of the MOSFET structures and fabrication processes

hole mobilities, and $D_n$ and $D_p$ the electron and hole diffusion coefficients. The diffusion coefficients are related to the mobilities by the Einstein relations

\begin{align}
D_n &= \mu_n \frac{k_B T}{q} \\
D_p &= \mu_p \frac{k_B T}{q}
\end{align}

where $k_B$ is Boltzmann’s constant and $T$ is absolute temperature.

To obtain a numerical solution of the aforementioned equations, Sentaurus Device solves the equations on a discrete mesh using Newton’s iterative method. After a numerical solution of the equations is found, the simulated electrical characteristics can be visualized and compared with experiments. The ability to compare simulations with experiments allows to check the accuracy of the simulation results.

2.2 Description of the MOSFET structures and fabrication processes

To fabricate SiC n-channel lateral MOSFETs, several device manufacturing runs were performed. In a first run, SiC MOSFETs (#E1) were manufactured on p-type 4° off-axis (0001) Si-face 4H-SiC epitaxial layers with a thickness of 10 µm and with an aluminum (Al) concentration of $5 \cdot 10^{17}$ cm$^{-3}$. The gate oxide was grown by thermal oxidation in N$_2$O atmosphere at 1550 K for 180 min and annealed at the same temperature for 30 min in an N$_2$ ambient. The thickness of the gate oxide of the MOSFETs (#E1) is 34 nm. In a second run, SiC MOSFETs (#E2, #W1, #W2) were fabricated on p-type 4° off-axis (0001) Si-face 4H-SiC epitaxial layer with a thickness of 5 µm and with different doping concentrations of Al. The Al concentrations are $1 \cdot 10^{15}$ cm$^{-3}$, $1 \cdot 10^{16}$ cm$^{-3}$ and $5 \cdot 10^{16}$ cm$^{-3}$ for the samples #E2, #W1 and #W2, respectively. To
obtain Al concentrations of $1 \cdot 10^{16}$ cm$^{-3}$ and $5 \cdot 10^{16}$ cm$^{-3}$, box-shaped, p-type wells were fabricated by multiple Al-implantations into the epitaxial layer with a concentration of $1 \cdot 10^{15}$ cm$^{-3}$. The oxidation process was performed under the same conditions as in the first run but with a thermal oxidation time of 150 min. Due to the shorter thermal oxidation, the oxide thickness of the samples #E2, #W1, #W2 is 25.5 nm. The information about doping concentrations and gate oxide thicknesses for all investigated MOSFETs is summarized in Table 2.

### Table 2. Doping concentrations and oxide thicknesses for the investigated MOSFETs

<table>
<thead>
<tr>
<th>Sample</th>
<th>Doping concentration epitaxial layer (cm$^{-3}$)</th>
<th>Doping concentration p-type well (cm$^{-3}$)</th>
<th>Gate oxide thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#E1</td>
<td>$N_A = 5 \cdot 10^{17}$</td>
<td>–</td>
<td>34</td>
</tr>
<tr>
<td>#E2</td>
<td>$N_A = 1 \cdot 10^{15}$</td>
<td>–</td>
<td>25.5</td>
</tr>
<tr>
<td>#W1</td>
<td>$N_A = 1 \cdot 10^{15}$</td>
<td>$N_A = 1 \cdot 10^{16}$</td>
<td>25.5</td>
</tr>
<tr>
<td>#W2</td>
<td>$N_A = 1 \cdot 10^{15}$</td>
<td>$N_A = 5 \cdot 10^{16}$</td>
<td>25.5</td>
</tr>
</tbody>
</table>

To form the gate electrode in both runs, phosphorus-doped polycrystalline silicon was deposited and patterned. Source and drain regions were box implanted with nitrogen with a peak concentration of $5 \cdot 10^{19}$ cm$^{-3}$. Afterwards, they were annealed in argon (Ar) at a temperature of 1970 K for 30 min. For the fabrication of the source, drain, bulk and p-well contacts, SiC was alloyed with nickel (Ni) at 1370 K for 2 min and thereafter a metallization stack containing titanium (Ti) and platinum (Pt) was deposited and patterned. The length ($L$) and width ($W$) of the channel were 500 µm and 80 µm, respectively. It should be noted that all the investigated MOSFETs are Hall-Bar structures which are designed with additional contact taps to the channel region. A top view of the Hall-Bar structure is shown in Fig. 3. Further details of the fabrication processes can be found in the work of C. Strenger [31].
2.3 Description of electrical measurements of SiC MOSFETs

The MOSFETs studied in this work have been characterized electrically by current-voltage and Hall-effect measurements at LAAS-CNRS, France. The drain-source voltage $V_D$ in the measurements was set to 0.1 V and the gate voltage was varied from 0 V to 20 V. The Hall-effect measurements were carried out using a permanent magnet with a magnetic field of 0.33 T. Further details of the experiments and their setup can be found elsewhere [31].

From the results of the Hall-effect measurements the sheet carrier density of electrons $n_{inv}$ and the drift mobility $\mu$ in the inversion layer were determined as a function of gate voltage from the measurable quantities considering the Hall factor $r_H$ by the formulas:

$$n_{inv} = r_H \frac{I_D B}{q V_H}$$

$$\mu = \frac{1}{r_H \rho I_D B} \frac{V_H}{r_H}$$
Therein, $I_D$ denotes the channel current, $B$ the magnetic field, $V_H$ the Hall-effect voltage, and $\rho$ the channel resistivity.

The electrical characterization of the MOSFETs has been carried out in the temperature range from 50 K till 500 K. However, because of a bad convergence in the simulation at low temperatures and, considering the importance of the application of SiC MOSFETs at high temperatures, numerical simulations have been performed only from 300 K till 500 K. The results of the electrical measurements interpreted in this work will be shown and discussed together with the simulation results in Chapter 6.
Chapter 3  Physical Models

Device simulation depends significantly on the physical models and their parameters. However, most of the programs for the simulation of the device characteristics are based on models developed for silicon. Considering the difference between Si and SiC, parameter sets in the physical models need to be adjusted for simulations of SiC devices.

In addition, for SiC MOS-device simulation, where one of the most crucial physical parameters is the charge at the SiC/SiO$_2$ interface, such models as Near-Interface Trap (NIT) and Mobility degradation at the interface have to be properly included. The following sub-sections describe the models and parameters used in the current work for 4H-SiC MOSFETs simulations.

3.1 Fermi-Dirac statistics

The fundamental understanding of the semiconductor devices is based on band structure of semiconductors. In Sentaurus Device the energy band model is simplified by default and characterized by four quantities [30]:

- bandgap and electron affinity;
- effective density of states for electrons and holes.

In reality the band structure of semiconductors is very complex and consists of a large number of discrete energy states. These energy states form energy bands which are separated by gaps. However, for the current flow in semiconductors only the valence and conduction bands are important [32]. This is the reason for the simplification of the band structure used in device simulation.
The electron current in semiconductors is proportional to the free electrons in the conduction band. The presence of electrons in the conduction band physically indicates that energetic states in the conduction band are occupied by electrons. To describe the free electron concentration, the probability \( f(E) \) that an electron occupies an energy level \( E \) can be given by the Fermi-Dirac statistic

\[
f(E) = \frac{1}{1 + e^{(E - E_F)/k_B T}}
\]

where \( E_F \) is the Fermi level. The schematic representation of the Fermi-Dirac distribution is shown in Fig. 4.

As it can be seen, if the energy of state \( E \) is higher than \( E_F \), the occupation probability tends to zero. If the energy of state \( E \) is lower than \( E_F \), the occupation probability tends to 1. The probability of occupation at \( E_F \) is equal to \( \frac{1}{2} \). At temperatures which are close to 0 K, the Fermi-Dirac distribution is described by a step function, where all the energetic states below \( E_F \) are occupied, i.e. \( f(E) = 1 \), and all the energetic states above \( E_F \) are empty, i.e. \( f(E) = 0 \). With an
increase in temperature, the probability that an electron will occupy the energetic state \( E \) decreases for \( E \) below \( E_F \) and increases for \( E \) above \( E_F \).

In Sentaurus Device, if Fermi-Dirac statistics is included in the simulation, electron \((n)\) and hole \((p)\) concentrations in the conduction and valence bands are computed by [30]

\[
n = N_C F_{1/2} \frac{E_{F,n} - E_C}{k_B T} \tag{11}
\]

\[
p = N_V F_{1/2} \frac{E_V - E_{F,p}}{k_B T} \tag{12}
\]

where \( F_{1/2} \) is the Fermi integral of order \( 1/2 \), \( E_{F,n} \) and \( E_{F,p} \) are the quasi-Fermi energies for electrons and holes.

The quantities \( N_C \) and \( N_V \) in Eq. (11) and Eq. (12) are the effective densities of states in the conduction and valence bands. In this work their values have been adjusted for 4H-SiC and described in Sentaurus Device as [33]

\[
N_C \cong 3.25 \cdot 10^{15} T^{3/2} \tag{13}
\]

\[
N_V \cong 4.8 \cdot 10^{15} T^{3/2} \tag{14}
\]

\section*{3.2 Bandgap energy and its temperature dependence}

The bandgap energy \( E_G \) is the energy defined as the difference between the bottom of the conduction band \( E_C \) and the top of the valence band \( E_V \):

\[
E_G = E_C - E_V \tag{15}
\]
The value of the bandgap is strongly affected by temperature. An increase in temperature leads to a decrease of the bandgap. Considering that the bandgap variation affects also the parameters which depend on it, an appropriate model has to be included for accurate device simulation.

To describe the temperature dependence of semiconductor bandgaps, the function

\[ E_G = E_G(0) - \frac{\alpha T^2}{(T + \beta)} \]  

(16)

can be applied [30,34], where \( E_G(0) \) is the bandgap energy at 0 K, and \( \alpha \) and \( \beta \) fitting parameters. For 4H-SiC the bandgap energy \( E_G(0) \) is 3.26 eV [35], \( \alpha \) and \( \beta \) are \( 6.5 \cdot 10^{-4} \) eV/K and 1300 K, respectively [33]. The calculated temperature dependence of the 4H-SiC bandgap is shown in Fig. 5.

![Graph showing the bandgap energy of 4H-SiC as a function of temperature.](image)

Fig. 5: Bandgap energy of 4H-SiC as a function of temperature.
3.3 Incomplete ionization

In semiconductors one of the limiting factors for the maximum carrier concentration which can be obtained by doping is the ionization energies of impurities. In SiC at room temperature, because of the very high ionization energies, the impurity atoms are not fully ionized. This effect, known as incomplete ionization, affects significantly the properties of the semiconductor and has to be considered [36].

In Sentaurus Device, incomplete ionization is described by the following model [30]

\[ N_D^+ = \frac{N_D}{1 + g_D e^{(E_{F,n} - E_D)/k_B T}} \]  \hspace{1cm} (17)

\[ N_A^- = \frac{N_A}{1 + g_A e^{(E_A - E_{F,p})/k_B T}} \]  \hspace{1cm} (18)

where \( N_D^+ \) and \( N_A^- \) are the ionized donor and acceptor impurity concentrations, \( N_D \) and \( N_A \) are the total donor and acceptor concentrations, \( g_D \) and \( g_A \) are the donor and acceptor degeneracy factors. The parameters \( E_D \) and \( E_A \) are the ionization energies of the donors and acceptors, which can be described as a function of the total doping concentration \( N_{tot} = N_A + N_D \) [30,37]:

\[ E_D = E_{D,0} - \alpha_D N_{tot}^{1/3} \]  \hspace{1cm} (19)

\[ E_A = E_{A,0} - \alpha_A N_{tot}^{1/3} \]  \hspace{1cm} (20)

Therein, \( E_{D,0} \) and \( E_{A,0} \) are ionization energies for low donor and acceptor concentrations, \( N_{tot}^{-1/3} \) is an average distance between dopant atoms, \( \alpha_D \) and \( \alpha_A \) are fitting parameters. For nitrogen in 4H-SiC, \( E_{D,0} \) is equal to 105 meV and \( \alpha_D \) to 4.26·10^{-5} \, \text{meV cm} [38]. For aluminum in 4H-SiC, \( E_{A,0} \) is equal to 205 meV and \( \alpha_A \) to 1.7·10^{-5} \, \text{meV cm} [39].
In Eq. (19) and Eq. (20) it can be seen that the ionization energy of impurities decreases with an increase in the doping concentration. This can be explained by the screening of the impurity atoms by the majority charge carriers [37,40]. To demonstrate the impact of the doping dependence of the ionization energy on the concentration of the ionized impurities, the percentage of ionized Al atoms was calculated for an Al concentration of $5 \cdot 10^{17}$ cm$^{-3}$ for two cases. The first one assumes that the ionization energy is a function of doping concentration as in Eq.(20). The second one is that the ionization energy is independent of doping, meaning that $E_A = E_{A,0}$. The results of the calculation are shown in Fig. 6.

![Graph showing the percentage of ionized Al atoms](image)

**Fig. 6:** Comparison of the percentage of the ionized Al atoms calculated with and without the inclusion of doping dependence of the ionization energy.

The inclusion of doping dependence in the calculation of the ionization energy results in a lower $E_A$ in comparison to $E_{A,0}$. The lower ionization energy leads to a higher percentage of ionized atoms as shown in Fig. 6. However, this effect is not significant. As an example, the difference between the concentrations of ionized atoms calculated with a doping-dependent $E_A$ and with a constant one is 2 % at 300 K and 5% at 500 K.
Taking into account the doping dependence of the Al ionization energy, the percentage of ionized atoms was calculated as a function of temperature for SiC doped with an Al concentration of $5 \cdot 10^{16} \text{ cm}^{-3}$. The results of the calculation are compared in Fig. 7 with the results obtained previously for an $N_A$ of $5 \cdot 10^{17} \text{ cm}^{-3}$.

As it can be seen, at room temperature, the percentage of the ionized atoms decreases from 21% to 8% with $N_A$ increasing from $5 \cdot 10^{16} \text{ cm}^{-3}$ to $5 \cdot 10^{17} \text{ cm}^{-3}$. With increasing temperature, the percentage of the ionized atoms increases for both doping concentrations. The change in the concentration of ionized atoms with doping concentration and temperature is related to the change of the Fermi level. With increasing Al doping as well as with decreasing temperature, the Fermi level goes towards the valence band, thereby decreasing the probability of the impurity atoms to be ionized.

Applying the incomplete ionization model to the numerical simulations of SiC MOSFETs, it was found that the concentration of the ionized atoms depends indirectly also on the electric field of the semiconductor. For clarity, an n-channel SiC MOSFET with an $N_A$ of $5 \cdot 10^{17} \text{ cm}^{-3}$ was
simulated with an ideal interface, i.e. without any traps or fixed charges. Afterwards, the ionized doping concentration of Al was extracted from Sentaurus Device at gate voltages of 0 V and 5 V for 300 K. The result of the extraction is presented in Fig. 8.

Fig. 8: Ionized doping concentration as a function of depth at different gate voltages applied to n-channel SiC MOSFET with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$.

As it can be seen, in the region close to the interface, the aluminum atoms in the SiC are fully ionized and have a concentration of $5 \cdot 10^{17}$ cm$^{-3}$. Moving from the interface to the SiC bulk, the concentration of ionized atoms decreases and at some depth has a constant value of $4 \cdot 10^{16}$ cm$^{-3}$. The width of the region of full ionization changes with the gate voltage applied. The same effect can be observed, for example, by introducing the interface charges. For clarity, simulations of an n-channel MOSFET with $N_A$ of $5 \cdot 10^{17}$ cm$^{-3}$ have been performed with different concentrations of positive fixed charge at the interface. From the simulations the ionized doping concentration of Al was extracted as a function of depth at the gate voltage of 0 V. The results of the extraction are shown in Fig. 9 in comparison with the ideal case.
3.3 Incomplete ionization

As it can be seen, the width of the region of full ionization increases with an increase in the concentration of the positive fixed charge. In comparison with the ideal case the change in the width is insignificant if \( Q_F \) is low, \( 1 \cdot 10^{11} \text{ cm}^{-2} \). The effects of full ionization of the impurity atoms in MOSFETs with an ideal interface at gate voltages of 0 V and 5 V as well as in the MOSFETs with different concentrations of fixed charge can be explained as follows. In SiC n-channel MOSFETs with an ideal interface, due to the work-function difference between semiconductor and gate material, the energy bands bend slightly downward even at 0 V. This results in an electric field which leads to a depletion of holes at the interface. Applying a larger positive voltage, the bands bend even more downward increasing the electric field at the interface. This results in a stronger depletion of holes and an accumulation of electrons at the interface. The same effect is obtained by introducing different sheet concentrations of the positive fixed charge. The higher its concentration, the larger the electric field at the interface. Considering that the concentration of holes is related to the quasi-Fermi level as \( p \sim \exp\left(\frac{E_V - E_F}{k_B T}\right) \), the concentration of the ionized acceptors can be described in terms of the hole concentration instead of the quasi-Fermi level:

![Graph showing ionized doping concentration as a function of depth at \( V_G = 0 \text{ V} \) applied to n-channel SiC MOSFET with \( N_A = 5 \cdot 10^{17} \text{ cm}^{-3} \) and different concentrations \( Q_F \) of fixed charge.](image)
\[
N_A^- = \frac{N_A}{1 + g_A p \frac{E_A - E_V}{N_V e^{\frac{E_A - E_V}{k_BT}}}}
\]  

(21)

In Eq. (21) it can be seen that the depletion of holes leads to a full ionization of impurity atoms at the interface. The wider the depletion region, the wider the region of full ionization. This allows to conclude that in n-channel SiC MOSFETs the properties of the semiconductor near the interface are not affected by incomplete ionization. However, the effect of incomplete ionization has to be considered in the bulk.

3.4 Near-Interface Trap model

3.4.1 The fundamental knowledge of traps

The quality of the SiC/SiO\textsubscript{2} interface is a critical factor for the performance of 4H-SiC MOSFETs with a surface channel. It is mainly determined by the charges located at the interface or in the oxide. A thermally grown SiO\textsubscript{2} contains different kinds of charges. The presence of carbon during oxidation of SiC leads to a higher concentration of defects at the interface in comparison to the oxidation of Si. However, the main kinds of charges in SiO\textsubscript{2} are the same for Si and SiC. A schematic representation of the charges associated with the thermally grown SiO\textsubscript{2} on SiC is shown in Fig. 10 [41,42], where all the oxide charges are classified as:

- Mobile ion charges – positive charges within the oxide associated with the incorporation of such atoms as sodium (Na) and potassium (K) during the oxidation process [43]. Being presented in the oxide, they can diffuse to the interface during the operation of MOS-devices and produce a threshold voltage shift.
3.4 Near-Interface Trap model

- **Oxide trapped charges** – charges in the oxide which are related to oxide imperfections. These charges are usually not located at the interface, but distributed in the bulk of the oxide [42].

- **Fixed charges** – immobile charges near or at the interface. The sheet concentration of the fixed charges depends on the oxidation process, oxidation ambient and temperature [42]. This kind of charge can not exchange charge carriers with the SiC [41]. However, due to their location they play a role of scattering centers and strongly influence the threshold voltage of the MOS-devices.

- **Interface trapped charges** – charges at the interface related to the traps which have energy levels in the bandgap of the semiconductor. These traps can exchange charge carriers with the semiconductor. This means that the amount of trapped charges depends on the position of the trap levels in relation to the Fermi level.

![Diagram of Oxide and Interface Charges]

Fig. 10: Oxide and interface charges in thermally grown SiO$_2$ [41].

In addition to this classification, the interface traps can be classified into fast and slow states. The fast states are in the lower part of the SiC bandgap [17]. Slow states can be found mainly near the conduction band of 4H-SiC. They are expected to originate from oxide defects which are located close to the interface and known as near-interface traps (NITs) [4]. In comparison with the fast
states, the slow states have a more crucial impact on the performance of n-channel SiC MOSFETs and are needed to be accurately characterized.

Naturally, interface traps can be donor-like and acceptor-like states. The behavior of the traps is considered to be similar to the doping impurities [41]. The charge states of donor and acceptor traps are changed in dependence on the Fermi level as shown in Fig. 11.

![Fig. 11: Change of charge state of traps in dependence on the Fermi level.](image)

Donor traps with levels above the Fermi level are positively charged and donate electrons to the conduction band. As soon as they fall below the Fermi level, donor traps become occupied and change their charge state from positive to neutral. For acceptor traps, the dependence on the Fermi level is opposite. All the traps with levels above the Fermi level are neutral. When they fall below the Fermi level, they accept (trap) electrons and, thereby, change their charge state from neutral to negative.

To understand the impact of donor and acceptor traps on the electrical characteristics of MOSFETs, an analysis of positively and negatively charged traps has been performed with Sentaurus Device. For this purpose, firstly, current-voltage characteristics were computed using the default simulation model that assumes an ideal SiC/SiO₂ interface. To demonstrate the impact of negatively charged interface traps, acceptor traps with a concentration of $2 \cdot 10^{12} \text{ cm}^{-2}$ and a level 50 meV below the 4H-SiC conduction band were added to the ideal interface. A
3.4 Near-Interface Trap model

comparison between the current-voltage characteristics simulated assuming an ideal interface and in presence of the acceptor traps at the interface is shown in Fig. 12.

![Graph showing comparison between current-voltage characteristics](image)

Fig. 12: Impact of acceptor traps on the current-voltage characteristics of SiC MOSFETs. The acceptor traps have been simulated with a concentration of $2 \cdot 10^{12} \text{ cm}^{-2}$ and a level of 50 meV below $E_C$.

The negatively charged acceptor traps have several effects on the device performance. The first effect is a trapping of electrons from the inversion layer, excluding them from participating in the electronic transport in the transistor channel. The second effect is a shift of the threshold voltage of n-channel MOSFETs to higher values. The third effect is the scattering of electrons in the inversion layer at the negatively charged centers. The latter leads to a reduction of the mobility of the electrons in the inversion layer. All these effects contribute to the decrease of the MOSFET drain current and enlarge the threshold voltage in comparison with the ideal MOSFETs behavior without any traps.

To show the impact of positive interface charges on the current-voltage characteristics, simulations with two assumptions were performed. The first one takes into account the positive fixed charges and the second one donor traps at the interface. The fixed charges were placed at the interface with concentrations of $5 \cdot 10^{11} \text{ cm}^{-2}$ and $2 \cdot 10^{12} \text{ cm}^{-2}$. The donor traps were added with a concentration of $2 \cdot 10^{12} \text{ cm}^{-2}$ and with a level 50 meV below the 4H-SiC conduction band.
A comparison between the simulation assuming an ideal interface and simulations with positive charges at the interface are shown in Fig. 13.

Fig. 13: Impact of positive fixed charges (left) and donor traps (right) on the current-voltage characteristics of SiC MOSFET. The donor traps have been simulated with a concentration of $2 \cdot 10^{12} \text{ cm}^{-2}$ and a level of 50 meV below $E_C$.

In n-channel MOSFETs positive charges, either fixed charges or donor traps, act as scattering centers. However, in contrast to acceptor traps, their presence leads to a decrease of the threshold voltage $V_{TH}$. Despite the same effect of a decrease in $V_{TH}$, there is also a difference between the behavior of fixed charges and donor traps. As it was mentioned above, fixed charges do not depend on the Fermi level. The presence of positive fixed charges at the interface produces only a parallel shift of the threshold voltage to lower values, thereby increasing the MOSFET drain current. The higher the concentration of the positive fixed charge, the lower the threshold voltage. Donor traps being above the Fermi level also decrease the threshold voltage, providing positive charges at the interface. However, after they fall below the Fermi level, donor traps become neutral and do not affect the MOSFET drain current. Assuming the presence of only donor traps and considering that the Fermi level depends on gate voltage, this means that at some gate voltages when all donor traps are occupied, the drain current is the same as the one simulated with an ideal interface.
3.4 Near-Interface Trap model

3.4.2 Simulation of the interface trap density in n-channel SiC MOSFETs

Of all oxide charges presented in Section 3.4.1 fixed charges and interface trapped charges are usually used for simulation of lateral n-channel SiC MOSFETs. Due to their location at or near the interface they directly impact the device performance by degrading the channel mobility. For the description of the interface trap density ($D_{IT}$) as a function of the trap energy $E_T$ in simulations, an exponential distribution is usually assumed in literature [44,45]:

$$D_{IT}(E_T) = D_{IT}^{mid} + D_{IT}^{edge} e^{(E_T-E_C)/\sigma}$$ (22)

Therein, the first term on the right hand side, $D_{IT}^{mid}$, is the density of traps at midgap. The other component, $D_{IT}^{edge}$, is the density of states near the band edge. The parameter $\sigma$ is the band-tail energy which determines the sharpness of the energetic profile. Using this model for the simulation of the electrical characteristics of n-channel MOSFETs, it is commonly accepted to consider only the presence of acceptor traps in the upper half of the SiC bandgap. Examples of acceptor trap distributions modeled by the aforementioned NIT model are shown in Fig. 14.

![Diagram](image.png)

Fig. 14: Acceptor trap distributions modeled with $D_{IT}^{mid} = 2.4 \cdot 10^{11}$ cm$^{-2}$ eV$^{-1}$, $D_{IT}^{edge} = 4.6 \cdot 10^{13}$ cm$^{-2}$ eV$^{-1}$. The parameter $\sigma$ was varied as 0.047 eV, 0.067 eV, 0.087 eV.
It should be noted that the parameters in the current model have well-defined meanings. However, they are usually just fitting parameters to reproduce some characteristics of the electrical behavior of MOSFETs. To avoid inaccuracies in simulations associated with the NIT model described in Eq. (22), the interface trap density can be extracted from Hall-effect and C-V measurements. This method of extraction of the interface trap density from electrical measurements is self-consistent in the sense that it describes such properties of the interface as the trapping of the electrons in the NITs. The results of the $D_{IT}(E_T)$ extraction from C-V and Hall-effect measurements are often combined. It is known that the $D_{IT}(E_T)$ distribution from the Hall-effect method can be obtained only when the MOS device is in inversion [46]. Considering this condition, the minimum energy of the $D_{IT}$ distribution can be given as $E_C - ~ 0.1$ eV and $E_C - ~ 0.26$ eV for the MOSFETs with the background doping concentrations $N_A$ of $5\cdot10^{17}$ cm$^{-3}$ and $1\cdot10^{15}$ cm$^{-3}$, respectively. The part of the $D_{IT}(E_T)$ distribution at lower trap energies can be determined from C-V measurements. This method, as opposite to the Hall-effect one, allows to determine accurately $D_{IT}(E_T)$ closer to the center of the bandgap, but near the band-edge it gives large errors [46,47]. The limitation in the determination of the energetic position of the interface traps from the Hall-effect and capacitance-voltage measurements is the main reason for the combination of the $D_{IT}(E_T)$ distributions extracted from the aforementioned measurements.

In this work, to characterize SiC MOSFETs by numerical simulations, NIT model was developed on the basis of the $D_{IT}(E_T)$ extraction from Hall-effect and capacitance-voltage measurements with a subsequent numerical optimization of the extracted distributions. To develop the NIT model for all studied samples, #E1, #E2, #W1 and #W2, the following steps have been done:

- Extraction of $D_{IT}(E_T)$ near the conduction band from Hall-effect measurements
- Extraction of $D_{IT}(E_T)$ at lower trap energies from C-V measurements
- Introduction of the extracted energetic profiles of the interface traps as initial distributions into Sentaurus Device via a table function
- Optimization of $D_{IT}(E_T)$ by the reproduction of the current-voltage ($I_D(V_G)$) and Hall-effect measurements ($n_{inv}(V_G), \mu(V_G)$) in the numerical simulations
To extract $D_{IT}(E_T)$ from Hall-effect measurements, C++ scripts have been written based on the method described in Chapter 4. It should be noted that the scripts used in the calculations assume simplified models, for example, step function for the probability of trap occupation, neglect of potential drop along the channel from source to drain as well as of field dependence of the ionization of impurity atoms. The introduction of the initial $D_{IT}(E_T)$ distributions, calculated using C++ scripts, into Sentaurus Device, for instance, for the simulation of the drain currents led to deviations between simulations and measurements. The reason of the deviations can be explained by the usage of simplified models in the scripts for the extraction of the $D_{IT}(E_T)$ distributions. To minimize the deviations, a numerical optimization has been performed. The optimization in Sentaurus Device has been done considering that the position of the Fermi level and, as a consequence the occupation of traps, is related to the gate voltage applied. Taking this into account, the initial $D_{IT}(E_T)$ distributions, extracted from Hall-effect and C-V measurements and implemented in the simulations via table functions, have been corrected at certain gate voltages to reproduce the set of measurements, i.e. the drain currents, sheet carrier density and channel mobility as a function of gate voltage. Additionally, the $D_{IT}(E_T)$ distributions, extracted from Hall-effect measurements, have been adjusted using the newly calculated Hall factor in the channel of the studied MOSFETs described in Chapter 6. The process of the optimization of the initial $D_{IT}(E_T)$ distributions is summarized in Fig. 15.

Here it should be noted that the extraction of the $D_{IT}(E_T)$ distribution only from experimental data can be considered as a conventional method which is used in literature for the characterization of the interface traps. However, an accuracy of this method is limited by the simplified assumptions, as it was discussed above. Thus, it is expected that the method suggested in this work, which accounts also for the numerical optimization of $D_{IT}(E_T)$ by the comparison between the set of simulations and measurements, gives physically more reasonable results for the extracted $D_{IT}(E_T)$ distributions.
Fig. 15: Diagram of optimization for density of the interface traps $D_{IT}(E_T)$ extracted from Hall-effect and capacitance-voltage measurements.

The final distributions of the interface trap density found by numerical simulations with Sentaurus Device are shown in Fig. 16. All the traps, the densities of which have been extracted, were assumed to be acceptors. The results of the interface trap density extraction from Hall-effect and C-V measurements as initial distributions are shown and discussed in details in Chapter 4.
3.4 Near-Interface Trap model

Fig. 16: $D_{IT}(E_T)$ distributions used in the simulations of the studied MOSFETs.

In addition to the interface traps, to simulate the electrical characteristics of MOSFETs, fixed charges were taken into account. Their concentrations used in the simulations are presented in Table 3. Therein, it can be seen that the concentrations of fixed charges used in the simulations for the MOSFETs from the first (#E1) and second (#E2, #W1, #W2) manufacturing runs are different. Similar values have been also found in C-V measurements on MOS capacitors, fabricated under similar oxidation conditions as used for the studied MOSFETs [31]. In accordance with the C-V measurements, the concentrations of fixed charges should be equal to $6.9 \cdot 10^{11}$ cm$^{-2}$ for the MOSFET #E1 and $2.7 \cdot 10^{11}$ cm$^{-2}$ for the MOSFETs #E2, #W1 and #W2. These values are in a good agreement with the values used in Sentaurus Device and found by the best fit between simulations and measurements.

Table 3. Concentration of fixed charge used in the simulations

<table>
<thead>
<tr>
<th>Sample</th>
<th>Gate oxide thickness (nm)</th>
<th>Fixed charge (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#E1</td>
<td>34</td>
<td>$4 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#E2</td>
<td>25.5</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#W1</td>
<td>25.5</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#W2</td>
<td>25.5</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
</tbody>
</table>
3.5 Mobility degradation model

It is widely accepted that the channel mobility in lateral SiC MOSFETs can be modeled as a combination of the mobility components associated with the following scattering mechanisms:

- Coulomb scattering at ionized impurities in the bulk ($\mu_{IMP}$);
- Coulomb scattering at the interface charges ($\mu_C$);
- surface-roughness scattering ($\mu_{SR}$);
- surface-phonon scattering ($\mu_{SP}$);
- bulk-phonon scattering ($\mu_{BP}$);

Assuming the scattering mechanisms to be independent of each other, the total channel mobility can be calculated by Matthiessen’s rule as [44,48,49]

$$\mu = \left(\frac{1}{\mu_{IMP}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_{BP}}\right)^{-1} \quad (23)$$

In Eq. (23) $\mu_{IMP}$ and $\mu_{BP}$ are the mobility components which determine the total mobility in the bulk $\mu_B$. Assuming again Matthiessen’s rule $\mu_B$ can be given by

$$\mu_B = \left(\frac{1}{\mu_{IMP}} + \frac{1}{\mu_{BP}}\right)^{-1} \quad (24)$$

To simulate the temperature dependence of the electrical characteristics of the studied MOSFETs with low and high background doping concentrations, a new model for the bulk mobility $\mu_B$ was developed on the basis of the conventional one [50,51,52,53] and implemented into Sentaurus Device via “Physical Model Interface (PMI)” in the form

$$\mu_B = \mu_{\text{min}} \left(\frac{T}{300K}\right)^\alpha + \mu_{BP1} \left(\frac{T}{300K}\right)^\xi \mu_{BP2} \left(\frac{T}{300K}\right)^\chi - \mu_{\text{min}} \left(\frac{T}{300K}\right)^\alpha \frac{N_{\text{ref}}}{\left(\frac{N_{\text{ref}}}{\chi}\right)^\delta \left(N_A^\chi\right)} \quad (25)$$
3.5 Mobility degradation model

Therein, \( \mu_{\text{min}} \) is the mobility in highly doped material, where Coulomb scattering at the ionized impurities is dominant, \( \mu_{\text{BP1}} \) and \( \mu_{\text{BP2}} \) are components of the mobility in lightly doped material, where bulk-phonon scattering is the main scattering mechanism, \( N_{\text{ref}}, \alpha, \xi, \kappa, \vartheta, z \) are fitting parameters. The values of the model parameters used in the simulations are summarized in Table 4. A detailed description of the model and its calibration will be given in Section 6.4, where the temperature dependence of the electrical characteristics of SiC MOSFETs will be discussed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \mu_{\text{min}} )</td>
<td>40</td>
<td>cm(^2)/Vs</td>
</tr>
<tr>
<td>( \mu_{\text{BP1}} )</td>
<td>500</td>
<td>cm(^2)/Vs</td>
</tr>
<tr>
<td>( \mu_{\text{BP2}} )</td>
<td>450</td>
<td>cm(^2)/Vs</td>
</tr>
<tr>
<td>( N_{\text{ref}} )</td>
<td>( 2 \cdot 10^{17} )</td>
<td>cm(^{-3})</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>-0.5</td>
<td></td>
</tr>
<tr>
<td>( \xi )</td>
<td>-11.6</td>
<td></td>
</tr>
<tr>
<td>( \kappa )</td>
<td>-2.74</td>
<td></td>
</tr>
<tr>
<td>( \vartheta )</td>
<td>-12.5</td>
<td></td>
</tr>
<tr>
<td>( z )</td>
<td>0.76</td>
<td></td>
</tr>
</tbody>
</table>

In lateral n-channel 4H-SiC MOSFETs Coulomb scattering at the interface charges is the dominant scattering mechanism due to the high density of interface traps. Taking this into account, the model for the mobility component \( \mu_{\text{C}} \) is one of the most important models in the simulations of the electrical characteristics of MOSFETs. In Sentaurus Device this model is included in the form [30]

\[
\mu_{\text{C}} = \mu_1 \left( \frac{T}{300 K} \right) \left[ 1 + \left( \frac{n/(n_{\text{trans}} \left( \frac{N_c}{N_0} \right)^n)}{\left( \frac{N_c}{N_0} \right)^n} \right)^\eta \right] \right]^{\nu} \left[ \left( \frac{N_c}{N_0} \right)^n \cdot D(x) \cdot f(E_{\perp}) \right] \tag{26}
\]

where \( \mu_1 \) is a fitting parameter, \( n \) is the concentration of electrons near the interface, \( N_c \) is the interface charge density, \( x \) is a distance from the interface, \( E_{\perp} \) is the electric field perpendicular to the oxide/semiconductor interface. The functions \( D(x) \) and \( f(E_{\perp}) \) are given by [30]:
\[ D = e^{(-x/l_{\text{crit}})} \]  
\[ f(\mathcal{E}_\perp) = 1 - e^{[-(\mathcal{E}_\perp/E_0)\gamma]} \]  

In this work, it was observed that to simulate the electrical characteristics of SiC MOSFETs with different background doping concentrations the Coulomb mobility model implemented in Sentaurus Device has to be calibrated for each \( N_A \). For this purpose, the parameter \( n_{\text{trans}} \) which represents the screening of carriers in the inversion layer was taken as the calibration parameter. By fitting the simulations to the electrical measurements, values for \( n_{\text{trans}} \) were obtained for each \( N_A \) and can be found in Table 5. The rest of the parameters, i.e. \( \mu_1, N_0, \eta_1, v, \eta_2, E_0, \gamma \), and \( l_{\text{crit}} \), were used with default values of Si from Sentaurus Device [30].

Table 5. Parameter values of \( n_{\text{trans}} \) adjusted in the model for Coulomb scattering at the interface charges

<table>
<thead>
<tr>
<th>Sample</th>
<th>( n_{\text{trans}} )</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>#E1 with ( N_A = 5 \cdot 10^{17} ) cm(^{-3})</td>
<td>( 1.55 \cdot 10^{19} )</td>
<td>cm(^{-3})</td>
</tr>
<tr>
<td>#W2 with ( N_A = 5 \cdot 10^{16} ) cm(^{-3})</td>
<td>( 2.5 \cdot 10^{17} )</td>
<td>cm(^{-3})</td>
</tr>
<tr>
<td>#W1 with ( N_A = 1 \cdot 10^{16} ) cm(^{-3})</td>
<td>( 8 \cdot 10^{16} )</td>
<td>cm(^{-3})</td>
</tr>
<tr>
<td>#E2 with ( N_A = 1 \cdot 10^{15} ) cm(^{-3})</td>
<td>( 2.8 \cdot 10^{16} )</td>
<td>cm(^{-3})</td>
</tr>
</tbody>
</table>

In addition to the interface charges, the oxide/semiconductor interface is also characterized by physical roughness. Its origin is usually related to the fabrication processes of devices such as oxidation [54] and ion implantation. However, for SiC the roughness of the surface can be affected additionally by cut-off angles of substrates [55]. For instance, the studied MOSFETs have \( 4^\circ \) off-axis substrate. The usage of off-axis substrate is important for the epitaxial growth of SiC. This method of growth, known as “step-controlled epitaxy”, was developed for SiC to avoid inclusion of different polytypes and obtain high-quality epitaxial layers [56,57].

In lateral MOSFETs the roughness of the interface results in the scattering of the electrons which leads to a degradation of the channel mobility. In Sentaurus Device the mobility component associated with surface-roughness scattering is modeled in the form [30]
\[ \mu_{SR} = \left( \frac{(\mathcal{E}_/ / \mathcal{E}_{ref})^2}{\delta} + \frac{e^3}{\eta} \right)^{-1} \frac{1}{D} \]  

(29)

where \( \mathcal{E}_{ref} \) is the reference field equal to 1 V/cm, \( \delta \) and \( \eta \) are fit parameters which depend on the roughness of the SiC/SiO\(_2\) interface and account for such interface characteristics as correlation length and average step height [58,48]. From Eq. (29) it can be seen that the higher the values of \( \delta \) and \( \eta \), the higher the mobility \( \mu_{SR} \) which indicates a lower roughness of the surface.

Considering the dependence of \( \mu_{SR} \) on the electric field, the contribution of surface-roughness scattering to the channel mobility is stronger at higher gate voltages. Taking this into account, \( \delta \) and \( \eta \) were modified in the current work from the Si default values by bringing the simulated and experimental current-voltage characteristics at higher gate voltages into agreement. The values of \( \delta \) and \( \eta \) used in the simulations are shown in Table 6. Therein, it can be seen that the fitting parameters for the MOSFETs from the first (#E1) and second (#E2, #W1, #W2) manufacturing runs differ almost by a factor of 10. The simulation results reveal that the interface is rougher for the MOSFET #E1 which has a thicker oxide and a thicker epitaxial layer. This result is in agreement with the works [54,59,60] in which it was shown that surface roughness increases with an increase in the oxide thickness as well as with an increase in the thickness of the epitaxial layer.

Table 6. Parameter values for the surface-roughness mobility component (\( \mu_{SR} \))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value for #E1 with ( T_{ox} = 34 ) nm</th>
<th>Value for #E2, #W1, #W2 with ( T_{ox} = 25.5 ) nm</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \delta )</td>
<td>( 1.7\times10^{13} )</td>
<td>( 1.6\times10^{14} )</td>
<td>( \text{cm}^2/(\text{V} \cdot \text{s}) )</td>
</tr>
<tr>
<td>( \eta )</td>
<td>( 1.7\times10^{29} )</td>
<td>( 1.6\times10^{30} )</td>
<td>( \text{V}^2/(\text{cm} \cdot \text{s}) )</td>
</tr>
</tbody>
</table>

In addition to the scattering mechanisms discussed above, the contribution attributed to surface-phonon scattering is modeled in Sentaurus Device by [30]
\[ \mu_{SP} = \left( \frac{B}{\varepsilon_\perp} + \frac{C(N_A^-)^{\alpha_1}}{\varepsilon_\perp^{1/3}T} \right) \frac{1}{D} \] \tag{30}

where \( B, C \) and \( \alpha_1 \) are fitting parameters. In literature it is usually assumed that the contribution of surface-phonon scattering to the channel mobility of 4H-SiC MOSFETs is insignificant at room temperature \([61]\). One of the reasons of its low contribution is the strong Coulomb scattering at the interface charges. However, at high temperatures because of the increase in the amount of phonons and decrease in Coulomb scattering at the interface, surface-phonon scattering becomes more and more important.

The model parameters for the mobility components associated with surface-phonon scattering were taken for 4H-SiC from the literature and listed in Table 7 \([49]\).

**Table 7. Parameter values for the surface-phonon mobility component (\( \mu_{SP} \))**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( B )</td>
<td>( 1 \cdot 10^9 )</td>
<td>( \text{cm/s} )</td>
</tr>
<tr>
<td>( C )</td>
<td>( 3.23 \cdot 10^9 )</td>
<td>( \text{K cm/s (V/cm)}^{2/3} )</td>
</tr>
<tr>
<td>( \alpha_1 )</td>
<td>( 0.0284 )</td>
<td>1</td>
</tr>
</tbody>
</table>
Chapter 4 Extraction of the Density of Interface Traps from Electrical Measurements

The occupation of the interface traps and, as a consequence the interface trapped charge \( Q_{IT} \), is determined by the position of the Fermi level in relation to the energy levels of traps. In MOS devices the Fermi level can be controlled by the gate voltage applied. This means, when the gate voltage changes, the interface trapped charge also changes. Considering that energy levels of interface traps are distributed across the bandgap, their density \( D_{IT} \) is defined as number of charges per unit area and unit energy difference in the bandgap [41]

\[
D_{IT} = \frac{1}{q} \frac{dQ_{IT}}{dE}
\]  

(31)

The change of the interface trapped charge with gate voltage is the basis for the \( D_{IT} \) determination from experimental methods such as Hall-effect and capacitance-voltage measurements.

4.1 Hall-effect measurements

From semiconductor theory it is known that the gate voltage applied to MOSFETs with an ideal interface, i.e. no interface charges, is balanced by a space charge induced by the electric field. Assuming a source-drain voltage \( V_D \) equal to 0 V the charge balance for n-channel MOSFETs with ideal interface can be expressed by [41]
\[ V_{G,\text{ideal}} = \phi_{MS} + \psi_S + \frac{Q_S(\psi_S)}{C_{ox}} \]  

(32)

where \( \phi_{MS} \) is the semiconductor-gate material work function, \( \psi_S \) is the band-bending at the interface and \( Q_S \) is the space charge.

For p-type semiconductor \( \phi_{MS} \) is determined as

\[ \phi_{MS} = \phi_M - (\chi + \frac{E_G}{2q} + \psi_B) \]  

(33)

where \( \phi_M \) is the work function of gate material, \( \chi \) is the electron affinity and \( \psi_B \) is the bulk potential, defined by

\[ \psi_B = \frac{k_B T}{q} \ln\left(\frac{N_A^-}{n_i}\right) \]  

(34)

with the intrinsic carrier concentration \( n_i \)

\[ n_i = \sqrt{N_C N_V e^{-E_G/2k_B T}} \]  

(35)

The space charge \( Q_S \) depends on the band-bending \( \psi_S \) and can be calculated for a uniformly doped semiconductor by [41]

\[ Q_S = \frac{\sqrt{2 \varepsilon_S k_B T}}{qL_D} F(\beta \psi_S, \frac{n_{p0}}{p_{p0}}) \]  

(36)

where \( L_D \) is the Debye length, \( n_{p0} \) and \( p_{p0} \) are the densities of electrons and holes which are given by

\[ p_{p0} \approx N_A^- \]  

(37)
4.1 Hall-effect measurements

\[ n_{p0} \approx \frac{n_t^2}{N_A} \]  \hspace{1cm} (38)

The Debye length and the function \( F(\beta \psi_S, \frac{n_{p0}}{p_{p0}}) \) are given by [41]

\[ L_D \equiv \frac{k_B T \varepsilon_S}{p_{p0} q^2} \]  \hspace{1cm} (39)

\[ F \left( \beta \psi_S, \frac{n_{p0}}{p_{p0}} \right) \equiv \sqrt{\left[ (e^{-\beta \psi_S} + \beta \psi_S - 1) + \frac{n_{p0}}{p_{p0}} (e^{\beta \psi_S} - \beta \psi_S - 1) \right]} \]  \hspace{1cm} (40)

In reality, the oxide/semiconductor interface is characterized by different types of charges. Their presence changes the charge balance of the MOSFET in comparison with the ideal one for a given gate voltage. Considering the influence of the positive fixed charge \( Q_F \) and the interface trapped charges, where the contributions from acceptor \( (Q_{IT}^A) \) and donor \( (Q_{IT}^D) \) traps are accounted for, Eq.(32) has to be rewritten in the form

\[ V_{G, real} = \phi_{MS} + \psi_S + \frac{Q_S(\psi_S)}{C_{ox}} + \frac{Q_{IT}^A(\psi_S)}{C_{ox}} - \frac{Q_{IT}^D(\psi_S)}{C_{ox}} - \frac{Q_F}{C_{ox}} \]  \hspace{1cm} (41)

Comparing Eq.(32) and Eq.(41), it can be seen that the charges at the interface result in a difference between the real gate voltage and the ideal one for the same value of \( \psi_S \). Taking into account this difference, the density of interface traps can be extracted. A key issue in the extraction of the \( D_{IT}(E_T) \) distribution is the determination of the real relation between \( \psi_S \) and \( V_G \) which depends on \( Q_{IT} \) and \( Q_F \). The usage of Hall-effect measurements allows to determine \( \psi_S(V_G) \) directly from the measured sheet carrier density independently of \( Q_{IT} \) and \( Q_F \). This is the main advantage of this method of \( D_{IT} \) extraction. When the real and ideal \( \psi_S(V_G) \) curves are determined, the interface trap distribution can be calculated by the difference in the change of the real and ideal gate voltages required for a small change in \( \Delta \psi_S \) using Eq. (42) [46]
where \( C_{\text{ox}} \) represents oxide capacitance and \( E_T \) the trap energy which is related to the Fermi level \( E_F \) and described as

\[
E_T - E_V = \psi_S + \frac{E_G}{2} - \psi_B
\]  

(43)

For clarity, the method is graphically illustrated in Fig. 17. The steps which have to be done to calculate \( D_{IT}(E_T) \) from Hall-effect measurements are summarized below the figure.

- The ideal dependence of \( \psi_S(V_G) \) has to be calculated assuming no charges at the interface and using Eq. (32).
- The real dependence of \( \psi_S(V_G) \) has to be calculated from \( n_{\text{inv}}(V_G) \) obtained from Hall-effect measurements.
4.1 Hall-effect measurements

- Assuming a small change in $\Delta \psi_S$ for the ideal and real $\psi_S(V_G)$ curves, the required change in the gate voltage $\Delta V_{G,real}$ and $\Delta V_{G,ideal}$ for $\Delta \psi_S$ has to be calculated.
- The density of interface traps can be determined using Eq. (42).

In this work, the real $\psi_S(V_G)$ curve was computed from

$$ n_{inv}(V_G) = \frac{q n_p L_D}{\sqrt{2k_B T}} \int_0^{\psi_S} \frac{e^{\beta \psi} - 1}{F(\beta \psi, \frac{n_p}{p_p})} d\psi $$

(44)

using the sheet carrier density derived from the Hall-effect measurements [41].

The results of the $D_{IT}(E_T)$ extraction are shown in Fig. 18 for all the studied MOSFETs. In terms of nature of traps, all the traps, the densities of which have been extracted, were assumed to be acceptors. Considering that both donor and acceptor states trap electrons from the inversion layer, their nature can not be distinguished from the Hall-effect measurements.

![Fig. 18: Interface trap density extracted from Hall-effect measurements. The Hall factor $r_H$ was assumed to be unity in the calculation.](image)

- #E2 with $N_A = 1 \cdot 10^{15}$ cm$^{-3}$
- #W1 with $N_A = 1 \cdot 10^{16}$ cm$^{-3}$
- #W2 with $N_A = 5 \cdot 10^{16}$ cm$^{-3}$
- #W1 with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$
- $r_H = 1$
Here it should be noted that the method of $D_{IT}(E_T)$ extraction from Hall-effect measurements is very sensitive but its accuracy depends on several effects. The first one is the dependence of the sheet carrier density obtained from Hall-effect measurements on the Hall factor. The result of $D_{IT}(E_T)$ in Fig. 18 was obtained from $n_{inv}$ derived with the assumption of a Hall factor $r_H$ being equal to 1. However, as it will be discussed in Chapter 6, $r_H$ differs in the channel of SiC MOSFETs from 1 and varies depending on the dominant scattering mechanisms. Considering Eq. (8), it is obvious that different values of the Hall factor will result in different distributions of the interface trap density. To see the influence of the Hall factor, the $D_{IT}(E_T)$ distribution for the MOSFET #E1 was recalculated using two constant values of $r_H$ being equal to 1.25 and 1.5. The results of the calculation are shown in Fig. 19 in comparison with the result obtained previously assuming $r_H = 1$.

![Diagram](image.png)

Fig. 19: Influence of Hall factor on the energetic profile of interface trap density extracted from the Hall-effect measurements.

It can be seen that higher values of the Hall factor lead to lower interface trap densities. In this way, it is obvious that the uncertainties in the value of the Hall factor introduce inaccuracies in the method of $D_{IT}(E_T)$ extraction from Hall-effect measurements. In this work, the Hall factor has been calculated in the channel of all studied MOSFETs using the method described in
Chapter 5. Taking the results of the Hall factor obtained, the $D_{IT}(E_T)$ distributions have been self-consistently determined. The final $D_{IT}(E_T)$ distributions, used in the simulations, which take into account the newly calculated Hall factor have been shown in Fig. 16.

The second effect which may lead to an inaccuracy of the $D_{IT}(E_T)$ extraction from Hall-effect measurements is the accuracy of the determination of $\psi_S(V_G)$. An example can be given on the basis of the analytical calculation of $\psi_S(V_G)$. It is known that in MOSFETs the band-bending $\psi_S$ depends not only on the applied gate voltage but also on the applied drain-source voltage $V_D$, and hence on the potential drop along the channel from source to drain. However, the analytical solution of the equations for the determination of $\psi_S(V_G)$ does not take this effect into account. This will introduce an inaccuracy in the calculation of $\psi_S(V_G)$ of MOSFETs and, thereby, the inaccuracy in the determination of the energy trap position. More accurately the relation between $\psi_S$ and $V_G$ can be obtained using numerical TCAD simulations where the aforementioned effect is automatically considered.

Furthermore, the extraction of $D_{IT}$ from the measurements, Hall-effect as well as C-V, is based on a simplified model for the trap occupation probability. There, the occupation probability of a trap takes a value of 0 when it above the Fermi level and 1 when it below the Fermi level. In reality, the probability of the trap occupancy obeys the Fermi-Dirac statistic, discussed in Chapter 3. This can result in the redistribution of the calculated $D_{IT}$ over trap energy in comparison with the measured one.

### 4.2 Capacitance-voltage measurements: High-low frequency method

Capacitance-voltage (C-V) measurement is one of the methods to characterize an oxide/semiconductor interface. In contrast to the Hall-effect measurements discussed above, this method is applied to a MOS capacitor and based on measuring its total capacitance $C$ defined as a change of its total charge per voltage
Chapter 4 Extraction of the Density of Interface Traps from Electrical Measurements

\[ C \equiv \frac{\Delta Q}{\Delta V} \]  

To perform C-V measurements, AC and DC voltages have to be applied simultaneously. The DC voltage sweeps in time and controls the position of the Fermi level. The AC voltage with a fixed amplitude and frequency provides the small signal bias and allows to measure the capacitance of the device at a given \( E_F \).

To understand better C-V measurements, a MOS capacitor is usually represented by a capacitance equivalent circuit. The capacitance circuit of MOS structure which takes into account traps at the interface is shown in Fig. 20.

![Capacitor circuit of MOS capacitor with the interface traps](image)

Fig. 20: Capacitor circuit of MOS capacitor with the interface traps. The figure is adjusted from [62].

It can be seen that the capacitance circuit, in which the effect of the interface traps is included, is composed of capacitance \( C_{IT} \) and resistance \( R_{IT} \) associated with the interface traps, gate oxide capacitance \( C_{ox} \) and capacitance of the depletion region \( C_D \). The product of \( C_{IT} R_{IT} \) gives a lifetime \( t \) of the interface traps, which determines the behavior of traps at different frequencies [41]. The frequency behavior of traps is the basis of the high-low frequency method, where the total capacitance of the MOS structure is measured as a function of gate voltage at low \( (\omega_{LF}) \) and high \( (\omega_{HF}) \) frequencies.
During low-frequency measurements the interface traps can follow the AC signal and, thereby, modify the total capacitance of the MOS structure by changing $Q_{IT}$ with increasing gate voltage. In this way, the total capacitance of the MOS structure $C_{LF}$ at low frequency can be expressed by [63,64]

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{IT} + C_D}$$  \hfill (46)

At high frequency the interface traps can not adjust their charge state fast enough to keep pace with the applied AC signal [41,63]. The capacitance $C_{IT}$ associated with the interface traps can than be ignored. Thus, the MOS capacitance $C_{HF}$ at high frequency $\omega_{HF}$ can be correlated to the capacitance of the ideal MOS structure, i. e. structure without interface traps, and presented as a serial connection of the oxide and depletion region capacitances [65]

$$C_{HF} = \frac{C_{ox}C_D}{C_{ox} + C_D}$$  \hfill (47)

For clarity, the equivalent capacitance circuits at low and high frequencies are shown in Fig. 21.

![Capacitance circuits at low (left) and high (right) frequencies. The figure is adjusted from [62].](image)

Fig. 21: Capacitance circuits at low (left) and high (right) frequencies. The figure is adjusted from [62].
Chapter 4 Extraction of the Density of Interface Traps from Electrical Measurements

Due to the inability of the interface traps to respond to the small signal at high frequencies, the interface trap density can be determined from the low and high-frequency capacitances [47].

Considering that the interface trap density associated with $C_{IT}$ can be calculated by

$$D_{IT} = \frac{C_{IT}}{q^2},$$  \hspace{1cm} (48)

from C-V measurements at low frequency $D_{IT}$ can be expressed as [64]

$$D_{IT} = \frac{1}{q^2} \left( \frac{C_{ox} C_{LF}}{C_{ox} - C_{LF}} - C_D \right)^{-1}$$ \hspace{1cm} (49)

Extracting the capacitance associated with the depletion region $C_D$ from C-V measurements at high frequency, the interface trap density can be obtained [64]

$$D_{IT}(V_G) = \frac{C_{ox}}{q^2} \left( \frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}} \right)$$ \hspace{1cm} (50)

To correlate $D_{IT}$ with the position of the Fermi level in the bandgap, the band-bending as a function of the gate voltage was determined. The calculation of the band-bending-gate-voltage relation was done using the Berglund integral [64]

$$\psi_S = \psi_{S0} + \int_{V_{G0}}^{V_G} \left( 1 - \frac{C_{LF}(V_G)}{C_{ox}} \right) dV_G$$ \hspace{1cm} (51)

where $\psi_{S0}$ corresponds to the band-bending at the gate voltage $V_{G0}$ and can be obtained from comparison with an ideal C-V curve for conditions where the interface traps are negligible in comparison to the charge in the channel.

The results of the $D_{IT}(E_T)$ distribution extracted by the high-low frequency method, performed on a p-MOS capacitor with $N_D = 8 \cdot 10^{15}$ cm$^{-3}$ and an oxide thickness of 27.1 nm, is shown in Fig. 22. The oxidation process of the capacitor has been done under similar conditions as for the
MOSFETs from the second manufacturing run. The measurements of the capacitance-voltage characteristics and the extraction of the interface trap density have been done by C. Strenger in the framework of the MobiSiC project. The details of the measurements can be found in the work [31].

Taking into account that interface traps are mostly related to the oxidation process, the interface trap density extracted from C-V measurements of MOS capacitors is often assumed to be characteristic also for MOSFETs. This method of the characterization has one big disadvantage. In n-channel MOSFETs the traps near the conduction band are of primary interest. To characterize electron traps near the conduction band edge from C-V measurements, a p-MOS capacitor with n-doped substrate is required. Nevertheless, n-channel MOSFETs are fabricated on p-doped substrate. The interface traps on n- and p-doped structures are not necessarily the same, even under identical fabrication processes [46]. However, it was shown by Saks that the comparison of the $D_{IT}(E_T)$ distributions from C-V and Hall-effect measurements at low doping concentrations, $N_D$ and $N_A \sim 1 \cdot 10^{16}$ cm$^{-3}$, shows a very good agreement between both methods meaning that they could be used in combination for the characterization of the SiC/SiO$_2$ interface traps [46].
The results of the extraction of the interface trap density from the two methods have been compared also in the current work. It should be noted that the interface trap density extracted from C-V measurements for the characterization of MOSFETs is often assumed to be insensitive to the doping concentration of the MOS capacitor. This can be mostly explained by the fact that, for example, p-MOS capacitor and n-channel MOSFET have different types of substrate doping. In the MobiSiC project the extraction of the interface trap density from C-V measurements has been also performed with the assumption that the $D_{IT}(E_T)$ distribution does not depend on $N_D$ and, thus, the interface trap density was obtained on a p-MOS capacitor only with $N_D$ of $8 \cdot 10^{15}$ cm$^{-3}$. However, the introduction of the extracted $D_{IT}(E_T)$ into simulation for the characterization of the MOSFETs with different $N_A$ showed the necessity to shift the $D_{IT}(E_T)$ distribution obtained from C-V characteristics. The required shift as well as its possible origin will be shown and discussed in Section 6.3, where the effect of the bulk potential will be discussed. Here, just for the comparison of the two methods of extraction, the $D_{IT}(E_T)$ distribution obtained by the high-low frequency method has been compared with the interface trap densities extracted from the Hall-effect measurements performed for the MOSFETs with $N_A$ of $1 \cdot 10^{15}$ cm$^{-3}$ and $5 \cdot 10^{17}$ cm$^{-3}$. A comparison is shown in Fig. 23. For simplicity, the Hall factor was assumed to be equal to 1.

![Fig. 23: Interface trap density extracted from C-V and Hall-effect measurements.](image)
At first sight it can be seen from the comparison that the interface trap density measured on an n-doped MOS capacitor fits well to the $D_{IT}$ extracted from Hall-effect measurements performed for MOSFETs with different Al concentrations. However, between the $D_{IT}$ distributions extracted from C-V and Hall-effect measurements there is an uncovered part of the energetic distribution of traps. The existence of this part can be explained by the limitations of the methods in the determination of the energetic position of the traps, discussed in Section 3.4.2. This part in the $D_{IT}(E_T)$ distribution can be replaced, for example, using a linear interpolation. Nevertheless, considering the non-uniform $D_{IT}$ distributions over the SiC bandgap, the existence of small peaks instead of a linear distribution can not be excluded.
Chapter 5  Method of Hall Factor Calculation

Hall-effect measurements in combination with sheet resistivity measurements are well established to determine sheet carrier density and mobility of charge carriers independently in semiconductors and metals. However, from the combination of the measured values one obtains an effective Hall mobility \( \mu_H \) rather than the drift mobility \( \mu \) of the majority charge carriers. The ratio of the two is called Hall factor or scattering factor and needs to be known a-priori for an accurate interpretation of Hall-effect measurements. For lower fields and non-degenerate semiconductors, the Hall factor depends on the particular mechanisms by which the charge carriers are scattered and this may depend in turn on material and measurement condition. For bulk SiC, \( r_H \) was determined experimentally and investigated theoretically \([66,67,68]\). For the significantly more complicated situation in the channel of SiC MOSFETs, it is common practice to assume a Hall factor equal to unity \([52]\). From the theory of Hall-effect measurements it is known that \( r_H \) approaches unity in strong magnetic fields \( B \) for which the condition \( \mu B \gg 1 \) is satisfied. For a magnetic field of \( B = 1 \) T, as an example, this means that the mobility should be significantly higher than 10,000 cm\(^2\)/Vs. In SiC MOSFETs, the drift mobility in the channel is typically on the order of 10 to 100 cm\(^2\)/Vs \([45,52]\). As a consequence, the assumption of \( r_H = 1 \) may lead to a misinterpretation of Hall-effect measurements by up to some 10% which is considerable for such devices.

In literature, various approaches have been presented to calculate transport properties and Hall factors. They are typically based on Monte Carlo methods or solutions of the Boltzmann transport equation taking the full band structure into account \([67,69]\). Despite being computationally demanding, they still need comparison with experiments and cannot be easily
applied to general conditions in macroscopic devices. In this work, a new method for the calculation of Hall factors is presented. It is based on the fact that both Hall factor and mobility depend on the mechanisms by which the charge carriers are actually scattered [VU1]. The links between the various mobility components and the Hall factor are the respective relaxation scattering times. A particular advantage of the method is that it can be easily applied for different materials under different measurement conditions.

5.1 On the calculation of Hall factor for the characterization of electronic devices

The Hall factor $r_{H0}$ is defined as the ratio of the Hall mobility to drift mobility and can be expressed in the relaxation scattering time approximation through certain mean values of relaxation times:

$$r_{H0} = \frac{\mu_H}{\mu} = \frac{<\tau^2>}{<\tau>^2}$$

Therein, the parameter $\tau$ denotes the relaxation time, i.e. the mean free flight time between carrier collisions. In general, it will depend on the energy of the charge carriers. The squared brackets denote an averaging over the energy of the charge carriers. The inverse of the relaxation time $1/\tau$ is the average number of scattering events per unit time. For many scattering processes, the energy dependence of the relaxation time can be expressed as a simple power law:

$$\tau = aE^{-s}$$

where $a$ and $s$ are constants whose values depend on the involved types of scattering mechanisms. For example, for semiconductors with acoustic phonon or ionized impurity scattering, $\tau$ is proportional to $E^{-1/2}$ ($s = 1/2$) or to $E^{-3/2}$ ($s = -3/2$), respectively [41].

As long as the relaxation time can be expressed in the form of a power law, the values of the averages $<\tau>$ and $<\tau^2>$ can be calculated analytically:
5.1 On the calculation of Hall factor for the characterization of electronic devices

\[ < \tau > = \frac{a(kT)^{-s} \Gamma\left(\frac{5}{2} - s\right)}{\Gamma\left(\frac{5}{2}\right)}, \]  

(54)

\[ < \tau^2 > = \frac{a^2(kT)^{-2s} \Gamma\left(\frac{5}{2} - 2s\right)}{\Gamma\left(\frac{5}{2}\right)} \]  

(55)

where \( \Gamma(n) \) is the gamma function defined as:

\[ \Gamma(n) \equiv \int_0^{\infty} x^{n-1} e^{-x} \, dx \]  

(56)

In accordance with Eq. (52), it follows from the expressions above that the Hall factor becomes \( r_{H0} = 1.18 \) for surface-phonon scattering and \( r_{H0} = 1.93 \) for ionized impurity scattering. It was also suggested by Erginsoy that the relaxation time for scattering at neutral impurities is independent of the energy of the charge carriers \( (s = 0) \) [70]. For such a mechanism dominating at extremely low temperature or for heavily doped semiconductors, the Hall factor becomes \( r_{H0} = 1 \). In summary, depending on the actual scattering mechanism, values of the Hall factor \( r_{H0} \) may vary between 1 and 1.93.

In a real electronic device, several charge scattering mechanisms are usually involved in parallel. In order to calculate the Hall factor from Eq. (52), the values of \( <\tau> \) and \( <\tau^2> \) have to be determined for such conditions. This can be done by accounting these several scattering mechanisms when averaging relaxation times over energy. As suggested by Iwata [68], the various scattering mechanisms can be combined in the form:

\[ <\tau> = \frac{\int_0^{\infty} x^{3/2} e^{-x} \, dx}{\int_0^{\infty} x^{3/2} e^{-x} \, dx} \]  

(57)
\[<\tau^2> = \frac{\int_0^\infty x^{3/2} e^{-x} \, dx}{\int_0^\infty x^{3/2} e^{-x} \, dx} \]

where \(x\) stands for \(\varepsilon/k_BT\) with \(\varepsilon\) denoting the kinetic energy of an electron and the index \(i\) the particular scattering mechanism.

To apply Eq. (57) and Eq. (58) to certain experimental conditions, the relaxation times for each of the scattering mechanisms and their dependence on the energy of the charge carriers under investigation have to be known. For example, for measurements in a MOS structure, only scattering of the prevalent charge carriers in the inversion layers should be considered. A peculiarity of Hall-effect measurements in MOSFETs is scattering at interface charges which is largely negligible for measurements on bulk semiconductor samples. This difference in the measurement conditions can manifest itself in different Hall-factor values. The new method for the calculation of Hall factors presented in this work allows master the complexity of the necessary calculations. As indicated above, it takes advantage of the interdependence of the scattering time with mobility. In general, the electron mobility in a semiconductor can be expressed as:

\[\mu_n = \frac{q <\tau>}{m_e^*} \]

where \(<\tau>\) is the mean relaxation time that may contain the contributions from several scattering processes, and \(m_e^*\) stands for the effective electron mass. It is further assumed that the scattering events are independent of each other so that neither of the \(\tau_i\) is affected by other scattering process. The contributions of the individual scattering times \(\tau_i\) to the global scattering time \(\tau\) can then be combined in the form:

\[\frac{1}{\tau} = \sum_i \frac{1}{\tau_i} \]
5.1 On the calculation of Hall factor for the characterization of electronic devices

Since the electron mobility is proportional to $\tau$, Eq.(60) can be rewritten in terms of the mobility components $\mu_i$ associated with the various scattering mechanisms

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu_i}.$$  \hspace{1cm} (61)

From Eq. (59) it is seen that the relaxation time and electron mobility differ only by a constant factor of $q/m_e^*$. Having the possibility to calculate specific mobility components $\mu_i$, the components of scattering time $\tau_i$ associated with these mechanisms can be easily found. If a power-law dependence of the relaxation time on the electron energy can be assumed, the unknown constant $a$ in Eq. (53) can be calculated from Eq. (54) and Eq. (59). Given $a$, the energy dependence of the relaxation time for $i$th scattering component can be derived as:

$$\tau_i(E) = \frac{\mu_i m_e^* \Gamma \left(\frac{5}{2}\right) E^{-s_i}}{q(k_B T)^{-s_i} \Gamma \left(\frac{5}{2} - s_i\right)}$$  \hspace{1cm} (62)

It should be noted that these formulas are valid for non-degenerate semiconductors with a single-valley spherical energy band. For multi-valley semiconductors, such as Si, SiC and Ge, the expression for the Hall factor has to be modified. For this purpose, the Hall factor given by Eq. (52) for the single-valley model is multiplied by a constant $a_0$ that accounts for the anisotropy of the effective electron mass. Thus, the Hall factor for the case of a multiple conduction valley semiconductor can be expressed in the form [71]

$$r_H = r_{H0} a_0$$  \hspace{1cm} (63)

where $r_{H0}$ is the scattering factor given by Eq.(52) for single-valley semiconductors assuming isotropic model, and $a_0$ is known as the “Hall mass factor” or anisotropy factor of the Hall-effect. The latter is given by [71]
with $K$ being the ratio of longitudinal and transverse effective masses of the electrons. For Si, SiC and Ge, the Hall mass factor $a_0$ takes values of 0.87, 0.98 and 0.785, respectively.

Using Eqs. (57-62), and assuming the concurrent action of different scattering mechanisms, the Hall factor can be easily determined and corrected with the anisotropy model given in Eq.(63).

### 5.2 Hall factor in bulk silicon

To check the feasibility of the new method for the calculation of Hall factors, it was applied to the calculation of the Hall factor in bulk silicon, the values of which was extensively investigated in the literature. Specifically, the dependence of the Hall factor in n-type silicon at room temperature on the doping concentration was investigated. For this purpose, simulations of electronic transport in phosphorus-doped silicon samples were performed for the range of phosphorus concentration from $1 \cdot 10^{17}$ cm$^{-3}$ to $2 \cdot 10^{20}$ cm$^{-3}$. Given bulk silicon, it was assumed that the mobility is determined by Coulomb scattering at ionized impurities and by bulk-phonon scattering. To model the mobility component due to bulk-phonon scattering, a constant mobility of $\mu_{BP} = 1417$ cm$^2$/Vs at $T = 300$ K was adopted from the work of Lombardi et al. [72]. The mobility component due to charged impurity scattering was calculated using the Arora model as implemented in TCAD Sentaurus and is described by [30]

$$\mu_B = \mu_{min1} + \frac{\mu_d}{1 + \left(\frac{N_D^+}{N_0}\right)^{A^*}}$$

(65)

with $N_D^+$ standing for the ionized donor concentration and $\mu_{min1}$, $\mu_d$, $N_0$ and $A^* > 0$ for some given parameters of the model. To predict the dependence of the Hall factor on the dopant concentration, an analysis of Eq. (65) was done. It is clear from the functional dependence that
the doping-related component will strictly decrease with an increasing doping concentration. This is shown also in Fig. 24. It can be interpreted as an increase of the number of scattering centers in the bulk with an increasing dopant concentration, leading further to a monotonic increase of Coulomb scattering.

![Bulk mobility in Si, calculated by the Arora model](image)

**Fig. 24:** Bulk mobility as a function of phosphorus concentration [VU1].

Keeping in mind that the Hall factor is \( r_{H0} = 1.18 \) for the limiting case of exclusive phonon scattering and \( r_{H0} = 1.93 \) for the exclusive case of ionized impurity scattering, one expects also an increase of the Hall factor with doping concentration. On the other hand, several groups found experimentally that the Hall factor in n-type silicon increases with donor concentrations but only until a doping level of about \( 3 \cdot 10^{18} \) cm\(^{-3} \) [73,74,75,76]. With a further increase of doping concentration, the Hall factor decreases and, for doping concentrations exceeding \( 10^{20} \) cm\(^{-3} \), the Hall factor approaches the theoretical value of \( r_H = 0.87 \) [75]. This value of \( r_H \) results from \( r_{H0} = 1 \) in Eq. (63) with the anisotropy of the electron mass in silicon taken into consideration. It is important here to point out that a value of \( r_{H0} = 1 \) indicates that the semiconductor has already become degenerate [77]. Vice versa, the reduction of the Hall factor can be taken as an indication that the importance of scattering at charged impurities decreases at sufficiently high doping
levels. The apparent contradiction between the Hall factor found experimentally and predicted by the model can be reconciled by noting that the effect of the screening due to the presence of majority charge carriers has not been accounted for. This kind of screening is expected at very high doping levels at which doping acts not only as a source of Coulomb scattering at ionized impurities but simultaneously reduces it due to the increase in the concentration of majority carriers.

To account for the screening of ionized impurities by majority carriers, the model proposed should be adapted accordingly. The suggested modification for the degenerate case is based on an analogy between screened ionized impurities and neutral impurities. At sufficiently low dopant concentration, the distances between the ionized impurities are sufficiently large so that the free electrons can be considered to exist separately from them. As the impurity concentration and with it the concentration of free electrons increases, electrons will spend on their paths more and more time in the vicinity of ionized impurities. For very high dopant concentrations, impurities will find themselves surrounded by alternating electrons which compensate their charge. In terms of the power-law energy dependence of the relaxation times, the power index \( s \) in Eq. (53) should change accordingly from the value of \(-3/2\) typical for ionized impurity scattering to the value of 0 that is valid for the scattering on the neutral centers. Evidence from the measurements of Hall factors indicates that this decrease happens at a doping level exceeding about \(3 \cdot 10^{18} \text{ cm}^{-3}\) which corresponds closely to the Mott transition \([78]\). To include the effect in our Hall-factor calculation, based on the reasoning above, the predicted dependence of the power index \( s \) on doping concentration \( N_D \) was modeled empirically in the following form:

\[
s = 1.5 \cdot \left( \frac{1}{1 + \left( \frac{3 \cdot 10^{19}}{N_D} \right)^{1.2} - 1} \right) \tag{66}
\]

A graphical representation of this relationship can be found in Fig. 25. In accordance with Eq. (66), the power index \( s \) changes from \(-3/2\) to 0 when dopant concentration grows from zero.
5.2 Hall factor in bulk silicon

to infinity. At low dopant densities, when screening of impurities by electrons is negligible, $s$ has its minimum equal to $-3/2$. With increasing screening, the importance of Coulomb scattering will decrease, which is reflected in the increase of the constant $s$. Finally, at high doping levels around $2 \cdot 10^{20}$ cm$^{-3}$, the scattering is similar to that at neutral impurities, which is reflected in the tendency of $s$ towards the value of 0.

![Screening of the ionized centers](image)

$\tau_{\text{coul}} = a \cdot E^{-s_{\text{coul}}}$

**Fig. 25**: Dependence of the power index $s$ for Coulomb scattering on dopant density including screening [VU1].

Taking the mobility degradation due to phonon and Coulomb scattering in the phosphorus-doped silicon bulk material and introducing the effect of screening at high doping levels discussed above into account, the Hall factor in the bulk Si was calculated using the method presented in Section 5.1 as a function of dopant concentrations. The results of this calculation are shown in Fig. 26 in comparison with the measurements reported in the literature for Si [74].

In accordance with the predictions of the new method, the Hall factor in bulk silicon increases up to a doping level of $4 \cdot 10^{18}$ cm$^{-3}$. When the phosphorus concentration increases further, the screening of the ionized impurities by the majority charge carriers sets in and leads to a
Chapter 5 Method of Hall Factor Calculation

continuous reduction of $r_H$ towards a value of 0.87 when the dopant density reaches a value of $2 \cdot 10^{20}$ cm$^{-3}$.

For a correct interpretation of the results, typical error bars of these measurements which are about 12% and independent of doping level are presented in Fig. 26. A very good agreement between calculations and experimental results confirms the validity of the new method for the calculation of Hall factors and allows to apply this method further to electronic devices like MOSFETs for which the additional complication by the interface imposes conventional approaches. The calculation of the Hall factor in the channel of SiC MOSFETs performed with the method described will be shown in Chapter 6, where the Hall-effect measurements are discussed.

![Fig. 26: Hall factor for electrons against phosphorus doping concentration in silicon [VU1].](image)
Chapter 6  Simulation Results and Discussions

To interpret the electrical characteristics of n-channel 4H-SiC MOSFETs determined by current-voltage and Hall-effect measurements, numerical simulations have been performed. On the basis of the MOSFET #E1 with a high background doping concentration, a simulation methodology has been developed and applied further to study the effects of temperature and bulk potential engineering upon transport properties in the channels of MOSFETs.

6.1 Simulation methodology: Current-voltage characteristics

To simulate the electrical characteristics of SiC MOSFETs, the interface traps which affect its performance have to be properly described. Currently, in simulations it is commonly accepted to focus on the traps which are related to the oxidation process of SiC, energetically located near the conduction band of SiC and assumed to be acceptors. However, it can not be excluded that other traps, which are specific to one or another fabrication process, can be introduced in addition and have an impact on the performance of MOSFETs. There are a few research groups who suggest that nitridation leads to a generation of donor impurity levels in the SiC bandgap which affect the transport properties in the channel of SiC MOSFETs. Different measurement techniques have been used already to investigate the behavior of nitrogen atoms introduced during the nitridation. As an example, using x-ray photoelectron spectroscopy (XPS), Kosugi et al. [79] showed that nitrogen atoms are not only embedded in the oxide layer but also remain fixed at the SiC/SiO₂ interface with an areal density of 1·10¹⁴ cm⁻² even after removal of the oxide layer by hydrogen-fluoride (HF) etching. To explain this result two assumptions have been made. The first one is that nitrogen atoms can form strong chemical bonds at the interface. The
second one is that nitrogen can be incorporated into the SiC and act as shallow donors. A similar conclusion has been given by Fiorenza et al. in [80], where an effect of post-deposition annealing (PDA) in N$_2$O ambient was analyzed using scanning capacitance microscopy. By measuring the carrier concentration in the n-type epitaxial layer of the MOS structure, it was demonstrated that PDA in N$_2$O ambient leads to the formation of a sharp concentration peak below the SiC/SiO$_2$ interface. For example, an increase of the active doping concentration at the interface from $5 \cdot 10^{15}$ cm$^{-3}$, which is the concentration of the n-type epitaxial layer, up to $5 \cdot 10^{17}$ cm$^{-3}$ has been observed. The groups of Liu et al. [81] and Umeda et al. [82] have also proposed that some nitrogen atoms can diffuse into a very thin layer of 1-2 nm of SiC forming an “interfacial counter doping” during post-nitridation annealing. As a consequence, it can lead to the increase of the carrier concentration in the channel and to a decrease of $V_{TH}$ in the MOSFETs. Nevertheless, the current status of investigation of nitridation does not allow to assert explicitly how donor impurities influence the electrical properties of MOSFETs. For example, the recent investigation of Yoshioka reveals that because of the generation of donor traps near the SiC conduction band the channel mobility can increase if NO annealing is performed at a certain temperature [83].

It can be seen that the behaviour of nitrogen atoms introduced during nitridation as well as its role are very complex and still not fully understood. However, it seems that there is a common agreement that nitridation leads to the incorporation of donor impurities close to the conduction band of SiC. The same conclusion has been drawn in the current work analyzing the measurements with Sentaurus Device.

In this thesis, one of the main tasks for numerical simulation is to explain the physical reasons for the low performance of MOS transistors based on 4H-SiC with a gate oxide fabricated by thermal oxidation in N$_2$O atmosphere. For this purpose, numerical simulations with Sentaurus Device have been performed and analyzed step by step. First, for reference, current-voltage characteristics of n-channel transistors were calculated using the default simulation model that assumes an ideal interface between the gate oxide and the 4H-SiC semiconductor. The results of such simulations for the SiC MOSFET #E1 at a source-drain voltage of 0.1 V is shown in Fig. 27 in comparison with the results of the measurements.
Fig. 27: Comparison of default simulations and measurements for the MOSFET #E1.

As expected, the default simulations deviate from measurements significantly. This result confirms the necessity to include appropriate models in the simulation for physical processes which must be considered in SiC MOSFETs. As it was already discussed in the previous chapters, Near-Interface Trap and mobility degradation models are the most important models in the simulations of the lateral SiC MOSFETs. However, before applying the physical models to improve agreement with the measurements, a more careful look at the drain current simulated for an ideal interface and the measured drain current has to be taken. In Fig. 27 it can be seen that the SiC MOSFET with an ideal interface has at higher gate voltages, according to simulation, a significantly, i.e. about a factor of 50, higher current than the measured one. The inclusion of acceptor traps at the SiC/SiO$_2$ interface will reduce the drain current but enlarge the threshold voltage in comparison with the ideal MOSFETs behavior, as it was shown in Section 3.4.1. In Fig. 27 the opposite case is observed. The experimental threshold voltage is lower than that predicted by the simulation for an ideal MOSFET without any interface traps. Such a low threshold voltage can be explained either by the presence of a large amount of positive fixed charges at the SiC/SiO$_2$ interface or by the presence of donor states located energetically close to the conduction band of SiC. The initial research of the investigated MOSFET #E1 [84] indicated
two possible NIT models. The first one is the conventional model which is usually used in literature, where acceptor traps in the vicinity of the conduction band and a high concentration of positive fixed charges are assumed. The second one is a new NIT model which extends the conventional one by postulating the existence of donor traps near the conduction band in order to avoid unreasonably high concentrations of fixed charges at the interface. It was also proposed that the origin of the donor traps could be related to donor impurities introduced during oxidation. Considering that the oxidation and afterwards annealing have been done in a nitrogen-containing ambient, nitrogen is the best candidate for the donor traps. In accordance with the typical behavior of donor impurities, they provide additional electrons to the inversion layer of SiC MOSFETs, leading to a decrease of the threshold voltage.

To assess the amount of nitrogen which could affect the electrical characteristics of the studied MOSFETs, secondary ion mass spectroscopy (SIMS) has been performed by Probion Analysis in France. The sample used for the SIMS analysis was a MOS capacitor which has been oxidized in N$_2$O atmosphere and annealed in N$_2$ ambient under similar conditions as the studied MOSFETs. The result of the SIMS measurement is shown in Fig. 28.

Fig. 28: Nitrogen profile measured by secondary ion mass spectroscopy.
6.1 Simulation methodology: Current-voltage characteristics

The SIMS profile demonstrates the presence of a huge amount of nitrogen in the oxide and around the SiC/SiO\textsubscript{2} interface. The peak concentration of the nitrogen distribution was measured to be equal to \(3 \cdot 10^{20} \text{ cm}^{-3}\). It is usually expected that the depth of the peak is correlated with the position of the interface between oxide and semiconductor. However, it should be noted that the precise distribution of N at the interface and in SiC can not be obtained from SIMS because of the following effects. Firstly, SIMS gives the total concentration of the studied species instead of the electrically active one. Secondly, as the accurate position of the SiC/SiO\textsubscript{2} interface is unknown and ion beam mixing has occurred during measurement, the amount of nitrogen penetrated into the SiC can not be determined precisely. However, based on the existence of such a high concentration of nitrogen, as seen in Fig. 28, diffusion of N atoms in SiC at the high process temperatures used during device fabrication can not be excluded.

Taking into account the results of the SIMS measurement and the investigations of the research groups discussed above, the extended NIT model was decided to be used further in this work. The amounts of positive charges at the interface, i.e. the concentration of donor traps as well as positive fixed charges, were chosen to reproduce the sub-threshold slope in the current-voltage characteristics and the sheet carrier density obtained from the Hall-effect measurements. The best description of the measured electrical characteristics of the MOSFET #E1 was obtained by introducing donor traps with a level 50 meV below the conduction band and a concentration of \(2.5 \cdot 10^{12} \text{ cm}^{-2}\). Here it should be noted that a level at \(E_C – 50 \text{ meV}\) corresponds well to the level of the normal nitrogen donors on the hexagonal site in 4H-SiC, for which the ionization energy is equal to 52.1 meV [85].

To assess the influence of all interface charges of the NIT model on the electrical characteristics of SiC MOSFETs, i.e. positive fixed charge as well as donor and acceptor traps, the Near-Interface Trap model was included in the simulation without accounting for a mobility degradation model. To consider the effect of acceptor traps, the \(D_{IT}(E_T)\) distribution, shown in Fig. 16 for the MOSFET #E1, has been used. The parameters of the NIT models used for the simulations of MOSFETs #E1 as well as #E2, #W1 and #W2 are summarized in Table 8.
Chapter 6 Simulation Results and Discussions

Table 8. Parameterization of the extended NIT models used in the simulations

<table>
<thead>
<tr>
<th>Sample</th>
<th>Concentration of donor traps with level $E_C - 50$ meV (cm$^{-2}$)</th>
<th>Acceptor traps $(\text{cm}^{-2}\text{eV}^{-1})$</th>
<th>Fixed charge $(\text{cm}^{-2})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>#E1</td>
<td>$2.5 \cdot 10^{12}$</td>
<td>$D_{IT}(E_T)$ from Fig. 16</td>
<td>$4 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#E2</td>
<td>$1 \cdot 10^{11}$</td>
<td>$D_{IT}(E_T)$ from Fig. 16</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#W1</td>
<td>$1 \cdot 10^{11}$</td>
<td>$D_{IT}(E_T)$ from Fig. 16</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
<tr>
<td>#W2</td>
<td>$1 \cdot 10^{11}$</td>
<td>$D_{IT}(E_T)$ from Fig. 16</td>
<td>$1 \cdot 10^{11}$</td>
</tr>
</tbody>
</table>

The result of the simulation for the MOSFET #E1, performed only with the extended NIT model, is presented in Fig. 29 in comparison with the ideal and measured current-voltage characteristics.

![Fig. 29: Comparison between the simulated and measured current-voltage characteristics. The simulations have been performed assuming an ideal interface (solid line) and with the NIT but without mobility degradation models (dashed line).](image)

In Fig. 29 it can be seen that the simulation performed with the NIT but without mobility degradation models describes the sub-threshold slope of the measurements better than the simulation with an ideal interface. In comparison with the default simulation, the interface charges introduced a shift of the threshold voltage to lower values and decreased the current at gate voltages from 8 V till 20 V. The lowering of the threshold voltage is explained by the
inclusion of donor traps which provide electrons in the channel till their energetic level falls below the Fermi level.

To confirm the idea that the donor traps used in the simulations are related to nitrogen diffused in SiC, simulations with a very sharp profile of nitrogen described by an error function have been performed. It was found that a nitrogen profile with a peak concentration of \(4.8 \times 10^{19} \text{ cm}^{-3}\) within 1.5 – 2 nm at the interface, as shown in Fig. 30, results in a similar simulated \(I_D(V_G)\) curve as the single donor trap level used in the simulation of the MOSFET #E1. The main aim of such a simulation is to show that donor traps near the conduction band and nitrogen distributed within a thin layer on the SiC side lead to the same electrostatic properties of the transistor. For this purpose, taking an identical mobility of 50 cm\(^2\)/Vs and assuming no fixed charges and no acceptor traps at the interface, the current-voltage characteristics were simulated for both cases. A comparison of the current-voltage characteristics is shown in Fig. 31.

![Simulated nitrogen profile resulting in the “Nitrogen distribution” \(I_D(V_G)\) curve shown in Fig. 31.](image1)

![Comparison of the current-voltage characteristics simulated either with the donor trap level or with a nitrogen profile.](image2)

A quite good agreement between the drain currents simulated with the aforementioned models can be seen. The deviations at low gate voltages and up to 9 V are related to the different filling of charge state in these models during the variation of the gate voltage. Despite of it, the inclusion of the models in the simulations, either with the single donor trap level at the interface
or with the nitrogen distribution in the thin layer at the interface, leads to a lower threshold voltage similar as observed in the electrical measurements of the MOSFET #E1.

In a semiconductor, the energetic position of impurity levels depends on the impurity concentration. If the impurity concentration is low, the impurity atoms are located far from each other and a single impurity level in a bandgap of a semiconductor is formed. With an increase in the impurity concentration the distance between impurity atoms decreases and the concentration of the majority carriers increases. These effects lead to a shift of the single impurity level. See Section 3.3. Thus, if the impurity atoms have different concentrations, a band of states will form [78]. This means that, in reality, N atoms introduced in a thin layer in the SiC should form a band of donor states instead of a single level. For clarity, the N profile shown in Fig. 30 was converted into a relationship between interface trap density and trap energy, using Eq. (19). The result of the conversion is presented in Fig. 32.

![Graph showing donor trap density as a function of trap energy](image)

**Fig. 32:** Donor trap density as a function of trap energy calculated for the nitrogen profile shown in Fig. 30.

As it can be seen, nitrogen which is incorporated in a very thin SiC layer with the peak concentration at the interface leads to the formation of a donor band which merges into the conduction band at high dopant concentrations. To compare the effects of a single trap level and
6.1 Simulation methodology: Current-voltage characteristics

a band of traps on the drain currents, the density of donor traps as a function of trap energy, shown in Fig. 32, was introduced into Sentaurus Device via a table function. The current-voltage characteristics were simulated in analogy to the simulations presented in Fig. 31. A comparison between simulated results performed with the single donor trap level, the band of donor states and the sharp nitrogen distribution is shown in Fig. 33.

![Fig. 33: Comparison of the drain currents simulated with a single donor trap level, with a nitrogen profile or with a band of donor traps.](image)

From the comparison it can be seen that the simulations carried out with the three different models are in a quite good agreement. This means that all of them can be used in the numerical simulation of the electrical characteristics of the studied MOSFETs. However, considering computational and time demands, the usage of the model with the nitrogen distribution is much less beneficial in comparison with the two others. The inclusion of the band of donor states in the simulation does not give a significant difference with the simulation performed with a single donor trap level. The explanation of this result is that donor traps near the conduction band have the main impact upon the electrical characteristics of the MOSFETs. Thus, for the sake of
simplicity, the conventional NIT model extended by introducing a single donor trap level was used in the simulations discussed further below.

It can be clearly seen in Fig. 29 that when only the electrostatic effect of the NIT model is included, the simulated drain current is still much higher than the measured one. This is explained by the fact that no mobility degradation by carrier scattering was taken into account yet. The results of this analysis indicate that the main reason for the low performance of SiC MOSFETs in the on-state is the scattering of the electrons in the inversion layer. To improve further the agreement between simulated and measured results, mobility degradation, as described in Chapter 3, has been accounted for in addition to the NIT model. The final simulation result for the current-voltage characteristics of the MOSFET #E1 is presented in linear and logarithmic scales in Fig. 34. Therein, it can be seen that the simulation with the newly developed NIT and the calibrated mobility models for 4H-SiC excellently reproduce the measurements.

![Fig. 34: Comparison of current-voltage characteristics simulated with NIT and mobility degradation models with the measurements for the MOSFET #E1.](image-url)
Simulations of the current-voltage characteristics for the MOSFETs #E2, #W1 and #W2 from the second manufacturing run, results of which will be shown in Section 6.3, have been performed in analogy to the simulations of the MOSFET #E1. Here it should be noted that the amount of positive charge needed to bring the simulated and measured threshold voltage for the MOSFETs #E2, #W1, #W2 into agreement was significantly less in comparison to the amount for the MOSFET #E1. The required concentration of donor traps with the same level of $E_C - 50$ meV was only $1 \cdot 10^{11}$ cm$^{-2}$. Additionally, the reduction of the concentration of positive fixed charges was also found for the MOSFETs #E2, #W1 and #W2 as mentioned in Section 3.4.2.

The decrease of the concentration of the donor traps in the samples from the second manufacturing run can be partially explained by a shorter nitridation time [86]. However, the total reduction of the positive charges, i.e. the concentrations of donor traps and fixed charges, can be related mainly to a replacement of the inner tube of the oxidation furnace before the second manufacturing run [87]. The necessity of the replacement was caused by the contamination of the tube with a high concentration of positive ions as observed experimentally. This means that chemical elements as phosphorus, sodium and other donor impurities possibly present in the first run could have an impact on the electrical characteristics of MOSFET #E1.

### 6.2 Simulation methodology: Hall-effect measurements

The correct determination of the channel mobility is one of the main challenges in the characterization of SiC MOSFETs. One of the easiest methods to obtain the channel mobility is to extract it from current-voltage characteristics by calculation of field-effect $\mu_{FE}$ or effective $\mu_{EFF}$ mobilities [46]:

$$\mu_{FE} = \frac{L}{WV_D C_{ox}} \left( \frac{\partial I_D}{\partial V_G} \right)$$  \hspace{1cm} (67)
The calculation of field-effect and effective mobilities is widely used and well established in Si MOSFETs. In SiC MOSFETs it can be used also but only for a qualitative analysis [46]. The existence of a high trap density at the SiC/SiO₂ interface in comparison to the Si/SiO₂ interface introduces inaccuracies in the determination of the mobility in SiC MOSFETs from their current-voltage characteristics. The main inaccuracy in the calculation is related to the fact that Eq. (67) and Eq. (68) is valid if the sheet carrier density in the inversion channel \( n_{\text{inv}} \) is approximately equal to the total number of electrons \( n_{\text{total}} = C_{\text{ox}}(V_G - V_{\text{TH}})/q \) which can be theoretically induced at the interface by applying a certain gate voltage [46]. However, due to the high density of traps at the SiC/SiO₂ interface, this approach is not suitable for SiC MOSFETs and leads to an underestimation of the mobility in the channel. To perform precise studies of the transport properties in SiC MOSFETs and to analyze the transport mechanisms in the channel of the devices, a more accurate method of characterization is needed. One of the methods which allows to determine the sheet carrier density as well as the mobility in the inversion layer independently is based on Hall-effect measurements. However, as it was already discussed in Chapter 5, the major disadvantage of the Hall-effect measurements is the unknown Hall factor. In case of SiC MOSFETs, the uncertainty related to the Hall factor is even more critical than in Si MOSFETs because of the dominance of Coulomb scattering in the inversion channel. The higher the amount of interface traps, the higher the Coulomb scattering. Considering that in theory the Hall factor calculated for the exclusive case of Coulomb scattering has a maximum value of 1.93 [41], a higher value of the Hall factor will be expected in the inversion channel of SiC MOSFETs than of Si ones. This means, to determine the sheet carrier density and the mobility in the channel of SiC MOSFETs from Hall-effect measurements accurately, one has to calculate the Hall factor in the channel of the transistor.

In order to calculate the Hall factor for the electrons in the channel of SiC MOSFETs using the scattering relaxation time approximation discussed in Chapter 5, the values of \( <\tau> \) and \( <\tau^2> \) at
the SiC/SiO\textsubscript{2} interface have to be determined. Based on the method of the Hall factor calculation, where the interdependence between scattering relaxation time and mobility is considered, the Hall factor and the mobility in the channel of MOSFETs are determined by the same scattering mechanisms. It is well known that the main limiting mechanisms of the total mobility in the inversion layer of SiC MOSFETs are Coulomb scattering at ionized impurities in the bulk and at the interface charges as well as surface-roughness, surface-phonon and bulk-phonon scattering. Taking into account scattering mechanisms which are specific for the channel of MOSFETs and using Eq. (57) and Eq. (58), the average scattering relaxation times can be given [68]:

\[
< \tau > = \frac{\int_{0}^{\infty} x^{3/2} e^{-x} dx}{\int_{0}^{\infty} x^{3/2} e^{-x} dx} \tau_{IMP}^{-1}(x) + \tau_{C}^{-1}(x) + \tau_{SR}^{-1}(x) + \tau_{SP}^{-1}(x) + \tau_{BP}^{-1}(x)
\]  

\[
< \tau^{2} > = \frac{\int_{0}^{\infty} x^{3/2} e^{-x} dx}{\int_{0}^{\infty} x^{3/2} e^{-x} dx} \left[ \tau_{IMP}^{-1}(x) + \tau_{C}^{-1}(x) + \tau_{SR}^{-1}(x) + \tau_{SP}^{-1}(x) + \tau_{BP}^{-1}(x) \right]^{2}
\]  

Therein, the scattering relaxation time components \( \tau_{IMP} \) and \( \tau_{C} \) are associated with Coulomb scattering at ionized impurities in the bulk and at the interface charges, \( \tau_{SR} \), \( \tau_{SP} \) and \( \tau_{BP} \) with surface-roughness, surface-phonon and bulk-phonon scattering, respectively.

Applying the method of Hall factor calculation, the scattering relaxation time components in Eq. (69) and Eq. (70) can be easily determined from the respective mobility components. In the current work, the calculation of the mobility components is based on the TCAD simulation of the current-voltage characteristics, which reproduce the measured one. However, it should be noted here that the implementation of the mobility degradation models in Sentaurus Device allows only to assess the total channel mobility via its influence on the drain current and not the individual mobility components themselves. To evaluate the contributions of the mobility components to the total channel mobility, a method of small variations was used in the simulations. This method
Chapter 6 Simulation Results and Discussions

is based on applying a small variation to one of the mobility components via its accessible parameters and in calculating its value from the resulting variation of the channel current.

To present clearly the idea of the method of small variations, the method is illustrated by the following example. It is known that for small drain voltages, i.e. $V_D \leq 0.10$ V, the average mobility of the electrons in the inversion layer can be derived from the current-voltage characteristics of the device [46]:

$$\mu = \frac{I_D L}{qWV_D n_{inv}}$$  \hspace{1cm} (71)

If the total mobility varies from the initial value $\mu$ to a new value $\mu'$ that is close to $\mu$, the following expression can be obtained from Eq. (71):

$$\frac{\mu'}{\mu} = \frac{I_D'}{I_D}$$  \hspace{1cm} (72)

Therein, $I_D'$ is a recalculated drain current that reflects the change in mobility from $\mu$ to $\mu'$.

The channel mobility determined by Eq. (71) from the current-voltage characteristics can be also given as a sum of the mobility components using Matthiessen’s rule in Eq. (23). Based on it one of the inverse mobility components $\mu_i^{-1}$ can be varied by the multiplication with a value $\delta=1+\Delta$, where $\Delta$ is much smaller than unity. Then, applying some mathematical transformations to Eq. (23), the following expression for the new value of $\mu'$ can be obtained:

$$\frac{1}{\mu'} = \frac{1}{\mu} + \frac{\Delta}{\mu_i}$$  \hspace{1cm} (73)

Varying each mobility component used in the TCAD simulation of the current-voltage characteristics, the mobility component $\mu_i$ associated with the particular scattering mechanisms in the channel of SiC MOSFETs can be derived by:
6.2 Simulation methodology: Hall-effect measurements

\[ \mu_i = \frac{I_D' \mu \Delta}{I_D (1 - I_D')} \]  

(74)

Using the method of small variations as described above, the mobility components have been calculated as a function of gate voltage. To check the correctness of the method, the total mobility in the MOSFET #E1 was calculated by Matthiessen’s rule using the mobility components extracted and compared with the mobility calculated from the simulated current-voltage measurements, using Eq. (71). Here it should be noted that for the calculation of the total mobility with Eq. (71), the sheet carrier density \( n_{inv} \) was extracted from the numerical simulation of the current-voltage characteristics. A comparison of the total mobilities obtained by the two methods is presented in Fig. 35.

Fig. 35: Comparison of the total mobility in the channel of the MOSFET #E1 calculated from the simulated current-voltage measurements and from the mobility components using Matthiessen’s rule. The mobility components have been obtained using the method of small variations.
From the comparison it can be seen that the mobility calculated using Matthiessen’s rule and the mobility extracted directly from the current-voltage characteristics shown in Fig. 34 are in excellent agreement. This means that the method of small variations is self-consistent and can be applied to extract the mobility components required for the calculation of the Hall factor.

The results of the extraction of the mobility components in the channel of the MOSFET #E1 is shown in Fig. 36 in comparison to the total channel mobility. To allow an entire comparison of the impact of the individual scattering mechanisms upon the total mobility, the mobilities are depicted as reverse values.

![Graph showing inverse mobility components in comparison to the inverse total mobility for the MOSFET #E1.](image)

Fig. 36: Inverse mobility components in comparison to the inverse total mobility for the MOSFET #E1.

In Fig. 36 it can be seen that the inverse mobility components associated with Coulomb scattering at ionized impurities in the bulk ($1/\mu_{IMP}$) as well as bulk-phonon ($1/\mu_{BP}$) and surface-phonon ($1/\mu_{SP}$) scattering are much lower than the inverse total mobility in the channel. This indicates their negligibility for the total mobility as well as for the electrical performance of the device. In contrast, the inverse mobility components associated with Coulomb scattering at the interface charges ($1/\mu_C$) and with surface-roughness scattering ($1/\mu_{SR}$) are the predominant
contributions to the total channel mobility for the MOSFET with a high background doping concentration. This conclusion is also in agreement with findings of others [52].

Taking the dependence of the mobility components on the gate voltage and using the method of Hall factor calculation presented, the Hall factor in the n-channel of SiC MOSFETs was calculated. The result of the calculation is shown in Fig. 37 and reveals a strong dependence of \( r_H \) on the gate voltage applied. It should be noted that mass anisotropy, discussed in Section 5.1, was already taken into account by multiplying the Hall factor with the Hall mass factor of 0.98 for SiC.

![Fig. 37: Hall factor as a function of gate voltage in the channel of the MOSFET #E1 [VU2].](image)

Depending on the gate voltage applied, \( r_H \) varies in the case of the MOSFET #E1 between 1.29 and 1.43. The relatively high values of the Hall factor can be explained by the predominance of Coulomb scattering at the interface charges and surface-roughness scattering. In theory it was shown by Sze that the Hall factor for the exclusive case of Coulomb scattering is equal to 1.93 when the mass anisotropic effect is neglected [41]. For the exclusive case of surface-roughness scattering, assuming that its scattering centers are neutral and the scattering mechanism is independent of electron energy [70], the Hall factor is equal to unity. Considering that \( r_H \) in the
channel of the MOSFET #E1 is determined predominantly by the two aforementioned scattering mechanisms, the values of $r_H$ are expected somewhere between the two extreme values for these scattering mechanisms. The reduction of the Hall factor with an increase in gate voltage reflects the behavior of the mobility components as a function of gate voltage. For clarity, the dominant mobility components associated with Coulomb scattering at interface charges and surface-roughness scattering are shown as a function of gate voltage in Fig. 38. To demonstrate better how mobility components change with gate voltage, the mobilities are depicted in a linear scale.

![Graph showing mobility components associated with Coulomb scattering and surface-roughness scattering](image)

**Fig. 38:** Mobility components associated with Coulomb scattering at the interface charges and surface-roughness scattering in comparison to the total mobility for the MOSFET #E1.

As it can be seen for the MOSFET #E1, the mobility component associated with surface-roughness scattering $\mu_{SR}$ slightly decreases with increasing gate voltage. The mobility component $\mu_C$ shows a distinct increase with increasing gate voltage. An important effect here is that the relative change of $\mu_C$ with the gate voltage is much stronger than $\mu_{SR}$. This means that the dependence of $r_H$ on the gate voltage mainly relates to Coulomb scattering at the interface charges. The increase of the mobility component $\mu_C$ indicates a reduction of Coulomb scattering at higher gate voltages. It can be explained by an increase of screening of the scattering centers.
due to the rise in the density of inversion electrons. As a consequence, a strong reduction of $r_H$ is observed.

Taking the results of the calculation of the Hall factor, shown in Fig. 37, and using Eq. (8) and Eq. (9) for the sheet carrier density and the channel mobility, respectively, the Hall-effect measurements were corrected with the newly calculated Hall factor. The results of the newly interpreted Hall-effect measurements are compared with the simulation results in Fig. 39 and Fig. 40 for the sheet carrier density and the drift mobility, respectively [VU2]. In addition, a standard interpretation of the same measurements using the assumption of $r_H = 1$ is shown. The simulated sheet carrier density depicted in Fig. 39 was derived from the numerical simulations of the current-voltage characteristics, shown in Fig. 34. Afterwards, the channel mobility was calculated from Eq. (71) using the same current-voltage characteristics and the sheet carrier density derived from the numerical simulation.

Fig. 39: Sheet carrier density as a function of gate voltage in the channel of MOSFET #E1.

Fig. 40: Drift mobility as a function of gate voltage in the channel of MOSFET #E1.

A quite good agreement between the measurements corrected with our new gate-voltage-dependent Hall factor and the simulations performed with Sentaurus Device of Synopsys is demonstrated in Fig. 39 and Fig. 40. The deviations seen for the mobility at low gate voltages are not well understood. One of the explanations can be inaccuracies in the relative contributions of the scattering mechanisms to the channel mobility.
The interpretation of the Hall-effect measurements with $r_H = 1$ shows deviations from the simulated results and leads to an underestimation of the sheet carrier density and to an overestimation of the mobility. The misinterpretation of the Hall-effect measurements amounts approximately to 30 – 40% depending on the gate voltage and can be easily prevented by considering the dependence of the Hall factor on the scattering mechanisms specific for the electron transport in the channel of SiC MOSFETs.

6.3 Effect of bulk potential engineering upon transport properties in SiC MOSFETs

The scattering of electrons in the channel is the main reason for the low performance of n-channel SiC MOSFETs, as it was shown in Section 6.1. In particular, for the case of MOSFETs with a high background doping concentration, it was demonstrated that Coulomb scattering at the interface charges is the dominant scattering mechanism. This means, to increase the channel mobility, the impact of Coulomb scattering at the interface charges has to be reduced. Currently, the main strategy for the reduction of the aforementioned scattering mechanism is based on methodologies for the passivation of the interface traps. However, it is important to note that the intensity of Coulomb scattering depends not on the amount of traps by itself but on the amount of traps which are occupied and charged. The lower the amount of the charged interface traps, the lower the intensity of Coulomb scattering and the higher the channel mobility. In addition to the passivation methodologies, the amount of charged interface traps can be controlled by changing the background doping concentration $N_A$. A change in the background doping concentration corresponds to a change in the bulk potential $\psi_B$. That’s why a variation in the background doping concentration can be referred to as “bulk potential engineering”. By changing the bulk potential and, as a consequence, the band-bending required to invert the MOSFET channel, the occupation of the traps located at the interface also changes. Along that line, assuming acceptor-like traps it has been suggested that a reduction of the background
doping concentration leads to a reduction of the density of charged interface traps and with them of Coulomb scattering [31,88,89]. The reduced density of charged interface traps was then taken as an explanation for the mobility increase in lateral SiC MOSFETs found experimentally. However, it was found in the current work that an explanation of the increased channel mobility requires a broader view of the effects associated with a decreasing $N_A$.

To study the effect of bulk potential engineering, only the MOSFETs #E2, #W1 and #W2, which have been fabricated under identical conditions, have been taken into account. As it was mentioned in Chapter 2, the background doping concentration in the MOSFETs #W1 and #W2 was changed by multiple implantations. It is well known that implantation can introduce additional defects which could affect the electrical characteristics of the device. However, it was found out on the basis of lateral n-channel SiC MOSFETs that implantation does not generate any traps which have an impact on the device performance [31,90]. In contrast, it was shown that implanted MOSFETs may even have higher mobilities than MOSFETs fabricated on epitaxial layers with the same background doping concentrations. Based on these results and considering that the interface traps are mainly determined by the oxidation process, one would expect that devices fabricated under the same oxidation conditions have a very similar $D_{IT}(E_T)$ distribution despite the different doping concentrations $N_A$.

To interpret the doping dependence of the electrical measurements performed, the simulation methodology developed for the MOSFET #E1 was applied. Firstly, the current-voltage characteristics have been reproduced numerically in Sentaurus Device using NIT and mobility degradation models. The NIT model used in the simulations takes into account the contributions of acceptor traps described by the $D_{IT}(E_T)$ distributions shown in Fig. 16, as well as of donor traps and fixed charges as discussed in Section 6.1. A description of the mobility degradation model was given in Chapter 3. A comparison of the simulated and measured drain currents is shown in Fig. 41.
Based on the successful simulation of the current-voltage characteristics, the Hall factor in the channel was calculated for all studied MOSFETs #E2, #W1 and #W2 in analogy to the calculation done for the MOSFET #E1 in Section 6.2. The respective results are presented in Fig. 42.

**Fig. 41**: Comparison of the simulated (lines) and measured (symbols) current-voltage characteristics [VU3].

**Fig. 42**: Hall factor in the channel of SiC MOSFETs with different background doping concentrations [VU3].
It can be seen that the Hall factor depends not only on the gate voltage applied but also on the background doping concentration of the MOSFETs. With decreasing doping concentration $N_A$, the values of the Hall factor decrease strongly. Considering that for the exclusive case of Coulomb scattering, the Hall factor has the maximum value of 1.93, as discussed in the previous chapters, the strong reduction of the Hall factor with decreasing $N_A$ can be mainly explained by the reduction of Coulomb scattering in the channel. Taking the results in Fig. 42 and using Eq. (8) and Eq. (9), the sheet carrier density and the channel mobility were determined from the Hall-effect measurements. In Fig. 43 and Fig. 44, the respective values are compared to the simulation results obtained in analogy to the previous one for the MOSFET #E1 from the reproduced doping dependence of the current-voltage characteristics presented in Fig. 41 [VU3].

In Fig. 43 and Fig. 44 it can be seen that the sheet carrier densities as well as the drift mobilities derived via the doping-dependent Hall factor are in very good agreement with the simulations. Analyzing the substrate doping dependence of the SiC MOSFET characteristics, it can be seen that the drain current and channel mobility, presented in Fig. 41 and Fig. 44, increase strongly with decreasing $N_A$ while the sheet carrier density shown in Fig. 43 decreases.
As it was mentioned above, the $D_{IT}(E_T)$ distribution is usually assumed to be independent of the background doping concentration of MOSFETs. However, to reproduce the electrical measurements performed, in particular the sheet carrier density, it was observed that different $D_{IT}(E_T)$ distributions for the MOSFETs #E2, #W1 and #W2 had to be used in Sentaurus Device. Thus, considering that the interface trap density at high trap energies has been extracted from the Hall-effect measurements which have been performed exactly on the studied MOSFETs, the $D_{IT}(E_T)$ distribution at low trap energies, obtained from C-V measurements and shown in Fig. 22, has been mostly adjusted in the simulations. A comparison of the interface trap density as a function of trap energy used in Sentaurus Device and the one extracted from C-V measurements is shown in Fig. 45.

![Fig. 45: Comparison of the $D_{IT}(E_T)$ distributions used in the simulations of the MOSFETs #E2, #W1 and #W2 and the $D_{IT}(E_T)$ distribution extracted from C-V measurements.](image)

Comparing the parts of the $D_{IT}(E_T)$ distributions at low trap energies as found by the simulations, it can be seen that with an increase in $N_A$ the density of interface traps decreases. The observed shift of the $D_{IT}(E_T)$ distribution extracted from C-V measurements is not well understood and needs to be investigated further. One of the reasons can be related to the usage of the p-MOS capacitor on an n-doped substrate for the characterization of the n-channel MOSFET on a p-
doped substrate. However, in Fig. 45 it can be seen that the $D_{IT}(E_T)$ distribution extracted from C-V measurements fits to the $D_{IT}(E_T)$ distribution found in the simulation for the MOSFET #W1. It is interesting to note that in this case the background doping concentrations of the n-channel MOSFET and the p-MOS capacitor were quantitatively similar, $N_A$ and $N_D$ were $1 \cdot 10^{16} \text{ cm}^{-3}$ and $8 \cdot 10^{15} \text{ cm}^{-3}$, respectively.

A decrease of the interface trap density with increasing $N_A$ has been observed also at high trap energies by Hall-effect measurements as shown in Fig. 18. This result is unexpected. In the work of Kobayashi [91] it was shown that doping concentration and conduction type of SiC affect the thermal oxidation rate. The study has been carried out in the doping range from $2 \cdot 10^{15} \text{ cm}^{-3}$ till $1 \cdot 10^{19} \text{ cm}^{-3}$ and from $2 \cdot 10^{16} \text{ cm}^{-3}$ till $1 \cdot 10^{19} \text{ cm}^{-3}$ for p- and n-doped samples, respectively. It was found that in n-doped SiC the oxidation rate increases with increasing doping concentration while it slightly decreases in p-doped samples. The change of the oxidation rate was mostly observed at high doping concentrations. These results have been obtained by measuring the oxide thickness with spectroscopic ellipsometry. The decrease of the oxidation rate seen for p-doped SiC could explain the lower density of traps at high doping concentrations. However, in the framework of the MobiSiC project a determination of oxide thickness from C-V measurements did not show any dependence on the doping concentrations and, thus, can not be used as an argument to explain the difference of the $D_{IT}(E_T)$ distributions for the MOSFETs #E2, #W1 and #W2.

To see what happens when a common $D_{IT}(E_T)$ distribution is used for all three MOSFETs, the $D_{IT}(E_T)$ distributions shown in Fig. 45 were averaged and introduced into Sentaurus Device to simulate the sheet carrier density. The result of the averaging of the density of the interface traps is shown in Fig. 46.
Chapter 6 Simulation Results and Discussions

Fig. 46: Density of traps obtained by averaging of the $D_{IT}(E_T)$ distributions, shown in Fig. 45.

In addition to the simulations with the averaged density of traps, simulations have been performed under the assumption of an ideal interface. The results of the sheet carrier densities extracted from the respective simulations are presented in Fig. 47.

Fig. 47: Sheet carrier density for the MOSFETs with different $N_A$ simulated with the assumption of an ideal interface (left) and with the averaged $D_{IT}(E_T)$ distribution (right).

From both simulations it can be seen that a decrease in $N_A$ leads to an increase of $n_{inv}$ for the same gate voltage. However, in the Hall-effect measurements, a decreasing sheet carrier density was observed for decreasing $N_A$ values. The lower $n_{inv}$ at lower $N_A$ indicates an increase in the
amount of trapped electrons. Considering that the studied MOSFETs have identically fabricated gate oxides and that the implantation does not generate any additional defects which affect the MOSFET performance, the higher amount of charged traps at lower $N_A$ values is unexpected.

The results of the simulation performed with the averaged density of traps reveal that the impact of interface traps only on the performance of SiC MOSFETs can not describe the tendency of the sheet carrier density with $N_A$ in the measurements. This means that a broader view on the effect of bulk potential engineering has to be taken. In the current work it is suggested to explain the observed results on the basis of a model proposed by Agarwal [92]. There, it was suggested that not only interface traps influence the performance of SiC MOSFETs but also bulk traps located in the depletion width. It was further speculated that the bulk traps can be introduced during the fabrication processes. Irrespective of their origin, the mechanisms by which they might impact on the transport properties in the channel are the same as for interface traps, namely trapping and scattering of electrons. For clarity, the traps located at the interface and in the depletion width of SiC are shown in Fig. 48. Here, it should be noted that in the current work the influence of bulk traps is considered only as hypothesis which needs to be verified further.

Fig. 48: Band diagram with the traps located at the interface and in the depletion width [92].
To understand the possible effect of bulk traps, an analysis of the effects introduced by changing the background doping concentration of MOSFETs has been performed. As one of the characteristic parameters, the effective thickness of the inversion channel was estimated using the approximation suggested by Schwarz and Russek [93]:

\[ Z_{AV} = Z_{CL} + Z_{QM} \]  \hspace{1cm} (75)

where \( Z_{CL} \) and \( Z_{QM} \) are classical and quantum components of the average channel thickness described in terms of the effective field \( \mathcal{E}_{EFF} \):

\[ Z_{CL} = \frac{3}{2} \frac{k_B T}{q \mathcal{E}_{EFF}} \]  \hspace{1cm} (76)

\[ Z_{QM} = \left( \frac{9 \hbar^2}{4 m \perp q \mathcal{E}_{EFF}} \right)^{1/3} \]  \hspace{1cm} (77)

Therein, \( \hbar \) is the Dirac constant and \( m \perp \) is the effective electron mass in the direction perpendicular to the interface. The effective field was calculated by Eq. (78), with the sheet carrier density obtained from the Hall-factor-corrected Hall-effect measurements.

\[ \mathcal{E}_{EFF} = \frac{q}{\varepsilon_s} \left( N_A^+ x_D + \frac{1}{2} n_{inv} \right) \]  \hspace{1cm} (78)

Here it should be noted that under the effective thickness of the inversion channel one has to understand the average distance of the electrons in the inversion layer from the interface defined by [94]:

\[ Z_{AV} = \frac{\int_0^\infty n(x) x \, dx}{\int_0^\infty n(x) \, dx} \]  \hspace{1cm} (79)
The results of the calculation of the effective channel thickness are presented in Fig. 49 for different doping concentrations $N_A$ and gate voltages of 2 V, 10 V and 20 V.

According to the calculation of the effective channel thickness, the inversion layer becomes wider with decreasing doping concentration for all gate voltages applied. For example, at a gate voltage of 2 V the average thickness of the channel strongly increases from 4 nm to 13 nm with a decrease in $N_A$ from $5 \cdot 10^{16}$ cm$^{-3}$ to $1 \cdot 10^{15}$ cm$^{-3}$.

As a further characteristic, the band diagrams for the MOSFETs with $N_A$ being equal $5 \cdot 10^{16}$ cm$^{-3}$, $1 \cdot 10^{16}$ cm$^{-3}$ and $1 \cdot 10^{15}$ cm$^{-3}$ have been extracted from Sentaurus Device. They are shown in Fig. 50 together with the bulk potential $\psi_B$ and the depletion width $x_D$. Therein, $\psi_B$ and $x_D$ were calculated using Eq. (34) and Eq. (80) and assuming fully ionized dopants:

$$x_D = \sqrt{\frac{4\varepsilon_S \psi_B}{qN_A}}$$  \hspace{1cm} (80)
Chapter 6 Simulation Results and Discussions

Fig. 50: Band diagrams for n-channel MOSFETs with a) $N_A = 5 \cdot 10^{16}$ cm$^{-3}$ b) $N_A = 1 \cdot 10^{16}$ cm$^{-3}$ and c) $N_A = 1 \cdot 10^{15}$ cm$^{-3}$ [VU3].
6.3 Effect of bulk potential engineering upon transport properties in SiC MOSFETs

From the comparison of the band diagrams, shown above, it can be seen that with a decrease in $N_A$ from $5 \cdot 10^{16} \text{ cm}^{-3}$ to $1 \cdot 10^{15} \text{ cm}^{-3}$, $\psi_B$ decreases only from 1.45 V to 1.35 V while $x_D$ changes strongly and shows an increase from 0.25 $\mu$m to 1.7 $\mu$m.

Summarizing the results obtained, a decrease of the background doping concentration of MOSFETs leads to:

- a decrease of the bulk potential;
- an increase of the depletion width;
- an increase of the inversion channel thickness;

Thus, the lower sheet carrier density observed in the measurements at lower $N_A$ can be explained by the following hypothesis. Considering that at high doping concentrations the depletion width is small and that the inversion layer is located close to the interface, the sheet carrier density as well as the channel mobility is determined mainly by the traps located at the interface. With decreasing $N_A$ the depletion region as well as the inversion layer become wider and more and more bulk traps will affect the electron transport in the channel of the transistor in addition to the interface traps, leading to the observed decrease of the sheet carrier density.

Considering that the interface and bulk traps have electrically the same impact on the device characteristics, i.e. trapping and scattering of electrons from the inversion channel, the two kinds of traps can not be distinguished from the measurements performed. Thus, the density of traps extracted from the Hall-effect and C-V measurements is a sum of the densities of the interface and bulk traps. Taking the different contributions of the bulk traps at different doping concentrations into account, the difference of the $D_{IT}(E_T)$ distributions, observed for the studied MOSFETs and shown in Fig. 45, can be explained.

Based on the existing models of traps in Sentaurus Device a qualitative analysis of the impact of bulk traps upon transport properties in the channel of SiC MOSFETs has been performed. For this purpose, the sheet carrier densities of the MOSFETs with $N_A$ of $1 \cdot 10^{15} \text{ cm}^{-3}$, $1 \cdot 10^{16} \text{ cm}^{-3}$, $5 \cdot 10^{16} \text{ cm}^{-3}$ have been simulated considering the effect from the bulk traps only. A homogeneous
distribution of the bulk traps has been assumed in these simulations. For all three MOSFETs, the concentration of the traps was varied in the range from $1 \cdot 10^{15}$ cm$^{-3}$ till $1 \cdot 10^{17}$ cm$^{-3}$, as it was suggested by Agarwal [92], and further up to $1 \cdot 10^{19}$ cm$^{-3}$. The results of the simulation showed for all concentrations of bulk traps an increase of the sheet carrier density in the channel with decreasing $N_A$. This means that a lower sheet carrier density at lower $N_A$, as it was observed in the Hall-effect measurements, can not be explained by a simple model of bulk traps. Considering that it was assumed, for simplicity, that the concentration of bulk traps does not depend on the doping concentration $N_A$ and changes for the studied MOSFETs only because of the change of their depletion width, the results of the simulation can mean that for the reduction of $n_{inv}$ with decreasing $N_A$ the bulk traps could be non-uniformly distributed over depth in the SiC. However, because of limitations of the models for the spatial distributions of traps and limitation of time for the current work, only a homogeneous distribution has been tested. Here it should be noted that even with the homogeneous distribution of traps it was found that the most probable influence from the traps in the bulk can be expected from traps located closer to the interface with energetic levels near the conduction band of SiC.

To understand the reason for the increase of the channel mobility despite the increase of the amount of charged traps, the mobility components as a function of gate voltage have been analyzed for the studied MOSFETs. The calculation of the mobility components has been done using the method of small variation described in Section 6.2. The results of the calculations are presented in Fig. 51. It should be noted that the mobility components associated with Coulomb scattering at ionized impurities in the bulk ($\mu_{IMP}$) and with bulk-phonon scattering ($\mu_{BP}$) are not shown here because of their negligible contributions to the channel mobility at room temperature.
6.3 Effect of bulk potential engineering upon transport properties in SiC MOSFETs

Fig. 51: Mobility components in the channel of 4H-SiC MOSFETs with a) $N_A = 5 \cdot 10^{16} \text{ cm}^{-3}$ b) $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$ c) $N_A = 1 \cdot 10^{15} \text{ cm}^{-3}$. 
From the comparison of the most relevant mobility components in Fig. 51, it can be seen that Coulomb scattering at the interface charges is the dominant scattering mechanism at room temperature for all doping concentrations and gate voltages. With decreasing doping concentration the mobility component associated with Coulomb scattering at the interface charges increases strongly. As a result, the channel mobility also increases with decreasing doping concentration. For clarity, the mobility component $\mu_C$ is shown separately in Fig. 52 for the studied MOSFETs. The increase of $\mu_C$ indicates a reduction of Coulomb scattering at the charged traps despite the higher amount of charged traps at lower $N_A$ as discussed above. This means that the impact of the charged traps upon the channel mobility decreases with decreasing doping concentration.

![Fig. 52: Mobility component associated with Coulomb scattering at the interface ($\mu_C$) in the channel of SiC MOSFETs with different background doping concentrations.](image)

Here it should be noted that in the current simulation the effect of the decrease of Coulomb scattering at the interface charges despite the higher density of interface traps has been achieved artificially by the calibration of the model for $\mu_C$ to reproduce the electrical measurements. However, taking into account the model of Agarwal who suggests the existence of bulk traps, the increase of the channel mobility with decreasing doping concentration can be explained by the combination of several mechanisms. Firstly, the additional charged bulk traps at lower values of
$N_A$ contribute additionally to Coulomb scattering of the channel electrons. However, since the density of the bulk traps is usually much smaller than the local density of the traps at the interface, Coulomb scattering at the former should be much smaller than at the latter. Secondly, due to the decrease of the bulk potential with decreasing $N_A$, the amount of the charged interface traps decreases. Finally, since the thickness of the inversion layer depends on the doping concentrations, the depth dependence of the mobility in the transistor plays a role. In the work of Potbhare [44] it was shown that the local mobility of SiC MOSFETs strongly increases when moving away from the interface into the bulk of the SiC crystal. This was explained by the quick decrease of the Coulomb potential which leads to a lower impact of the charged interface traps on mobility. Considering that with decreasing background doping concentration, the thickness of the channel increases, the channel mobility also increases. Thus, the influence of bulk potential engineering on the transport properties in the channel of SiC MOSFETs can be explained by the combination of several effects, discussed above, which result in a lower sheet carrier density but in a much higher channel mobility and drain current at lower background doping concentrations.

### 6.4 On the temperature dependence of the electrical characteristics of SiC MOSFETs

Since SiC MOSFETs are well suited for operation at high temperatures due to the SiC material properties, the temperature dependence of the electrical characteristics of n-channel 4H-SiC MOSFETs was studied. For this purpose, in the current work, current-voltage and Hall-effect measurements have been numerically simulated in the temperature range from 300 K till 400 K for the MOSFET #E1 and from 300 K till 500 K for the MOSFET #E2. For the other MOSFETs, no temperature-dependent measurements were available from the MobiSiC project.

It is well known that the temperature variation has two main effects on the transport properties in the channel of SiC MOSFETs. The first one is a change in the contributions of the scattering
mechanisms to the channel mobility. It has been already discussed that the device performance of lateral SiC MOSFETs is limited by Coulomb scattering at ionized impurities in the bulk and at the interface charges as well as by surface-roughness, surface-phonon and bulk-phonon scattering. Each kind of scattering mechanisms has its specific temperature dependence. As an example, with an increase in temperature, Coulomb scattering decreases but phonon scattering increases. Depending on the relative contributions of the aforementioned scattering mechanisms to the channel mobility, the variation of the temperature could result in a change of the dominant mechanism by which carriers are scattered in the inversion channel. The second effect of temperature is a change of the bulk potential and, as a consequence, of the occupation of the interface traps. In analogy to a decrease of the doping concentration $N_A$, an increase of temperature leads to a decrease of the bulk potential. Assuming acceptor-like traps it was shown that it results in a lower amount of charged interface traps [89, 95]. Considering that these effects are taken automatically into account in Sentaurus Device when the device temperature is changed, the electrical characteristics of SiC MOSFETs have been numerically simulated on the basis of the NIT and mobility degradation models described in Chapter 3. The results of the simulations of the drain currents are compared with the measurements in Fig. 53.

![Fig. 53: Current-voltage characteristics for the MOSFETs #E1 (left) [VU4] and for the MOSFET #E2 (right). Lines represent the simulations, symbols measurements.](image)

From the comparison above it can be seen that the developed models excellently reproduce the temperature dependence of the drain currents. An interesting effect shown in Fig. 53 is that the
6.4 On the temperature dependence of the electrical characteristics of SiC MOSFETs

different background doping concentrations lead to different temperature dependences of the current-voltage characteristics. At high $N_A$ the drain current strongly increases with increasing temperature while at low $N_A$ the drain current is almost independent of temperature, showing a slight increase at low gate voltages and a slight decrease at high gate voltages. In n-channel 4H-SiC MOSFETs it is often assumed that Coulomb scattering at the interface charges is always the dominant scattering mechanism due to the high trap density. This would mean that with increasing temperature the drain current should always increase. However, the different temperature dependence of the drain current measured indicates a change in the dominant scattering mechanism in the channel of SiC MOSFETs with increasing temperature.

In Section 3.5 it has been mentioned that to reproduce the temperature dependence of the electrical characteristics of SiC MOSFETs with different doping concentrations, a new model for the bulk mobility, shown in Eq. (25), has been developed on the basis of the conventional one. To motivate the implementation of the new model, firstly, the conventional one has to be analyzed. The bulk mobility is usually given by [50]:

$$\mu_{B,\text{conv}} = \mu_{\text{min}} \left(\frac{T}{300K}\right)^\alpha + \frac{\mu_{B_P,\text{conv}} - \mu_{\text{min}} \left(\frac{T}{300K}\right)^\alpha}{1 + \left(\frac{N_A}{N_{\text{ref}}} \left(\frac{T}{300K}\right)^\alpha\right)^2}$$  \hspace{1cm} (81)

where $\mu_{B_P,\text{conv}}$ represents bulk-phonon scattering defined as

$$\mu_{B_P,\text{conv}} = 950 \text{cm}^2/\text{Vs} \left(\frac{T}{300K}\right)^{-2.4}$$ \hspace{1cm} (82)

The values of the fitting parameters for Eq. (81) and for all the equations given below in this section can be found in Table 4.

Applying the conventional model for the bulk mobility instead of the new one, the temperature dependence of the current-voltage characteristics has been simulated for the MOSFET #E2. The results of the simulations are shown in Fig. 54 in comparison with the measurements performed.
As it can be seen in Fig. 54, the simulated drain current, in contrast to the measured one, increases strongly with an increase in temperature from 300 K till 500 K. However, if the device temperature increases further in the simulations, the simulated drain current, shown in Fig. 55, saturates and decreases at high gate voltages similar to the measured one. To understand the decrease of the simulated drain current, the mobility components, calculated using the method of small variation, have been analyzed at different temperatures. It was found that the main reason for the reduction of the drain current is a strong increase of bulk-phonon scattering with increasing temperature. Based on this result it was assumed that the temperature dependence of the measured drain current of the MOSFET #E2 can be also explained by bulk-phonon scattering. However, the fact that the simulation predicts a reduction in the drain current at higher temperature than in the measurements could mean that the temperature dependence of bulk-phonon scattering implemented in the conventional model as $\mu_{BP,\text{conv}} \sim (T/300K)^{-2.4}$ is not sufficient to describe the transport properties in the channel of SiC MOSFETs. It should be emphasized that this conclusion is made on the assumption that the temperature dependence of the mobility components associated with Coulomb scattering at the interface charges, surface-roughness and surface-phonon scattering is described correctly and does not need any additional
6.4 On the temperature dependence of the electrical characteristics of SiC MOSFETs

modifications. The necessity to correct the conventional model for the electron mobility in the bulk can be related to the fact that Eq. (81) for the electron mobility in the bulk represents an empirical model. The fitting parameters of the model were obtained by measurements performed on n-type SiC. This can introduce some inaccuracies in the model which describes the contribution of the bulk mobility to the channel mobility of MOSFETs.

Taking into account the results of the analysis performed, the mobility component associated with bulk-phonon scattering has been modified in Eq. (81) by reproduction of the measured drain current for the MOSFET #E2. In accordance with the new model, presented in Section 3.5, it is given by

$$\mu_{BP,new} = \mu_{BP1} \left( \frac{T}{300K} \right)^{\xi} + \mu_{BP2} \left( \frac{T}{300K} \right)^{\kappa} \tag{83}$$

Using the conventional model in Eq. (82) and the new model in Eq. (83) the mobility component associated with bulk-phonon scattering has been calculated as a function of temperature and is shown in Fig. 56.

Fig. 56: Comparison of the mobility component associated with bulk-phonon scattering calculated using the conventional and new models.
As it can be seen, to simulate the measured current-voltage characteristics of the MOSFET with $N_A = 1 \cdot 10^{15}$ cm$^{-3}$, the contribution of bulk-phonon scattering at elevated temperatures has to be on the average by a factor of two higher than it is predicted by the conventional model. To check the applicability of the suggested model for higher doping concentrations, this model was applied in the simulations of the temperature dependence of the electrical characteristics for the MOSFET #E1 with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$. The simulations of the MOSFET #E1 revealed that the suggested model leads to some deviations between simulations and measurements because of the strong reduction of the bulk mobility with increasing temperature. From this result one of the conclusions could be that bulk-phonon scattering which represents the vibration of the lattice might depend on the background doping concentration. In the case of high doping concentrations, the lattice could vibrate less intensively than at low concentrations. At the same time in Section 3.5 it was mentioned that the mobility in the bulk is determined by two scattering mechanisms, bulk-phonon scattering and Coulomb scattering at ionized impurities. This means that another reason for the deviations between simulated and measured electrical properties at high $N_A$ could be an inaccurate description of the impact of Coulomb scattering at ionized impurities at elevated temperatures. Thus, assuming that bulk-phonon scattering is independent of doping concentration, Coulomb scattering at ionized impurities was analyzed using the conventional model presented in Eq. (81). Taking into account that bulk-phonon scattering and Coulomb scattering at ionized impurities are combined by Matthiessen’s rule as it was shown in Eq. (24), the mobility component associated with Coulomb scattering at the ionized impurities $\mu_{IMP}$ has been calculated by

$$\mu_{IMP} = \left( \frac{1}{\mu_B} - \frac{1}{\mu_{BP}} \right)^{-1}$$  \hspace{1cm} (84)

where $\mu_B$ was calculated using the conventional model in Eq. (81). For the bulk-phonon mobility $\mu_{BP}$ in Eq. (81) and Eq. (84), the new model in Eq. (83) was used. The result of the calculation is presented in Fig. 57 for the doping concentrations of $1 \cdot 10^{15}$ cm$^{-3}$ and $5 \cdot 10^{17}$ cm$^{-3}$. 


In Fig. 57 it can be seen that the mobility component $\mu_{IMP}$ decreases with increasing temperature from 300 K till 500 K which indicates an increase of Coulomb scattering. However, it is known that in this temperature range Coulomb scattering at ionized impurities decreases with increasing temperature which leads to an increase of the mobility limited by ionized impurity scattering $\mu_{IMP}$ [96,97]. To avoid the contradiction in the temperature dependence of Coulomb scattering at ionized impurities, the conventional model was corrected by introducing a term $(T/300K)^\vartheta$ with $\vartheta = -12.5$ in the denominator as shown below:

$$
\mu_B = \mu_{min} \left( \frac{T}{300K} \right)^\alpha + \frac{\mu_{Bp,new} - \mu_{min} \left( \frac{T}{300K} \right)^\alpha}{1 + \left( \frac{T}{300K} \right)\vartheta \left( N_A^{-} \right) z} \tag{85}
$$

It should be noted that in some works [51] the term $(T/300K)^\vartheta$ has been already used but with much lower absolute value of power coefficient, i.e. $\vartheta$ was taken -0.76 and 0.73. However, such powers do not change downward tendency of the temperature dependence of $\mu_{IMP}$. The
correction of Coulomb scattering at the ionized impurities, presented in Eq. (85), has been obtained from the reproduction of the temperature dependence of the current-voltage characteristics for both MOSFETs #E1 and #E2, shown in Fig. 53. Using now the new model for the bulk mobility, the mobility component $\mu_{IMP}$ was calculated for $1 \cdot 10^{15}$ cm$^{-3}$ and $5 \cdot 10^{17}$ cm$^{-3}$ using Eq. (84). The result of the calculation of $\mu_{IMP}$ in comparison to $\mu_{BP}$ is shown in Fig. 58. Therein, it can be seen that the mobility component associated with Coulomb scattering at the ionized impurities increases now with increasing temperature.

![Mobility components associated with Coulomb scattering at the ionized impurities ($\mu_{IMP}$) and bulk-phonon scattering ($\mu_{BP}$), calculated using the new model.](image)

Fig. 58: Mobility components associated with Coulomb scattering at the ionized impurities ($\mu_{IMP}$) and bulk-phonon scattering ($\mu_{BP}$), calculated using the new model.

Summarizing the results from the analysis performed, the new model for the electron mobility in the bulk has been developed assuming:

- stronger increase of bulk-phonon scattering with temperature than it is predicted by the conventional model;
- decrease of Coulomb scattering at ionized impurities in the bulk with increasing temperature;
Here it should be noted that in the new model at 300 K the ratio of the contributions of $\mu_{\text{IMP}}$ and $\mu_{\text{BP}}$ has been taken from the conventional model and unchanged. Although the new model can well reproduce the characteristics of the studied MOSFETs with two doping concentrations, $1 \cdot 10^{15}$ cm$^{-3}$ and $5 \cdot 10^{17}$ cm$^{-3}$, in the temperature range from 300 K till 500 K, further validation of the developed model is required for a broader range of doping concentrations and temperatures.

To understand the different dominant scattering mechanisms in the channel of SiC MOSFETs with high and low $N_A$, the Hall-effect measurements have been analyzed. To interpret the Hall-effect measurements in a range of temperatures, the Hall factor for the electron transport in the channel of SiC MOSFETs was calculated as a function of temperature. The results of the calculation are presented in Fig. 59 for the MOSFETs #E1 and #E2, respectively. Therein, it can be seen that the values of the Hall factor depend not only on gate voltage and background doping concentration but also on temperature. The behavior of the Hall factor with temperature reflects the changes of the relative contributions of the scattering mechanisms. As it is shown in Fig. 59, with an increase in temperature, the Hall factor in the channel of SiC MOSFETs strongly decreases for both background doping concentrations.

Fig. 59: Temperature dependence of the Hall factor in the channel of SiC MOSFET #E1 with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$ (left) [VU4] and of the MOSFET #E2 with $N_A = 1 \cdot 10^{15}$ cm$^{-3}$ (right).
Chapter 6 Simulation Results and Discussions

Taking the temperature dependence of the Hall factor into account and using Eq. (8) and Eq. (9), the sheet carrier density and the drift mobility were determined from the Hall-effect measurements. In Fig. 60 and Fig. 61, the respective values are compared with numerical simulations. The simulated values of the sheet carrier density and the drift mobility were derived from the simulations of the current-voltage characteristics shown in Fig. 53. All the calculations have been done in analogy to the ones performed at room temperature.

Fig. 60: Temperature dependence of the simulated (lines) and measured (symbols) sheet carrier density in n-channel SiC MOSFETs #E1 (left) [VU4] and #E2 (right).

Fig. 61: Temperature dependence of the simulated (lines) and measured (symbols) drift mobility in n-channel SiC MOSFETs #E1 (left) [VU4] and #E2 (right).
In Fig. 60 and Fig. 61 it can be seen that the simulations are in quite good agreement with the corrected Hall-effect measurements. The existence of some deviations between the simulated and measured results can be explained by inaccuracies in the relative contributions of the scattering mechanisms to the channel mobility. However, the results obtained confirm that the simulation methodology developed in the current work and applied for the interpretation of the measurements can consistently describe the temperature dependence as well as the doping dependence of the electrical characteristics of n-channel SiC MOSFETs.

The results of the Hall-effect measurements and simulations reveal that the sheet carrier density in the channel of SiC MOSFETs increases with increasing temperature for the studied doping concentrations. The increase in the sheet carrier density with temperature can be explained by the decrease in the amount of charged traps with increasing temperature due to the decrease in the bulk potential. In contrast to the sheet carrier density, the mobility in the channel of MOSFETs with different NA obtained by the Hall-effect measurements has different temperature dependences. In Fig. 61 it can be seen that at high doping concentrations the channel mobility increases in the studied temperature range with increasing temperature while it decreases at low doping concentrations. To understand the different temperature dependences, the mobility components have been analyzed at different temperatures for both doping concentrations NA. To calculate the temperature dependence of the mobility components, the method of small variation described in Section 6.2 was applied. It should be noted that calculations of the temperature dependence of the mobility components give the opportunity to determine the effect of temperature on each of the mechanisms by which electrons are scattered. The results of the calculation of the mobility components as a function of gate voltage at 300 K and 400 K for the MOSFETs #E1 and #E2 are shown in Fig. 62. It should be noted that the mobility component associated with surface-roughness scattering is not shown because of its insignificant contribution to the channel mobility with temperature.
Chapter 6 Simulation Results and Discussions

Fig. 62: Mobility components associated with Coulomb scattering at the interface charges ($\mu_C$), surface-phonon ($\mu_{SP}$) and bulk-phonon ($\mu_{BP}$) scattering at 300 K and 400 K for the MOSFETs with $N_A$ equal to $5 \cdot 10^{17}$ cm$^{-3}$ and $1 \cdot 10^{15}$ cm$^{-3}$.

In Sections 6.2 and 6.3 it was shown that Coulomb scattering at the interface charges is the dominant scattering mechanism at room temperature in the channel of SiC MOSFETs for all studied doping concentrations $N_A$. It is well known that with increasing temperature Coulomb scattering at the interface charges decreases. This effect is reflected in the increase of the respective mobility component with an increase in temperature seen in Fig. 62. The reduction of Coulomb scattering at the interface charges can be mainly explained by two coupled effects. The first one is a decrease in the amount of charged traps due to the change of the bulk potential with
temperature. The second one is an increase in screening of scattering centers due to the increase of the number of free electrons in the inversion channel. In contrast to Coulomb scattering, surface-phonon and bulk-phonon scattering increase with an increase in temperature. As a consequence, the mobility components associated with the aforementioned scattering mechanisms decrease, as it is shown in Fig. 62. Comparing the total mobilities for the MOSFETs #E1 and #E2, presented in Fig. 61, with the respective mobility components, the different temperature dependence of the drain currents and channel mobilities can be explained as following. The mobility component associated with surface-phonon scattering at high gate voltages has the same order of magnitude in the MOSFETs #E1 and #E2. Bulk-phonon scattering, as it was mentioned above, is assumed to be independent of \( N_A \) and increases equally with increasing temperature in both MOSFETs. However, the mobility component associated with Coulomb scattering at the interface charges is on average by a factor of 10 higher in the MOSFET #E2 than in the MOSFET #E1. This means that in the MOSFET #E1 Coulomb scattering at the interface charges is much stronger than in the MOSFET #E2, which is reflected in the lower channel mobility, seen in Fig. 61. Moreover, Coulomb scattering at the interface charges is so strong in the MOSFET #E1 that the contributions of surface-phonon scattering as well as bulk-phonon scattering to the channel mobility are negligible even at 400 K. This means that for the temperature dependence of the SiC MOSFET characteristics with high \( N_A \), at least in the temperature range from 300 K till 400 K, only Coulomb scattering at the interface charges plays a fundamental role. Considering that Coulomb scattering decreases with an increase in temperature, the channel mobility increases and, as a consequence, the drain current also increases. In case of the MOSFET #E2, where Coulomb scattering at the interface charges is relatively low even at 300 K, an increase of temperature leads to the effect that the contributions of surface-phonon as well as bulk-phonon scattering become significant. Considering that the temperature dependence of bulk-phonon scattering is stronger than the temperature dependence of surface-phonon scattering, \( \mu_{BP} \) decreases with increasing temperature faster and starts to dominate at high temperature. This results in the reduction of the channel mobility as well as the drain current.
Chapter 7  Conclusions and Outlook

One of the major challenges in the simulation of lateral SiC MOSFETs is a description of the SiC/SiO$_2$ interface. Simulation with ideal interfaces, i.e. without interface charges, is insufficient and can not describe the behavior of SiC devices. The high density of the interface traps $D_{IT}(E_T)$ limits the performance of SiC MOSFETs by degradation of the channel mobility and needs to be accurately characterized in simulations. The aim of this research activity was to understand the mechanisms which control the channel mobility of lateral 4H-SiC MOSFETs and to develop a self-consistent simulation methodology which can describe the electrical behavior of SiC field-effect transistors.

In the framework of the MobiSiC (Mobility Engineering for SiC Devices) project lateral n-channel 4H-SiC MOSFETs have been fabricated by the team and characterized electrically by current-voltage and Hall-effect measurements. The effects of temperature and bulk potential engineering upon the transport properties in the channel of SiC MOSFETs have been studied. In this work, to understand and explain the electrical measurements, numerical simulations have been performed with Sentaurus Device of Synopsys. In a first step a simulation methodology has been developed on the basis of the MOSFET with the highest background doping concentration. In a second step, the simulation methodology has been validated by the reproduction of the temperature and doping dependences of the electrical characteristics of SiC MOSFETs.

For the simulation of SiC MOSFETs, where charge at the SiC/SiO$_2$ interface is the most crucial parameter, the models for Near-Interface Traps (NIT) and mobility degradation are of primary
importance. In this work, for an accurate description of the interface defects the NIT model was developed on the basis of the $D_{IT}(E_T)$ distributions extracted from the electrical measurements and optimized by numerical simulations to reproduce the current-voltage characteristics as well as the sheet carrier densities and channel mobilities obtained from Hall-effect measurements. It was found that the NIT model, which usually includes only traps related to the oxidation of SiC and assumed to be acceptors, can be extended. It was shown that two kinds of traps, donors and acceptors, both energetically located near the conduction band of SiC, affect the electrical characteristics of SiC MOSFETs and have to be taken into account. The origin of the donor traps has been suggested to be related to nitrogen impurities incorporated during oxidation and annealing in nitrogen-containing atmosphere.

For a more accurate simulation of the channel mobility, obtained from the Hall-effect measurements, and the interpretation of its degradation mechanisms, the Hall factor for the electron transport in the channel of SiC MOSFETs was evaluated for the first time. The method of the Hall factor calculation, developed in this work, is based on the interdependence with mobility components via the respective scattering relaxation times. The new method allows an accurate determination of mobility and sheet carrier density from Hall-effect measurements. To demonstrate the general applicability of the method, it was used to predict the dependence of the Hall factor on dopant concentration in silicon which was then compared with measured Hall factors reported in the literature.

The simulation methodology applied in the current work for the interpretation of the measurements can consistently describe the temperature dependence as well as the doping dependence of the electrical characteristics of n-channel 4H-SiC MOSFETs. The simulation results allow to conclude that the main reason for the low performance of SiC MOSFETs is the scattering of electrons in the channel. Independently of the background doping concentration, Coulomb scattering at the interface charges is the dominant scattering mechanism at room temperature. With increasing temperature Coulomb scattering at the interface charges decreases which leads to an increase of the channel mobility and the corresponding drain current. However,
phonon scattering increases with increasing temperature. When the contributions from Coulomb and phonon scattering mechanisms become comparable at high temperatures, the channel mobility decreases with increasing temperature. In this work, it was found that the temperature dependence of the electrical characteristics of 4H-SiC MOSFETs depends on the doping concentration: For highly doped MOSFETs, the channel mobility increases with increasing temperature while it decreases for lowly doped ones. To reproduce the electrical measurements for the MOSFETs with low and high background doping concentrations at elevated temperatures, a new model for the mobility in the bulk has been developed and implemented via the “Physical Model Interface” of Sentaurus Device. It was found that the conventional model of bulk-phonon scattering can not reproduce the temperature dependence of the MOSFETs with low background doping concentration. Based on the simulation analysis performed, the contribution from bulk-phonon scattering has to be on the average by a factor of two higher than it is predicted by the conventional model. However, further experimental work, i.e. broader ranges of temperatures and doping concentrations, is required to confirm the validity of the newly proposed model.

Considering that at room temperature Coulomb scattering at the interface charges is the dominant scattering mechanism, its impact has to be reduced to improve the channel mobility. The intensity of Coulomb scattering at the interface charges depends on the amount of traps which are occupied and charged. Assuming the presence of acceptor-like traps, one of the strategies to decrease Coulomb scattering at the interface charges is to decrease the amount of charged interface traps by decreasing the background doping concentration. The study of this effect in the current work showed that the explanation of the improvement of the channel mobility with decreasing background doping concentration needs a broader view than it is usually presented in literature. One of the effects which have to be taken into account is a widening of the inversion channel with a decrease of the doping concentration. Considering that the impact of the interface traps decreases when moving from the interface to the bulk of SiC, the widening of the inversion layer results in an increase of the channel mobility. This means that a change of the thickness of the inversion layer affects the channel mobility.
Based on the simulations performed it was found that the model currently implemented in Sentaurus Device for the mobility component associated with Coulomb scattering at the interface charges can not adequately describe the depth dependence of the mobility. Thus, simulating the doping dependence of the electrical measurements for SiC MOSFETs, the model has been artificially calibrated for each studied doping concentration. However, the effect that the mobility depends on the distance from the interface, and that it changes with doping concentration is very important. Thus, new models for mobility, which can accurately describe the aforementioned effect, have to be developed and implemented in simulation software.

Summing up, using Sentaurus Device of Synopsys the electrical measurements performed for lateral n-channel 4H-SiC MOSFETs at different temperatures and background doping concentrations have been analyzed and well described using the developed simulation methodology. The numerical simulations performed are based on silicon models for which the parameter set has been calibrated. However, to use simulation software as a tool which can predict the behavior of SiC devices, in particular SiC MOSFETs, simulation models have to be improved.
Acknowledgement

I would like to express my deep gratitude to all those who gave me the possibility to perform this work and helped me during this time. First of all, I would like to thank my supervisor PD Dr. Peter Pichler for the patient guidance of my thesis and his support.

Special thanks go to Dr. Alex Burenkov for his supervising, support and advices during this time. Without his help it would have been difficult for me successfully to complete this work.

I would like also to thank all colleagues with whom I have been working on the MobiSiC project: Dr. Christian Strenger, Dr. Anton Bauer, Dr. Vincent Mortet, Dr. Elena Bedel-Pereira, Dr. Guillermo Ortiz and Dr. Cristiano Fuccio.

Big thanks go to Dr. Jürgen Lorenz for giving me the chance to work in the department Simulation at Fraunhofer IISB and his support.

I would like also to thank all colleagues at Fraunhofer IISB for the warm and friendly atmosphere during this time.

Last but not least, many thanks go to my family and my friends for their love, support and consideration.
References


[17] F. Devynck, "First-principles study of defects at the SiC/SiO₂ interface through hybrid


[34] Y.P Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*,
References


[51] D. Stefanakis and K. Zekentes, "TCAD models of the temperature and doping dependence of the bandgap and low field carrier mobility in 4H-SiC," *Microelectronic Engineering*,
References


References


References


Thesis Publications


List of Figures

Fig. 1 Schematic representation of the abilities of device simulation and modeling. ............... 5
Fig. 2 Diagram with the setup of device simulation. .................................................................
Fig. 3 Top view of the Hall-Bar structure [31]. ...................................................................... 15
Fig. 4 Schematic representation of Fermi-Dirac distribution. .................................................. 18
Fig. 5 Bandgap energy of 4H-SiC as a function of temperature .................................................. 20
Fig. 6 Comparison of the percentage of the ionized Al atoms calculated with and without the
inclusion of doping dependence of the ionization energy. ......................................................... 22
Fig. 7 Percentage of ionized Al atoms as a function of temperature for different doping
concentrations in bulk-SiC ........................................................................................................ 23
Fig. 8 Ionized doping concentration as a function of depth at different gate voltages applied to n-
channel SiC MOSFET with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$ .................................................................. 24
Fig. 9 Ionized doping concentration as a function of depth at $V_G = 0$ V applied to n-channel SiC
MOSFET with $N_A = 5 \cdot 10^{17}$ cm$^{-3}$ and different concentrations $Q_F$ of fixed charge ............... 25
Fig. 10 Oxide and interface charges in thermally grown SiO$_2$ [41]. ........................................ 27
Fig. 11 Change of charge state of traps in dependence on the Fermi level. .............................. 28
Fig. 12 Impact of acceptor traps on the current-voltage characteristics of SiC MOSFETs. The
acceptor traps have been simulated with a concentration of $2 \cdot 10^{12}$ cm$^{-2}$ and a level of 50 meV
below $E_C$ .................................................................................................................................... 29
Fig. 13 Impact of positive fixed charges (left) and donor traps (right) on the current-voltage
characteristics of SiC MOSFET. The donor traps have been simulated with a concentration of
$2 \cdot 10^{12}$ cm$^{-2}$ and a level of 50 meV below $E_C$ ......................................................................... 30
Fig. 14 Acceptor trap distributions modeled with $D_{IT}^{mid} = 2.4 \times 10^{11}$ cm$^{-2}$eV$^{-1}$, $D_{IT}^{edge} = 4.6 \times 10^{13}$ cm$^{-2}$eV$^{-1}$. The parameter $\sigma$ was varied as 0.047 eV, 0.067 eV, 0.087 eV. 

Fig. 15 Diagram of optimization for density of the interface traps $D_{IT}(E_T)$ extracted from Hall-effect and capacitance-voltage measurements. 

Fig. 16 $D_{IT}(E_T)$ distributions used in the simulations of the studied MOSFETs. 

Fig. 17 Illustration of the method of $D_{IT}(E_T)$ extraction from Hall-effect measurements. The figure is adjusted from reference [46]. 

Fig. 18 Interface trap density extracted from Hall-effect measurements. The Hall factor $r_H$ was assumed to be unity in the calculation. 

Fig. 19 Influence of Hall factor on the energetic profile of interface trap density extracted from the Hall-effect measurements. 

Fig. 20 Capacitor circuit of MOS capacitor with the interface traps. The figure is adjusted from [62]. 

Fig. 21 Capacitance circuits at low (left) and high (right) frequencies. The figure is adjusted from [62]. 

Fig. 22 Interface trap density extracted by the high-low frequency method. 

Fig. 23 Interface trap density extracted from C-V and Hall-effect measurements. 

Fig. 24 Bulk mobility as a function of phosphorus concentration [VU1]. 

Fig. 25 Dependence of the power index $s$ for Coulomb scattering on dopant density including screening [VU1]. 

Fig. 26 Hall factor for electrons against phosphorus doping concentration in silicon [VU1]. 

Fig. 27 Comparison of default simulations and measurements for the MOSFET #E1. 

Fig. 28 Nitrogen profile measured by secondary ion mass spectroscopy. 

Fig. 29 Comparison between the simulated and measured current-voltage characteristics. The simulations have been performed assuming an ideal interface (solid line) and with the NIT but without mobility degradation models (dashed line). 

Fig. 30 Simulated nitrogen profile resulting in the “Nitrogen distribution” $I_D(V_G)$ curve shown in Fig. 31.
Fig. 31 Comparison of the current-voltage characteristics simulated either with the donor trap level or with a nitrogen profile ................................................................. 71
Fig. 32 Donor trap density as a function of trap energy calculated for the nitrogen profile shown in Fig. 30 .................................................................................................................. 72
Fig. 33 Comparison of the drain currents simulated with a single donor trap level, with a nitrogen profile or with a band of donor traps .......................................................................................... 73
Fig. 34 Comparison of current-voltage characteristics simulated with NIT and mobility degradation models with the measurements for the MOSFET #E1 .................................................. 74
Fig. 35 Comparison of the total mobility in the channel of the MOSFET #E1 calculated from the simulated current-voltage measurements and from the mobility components using Matthiessen’s rule. The mobility components have been obtained using the method of small variations. ........ 79
Fig. 36 Inverse mobility components in comparison to the inverse total mobility for the MOSFET #E1 ................................................................................................................................. 80
Fig. 37 Hall factor as a function of gate voltage in the channel of the MOSFET #E1 [VU2]. .... 81
Fig. 38 Mobility components associated with Coulomb scattering at the interface charges and surface-roughness scattering in comparison to the total mobility for the MOSFET #E1........... 82
Fig. 39 Sheet carrier density as a function of gate voltage in the channel of MOSFET #E1...... 83
Fig. 40 Drift mobility as a function of gate voltage in the channel of MOSFET #E1.............. 83
Fig. 41 Comparison of the simulated (lines) and measured (symbols) current-voltage characteristics [VU3] .......................................................................................................................... 86
Fig. 42 Hall factor in the channel of SiC MOSFETs with different background doping concentrations [VU3] .................................................................................................................. 86
Fig. 43 Doping dependence of the simulated (lines) and measured (symbols) sheet carrier density. ............................................................................................................................... 87
Fig. 44 Doping dependence of the simulated (lines) and measured (symbols) drift mobility..... 87
Fig. 45 Comparison of the $D_{IT}(E_T)$ distributions used in the simulations of the MOSFETs #E2, #W1 and #W2 and the $D_{IT}(E_T)$ distribution extracted from C-V measurements. ....................... 88
Fig. 46 Density of traps obtained by averaging of the $D_{IT}(E_T)$ distributions, shown in Fig. 45. . 90
Fig. 47 Sheet carrier density for the MOSFETs with different $N_A$ simulated with the assumption of an ideal interface (left) and with the averaged $D_{IT}(E_T)$ distribution (right)............................. 90

Fig. 48 Band diagram with the traps located at the interface and in the depletion width [92].... 91

Fig. 49 Effective channel thickness for n-channel MOSFETs with different backround doping concentrations. ........................................................................................................ 93

Fig. 50 Band diagrams for n-channel MOSFETs with a) $N_A = 5 \cdot 10^{16} \text{ cm}^{-3}$ b) $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$ and c) $N_A = 1 \cdot 10^{15} \text{ cm}^{-3}$ [VU3]. .................................................................................................................. 94

Fig. 51 Mobility components in the channel of 4H-SiC MOSFETs with a) $N_A = 5 \cdot 10^{16} \text{ cm}^{-3}$ b) $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$ c) $N_A = 1 \cdot 10^{15} \text{ cm}^{-3}$ ............................................................................................................................... 97

Fig. 52 Mobility component associated with Coulomb scattering at the interface ($\mu_C$) in the channel of SiC MOSFETs with different background doping concentrations. ..................... 98

Fig. 53 Current-voltage characteristics for the MOSFETs #E1 (left) [VU4] and for the MOSFET #E2 (right). Lines represent the simulations, symbols measurements..................................... 100

Fig. 54 Current-voltage characteristics of the MOSFET #E2, simulated with the conventional model for $\mu_B$ (lines) in comparison to the measurements (symbols)................................. 102

Fig. 55 Current-voltage characteristics of the MOSFET #E2, simulated with the conventional model for $\mu_B$ at 500 K, 600 K and 700 K.................................................................................. 102

Fig. 56 Comparison of the mobility component associated with bulk-phonon scattering calculated using the conventional and new models. ................................................................. 103

Fig. 57 Mobility component associated with Coulomb scattering at the ionized impurities, calculated from the conventional model................................................................. 105

Fig. 58 Mobility components associated with Coulomb scattering at the ionized impurities ($\mu_{IMP}$) and bulk-phonon scattering ($\mu_{BP}$), calculated using the new model............................... 106

Fig. 59 Temperature dependence of the Hall factor in the channel of SiC MOSFET #E1 with $N_A = 5 \cdot 10^{17} \text{ cm}^{-3}$ (left) [VU4] and of the MOSFET #E2 with $N_A = 1 \cdot 10^{15} \text{ cm}^{-3}$ (right). ............ 107

Fig. 60 Temperature dependence of the simulated (lines) and measured (symbols) sheet carrier density in n-channel SiC MOSFETs #E1 (left) [VU4] and #E2 (right). ................................. 108
List of Figures

Fig. 61 Temperature dependence of the simulated (lines) and measured (symbols) drift mobility in n-channel SiC MOSFETs #E1 (left) [VU4] and #E2 (right). ................................................................. 108

Fig. 62 Mobility components associated with Coulomb scattering at the interface charges ($\mu_C$), surface-phonon ($\mu_{SP}$) and bulk-phonon ($\mu_{BP}$) scattering at 300 K and 400 K for the MOSFETs with $N_A$ equal to $5 \cdot 10^{17}$ cm$^{-3}$ and $1 \cdot 10^{15}$ cm$^{-3}$. ........................................................................................................ 110
List of Tables

Table 1. Material properties of 4H-SiC and Si [1]................................................................................. 2
Table 2. Doping concentrations and oxide thicknesses for the investigated MOSFETs .............. 14
Table 3. Concentration of fixed charge used in the simulations......................................................... 35
Table 4. Parameter values for bulk mobility component ($\mu_B$) ......................................................... 37
Table 5. Parameter values of $n_{trans}$ adjusted in the model for Coulomb scattering at the interface charges .......................................................................................................................... 38
Table 6. Parameter values for the surface-roughness mobility component ($\mu_{SR}$) ....................... 39
Table 7. Parameter values for the surface-phonon mobility component ($\mu_{SP}$) ......................... 40
Table 8. Parameterization of the extended NIT models used in the simulations......................... 70
## List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B$</td>
<td>Magnetic field</td>
<td>T</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>Gate oxide capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_D$</td>
<td>Capacitance of depletion width</td>
<td>F</td>
</tr>
<tr>
<td>$D_n$</td>
<td>Electron diffusion coefficient</td>
<td>cm²/s</td>
</tr>
<tr>
<td>$D_p$</td>
<td>Hole diffusion coefficient</td>
<td>cm²/s</td>
</tr>
<tr>
<td>$E$</td>
<td>Energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_A$</td>
<td>Ionization energy for acceptor impurity</td>
<td>eV</td>
</tr>
<tr>
<td>$E_D$</td>
<td>Ionization energy for donor impurity</td>
<td>eV</td>
</tr>
<tr>
<td>$E_C$</td>
<td>Conduction band energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_G$</td>
<td>Bandgap energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_T$</td>
<td>Trap energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_V$</td>
<td>Valence band energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_F$</td>
<td>Fermi energy</td>
<td>eV</td>
</tr>
<tr>
<td>$E_{F,n}$</td>
<td>Quasi-Fermi energy for electrons</td>
<td>eV</td>
</tr>
<tr>
<td>$E_{F,p}$</td>
<td>Quasi-Fermi energy for holes</td>
<td>eV</td>
</tr>
<tr>
<td>$\mathcal{E}$</td>
<td>Electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>$\mathcal{E}_{EFF}$</td>
<td>Effective electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>$\mathcal{E}_\parallel$</td>
<td>Normal electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>$\hbar$</td>
<td>Dirac constant</td>
<td>Js</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current</td>
<td>A</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
<td>--------------</td>
</tr>
<tr>
<td>$J_n$</td>
<td>Electron current density</td>
<td>A/cm$^2$</td>
</tr>
<tr>
<td>$J_p$</td>
<td>Hole current density</td>
<td>A/cm$^2$</td>
</tr>
<tr>
<td>$k_B$</td>
<td>Boltzmann constant</td>
<td>J/K</td>
</tr>
<tr>
<td>$L$</td>
<td>Channel length</td>
<td>$\mu$m</td>
</tr>
<tr>
<td>$m_e^*$</td>
<td>Effective electron mass</td>
<td>kg</td>
</tr>
<tr>
<td>$m_\perp$</td>
<td>Electron mass perpendicular to the oxide/semiconductor interface</td>
<td>kg</td>
</tr>
<tr>
<td>$N_A$</td>
<td>Acceptor concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_C$</td>
<td>Effective density of states in conduction band</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_D$</td>
<td>Donor concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_{tot}$</td>
<td>Total doping concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_V$</td>
<td>Effective density of states in valence band</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$n$</td>
<td>Electron concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic charge carrier concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$n_{inv}$</td>
<td>Sheet carrier density in inversion channel</td>
<td>cm$^{-2}$</td>
</tr>
<tr>
<td>$p$</td>
<td>Hole concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$Q_F$</td>
<td>Fixed charge</td>
<td>charge/cm$^2$</td>
</tr>
<tr>
<td>$Q_{IT}$</td>
<td>Charge of interface traps</td>
<td>charge/cm$^2$</td>
</tr>
<tr>
<td>$Q_S$</td>
<td>Space charge</td>
<td>charge/cm$^2$</td>
</tr>
<tr>
<td>$q$</td>
<td>Elementary charge</td>
<td>C</td>
</tr>
<tr>
<td>$r_H$</td>
<td>Hall factor</td>
<td></td>
</tr>
<tr>
<td>$T$</td>
<td>Absolute temperature</td>
<td>K</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Drain voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_G$</td>
<td>Gate voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_H$</td>
<td>Hall-effect voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage</td>
<td>V</td>
</tr>
<tr>
<td>$W$</td>
<td>Channel width</td>
<td>$\mu$m</td>
</tr>
<tr>
<td>$x_D$</td>
<td>Depletion width</td>
<td>$\mu$m</td>
</tr>
</tbody>
</table>
### List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_{AV}$</td>
<td>Average thickness of channel</td>
<td>$\mu$m or nm</td>
</tr>
<tr>
<td>$\varepsilon_S$</td>
<td>Dielectric constant of semiconductor</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Relaxation scattering time</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{BP}$</td>
<td>Relaxation scattering time associated with bulk-phonon scattering</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_C$</td>
<td>Relaxation scattering time associated with Coulomb scattering at the interface charges</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{IMP}$</td>
<td>Relaxation scattering time associated with Coulomb scattering at the ionized impurities</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{SP}$</td>
<td>Relaxation scattering time associated with surface-phonon scattering</td>
<td>s</td>
</tr>
<tr>
<td>$\tau_{SR}$</td>
<td>Relaxation scattering time associated with surface-roughness scattering</td>
<td>s</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Channel mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_B$</td>
<td>Mobility in the bulk</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{BP}$</td>
<td>Mobility associated with bulk-phonon scattering</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_C$</td>
<td>Mobility associated with Coulomb scattering at the interface charges</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{EFF}$</td>
<td>Effective mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{FE}$</td>
<td>Field-effect mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_H$</td>
<td>Hall-effect mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{IMP}$</td>
<td>Mobility associated with Coulomb scattering at ionized impurity scattering</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_p$</td>
<td>Hole mobility</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{SP}$</td>
<td>Mobility associated with surface-phonon scattering</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\mu_{SR}$</td>
<td>Mobility associated with surface-roughness scattering</td>
<td>cm$^2$/Vs</td>
</tr>
<tr>
<td>$\rho_{trap}$</td>
<td>Density of surface charges</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$\chi$</td>
<td>Electron affinity</td>
<td>V</td>
</tr>
<tr>
<td>$\psi$</td>
<td>Electrostatic potential</td>
<td>V</td>
</tr>
<tr>
<td>$\psi_B$</td>
<td>Bulk potential</td>
<td>V</td>
</tr>
<tr>
<td>$\psi_S$</td>
<td>Band bending at the surface</td>
<td>V</td>
</tr>
</tbody>
</table>
# Index

A


B

Band-bending .................. 42, 47, 50, 84
Bandgap energy ............... 6, 19, 20
Bulk potential .......... 10, 42, 84, 93, 99, 100
Bulk traps .................. 91, 92, 95, 96, 98

D

Debye length .................. 42, 43
Depletion width .......... 91, 93, 95, 96
Device simulation ............. 4, 11, 17, 20
Diffusion coefficients .......... 13
Donor traps ...... 28, 30, 66, 68, 69, 71, 75, 85

E

Effective field .................. 92
Effective mobility ............. 75, 76
Effective thickness of channel .......... 92
Electrostatic potential .......... 12

F

Fermi integral .................. 19
Fermi level .................. 18, 23, 28, 30, 41, 47
Fermi-Dirac statistic .......... 9, 18, 19, 47
Field-effect mobility .......... 7, 8, 75, 76
Fixed charge .... 25, 27, 30, 35, 43, 68, 69, 75

H

Hall factor ...... 15, 33, 46, 55, 56, 59, 60, 61, 64, 76, 81, 86, 107, 108
Hall mass factor .......... 59, 60, 81
Hall-Barrier structures ........ 14, 15
High-low frequency method .... 47, 48, 50

I

Incomplete ionization .......... 9, 21, 23, 26
Interface trapped charges .... 27, 31, 41, 43
ITRS ............................. 4

M

Matthiessen’s rule .... 36, 78, 79, 80, 104
Mobile ion charges .................. 26
Mobility degradation... 9, 67, 70, 74, 85, 100
<table>
<thead>
<tr>
<th>Mott transition</th>
<th>62</th>
</tr>
</thead>
<tbody>
<tr>
<td>Newton’s iterative method</td>
<td>13</td>
</tr>
<tr>
<td>NIT model</td>
<td>31, 32, 68, 69, 70, 74, 85</td>
</tr>
<tr>
<td>Nitridation</td>
<td>3, 7, 65, 66, 75</td>
</tr>
<tr>
<td>Nitrogen distribution</td>
<td>69, 72, 73</td>
</tr>
<tr>
<td>NITs</td>
<td>6, 7, 27, 32</td>
</tr>
<tr>
<td>Numerical optimization</td>
<td>32, 33</td>
</tr>
<tr>
<td>Oxide trapped charges</td>
<td>27</td>
</tr>
<tr>
<td>Poisson equation</td>
<td>12</td>
</tr>
</tbody>
</table>

**S**
- Scattering relaxation time | 76, 77 |
- SIMS | 68, 69 |
- Step-controlled epitaxy | 38 |

**T**
- TCAD | 4, 5, 6, 60, 77, 78 |
- Threshold voltage | 8, 26, 29, 30, 67, 70, 72 |

**W**
- WBG semiconductors | 1, 2 |