The main and diversity antennas of modern cellular user equipment are integrated into the chassis of the device. Due to the limited space inside the device and high complexity of front-end electronics, the integrated antennas have small form factor, which leads to low radiation efficiency and high mismatch losses. The performance of the antennas is optimized with aperture tuning techniques. Commercial aperture tuners in modern cellular user equipment are based on high-voltage RF switches in bulk- or SOI-CMOS technologies. The focus of this research is put on the analysis of the second and third order nonlinear products caused by the RF switch, the influence of the substrate capacitance and the hardware characterization of antenna tuning ICs. Additionally, the functionality of the RF switch is extended and novel RF switch-based tuning ICs in CMOS technologies are investigated. All theoretical findings are verified either with measurements of the designed ICs or on the application level using a hardware demonstrator.
Oguzhan Özdamar

High-Voltage RF Switch-Based Antenna Tuning Circuits in CMOS Technologies
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Erlangen
FAU University Press
2022
High-Voltage RF Switch-Based Antenna Tuning
Circuits in CMOS Technologies

Hochvolt-HF-Schalter für Antennen-
abstimmschaltungen in CMOS-Technologien

Der Technischen Fakultät
der Friedrich-Alexander-Universität
Erlangen-Nürnberg

zur
Erlangung des Doktorgrades

DOKTOR-INGENIEUR

vorgelegt von

Oguzhan Özdamar, M.Sc.

aus Fürth
Als Dissertation genehmigt
von der Technischen Fakultät
der Friedrich-Alexander-Universität Erlangen-Nürnberg

Tag der mündlichen
Prüfung: 09.05.2022

Gutachter: Prof. Dr.-Ing. Dr.-Ing. habil. Robert Weigel
           Univ.-Prof. Dr.-Ing. Thomas Ußmüller
Acknowledgements

First of all, I would like to express sincere appreciation to Prof. Dr.-Ing. Dr.-Ing. habil. Robert Weigel for providing me the opportunity to perform my doctoral research at the Institute for Electronics Engineering, University of Erlangen-Nuremberg.
I am extremely grateful to my supervisor Dr. Valentyn Solomko from Infineon Technologies AG for his invaluable advice, continuous support and patience during my research work. Without his advice and guidance this thesis would have never been accomplished. I would like to thank him very much for his support over the past three years.
Also, I would like to express my thanks to Prof. Dr.-Ing. Amelie Hagelauer for her valuable support throughout the study. I would also like to show gratitude to Dr. Jochen Eßel, Danial Tayari, Pablo Nascimento, Dr. Johannes Rimmelspacher, Dr. Matthias Völkel, Dr. Kun Wang and Michael Mürke for their fruitful discussions, support and help during my PhD.
I would also like to thank my personal friends Emre, Erdem, Harun and Mikail who provided their support whenever needed.
Finally, I am especially indebted to my mother Esin, father Ali and sister Aysegül for their indefatigable faith and support throughout my life. And last but not least, I am extremely grateful to my beloved wife Esra for her endless support and love during my research work. Without my family, it would be impossible for me to complete my study.
Abstract

Due to esthetic considerations the antennas of modern cellular user equipment are integrated into the housing of the device. Since the space inside the device is limited, the electrical length of the antennas is short, which leads to low radiation efficiency and high mismatch of the intrinsic antenna. To overcome such constraints, aperture tuning is required to improve the efficiency of the intrinsic antenna. In addition, aperture tuning techniques substantially improve the bandwidth of the antenna by tuning it to various frequencies, thus fulfilling the requirements for frequency coverage of modern cellular standards. Aperture tuning in modern cellular user equipment is typically performed with high-voltage high-linear RF switches.

The research focuses on the analysis of second and third order nonlinear products caused by the RF switch, the influence of the substrate capacitance, the hardware characterization of the antenna tuning integrated circuits (ICs), extending the functionality of the RF switch, improving the performance of the antenna tuning system by application of co-design and investigating novel RF switch-based tuning ICs in complementary metal-oxide semiconductor (CMOS) technology.

The novel aspects of this work include:

1. Proposing a substrate capacitance model for metal oxide semiconductor field effect transistor (MOSFET) based RF switches on high-ohmic silicon substrates. The capacitance is calculated by applying microstrip line computation models. The analytical findings are verified with a prototype switch IC fabricated in a dedicated 130 nm bulk-CMOS technology.

2. Providing an analytical description of the nonlinearities in shunt aperture tuning RF switches operating in off-state. The focus is put on the analysis of second- and third-order nonlinear products and their power distribution as a function of geometry of the high-voltage MOSFET-based RF switches. The model-to-hardware correlation is presented with measurements for which two ICs were designed and manufactured in a dedicated 130 nm RF switch technology.

3. Demonstrating a method for the accurate measurement of the off-state shunt capacitance and the equivalent off-resistance of the antenna tuning RF switch IC assembled on a printed-circuit-board (PCB). For the extraction of the above parameters an empty (open) instance of the test
fixture on which the DUT is populated is measured and included into the de-embedding procedure. The proposed approach helps to improve the accuracy, repeatability, and reproducibility of the measurements.

4. A hardware demonstrator for rapid prototyping of antenna aperture tuning systems utilizing an inverted-F antenna (IFA), short, feed and aperture tuning network including the high-voltage RF switch is proposed. The demonstrator enables the measurements of the impedance at the feed and at the aperture tuning port as well as of harmonics. Using the demonstrator, an analysis of the harmonic distribution in the aperture-tuned IFA is provided. The analysis is based on a first-order transmission line model and allows identifying local minima for the second and third harmonics for a given use-case, which allows the minimization of the harmonic content generated by the tuning IC. The analytical findings are verified on a hardware demonstrator, comprising the reconfigurable IFA and RF switch-based aperture tuning network.

5. Extending the functionality of the switch by means of a voltage detector coupled to the sensed RF path of the RF switch. Voltage detectors are typically based on rectification circuits implemented in the art of charge pump circuits, which are intrinsically nonlinear. The challenge in this design is to reduce the harmonic feedback into the sensed RF path of the high-voltage RF switch. The reduction is achieved by adding linearization elements to the charge-pump-based rectifier. The detector is implemented and tested in hardware with two RF switches fabricated in a dedicated 130 nm RF switch technology. The target application for the detector is root mean square (RMS) voltage monitoring, which has been tested on the demonstrator.

6. Two novel RF switch-based tuning ICs are designed and manufactured in a dedicated 130 nm RF switch technology. One IC is designed for decoupling of multiple input multiple output (MIMO) antennas as well as for aperture and impedance tuning. The other IC is a monolithically integrated hybrid C-Tuner for antenna aperture tuning applications. The single C-Tuner design is capable of handling mid- and high-voltage classes in one single design. For both manufactured ICs, an application example on the hardware demonstrator is presented.
Kurzfassung

Aus ästhetischen Gründen sind die Antennen moderner zellularer Endgeräte im Gehäuse integriert. Aufgrund begrenzter Platzverhältnisse im Inneren des Geräts ist die elektrische Länge der Antenne klein, was zu einer geringen Strahlungseffizienz und einer hohen Fehlanpassung der intrinsischen Antenne führt. Die Effizienz der intrinsischen Antenne kann mittels Anpassung der Apertur verbessert werden. Darüber hinaus wird mit Hilfe von Anpassungstechniken die Bandbreite der Antenne, durch Abstimmung auf verschiedene Frequenzen, erheblich verbessert, sodass die Anforderung an die Frequenzabdeckung moderner Mobilfunkstandards erfüllt ist. Die Anpassung der Apertur in modernen Mobilfunkgeräten wird in der Regel mit hochlinearen Hochspannungs-HF-Schaltern realisiert.

Die Forschungsarbeit konzentriert sich auf die Analyse der durch den HF-Schalter verursachten Nichtlinearitäten erster sowie zweiter Ordnung, den Einfluss der Substratkapazität, die Hardware-Charakterisierung von Antennentuner-ICs, die funktionale Erweiterung des HF-Schalters, die Verbesserung der Perfomance des Antennentuning-Systems durch Co-Design-Anwendung und Implementierung neuartiger Antennentuner-ICs basierend auf HF-Schaltern in CMOS-Technologie.

Zu den neuen Aspekten dieser Arbeit gehören:


3. Die Demonstration einer Methode zur präzisen Messung der Off-Kapazität und des äquivalenten Off-Widerstands eines Antennentuner HF-


6. Die Entwicklung zweier neuartiger auf HF-Schalter-basierende Tuning-ICs, die in einer dedizierten 130 nm-HF-Switch-Technologie hergestellt worden sind. Einer der ICs ist für die Entkopplung von MIMO-Antennen sowie für die Apertur- und Impedanzanpassung konzipiert. Bei dem anderen IC handelt es sich um einen monolithisch integrierten hybriden C-Tuner für die Anwendung in Antennentunern. Der C-Tuner ist in der
Lage, Mittel- und Hochspannung in einem einzigen Design zu handhaben. Für beide hergestellten ICs wird jeweils ein Anwendungsbeispiel auf dem Hardware-Demonstrator vorgestellt.
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<th>Description</th>
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<tbody>
<tr>
<td>3GPP</td>
<td>Third generation partnership project</td>
</tr>
<tr>
<td>BEOL</td>
<td>Back-end-of-line</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried oxide</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass filter</td>
</tr>
<tr>
<td>BSIM</td>
<td>Berkeley short-channel IGFET model</td>
</tr>
<tr>
<td>BST</td>
<td>Barium strontium titanate</td>
</tr>
<tr>
<td>BTO</td>
<td>Barium titanate</td>
</tr>
<tr>
<td>CA</td>
<td>Carrier aggregation</td>
</tr>
<tr>
<td>CBRAM</td>
<td>Conductive-bridge random access memory</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide semiconductor</td>
</tr>
<tr>
<td>CPU</td>
<td>Central processing unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-analog converter</td>
</tr>
<tr>
<td>DMN</td>
<td>Decoupling and matching network</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic random access memory</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic discharge</td>
</tr>
<tr>
<td>FCV</td>
<td>Full-chip-verification</td>
</tr>
<tr>
<td>FEOL</td>
<td>Front-end-of-line</td>
</tr>
<tr>
<td>GeTe</td>
<td>Germanium telluride</td>
</tr>
<tr>
<td>GIDL</td>
<td>Gate-induced drain leakage</td>
</tr>
<tr>
<td>GISL</td>
<td>Gate-induced source leakage</td>
</tr>
<tr>
<td>GOX</td>
<td>Gate oxide</td>
</tr>
<tr>
<td>GPS</td>
<td>Global positioning system</td>
</tr>
<tr>
<td>GSM</td>
<td>Global system for mobile communications</td>
</tr>
<tr>
<td>GST</td>
<td>Germanium-antimony-telluride</td>
</tr>
<tr>
<td>HBM</td>
<td>Human body model</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>HR</td>
<td>High resistivity</td>
</tr>
<tr>
<td>HV</td>
<td>High-voltage handling tag</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>IFA</td>
<td>Inverted-F antenna</td>
</tr>
<tr>
<td>LDD</td>
<td>Lightly doped drain</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-pass-filter</td>
</tr>
<tr>
<td>LTE</td>
<td>Long term evolution</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro-electro-mechanical systems</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-insulator-metal</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multiple input multiple output</td>
</tr>
<tr>
<td>MN</td>
<td>Matching network</td>
</tr>
<tr>
<td>MOM</td>
<td>Metal-oxide-metal</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>MV</td>
<td>Mid-voltage handling tag</td>
</tr>
<tr>
<td>PA</td>
<td>Power amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed-circuit-board</td>
</tr>
<tr>
<td>PCM</td>
<td>Phase-change memory</td>
</tr>
<tr>
<td>PIFA</td>
<td>Planar inverted-F antenna</td>
</tr>
<tr>
<td>PSC</td>
<td>Parasitic surface conduction</td>
</tr>
<tr>
<td>PSP</td>
<td>Penn state philips</td>
</tr>
<tr>
<td>Radar</td>
<td>Radio detection and ranging</td>
</tr>
<tr>
<td>RAM</td>
<td>Random access memory</td>
</tr>
<tr>
<td>ReRAM</td>
<td>Resistive random access memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Silicon dioxide</td>
</tr>
<tr>
<td>SMA</td>
<td>Sub-miniature version A</td>
</tr>
<tr>
<td>SMD</td>
<td>Surface-mounted-device</td>
</tr>
</tbody>
</table>
# List of Symbols and Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMP</td>
<td>Sub-miniature push-on connector</td>
</tr>
<tr>
<td>SOG</td>
<td>Silicon-on-glass</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-on-insulator</td>
</tr>
<tr>
<td>SOL</td>
<td>Short-open-load</td>
</tr>
<tr>
<td>SP2T</td>
<td>Single pole two throw</td>
</tr>
<tr>
<td>SP4T</td>
<td>Single pole four throw</td>
</tr>
<tr>
<td>STI</td>
<td>Shallow trench isolation</td>
</tr>
<tr>
<td>STO</td>
<td>Strontium titanate</td>
</tr>
<tr>
<td>TDR</td>
<td>Time-domain reflectometry</td>
</tr>
<tr>
<td>TL</td>
<td>Thru-line</td>
</tr>
<tr>
<td>TRL</td>
<td>Thru-reflected-line</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal mobile telecommunication systems</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage controlled oscillators</td>
</tr>
</tbody>
</table>

# List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \alpha_2 )</td>
<td>Second-order nonlinear component of the first-order model of the nonlinear products</td>
</tr>
<tr>
<td>( \alpha_3 )</td>
<td>Third-order nonlinear component of the first-order model of the nonlinear products</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Propagation constant</td>
</tr>
<tr>
<td>( \beta_2 )</td>
<td>Second-order nonlinear component of the second-order model of the nonlinear products</td>
</tr>
<tr>
<td>( \beta_3 )</td>
<td>Third-order nonlinear component of the second-order model of the nonlinear products</td>
</tr>
<tr>
<td>( \epsilon_i )</td>
<td>Equalization error coefficient</td>
</tr>
<tr>
<td>( \epsilon_0 )</td>
<td>Permittivity of the vacuum ( \epsilon_0 = 8.854 ) ( \text{pF/m} )</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>-------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff}, \downarrow}$</td>
<td>Effective dielectric constant for flip-chip configuration</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff}, \uparrow}$</td>
<td>Effective dielectric constant for wire-bonded configuration</td>
</tr>
<tr>
<td>$\Gamma_0$</td>
<td>Reflection coefficient</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron mobility of the channel</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Scaling factor defining the layout size and stacking ratio between the low-voltage and high-voltage switch</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Switching time of the RF switch</td>
</tr>
<tr>
<td>$\varepsilon_{\text{ox}}$</td>
<td>Permittivity of the gate oxide</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>Relative permittivity</td>
</tr>
<tr>
<td>$\varepsilon_{r, \text{SiO}_2}$</td>
<td>Permittivity of silicon dioxide $\varepsilon_{r, \text{SiO}_2} = 3.9$</td>
</tr>
<tr>
<td>$\varepsilon_{r, \text{Si}}$</td>
<td>Permittivity of silicon $\varepsilon_{r, \text{Si}} = 11.65$</td>
</tr>
<tr>
<td>$\varepsilon_{r, \downarrow}$</td>
<td>Relative permittivity for flip-chip configuration</td>
</tr>
<tr>
<td>$\varepsilon_{r, \uparrow}$</td>
<td>Relative permittivity for wire-bonded configuration</td>
</tr>
<tr>
<td>$A_{\text{dB}}$</td>
<td>De-embedding error in dB</td>
</tr>
<tr>
<td>$A$</td>
<td>Area</td>
</tr>
<tr>
<td>$C_0$</td>
<td>Capacitance between two metal lines</td>
</tr>
<tr>
<td>$C_{1, \text{ez}}$</td>
<td>De-embedded capacitance</td>
</tr>
<tr>
<td>$C_{\sigma, i}(f)$</td>
<td>Standard deviation of measured capacitance</td>
</tr>
<tr>
<td>$C_{\text{ds}}$</td>
<td>Drain-source overlap capacitance</td>
</tr>
<tr>
<td>$C_{\text{eq}}$</td>
<td>Equalization capacitance</td>
</tr>
<tr>
<td>$C_{\text{fd}}$</td>
<td>Fringing capacitance along the feed line</td>
</tr>
<tr>
<td>$C_{\text{gd}}$</td>
<td>Gate-drain overlap capacitance</td>
</tr>
<tr>
<td>$C_{\text{gs}}$</td>
<td>Gate-source overlap capacitance</td>
</tr>
<tr>
<td>$C_{\text{max}}$</td>
<td>Maximum capacitance</td>
</tr>
<tr>
<td>$C_{\text{MIM}}$</td>
<td>Capacitance value of the MIM capacitor</td>
</tr>
<tr>
<td>$C_{\text{min}}$</td>
<td>Minimum capacitance</td>
</tr>
<tr>
<td>$C_{\text{MOM}}$</td>
<td>Capacitance value of the MOM capacitor</td>
</tr>
<tr>
<td>$C_{\text{off}}$</td>
<td>Off-capacitance</td>
</tr>
<tr>
<td>$C_{\text{pp,N}}$</td>
<td>Brick capacitance</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>-------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$C_{sub}$</td>
<td>Substrate capacitance</td>
</tr>
<tr>
<td>$CF_{TF}$</td>
<td>Power transfer coefficient from aperture tuning point to feed</td>
</tr>
<tr>
<td>$CF_{TO}$</td>
<td>Power transfer coefficient from aperture tuning point to open</td>
</tr>
<tr>
<td>$d_{\downarrow}$</td>
<td>Thickness of the package material or PCB laminate in flip-chip configuration</td>
</tr>
<tr>
<td>$d_{ox}$</td>
<td>Thickness of a thin dielectric sandwiched between two thick metal plates</td>
</tr>
<tr>
<td>$d_{\uparrow}$</td>
<td>Thickness of the silicon material in wire-bonded configuration</td>
</tr>
<tr>
<td>$E_{H}$</td>
<td>Voltage source describing the harmonics generated by the aperture tuner</td>
</tr>
<tr>
<td>$FOM$</td>
<td>Figure-of-merit</td>
</tr>
<tr>
<td>$H_{2}$</td>
<td>Second harmonic</td>
</tr>
<tr>
<td>$H_{3}$</td>
<td>Third harmonic</td>
</tr>
<tr>
<td>$I_{d}$</td>
<td>Drain current</td>
</tr>
<tr>
<td>$L_{FO}$</td>
<td>Distance from the feed to open</td>
</tr>
<tr>
<td>$L_{FS}$</td>
<td>Distance from the feed to short</td>
</tr>
<tr>
<td>$L_{TF}$</td>
<td>Distance from the feed to aperture tuning point</td>
</tr>
<tr>
<td>$L_{TO}$</td>
<td>Distance from the aperture tuning point to open</td>
</tr>
<tr>
<td>$L$</td>
<td>Physical length</td>
</tr>
<tr>
<td>$P_{max}$</td>
<td>Maximum available power</td>
</tr>
<tr>
<td>$P_{TF}$</td>
<td>Harmonic power coupled back to the feed point</td>
</tr>
<tr>
<td>$P_{TO}$</td>
<td>Radiated harmonic power</td>
</tr>
<tr>
<td>$R_{\Omega}$</td>
<td>Sheet resistance of the poly silicon film</td>
</tr>
<tr>
<td>$R_{G}$</td>
<td>Gate resistor</td>
</tr>
<tr>
<td>$R_{Lin}$</td>
<td>Linearization element for Dickson charge pump</td>
</tr>
<tr>
<td>$R_{off}$</td>
<td>Off-resistance</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>On-resistance</td>
</tr>
<tr>
<td>$R_{poly}$</td>
<td>Resistance of the poly silicon</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$R_R$</td>
<td>Radiation and loss resistance</td>
</tr>
<tr>
<td>$S_{dut,fix}$</td>
<td>$S$-parameter matrix of the non-de-embedded measured test fixture with DUT</td>
</tr>
<tr>
<td>$S_{dut}$</td>
<td>$S$-parameter matrix of the de-embedded DUT</td>
</tr>
<tr>
<td>$S_{open,fix}$</td>
<td>$S$-parameter matrix of the non-de-embedded measured test fixture without DUT</td>
</tr>
<tr>
<td>$S_{C,ez}$</td>
<td>Sensitivity of the de-embedded capacitance</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>Thickness of the gate oxide</td>
</tr>
<tr>
<td>$t_l$</td>
<td>Thickness of the silicon material in flip-chip configuration</td>
</tr>
<tr>
<td>$V_{ds}$</td>
<td>Drain-source voltage</td>
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<tr>
<td>$V_{dut,in,RF,peak}$</td>
<td>Peak RF voltage at the input of the shunt DUT</td>
</tr>
<tr>
<td>$V_{dut,out,RF,peak}$</td>
<td>Peak RF voltage at the out of the shunt DUT</td>
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<tr>
<td>$V_{g0}$</td>
<td>DC gate-source component</td>
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<td>$V_{gs}$</td>
<td>Gate-source voltage</td>
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<td>$V_g$</td>
<td>Gate control voltage</td>
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<tr>
<td>$V_{RF,BR}$</td>
<td>Breakdown voltage of the transistor</td>
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<td>$V_{RF,max}$</td>
<td>Maximum RF voltage handling</td>
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<td>$V_{RF,peak}$</td>
<td>Peak RF voltage</td>
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<tr>
<td>$V_{tn}$</td>
<td>Threshold voltage</td>
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<tr>
<td>$W$</td>
<td>Physical width</td>
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<tr>
<td>$Y_{dut,IL}$</td>
<td>Addmitance of the network including the L-pad</td>
</tr>
<tr>
<td>$Y$</td>
<td>Addmitance matrix</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>Characteristic impedance</td>
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<td>$Z_C$</td>
<td>Impedance of the gate-source overlap capacitance</td>
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<td>$Z_{dut,off}$</td>
<td>Input impedance of the DUT</td>
</tr>
<tr>
<td>$Z_{FS}$</td>
<td>Impedance of the transformed short by the transmission line $L_{FS}$</td>
</tr>
<tr>
<td>$Z_H$</td>
<td>Source impedance of the voltage source $E_H$</td>
</tr>
<tr>
<td>$Z_S$</td>
<td>Source impedance at the feed $Z_S = 50 , \Omega$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
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<tr>
<td>$Z_{TF}$</td>
<td>Impedance of the transformed total input impedance by the transmission line $L_{TF}$</td>
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<tr>
<td>$Z_{TO}$</td>
<td>Impedance of the transformed resistance $R_R$ by the transmission line $L_{TO}$</td>
</tr>
</tbody>
</table>
1 Introduction

Motivation
The introduction of smartphones in 2007 radically changed the mobile telecommunication industrial market and smartphones gained significant market share, making them one of the best-selling devices worldwide. Thanks to powerful central processing units (CPU), modern smartphones provide new applications and entertainment like social networking, streaming, gaming etc. in contrast to conventional telecommunication devices and become therefore an important device of our life. The amount of data consumption over the past decade increased significantly due to the high utilization of smartphones and influences directly the industrial market. The telecommunication standards like the global system for mobile communications (GSM) or the third generation universal mobile telecommunication systems (UMTS) don’t satisfy the customer requirements due to insufficient performance in terms of data rate and bandwidth [1]. The recent telecommunication standard long term evolution (LTE) – 4G increases the data rate and bandwidth in modern cellular user equipment. The quality of data transmission is achieved by utilizing various techniques, among others carrier aggregation (CA), MIMO and antenna tuning. Carrier aggregation is aimed at providing high data rates by simultaneously sending or receiving at different frequency bands and is one of the major features of the third generation partnership project (3GPP). The 3GPP developed the fifth telecommunication standard 5G, which is already implemented in actual flagship smartphones [2]. 5G improves the bandwidth and data rate furthermore by utilizing beamforming and massive MIMO antennas [3]. The mentioned techniques increase the complexity of modern cellular equipment front-ends. A simple example of a current cellular equipment front-end is portrayed in Fig. 1.1.

The main and diversity IFAs or planar inverted-F antennas (PIFAs) of a LTE smartphone are integrated into the chassis of the device as shown in Fig. 1.1 [4], [5]. Due to the high-complexity and limited size inside the device, the antennas have a small form factor resulting in low radiation efficiency and high mismatch loss of the intrinsic antenna. The performance of the antennas is optimized with tuning techniques by performing impedance tuning at the feed or aperture tuning along the antenna. In general, impedance matching improves the return loss at the feed and aperture tuning changes the distribution of voltage and current along the antenna, improving the radiation properties of the IFA and impedance matching at desired frequency bands [6],
The aperture tuning devices are directly attached to the antenna, as sketched in Fig. 1.1, and exposed to high radio frequency (RF) voltages even at moderate transmitter (TX) power levels. When the antenna is fed with the maximum available power, RF voltage peaks of around 80 V can be generated along the antenna. For convenience, aperture tuning devices are separated into two voltage handling classes, 40 V and 80 V, according to the voltage distribution along the antenna, as shown in Fig. 1.2(a). Commercial aperture tuners in modern cellular user equipment are based on high-voltage RF switches in bulk- or silicon-on-insulator (SOI)-CMOS technologies. In contrast to some alternative technologies, such as RF micro-electro-mechanical systems (MEMS), bulk- or SOI-CMOS-based RF switches offer monolithic integration capabilities, low manufacturing cost, overall good small- and large signal RF performance, outstanding electrostatic discharge (ESD) robustness, and reasonably low $R_{on}C_{off}$ figure-of-merit ($FOM$) [10], [11], [12]. Linearity of the high-voltage aperture tuners in modern cellular user equipment became of paramount importance for efficient carrier aggregation implementation.
because of their direct contact to the build-in antennas [13]. Two examples, where the receiver (RX) is desensed by the coupled nonlinear products of the uplink signal to the RF receive path are shown in Fig. 1.2(b). The third harmonic of the uplink TX band 17 in the first carrier aggregation scenario couples over the air to the receive path and falls into the RX band 4. In the second scenario a desensitization of the RX downlink signal in band 4 by the third-order intermodulation product of two TX bands 1 and 3 is demonstrated. High-voltage levels at the aperture tuner devices is the reason for potentially high nonlinear distortion generation that cannot be easily suppressed or filtered out, thus the improvement in terms of linearity for antenna tuners in general and aperture tuners in particular is essential [14]. The hard limit for the level of generated nonlinear products is set by 3GPP, where the radiated harmonics must satisfy the maximum out of band spurious emission requirements of –36 dBm [2].

The small signal parameters like on-resistance $R_{on}$, off-resistance $R_{off}$ and off-capacitance $C_{off}$ are key parameters for high-voltage RF switches. The power losses in the antenna tuning system contributed by the tuning IC are generally determined by $R_{on}$ and $R_{off}$. The power loss in on-state is determined by the voltage drop on the on-state switch, which obviously shall be kept as low as possible. $R_{off}$ represents the equivalent shunt resistance at the excited port of the off-state switch representing all contributors to the power loss at a given frequency. This parameter shall be minimized to keep losses low. In both on- and off-states the dissipated power should be reduced to a minimum. The off-capacitance determines the amount of parasitic loading and resonance frequency when the tuning element is disconnected from
the antenna and in general shall be kept as low as possible. A basic aperture tuning network consist of an inductor and a high-voltage RF switch connecting or disconnecting the tuning inductor to the ground. In combination with large inductors, $C_{\text{off}}$ may exhibit series resonance in the telecommunication high-frequency spectrum generating a short at the antenna.

**Goals of the Work**

The goal of the research is to investigate bulk- and SOI-CMOS-based high-voltage RF switches and applications thereof, with the special focus on:

- Improving small- and large-signal RF performance of the core switch by investigating different layouts of the switch and providing the description of nonlinearities in shunt aperture tuning switches operating in off-state. The latter focuses on second- and third-order nonlinear products and their power distribution as a function of layout geometry of the high-voltage RF switch transistor.

- Extending the functionality of the switch by adding a voltage detector with reduced harmonic feedback into the sensed RF path of the core switch for detecting the peak RF voltage distribution along the antenna.

- Improving the performance of the antenna tuning system by application co-design; providing an analysis of the harmonics distribution in the aperture-tuned IFA using first-order transmission line model. The analysis allows the prediction of the local minima for the second and third harmonics for a given use-case, enabling the optimization of the nonlinear performance of an antenna tuning system on the application level; proposing novel tuner architectures providing dual voltage handling class in one single design or for the use as decoupling and tuning element of MIMO antennas.

In order to fulfil the posed goals the following stages are accomplished:

- Design of test structures in bulk- and SOI-CMOS technologies for deep understanding of the performance $FOM$ for the core switch, optimization and verification of the analytical models.

- Novel RF switch-based tuning IC architectures are proposed by investigating antenna topologies and their issues in modern handheld cellular devices.
Design and layout of PCBs for verification of the fabricated hardware, including linearity, maximum voltage handling capabilities and small-signal performance of RF switches.

Propose a reconfigurable application-relevant demonstrator, with antenna and aperture tuning ICs for the evaluation of the proposed structures on the application level.

Part of this thesis has already been published in peer-reviewed international journals or conference digests, in particular in references no. 5, no. 10 and no. 15 cited in the list of publications of the author (see pages 115 – 116). In these three publications more than 95% of presented results are achieved by the author.

**Thesis Organization**

In the second Chapter an overview of technologies for reconfigurable RF front-ends is provided. Chapter 3 focuses on dedicated RF bulk- and SOI-CMOS technology, where the RF switch is described for both technologies and elementary devices are presented. In the fourth Chapter an insight into MOSFET-based RF switch transistor is given, the known operation mode, limitations and layout solutions are discussed. Chapter 5 starts with a general design overview of high-voltage RF switches and continues with the analytical description of the substrate capacitance and nonlinearities. The sixth Chapter covers the hardware characterization of antenna tuning ICs describing the measurement procedures for small- and large-signal evaluation. In Chapter 7 the application-relevant demonstrator for the evaluation of the proposed structures on the application level is presented. Theoretical findings regarding to the demonstrator are described in this section. Novel switch architectures are presented in the Chapters 8 – 10. Design, small- and large-signal measurements as well as a use-case on the application level is provided in these chapters. Finally, the thesis is closed with a conclusion and outlook in Chapter 11.
2 Technologies for Reconfigurable RF Front-Ends

A brief introduction into different technologies for reconfigurable RF front-ends is provided in this chapter. The advantages and drawbacks of the technologies are discussed and an overview of tunable antennas are presented. The chapter is summarized with a discussion.

2.1 CMOS Technology

CMOS technology introduced by Fairchild Semiconductors (meanwhile overtaken by ON Semiconductor) have been investigated for more than five decades. 1963 Frank Wanlass, a scientist at Fairchild semiconductors, demonstrated the use of complementary pairs with p-type channel and n-type channel MOS transistors in logic circuits [15], [16], [17]. CMOS devices are widely implemented in digital, analog and RF circuits, since CMOS devices provide low power consumption, high reliability, and low-cost manufacturing, which is desirable in high-volume applications. A paramount benefit of CMOS is the scalability enabling further reduction of the manufacturing cost [18]. In 1965 Gordon Moore, the founder of Intel, observed, that CMOS tends to shrink and the number of transistors in an IC doubles every 18 to 24 months, according to the popular Moore’s Law [19]. The first microchips based on CMOS technology comprises 2300 transistors with the gate lengths in the range of µm [20]. Meanwhile flagship microchips are manufactured in 7 nm CMOS technology and are composed of tenth billions of transistors [21]. The next technology step is CMOS transistors with 3 nm gate length, which is already in the starting gates. CMOS technology is principally based on bulk- or SOI-CMOS process using silicon based wafers. The difference of these technologies is their manufacturing costs and their performance with respect to the substrate isolation [22]. Silicon is a semiconductor, which is established in today’s RF, microwave, analog and digital circuits. Silicon enables low-cost manufacturing with overall good performance [23].

Bulk-CMOS Technology

In bulk-CMOS technology the circuit is composed directly on the silicon material without any galvanic substrate insulation. The isolation effect is achieved through reverse-biased pn-junctions. Some of the paramount parameters of the substrate material is the resistivity defining the behavior of the deposited
circuits over the substrate material since silicon is a lossy and nonlinear material. The nonlinear behavior of silicon substrates is related to the material resistivity. Silicon substrate materials with high-resistivity enable low coupling with the substrate, especially important for designing of RF circuits [24], and improves the nonlinear, small-signal, as well as large-signal performance. The resistivity of the substrate materials in bulk-CMOS technology is in the range between $10^{-4} \text{–} 10^4 \Omega \text{cm}$ and is influenced by the doping concentration of the material [25].

**SOI-CMOS Technology**

SOI process is among the most promising processes to reduce the die size and power consumption compared to circuits based on standard bulk-CMOS technology [22]. Silicon dioxide ($\text{SiO}_2$) is used as the insulating layer, also known as buried oxide (BOX). The artwork of example SEM cross section images as shown in Fig. 2.1 demonstrates the difference between SOI- and bulk-CMOS.

![Example SEM cross section images of typical (a) bulk-CMOS and (b) SOI RF NMOS transistor with sub-micron gate lengths.](image)

The BOX has the ability to:

- Reduce some of the parasitic capacitances (e.g. between drain and source of a MOSFET), thus improving the $R_{\text{on}}C_{\text{off}} FOM$ of the switch transistor by up to 20% [26].
- Leakage current towards the substrate due to the insulating BOX layer.
- Eliminate the risk of latchup.

However, these benefits are achieved at the expense of the increase in manufacturing cost and poorer thermal properties [22], [25]. Among the noticeable advantages and drawbacks that distinguish the CMOS technology from other technologies are:
Reasonable small signal performance: The $R_{on}C_{off}$ product of bulk- or SOI-CMOS switches are below hundred fs in state-of-art technologies.

High monolithic integration capabilities: The power and control unit, capacitors, resistors, as well as inductors can be integrated within a single die.

The switching time of MOS transistors is quite fast [25].

Linearity: High-resistive substrate materials with trap rich layer improve the linearity by reducing the coupling to the substrate material [26].

Low power consumption of the monolithically-integrated circuits: The static power consumption of a single transistor is in the range of nW per gate. The active power depends on the switching time, supply voltage, frequency, and output load [17].

ESD robustness: Devices based on CMOS technology easily achieve the industry ESD compliance level of above 1 kV human body model (HBM) [10], [27].

Manufacturing costs: Due to the high-volume utilization of CMOS-based technologies, the fabrication cost of CMOS is low compared to other technologies.

Substrate: As mentioned previously, the substrate is nonlinear and lossy. The coupling to the substrate is influenced by the frequency and increases with high frequency, thus lowering the Q-factor of the components. Large-area switches also suffer from excessive performance loss at high-GHz frequencies.

Power handling capabilities of the single transistors: A single transistor can handle RF voltages typically below 4 V. Since the RF switches are exposed to high RF voltages the stacking of RF transistors is indispensable. However, the stacking of transistors has an unfavorable impact on $R_{on}C_{off}$, space and nonlinear behavior.

2.2 Micro-Electro-Mechanical Systems

RF switches based on MEMS are used in various application areas such as in tunable filters and antennas as well as in reconfigurable matching networks since 1996. Some main application fields are for example radio detection and ranging (Radar) systems for defense applications, automotive radars, satellite communication systems, wireless communication systems and instru-
mentation. In modern cellular user equipment RF MEMS switches are used in the front-end as a single pole two throw (SP2T), single pole four throw (SP4T) switches [28]. Some smartphone models incorporated MEMS-based antenna aperture tuners [29], however the market share of the MEMS tuners in mobile phones is very low. Besides ohmic switches, RF MEMS are designed as capacitive switches for frequency application starting from 2 GHz to various 100 GHz, switched capacitors operating from 500 MHz up to several 100 GHz and analog varactors with a continuous tuning range [30]. A generic MEMS switch device consists of a membrane, called cantilever for a series switch or bridge for a shunt switch and is processed on SOI or silicon-on-glass (SOG) substrates [31]. An example of a cantilever series switch and air bridge shunt switch is portrayed in Fig. 2.2 [32]. To generate an electrical short- or open-circuit, MEMS switches use mechanical movements to actuate the membrane by obtaining electrostatic, magnetostatic, piezoelectric or thermal forces to the membrane. The majority of MEMS switches use electrostatic actuation, where a pull-down electrode is placed parallel to the RF path for a series switch and under the RF path for a shunt switch as shown in Fig. 2.2 [28].

![Figure 2.2: (a) Cantilever series and (b) shunt bridge switch.](image)

Applying a pull-down voltage of several tenth of volts pushes the cantilever or the bridge to the RF path and enable an electrical contact. For releasing the membrane, a reverse pull-down voltage is required [33]. In off-state the membrane in both switches is relaxed in the air, forming the parasitic off-capacitance $C_{\text{off}}$, which is basically defined by the distance between the membrane and the transmission line and the gap between the RF lines. In on-state the membrane is pushed towards the RF path generating a direct contact between the membrane and the RF path for resistive switches. Depending on the switch topology, the on-resistance $R_{\text{on}}$ is generated between the RF paths via the cantilever for the series switch or from the membrane to the ground.
for the shunt switch. The $FOM$ of RF switches is defined as a ratio of $R_{on}$ and $C_{off}$ according to Eq. (2.1):

$$FOM = R_{on}C_{off}.$$  \hspace{1cm} (2.1)

Apparently, low $R_{on}$ and $C_{off}$ results in superior electrical performance of the RF switches. RF MEMS switches implicates following advantages and drawbacks over other switch technologies:

- **High isolation**: The $C_{off}$ is due to the air (insulator) between the membrane and RF path very low [12].

- **Low insertion loss**: The direct metal-to-metal contact in on-state enables a low $R_{on}$, which extremely lowers the loss and increases the Q-factor of the device [30].

- **$FOM$** in the range of 20 fs, which is substantially below the state-of-art CMOS RF switch transistors [34].

- **Overall good linearity**: The harmonics of the RF MEMS switch is related to the substrate material, which has a significant impact on linearity. High resistivity (HR) substrates improves the linearity. With glass substrates MEMS switches can outperform other switch techniques in terms of linearity [35], [36].

- **For switching a high actuation voltage (pull-down voltage) in the range of several tenth of volts is necessary to push the membrane to the RF transmission line and relax it.** A high-voltage charge pump is required to generate the desired actuation voltage [33], [12].

- **RF power handling**: A parameter determining the RF power at which the MEMS switch fails to operate properly. A high RF power can actuate the membrane and push it to the RF transmission line. As long the high RF power is applied the force locks the membrane in on-state. In other words the membrane could not relax in the air [33]. The average RF power handling is up to 50 mW [28].

- **Weak intrinsic ESD robustness**: RF MEMS switches are very sensitive to ESD and fails typically between 100 V and 200 V HBM ESD [11].

- **MEMS are less reliable compared to solid state circuits.** The lifetime as well as the switching time is not competitive to standard CMOS switch technologies [37].
High costs: Packaging is the most expensive and critical step, processing an RF MEMS switch and primarily effects the cost of production. The seal of the packaging process for MEMS switches must be hermetic or near hermetic since MEMS switches are very sensitive to moisture [28]. The production cost can be reduced by using wafer-scale packaging solutions as glass-to-glass bonding [38].

2.3 Thin-Film BST Materials

Barium strontium titanate (BST) is based on the solid solution of the oxides barium titanate (BTO) and strontium titanate (STO) [39]. BST is suitable for the application in dynamic random access memory (DRAM), bypass capacitors, nonvolatile memories, as well as in tunable RF and microwave components [40]. The material has a temperature depended behavior defined as the Curie temperature. Below the Curie temperature the material is ferroelectric, making the device unsuitable for tunable RF applications, since ferroelectric materials are very nonlinear and possess a hysteresis that generates losses and nonlinearities. Above the Curie temperature the BST material becomes para-electric generating a high dielectric constant [39]. However, para-electric materials produce high nonlinear distortions. Thin-film BST materials allow to reduce the temperature dependency and avoid the Curie effect [25] making them suitable for the fabrication of tunable RF components, such as tunable filter, voltage controlled oscillators (VCO) and phase shifters [41]. Application examples are reported in literature [40], [42], [43], [44]. One of the most important features of thin-film BST is the field depended permittivity, which can be tuned by applying a DC voltage [40], [41]. The cross section and the capacitance curve over the DC bias voltage is depicted in Fig. 2.3(a) and Fig. 2.3(b) respectively [41].

The maximum available capacitance value $C_{\text{max}}$ is reached when the material is stimulated with zero DC bias voltage. Inversely applying DC voltage levels close to the breakdown of the thin-film material diminish the capacitance value to the minimum $C_{\text{min}}$ [42]. Since the capacitance curve of the thin-film BST is according to Fig. 2.3(b) in a nonlinear fashion, RF voltage swings may modulate the capacitor value and generate greater harmonics [25]. Tunable components based on thin-film BST offers some advantages and drawbacks, which are summarized below:

- Tunable components realized with thin-film BST demonstrates in overall a high Q-factor [41], [42].
Almost zero energy consumption except for leakage current from the material [25].

High RF breakdown voltages of above 80 V are demonstrated.

Since thin-film BST is ferroelectric, linearity has been a concern, especially for high-power applications [45]. The linearity can be improved with reducing the tuning range of the BST device [25].

For controlling, BST materials requires a DC bias voltage. Therefore, an on-chip or off-chip high voltage charge pump and a digital-to-analog converter (DAC) are required. Typically, dedicated power control units are used, which may impact cost and compactness of BST-based solutions.

The ESD performance of thin-film BST materials is poor in contrast to standard CMOS or SOI technology [25].

### 2.4 Resistive Memory Technology

Nonvolatile resistive memory RF switches are some of the emerging technologies for reconfigurable RF front-ends. They are typically two-terminal passive devices, where the resistive state varies by the physical actuation among the different technologies. Depending on the technology the actuation is controlled by an electrical field, current or heat. Some technologies for resistive memory switches are conductive-bridge random access memory (CBRAM), resistive RAM (ReRAM) and phase-change memory (PCM). The reduced power consumption and back-end-of-line (BEOL) compatibility
makes resistive memory switches potentially suitable for the utilization in modern cellular user equipment [46].

**Conductive-Bridge RAM Switches**

CBRAM-based RF switches are based on nanoionics behavior and consist of a simple two-electrode coplanar geometry, where the electrodes are separated within a small gap [47]. The operating modes are set with a conductive filament, which is deposited in the small gap between the electrodes. The conductive filament is formed with electrochemical reactions, ion migration or Joule heating [48]. The on-state is performed with a positive voltage relative to the inner electrode, wherein a voltage with reversed polarity removes the electrochemically grown filament and forces the device into the off-state [49]. The $R_{on}$ is related to the gap size, since a smaller gap between the electrodes reduces the filament length, thus reducing $R_{on}$. On the other hand, $C_{off}$ increases with a smaller gap, due to the reduced distance between the electrodes [46].

Some advantages and drawbacks of CBRAM-based RF switches are:

- ✔ Superior $FOM$ due to low $R_{on}$ and $C_{off}$ [49], [50].
- ✔ Fast switching time.
- ✗ Reliability issues: Oxidation of electrodes and filament instability; reset failure due to filament overgrowth [51]; low resistive state increases with time and temperature [47].
- ✗ Power handling capability of up to 50 mW [49].
- ✗ Design issues due to the parasitic resistance surrounding the devices.
- ✗ For BEOL-compatible, diffusion barriers are required to prevent the contamination of the underlying transistors [46].

**Resistive RAM RF Switches**

ReRAM-based RF switches are constructed similar to CBRAM with a metal oxide sandwiched between two metal electrodes in a metal-insulator-metal (MIM) structure [52]. The switching operation is performed by moving oxygen anions in the oxide lattice [53]. As in CBRAM a conductive filament formed after electroforming sets the switch into on-state. The off-state is realized by Joule Heating and ion migration. The oxidization of the conductive filament or oxygen ions migrating back to the oxygen vacancies increases the resistance to the high resistive state [46].
2.4 Resistive Memory Technology

Some advantages and drawbacks of ReRAM-based RF switches compared to other technologies are:

✔ ReRAM devices offer fast switching and demonstrate switching time in the order of nanoseconds [54], [55].

✔ ReRAM devices show low-power energy consumption [56], [57].

✖ ReRAM switches are limited for the applicability in tunable components, since the demonstrated $R_{on}$ is high compared to other technologies [58].

✖ ReRAM devices suffer from reliability issues regarding the anomalous reset, resistance variation and increasing $R_{on}$. The anomalous effect is caused by obtaining a large current after a reset operation, which leads to defects in the bottom electrode. Defects in the conductive filament and in the depleted gap generates the time-to-time resistance variation [51]. The increasing $R_{on}$ is due to gradual dissolution of the conductive filament, which is further accelerated with high temperatures [46].

Phase-Change Memory RF Switches

PCM-based RF switches are the most suitable resistive memory technology for the application in tunable RF components due to the high endurance in terms of switching cycle compared to other resistive technologies [46]. PCM devices are constructed from two electrodes, a phase-change material, such as Ge$_2$Sb$_2$Te$_5$ germanium-antimony-telluride (GST) or germanium telluride (GeTe), placed between the two electrodes as well as a heater located below the phase-change material as portrayed in Fig. 2.4(a) [59].

![Figure 2.4](image-url)

**Figure 2.4:** (a) Generic structure of a PCM according to [59] and (b) the cross section of a directly heated two-terminal PCM-based RF switch [46].
In the initial state the PCM switch is in on-state since the phase-change material is in the crystalline state due to the processing temperature of the BEOL. The off-state is realized with a rapid temperature change in the phase-change material. First the programming region is melted with high local temperatures, typically above 600°C, and then quenched quickly to temperatures below the crystallization temperature to prevent the phase-change-material from crystallization. This large and rapid temperature change is achieved by a current with a large amplitude and short pulse width [46], [59]. So far two-, three, and four-terminal PCM RF switches are reported in [60], [61], [62]. The heating of the phase-change-material is performed directly for two-terminal RF switches requiring voltages between 3 V – 7 V. Three- and four-terminal PCM-based RF switches can be heated directly or indirectly, where voltages as high as 10 V are necessary for indirect heating [63], [64]. A cross section of a directly heated two-terminal PCM-based RF switch is shown in Fig. 2.4(b) [60].

As PCM-based RF switches belong to resistive memory technologies the advantages and drawbacks are similarly to CBRAM and ReRAM. However, some discrepancies are listed below:

- ✔ PCM-based RF switches provide beneficial FOM, since $R_{\text{on}}$ and $C_{\text{off}}$ is low [60], [62], [63], [64].
- ✔ Low power energy consumption.
- ✔ Small area compared to other tunable RF technologies.
- ✗ Since the actuation of PCM-based RF switches is performed by a heater, the lifetime over switching cycles is less compared to solid-state circuits. However, PCM offers high endurance compared to other resistive memory technologies.
- ✗ PCM-based RF switches are not able to compete in switching time with standard solid-state technologies, since the switch requires 100 ns for amorphization and 1 µs for crystallization [46].

### 2.5 Tunable Antenna

Due to the increasing complexity and demanding esthetical requirements for modern cellular user equipment like smartphones, tablets, smart watches etc. the space left in the device for antennas is very constrained. The antennas of modern cellular user equipment are integrated into the housing of the device. The most promising candidates satisfying the demands of modern
2.5 Tunable Antenna

telecommunication standards including LTE and 5G are single-arm IFA and PIFA antennas. These antennas possess attributes like small formfactor, easy mounting and reconfigurability [65]. A single-arm IFA is constructed from a radiating arm, which is short-circuited to the device chassis. The chassis represents the ground plane of the antenna [65]. Modern cellular user equipment operates in multiple telecommunication frequency bands simultaneously and independently from each other. This is addressed by the IFA/PIFA, since they are suitable to provide dual- or multi-band coverage [65]. However, the integration into the housing and the small form factor of the antenna has some drawbacks, which cannot be neglected. The RF performance of the antenna is dramatically reduced due to the small formfactor and proximity to grounded metallic elements of the phone, for example USB or headphone plugs. In general, the radiation efficiency and the mismatch loss of the intrinsic antenna are reasonably high only at a small fraction of the cellular spectrum and cannot reasonably address all the required cellular bands. Consequently, antenna tuning is required to improve the RF performance and frequency coverage.

In the present days antenna aperture tuning has become de-facto standard in modern cellular user equipment and provides the direct control of the antenna resonance frequency. This is achieved by changing the effective electrical length of the antenna and can be accomplished physically or electrically [39]. There are many ways to perform aperture tuning. More than two decades ago first investigations to shrink the antenna size and increase the radiation efficiency of mobile telephone handset have been conducted [66]. Capacitively loaded inverted-F antennas reduced the dimensions of the antenna significantly for a given resonance frequency and improved the performance in terms of radiation efficiency and return loss [7], [66]. An antenna loaded by a pair of BST varactors is demonstrated in [67] and a PIFA tuned by a LC resonator in [9]. However, this tuning application aims at providing continuous tuning within or between cellular frequency bands. LTE and 5G devices utilize CA techniques, which cannot be realized with the above mentioned tuning topologies. Antennas that aim at switching between distinct cellular frequency bands fulfil the requirement on CA [68]. In this work the focus is primarily on single non-bended radiating arm IFA topologies tuned by high-voltage RF switches and RF switchable capacitors.

Antenna tuning circuits based on RF high-voltage switches typically comprise off-chip surface-mounted-device (SMD) inductors or capacitors. In [68] an aperture tuning circuit based on RF MEMS switchable capacitors is demonstrated. The antenna covers only cellular low- or mid-band. A triple-band antenna integrated in a metallic back cover mobile phone mock-up tuned by
three MEMS-based capacitors is reported in [69]. The antenna is tuned to the respective cellular frequency bands: low-, mid- or high-band. Since MEMS devices are sensitive to ESD and less reliable compared to bulk- or SOI-CMOS RF switches, switchable capacitors based on bulk- or SOI-CMOS with linear capacitors additionally integrated into the same die, also known as C-Tuners, are a practical embodiment of aperture tuner based on switchable capacitors. An example of the adjustable single-arm IFA covering three bands tuned by a single C-Tuner is demonstrated in [70]. Examples of antenna tuning systems are shown in Fig. 2.5. One IFA is tuned by an aperture tuning circuit based on high-voltage RF switches [6]. The second IFA is tuned by an aperture tuning circuit comprising a C-Tuner and shunt off-chip inductor $L_T$.

![Diagram](image)

**Figure 2.5:** Antenna tuner topology based on high-voltage RF switch (left) and C-Tuner (right).

**Discussion**

Different technologies for reconfigurable RF front-ends have been demonstrated in this chapter. Aperture tuning circuits based on BST, MEMS and CMOS technology have their own pros and cons in RF applications. BST varactors generate high harmonics when the device is exposed to large RF voltage amplitudes, since BST devices are constructed from ferroelectric material, which has an inherent nonlinear nature. In addition, BST varactors require high analog control voltages, which requires an external dedicated power management ICs. PCM may be a good contender in aperture tuning circuits due to their superior $R_{on}C_{off}$ product compared to other technologies. However, this technology needs more investigations in terms of reliability and ESD. Furthermore, the heater sandwiched between the two electrodes of the PCM devices requires high voltages. As in BST, off-chip power management ICs are required for PCM. MEMS capacitive tuners offer good quality factor and linearity. Nevertheless, their high sensitivity to ESD and limited reliability prevent their extensive use in antenna tuning applications. These commercially available and emerging high-performance RF switch technologies shares the common challenges in terms of integration, high-volume production and cost. Bulk- or SOI-CMOS offers superior ESD performance achieving easily the
industry ESD compliance level of above 1 kV HBM, high reliability over lifetime, high monolithic integration capabilities, high linearity and reasonable $R_{on}C_{off}$ product, which makes bulk- or SOI-CMOS technology as a favorable solution to industrial applications to date.
3 Dedicated RF Bulk- and SOI-CMOS Technologies

Most of today’s ICs for antenna tuning applications in cellular user equipment in commercial high-volume fabrication are based on either bulk- or SOI-CMOS technologies. This chapter focuses on the description of RF switch transistors in both technologies. In addition, a metal stack as well as elementary devices such as resistors and capacitors for both technologies are shown.

3.1 Bulk-CMOS RF Transistor

CMOS technology enables the fabrication of n-type (NMOS) and p-type (PMOS) transistors on the same die [71]. NMOS and PMOS transistors fabricated on a silicon p-substrate in bulk-CMOS technology are portrayed in Fig. 3.1(a) and Fig. 3.1(b).

Figure 3.1: (a) N-type and (b) p-type RF transistor in bulk-CMOS technology.

MOSFETs are four-terminal devices, where the source and drain contacts are symmetrical. By applying a reverse voltage to the substrate – typically the most negative voltage in the system – the source-drain junction will be reverse biased, which reduces the capacitance to the substrate and improves the nonlinear properties of the semiconductor device [26]. This technique is known as body biasing and is performed through an ohmic $p^+$ or $n^+$ region, depending on the MOSFET type. In MOSFET switch transistors the body (substrate) is biased by a relatively large negative voltage, comparable to the gate voltage. The gate is composed of heavily doped polysilicon over a thin layer of $\text{SiO}_2$, called gate oxide (GOX), which insulates the gate from the conductive channel, where the permittivity of the silicon dioxide is $\varepsilon_{\text{r, SiO}_2} = 3.9$ and the
thickness is in the range of a few nanometer. The gate length and width are important design parameters. The gate length of a MOSFET is defined as the distance along the source-drain path, wherein the gate width is perpendicular to the length. Most of the CMOS processes up to date use p-type silicon substrates [72]. Therefore, n-type transistors are fabricated directly on the substrate, whereas p-type transistors are placed in a local substrate. There are also double- or triple well techniques, which require further fabrication steps and increase the manufacturing costs. The source and drain of an n-type MOS is deposited with heavily doped \( n^+ \) regions placed symmetrically to the gate as shown in Fig. 3.1. The p-type transistor consists of an n-well, where the diffused layers are complementary doped compared to the n-type MOS transistor. In order to isolate different transistors, enhance the transistor density and reduce the leakage current, the CMOS-process utilizes shallow trench isolation (STI) process step. The lightly doped drain (LDD) is mandatory especially for n-type transistors to prevent hot carrier effects. The hot carrier effect may occur if very high voltage amplitudes are applied at the drain-source terminal of the n-type MOSFET leading to electrons with high kinetic energy in the channel. The excited electrons may penetrate the GOX and reach the gate, thus degrading the gate oxide and the threshold voltage of the device. The LDD is a narrow, self-aligned \( n^- \) region located between the channel and the source-drain diffusion. Besides preventing hot carrier effects, LDD enables increased power supply, which improves the voltage handling capabilities of a single transistor or reduce the channel length [73]. Since the channel mobility of holes are less compared to electrons, p-type MOSFETs suffer less from hot carrier effects in contrast to n-type MOSFETs.

### 3.2 SOI-CMOS RF Transistor

Since more than one decade SOI-CMOS technology has been established in antenna switches with more than 85% market share and is available in many foundries [26]. In 2015, improvements of 20% in \( R_{on}C_{off} \) product has been recorded [74]. Since then, the \( R_{on}C_{off} \) product has been reduced by more than two times. N-type and p-type MOS transistors in SOI-CMOS technology are depicted in Fig. 3.2(a) and Fig. 3.2(b). The BOX isolates the MOSFETs from the substrate, thus decreasing the parasitic drain-source capacitance due to the lower permittivity compared to silicon. SOI-CMOS technology provides less leakage current between the devices since each transistor is galvanically isolated from the others. SOI RF transistors are fabricated on HR silicon substrates, with resistance values higher than \( 1 \, \text{k} \Omega \cdot \text{cm} \) [75] and such materials are essential in antenna aperture tuning devices to reduce the substrate losses.
at high frequencies [76], [75]. However, oxidized HR-Si wafers are affected from parasitic surface conduction (PSC). Fixed charges within the oxide excite free carries near the substrate/buried oxide interface reducing the effective substrate resistivity and increasing the substrate losses [24]. Furthermore, this effect has a negative impact on the nonlinear performance of the transistor and sensitivity to DC voltage variations [24]. An effective technique to eliminate PSC is the introduction of trap-rich layer between the BOX and the HR silicon handle wafer. The free carriers at the substrate/BOX interface are captured by the trap-rich layer. The substrate recovers to its nominal resistivity, linearity and eliminating the high sensitivity to DC voltage variations. On the top of that, the trap-rich layer leads to a significant reduction of RF losses and crosstalk [24].

3.3 Metal Stack of RF CMOS Technologies

An example metal stackup for general-purpose RF CMOS technologies is portrayed in Fig. 3.3. The CMOS technology in the example consist of four metal layers, where each layer is isolated by SiO$_2$. The bottom metals are typically based on copper and the top metal is aluminum or may also be copper. The top-most thick metal layers are used to provide low-loss RF and power routing. The electrical properties of the typical conductive layers in 90 nm – 120 nm CMOS processes are provided in Table 3.1 [25].

3.4 Resistors in RF CMOS Technologies

Passive components like resistors, capacitors and inductors are mandatory for integrating a complete analog/RF circuit or system on a single chip. Resistors in integrated circuits are constructed by a doped silicon layer or a conductive
Dedicated RF Bulk- and SOI-CMOS Technologies

Figure 3.3: Metal stack of RF CMOS technologies.

Table 3.1: Properties of the metal layer of a typical general-purpose RF CMOS technology.

<table>
<thead>
<tr>
<th>Metal Layer#</th>
<th>Material</th>
<th>Thickness</th>
<th>Sheet resistance $\Omega/\square$</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Aluminum/Copper</td>
<td>3.00 µm</td>
<td>0.01/0.006</td>
</tr>
<tr>
<td>3</td>
<td>Copper</td>
<td>0.35 µm</td>
<td>0.1</td>
</tr>
<tr>
<td>2</td>
<td>Copper</td>
<td>0.35 µm</td>
<td>0.1</td>
</tr>
<tr>
<td>1</td>
<td>Copper</td>
<td>0.35 µm</td>
<td>0.1</td>
</tr>
</tbody>
</table>

thin film [77]. The latter is commonly applied in today's RF bulk- or SOI-CMOS technologies. Poly silicon is a proper material to implement linear, precise and high-resistive resistors with a small form factor compared to other conductive materials due to its higher resistivity per unity area, which may be varied by doping. A resistor made of poly silicon is shown in Fig. 3.4(a). The STI underneath the poly silicon isolates the resistor from the substrate, thus minimizing the substrate loss and improving the linearity of the resistor. The circuit model of the resistor is depicted in Fig. 3.4(b). The resistance of the poly silicon is defined as follows:

$$R_{\text{poly}} = R_\square \frac{W}{L},$$  \hspace{1cm} (3.1)
3.5 Capacitors in RF CMOS Technologies

Capacitors in integrated circuits are realized with two conductive plates separated by a thin insulating layer. Below are the key parameters which have to be considered when designing an integrated capacitor:

- **Capacitance density per unit area**: High capacitance density is required to form large capacitors. Typical values are in the range between 1 fF/µm$^2$ and 8 fF/µm$^2$ [78].

- **Voltage handling**: Since antenna aperture tuning switches and switchable capacitors are exposed to high RF voltages, the voltage handling capabilities of the capacitors should be carefully considered. The voltage handling varies from a few volts to 20 V for a typical single unit.

- **Q-factor**: Defines the ratio between stored energy to the lost energy. The losses of the capacitor must be minimized.

The standard available capacitors in bulk- or SOI-CMOS technology are MIM- and metal-oxide-metal-capacitors (MOM). Fig. 3.5(a) and Fig. 3.5(b) portray...
two implementations of MIM capacitors with respective layout views. The corresponding equivalent circuit diagram is shown in Fig. 3.6. In Fig. 3.5(a) the MIM capacitor is composed of a thin dielectric sandwiched between two thick metal plates. The MIM capacitance value can be extracted from Eq. (3.2) as:

\[
C_{\text{MIM}} = \frac{\varepsilon_0 \varepsilon_r A}{d_{\text{ox}}},
\]

where \( A \) represents the area of the minimum plate surface. Eq. (3.2) is valid for large-area MIMs with close to quadratic form-factors. For small capacitors the fringing part has to be carefully taken into account, which significantly adds to the total capacitance value. The capacitance of the MIM structure depends on the effective surface area of the small metal plate and the geometry of the dielectric material. Since the resistivity of the thick metal plates is low, the quality factor of the MIM structure from Fig. 3.5(a) is quite high. The MIM capacitors are typically rated for maximum voltage handling between 5 V and 30 V depending on the technology flavor. The MIM structure as shown in Fig. 3.5(b), is composed of two thin electrodes separated by a thin dielectric layer. The capacitor is wired with the same metal layer on the upper and lower electrode, approaching the electrodes from the sides. The Q-factor can be optimized by increasing the metal fingers density. In contrast to MIM capacitors, MOM capacitors are formed by lateral capacitive coupling between

![MIM capacitor variants with the respective layout views.](image)
3.5 Capacitors in RF CMOS Technologies

metal fingers as sketched in Fig. 3.7. The total capacitance value of MOM can be improved by overlaying more metal layers. The capacitance density is limited by the minimum distance between the metal fingers, height of the metal stack and dielectric constant of the dielectric material between the fingers. The total capacitance of MOM capacitors is described as:

\[ C_{\text{MOM}} = C_0 (n - 1) \]

(3.3)

where \( n \) is the number of fingers and \( C_0 \) the capacitance between two metal lines [78]. Depending on the requirements, there are advantages and drawbacks for both variants which have to be taken into account.

- The dielectric in MIM capacitors have almost double the permittivity compared to MOM capacitors. This means that MIM capacitors achieve double the capacitance density per unit area.

- Typically MIM capacitors are monitored in the production process which is not done for MOM capacitors. As a result, the tolerances of MIM capacitors are lower, in the range of ±10%, whereas MOM capacitor are fabricated with tolerances of up to ±20%.

- MIM structures require additional layer for the electrodes. For MOM capacitors there is no demand for additional process steps since it can be formed with standard available metal layers.
4 MOS RF Switch Transistor

In this chapter, the electrical characteristics of MOS RF switch transistors in terms of operation modes, parasitic elements, FOM and device limitations are presented. The layout considerations for improving the FOM of a single RF switch transistor are discussed.

4.1 General Description

The core structure of a linear RF switch consists of a high-ohmic resistor in series to the gate terminal of a MOSFET. The circuit of a MOSFET-based RF switch is shown in Fig. 4.1.

The gate resistor $R_G$ defines the nonlinear behavior and switching time of the switch. The time constant defining the switching time of the RF switch is described by Eq. (4.1):

$$\tau = R_G (C_{gs} + C_{gd}) = 2R_GC_{gs}. \quad (4.1)$$

According to Eq. (4.1) the switching time is linearly proportional to the gate resistor. The switching time could theoretically approach 0 s if the gate resistor is removed. However, such scenario would lead to strong linearity issues and power losses due to the non-even voltage division at the gate-source and gate-drain terminals. Ideally, the voltage distribution at the overlap capacitances $C_{gd}$ and $C_{gs}$ should be equal. Therefore, the gate resistor is much larger compared to the impedance $Z_C$ of the gate-source overlap capacitance. For $R_G \gg Z_C$ the RF current flows primarily through $C_{gd}$ and $C_{gs}$, which maximizes the linearity of the device. It is apparent, that the switching time and linearity together with the power losses of an RF switch is dependent from each other and can be adjusted by the gate resistor. Antenna aperture tuning switches...
have stringent requirements on linearity, while the switching time can be in the range between 2 µs– 10 µs [79].

4.2 Basic Operation Modes

First, we consider an RF switch transistor having a high-ohmic resistor at the gate $R_G \gg Z_C$ in off-state. An equivalent circuit diagram and the corresponding cross section including parasitic elements are shown in Fig. 4.2. For the above-mentioned bias condition with $R_G \gg Z_C$ the resistor is removed from the circuit diagram for convenience. The transistor operates in off-state, when the gate voltage $V_G$ is below the threshold voltage $V_{th}$. The threshold voltage is defined as the gate voltage, where the electron concentration underneath the gate equals to the concentration of the holes in the $p-$ substrate far from the gate. In other words, if the gate voltage exceeds the threshold voltage, the channel will be inverted, and a current between the drain and source may flow. Inversely, if the gate voltage is much below the threshold voltage the transistor operates in the cut-off region (meaning, off-state for the RF switch transistor) and no significant current flows through the transistor [80]. The AC current is defined and limited by the total capacitance between the source and drain terminals. The threshold voltage for an RF switch transistor lies in the rage between 0.1 V– 0.5 V. The RF switch transistor operates in off-state similarly to a capacitor as sketched in Fig. 4.2(a). The main contributors to the off-capacitance $C_{off}$ are the nonlinear parasitics overlap capacitances $C_{gd}$, $C_{gs}$ and the drain-source capacitance $C_{ds}$. The cross section of an off-state RF transistor including parasitics is portrayed in Fig. 4.2(b). Even small bias voltage at the body of an RF switch transistor generates a large depletion region due to the low substrate doping, which dramatically reduces the junction

![Figure 4.2](https://example.com/figure_4_2.png)

**Figure 4.2:** (a) Equivalent circuit diagram of a single RF switch transistor in off-state and (b) corresponding cross section.
4.2 Basic Operation Modes

Capacitance $C_{sb}$, $C_{db}$ and are negligible for the $C_{off}$ calculation of a single RF switch transistor. $C_{off}$ is calculated as the parallel connection of $C_{gs}$, $C_{gd}$ and $C_{ds}$ as shown in Fig. 4.2(a). Assuming that $C_{gs} = C_{gd}$:

$$C_{off} = \frac{1}{2} C_{gs} + C_{ds}.$$  \hspace{1cm} (4.2)

$C_{gs}$ and $C_{gd}$ are formed between the overlapping gate and source/drain diffusions separated by a thin gate oxide. The top-view of the cross section of a single RF switch transistor is depicted in Fig. 4.3 [81].

![Top view of the RF switch transistor.](image)

**Figure 4.3**: Top view of the RF switch transistor.

Since there is no channel between the drain and source in off-state, the overlap capacitances are calculated according to Eq. (4.3):

$$C_{gs} = C_{gd} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}} W L_{ov},$$  \hspace{1cm} (4.3)

where $L_{ov}$ describes the effective overlapping length of the source/drain diffusions with the gate, whereas $W$ is the gate width. Since the gate oxide is very thin the overlap capacitance in a single transistor is very large compared to the substrate capacitance $C_{sub}$. Therefore, the substrate capacitance is not considered for the calculation of the $C_{off}$. The drain to source capacitance is formed between the source-drain junctions separated by the highly doped p region. An attempt of the analytical derivation of the source-drain capacitance can be found in literature [82]. The source-drain capacitance is described using an electrical field, generated from the potential between the source-drain junction. Since the dielectric material is silicon, the gate-source capacitance is small compared to the overlap capacitances. According to [82] the drain-source voltage can be described as:

$$C_{ds} = \frac{\varepsilon_{Si}\varepsilon_0 \xi W}{L},$$  \hspace{1cm} (4.4)
where $\xi$ is the depth of the positive charge attracted to the channel between the drain-source diffusions. The value of the drain-source capacitance varies with the terminal voltage levels [82]. In the active mode the gate voltage is above the threshold voltage, which inverts the channel between the drain and source to an $n^+$ region. Depending on the gate voltage the transistor operates in weak, moderate, or strong inversion. The channel does not become inverted, as the voltage slightly increases above the threshold voltage. If the gate voltage is in the range of 100 mV or higher below the threshold voltage, the transistor operates in weak inversion also called subthreshold operation. Strong inversion occurs when the gate voltage is 100 mV or higher above the threshold voltage. It should be noted that most of the transistors in RF applications, including RF switches are operating in strong inversion. Moderate inversion is in between both regions. The considerations made in this chapter assume strong inversion operation [80]. An equivalent circuit and cross section of a single RF transistor in on-state are shown in Fig. 4.4. As the gate voltage exceeds the threshold voltage, a channel between the drain/source junctions is opened and current may flow from drain to source. In on-state the RF switch transistor is represented by $R_{on}$ between the drain/source terminals as shown in Fig. 4.4 (a). First, we consider the operation modes of the on-state RF switch transistor. When $V_{ds} \leq (V_{gs} - V_{tn})$ the transistor operates in triode region. The drain current follows the square law according to Eq. (4.5):

$$I_d = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} W \left[ \left( V_{gs} - V_{tn} \right) V_{ds} - \frac{V_{ds}^2}{2} \right]$$  \hspace{1cm} (4.5)$$

where $\mu_n$ is the electron mobility of the channel, $L$ is the effective length of the gate and $W$ is the width of the gate, $t_{ox}$ – gate oxide thickness, $\varepsilon_{ox}$ – permittivity of the oxide. Eq. (4.5) can be transformed to Eq. (4.6) considering the following

![Figure 4.4](image-url)
operating condition: $V_{gs} = V_{gs0} + V_{ds}/2$, (here the AC component of the $V_{gs}$ is half of the $V_{ds}$), where $V_{gs0}$ is the DC gate-source component (operating point) of the RF switch transistor, $V_{ds}$ is the voltage across the switch transistor, which has zero DC component:

$$I_d = \mu_n \frac{\varepsilon_{ox} W}{t_{ox}} \left[ \left( V_{gs0} + V_{ds}/2 - V_{tn} \right) V_{ds} - \frac{V_{ds}^2}{2} \right] = \mu_n \frac{\varepsilon_{ox} W}{t_{ox}} \left[ \left( V_{gs0} - V_{tn} \right) V_{ds} \right].$$

(4.6)

For applied drain-source voltage levels the drain current varies linearly with the drain-source voltage, thus the switch operates in the linear ohmic state. The on-channel resistance of a single RF switch can be described by differentiating Eq. (4.6):

$$R_{on} = \left( \frac{\partial I_d}{\partial V_{ds}} \right)^{-1} = \frac{1}{\mu_n \frac{\varepsilon_{ox} W}{t_{ox}} L \left( V_{gs0} - V_{tn} \right)}. \quad (4.7)$$

Since the gate width of RF switch transistors are typically several millimeters, the $R_{on}$ of the single transistor is typically well below $1\,\Omega$, which is much lower compared to the load impedance of an aperture tuning network. Therefore, the drain-source voltage drop over the transistor is very small compared to the voltage drop over the reactive tuning network. It should additionally be noted that the drain-source voltage drop in on-state is very low compared to the gate-source DC bias voltage. Due to this operation condition the RF switch transistor is always operating in linear ohmic region in the on-state (even though according to Eq. (4.6) it is not required to have a low drain-source voltage for linear operation, the higher order nonlinear effects not accounted for in Eq. (4.6) become more pronounced and make the response of the switch more nonlinear). It is mandatory to achieve a constant on-channel resistance over the full range of the applied RF excitation. This is primarily achieved by using a large gate resistor. In this case the whole transistor swings with the RF voltage and the gate-source voltage stays constant over the complete RF period. Another issue, which has to be mentioned here is, that during the negative RF swing the source-substrate diode is biased in forward direction. In order to prevent a current flow into the substrate, a substrate material with high resistivity and a negative bias substrate voltage is utilized.
4.3 Limitations of MOS Transistors for RF Switch Applications

The major limitations of the RF switch transistor are the drain-source breakdown voltage, which defines the voltage handling capabilities of a single transistor, the nonlinear distortions and gate-induced drain leakage (GIDL).

4.3.1 Breakdown Voltage

Aperture tuning devices are excited by high RF voltage levels, while operating in off-state. This results in high voltage drop across the drain-source nodes of the transistor. The breakdown voltage of RF switch transistors is defined as the voltage, where the transistor transits from off into on-state for a short time. This generates large harmonics, and the transistor may breakdown due to excessive thermal stress. An example is presented in Fig. 4.5.

\[ V_{RF,peak} = 2 \left( V_{tn} - V_{gs,dc} \right) \]  \hspace{1cm} (4.9)

**Figure 4.5:** Example for the calculation of the breakdown voltage \( V_{RF,BR} \).

The threshold voltage for the RF switch transistor is 0.4 V. The total gate-source voltage is composed of the RF signal distribution at the gate-source capacitance and the DC gate voltage. Since the gate-drain capacitance equals to the gate-source capacitance, half of the \( V_{RF,peak} \) signal drops over the gate-source capacitance. The total gate-source voltage \( V_{gs} \) is calculated by Eq. (4.8):

\[ V_{gs} = V_{gs,dc} + \frac{V_{RF,peak}}{2}. \]  \hspace{1cm} (4.8)

For \( V_{gs} > V_{tn} \) the transistor transits into on-state. Using Eq. (4.8) the breakdown voltage \( V_{RF,BR} \) of the transistor can be described as follow:

\[ V_{RF,BR} = 2 \left( V_{tn} - V_{gs,dc} \right). \]  \hspace{1cm} (4.9)
4.3 Limitations of MOS Transistors for RF Switch Applications

For a maximum $V_{RF,peak}$ of 7.4 V or higher the total gate-source voltage exceeds the threshold voltage of 0.4 V and the transistor will be open for the positive wave of the input RF signal. The breakdown voltage is influenced by the DC bias voltage and the threshold voltage. Since the threshold voltage depends on the effective gate length of the transistor, large gate length increases the threshold voltage of an RF switch transistor. However, increasing the gate length will decrease the small-signal $FOM$ of the device. The breakdown voltage and the $R_{on}C_{off}$ product are interdependent.

4.3.2 Nonlinear Distortions

The principal nonlinear contributors in a single off-state RF MOSFET are presented in Fig. 4.6. The odd-order nonlinearities are generated by the nonlinear overlap capacitances $C_{gs}$, $C_{gd}$ and $C_{ds}$. Since these capacitances are proportional to the width of the MOSFET, the odd-order nonlinearities can be traded-off later by proper sizing the RF switch in design-in phase. The substrate capacitance $C_{sub}$ contributes to the even-order nonlinear products, which can be improved with high resistivity substrate materials and trap-rich silicon substrates [83], [84]. Prof. Raskin and his team extensively investigate large-signal properties of HR-Si substrates over the last years [85]. Static harmonic distortion models show simulation errors greater than 15 dB for a coplanar transmission lines on HR substrates [86]. Further attempts to describe the nonlinear behavior of HR substrate have been made in [86]. However, the nonlinear substrate modeling is still in the premature state according to [86].

![Nonlinear contributors in a single RF MOSFET in off-state.](image)

**Figure 4.6:** Nonlinear contributors in a single RF MOSFET in off-state.
Penn state phils (PSP) model of the transistor can be used to predict the nonlinear behavior of a single transistor. It should be noted that the PSP model is more suitable than the widely used berkeley short-channel IGFET model (BSIM) in RF switch applications [87]. In [82] the modeling of the third harmonic based on the overlap and direct capacitances of a MOSFET with Volterra series is presented. The model shows a prediction error of up to 5 dB for the third harmonic of an off-state transistor. An attempt to predict the harmonics of an RF switch will be provided in Section 5.3. The prediction is based on investigated nonlinear performance of a reference structure and is performed in delta-terms [88].

4.3.3 Gate-Induced Drain Leakage (GIDL)

GIDL is one of the major limitations in high-stacked RF switches. It has a significant impact on the voltage handling capabilities of the switch. In highly scaled RF MOSFETs, the gate slightly overlaps the drain-source junctions. GIDL current is attributed to the gate-to-drain overlap region as illustrated in Fig. 4.7 [89].

![Figure 4.7: (a) GIDL of an off-state RF MOSFET and (b) schematic description of GIDL mechanism.](image)

The drain current over the gate-source voltage is shown in Fig. 4.7(a). Applying large voltage levels to the drain region forms a deep depletion region direct below the gate-drain overlap surface. High voltage levels at the drain region leads to high electric fields in the gate-drain overlap region, which induces a tunneling of valence band electrons into the conduction band [89], [90]. This effect occurs when the band bending is larger than the energy band gap [89]. The electron-hole pairs generated by the tunneling effect are collected by the drain and substrate. The minority carriers in the gate-drain overlap region flow to the substrate as substrate current and the majority carries flow to the drain as shown in Fig. 4.7(b). The mandatory electrical field for triggering
this effect depends on the concentration in the diffusion region, difference between the drain- and gate-source voltage as well as the oxide thickness. GIDL becomes more significant with decreasing oxide thickness, since the voltage required to generate the sufficient electrical field at the overlap region is directly proportional to the oxide thickness [90]. The GIDL current can be simulated in widely used BSIM [91].

4.4 Layout of the RF Switch MOSFET

The layout of an RF switch MOSFET with the corresponding circuit diagram is shown in Fig. 4.8. As mentioned, the RF switch transistor have gate widths of several millimeters in order to achieve low $R_{on}$. The gate length $L$ is set by the poly layer as depicted in Fig. 4.8. Large gate widths are realized with multiple fingers over the diffusion layer sketched as vertical red stripes.

![Figure 4.8: Layout of a SOI RF switch transistor and corresponding circuit diagram.](image)

The total width of the MOSFET is defined as:

$$W_{\text{total}} = W_f n_f$$

where $n_f$ is the number of fingers. The metal wiring of the drain-source region is conducted with the first metal layer to the highly doped $n^+$ regions as portrayed in Fig. 4.8. The local body contact is located at the top of the transistor.
and is conducted to a highly doped $p^+$ region. The shown layout represents a SOI switch transistor, the bulk-MOSFET does not have a body contact in close proximity to the transistor diffusion, but rather far away from the transistor and is common to all devices. The $R_{on}C_{off}$ product of a single transistor can be optimized using additional metal layers and design topologies. The simulated $R_{on}C_{off}$ products for different layout implementations are presented in Fig. 4.9. The total $R_{on}$ and $C_{off}$ of a single transistor vary with the used metal stacks. The total gate width of the transistor has to be minimized if tapered metal layers are used in the transistor design to achieve the equal layout dimensions. The best $FOM$ shows the RF MOS transistor using tapered metal fingers with 40% coverage over the active transistor area. The transistor with tapered metal and additional thick metal layer over drain and source provides lower $R_{on}$. Adding more metal layers to the drain-source regions will reduce the total $R_{on}$ of the transistor. On the other hand, the $C_{off}$ will increase since the stacking of metal layers increases the total capacitance. The $R_{on}$ and $C_{off}$ of a single transistor are in trade-off and can be influenced by the layout structure as shown in Fig. 4.9.
Figure 4.9: Simulated $R_{on}C_{off}$ product of a single RF MOSFET for several layout designs.
5 Design and Layout of High-Voltage RF Switches

In this chapter the general architecture of a high-voltage RF switch in terms of stacking, ESD protection, biasing and layout is presented. Furthermore, the influence of the substrate capacitance on the stacked device and in-depth linearity analysis of high-voltage RF switches based on delta-terms is discussed.

5.1 Design Aspects of High-Voltage RF Switches

Since the antenna aperture tuning switch is exposed to high RF voltage levels, RF switches are composed of highly stacked series RF MOSFETs as shown in Fig. 5.1. The number $N$ of the stacked devices is linearly proportional to the maximum RF voltage handling $V_{RF,max}$ and influences the total $R_{on}$ and $C_{off}$, since these parameters are scaled according to the number of stacked devices. The total $R_{on}$ and $C_{off}$ are given in Eq. (5.1) and (5.2).

$$R_{on,\Sigma} = R_{on}N \tag{5.1}$$

$$C_{off,\Sigma} = \frac{C_{off}}{N} \tag{5.2}$$

As $R_{on}$ and $C_{off}$ are linearly scaled with the transistor width, the $R_{on}C_{off}$ ratio remain theoretically constant (in first approximation) and is independent from the stack size and transistors width. However, the $R_{on}C_{off}$ ratio of products is higher due to routing, packaging, and PCB parasitic.

On the application level the aperture tuning circuits are grouped in two classes with different requirements and design trade-offs. Antenna tuning close to the feed or low-ohmic tuning requires mid-voltage handling tag (MV) devices, designed for RF voltage levels of around 40 V. The high-voltage handling tag (HV) device are utilized at the high-ohmic aperture tuning plane and designed for RF peak voltages exceeding 80 V [92]. As the MV device is designed for a maximum voltage handling capability of 40 V the required stack size is halved compared to HV devices. For providing the same $R_{on}C_{off}$ the HV device occupies four times larger silicon area than a MV device [88]. The antenna tuning switch trade-offs regarding $R_{on}$, $C_{off}$ and $V_{RF,max}$ are summarized in Fig. 5.2. The optimization of $R_{on}$ is performed by increasing the width and reducing the stack size. On the other hand, the $C_{off}$ will increase. The voltage handling, meaning $V_{RF,max}$ improves with increasing stack size.
The equivalent circuits in the off- and on-states are depicted in Fig. 5.1. In off-state the device is represented by $C_{\text{off}}$ and $R_{\text{off}}$, whereas in on-state the switch is modeled by $R_{\text{on}}$. Typical values for $R_{\text{on}}$ are in the range of 1 Ω for MV and 2 Ω for HV devices. $C_{\text{off}}$ varies from 200 fF to 140 fF and typical $R_{\text{off}}$ value is in the vicinity of 30 kΩ at 1 GHz for both voltage handling classes. $R_{\text{off}}$ has a frequency dependent behavior and gets lower with the increasing frequency. The bias network in high-voltage RF switches impacts the operating parameters such as cutoff frequency, switching speed, the uniformity of the RF voltage distribution and losses in the bias circuit. There are several bias topologies known in the art. The choice of the bias topology depends on the required specification, available bias supplies, power handling capability, switch architecture, and fabrication process [93]. Two widespread bias circuit topologies for RF switches are shown in Fig. 5.3. In the star-topology each RF MOSFET has a gate resistor connected between the gate and common bias supply. The drain resistor shorts the drain region as well as the shared drain-source regions of the FETs to ground. Each body connection of the RF MOSFETs is connected via a high-ohmic substrate resistance to the common substrate bias as shown in Fig. 5.3(a). In the series bias topology, the switch is biased via gate-to-gate, drain-to-source, and body-to-body resistors according to Fig. 5.3(b). The resistors $R_{G}$, $R_{D}$, $R_{DS}$ and $R_{\text{sub}}$ share the same values. During the off-state operation the voltage drop on the drain-gate should be the same as the voltage on the gate. Therefore, the gate resistor $R_{G}$ is chosen as high as possible. High values of the gate resistor reduce the power dissipation.
5.1 Design Aspects of High-Voltage RF Switches

of the monolithic switch sacrificing the switching time. A high ohmic body resistor is required to catch a part of the RF amplitude and to prevent the body effect in on-state. The drain or drain-source resistor defines the DC bias drain-source voltage. Another important point is, that GIDL and gate-induced source leakage (GISL) must be considered, while sizing the resistor values since GIDL changes the operating point of the RF MOSFET at high RF voltage excitations. The biasing resistors ranges from 5 kΩ to 50 kΩ for series – and 50 kΩ to 1 MΩ for star-biasing depending on the application requirements.

A layout of an n-stack high-voltage switch including bias circuitry and corresponding circuit diagram is portrayed in Fig. 5.4. The switch is biased with poly resistors. The body resistors are connected to a highly doped p+ region typically with the bottom metal layer. The gate contact is created by a via to the first metal layer. The drain-source resistor can be connected to the drain and source fingers of the RF MOSFET as depicted in Fig. 5.4. High-voltage RF switches can also be implemented as series switches by adding a second RF port. They require a dedicated ESD protection by the auxiliary shunt switch. Adequate ESD protection is mandatory in high-voltage RF switches due to the industry ESD compliance level of above 1 kV HBM \[10\]. The RF pins of the off-state RF switches are protected by shunt off-state ESD RF switches, whereas digital and supply pins are protected by diodes as shown in Fig. 5.5(a)

Figure 5.3: RF switch with (a) star-biasing and (b) series-biasing.
Figure 5.4: Layout of a shunt high-voltage RF switch including series bias topology.

Figure 5.5: ESD protection circuits for (a) RF pins and (b) digital/supply pins.

and Fig. 5.5(b) respectively. In terms of ESD protection, the shunt RF switch is more appropriate since it protects itself and requires no dedicated ESD protection, meaning the shunt switch provides the most efficient use of silicon area and does not degrade the RF characteristics of the switch. Series RF switch requires one dedicated ESD protection circuit in shunt.
5.2 Influence and Modeling of the Substrate Capacitance

As the RF switch transistors are stacked, the influence of the substrate capacitance $C_{\text{sub}}$ becomes of paramount importance for high-voltage RF switches and affects the uniformity of the voltage division in the stack, even-order non-linear products, power, and voltage handling capability of the switch [94]. The RF switch can be represented by rectangular shapes indicating the individual transistors in the stack as depicted in Fig. 5.6 [95].

![Figure 5.6: Layout of a high-voltage RF switch deposited on a high-ohmic substrate material.](image)

The substrate capacitance between the switch cells and ground is formed by an electrical field penetrating through the high-ohmic substrate, which serves as an insulator with the relative permittivity of $\varepsilon_{r,\text{Si}} = 11.65$ at room temperatures and frequencies below 10 GHz, when the switch is excited by an RF voltage. The ground plane implicates, for example, a conductive sheet of an application board [95]. $C_{\text{sub}}$ can be determined with a 3D-EM simulation or an analytical evaluation based on microstrip transmission line models. Three possible approaches for the analytical calculation are the microstrip transmission line models by Wheeler, Schneider and Hammerstad-Jensen [96], [97], [98].

5.2.1 Model of Substrate Capacitance Inspired by Inverted Microstrip Line

The direct measurement of $C_{\text{sub}}$ is usually very challenging and prone to errors, especially for ICs flip-chip mounted on an evaluation PCB. In this section a simple calculation model based on microstrip transmission line model for estimating the substrate capacitance of wire-bonded and flip-chip RF switches is presented. The models are evaluated numerically and compared with EM simulations. The capacitor values are verified on a hardware demonstrator [95].
Microstrip Transmission Line Models

First, we consider the cross-section for a generic wire-bonded (face-up mounted) and flip-chip bonded (face-down mounted) RF switch ICs on a dielectric substrate as portrayed in Fig. 5.7 [95]. Fig. 5.7(a) illustrates the cross-section of a wire-bonded RF switch, where the switch is represented by the conductive layer deposited on the silicon substrate $[d_↑, \varepsilon_{r,\text{Si}}]$ on the infinite ground plane. $W$ is the width of the conductive layer and $d_↑$, $\varepsilon_{r,\text{Si}}$ are the thickness and relative permittivity of the silicon material. The switch is surrounded by a dielectric layer $\varepsilon_{r,↑}$ with infinite thickness.

![Figure 5.7: Generic stackup for (a) wire-bonded and (b) flip-chip RF switch.](image)

The surrounding dielectric layer might be a packaging material or air if the top of the IC is supposed to be open. Since the ratio of $d_↑$ to the total thickness of the front-end-of-line (FEOL) and BEOL portion of an RF switch IC is at least 50, the thickness of the conductive layer is negligible and assumed to be zero [95]. The dielectric stack of the face-down chip in Fig. 5.7(b) is flipped with respect to ground compared to the face-up mounted IC. The package material or PCB laminate on which the IC is flip-chip mounted is described by the dielectric layer $\varepsilon_{r,↓}$, where $d_↓$ is the thickness of the layer as shown in Fig. 5.7(b). The electrical and geometrical properties such as thickness, dielectric constants etc. of the dielectric layer in face-down mounted IC differs generally from the face-up setup. Since the dielectric constant of a package material or PCB laminate are substantially lower than the relative permittivity of silicon the assumption (5.3) holds true for almost all practical implementations [95]:

\[
\varepsilon_{r,↓} < \varepsilon_{r,\text{Si}} \quad \text{and} \quad \varepsilon_{r,↑} < \varepsilon_{r,\text{Si}} \quad (5.3)
\]

The calculation of the effective dielectric constant in the transmission line model depends on the configuration, because the ratio in dielectric constant of the insulating layers below and above the conductive switch stripe differences
between the flip-chip and wire-bonded IC and is discussed later in the dissertation [95]. Various computational models for microstrip transmission lines have been investigated in microwave engineering. In 1963, Wheeler introduced the analytical description of transmission line properties of parallel wide stripes based on conformal mapping technique. From this work, he has derived an analytical model describing the properties of a stripline on a dielectric sheet on a plane. $C_{\text{sub}}$ per unit length of the RF switch obtaining Wheeler’s formula is calculated as [96]:

$$
C_{\text{sub,W}} = \frac{4\pi\varepsilon_0\varepsilon_{\text{eff}}}{\ln \left[1 + \frac{1}{2} \frac{8d}{W} \left(\frac{8d}{W} + \sqrt{\left(\frac{8d}{W}\right)^2 + \pi^2}\right)\right]},
$$

(5.4)

where $W$ and $d$ are the dimensions of the respective layers as shown in the cross-sections in Fig. 5.7 and $\varepsilon_{\text{eff}}$ is the effective dielectric constant. Alternatively, the substrate capacitance considering Schneider [97] and Hammerstad-Jensen models is defined as follows [98]:

$$
C_{\text{sub,S}} = \begin{cases} 
\frac{2\pi\varepsilon_{\text{eff}}\varepsilon_0}{\ln \left(\frac{8d}{W} + \frac{W}{4d}\right)} & \text{if } \frac{d}{W} \leq 1 \\
\frac{\varepsilon_{\text{eff}}\varepsilon_0}{\frac{W}{d} + 2.42 - 0.44 \frac{d}{W} + \left(1 - \frac{d}{W}\right)^6} & \text{if } \frac{d}{W} > 1 
\end{cases}
$$

(5.5)

and

$$
C_{\text{sub,H}} = \frac{2\pi\varepsilon_{\text{eff}}\varepsilon_0}{\ln \left[f_u \frac{d}{W} + \sqrt{1 + \left(2 \frac{d}{W}\right)^2}\right]},
$$

(5.6)

where

$$
f_u = 6 + (2\pi - 6)e^{-\left(30.666 \frac{d}{W}\right)^{0.7528}}.
$$

(5.7)

The formulas (5.4) – (5.6) are valid to both face-down and face-up mounted models and the capacitance value is measured in F/m. As mentioned, the only parameter, which differs between face-down and face-up mounting is the effective dielectric constant $\varepsilon_{\text{eff}}$. 

Definition of the Effective Dielectric Constant

The effective dielectric constant of a wire-bonded switch calculated according to the formula for a standard microstrip transmission line is [97]:

\[
\varepsilon_{\text{eff},\uparrow} = \frac{\varepsilon_{r,\text{Si}} + \varepsilon_{r,\uparrow}}{2} + \frac{\varepsilon_{r,\text{Si}} - \varepsilon_{r,\uparrow}}{2} \left(1 + \frac{10d_{\uparrow}}{W}\right)^{-\frac{1}{2}}.
\] (5.8)

However, the formula (5.8) is not valid for the flip-chip switch configuration, since only a minor fraction of the electric field lines penetrates through the silicon material over the switch [97]. The flip-chip configuration is comparable to standard inverted microstrip transmission line. Therefore, the C_{sub} calculation of flip-chip mounted devices is performed by applying quasi-static model for the inverted microstrip line. A comprehensive study about this type of transmission line can be found in literature [99]. The effective dielectric constant for a face-down mounted switch according to [99] is defined as:

\[
\varepsilon_{\text{eff},\downarrow} = \left(\sqrt{\varepsilon_{r,\downarrow}} + \sqrt{\varepsilon_{r,\text{Si}} - \sqrt{\varepsilon_{r,\downarrow}}} c_0 + (W/d_{\downarrow}) c_1\right)^2,
\] (5.9)

where

\[
c_0 = 2.359 - 0.097 \ln \varepsilon_{r,\text{Si}} - 0.00577 \ln^2 \varepsilon_{r,\text{Si}} + 0.0114 \ln^3 \varepsilon_{r,\text{Si}} + [0.04856 - 0.03408 \ln \varepsilon_{r,\text{Si}} + 0.15296 \ln^2 \varepsilon_{r,\text{Si}} - 0.02418 \ln^3 \varepsilon_{r,\text{Si}}] (d_{\downarrow}/t_{\downarrow}) \]

(5.10)

\[
c_1 = 0.219 - 0.253 \ln \varepsilon_{r,\text{Si}} + 0.208 \ln^2 \varepsilon_{r,\text{Si}} - 0.027 \ln^3 \varepsilon_{r,\text{Si}} + [0.915 + 0.338 \ln \varepsilon_{r,\text{Si}} - 0.253 \ln^2 \varepsilon_{r,\text{Si}} + 0.04 \ln^3 \varepsilon_{r,\text{Si}}] (d_{\downarrow}/t_{\downarrow}).
\]

(5.11)

All practical use cases are covered by the model, which is applicable for dielectric constant values of up to 20 and does not break at \(W = d_{\downarrow}\).

Numerical Evaluation of the Models

The material stack parameters for the numerical evaluation of the models (5.4) – (5.6) together with (5.8) – (5.9) are summarized in Table 5.1 and are given by the available options for the hardware implementation. Dielectric layers with a constant permittivity in the range between 1 and 4 and thicknesses starting of up to 1000 μm may occur in other practical applications [95]. The numerical evaluation of the capacitance per 1 μm layout length over the layout width \(W\) according to the models provided in (5.4) – (5.6) are plotted in Fig. 5.8. The curves of the wire-bonded and flip-chip configuration are in overall equal with the average difference below 0.6% and 0.7%, respectively.
Table 5.1: Material stack parameters for the numerical evaluation of the models.

<table>
<thead>
<tr>
<th></th>
<th>d</th>
<th>$\varepsilon_r$</th>
<th>$\varepsilon_{r,\text{Si}}$</th>
<th>t</th>
</tr>
</thead>
<tbody>
<tr>
<td>flip-chip</td>
<td>200 µm</td>
<td>3.4</td>
<td>11.65</td>
<td>200 µm</td>
</tr>
<tr>
<td>wire-chip-bonded</td>
<td>750 µm</td>
<td>1</td>
<td>11.65</td>
<td>$\infty$</td>
</tr>
</tbody>
</table>

Figure 5.8: Numerical versus EM simulation results of the substrate capacitance models for (a) flip-chip and (b) wire-bonded stacks.

The numerical evaluation is compared with an EM simulation in Sonnet Light and a free electromagnetic field solver OpenEMS [100]. The difference between the capacitance curve obtained from the EM simulations and the calculated curves is below 8.7% for the wire-bonded and 3.5% for the flip-chip configuration. Despite the simplicity of the material stack of an RF switch and strong abstraction the calculation of the substrate capacitance based on transmission line model represents all first-order substrate capacitive coupling effect reasonably well and satisfies practical RF switch engineering requirements within practical tolerances. A full 3D EM simulation is recommended, if more accurate modeling is required [95].

Verification of the Presented Models

The RF breakdown voltage $V_{RF,\text{BR}}$ of an RF switch is a suitable criteria to verify the substrate models (5.4) – (5.6). The $V_{RF,\text{BR}}$ is sensitive to $C_{\text{sub}}$ variations and the measurement setup for evaluating the breakdown voltage is well known.
$V_{RF,BR}$ of the stacked switch is defined by $C_{\text{sub}}$ together with the drain-source capacitance $C_{ds}$ of a MOS transistor [94]:

$$V_{RF,BR} = \sqrt{\frac{C_{ds}}{C_{\text{sub}}}} \frac{\sinh (2N\alpha)}{\cosh((2N-1)\alpha)} V_{\text{ds,max}}, \quad (5.12)$$

where $V_{\text{ds,max}}$ describes the breakdown voltage of the individual transistors in the stack and $\alpha = \text{arsinh} \left( \frac{1}{2} \sqrt{\frac{C_{\text{sub}}}{C_{ds}}} \right)$. For the verification of the numerical evaluation of the presented models a test chip comprising an RF switch has been designed in Infineon 130 nm RF switch bulk-CMOS technology. The RF switch is constructed from $N_{\text{stk}} = 28$ identical MOS transistors in series and DC biased as shown in Fig. 5.9(a). All transistors in the stack have the same $W/L = 7 \text{ mm}/120 \text{ nm}$ and the resistors are sized as $R_{G,C} = 20 \text{ k}\Omega$, $R_G = 300 \text{ k}\Omega$ and $R_D = 600 \text{ k}\Omega$. The breakdown voltage of the RF switch is determined by the measurement of the third harmonic of an off-state RF switch. The equivalent circuit including $C_{\text{sub}}$ to ground of the switch in off-state is shown in Fig. 5.9(b) and the fabricated IC is depicted in Fig. 5.9(c). The effective drain-source capacitance of the switch is $C_{ds} = 2.45 \text{ pF}$ and the breakdown voltage is 2.5 V [95].

![Figure 5.9](image.png)

**Figure 5.9:** (a) Circuit diagram, (b) corresponding equivalent circuit and (c) die photograph of the manufactured RF switch IC.

The total layout size of the designed IC is $W \times L = 200 \times 620 \mu\text{m}^2$, wherein a single transistor occupies $W \times \Delta L = W \times L/N_{\text{stk}} = 200 \times 22.14 \mu\text{m}^2$. The wire-bonded configuration is represented by a measurement setup, where the IC on a 750 $\mu$-thick wafer has been measured on an RF probe station. The handle wafer has been face-up attached on a metal chuck of the probe station, which represents the ground in the wire-bonded stack. For the flip-
chip configuration a 200 µm-thick diced IC has been flip-chip mounted on a multi-layer PCB for measurements. The RF layer of the board is constructed from a 200 µm-thick Rogers RO4003C laminate material and the bottom metal layer is used as an RF ground. Since the nominal relative permittivity for the RO4003 laminate is 3.4, such setup represents the flip-chip configuration. The numerical parameters for evaluation of the $C_{\text{sub}}$ and corresponding breakdown voltage are listed in Table 5.2 [95].

Table 5.2: Numerical evaluation of the substrate capacitance and breakdown voltage for the wire-bonded and flip-chip configuration.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$d$</th>
<th>$t$</th>
<th>$C_{\text{sub}}$</th>
<th>$V_{RF,\text{BR}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>flip-chip</td>
<td>200 µm</td>
<td>200 µm</td>
<td>2.92 fF</td>
<td>54.8 V</td>
</tr>
<tr>
<td>wire-chip-bonded</td>
<td>750 µm</td>
<td>∞</td>
<td>2.61 fF</td>
<td>56.0 V</td>
</tr>
</tbody>
</table>

The measurement results of the third harmonics of an off-state RF switch in wire-bonded and flip-chip configuration are demonstrated in Fig. 5.10. The third harmonics have been measured at the $RF_2$ terminal of the off-state switch. The breakdown voltage is demonstrated by the abrupt jump of the third harmonic power level and shows maximum voltage handling values of 55.4 V and 51.4 V for the wire-bonded and flip-chip configurations respectively. The voltage difference of the estimated design is 0.6 V and 3.4 V, which indicates an error in the effective $C_{\text{sub}}$ calculation of 7% and 24%, respectively. The lower measured breakdown voltage relies on the fact that the ground lines running in parallel to the switch layout, which increases the effective $C_{\text{sub}}$. Moreover, the models do not consider any PCB wiring [95].

5.2.2 Influence on the Voltage Distribution along the Stack

The substrate capacitance influences especially the uniformity of the voltage division in the stack and even-order nonlinear products. The latter is discussed in the next section. It causes an imbalance of the voltage distribution along the stack and gets stronger with increasing $C_{\text{sub}}$. A detailed equivalent circuit of an off-state RF switch including node voltages, current and $C_{\text{sub}}$ is drawn in Fig. 5.11(a). By applying Kirchhoff’s law at each node, it becomes apparent, that the transistor connected close to the RF source (also called RF hot side), sees the highest voltage along the stack, while the lowest voltage drops at the transistor close to the grounded side (also called cold side) of the RF switch. The voltage distribution along the stack is obtained by Eq. (5.13) [94]:

\begin{equation}
51
\end{equation}
Figure 5.10: RF breakdown voltage measurement results.

Figure 5.11: (a) Equivalent circuit of an off-state RF switch including the voltage distribution at each MOSFET and (b) voltage distribution along the stack.

\[
V_{\text{ds},i} = \sqrt{\frac{C_{\text{sub}}}{C_{\text{off}}} \frac{\cosh\left((2(i - 1) + 1)\alpha\right)}{\sinh(2N\alpha)}} V_{\text{RF,peak}}, \quad (5.13)
\]

where \( i \) is the \( i \)-th MOSFET in the stack and \( N \) is the stack size of the RF switch. The simulated and calculated voltage distribution for the wire-bonded RF switch with 28 stacked MOSFET, \( C_{\text{sub}} = 2.95 \text{ fF} \) and \( V_{\text{RF,peak}} = 54.8 \text{ V} \) is portrayed in Fig. 5.11(b). The simulation using a standard circuit simulation...
tool and calculations are exactly the same. Due to the imbalanced RF switch, the first transistor located at the hot side operates near or at the breakdown voltage of the device, when the RF switch is excited by moderate RF voltages. Accordingly, the voltage handling capability of an RF switch is directly related to $C_{\text{sub}}$ and can be improved by equalization techniques, which is performed by capacitors connected at each drain-source of the transistor according to Fig. 5.12(a). The equalization capacitances $C_{\text{eq},i}$ can be derived using textbook linear network analysis assuming that after equalization the voltage drop $V_{\text{ds}}$ at each MOSFET in the stack is the same [101]. The values of the capacitors decrease from hot side toward the cold side of the RF switch as plotted in Fig. 5.12(b) and is calculated by Eq. (5.14) [101]:

$$C_{\text{eq},i} = \frac{i(i-1)}{2}C_{\text{sub}}.$$  \hspace{1cm} (5.14)

After equalization, the voltage distribution along the stack is constant (see Fig. 5.12(b)), meaning that all transistors are exposed to $54.8 \text{ V}/N = 1.97 \text{ V}$, which is below the RF breakdown voltage of a single transistor, thus enabling the increase of power at the input by about 30%.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{5.12.png}
\caption{(a) Equalized RF switch and (b) balanced voltage distribution.}
\end{figure}
5.3 Linearity Analysis of High-Voltage RF Switches

Even moderate TX power levels may generate high peak RF voltages along the antenna. When the antenna is fed with the maximum available power, RF voltage peaks of up to 80 V occurs along the antenna. Since the RF switches in aperture tuning systems are directly attached to the build-in antenna, such operation conditions produce high nonlinear distortions at aperture tuners that cannot be simply suppressed or filtered out [88]. The linearity of MOSFET-based RF switches is particularly influenced by the semiconductor material, nonlinear parasitic elements along the channel of an intrinsic transistor and the unbalanced voltage division in the stack [102], [103]. As mentioned, the even-order nonlinear products are in general generated by the nonlinear substrate capacitance $C_{\text{sub}}$ and the overlap capacitances $C_{gs}, C_{gd}$ together with the drain-source capacitance $C_{ds}$ contribute to the odd-order nonlinearities in the I-V response of the RF switch. Another contributor especially to the third-order nonlinear products is the unequal RF voltage distribution along the stack of MOSFETs in the switch, which is explained by the fact that the third-order term grows cubically with the applied voltage, thus adding more distortions at high-voltage levels than reducing the distortion at comparable lower voltage levels [104]. A possible approach to minimize the influence of the mentioned effect is using equalization techniques. In this section the second- and third-order nonlinear products are analyzed assuming that the switch is in shunt configuration as shown in Fig. 5.13, where the individual transistors in the stack are represented by the rectangular cells.

![Figure 5.13: Schematic and corresponding layout of a stacked RF switch.](image-url)
When the switch is excited by a sinusoidal voltage signal $V_{RF}(t)$ the nonlinear voltage-to-current response is described by a polynomial function [105]:

$$I(t) = \sum_{i=0}^{M} \alpha_i V_{RF}^i(t). \tag{5.15}$$

The order $M$ of the polynomial function is limited to 3 and the resulting relevant nonlinear components for the analytical description are listed in Table 5.3 [104].

**Table 5.3**: Relevant nonlinear components for single- and two-tone harmonic excitation [104].

<table>
<thead>
<tr>
<th>Excitation $V_{RF}(t)$</th>
<th>Nonlinear Components</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RF, pk} \cos(\omega t)$</td>
<td></td>
</tr>
<tr>
<td>$V_{RF, pk} \cos(\omega_1 t) + V_{RF, pk} \cos(\omega_2 t)$</td>
<td></td>
</tr>
<tr>
<td>IMD$_2$</td>
<td>$\omega_1 \pm \omega_2$</td>
</tr>
<tr>
<td>IMD$_2$</td>
<td>$\omega_2 \pm \omega_1$</td>
</tr>
<tr>
<td>IMD$_3$</td>
<td>$2\omega_1 \pm \omega_2$</td>
</tr>
<tr>
<td>IMD$_3$</td>
<td>$2\omega_2 \pm \omega_1$</td>
</tr>
</tbody>
</table>

The level of the nonlinear distortion for the RF switch as a whole is determined by the first-order factors $\alpha_2$ and $\alpha_3$, where:

- $\alpha_2$ is depended on the nonlinear substrate capacitance $C_{\text{sub}}$ and is therefore proportional to the total layout area $F$ of the switch: $\alpha_2 \sim F$ [102].
- $\alpha_3$ is proportional to the width $W$ of the individual transistors in the stack: $\alpha_3 \sim W$.  

55
A low-voltage (LV) and high-voltage (HV) switch, designed for 40 V and 80 V handling, is considered for the analytical description. They are proportionally scaled in terms of stack and width providing identical series $C_{\text{off}}$ and $R_{\text{on}}$. The predictions of the nonlinear products are demonstrated in delta-terms based on the given nonlinear performance of a reference structure and are split in first- and second-order models. In the first-order model the RF switch is considered as a whole, whereas the second-order model accounts for the individual MOSTEs in the stack. The $C_{\text{sub}}$ of each individual transistor is calculated with Schneider’s microstrip transmission line model and an equalization error is added to the respective MOSFETs in the stack [104].

5.3.1 First-Order Model of 2$^\text{nd}$ and 3$^\text{rd}$ Order Nonlinearities

The difference between the HV- and LV-switches in terms of second and third harmonics can be described considering Fig. 5.14. The HV RF switch in Fig. 5.14(b) has double stack size and is constructed from twice wider transistors compared to the LV switch as shown in Fig. 5.14(a).

Since the factor $\alpha_2$ is directly proportional to the total layout area of the RF switch, it becomes apparent that:

$$\alpha_2^{(HV)} = 4\alpha_2^{(LV)},$$

(5.16)

where $\alpha_2^{(LV)}$ and $\alpha_2^{(HV)}$ are the second-order polynomial factors for the LV and HV switches, respectively. The third-order polynomial factor can be observed
5.3 Linearity Analysis of High-Voltage RF Switches

by Fig. 5.14(c). The HV switch is divided into four uniform cells, where each cell is equal to the LV switch and sharing the same odd-asymmetry factor [88]:

\[ \alpha_3^{(HV)} = \alpha_3^{(LV)}. \]  (5.17)

The ratio in terms of power between the second and third harmonics for two RF switches excited by the same RF voltage \( V \) can be described using Fig. 5.14(a) and Fig. 5.14(c):

\[ \Delta H_2 = H_2^{(HV)} - H_2^{(LV)} = 10 \log_{10} \left( \frac{4 \alpha_2^{(LV)} V^2}{\alpha_2^{(LV)} V^2} \right) = 6 \text{ dB} \]  (5.18)

\[ \Delta H_3 = H_3^{(HV)} - H_3^{(LV)} = 10 \log_{10} \left( \frac{2 \alpha_3^{(LV)} \left( \frac{V}{2} \right)^3}{\alpha_2^{(LV)} V^3} \right) = -6 \text{ dB}. \]  (5.19)

The first-order assumption reveals that the HV switch is expected to exhibit 6 dB stronger second harmonic, since the occupied silicon area is four times large compared to the LV device. On the other hand, the third harmonic is reduced by 6 dB, because the voltage drop on each transistor is halved [88].

5.3.2 Second-Order Model of 2\textsuperscript{nd} and 3\textsuperscript{rd} Order Nonlinear Products

In the second-order model the individual transistors in the stack are considered, which increases the accuracy of the model. Further, a scaling factor \( \rho \) that defines the layout size and stacking ratio between the LV and HV switches is introduced:

\[ W^{(HV)} = \rho W^{(LV)}, \quad L^{(HV)} = \rho L^{(LV)}, \quad N^{(HV)} = \rho N^{(LV)}, \]  (5.20)

where \( W, L \) are the total layout width and length of the RF switch and \( N \) is the number of MOSFETs in the stack. The following sections focus on the harmonics as a parameter for analysis. The investigations are mapped to intermodulation products, since they depend on the same set of parameters and vary by the constant scaling coefficients [104].
Description of the Second-Order Nonlinear Products

The second harmonic of an RF switch with \( N \) stacked MOSFETs can be expressed as the sum over all stacked MOSFETs:

\[
H_2 = 10 \log \left[ \sum_{i=1}^{N} \beta_{2,i} V_{d,i}^2 \right] = 10 \log \left[ \sum_{i=1}^{N} \beta_{2,i} \left( \frac{i V_{RF,pk}}{N} \right)^2 \right],
\]

(5.21)

where \( V_{d,i} \) is the drain voltage of the \( i \)-th MOSFET with respect to ground. The nonlinearities of an individual transistor in the switch branch are described by the factor \( \beta_{2,i} \). The polynomial factor \( \alpha_2 \) of the first-order model can be mapped to its counterpart \( \beta_2 \) by the Eq. (5.22) \[104\].

\[
\frac{\alpha_2}{2} = \sum_{i=1}^{N} \beta_{2,i} \left( \frac{i}{N} \right)^2.
\]

(5.22)

The factor \( \beta_{2,i} \) is directly proportional to the substrate capacitance \( C_{\text{sub},i} \) of the \( i \)-th transistor in the stack.

\[
\beta_{2,i} \sim C_{\text{sub},i}.
\]

(5.23)

Schneider’s model for calculating the substrate capacitance of an individual transistor in the stack is used for the second-order analytical description of the second nonlinear products:

\[
C_{\text{sub}}(w, l) = \begin{cases} 
2 \pi \varepsilon_0 \varepsilon_{\text{eff}} l \ln \left( \frac{8h}{w} + \frac{w}{4h} \right), & \frac{w}{h} \leq 1 \\
\varepsilon_0 \varepsilon_{\text{eff}} \left[ \frac{w}{h} + 2.42 - 0.44 \frac{h}{w} + \left( 1 - \frac{h}{w} \right)^6 \right], & \frac{w}{h} > 1,
\end{cases}
\]

(5.24)

where \( h \) is the silicon substrate thickness, \( w \) and \( l \) are the layout width and length of a single MOSFET in stack. The effective dielectric constant \( \varepsilon_{\text{eff}} \) can be calculated with the formula for wire-bonded configuration (5.8) or flip-chip configuration (5.9). Schneider’s model does not take the fringing capacitance \( C_{\text{fd}} \) along the feed line into account. The single-sided fringing capacitance is included by a stand-alone conductive stripe sized as the first transistor as shown in Fig. 5.15. Eq. (5.24) provides the total capacitance of the stripe along the width \( W \) if the arguments of the function \( C_{\text{sub}}(w, l) \) is set to \( w = L/N \) and \( l = W \). The fringing capacitance along the feed line is extracted through the
5.3 Linearity Analysis of High-Voltage RF Switches

Figure 5.15: Electrical field and substrate capacitances of an RF switch including the section for calculating the fringing capacitance at the feed edge.

The total capacitance and the brick capacitance $C_{pp,N}$. The brick capacitance can be calculated with the parallel-plate capacitance model [104]:

$$C_{pp,N}(w, l) = \varepsilon_0 \varepsilon_r \frac{wl}{h}, \quad (5.25)$$

where the arguments are set as $w = W$ and $l = L/N$. According to Fig. 5.15 the total capacitance under the stripe is formed by the brick capacitance $C_{pp,N}$ and $2C_{fd}$, from which the necessary fringing capacitance $C_{fd}$ can be derived as [104]:

$$C_{fd}(w, l) = \frac{1}{2}(C_{sub}(l, w) - C_{pp,N}(w, l)). \quad (5.26)$$

The factor $\beta_{2,i}$ of the $i$-th transistor in stack determining the second-order nonlinear product is formed to:

$$\beta_{2,i} \sim \begin{cases} 
C_{sub}\left(W, \frac{L}{N}\right), & i < N \\
C_{sub}\left(W, \frac{L}{N}\right) + C_{fd}\left(W, \frac{L}{N}\right), & i = N 
\end{cases} \quad (5.27)$$

The formula (5.21) can be transformed with the formulas (5.26), (5.27) and $\sum_{i=1}^{N} i^2 = N(N + 1)(2N + 1)/6$ to:

$$H_2 \sim 10 \log \left[ V_{RF,pk}^2 \left( \frac{C_{sub}\left(W, \frac{L}{N}\right)}{N^2} \sum_{i=1}^{N} i^2 + C_{fd}\left(W, \frac{L}{N}\right) \right) \right] \sim \quad (5.28)$$
~ 10 \lg \left( V_{RF, pk}^2 \left( \frac{(N + 1)(2N + 1)C_{sub}(W, \frac{L}{N})}{6N} + C_{fd}(W, \frac{L}{N}) \right) \right).

Similar to the first-order model, the ratio in terms of power between the second-order nonlinear products of the high-voltage as well as low-voltage switches, driven by the same RF voltage is described as:

\[ \Delta H_2 = H_2^{(HV)} - H_2^{(LV)} = \]
\[ = 10 \lg \left( \frac{(\rho N + 1)(2\rho N + 1)C_{sub}(\rho W, \frac{L}{N}) + 6\rho NC_{fd}(\rho W, \frac{L}{N})}{\rho(N + 1)(2N + 1)C_{sub}(W, \frac{L}{N}) + 6\rho NC_{fd}(W, \frac{L}{N})} \right). \] (5.29)

Last but not least, \( C_{fd} \) can be neglected for large \( N \) and Eq. (5.29) can be simplified to [104]:

\[ \Delta H_2 \approx 10 \lg \left( \frac{\rho C_{sub}(\rho W, \frac{L}{N})}{C_{sub}(W, \frac{L}{N})} \right). \] (5.30)

Description of the Third-Order Nonlinear Products

The odd components in the nonlinear response of the RF switch i.e., third-, fifth-, etc. order products, are formed by the parasitic capacitances \( C_{gs}, C_{gd} \) and \( C_{ds} \) parallel to the channel. Also, the subthreshold and leakage currents in the channel of the transistor contribute to odd asymmetry of the series switch path. The parasitic capacitances are proportional to the width of the MOSFET, thus influencing the factor \( \beta_3 \) of the third-order nonlinear component as follows [104]:

\[ \beta_3 \sim W, \] (5.31)

where \( \beta_3 \) describes the coefficient of the polynomial function of the second-order model and is equal to \( \alpha_3 \) in (5.15): \( \beta_3 = \alpha_3 \). In order to distinguish clearly between the first- and second-order model the variable \( \beta_3 \) will be used for further derivation. Moreover, it is assumed that equalization technique is applied to the RF switch. First, we consider a perfectly equalized RF switch, where the RF current flow into the substrate is solely taken from the equalization capacitors, resulting in a simplified equivalent circuit of the RF switch with perfectly equalized voltage distribution as shown in Fig. 5.16(a). Subsequently, the third harmonic can be expressed as [104]:

[5 Design and Layout of High-Voltage RF Switches]
5.3 Linearity Analysis of High-Voltage RF Switches

\[ H_3 = 10 \log \left( \frac{\beta_3}{4} \left[ \frac{V_{RF, pk}}{N} \right]^3 \right), \]

or given (5.31) as:

\[ H_3 \sim 10 \log \left( \frac{W}{4} \left[ \frac{V_{RF, pk}}{N} \right]^3 \right). \]

However, it is practically impossible to accomplish a perfectly equalized voltage distribution in actual hardware due to inaccuracy of simulation models and fabrications process variations. The voltage equalization errors are modeled by the capacitances \( C_{\epsilon_i} \), coupled in parallel to the stack as portrayed in Fig. 5.16(b). The voltage drop at the individual transistors in the stack is defined as \( V_{RF, pk}/N (1 + \epsilon_i) \), where \( \epsilon_i \) is the equalization error coefficient fulfilling the condition [104]:

\[ \sum_{i=1}^{N} \epsilon_i = 0. \]

This is required to ensure that the sum of voltages at all transistors in stack remains equal to \( V_{RF, pk} \). Since \( \epsilon_i \) is not related to the stack configuration and does not collate with \( \rho \), the equalization error is distinguished by high- and

Figure 5.16: (a) Simplified equivalent circuit of a perfectly equalized RF switch and (b) equivalent circuit of an RF switch with equalization errors.
low-voltage switches as $\epsilon_i^{(HV)}$ and $\epsilon_i^{(LV)}$ respectively. The third harmonic of the not perfectly equalized RF switch depends on the voltage deviation at each individual transistor in the stack and can be written as:

$$H_3 \sim 10 \log \left[ \frac{W}{4} \left( \frac{V_{RF, pk}}{N} \right)^3 + \frac{W}{4} \sum_{i=1}^{N} \left( \frac{\epsilon_i V_{RF, pk}}{N} \right)^3 \right], \quad (5.35)$$

where the term $\epsilon_i V_{RF, pk}/N$ is the error voltage at the $i$-th element in the stack. The ratio of the third harmonics in terms of power between the high- and low-voltage switch driven by the same RF voltage $V_{RF, pk}$ is calculated by Eq. (5.36) [104]:

$$\Delta H_3 = H_3^{(HV)} - H_3^{(LV)} =$$

$$= 10 \log \left[ \frac{\rho W}{4} \left( \frac{V_{RF, pk}}{\rho N} \right)^3 + \frac{\rho W}{4} \sum_{i=1}^{N} \left( \frac{\epsilon_i^{(HV)} V_{RF, pk}}{\rho N} \right)^3 \right]. \quad (5.36)$$

After simplification Eq. (5.36) transforms to:

$$\Delta H_3 = 10 \log \left[ \frac{1}{\rho^2} \left( 1 + \frac{\rho N}{\sum_{i=1}^{N} \left( \epsilon_i^{(HV)} \right)^3} \right) \right]. \quad (5.37)$$

The first-order model can be obtained by setting $\epsilon_i = 0$, resulting in $\Delta H_3 = -6$ dB.

### 5.3.3 Numerical Evaluation of Second and Third Harmonics Ratio

For numerical evaluation of the second and third harmonic power ratio two RF switches were designed with the parameters listed in Table 5.4.

| Table 5.4: Layout dimensions and stack of the designed RF switches. |
|-------------------|-------|-------|-------|
|                   | $W$   | $L$   | $N$   |
| Low-voltage switch| 110 µm | 330 µm | 17    |
| High-voltage switch ($\rho \approx 2$) | 225 µm | 640 µm | 32    |
5.3 Linearity Analysis of High-Voltage RF Switches

As a reference, the low-voltage switch is chosen for the numerical evaluation and the substrate thickness is set to $h = 200 \, \mu m$. Since the switches are proportionally scaled in terms of stack and width, the high-voltage switch has double the layout width, length and stacking resulting in a scaling factor of $\rho \approx 2$. For the evaluation of Eq. (5.37) the equalization error function $\epsilon_i$ has to be defined. In a straightforward embodiment, $\epsilon_i$ is a hyperbolic sine/cosine function as described in Section 5.2.1. For the sake of simplicity $\epsilon_i$ is set to a quadratic function, which estimates a monotonic error progression in the values of the equalization capacitors. It should be noted that $\epsilon_i$ can be any function including non-monotonic functions [104].

$$
\epsilon_i = \kappa \left[ \frac{i^2}{N^2} - \frac{1}{N} \sum_{k=1}^{N} \frac{k^2}{N^2} \right] = \kappa \left[ \frac{i^2}{N^2} - \frac{(N+1)(2N+1)}{6N^2} \right].
$$

(5.38)

The second term in the brackets defines the mean value of the quadratic function satisfying the condition (5.34). The minimum and maximum values of Eq. (5.38) are limited by the scaling coefficient $\kappa$, which specifies the strength of the voltage unbalance in the stack:

$$
\epsilon_N - \epsilon_1 = \kappa.
$$

(5.39)

If $\kappa = 0$ the voltage drop at each transistor in the stack is equal, while $\kappa > 0$ results in an unbalanced voltage drop, where the MOSFET connected at the hot side of the switch is exposed to higher RF voltage than the MOSFET at the cold side. The numerical evaluation of Eq. (5.29) and Eq. (5.37) with the proposed error function are plotted over the scaling factor $\rho$ in Fig. 5.17. The effective dielectric constant $\varepsilon_{\text{eff}}$ is calculated for the wire-bonded stack configuration. Since the prediction is based on delta-terms, the absolute accuracy is not of high relevance. The high-voltage switch exhibits 4.1 dB stronger second harmonic for the scaling factor $\rho = 2$, which is related to the 4 times larger occupied silicon area. The $\Delta H_3$ has been evaluated for the cases when: both switches are perfectly equalized, meaning $\kappa^{(\text{HV})} = \kappa^{(\text{LV})} = 0$. Either of the two RF switches have equalization error. If the switches are perfectly equalized, the third harmonic of the high-voltage switch is reduced by 6 dB compared to the low-voltage switch. A suboptimal harmonic performance of the high-voltage switch occurs, when the high-voltage switch is not equalized properly, while the low-voltage switch is perfectly equalized ($\kappa^{(\text{HV})} = 1$, $\kappa^{(\text{LV})} = 0$). Inversely, when the low-voltage switch is suboptimally equalized the opposite occurs. The equalization error may cause a deviation in the range of $\pm 1$ dB of $\Delta H_3$ for the designed RF switches with the scaling factor $\rho = 2$ [104].
5 Design and Layout of High-Voltage RF Switches

1.25
1.5
1.75
2
2.25
2.5
2.75
3

−15
−10
−5
0
5
10
15

\( \rho \)

\( \Delta H \)

\( (\text{dB}) \)

\( \Delta H_2 \)

\( \Delta H_3 \) \((\chi^{(LV)} = 0, \chi^{(HV)} = 0)\)

\( \Delta H_3 \) \((\chi^{(LV)} = 1, \chi^{(HV)} = 0)\)

\( \Delta H_3 \) \((\chi^{(LV)} = 0, \chi^{(HV)} = 1)\)

Figure 5.17: Ratio of the second and third harmonics between the high- and low-voltage switch scaled by the factor \( \rho \).

5.3.4 Hardware Proof

The analytical findings were proved by two prototype ICs designed and fabricated in Infineon 130 nm bulk-CMOS RF switch technology. The circuit diagram and the die photographs are shown in Fig. 5.18. The switches are biased with a series of high-ohmic resistor at the drain-source nodes and gates, where the values for the resistors are set to: \( R_G = 400 \, \text{k}\Omega \), \( R_{G,C} = 100 \, \text{k}\Omega \) and \( R_{DS} = 20 \, \text{k}\Omega \) [104]. In order to equalize the voltage distribution along the stack, MIM capacitors \( C_{eq,i} \) have been coupled in parallel to the channel of the respective MOSFETs as depicted in Fig. 5.18(a). The values of the equalization capacitors decrease from the RF hot to the grounded side of the switch, which can be clearly obtained by the die photograph of the high-voltage RF switch in Fig. 5.18(b) and Fig. 5.18(c). The high-voltage switch is designed for voltages of up to 80 V and comprises 32 stacked transistors with 7 mm gate width, whereas the low-voltage switch is constructed from 17 stacked transistor with 3.5 mm gate width and is capable of handling RF voltages of up to 40 V. Since the switches are scaled proportional, both designs achieve the same \( R_{on}C_{off} \) ratio. The gate length for all transistor in both designs is 120 nm. Given the layout dimensions in Table 5.4, the high-voltage switch has almost double layout length, width and size resulting in the scaling factor of \( \rho \approx 2 \). The numeric values of the equalization capacitances for the high-voltage switch are \( C_{eq,32}^{(HV)} = 2867 \, \text{fF} \), \( C_{eq,31}^{(HV)} = 2697 \, \text{fF} \) etc. and for the low-voltage switch \( C_{eq,17}^{(LV)} = 310 \, \text{fF} \), \( C_{eq,16}^{(LV)} = 276 \, \text{fF} \) etc. It is assumed that both switches are perfectly equalized and the scaling coefficient for both designs is set to: \( \chi^{(HV)} = \chi^{(LV)} = 0 \) [104].
5.3 Linearity Analysis of High-Voltage RF Switches

The devices were excited by 824 MHz and 1800 MHz fundamental tone frequencies representing cellular low- and high-band respectively. For both fundamental frequencies, the applied power for the low-voltage switch is swept from 20 dBm to 35 dBm corresponding to peak RF voltages between 6.3 V and 35.6 V. The power applied to the high-voltage switch was swept from 20 dBm to 41 dBm, resulting in the peak RF voltage of 71 V. For both high- and low-voltage switches the second and third harmonics at 1648 MHz / 2472 MHz for the 824 MHz fundamental tone and 3600 MHz / 5400 MHz for the 1800 MHz are recorded in Fig. 5.19. As predicted, the high-voltage switch exhibits lower third harmonic and the low-voltage switch demonstrates lower second harmonic for both fundamental frequencies. The difference in terms of power of the second and third harmonics at 824 MHz are 11 dB and –8 dB, respectively. At the high-band fundamental tone the deviation in power is 5 dB for the second and –8 dB for the third harmonic [104].

The measurement of the second- (IMD2) and third-order intermodulation products (IMD3) demonstrates a typical blocking scenario for downlink LTE band 5 and band 1 by IMD2 and IMD3 products, respectively. Therefore, two RF signals at 800 MHz and 1700 MHz are combined and applied to the DUT for obtaining the IMD2 at 900 MHz. The IMD3 is verified with the combination of the tones at 1800 MHz and 2000 MHz generating IMD3 at 2200 MHz. The DUT was excited by the same power level for both tones and swept simultaneously from 10 dBm to 24 dBm, corresponding to the RF voltage levels between 2 V and 10 V. The measurement results of the intermodulation products for both switches were recorded and plotted in Fig. 5.20. In general, the trend in the curves follows the predictions made in Eq. (5.29) and
Figure 5.19: Measurement results of the second and third harmonics of the low- and high-voltage switches at cellular low- and high-band frequencies.

Figure 5.20: Measured intermodulation products of both high- and low-voltage switches.
Eq. (5.37). The second-order intermodulation products of the high-voltage switch is 4 dB...12 dB stronger and the third-order intermodulation product is 3 dB...7.5 dB less compared to the low-voltage switch. It should be noted here that the calculation of the difference starts from $V_{RF,pk} \approx 4\,V$, since the measured IMD2 power at $V_{RF,pk} \approx 2\,V$ approaches the noise floor of the setup. The numerical evaluation of the first- and second-order analytical models as well as the respective measurement results are summarized in Table 5.5 [104].

**Table 5.5:** Model-to-hardware correlation.

<table>
<thead>
<tr>
<th></th>
<th>$H_2^{(HV)} - H_2^{(LV)}$</th>
<th>$H_3^{(HV)} - H_3^{(LV)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>First-order model [88]</td>
<td>6 dB</td>
<td>-6 dB</td>
</tr>
<tr>
<td>Second-order model [104]</td>
<td>4.1 dB</td>
<td>-6$\pm$1 dB</td>
</tr>
<tr>
<td>Harmonics measurements at 824 MHz fundamental tone</td>
<td>10...12 dB</td>
<td>-7...-9 dB</td>
</tr>
<tr>
<td>1800 MHz fundamental tone</td>
<td>4...6 dB</td>
<td>-8 dB</td>
</tr>
<tr>
<td>IMD measurements</td>
<td>4...12 dB</td>
<td>-3...-7.5 dB</td>
</tr>
</tbody>
</table>

The third-order nonlinear products follow the polynomial response (5.15) showing almost 30 dB slope per 10 dB increasing input power. The slope is not visible in the presented measurement results, because the graphs are plotted over the RF voltage instead of input power. The difference between the high- and low-voltage switch is between -7 dB to -8 dB over the nonlinear product types and different frequencies, which is close to the calculated value of -6 dB. The second-order nonlinear products behave differently over the measured frequency and nonlinear product types and do not follow the polynomial model (5.15), where a 20 dB slope per 10 dB increase of applied power is expected. This is related to the complex physical nature of the substrate nonlinearities. Various effects have also a significant impact on the nonlinear distortions, which generates a significant deviation from the expected 20 dB slope per 10 dB increase input power. This results on average in a stronger deviation of the measurement results from the prediction (5.32) compared to third-order nonlinearities. Moreover, the model does not support the influence of such layout structures as RF routing lines and ground shapes surrounding the switch [104]. The variation of the measured nonlinear distortions difference with the model prediction do not exceed 6 dB and is even less than 3 dB for most cases. The quality of the prediction model is improved.
with the second-order model in contrast to universal scalable models, where the accuracy is about 15 dB for the substrate-related contributors [85] and 5 dB for the third-order harmonic in an off-state intrinsic transistor [82]. It should be noted that the proposed model is applicable to only shunt high-stacked switches operating in off-state and does not consider phase effects in the low-order polynomial function and does not respect substrate carrier dynamics as well as finite inertia. However, the calculated ratio in terms of second- and third-order nonlinear products correlates reasonably well with the measurements and correctly predicts the trend in nonlinear performance. The prediction models are valid for either bulk- and SOI-CMOS RF switch processes on high-ohmic substrates and may be used at the IC floorplanning stage for rapid estimation of the RF switch geometry [104].
6 Hardware Characterization of Antenna Tuning ICs

Among the RF parameters specific to antenna tuners are small-signal $C_{\text{off}}$, $R_{\text{off}}$, $R_{\text{on}}$ and large-signal breakdown voltage $V_{\text{RF,max}}$, harmonics, and intermodulation distortions. Since the hardware switch is mostly assembled on a PCB, the accurate and repeatable measurements of small-signal parameters especially $C_{\text{off}}$ and $R_{\text{off}}$ are associated with a number of challenges. Assembly variations and limited accuracy of the measurement equipment as well as fabrication tolerances of the testboard and calibration structures result in uncertainties, for example $C_{\text{off}}$ measurements well exceed 50 fF for the frequency range of 500 MHz to 6 GHz. The accuracy of the obtained results may be influenced by the experience of an operator and effort spent for manual assembly. However, the ability to repeat the measurement by different operators in a thuput optimized flow is still limited by the points mentioned above [106], [107]. This chapter proposes a measurement and de-embedding method for the accurate characterization of small-signal parameters that allows reducing the measurement error, improving the repeatability and reproducibility of the RF switch. Furthermore, an overview of the large-signal measurement setup is provided.

6.1 Characterization of Small-Signal Parameters

The first-order equivalent circuit of an off-state shunt RF switch is depicted in Fig. 6.1(a), where the capacitances $C_1 - C_n$ and $R_{\text{off,1}} - R_{\text{off,n}}$ model the $n$ throws of the switch. Representing the switch by a $n$-port linear network, the shunt capacitance and resistance of the $i$-th throw can be obtained using $Y$–parameters of the demonstrated network [106], [107]:

$$C_i = \frac{\Im \{Y_{ii}\}}{\omega} \quad (6.1)$$

$$R_{\text{off},i} = \frac{1}{\Re \{Y_{ii}\}} \quad (6.2)$$

Alternatively, the capacitance can be calculated using $Z$-parameters of the network as $-1/\Im \{Z_{ii}\}$. However, using $Z$-parameters instead of $Y$–parameters results in slightly different frequency response and a bit lower absolute value for the real switch. The minor differences are related to the finite isolation between the RF ports and different termination impedances at the unexcited
ports, while evaluating the shunt capacitance at the \(i\)-th port of the network, which is depending on the definition for \(Y\)- and \(Z\)-parameters [108]. For evaluation, the switch (also referred as DUT) is mounted on a test fixture for measurements (in this work the DUT is soldered on a PCB). The test fixture extends the DUT by interconnect (embedding) networks \(F_{ai}\) representing e.g. planar transmission lines and coaxial interface to the measurement equipment [106], [107]. The corresponding equivalent circuit of the DUT mounted on a test fixture is presented in Fig. 6.1(b). In order to keep the de-embedding effort low, all interconnect networks are aimed to be identical by design. However, in practical hardware it is impossible to achieve equality of all embedding structures due to assembly variations and limited accuracy of the measurement equipment as well as fabrication tolerances of the testboard and
calibration structures [106], [107]. In certain cases, it is not possible to design identical interconnect structures for all ports of the DUT, which results in additional systematic difference to the embedding networks. An example for this case are boards with bended transmission lines, which are known to have a frequency-dependent equivalent electrical length defined by the bending configuration [109]. A de-embedding procedure as shown in Fig. 6.1(c) helps to remove the effect of test fixture on the DUT response [110]. For the sake of simplicity a common de-embedding network $F_z$ is typically used at all ports of the structure. The mathematics behind de-embedding is well known and can be found in literature [110]. After de-embedding, a residual error at each of the $n$ ports remains, which can considerably distort the extracted capacitance and resistance values [106], [107]. A de-embedding approach based on custom OPEN standard regularly used for on-wafer measurements implies subtracting the response of a dedicated empty test fixture from the measured response of the embedded DUTs eliminating the systematic de-embedding uncertainties caused by the board design [111]. Considering the fact that different instances of the test fixture are used for the DUT measurement and de-embedding, random variations caused by the board assembly remain uncorrected. The challenge is that the embedding networks $F_{bi}$ shown in Fig. 6.1(d) of the dedicated OPEN standard do not match the networks $F_{ai}$ of the DUT mounted on a different instance of the board as shown in Fig. 6.1(b) [106], [107].

### 6.1.1 Sensitivity Analysis of $C_{\text{off}}$ Extraction

**Physical Length and Characteristic Impedance**

The accuracy of measured shunt capacitance is supposed to be very sensitive to physical length de-embedding errors, since an electrically short transmission line transforms a high impedance in a similar way as a shunt capacitance. Fig. 6.2(a) shows the DUT capacitance followed by a transmission line $\text{TL}_{e}$, which models the effect of physical length de-embedding error.

The capacitance after the transmission line $\text{TL}_{e}$ is defined as [106]:

$$C_{1,ez} = \frac{\Im\left\{Y_{\text{dut,ez}}\right\}}{\omega}, \quad (6.3)$$

where $Y_{\text{dut,ez}}$ is [110]:

$$Y_{\text{dut,ez}} = \frac{1}{Z_e} \frac{Z_e + jY_{\text{dut}}^{-1} \tan \beta_e l_e}{Z_e Y_{\text{dut}}^{-1} + jZ_e \tan \beta_e l_e}. \quad (6.4)$$
Considering $Y_{\text{dut}} = j\omega C_1$, Eq. (6.4) transforms to:

$$Y_{\text{dut,ez}} = j \left[ \frac{1}{Z_e} \left( \frac{\omega C_1 Z_e + \tan \beta_e l_e}{1 - \omega C_1 Z_e \tan \beta_e l_e} \right) \right].$$

(6.5)

where $Z_e$, $l_e$, and $\beta_e$ are the characteristic impedance, physical length and propagation constant of the transmission line, respectively. By differentiating Eq. (6.3) with respect to $l_e$, the sensitivity of de-embedded capacitance $C_{1,ez}$ to the variation of the physical length $l_e$ is calculated as:

$$S_{C_{1,ez}} = \frac{\partial C_{1,ez}}{\partial l_e} = \frac{\partial}{\partial l_e} \left[ \frac{1}{\omega Z_e} \left( \frac{\omega C_1 Z_e + \tan \beta_e l_e}{1 - \omega C_1 Z_e \tan \beta_e l_e} \right) \right].$$

(6.6)

The numerical evaluation of Eq. (6.6) for $l_e = 0$ mm, $100 \text{ fF} < C_1 < 300 \text{ fF}$, $40 \Omega < Z_e < 60 \Omega$, $0.5 \text{ GHz} < f < 6 \text{ GHz}$ and $\beta_e = 35f/f_0 \text{ rad/m}$ with $f_0 = 1 \text{ GHz}$ shows that the de-embedding uncertainty corresponding to 1 mm physical line length adds around 100 fF error to the target capacitance value. $S_{C_{1,ez}}$ is non-negligibly influenced by the characteristic impedance of the transmission line $Z_e$ and increases with the frequency and capacitance value [106]. It should be noted here that the value of the propagation constant is obtained for a 50-Ω transmission line on a 100-μm thick RO4003C laminate substrate, which is usually used for RF applications. The detailed numerical evaluation is demonstrated by the plot in Fig. 6.3. Considering the results of the numerical evaluation the effective physical length de-embedding variation must be below ±100 μm in order to achieve the target capacitance measurement accuracy of ±10 fF. Other possible uncertainties generated in the de-embedding network is not accounted in the evaluation. Such low variation is challenging to achieve in practice. Furthermore, uncertainties in the characteristic impedance of the de-embedding structure may amplify the error caused by physical length variations [106].

Figure 6.2: Equivalent circuit of the off-state shunt switch with (a) electrical length de-embedding and (b) insertion loss errors.
6.1 Characterization of Small-Signal Parameters

Figure 6.3: Calculated sensitivity of the de-embedded capacitance $C_{1,ez}$ with $\beta_e = 35 \frac{f}{1 \text{ GHz}}$ rad/m and $l_e = 0$ mm.

### Insertion Loss

The influence of the insertion loss de-embedding error on the extracted capacitance can be modeled by adding an L-pad attenuating network in front of the capacitance $C_1$ as demonstrated in Fig. 6.2(b). The admittance of the network including the L-pad is obtained as [106]:

$$Y_{dut,IL} = \frac{1}{R_{e2}} + \frac{\omega R_{el} C_1}{1 + \omega^2 R_{el}^2 C_1^2} + \frac{j \omega C_1}{1 + \omega^2 R_{el}^2 C_1^2}. \quad (6.7)$$

Considering Eq. (6.3), the shunt capacitance is calculated as:

$$C_{1,IL} = \frac{1}{1 + \omega^2 R_{el}^2 C_1^2} C_1. \quad (6.8)$$

Given that the insertion loss caused by the de-embedding uncertainties is considerably to be less than 0.5 dB, the $R_{el}$ shall not exceed 1 $\Omega$ according to the analytical model for the L-pad [112]. Considering the target operating frequency range of up to 6 GHz and the capacitance values not exceeding 300 fF, the maximum deviation of $C_{1,IL}$ from $C_1$ is expected to be 1%, which can assume to be insignificant [106].

#### 6.1.2 De-Embedding Accuracy Requirements for $R_{off}$ Extraction

De-embedding accuracy in terms of dissipative power losses is of paramount importance for enabling $R_{off}$ measurements, especially at sub-GHz frequencies.
The effect of power loss error is demonstrated by a Π-type attenuator coupled between the input node and the DUT as shown in Fig. 6.4 [107].

![Diagram of DUT with added insertion loss de-embedding error.](image)

**Figure 6.4:** DUT with added insertion loss de-embedding error.

Considering the analytical model for a Π-pad [113]:

\[ R_1 = |Z_0| \frac{10^{\frac{A_{\text{db}}}{10}} + 1}{2} \left( 10^{\frac{A_{\text{db}}}{20}} - 1 \right) \]
\[ R_2 = |Z_0| \frac{10^{\frac{A_{\text{db}}}{10}} - 1}{2} \left( 10^{\frac{A_{\text{db}}}{20}} \right), \quad (6.9) \]

where \( A_{\text{db}} \) is the de-embedding error in dB and \( Z_0 \) is the characteristic impedance of the measurement setup. Good de-embedding shall not influence the \( R_{\text{off}} \) readings at the input, if the conditions \( R_1 \gg R_{\text{off}} \) (\( R_1 = 100 \, \text{k}\Omega \), barely acceptable given the high values of \( R_{\text{off}} \) at sub-GHz range) and \( A_{\text{db}} < 0.0086 \) dB is fulfilled. Such de-embedding accuracy in manually-assembled PCB-based test fixture is hardly possible to realize in practice because of the mismatch between the actual test fixture and de-embedding structures. This is related to board fabrication tolerances, uncertainties of manual assembly, possible systematic de-embedding errors, and the limited accuracy of the measurement equipment [107].

### 6.1.3 Measurement and De-Embedding Procedure

In order to improve the accuracy, repeatability and reproducibility of \( C_{\text{off}} \) and \( R_{\text{off}} \) measurements, the proposed method is based on the individual correction of the physical length and characteristic impedance for every instance of the assembled DUT on board. The correction is performed by removing the DUT and measuring the empty (open) instance of the board with all other components remaining unchanged. The data is further used for the correction of the measured response [106], [107].

#### Measurement Procedure

The measurements are executed in three steps:

- **Step 1:** The populated board with the DUT is measured.
6.1 Characterization of Small-Signal Parameters

- Step 2: The DUT is removed from the board, while all other elements like SMA (sub-miniature version A) or other connector interface for coaxial cable remain soldered on the board.

- Step 3: The board without the DUT is measured on the same setup as the populated one [106], [107].

It should be mentioned that the measurement procedure can be performed in reversed order, by measuring the board without DUT first and afterwards soldering the DUT on it. The order does not have an essentially impact on the final extracted results. It might be a matter of individual preference of a particular operator [106], [107]. Apart from that, the main difference of the proposed method from known processes of the similar kind is the individual characterization of test fixtures in the high-ohmic impedance plane, which considerably reduces the board assembly variations on the DUT capacitance and resistance measurements [106]. Alternatively, a common de-embedding network $F_z$ as shown in Fig. 6.1(c) is obtained using any suitable method known in the art, for example thru-reflected-line (TRL) [114] or numerical thru-line (TL) [115]. The term common symbolizes a de-embedding network suitable for the use with a nominal test fixture, but not matching the populated boards concerning assembly uncertainties and board fabrication tolerances [106], [107].

De-Embedding Procedure

In the following two variants of de-embedding procedure, the OPEN de-embedding and OPEN correction methods are proposed. The OPEN de-embedding variant is implemented according to Eq. (6.10):

$$S_{dut} = S_{dut,\text{fix}}S_{\text{open,fix}}^{-1}. \quad (6.10)$$

The $S$-parameters $S_{dut,\text{fix}}$ and $S_{\text{open,fix}}$ are matrices of the non-de-embedded measured test fixture with and without DUT according to Fig. 6.1(b) and Fig. 6.5(a). $S_{dut}$ is then converted to $Y$-parameters matrix $Y_{dut}$ using the $S$– to $Y$–parameters conversion (the formulas can be found in [108]). The difference between OPEN standard according to the proposed method in Fig. 6.5(a) and its conventional counterpart in Fig. 6.1(d) is that in the proposed OPEN structure the embedding networks $F_{ai}$ match the embedding networks of the measured DUT on board [106], [107].

For the OPEN de-embedding method, a common de-embedding network is not necessary, which means that it does not introduce uncertainties associated with variations of the characteristic impedance peculiar to common
de-embedding structure [106], [107]. It is worth emphasizing that the OPEN de-embedding is only suitable for off-state characterization of the DUT exhibiting high-impedance shunt response, which is actually defined as a target operation mode in most of the small-signal measurements in this work. The OPEN de-embedding is not applicable for the characterization of the DUT in on-state [106], [107]. The on-state resistance $R_{on}$ can be accurately measured at DC. In the OPEN correction method, the measured DUT and empty board responses are de-embedded by a common de-embedding network. The OPEN correction method is implemented as follows:

$$Y_{dut} = Y_{dut,deemb} - Y_{open,deemb}, \quad (6.11)$$

where $Y_{dut,deemb}$ is the $Y$-parameter matrix of the de-embedded measured DUT on board with $F_z$ network as shown in Fig. 6.1(c). $Y_{open,deemb}$ is the $Y$-parameter matrix obtained after de-embedding of the measured empty board with $F_z$ network according to Fig. 6.5(b), where $F_z$ denotes the common de-embedding network. The OPEN correction procedure enables the minimization of the errors caused by physical length variation of the assembled board. It accounts for most of the power losses in the test fixture, which is not essential for the accurate $C_{off}$ and $R_{off}$ extraction. At the same time, the common de-embedding network may influence the absolute value of the de-embedded capacitance [106], [107].

**Figure 6.5:** OPEN standard applied in the proposed method: (a) embedded open test fixture, (b) de-embedded open test fixture.
6.1.4 Experimental Proof

In order to prove the efficiency of the proposed method, a four-throw shunt aperture tuning high-voltage RF switch has been designed in CMOS RF-switch technology. The switch provides RF voltage handling of up to 90 V, on-state resistance of sub-$2\,\Omega$ and off-state capacitance of 160 fF at sub-6 GHz cellular frequencies. Other design aspects of the DUT are outside the scope in this chapter because the proposed measurement and de-embedding procedure is not limited by a specific switch architecture. The switch is considered as a black box solely for the purpose of $C_{\text{off}}$ and $R_{\text{off}}$ measurements. The fabricated chips have been flip-chip assembled into a 10-pin leadless plastic package with 400 µm pad pitch and flip-chip mounted on PCB for measurements. The pinout of the packed device and the assembled testboard is shown in Fig. 6.6(a) and Fig. 6.6(b) respectively. The testboards are manufactured on a Megtron6 substrate material and the transmission lines are designed for 50-Ω characteristic impedance. For testing of the proposed de-embedding method five samples of the testboard, namely DUT1-DUT5, including the switch have been prepared for measurements [106], [107].

For comparison of the proposed measurement procedure with a conventional method, additionally, two transmission line structures as shown in Fig. 6.6(c) have been prepared for obtaining a common de-embedding network according to the numerical TL calibration technique [115]. Since the number of samples are relatively low for any representative statistical analysis, assembly “artifacts” have been intentionally introduced into some samples to model worst-case scenario that might occur during manual assembly process and better demonstrate the capabilities of the proposed measurement and de-embedding method [106], [107]. Particularly, one sample (DUT3) contains an excessive 0.5 mm gap between the solder plane of the SMA connector and the board edge, modeling the uncertainties in the physical length of the test fixture line. For introducing some variation into the characteristic impedances at higher frequencies, the RF1 SMA connector of DUT3 is not soldered at the backside of the board, although all others are soldered at the bottom as well. Yet another packed IC is slightly tilted with respect to the target orientation on the DUT4 board. The remaining testboards are assembled normally without any intentionally introduced artifacts. The prepared variants including introduced errors are provided in Table 6.1 [106], [107].

Measurement Results

The measurement for each board is conducted in exact accordance with the steps described in Section 6.1.3. First, the 4-port $S$-parameters of the five
Figure 6.6: (a) Pinout of the fabricated high-voltage aperture tuner switch, (b) photograph of the assembled board as well as (c) thru and line boards for common de-embedding network generation.

Table 6.1: List of assembled samples.

<table>
<thead>
<tr>
<th>DUT ID</th>
<th>IC bonding</th>
<th>SMA mounting</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT1</td>
<td>normal</td>
<td>normal</td>
</tr>
<tr>
<td>DUT2</td>
<td>normal</td>
<td>normal</td>
</tr>
<tr>
<td>DUT3</td>
<td>normal</td>
<td>RF1 SMA not soldered to board backside ground plane</td>
</tr>
<tr>
<td>DUT4</td>
<td>tilted, Fig. 6.7(a)</td>
<td>normal</td>
</tr>
<tr>
<td>DUT5</td>
<td>normal</td>
<td>gap between RF1 SMA and board edge, Fig. 6.7(b)</td>
</tr>
</tbody>
</table>

Figure 6.7: Intentionally introduced assembly "artifacts": (a) – tilted DUT, (b) – gap between the SMA connector and the testboard.
6.1 Characterization of Small-Signal Parameters

Assembled boards with DUTs have been recorded to obtain $S_{\text{dut,fix}}$, then the DUTs have been removed from the boards and the $S$-parameters are measured again providing $S_{\text{open,fix}}$. The de-embedding is performed according to Eq. (6.10). Furthermore, the measured $S_{\text{dut,fix}}$ response of each board has been de-embedded with the two transmission line structures as shown in Fig. 6.6(c) representing OPEN correction method. Since the DUT is removed and the resulting open testboard is remeasured, the overall effort comparing to common de-embedding approach is increased, with estimated time penalty of around 20% for completing these additional steps. The experiment is performed in one measurement session, such that the room temperature, equipment calibration etc. do not drift and notably distort the results. The $S$-parameters have been recorded using the Agilent E5071B VNA [106], [107]. The obtained measurement results of $C_{\text{off}}$ with and without de-embedding is shown in Fig. 6.8 – Fig. 6.10. Each plot comprises five curves corresponding to one throw (SW1 – SW4) of the five measured samples. The curves with anomalous (outlier) are marked with the corresponding sample ID. According to the measurements, the common de-embedding procedure results in a very large variation of the measured capacitance, which well exceeds the target accuracy of $\pm 10\, \text{fF}$. As predicted the most pronounced outlier is recorded at RF1 pin of the DUT5 sample with the extended physical length because of the introduced gap. Both OPEN correction and OPEN de-embedding methods substantially improve the repeatability of the capacitance measurements and provides curves close to the expected nominal value of $C_{\text{off}}$ for the designed IC. However, the variations attributed to assembly errors are still present, but less pronounced owing to individual de-embedding of each instance of the test fixture. Both proposed methods satisfy the target measurement accuracy of $\pm 10\, \text{fF}$ over most of the frequency range [106]. Additionally, a standard deviation of the measured capacitance as a function of frequency and throw number is calculated enabling the quantification of the improvement brought

Figure 6.8: Shunt $C_{\text{off}}$ of the samples DUT1 – DUT5 obtained $Y_{\text{dut,deemb}}$ after common de-embedding of measured data according to Fig. 6.1(c).
Figure 6.9: Extracted shunt $C_{\text{off}}$ of the switch after applying OPEN de-embedding procedure.

Figure 6.10: Extracted shunt $C_{\text{off}}$ of the switch after OPEN correction procedure.

by the OPEN de-embedding and OPEN correction procedure and is calculated as [106]:

$$C_{\sigma,i}(f) = \sqrt{\frac{1}{5} \sum_{s=1}^{5} (C_i(f,s) - C_{\mu,i}(f))^2}, \quad (6.12)$$

where $C_i(f,s)$ is the measured capacitance of the $s$-th sample at $i$-th throw at the frequency $f$ and $C_{\mu,i}(f) = \frac{1}{5} \sum_{s=1}^{5} C(f,s)$ is the mean capacitance at $i$-th throw at $f$ over all five measured samples [106]. After evaluation, $C_{\sigma,i}(f)$ is averaged over all four throws and following frequency points: 0.5, 1, 2, 3, 4, 5, 6 GHz resulting in average standard deviation for common de-embedding method of 13.25 fF, for OPEN correction and OPEN de-embedding 5.45 fF and 5.6 fF respectively. The proposed procedure shows an improvement in terms of capacitance accuracy measurements by more than 2.3 times [106]. The measurement results of $R_{\text{off}}$ extracted with and without de-embedding is shown in Fig. 6.11 – Fig. 6.13. Each plot contains five curves correspond to the measured boards DUT1 – DUT5 similar to capacitance measurements. It can be observed that the response of the resistance calculated from common de-embedded measurements (Fig. 6.11) is not stable below 2 GHz due to the poor accuracy of the de-embedding procedure. Furthermore, the response is not dropping log-linearly over the frequency as predicted. The sample DUT5
demonstrates an obvious outlier, proving insufficient immunity of this de-embedding approach against assembly uncertainties [107]. The measurement results of the off-state equivalent resistance obtained with the proposed OPEN de-embedding and OPEN correction approaches as depicted in Fig. 6.12 and Fig. 6.13 respectively, show superb stability of $R_{\text{off}}$ readings over frequency with expected log-linear dropping. As in the capacitance measurements, the effect of assembly artifact of the sample DUT5 is visible but less pronounced compared to the results with OPEN correction de-embedding, which confirms the capability of the proposed de-embedding procedure to tolerate large assembly errors. The measured curves at the RF2 pin of the boards without intentionally introduced assembly errors are almost overlapping [107]. From

![Figure 6.11: $R_{\text{off}}$ of the samples DUT1 – DUT5 obtained $Y_{\text{dut,deemb}}$ after common de-embedding of measured data according to Fig. 6.1(c).](image1)

![Figure 6.12: Extracted $R_{\text{off}}$ of the switch after applying OPEN de-embedding procedure.](image2)

![Figure 6.13: Extracted $R_{\text{off}}$ of the switch after OPEN correction procedure.](image3)
the performed experiments, it can be concluded that the proposed OPEN
de-embedding method has proven to be efficient and robust against assembly
uncertainties, providing accurate and repeatable response over the target
cellular frequency range. The method is suitable to remain as a primer choice
for the characterization of state-of-art or next-gen antenna tuning switches
fabricated in established or disruptive technologies with even lower power
losses in off-state and off-capacitances in sub-100 fF range [106], [107].

6.2 Evaluation of Large Signal Parameters

6.2.1 Harmonics Measurement Setup

The second and third harmonics of the DUT are indicators of the switch lin-
earity and used for evaluating the RF breakdown voltage. The measurements
are performed on a setup demonstrated in Fig. 6.14.

![Block diagram of the harmonic measurement setup.](image)

The setup is excited by an RF signal with typical cellular center frequencies such
as 824 MHz or 1800 MHz related to cellular low- and high-band, respectively.
The single tone RF signal from the signal generator is applied to the power
amplifier (PA). The PA is followed by a circulator to prevent the reflected
signal from loading the PA. Furthermore, the circulator enables the accurate
control of the power applied to the DUT by preventing the reflected signal
from load-pulling the PA output. The generated second and third harmonics
of the PA are suppressed by a low-pass-filter (LPF) to the level below $-110$ dBm.
After filtering, the signal is applied to the high-ohmic DUT with an off-state
RF switch in the 50 $\Omega$ sensing RF path, where the DUT can be either a shunt
or a series device as shown in Fig. 6.9. The input impedance $Z_{in,DUT}$ of the
DUT can be approximated as follows:

$$Z_{DUT,off} \approx \frac{1}{j2\pi f_0 C_{off}}, \quad (6.13)$$
where $f_0$ is the fundamental excitations frequency from the RF signal applied to the DUT. The numeric value of $|Z_{\text{in,DUT}}|$ is very high compared to the 50 $\Omega$ characteristic impedance of the RF signal path and load, generating almost full reflection conditions at the DUT input. The peak RF voltage at the input of the shunt DUT is calculated as:

$$V_{\text{DUT,in,RF,peak}} \approx 2 \cdot 10^{\frac{P_{\text{dBm}} - 10}{20}}.$$  \hspace{1cm} (6.14)

In case of a series device, the voltage at the output of the DUT is:

$$V_{\text{DUT,out,RF,peak}} = V_{\text{DUT,in,RF,peak}} \left| \frac{Z_0}{Z_0 + Z_{\text{in,DUT}}} \right|,$$  \hspace{1cm} (6.15)

where the deviation from the input voltage is very small. Under this condition the assumptions made in the previous chapter are satisfied as the DUT operates in “quasi shunt mode”. The diplexer attached after the DUT, splits the main fundamental tone and harmonics. The second and third harmonics are recorded at the high-pass output branch of the diplexer by a spectrum analyzer as shown in Fig. 6.14 [116], [101]. An example testboard for conducting the harmonics measurements is shown in Fig. 6.14, where two ICs in different excitation configurations can be attached by a jumper to the RF line.

### 6.2.2 Intermodulation Measurement Setup

The second- and third order intermodulation products are measured with the setup portrayed in Fig. 6.15. The same testboard from Fig. 6.14 is used for the measurement of the intermodulation products. The setup is excited by two RF signals which are combined after filtering the harmonics of the PA. The combined signal is then applied to the high-ohmic input of the DUT. The respective intermodulation products are measured at the output of the bandpass filter (BPF) by a spectrum analyzer. A photograph of the setup is shown in Fig. 6.16.
Figure 6.15: Block diagram of the measurement setup for determining the intermodulation products.

Figure 6.16: Photograph of the measurement setup for determining the intermodulation products.
7 Application Related Aspects of Antenna Tuning Technique – Hardware Toolkit for Antenna Tuning Applications

Driven by esthetic considerations, antennas of modern handheld cellular user equipment are integrated into the chassis of the device. In order to evaluate the designed chips on the application level, a hardware toolkit for rapid prototyping of antenna aperture tuning system has been constructed and is presented in this chapter. The hardware toolkit comprises a reconfigurable IFA, aperture tuning system, feed, short fixture elements enabling the measurement of small- and large-signal properties of the tuned antenna at the feed. The electrical properties of the IFA, particularly the structure implemented in the hardware toolkit, are analyzed using a transmission line model of the aperture-tuned IFA. Several application-level studies have been conducted with the toolkit and designed aperture tuning ICs. The results are presented in the respective chapters related to the designed circuits. Apart from that, the toolkit has been used for analysis of the harmonics distribution in the aperture-tuned IFA depending on the position of the aperture tuning system along the radiating arm of the antenna. This analysis, strongly based on said transmission line model, is presented further in this chapter.

7.1 Transmission Line Model of the Aperture-Tuned IFA

We start with considering a typical aperture-tuned single-arm IFA as depicted in Fig. 7.1(a). The aperture tuner is in general a switch-based reactive circuit coupled between the radiating arm and the ground. The corresponding transmission line model of the IFA is shown in Fig. 7.1(b) [7]. The model is assumed to be lossless and starts with a short on the very left side and ends with an open on the rightmost side. The open end of the antenna is represented by the resistance $R_R$, which models the radiation and loss resistance and is the only element dissipating the fed power in the circuit. The physical lengths of the sections are represented by the parameters $L_{FS}$, $L_{FO}$, $L_{TF}$ and $L_{TO}$, where [101]:

- The distance between the short and feed is described by $L_{FS}$.
- $L_{FO}$ is the distance from the feed to open.
Application Related Aspects of Antenna Tuning Technique – Hardware Toolkit for Antenna Tuning Applications

Figure 7.1: (a) Aperture-tuned IFA and (b) corresponding transmission line model.

- $L_{TF}$ is the distance between the feed and aperture tuning point.
- $L_{TO}$ describes the distance from the aperture tuning point to open.

The total physical length of the radiating arm $L_{TO}$ is the sum of the sections $L_{FS}$ and $L_{FO}$. The characteristic impedance $Z_o$ of the asymmetrical coplanar strip line can be determined empirically or analytically using the electrical and geometrical properties of the substrate material on which the antenna is deposited. $Z_o$ is in general formed by the radiating arm of the antenna and the chassis. The product $\beta L$ describes the electrical length of the corresponding section, where $L$ is the physical length and $\beta$ the propagation constant in the respective section of the transmission line. In a lossless transmission line, the propagation constant equals to the phase constant [101]. In spite of high abstraction level of the given structure, the proposed transmission line model is suitable for physical modelling of the return loss, voltage standing wave and
7.2 Harmonics Distribution in Aperture-Tuned IFA

The combination of 3D-EM simulated $S$-parameters, radiation properties of an intrinsic antenna and tuning network gives a good insight into return loss response. However, the precise prediction of the generated nonlinear distortions by the intrinsic RF switch radiated or fed back to the transceiver is more challenging due to the relatively low accuracy of the simulation models and large spread of nonlinear response over temperature and process variations in RF-switch MOSFETs [117]. The nonlinear performance of the intrinsic RF switch is mainly limited by the fabrication process and to author’s knowledge can hardly be improved by circuit design techniques in design-in phase of the switch. The coupling of the nonlinear products into the receive path is reduced by various methods while designing the RF front-end. The coupling of the nonlinear products is defined by the isolation between the diversity and main antenna, which is limited by the physical distance of the antennas integrated into the chassis of a mobile phone. PIFA antennas introducing notches or mismatches in the required bands to filter out the harmonics are demonstrated in [118], [119]. The approach presented in [118] enables the suppression of harmonics by generating a strong mismatch at the feed at the required frequency bands. However, the proposed antenna is not suitable for simultaneous reception of the signal at integer multiplies of the transmitted signal, which is mandatory for downlink CA. Moreover, the structure of such antennas is very complex, which makes them not easy to integrate into the chassis of a mobile phone. Using the transmission line model as shown in Fig. 7.1(b) the local minima for the second and third harmonic along the radiating arm of the antenna can be identified for a given use case.

The transmission line model enables the calculation of the power transfer coefficient from the tuner back to the feed, which is terminated by the 50-Ω impedance of the RF front-end circuitry and the radiated power at $R_R$. $Z_{TO}$ is the transformation of $R_R$ by the transmission line $L_{TO}$ and is calculated with Eq. (7.1):

$$Z_{TO} = Z_0 \frac{R_R + jZ_0 \tan (\beta (L_{FO} - L_{TF}))}{Z_0 + jR_R \tan (\beta (L_{FO} - L_{TF}))}.$$  \hspace{1cm} (7.1)
The impedance $Z_{TF}$ defines the harmonics power transferred from the aperture tuner to the feed, where the calculation of $Z_{TF}$ begins at the shorted end of the antenna. First, the short is transformed to the impedance $Z_{FS}$:

$$Z_{FS} = jZ_0 \tan(\beta L_{FS}) . \quad (7.2)$$

The total impedance at the feed is calculated by the parallel connection of the source impedance $Z_S$ and $Z_{FS}$ and is transformed by the section $L_{TF}$ into the impedance $Z_{TF}$:

$$Z_{TF} = Z_0 \frac{Z_S||Z_{FS} + jZ_0 \tan(\beta L_{TF})}{Z_0 + j(Z_S||Z_{FS}) \tan(\beta L_{TF})}, \quad (7.3)$$

where $Z_S = 50 \Omega$ is the source impedance at the feed. Using Eq. (7.1) and (7.3), the transmission line model from Fig. 7.1(b) can be simplified to the IFA impedance model at the tuning point as portrayed in Fig. 7.2. The harmonics generated by the aperture tuner are described by the voltage source $E_H$, where $Z_H$ is the source impedance. The corresponding amplitudes of the second and third harmonics are assumed to be $E_{H2}$ and $E_{H3}$, respectively. The voltage drop at $Z_{TO}$ defines the radiated harmonic power $P_{TO}$ and the power coupled back to the feed point $P_{TF}$ is evaluated with the voltage drop at $Z_{TF}$ according to the Eq. (7.4) and Eq. (7.5) [101]:

$$P_{TF} = \frac{1}{2}E_H^2 \left| \frac{Z_T}{Z_{TF}(Z_T + Z_H)} \right|^2 \Re\{Z_{TF}\} , \quad (7.4)$$

$$P_{TO} = \frac{1}{2}E_H^2 \left| \frac{Z_T}{Z_{TO}(Z_T + Z_H)} \right|^2 \Re\{Z_{TO}\} , \quad (7.5)$$

Figure 7.2: IFA impedance model for the calculation of the power distribution of the harmonics.
where \( Z_T = Z_{TO} \parallel Z_{TF} \). The value of the voltage source \( E_H \) is influenced by the operating conditions of the tuner with the amplitude of the fundamental tone \( V_T \) across the tuner being the most important one and nonlinear properties of the tuner. \( V_T \) is simply defined from the voltage standing wave ratio along the radiating arm of the antenna with \( V_R \) being the voltage drop at \( R_R \):

\[
V_T = V_R \left| 1 + \Gamma_0 e^{-2j\beta L_{TO}} \right| ,
\]

(7.6)

where the reflection coefficient \( \Gamma_0 \) at the open end of the antenna is calculated as follows:

\[
\Gamma_0 = \frac{R_R - Z_0}{R_R + Z_0} .
\]

(7.7)

The amplitudes of the second and third harmonic driven by a single-tone signal increase with:

\[
E_{H2} \sim V_T^2
\]

(7.8)

\[
E_{H3} \sim V_T^3 .
\]

(7.9)

For a specified boundary conditions at the open and well-known nonlinear characteristic of the tuning network, the harmonics power transferred from the tuner to feed, and \( R_R \) can be calculated as a function of the tuner position along the IFA according to Eq. (7.4) and (7.5), taking into account Eq. (7.6), Eq. (7.8) and Eq. (7.9). The power transfer coefficients \( CF_{TF} \) and \( CF_{TO} \) are described by Eq. (7.10) and Eq. (7.11) [101]:

\[
CF_{TF} = 10 \log \left( \frac{P_{TF}}{P_{max}} \right) ,
\]

(7.10)

\[
CF_{TO} = 10 \log \left( \frac{P_{TO}}{P_{max}} \right) ,
\]

(7.11)

where \( P_{max} \) is the maximum available power from the voltage source \( E_H \) transferred to the source impedance \( Z_H \).

\[
P_{max} = \frac{E_H^2}{4\Re \{Z_H\}}
\]

(7.12)

The second and third harmonics power distribution between the feed and \( R_R \) can be described by \( P_{TF} \) (7.4), \( P_{TO} \) (7.5), \( CF_{TF} \) (7.10) and \( CF_{TO} \) (7.11) as a function of the aperture tuner position along the radiating arm for a fixed location of the feed [101].
7.3 Physical Design of the IFA

The IFA is designed using a HFSS 3D-EM simulator on a 2 mm-thick FR4 substrate in a single metal layer. The layout properties of the designed antenna can be obtained from Fig. 7.1(a). The width of the radiating arm is 2 mm, and the gap between the radiating arm and the chassis is set to 3 mm. The total length of the radiating arm is $L_{\text{tot}} = 70$ mm and the distance between feed and short is $L_{\text{TF}} = 15$ mm. The aperture tuning system can be attached anywhere between the feed and open end of the radiating arm. The required transmission line model parameters such as radiation and loss resistance $R_R$ as well as characteristic impedance $Z_0$ is obtained from 3D-EM simulations. $Z_0$ is defined from the time-domain reflectometry (TDR) analysis of the linear antenna model, where the radiating arm is exposed to a voltage pulse from one end. The characteristic impedance $Z_0$ is extracted from the voltage-to-current ratio before the reflected wave arrived back to the source and is calculated as [101]:

$$Z_0 = 121\Omega. \quad (7.13)$$

The total electrical length of the transmission line model is evaluated from the simulated $S$-parameter data of the antenna and is approximately one-third of the wavelength at 900 MHz.

$$\beta L_{\text{tot}} = \frac{2\pi}{3} \quad (7.14)$$

The electrical length for the sections $L_{\text{FS}}$, $L_{\text{TF}}$ and $L_{\text{TO}}$ along the radiating arm can be derived from the total electrical length and is calculated as follows:

$$\beta L = \frac{2\pi}{3} \frac{L}{L_{\text{tot}}}. \quad (7.15)$$

$R_R$ of the transmission line model is set to 800 $\Omega$ in order to match the return losses at the feed of the model with the simulated $S$-parameters of the IFA. The accuracy of the model is identified by the impedance $Z_T$ at the tuning point of the antenna. After all required parameters are extracted, $Z_T$ is evaluated numerically and compared with the 3D-EM simulated model at 1.8 GHz and 2.7 GHz, which are the second and third-order harmonics of a low-band signal. The corresponding reflection coefficient of the transmission line model and 3D-EM simulation at the aperture tuning point with 50-$\Omega$ normalization impedance is shown in Fig. 7.3. Based on the obtained results, the general behavior of the transmission line model matches with the 3D-EM model. The discrepancy between the curves is related to the strong abstraction of the transmission line model, which does not cover all the high-order effects in the
7.3 Physical Design of the IFA

IFA. Using Eq. (7.4) and (7.5) the power of the second and third harmonics transferred to the feed and $R_R$ is numerically evaluated. The value of the voltage drop $V_R$ over $R_R$ at the open end of the antenna is chosen arbitrarily, since it defines only the absolute power of the harmonics but does not impact the course of change over the positions of the tuner and is set to 0.2 V. The second and third harmonics transferred to the feed and $R_R$ over the position along the antenna are plotted in Fig. 7.4 [101].

The numerical evaluation starts from 20 mm, which is 5 mm away from the feed point simulating virtually the impedance tuning case and ends at the open end of the antenna, meaning 70 mm away from the short. Applying the aperture tuner at the low-RF voltage plane (in other words, close to the feed)
results in the lowest harmonics generation at the expense of reduced sensitivity performance of the tuning system, which increases for the high-voltage plane and is experimentally demonstrated in [120]. Therefore, it is recommended to find local minima at larger distances away from the feed. According to Fig. 7.4, such minimum for example in the power of the second harmonic coupled into the feed of the IFA ($P_{TF}$) exists, when the tuner is attached 44 mm away from the short. At this point, the power of the second harmonic is reduced by roughly 15 dB and therefore this point is suitable for tuner placement in CA front-end, which shares the same main antenna for down- and uplink signals. Furthermore, the local minima can be highlighted with the power transfer coefficient for the second and third harmonics according to Eq. (7.10), Eq. (7.11) and are plotted in Fig. 7.5 [101].

![Graph](image)

**Figure 7.5:** Power transfer coefficient of the second and third harmonics transferred to the feed and $R_k$ over the tuner position.

The local minima in the harmonics coupling response are more noticeable since the dependence of the absolute harmonics power over the position of the tuner is eliminated in this view. For example, placing the aperture tuner 53 mm away from the short, the third harmonic coupled into the feed will improve almost by 15 dB comparing to the position in the range of ±5 mm away from this location. Therefore, it is more beneficial to place the tuner 53 mm away from the short to reduce the coupling of the third harmonic to the front-end circuitry [101].

### 7.4 Hardware Demonstrator – Hardware Toolkit

The antenna demonstrator is fabricated according to the layout configuration in Fig. 7.1(a) and is depicted in Fig. 7.6. Most of the area is covered by a large metal block, which models the chassis of a fully equipped cellular phone.
comprising the mainboard, battery, screen, and metal cover. Despite the simple structure of the proposed hardware demonstrator, it is capable to model all significant effects in the antenna of a real cellular handset [70]. The total size of the hardware demonstrator is $134 \times 70 \text{ mm}^2$, representing the typical size of a mobile phone and is deposited on a FR4 PCB. In order to improve flexibility and enable quick reconfiguration, the hardware demonstrator contains drill holes with 1-mm diameter placed in 3 mm raster around the radiating arm and chassis. The holes along the radiating arm define the fixed positions where the feed, short, and aperture tuning networks can be connected to the antenna. Besides this, the holes represent the ports of the antenna in the 3D-EM simulation. The feed and aperture tuning network are implemented on dedicated PCBs with a total size of $10 \times 17 \text{ mm}^2$ and contains also drill holes for fixing the board at the antenna by means of screws, as shown in Fig. 7.6 [101]. Such structure enables the discrete positioning of the tuning elements in a 3 mm raster. The backside of the feed and tuning PCBs has no solder resist to ensure a good contact with the chassis and radiating arm of the antenna. The feed board comprises a sub-miniature push-on connector (SMP). According to the 3D-EM simulation, the holes and screws in the radiation arm and chassis do not distort the fundamental behavior of the antenna up to at least 3 GHz, because no current is flowing through the screws since the boards are contacted bottom-to-top with each other [101]. The proposed hardware demonstrator combines application-level assemblies with IC-level sensing features. The demonstrator enables quick reconfiguration since all tuning components are mechanically attached to the antenna by means of screws instead of soldering as in most demonstrators presented to date. Apart from
reconfigurability and flexibility, the hardware demonstrator provides some extra features such as the measurement of the impedance at the aperture tuning point by using a second instance of the feed board instead of the aperture tuning board. Furthermore, the back-to-back connection of the feed and tuning board enables measuring the one-port response of the tuning board instance used in the prototype antenna tuning system [117].

7.5 Harmonics Measurement of an Aperture-Tuned IFA

For the verification of the analytical findings, an aperture tuning circuit comprising a high-voltage RF switch with 80 V target voltage handling and shunt high-Q 27 nH SMD inductor has been designed for measurements. The RF switch is fabricated in a dedicated bulk-CMOS technology. For measurements, we assume the frequencies of the main tone, the second and the third harmonics to be 900 MHz, 1.8 GHz, and 2.7 GHz, respectively [101]. The assembled hardware toolkit including short, feed and tuning board is demonstrated in Fig. 7.7.

![Photograph of the assembled hardware toolkit.](image)

Figure 7.7: Photograph of the assembled hardware toolkit.

First, the load impedance $Z_T$ at the aperture tuning point is measured by removing the tuning board and mounting a second instance of a feed board instead. The measurements were performed by sweeping the position of the second feed board between the feed and the open end of the antenna. The input reflection coefficient $S_{11}$ at 1.8 GHz and 2.7 GHz has been recorded and evaluated in a dedicated circuit simulator. During measurement, the feed is terminated by a 50-Ω impedance. The comparison of the evaluated measurement results of the reflection coefficient with the 3D-EM simulated and transmission line model is demonstrated in Fig. 7.8 [101]. Considering the Smith chart plots in Fig. 7.8, the transmission line model provides a
Figure 7.8: Comparison of the measured, simulated, and calculated reflection coefficients corresponding to the impedance $Z_T$ over the position of the tuning network at 1.8 GHz (left) and 2.7 GHz (right).

reasonably good hardware-to-model correlation. Some discrepancies between the simulated and measured reflection coefficient are presumably caused by the influence of the second feed board mounted on the antenna, which has not been considered in the simulation setup. The nonlinear performance of the aperture-tuned IFA is investigated with the measurement setup sketched in Fig. 7.9 [101].

Figure 7.9: Measurement setup for evaluating the harmonics along the radiating arm of the antenna.
An RF signal at 900 MHz is applied to the antenna feed via a diplexer, the second and third harmonics reflected to the feed are measured at the high-pass output of the diplexer by a spectrum analyzer as sketched in Fig. 7.9. The high-voltage RF switch is operating in off-state during the measurement. The position of the aperture tuning board is swept between 33 mm and 69 mm away from the short and the second and third harmonics coupled back to feed are recorded. The results are plotted in Fig. 7.10. According to the obtained curves the optimal locations for reducing the coupled second and third harmonic into the CA RF front-end are 42 mm and 51 mm. Depending on the requirements, it is recommended to place the tuner between the two minima for optimal nonlinear performance. The position of the measured local minima fits very well with the calculated minima. The predictions provided in this chapter correlates well with the measurements. Apart from that the measured harmonics correlates also with the impedance at the aperture tuning point, generating the lowest harmonics level, when the impedance at the respective frequency is low. Some differences in the slope and absolute power level of the harmonics are related to the fact that the nonlinear behavior of the practical switch is not exactly following the polynomial behavior assumed in Eq. (7.8) and (7.9) [101].

![Figure 7.10: Comparison of the measured and calculated second and third harmonics reflected to the feed.](image)
8 RF Voltage Detector with Low Harmonic Feedback for Antenna Tuning Switches

An RF voltage detector with reduced harmonic feedback into the sensed RF path for the use in highly linear, high-voltage antenna aperture tuning switches is demonstrated in this chapter. The voltage detector is implemented and tested in hardware with two high-voltage RF switches, where the ICs were manufactured in the Infineon 130 nm RF switch process. The proposed voltage detector integrated into the antenna aperture tuning switch targets RMS RF voltage monitoring function without degrading the nonlinear performance of the switch. In other words, the voltage detector shall not introduce harmonic distortions beyond the level of the intrinsic RF switch. The general block diagram of the proposed IC is demonstrated in Fig. 8.1 [116].

![Block diagram of the voltage detector including coupled harmonics to the RF path.](image)

**Figure 8.1**: Block diagram of the voltage detector including coupled harmonics to the RF path.

8.1 Description of the Voltage Detector

Voltage detectors are usually based on rectification circuits. Several implementations are known in the art of voltage multipliers or charge pump circuits constructed from diodes. Since charge pump circuits based on diodes are not compatible with standard CMOS technology, the diodes have to be replaced by MOSFETs, where the gate terminal is shorted with the drain terminal [121]. Rectification circuits implemented by charge pumps are intrinsically nonlinear providing a nonlinear input impedance. The more nonlinear the response is, the higher sensitivity has the charge pump. However, this contradicts with the requirements for linear RF switches. Consequently, linearization of the charge pump is required [116]. The general architecture of a voltage detector
based on the Dickson charge pump is shown in Fig. 8.2 [122]. For describing the behavior of the given structure in Fig. 8.2 in terms of sensitivity and harmonics, only the left half is considered under bias conditions. The values of the bias voltage $V_{\text{bias}}$ and $V_{\text{out}}$ are chosen such, that all transistor operating in saturation region in the DC operating point. Since the structure of the voltage detector is symmetrical, the same conditions can be applied to both sides by only changing the signs. First, we focus on the Dickson charge pump without linearization elements in Fig. 8.2.

![Figure 8.2: General architecture of the voltage detector without linearization.](image)

For the negative half-wave of the input signal the transistors operate in saturation region, thus the gate-source voltage equals to the drain-source voltage in $M_1$ and $M_2$. For the positive half-wave, the transistor may transit into the cut-off. Such operation indicates a quadratic dependence of the input current from the input voltage generating strong harmonic content, which becomes more noticeable at larger input voltage amplitudes [80]. The input current $I$ is described as follows:

$$I_{d,1} = \frac{\mu_n C_{\text{ox}}}{2} (V_{gs,1} - V_{tn})^2 (1 + \lambda V_{ds,1}).$$ (8.1)

In order to minimize the harmonic content linearization elements as shown in Fig. 8.3(a) and Fig. 8.3(b) are introduced. The transistors $M_1$ and $M_2$ in Fig. 8.2 can be replaced by these structures. During the negative half-wave of the input signal the transistors with linearization element also operates in active region. The resistors in series to the MOSFET device provide linearization effect reducing the harmonic content of the input current. The improvement in linearity is achieved scarifying the sensitivity of the voltage detector. As the linearity improves, the sensitivity drops due to the reduced transconductance of the linearized diode [116].

The linearization structure shown in Fig. 8.3(b) provides the improvement of the trade-off between the harmonic content and sensitivity [123]. Initially the transistors $M_1$ and $M_2$ are biased at the saturation region, meaning that:

$$V_{ds,\beta} = V_{gs,\beta} - V_{R_{\text{Lin}}} = V_{gs,\beta} - I_{d,\beta} R_{\text{Lin}} > V_{ov,\beta},$$ (8.2)
8.1 Description of the Voltage Detector

where $V_{ov,\beta}$ is the overdrive voltage of $M_1$ and $M_2$. The value of the linearization resistance $R_{Lin}$ is specified such that there is some room left for the drain-source voltage $V_{ds}$ to avoid $M_1$ and $M_2$ from transitioning into the triode operation region at low input amplitudes of below 0.1 V. At input amplitudes below 0.1 V the MOSFETs operates similar to the circuit in Fig. 8.2 in saturation region providing a comparable I-V response where the drain-current $I_{d,\beta}$ is expressed as:

$$I_{d,\beta} \approx \frac{\mu n C_{ox}}{2} (V_{gs,\beta} - V_{tn})^2 (1 + \lambda V_{ds,\beta}).$$  \hspace{1cm} (8.3)

If the output resistance of the $M_1$ and $M_2$ is infinite, the response of the transistors in Fig. 8.2 equals to the circuit with linearization element in Fig. 8.3(b):

$$I_{d,1} = I_{d,\beta} \quad \text{if} \quad \lambda = 0. \hspace{1cm} (8.4)$$

According to Eq. (8.4), both the Dickson charge pump and linearized charge pump may provide the same transfer gain at low input voltage amplitudes. In reality, the channel length modulation coefficient $\lambda$ is not zero resulting in a lower gain of the linearized circuit. The MOSFETs of the linearized charge pump are driven by the voltage drop on $R_{Lin}$ to the triode region with increasing input voltage amplitudes. As a result, the transfer gain drops, but the circuit generates low harmonic content at the input compared to the Dickson charge pump without linearization element. The harmonic content is reduced due to the more linear input impedance. At such high input voltages, the drop in transfer gain creates no drawbacks at the application level since there are no stringent requirements to the sensitivity at such operation conditions. The sensitivity is high enough to distinguish the RF voltage at the switch within the appropriate limits of $\pm 1$ V. The simulated input currents over the applied input voltage of the detector with and without linearization elements are plotted in Fig. 8.4 [116]. For the sake of simplicity only the low frequency response of the circuit is considered. The simulation proves that the transfer gain between the Dickson charge pump without linearization and applied linearization circuit according to Fig. 8.3(b) is almost the same at low input voltage amplitudes. At high voltage amplitudes the current to voltage
response becomes straight, effectively reducing the harmonic content in the input current. Taking the simulation as shown in Fig. 8.4 and the theoretical findings into account, the proposed detector circuit with linearization element in Fig. 8.3(b) provides the best trade-off regarding linearity and transfer gain for the application in RF high voltage antenna aperture tuning switches [116].

8.2 Circuit Design of the RF Switch with Integrated Voltage Detector

Two prototype ICs for evaluating the concept of linearized voltage detector are designed in the Infineon 130 nm RF switch technology. The first IC comprises a shunt RF switch designed for target 80 V RF operation, whereas a 40 V class handling RF switch is implemented in the second IC. The circuit diagram for both RF switches is shown in Fig. 8.5 [116]. The first switch is composed of 32 MOSFETs stacked in series, where the ratio $W/L = 7 \text{ mm}/130 \text{ nm}$. The second switch comprises 17 MOSFETs stacked in series, each sized as $W/L = 2.9 \text{ mm}/130 \text{ nm}$. The size of the switches are scaled such to provide the same $R_{on}C_{off}$ ratio. Each MOSFET forms a parasitic capacitance $C_{sub} = 5.8 \text{ fF}$ to the high-ohmic substrate, which is responsible for the uneven voltage distribution along the stack. In order to equalize the voltage distribution along the stack, MIM capacitors are added in parallel to the channel of the respective MOSFETs as sketched Fig. 8.5. The values of the capacitors are calculated with Eq. (5.14). The numeric values for the 80 V switch starting from the hot side are $C_{80,32} = 2.867 \text{ pF}$, $C_{80,31} = 2.697 \text{ pF}$ etc. For the 40 V switch the equalization capacitors starting from the hot side are $C_{40,17} = 0.310 \text{ pF}$, $C_{40,16} = 0.276 \text{ pF}$.
8.2 Circuit Design of the RF Switch with Integrated Voltage Detector

etc. Both switches are biased via a ladder of high-ohmic resistors at the gate and drain-source nodes, where \( R_{DS} = 20 \, \text{k}\Omega \), \( R_G = 400 \, \text{k}\Omega \), \( R_{G,C} = 100 \, \text{k}\Omega \). The switches are driven by the gate control voltage \( V_G \) of \(-2.4\,\text{V}\) and \(+3.3\,\text{V}\) for off- and on-state, respectively [101]. The RF signal is applied at the \( RF_{in} \) terminal, which is the hot side of the switch. Simultaneously, the RMS RF voltage at \( RF_{in} \) has to be sensed by the voltage detector. The proposed voltage detector is not capable of handling high RF voltage amplitudes. Therefore, a linear capacitive voltage divider \( C_1 - C_2 \) is attached between the \( RF_{in} \) terminal and \( V_{in} \) to scale down the voltage before applying to the voltage detector. In order to avoid additional capacitances at the \( RF_{in} \) node the value of \( C_1 \) is fixed to 10 fF and \( C_2 \) depends on the voltage handling class of the intrinsic switch. For the 80 V switch the value of \( C_2 \) is chosen to 550 fF and the voltage at the input of the voltage detector corresponds to 1.8% of the total voltage at the RF line. For the 40 V switch the value of \( C_2 \) is 200 fF reducing the voltage at the RF line to 4.8% of the applied RF voltage. The capacitor \( C_2 \) is physically implemented as a MIM capacitor and \( C_1 \) as a metal capacitance between top-most metal layers providing breakdown voltage well above 80 V.

The voltage detector is biased via the voltage \( V_{bias} \) and the 100 k\Omega resistor \( R_{bias} \). The fabricated IC is demonstrated in Fig. 8.6(a). The voltage detector as well as the voltage divider are connected to the switch SW1 as shown in Fig. 8.6(a). For measuring the difference in harmonics between the switch

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**Figure 8.5:** Circuit diagram of the designed prototype.
with and without detector, the same switch SW2 is placed on the right side of the die as a reference [116].

### 8.3 Evaluation of the RF Switch with Voltage Detector

The fabricated ICs were flip-chip mounted on a PCB (see Fig. 8.6(b)) for measurement. The measurements are conducted in the setup as shown in Section 6.2.1. The RF input power at the 80V-DUT is swept from 20 dBm to 41 dBm, corresponding to the peak voltages between 6.32 V and 70.96 V, whereas the input power of the 40V device is swept till 35 dBm, which equals to the peak RF voltage of 35.56 V. In order to prevent the switch from breakdown, the peak RF voltages do not reach the 40 V and 80 V breakdown voltages of the switches. The recorded second and third harmonics over the applied peak RF voltage for each DUT with and without detector are shown in Fig. 8.7 and Fig. 8.8 [116]. According to both measurements, the detector have no significant influence on the nonlinear performance of the intrinsic switch. Keeping a close eye on the plots, the switch attached to the voltage detector generates slightly lower level of harmonics, which may be related to the slightly higher input capacitance for the DUT with connected voltage detector to it. The measured DC output voltage of the voltage detectors for both variants is presented in Fig. 8.9. Both implementations reach roughly the value of 1.3 V and the sensed output voltage increases linearly with the input peak RF voltage [116].
8.3 Evaluation of the RF Switch with Voltage Detector

Figure 8.7: Measured second and third harmonics of the 80 V DUT with and without detector.

Figure 8.8: Measured second and third harmonics of the 40 V DUT with and without detector.

Figure 8.9: Recorded DC output voltage of the voltage detector.
8.4 Application Example on the Hardware Demonstrator

A basic two-state aperture tuning circuit based on the fabricated IC is designed for the hardware demonstrator. The aperture tuner is composed of an off-chip high-Q SMD inductor attached parallel to the \( RF_{in} \) terminal of the IC. The assembled application board, including short, feed, and aperture tuning board is shown in Fig. 8.10. To achieve parallel resonance at cellular low-band frequency of 960 MHz, the value of the inductor is calculated as follows [101]:

\[
\omega = \frac{1}{\sqrt{LC_{\text{off}}}}.
\]  

(8.5)

The off-capacitance \( C_{\text{off}} \) of the switch IC, including the switch core capacitance, the shielded pad capacitance, the PCB, contacts, and wiring parasitic is approximately 1 pF. Considering the target operation frequency and \( C_{\text{off}} \), the inductor is calculated to be 27.48 nH. The high-Q 27 nH SMD inductor LQW45AN27NG80 is used in the aperture tuning circuit. The target is to cover low-, mid-, and high-band of the cellular frequency spectrum. Moreover, the voltage along the radiating arm should be sensed at different aperture tuning points [101].

![Figure 8.10: Configuration of the hardware demonstrator.](image)

Before the return loss at the feed is measured, the small-signal measurement setup is calibrated by a custom short-open-load (SOL) kit assembled on the feed board. The SOL kit is composed of a 0-Ω jumper, an empty board, and a 50-Ω resistor soldered between the antenna feed contact and the ground plane at the backside of the feed PCB for short, open and load, respectively. The measured return loss at the antenna feed of the antenna configured according to Fig. 8.10 in off- and on-state of the aperture tuning device is plotted in
Fig. 8.11. The aperture-tuned antenna covers upper low- and high-band cellular frequencies in off-state of the switch and mid-band in the on-state. The first case is appropriate for the CA scenario in which the downlink high-band signal is combined with the uplink low-band signal. The discrepancies between measured and simulated return loss is associated to the inaccuracies of the simulation model for the aperture tuning network due to the simplified layout parasitics of the tuning board. Apart from that, the simplicity of the tuning network and only two tuning states limits the frequency response, particularly the return loss at the feed do not reach the 6 dB target, relatively narrowband frequency response or decentering of the impedance match with respect to the center frequency of the band. The measured peak RF voltage along the radiating arm is plotted in Fig. 8.12 [101].

Figure 8.11: Measured and simulated return losses at the feed of the antenna in off- and on-state of the aperture tuner device.

Figure 8.12: Measured peak RF voltage over the position of the tuner.
The power at the feed of the antenna is set to 34 dBm. The voltage along the radiating arm increases from the feed to the open end, reaching 76 V at the right-most point. The corresponding measured voltage at the output of the voltage detector is 1.776 V. The measurements are obtained by moving the aperture tuning network next to the feed point towards the open end of the antenna, where the movement have no influence to the return loss, thus the peak of the return loss at the feed remains due to the parallel resonance of the network at 960 MHz [101].
9 Integrated Circuit for Decoupling and Tuning of Inverted-F Antennas

MIMO implementations require spatial separation and high RF isolation between the antennas. Approximately a half-wavelength distance between the MIMO antennas should be maintained [124], meaning for a mid-band signal at 2 GHz a spatial separation of 75 mm is needed. Since the antennas are integrated in the housing, the required distance cannot be always maintained in modern handheld cellular equipment. Because of the limited space inside the device, the spatial separation of the antennas decreases, and the impact of mutual coupling increases notably, thus reducing the system benefit of MIMO [124]. Therefore, decoupling techniques between the antennas or at each input port are utilized enabling the reduction of the distance between the antennas to less than 0.1 times of the wavelength [125]. Various decoupling techniques have been investigated in the recent years. Decoupling techniques can be typically classified as circuit-based or geometry-based methods. For example, the multiport conjugate matching is a circuit-based decoupling technique, which involves the utilization of decoupling and matching networks for simultaneous decoupling and matching [126]. Ground plane modifications, the neutralization line technique and the use of parasitic scatters are examples of geometry-based methods. However, these approaches operate usually across a narrow bandwidth [126]. An attempt to increase the operational bandwidth by extended ground plane decoupling method is presented in [127]. In this chapter, an IC for decoupling of MIMO antennas as well as for aperture and impedance tuning is demonstrated. The IC is based on high-voltage RF switches and switchable MOS capacitors, also known as C-Tuners. The IC decouples the adjacent stripes of the IFA forming two separate IFAs for MIMO operation in mid- and high-band cellular frequencies. For low-band operation, the IC connects the stripes, forming a single IFA with double physical length and at the same time disables the MIMO configuration. An application example is shown in Fig. 9.1 [128].

9.1 Architecture of the IC

First, we consider the topology of the IC as sketched in Fig. 9.1. The IC is constructed from series and shunt switches as well as a 2-bit C-Tuner. The IC can be attached between two radiating arms of an IFA and can also be interposed between the RF source and the feed of the antenna, serving as an impedance tuning network [128]. The approach aims at covering low-,
Figure 9.1: Application example with reconfigurable IFA for low-band SISO and mid-/high-band MIMO configuration.

mid- and high-band cellular frequencies. For this purpose, the series switch is closed for low-band tuning connecting the two radiating arms by a low-ohmic path with each other. This extends the total physical length of the antenna and increases the antenna efficiency. Moreover, the C-Tuner operates in its highest capacitive state to extend the electrical length furthermore and to achieve good matching at low-band cellular frequencies at the RF feed point of the antenna. While targeting low-band operation, the shunt switch operates in off-state [128]. For cellular mid- and high-band the series switch operates in off-state, thus decoupling the antennas and enabling MIMO. One antenna is aperture-tuned by the C-Tuner to the desired frequency bands and the sufficient isolation between the antennas is ensured by the on-state shunt switch. Such operation connects the left end of the second antenna directly to the chassis and provides a high isolation between both antennas. Additionally, the isolation can be further improved with off-chip passive SMD components. Apart from that, a second RF signal source for the second antenna can be attached via the proposed IC. The RF signal is coupled via the series switch to the RF line. The C-Tuner enables impedance matching and tunes the antenna to the desired frequency bands without further aperture tuning. The ability to address decoupling and tuning functionality by a single switch structure makes the IC universal and proves the flexibility on the application level [128].

9.2 Circuit Design of the IC

The circuit diagram of the designed chip including the transistor parameters is shown in Fig. 9.2. The IC comprises two switches SW₁, SW₂, a 2-bit C-Tuner implemented by the switches SW₃ and SW₄ as well as additional voltage detectors VD₁ and VD₂ attached to the RF pins for sensing the RF voltage. The series switch SW₁ is connected between the RF₁ and RF₂ terminal of the
9.2 Circuit Design of the IC

Figure 9.2: Circuit diagram of the designed decoupling and matching IC.

IC. The shunt switch SW2 is coupled to the $RF_2$ pin and the C-Tuner to the $RF_1$ pin. The RF signal is conducted via the $RF_1$ terminal if the IC is used for impedance tuning of the second antenna. The values of the biasing resistors and fixed MIM capacitors for the two switchable branches of the C-Tuner are provided in Table 9.1 [128].

Table 9.1: Values of the biasing resistors and fixed MIM capacitors of the C-Tuner.

<table>
<thead>
<tr>
<th>$R_G$</th>
<th>$R_{DS}$</th>
<th>$R_{G,C1}$</th>
<th>$R_{G,2}$</th>
<th>$R_{DS,C}$</th>
<th>$C_{MSB}$</th>
<th>$C_{LSB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 kΩ</td>
<td>20 kΩ</td>
<td>100 kΩ</td>
<td>100 kΩ</td>
<td>100 kΩ</td>
<td>7.8 pF</td>
<td>3.8 pF</td>
</tr>
</tbody>
</table>

9.2.1 Decoupling and Tuning IC: RF Switches

The transistor width of SW1 is intentionally chosen large. For the use between two antennas, a high-impedance switch could be more appropriate. Since the chip should not only be interposed as an antenna decoupling element but also as an impedance matching network at the feed of the second antenna, a low-ohmic switch is designed [128]. The IC is designed for a maximum RF
voltage handling of at least 45 V between the RF pins and ground. Therefore, all switches SW1, SW2, SW3 and SW4 are constructed from 25 MOSFETs stacked in series. The smallest switch in the design is SW4 of the C-Tuner, which has the worst ratio between the off-state capacitance and substrate capacitance $C_{\text{sub}}$ leading to the strongest disbalance in the voltage distribution among all switches in the design. The imbalance of the voltage distribution at SW4 is compensated by applying equalization technique to this particular switch. MIM capacitors are connected between the drain and source terminals of each transistor [128]. The value of the equalization capacitors is calculated by Eq. (5.14) starting from the hot side $C_{eq,25} = 243 \text{ fF}$, $C_{eq,24} = 221 \text{ fF}$ etc [128].

### 9.2.2 Decoupling and Tuning IC: C-Tuner

The 2-bit C-Tuner is constructed from two switchable branches in series with fixed MIM capacitors $C_{\text{MSB}}$ and $C_{\text{LSB}}$. In order to achieve the target 45 V voltage handling, four MIM capacitors are stacked in series. The tuner is adjusted with $C_{\text{min}}/\Delta C/C_{\text{max}} = 0.3 \text{ pF}/1 \text{ pF}/3.3 \text{ pF}$. The crucial parameters are the $Q$-factor and the minimum capacitance value and are directly related to the characteristics of the switch in the C-Tuner. The minimum capacitance value in the lowest state of the C-Tuner is limited by the $C_{\text{off}}$ of the switches, whereas the $Q$-factor is limited by the on-resistance. In order to achieve constant $Q$-factor for all tuning states, the width of the transistors for each branch are binary-weighted. The minimum capacitance value can be expressed as follows [129], [130]:

$$C_{\text{min}} = \sum_{k=1}^{m} \frac{C_{\text{off}}C_{\text{MIM,MSB}}}{2^{k-1}(C_{\text{off}} + C_{\text{MIM,MSB}})},$$  \hspace{1cm} (9.1)

where $m = 2$ is the resolution of the C-Tuner, $C_{\text{MIM,MSB}}$ is the largest capacitance in the switchable branch of the tuner.

### 9.2.3 Decoupling and Tuning IC: Full-Chip Verification

The general functionality of the designed IC is tested by performing a full-chip-verification (FCV). The block-diagram of the testbench and an example of the simulated response are shown in Fig. 9.3. The chip is controlled by a two-wire series interface ($\text{CLK}$ and $\text{DATA}$), and $\text{chip select (Sel)}$. For verification, the gate and body voltages are saved during the simulation. Furthermore, the VIO current, as well as the control voltages are observed. First, the switch is powered up. After powering up the extended registers are programmed with the second command. The third frame sets SW2 and SW4 in on-state. The
gate and body voltage of both switches jump close to 3.3 V and 0 V after the command, as depicted in Fig. 9.3. The fourth data block sets SW1 and SW3 into on-state and SW2 and SW4 into the off-state. The last command set all switches into off-state.

Figure 9.3: Testbench and FCV of the proposed decoupling and matching IC.

9.3 Evaluation of the Decoupling and Tuning IC

The fabricated IC as shown in Fig. 9.4 comprises an RF circuit constructed from the series switch between the RF pins, shunt switch and C-Tuner as well as a control unit for programming the device.

Figure 9.4: Die photograph of the designed decoupling and matching IC.

9.3.1 Large-Signal Measurements

The IC is flip-chip mounted onto a PCB for measurements. For the evaluation of the nonlinear performance, the RF signal was applied to the $RF_2$ terminal with $RF_1$ shorted to ground, meaning the measurements are performed in
shunt mode using the harmonic measurement setup. The measured second and third harmonics at the output of the diplexer are shown in Fig. 9.5 [128]. The IC has got damaged at the applied RF voltage magnitude of 47 V. According to the measurements, the IC reached the target 45 V handling, demonstrating the harmonic level of about $-40$ dBm at 45 V input. It should be noted, that the chip is measured in complete off-state, meaning all switches are off and the C-Tuner is set to the lowest capacitive state [128].

### 9.3.2 Small-Signal Measurements

The small-signal parameters $C_{\text{off}}$, $R_{\text{on}}$, as well as the $Q$-factor and the capacitance values of the C-Tuner $C_T$ were evaluated based on the measured two-port $S$-parameters. The measurements were performed on the evaluation board shown in Fig. 9.6 [128].
Fig. 9.7 shows the equivalent circuit of the IC in on- and off-state for extracting the small-signal parameters from measured $S$-parameters. $C_{\text{off}}$ and $C_T$ for different states can be calculated according to Fig. 9.7(a) as follows:

$$C_{\text{off,SW1}} = -\mathcal{Z}\left\{ \frac{Y_{12}}{\omega} \right\}$$
$$C_{\text{off,SW2}} = \mathcal{Z}\left\{ \frac{Y_{11}}{\omega} \right\} + \mathcal{Z}\left\{ \frac{Y_{12}}{\omega} \right\}$$
$$C_T = \mathcal{Z}\left\{ \frac{Y_{22}}{\omega} \right\} + \mathcal{Z}\left\{ \frac{Y_{12}}{\omega} \right\}$$

(9.2)

The evaluated results and the Q-factor are plotted in Fig. 9.8. The minimum capacitance of the C-Tuner is around $330 \text{ fF}$ and reaches its maximum at $3.3 \text{ pF}$. The peaks in the curves denote series self resonance frequency. Between cellular low- and mid-band frequencies, the $Q$-factor reaches the maximum of 20 and 40 [128].

The on-resistance $R_{\text{on}}$ of the series switch SW1 and the shunt switch SW2 can be evaluated according to the equivalent two-port network in Fig. 9.7(b) and Fig. 9.7(c), where the switches in the IC are assumed to be in on-state. The $R_{\text{on}}$ for both switches is described by Eq. (9.3) and Eq. (9.4) and are $2.2 \Omega$ for the series switch SW1 and $1.4 \Omega$ for the series switch SW1 at low-band frequencies [108]:

$$R_{\text{on,SW1}} = \Re\left\{ 50\Omega \frac{1 + S_{11}}{1 - S_{11}} \right\} - 50 \Omega$$

(9.3)

$$R_{\text{on,SW2}} = \Re\left\{ 50\Omega \frac{1 + S_{11}}{1 - S_{11}} \right\}$$

(9.4)
9 Integrated Circuit for Decoupling and Tuning of Inverted-F Antennas

![Graphs showing capacitance values and Q-factor for all states of the C-Tuner.](image)

**Figure 9.8:** Measured off-capacitance of the switches, capacitance values and Q-factor of the C-Tuner for all states.

## 9.4 Reconfigurable Inverted-F Antenna for MIMO

As mentioned, the chip reconfigures the physical length of the IFA, making the antenna longer for cellular low-band operation and splitting the antenna in two IFAs for cellular mid/high-band MIMO operation. The hardware demonstrator is based on the approach presented in Chapter 7. For MIMO operation the radiating arms of the handle board is cut in the middle as shown in Fig. 9.9(a). The decoupling and matching network (DMN) is attached between both antennas and the right arm of the antenna is fed by a second instance of the IC [131].

![Diagram of MIMO operation showing the modified handle board and the circuit diagram of the decoupling and tuning system.](image)

**Figure 9.9:** (a) Modified handle board for MIMO operation and (b) circuit diagram of the decoupling and tuning system.
9.4.1 Design of the Decoupling and Matching Network

The MIMO demonstrator targets to operate in the cellular low- and mid-band, at 750 MHz and 2 GHz, respectively. Fig. 9.9(b) shows the detailed circuit diagram of the DMN including the MIMO IFA. In order to improve the radiation efficiency and the return loss of the antenna in cellular low-band, the switch SW1 is closed when the system operates in low-band, meaning both radiating arms are connected together increasing the physical length of the antenna. Meanwhile, the C-Tuner operates in the highest state to maximize the electrical length of the antenna and achieve good matching in cellular low-band frequencies. The matching in low-band is further improved by the high-Q off-the-shelf SMD inductor $L_1 = 4.7$ nH. In MIMO operation the second feed is excited via another instance of the same IC to the right radiating arm. While operating in low-band, the series switch of the second instance is open, meaning no RF signal is applied to the antenna. For comparison of the radiation efficiency in low-band and isolation in mid-band two antenna configurations, single-stripe and dual-antenna as sketched in Fig. 9.10, are simulated using an 3D-EM simulation. The latter is targeting MIMO operation, where both antennas are isolated from each other and independently tuned to the desired frequency bands [131].

![Diagram](image)

**Figure 9.10:** (a) Low-band configuration with long radiating arm and (b) MIMO mid-band configuration with separated radiating arm.

The antenna efficiency simulation in Fig. 9.11 proves the necessity of using a single radiating arm for low-band operation. According to the simulation results, the radiation efficiency of the long antenna created by the proposed IC is 5% higher compared to the MIMO configuration in Fig. 9.10(b). This is partly achieved due to the simplicity of the matching of the long IFA in cellular low-band. Considering the simulation results, the implementation of MIMO technique in cellular low-band with two antennas along the short side of the cellular device might be inefficient [131]. Therefore, MIMO is implemented starting from mid-band in which the series switch SW1 of the first IC operates in off-state, meaning the switch is open and the antennas are separated. The feed is attached to the right radiating arm, as shown in Fig. 9.9(b). The second RF signal is fed to the antenna via the impedance matching network (MN) coupled in series with the IC. For MIMO operation both radiating arms have
to be matched to the same cellular mid-band frequency. If the antennas are successfully matched to the same desired frequency point simultaneously, the mutual coupling between the antennas increases. In order to maximize the isolation between the antennas, a short connection is provided to the chassis at the second radiating arm right after the open end of the first radiating arm. For this purpose, the shunt switch SW2 of the IC interposed between the antennas operates in on-state \[131\]. The left antenna is matched by the DMN to cellular mid-band frequencies. The return loss in mid-band is improved by the high-Q SMD inductor $L_2$ connected between the antennas. Furthermore, the inductor protects the front-end electronics from the system-level ESD stress, which may occur at the radiating arm of the antenna. The value of $L_2$ is chosen 1.5 nH and the C-Tuner of the first IC is set to the highest state, namely to the largest capacitance value of 3 pF \[131\]. The radiating arm on the right is matched by the impedance MN at the feeding point. The capacitance value of the C-Tuner is programmed to 1 pF and the shunt switch SW2 operates in off-state. The circuit diagram of the MN shown in Fig. 9.9(b) improves the return loss in cellular mid-band at 2 GHz. The value of the capacitor $C_1$ is 1.1 pF, the inductors $L_3$ and $L_4$ are 2.2 nH and 1.5 nH respectively \[131\]. The isolation between the concepts presented in Fig. 9.9(b) and Fig. 9.10(b) is compared with simulations. According to the results plotted in Fig. 9.12 both concepts provide sufficient isolation. However, taking the investigations made in this section into account, the MIMO antenna configured with the DMN improves the low- and mid-band return loss, providing a slightly better radiation efficiency and fulfilling the isolation requirements \[131\].
9.4.2 Design of the Hardware Prototype of the MIMO System

A single PCB is designed for decoupling and matching as well as feeding of the second antenna. The top- and bottom-view of the PCB is depicted in Fig. 9.13. In order to ensure a good contact to the handle board, the backside has no solder resist.

![Figure 9.13: Top- and bottom-views of the PCB for DMN and MN.](image)

The PCB also comprises drill holes for mechanically fixing the board with screws to the antenna. The PCB is configured with SMD components and jumper. For the use as a feeding element, a miniature SMP push-on connector is used [131]. The photograph of the final assembled demonstrator is shown in Fig. 9.14. The most left point A of the IFA is shorted to the ground by a fixed metal stripe. The first feed is located at the left radiating arm 12 mm away from the short, at the point B. The DMN is attached between the radiating arms with a distance of 30 mm to the fixed short (point C). The second feed is connected via the second instance of the same PCB to the second radiating element 60 mm away from the fixed short at point D. The second PCB includes an impedance matching network to tune the left antenna to the desired frequency bands [131]. The chips are configured by a controller using two-wire MIPI interface [132].
9.4.3 Measurement Results

First, the one-port calibration of the measurement setup is fulfilled by a custom SOL kit assembled on the feed board. The measured return loss for low- and mid-band operation are demonstrated in Fig. 9.15(a) and Fig. 9.15(b). In low-band operation the antenna covers the bandwidth between 710 MHz and 750 MHz sustaining the target 6 dB return loss limit. When configured to operate in mid-band MIMO mode, both antennas cover the bandwidth 1.9 GHz–
2.1 GHz. The isolation in mid-band MIMO mode is plotted in Fig. 9.15(c) demonstrating an isolation of around 19 dB, which is a reasonable value given the low distance between the antennas [131]. For comparison, the decoupling technique based on transmission lines in [133] provides an isolation of 11 dB. The extended ground plane approach in [127] demonstrates an isolation of roughly 15 dB.

Figure 9.15: Measured return loss at (a) low-band and (b) mid-band as well as (c) isolation in mid-band MIMO mode.
10 Hybrid C-Tuner for 40V/80V Antenna Aperture Tuning Applications

One possible embodiment of aperture tuner devices is the switch-based tunable capacitor, also known as C-Tuner. Similar to high-voltage RF switches, C-Tuners are also separated between mid-voltage and high-voltage handling class devices. The voltage handling and tuning range requirements for C-Tuners are inversely related to each other, thus the mid-voltage handling class device provides larger tuning range compared to high-voltage handling class aperture tuner devices due to the different sensitivity to the shunt capacitive loading of the antenna. At the low-ohmic plane the upper capacitance value is defined to reach up to 10 pF, which offers a good trade-off between the tuning sensitivity and power losses at the low-ohmic aperture tuning plane [120]. On the other hand, the capacitance range of up to 3 pF might be sufficient at the high-ohmic plane, since the impedance at the tuning point is high, thus the sensitivity at this tuning point is increased [129]. At the same time, high-voltage tuners, including C-Tuners are intended to achieve very low minimum capacitance values in order to minimize the parasitic capacitive loading of the antenna and avoid undesired resonances in the aperture tuner topologies comprising off-chip inductors [92]. A monolithically integrated hybrid C-Tuner for antenna aperture tuning applications in handheld cellular devices is demonstrated in this chapter. The proposed hybrid C-Tuner topology is capable of fulfilling all requirements for mid-voltage and high-voltage handling classes in one single design with no penalty in RF performance compared to conventional aperture tuner devices. To the extent of authors knowledge, there are no aperture tuning devices published up to date that can address both 40 V and 80 V class requirements within a single design. Fig. 10.1(a) shows an application example of the proposed hybrid C-Tuner, where one tuner is attached close to the open end and the other one close to the feed. In the state-of-art tunable antenna system, such configuration requires two different types of tuners, optimized for mid- and high-voltage operation. The aperture-tuned antennas cover low-, low-mid, mid- and high-band cellular frequency bands [92].

10.1 Architecture of the Hybrid C-Tuner

First, we consider the general block diagram of the hybrid C-Tuner shown in Fig. 10.1(b) and Fig. 10.1(c). The tuner is composed of two functionally equivalent branches $C_L$ and $C_R$, where each branch is constructed from three
binary-weighted capacitors in series with the proportionally scaled RF MOS switches. $C_L$ and $C_R$ are accessed from outside by the pins $RF_1$ and $RF_2$ and wired on the application board according to the required voltage handling. Each branch is designed to handle peak voltages of up to 40 V. If 80 V handling is required, the two branches are excited in series such that the voltage drop at each branch does not exceed 40 V. For operation at the high-voltage tuning plane the IC is excited from the $RF_1$ pin, while the $RF_2$ pin is left floating according to Fig. 10.1(b). At the mid-voltage tuning plane, the C-Tuner operates in shunt configuration, where the IC is excited from the $RF_2$ pin and $RF_1$ pin is grounded on the application level as sketched in Fig. 10.1(c). In shunt operation, the C-Tuner can handle voltages of up to 40 V. If we assume, that $C_L$ equals to $C_R$: $C = C_R = C_L$, the corresponding total capacitance in 80 V operation is $C^{(80)} = C/2$, while in 40 V operation mode the maximum capacitance value of the C-Tuner is quadrupled due to the parallel connection of the two tunable branches $C_L$ and $C_R$: $C^{(40)} = 2C$. Such maximum capacitance scaling between mid- and high-voltage operation fulfils the application requirements for the respective tuners and the quadrupled capacitance values in the shunt mode enable fine tuning capabilities as well as flexibility on the application level, because the large tuning range in shunt mode enables
covering the low-band cellular frequency band with fine tuning steps. Both mid- and high-voltage tuners utilize similar silicon area for the RF switches to maintain constant series resistance per unity capacitance. Therefore, both 40 V and 80 V C-Tuners achieve similar Q-factor, which can be expressed by Eq. 10.1 [92]:

$$Q_C = \frac{1}{\omega R_{esr} C},$$  \hspace{1cm} (10.1)

where $R_{esr}$ is the equivalent series resistance of the capacitance $C$ and is mainly defined by the on-resistance of the switch branch. In 40 V mode the total capacitance is doubled and the $R_{esr}$ is halved, whereas in 80 V operation mode the total capacitance is halved but the $R_{esr}$ is doubled with respect to the single tunable branch resulting in equal $Q_C^{(80)} = Q_C^{(40)}$ [92].

### 10.2 Circuit Design of the Hybrid C-Tuner

The simplified circuit diagram of the designed hybrid C-Tuner including all parameters and used components is provided in Fig. 10.2. The widths of the transistor in each capacitive branch are binary weighted and the two switches on the bottom of the diagram constructed from the MOSFETS $M_{E1}$ and $M_{E2}$ provide ESD protection [10]. In order to fulfil the voltage requirements, equalization capacitors are added to each channel of the MOSFETs. The values of the equalization capacitance in the branch $C_R$ can be calculated by Eq. (5.14). The substrate capacitance of the single transistor in the respective switch is accurately extracted from a 3D-EM simulation. The 3D-EM model of the hybrid C-Tuner is portrayed in Fig. 10.3. The excited (hot) side of the C-Tuner branch $C_R$ is always at the $RF_2$ pin in both operating nodes, while the excited side for the left branch $C_L$ depends on the operation mode and is $RF_1$ if the C-Tuner operates in 80 V mode (series mode) and $RF_2$ in the 40 V mode (shunt mode). This makes equalization according to Eq. (5.14) impossible [92]. Considering the undefined hot side location, the switch stack size for the left branch $C_L$ of the IC is increased, comprising 18 stacked MOSFETs and 16 stacked MOSFETs in the right branch $C_R$ as shown in Fig. 10.2. Besides that, some reduced equalization capacitors are connected to the first 5 transistors in stack, where $C_{eq,Sx,18} > C_{eq,Sx,17} > ... > C_{eq,Sx,14}$. In the following description of the hybrid C-Tuner we use series mode for 80 V mode and shunt mode for 40 V. Another challenge in the design of the hybrid C-Tuner is the finite parasitic shunt capacitor at $RF_2$ formed by the application board pad, while operating in series mode. The parasitic capacitor has a crucial impact on the voltage distribution along the stack in series mode. It should be noted that the $RF_2$ pin in series mode is kept floating. The influence of the pad
Figure 10.2: Simplified circuit diagram of the hybrid C-Tuner with $R_G = R_{DS} = 20 \, \Omega$ and $C_{eq,pad} = 3.37 \, pf$.

Figure 10.3: 3D-EM model of the hybrid-C tuner for evaluating the substrate capacitance.

shunt capacitance is compensated by the ESD switch and the capacitors $C_{pad}$ added to the ESD transistors $M_{E1}$. The goal is to realize an equal voltage drop at each branch, while operating in series mode. In other words, the voltage drop at $RF_2$ is aimed to be half of the applied RF voltage at the $RF_1$ pin of the IC. The required single compensation capacitance $C_{pad}$ is estimated by various 3D-EM iterations and is calculated to be 168.5 $\mu$F. The evaluated capacitor is distributed along the ESD transistors $M_{E1}$ resulting in the total capacitance value $C_{eq,pad} = 20 \times 168.5 \, \mu F = 3.37 \, \mu F$. Due to $C_{pad}$ no further
equalization is required for the ESD transistors $M_{E1}$. The capacitance range of the C-Tuner is defined by the fixed linear metal capacitors of 0.8 pF, 1.6 pF and 3.2 pF connected to each switchable branch. In the mid-voltage handling class device, the C-Tuner is controlled by the total of 6 digital voltages $V_{G,S1} - V_{G,S6}$ resulting in a tuning range of $C_{\text{min}}/\Delta C/C_{\text{max}} = 668 \text{ fF}/83 \text{ fF}/6 \text{ pF}$. In series mode the equal RF voltage drop on $C_L$ and $C_R$ must be provided, which is achieved by setting $C_L = C_R$. Therefore, the switches are controlled in pairs such that $V_{G,S1} = V_{G,S4}$, $V_{G,S2} = V_{G,S5}$ and $V_{G,S3} = V_{G,S6}$, resulting in effective 3-bit resolution with $C_{\text{min}}/\Delta C/C_{\text{max}} = 371 \text{ fF}/178 \text{ fF}/1.8 \text{ pF}$. The simulation results of the capacitance values versus the tuner state of both shunt and series mode are shown in Fig. 10.4 [92].

![Simulated capacitance values over the tuning states in shunt and series mode configurations.](image)

**Figure 10.4**: Simulated capacitance values over the tuning states in shunt and series mode configurations.

### 10.3 Evaluation of the Hybrid C-Tuner

The IC is fabricated in a dedicated SOI-CMOS RF switch technology and mounted on two different PCBs for small- and large-signal measurements. The total size of the packaged IC is $1.1 \times 1.5 \text{ mm}^2$. The large signal measurements are performed by the testboard demonstrated in Fig. 10.5(a). The C-Tuner IC can be configured according to Fig. 10.5(b) and Fig. 10.5(c) for operating in either one or other voltage class using the same board. For operation in series mode, the $RF_1$ pin is shorted to the RF line via a 0-Ω jumper and the $RF_2$ pin is kept floating as shown in Fig. 10.5(b). The configuration for shunt operation is depicted in Fig. 10.5(c). The $RF_2$ pin is connected to the RF line via a 0-Ω jumper and the $RF_1$ pin is directly grounded on the PCB. The evaluation board for small-signal measurements is composed of two RF lines directly connected to $RF_1$ and $RF_2$ pins of the C-Tuner IC. The small-signal
10 Hybrid C-Tuner for 40V/80V Antenna Aperture Tuning Applications

parameters of the tuner in series and shunt mode are evaluated from recorded S-parameters of the two-port network. The RF lines of the PCB were carefully de-embedded for measurements [92].

10.3.1 Large-Signal Measurement Results

The large-signal measurements are performed with the harmonic measurement setup. An RF signal at 900 MHz is applied to the PA and the output power is swept between 20 dBm to 43 dBm and 48 dBm for the tuner in shunt and series mode, respectively. The corresponding peak RF voltages are 45 V and 89 V over the C-Tuners. The measured power of the second and third harmonics for series and shunt mode is plotted in Fig. 10.6. The voltage handling capabilities of the designed C-Tuner are indicated by the abrupt increase of the harmonics level at 44 V and 85 V. The results prove, that the design target for 40 V and 80 V class is fulfilled. During the measurements, the C-Tuner is set to the lowest state, meaning all switches operating in off-state. This is explained by the fact, that in aperture tuning applications the largest RF voltage is expected to appear at the highest impedance of the C-Tuner. This happens when the tuner operates in the lowest capacitive state [92].
10.3.2 Small-Signal Measurement Results

The measured two-port $S$-parameters are fed to a circuit simulator for evaluating the tuning range and the Q-factor of the hybrid C-Tuner. The capacitance response for all states at 900 MHz and 1800 MHz are plotted in Fig. 10.7(a) and Fig. 10.7(b). The minimum capacitance value in series mode is measured to be 371 fF and reaching the maximum of 1.8 pF. The tuning range in 40 V mode is measured 668 fF for the lowest state and 6 pF for the highest state. The measurement of the capacitance values matches very well with the simulations. The Q-factor over the frequency in both operation modes is presented in Fig. 10.7(c) and Fig. 10.7(d). Both series and shunt operation mode show similar $Q$-factor reaching a maximum of 25 at about 800 MHz [92].

10.4 Quad-Band Inverted-F Antenna System Tuned by Hybrid C-Tuner

The proposed C-Tuner is tested on the hardware demonstrator. Two instances of the hybrid C-Tuner are attached to the low- and high-ohmic plane of an antenna at the same time. A photograph of the assembled hardware prototype is shown in Fig. 10.8. The hardware demonstrator aims covering low- , low-mid-, mid- and high-band cellular frequency ranges. Therefore, an aperture tuning network for the mid- and high-voltage planes are constructed including the hybrid C-Tuner and parallel high-Q shunt inductors according to the circuit diagram in Fig. 10.1. The shunt inductors connected to the RF line of the aperture tuning board enable resonating out the minimum capacitance value of the C-Tuner at low-band cellular frequencies and additionally protect the

\[\text{Figure 10.6: Measured nonlinear response and voltage handling capabilities of designed C-Tuner in shunt and series operation.}\]
IC from system-level ESD stress, which may occur at the radiating arm of the antenna. Similar to the aperture tuning network, shunt inductors are added to the feed in order to further improve the return loss at the desired bands and protect the front-end ICs from system-level ESD. The inductor at the feed and RF line of the mid-voltage device $L_{T,40}$ is a 15 nH off-chip high-Q SMD part. The inductor at the RF line of the high-voltage device is $L_{T,80} = 27$ nH. The tuners in the application example are independently controlled by a common two-wire interface as sketched in Fig. 10.8. A photograph of the complete measurement setup is shown in Fig. 10.9 [134]. The small-signal response of the prototype is measured in free space. The recorded 64 return loss curves at the feed of the upper antenna comprising the mid-voltage tuner and 8 curves of the lower IFA constructed from the high-voltage aperture tuner is shown in
Figure 10.8: Photograph of the assembled quad-band tunable antenna system demonstrator.

Figure 10.9: Photograph of the antenna measurement setup.
Fig. 10.10(a) and Fig. 10.10(b) respectively. The target return loss of 6 dB at the feed of the integrated antenna is achieved over most of the desired frequency range. The antenna system obtains complementary coverage of 4-bands of the cellular spectrum by utilizing only two tuners [134].

Furthermore, the quadrupled tuning range and high resolution of the hybrid C-Tuner operating in shunt mode provides the coverage of the complete cellular low-band with fine tuning steps [134]. Additionally, the isolation between the two antenna feeds is measured and plotted in Fig. 10.10(c). From the measurements it can be obtained, that the isolation is well above 20 dB over the target frequency bands. This is explained by the sufficient spacial separation of the two antennas, which may enable efficient low-band MIMO implementation with the proposed system [134].
11 Conclusion and Outlook

Conclusion

CMOS-based high-voltage RF antenna tuning circuits are widely used in modern cellular phones aimed at improving radiation efficiency and frequency coverage of integrated antennas. In the current work nonlinearities in shunt aperture tuning RF switches operating in off-state, influence of the substrate capacitance, a de-embedding method for accurate, repeatable and reproducible measurements, and an approach for extending the core functionality of aperture tuning circuits are investigated. Several antenna tuning circuits based on CMOS RF switches and aperture tuning systems using a hardware demonstrator are implemented. The research focuses mainly on the harmonic distortion of the core circuit and the antenna tuning system. All theoretical findings are verified either with measurements of the designed ICs or on the application level using the hardware demonstrator.

The main achievements of the work are summarized below.

1. A substrate capacitance model for MOSFET-based RF switches based on microstrip and inverted microstrip lines is investigated. The model-to-hardware correlation fits well with the predictions and all first-order effects are reproduced reasonably well. The demonstrated models can be used for rapid design of antenna tuning circuits based on CMOS RF switches in two popular package technologies (wire-bonded and flip-chip).

2. A linearity analysis of shunt high-voltage RF switches for antenna tuning applications operating in off-state with the focus on second- and third-order nonlinear products as a function of the RF switch geometry is demonstrated in this work. The proposed analysis for estimating the ratio in second- and third-order nonlinear products correlates reasonably well with the measurements and predicts the trend in nonlinear performance.

3. A de-embedding method based on OPEN de-embedding for accurate, repeatable, and reproducible measurement of off-state equivalent resistance and capacitance for shunt antenna tuning circuits mounted on PCB is proposed. The method is suitable being a primer choice for the characterization of state-of-art or next-gen antenna tuning circuits with even lower power losses and off-capacitances in sub-100 fF range.
4. Considerations for the harmonic distribution in aperture-tuned IFA for cellular phones using the first-order transmission line model for identifying the local minima of the harmonic distribution for a given use case is presented in this research work. Theoretical findings are proved on a hardware demonstrator comprising a mechanically-reconfigurable IFA and an RF switch-based aperture tuning network. An example of harmonics optimization by over 10 dB for the carrier aggregation RF front-end by fine-selecting the position of the tuner at the antenna is demonstrated.

5. The core functionality of aperture tuning circuits is extended by a voltage detector with reduced harmonic feedback into the sensed RF path. The measured voltage detector exhibits a linear transfer characteristic and the generated nonlinearities are below the intrinsic RF switch. The voltage detector enables sensing of the RF voltage distribution along the excited antenna.

6. An IC for decoupling MIMO antennas as well as for antenna tuning and a hybrid C-Tuner for 40V/80V antenna aperture tuning applications are demonstrated in this thesis. The first approach enables designing a less complex and more efficient matching network compared to short antennas, while providing the true MIMO operation at frequencies from mid-band onwards. The hybrid C-Tuner fulfils the requirements for both mid- and high-voltage handling classes in one single design, offering an universal solution for capacitive aperture tuners. It facilitates the flexibility of tuning network design and reduces the number of different components used in the antenna tuning system.

**Outlook**

The demand for higher data rates in modern communication devices is still increasing. The next telecommunication standard is already in the starting gates. The RF performance of antenna tuning circuits is primarily defined by the used technology and extensive effort is required to further improve the performance on circuit design level. This work focuses on investigation of circuit design and modelling techniques for RF switches in CMOS technologies allowing incremental improvement in RF performance and functionality. Disruptive technologies, such as PCM, offer superior RF performance, particularly in terms of $R_{on}C_{off}$ figure of merit. This technology has a potential to offer significant performance boost for future RF switches, reconfigurable RF components and is aimed to be investigated as next.
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Published Papers


9. O. Özdamar, R. Weigel, A. Hagelauer, and V. Solomko, "An Integrated Circuit for Decoupling and Tuning of Inverted-F Antennas in Cellular


Patents

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The main and diversity antennas of modern cellular user equipment are integrated into the chassis of the device. Due to the limited space inside the device and high complexity of front-end electronics, the integrated antennas have small form factor, which leads to low radiation efficiency and high mismatch losses. The performance of the antennas is optimized with aperture tuning techniques. Commercial aperture tuners in modern cellular user equipment are based on high-voltage RF switches in bulk- or SOI-CMOS technologies. The focus of this research is put on the analysis of the second and third order nonlinear products caused by the RF switch, the influence of the substrate capacitance and the hardware characterization of antenna tuning ICs. Additionally, the functionality of the RF switch is extended and novel RF switch-based tuning ICs in CMOS technologies are investigated. All theoretical findings are verified either with measurements of the designed ICs or on the application level using a hardware demonstrator.