

**Investigations of the electrical activity of defects in
group IV and group III-N alloys
integrated on Si substrates**

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Dedicated to my grandmother

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**1934 †2019*

who would have liked to learn more

Abstract

The hetero-integration of group IV and III-V epitaxial layers on silicon (Si) substrates enables the fabrication of novel devices for optoelectronic and high-power applications. However, lattice and thermal mismatches between the Si substrate and the grown epi-layer lead to an unavoidable formation of defects in hetero-epitaxy. The consideration of these defects is of great importance in semiconductor devices as they affect various material properties and impair the device performances. Besides the structural characterization of the unintentional introduced defects and the question of its origin, it is essential to evaluate their electrical activity in order to correctly describe their impact on the device performance.

This work explores the electrical activity of threading dislocations (TDs) in Ge-rich SiGe heterostructures integrated on Si substrates as well as the electrical active defects introduced by the growth of aluminium-nitride (AlN) seed layers for the integration of gallium-nitride (GaN) on Si substrates.

I applied two different device structures, p-n⁺ junction diodes and metal-oxide-semiconductor (MOS) capacitors, in order to assess the electrical properties of grown-in TDs in Si_{0.06}Ge_{0.94}/Ge/Si heterostructures. I demonstrated a defect-related p-type conductivity of intrinsically grown Si_{0.06}Ge_{0.94}/Ge heterostructures that reaffirms previous work of similar intrinsic Ge-based material. Moreover, I detailed the threading dislocation related leakage currents in rectifying devices, revealing a power law dependence on the threading dislocation density (TDD). By a variation of temperature I determined the dominant mechanism of transport of this leakage currents in different temperature regimes, for which I suggested possible interactions with TD related defect states including trap-assisted tunneling at room temperature, band-to-band tunneling at lower temperatures and Shockley-Read-Hall generation at higher temperatures. Based on the relation between generation and recombination lifetimes I estimated an energy level of included defect centers located at mid-gap position that shifts towards the band edges with an increasing number of TDs. Through the reduction of leakage currents in the fabricated MOS capacitors I was able to examine an effective carrier concentration of 5-6x10¹⁵ cm⁻³ in the nominally intrinsic Si_{0.06}Ge_{0.94} epitaxial layer in a temperature range between 50 K and 200 K, which decreases down to 1x10¹⁵ cm⁻³ in the Ge buffer underneath. By applying deep level transient spectroscopy (DLTS) I found one dominant hole trap at mid-gap position confirming the presence of an TD-related effective generation-recombination center in the Si_{0.06}Ge_{0.94}/Ge heterostructure. In addition, I investigated the hole trapping kinetics of this defect level and associated it with point defects that are trapped in the strain field around threading dislocations.

I obtained insights into defect formation in the Si substrate and at the AlN/Si interface in

dependence of the AlN growth temperature. A low temperature growth step prevented a deep in-diffusion of Al atoms into the Si substrate with simultaneous increase of the maximal p-type doping in the vicinity of the AlN/Si interface. Furthermore, I found a bulk hole trap inside the Si substrate at mid-gap position that showed an increase in density by applying a low temperature growth step. In contrast, the defect states at the AlN/Si interface decreased when a low temperature growth step was applied, in comparison to AlN layers grown at continuous high temperatures.

Zusammenfassung

Die Heterointegration von epitaktischen Schichten bestehend aus Gruppe IV und Gruppe III-V Elementen auf Silizium (Si) Substraten ermöglicht die Herstellung von innovativen Bauelementen für optoelektronische- und Hochleistungsanwendungen. Jedoch führen Gitterfehlpassungen und Unterschiede in den Wärmehausdehnungskoeffizienten zwischen dem Si Substrat und den aufgewachsenen epitaktischen Schichten zur unvermeidbaren Einbringung von Defekten bei der Heteroepitaxie. Die Berücksichtigung dieser Defekte in den Halbleiterbauelementen ist von großer Bedeutung, da sie verschiedene Materialeigenschaften beeinflussen und die Funktionsweise der Bauteile beeinträchtigen. Neben der strukturellen Charakterisierung der entstehenden Defekte und der Frage nach deren Entstehung, ist es unerlässlich deren elektrische Aktivität zu untersuchen, um deren Einfluss auf die Bauteilperformance korrekt beschreiben zu können.

Diese Arbeit untersucht die elektrische Aktivität von Durchstoßversetzungen in Silizium-Germanium (SiGe) Heterostrukturen mit hohem Germanium (Ge) Anteil, gewachsen auf Si Substraten, wie auch die elektrisch aktiven Defekte, welche durch das Wachstum von Aluminiumnitrid (AlN) Schichten entstehen, die dazu genutzt werden um Gallium-nitrid (GaN) auf Si Substraten zu wachsen.

Ich verwendete zwei verschiedene Bauteilstrukturen (p-n⁺ Dioden und Metall-Oxid-Halbleiter (MOS) Kondensatoren) um die elektrischen Eigenschaften von Durchstoßversetzungen in Si_{0,06}Ge_{0,94}/Ge/Si Heterostrukturen zu untersuchen, welche durch Heteroepitaxie entstanden sind. Ich konnte eine defektbedingte p-Dotierung in den undotiert gewachsenen Si_{0,06}Ge_{0,94}/Ge Schichten nachweisen, was frühere Arbeiten auf vergleichbaren undotierten Ge-basierten Materialien bestätigte. Darüber hinaus habe ich die versetzungsabhängigen Leckströme in gleichrichtenden Bauteilen detailliert beschrieben, wobei eine Potenzgesetzabhängigkeit von der Versetzungsdichte festgestellt wurde. Durch eine Variation der Temperatur konnte ich die dominierenden Transportmechanismen der Leckströme bestimmen und habe mögliche Interaktionen mit den versetzungsbedingten Defektbändern beschrieben. Diese beinhalteten Störstellen unterstütztes Tunneln bei Raumtemperatur, direktes Tunneln von Bandkante zu Bandkante bei niedrigeren Temperaturen und Shockley-Read-Hall Generation bei höheren Temperaturen. Anhand des Verhältnisses von Generation- und Rekombinationlebensdauer konnte ich die energetische Lage der Defektbänder im Zentrum der Bandlücke lokalisieren, welche sich zu den Bandkanten hin verschiebt wenn die Versetzungsdichte zunimmt. Durch das erfolgreiche Unterdrücken der Leckströme in MOS Kondensatoren bestimmte ich eine effektive Ladungsträgerkonzentration in der eigentlich intrinsischen Si_{0,06}Ge_{0,94} Schicht in Höhe von $5\text{-}6 \times 10^{15} \text{ cm}^{-3}$ im Temperaturbereich zwischen 50 K und 200 K. In der darunter liegenden Ge-Pufferschicht sank diese Ladungsträgerkonzentration auf $1 \times 10^{15} \text{ cm}^{-3}$ ab. Mit Hilfe von

Transientenspektroskopie tiefer Störstellen (DLTS) bestimmte ich eine löchereinfangende Störstelle in der Mitte der Bandlücke, die das Vorhandensein eines versetzungs-bedingten Generation-Rekombinationszentrum in der untersuchten $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ Heterostruktur bestätigte. Zusätzlich untersuchte ich die Löchereinfangkinetik des gefunden Defektlevels und ordnete es daraufhin Punktdefekten zu, die im Spannungsfeld der Durchstoßversetzungen lokalisiert sind.

Ich gewann Kenntnisse über die Bildung elektrisch aktiver Defekte im Si Substrat und an der AlN/Si Grenzfläche in Abhängigkeit von der AlN Wachstumstemperatur. Ein zusätzlicher Wachstumsschritt bei verringerter Temperatur verhinderte das tiefe Eindringen von Al Atomen in das Si Substrat im Vergleich zum AlN Wachstum bei konstant hoher Temperatur, wohingegen gleichzeitig die maximale Dotierung in der Nähe der AlN/Si Grenzfläche anstieg. Des Weiteren beobachtete ich ein Defektlevel im Si Substrat, das sich in der Mitte der Bandlücke befindet. Die Konzentration dieses Defektlevels nimmt zu wenn der zusätzliche Wachstumsschritt bei verringerter Temperatur durchgeführt wird. Im Gegensatz dazu nehmen die Defekte an der AlN/Si Grenzfläche ab bei Anwendung des zusätzlichen Wachstumsschrittes bei verringerter Temperatur.

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Papers

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1

Introduction

Semiconductor materials always contain defects, whether caused by foreign atoms incorporated into the host material or disturbances of the periodic crystalline structure. Foreign atoms, so-called impurities, can be introduced intentionally to act as dopant atoms primarily or unintentionally during crystal growth and device processing. Nowadays, silicon (Si) substrates can be fabricated with high quality and purity by various techniques such as the Czochralski method [1] and float-zone process [2]. Impurities like metallic contaminations after growth are below a density of 10^{10} cm^{-3} and densities of typically 10^{10} - 10^{12} cm^{-3} can be achieved after subsequent processing in the microelectronic industry [3]. It appears quite differently if hetero-epitaxial growth is applied to fabricate semiconductor devices. The aim is to integrate the hetero-epitaxial layers in the existing Si industry-platform for optoelectronic devices [4, 5, 6] and high-power applications [7, 8]. Lattice and thermal mismatches between the Si substrate and the grown epi-layer lead to the formation of stress in the material. Such stress itself, the process of relaxation beyond a critical thickness or contaminations during crystal growth are unavoidable sources for defect formation in hetero-epitaxy. The consideration of defects is of great importance in semiconductor devices as they determine various properties of the related materials. The resistivity and conductivity can be precisely controlled by impurity doping as well as the dopant diffusion is affected by included defects. Furthermore, the minority-carrier lifetime and reliability of devices are strongly corrupted by defects. In addition, the optical and optoelectronic properties of semiconductor devices are influenced by the presence of defects. Therefore, one of the challenges in semiconductor hetero-integration is the control of unintentional introduced defects, so that they do not accidentally affect the material properties as well as impair the device performances [3].

Defects in semiconductor materials are in general terms any form of deviation from perfection in crystal structures and can be classified according to their dimensions. Here, *zero-dimensional defects* include all kinds of point defects, like vacancies, interstitials and substitutionals. They are divided into intrinsic and extrinsic defects, whereby the imperfections are caused by atoms of the host material or foreign atoms, respectively. Line defects like dislocations are attributed to *one-dimensional defects* since the disturbance of the crystal lattice is extended along a line. If the disorder extends into a further dimension (plane), as for stacking faults

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or grain boundaries e.g. in polycrystalline material, the corresponding defects are grouped to *two-dimensional defects*. Large-scale defects like precipitates or voids consist in the most cases of an agglomeration of point defects in a certain volume, because they are ascribed to *three-dimensional defects*. As the structure of two- and three-dimensional defects can be considered an extension of zero- and one-dimensional defects, this work distinguishes between point and extended defects. For better visualization, the most frequently appearing types of defects are sketched in Fig. 1.1. A detailed overview on this topic can be found in [9, 10].

Point defects includes the substitution of an atom for another on a given lattice site, the absence of an atom or the position of an atom between two sites in a crystalline structure. The lack of a lattice atom is known as vacancy and is intrinsic to materials. While in elemental semiconductors there exists only one type, compound materials can have vacancies on each position of different participating atoms. Substitutional atoms can be either impurities that are not equal to the host material atoms and therefore referred to as extrinsic defects or antisites that are intrinsic to compounds when an atom of one sublattice is replaced by another. Interstitials can be impurities or atoms similar to the host material, so that they can be described as both intrinsic and extrinsic defects. Only point defects exhibit a sufficiently low formation energy to emerge in thermal equilibrium, while extended defects only occur during crystal growth (grown-in defects) or in subsequent processing (process-induced).

As described above, *extended defects* are classified by their number of dimensions in which they extend. Given the importance for this work, particular attention will be drawn to dislocations as representative for line defects. Here, the displacement of atoms leads to a distortion of the crystal lattice along a line. Dislocations are characterized by a line vector l , directed along the dislocation, the Burger's vector b that indicates the direction and amount of displacement for creating the dislocation and a glide plane, along which the dislocation can move. Dislocations can glide in the direction of the Burger's vector when an external force is applied. The angle between l and b determines the type of dislocation. In *edge dislocations*, b is perpendicular to l , that is why they are also called 90° dislocations. Here, an extra plane of atoms is inserted into the lattice. If b is parallel to l , the dislocation is of screw character with an angle of 0° . A *screw dislocation* can be visualized by shifting a cylinder of a certain material volume in height with respect to the surrounding lattice. The most common type are *mixed dislocations* with the the Burger's vector neither perpendicular nor parallel to l (0° - 90°), as they have partially edge-like and screw-like character. The lateral extension of the distortion due to a dislocation is framed within the first few atom spacing from the dislocation line and decreases with $1/r$, where r is the distance from the dislocation line. In addition, a dislocation can never end within the bulk, it either terminates at surfaces or interfaces instead. Dislocations that nucleate at the interface during epitaxial growth by partially releasing the accumulated strain in a pseudomorphic epi-layer are called misfit dislocations. Frequently associated with such misfit dislocation are threading dislocations running through the entire epi-film up to the free surface. Such threading arms can move from their nucleation point when an

external force is applied by creating long misfit dislocations at the interface. Sources for threading dislocations are fixed defect sources originating from substrate imperfections, surface half loops that are nucleated by inhomogeneities of the epi-layer surfaces [11] or multiplication processes by e.g. Frank-Read sources, which pin the dislocation and create a loop by expanding until it closes itself [12].

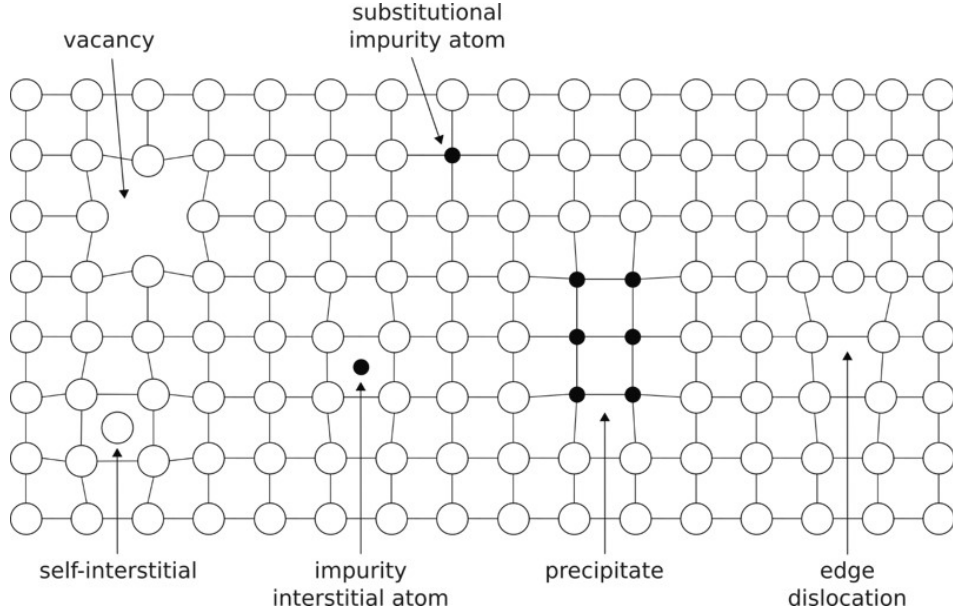


Figure 1.1: Sketch of crystal defects after [13].

Defects will not only impact the properties of the host material and corresponding devices, they also have intrinsic properties. The structural characteristics describe the location, shape, identification of the crystal imperfections and their origin, while the electronic properties determine the electrical activity of defects such as the position of defect states in the band structure and their interaction with free carriers. Even though the formation and structural characterization of defects in semiconductors are intensively studied in the past, there are still open questions regarding their electrical activity, especially in semiconductor heterostructures for novel device applications.

The aim of this thesis is to investigate the electrical activity of defects that result from hetero-epitaxial integration of III-V and group IV alloys on silicon substrates. In particular, the role of threading dislocations in Ge-rich SiGe/Ge/Si heterostructures for optoelectronic applications and the defect-related early vertical breakdowns in AlGaIn/GaN high-electron-mobility transistors (HEMTs) on Si substrates are investigated. In order to evaluate the electrical activity of incorporated defects, basic devices (p-n junctions and MOS capacitors) were fabricated that are as similar as possible to the final devices, but nevertheless reliably measurable by electrical characterization techniques. For this purpose, current-voltage (I-V) and capacitance-voltage (C-V) measurements as well as deep level transient spectroscopy (DLTS) are applied.

1.1 Thesis Outline

After introducing the role of defects in semiconductor heterostructures and their distinction of a structural point of view, chapter 1 further deals with the theoretical background of the electrical activity of defects in semiconductor materials. Here a difference has been made between point and extended defects. The physics of the two main basic devices studied, p-n junctions and metal-oxide-semiconductor (MOS)-capacitors, is explained in more detail and the principle of the applied electrical characterization techniques, I-V and C-V measurements along with DLTS is introduced.

In *chapter 2* the achieved results of studying the electrical activity of threading dislocations in Ge-rich SiGe heterostructures integrated on Si(001) are presented. Firstly, the increasing relevance of Ge- and Ge-rich SiGe-based alloys for a variety of novel applications and the need for a CMOS-compatible implementation is discussed. Furthermore, the defect-related type of background doping of intrinsically grown $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures is revealed by electrical measurements. By means of temperature dependent I-V analysis, the mechanisms of current leakage in p-n junction diodes induced by threading dislocations are investigated. Deep level transient spectroscopy on MOS-capacitors is used to evaluate threading dislocation-related defect properties in the investigated material system like densities, trap level energies and capture cross sections.

Chapter 3 includes the outcomes of studying the electrical active defects in AlGaN/GaN HEMT structures integrated on Si. A literature study on the advantages of using the group III-V material system and state-of-the-art research dealing with a premature vertical breakdown observed in AlGaN/GaN/Si HEMTs is presented. Detailed examination of the AlN/Si metal-insulator-semiconductor (MIS) system serves as a first step in understanding the interaction of defects in the complex structure of the heterostructure. Electrical characterizations are carried out in terms of C-V and DLTS measurements to detect included electrically active defects in temperature-dependent deposited AlN layer and their impact on the Si substrates underneath.

1.2 Electrical Activity of Defects in Semiconductor Materials

1.2.1 Point Defects

Point defects are not only altering the periodicity of the crystal structure of semiconductor materials but are also modifying the crystal lattice potential locally and consequently disturbing the energy band structure nearby. This leads to discrete energy levels in the band gap of semiconductor materials that can be responsible for e.g. doping, carrier traps and generation-recombination (G-R) centers and therefore influence the behavior of semiconductor devices. Impurity atoms of a similar chemical structure as the host atoms of the crystal usually cause a small disturbance of the periodic lattice potential and therefore modify the band structures of the host crystal, so-called matrix only to a little extent. Here, shallow defect levels close to the band edges appear. As the matrix changes for example during semiconductor alloying, the defect state changes too and remains shallow in all alloys of the semiconductor. Typical impurities that introduce shallow defect states in semiconductors are dopant atoms. Here, the impurity atoms are chemically similar to the matrix atoms except for the number of valence electrons. Assuming that an extra electron and proton are provided by an impurity atom, this additional electron is nearly free to move except when attracted to the additional proton, which is due to the electrostatic energy. But, this attraction to the positive charge is screened by the existing electrons in the material, so that the free electron is just weakly bound. This weak attraction leads to a defect level state that is only slightly reduced in energy compared to the conduction band. This principle is also known as the “hydrogenic” model where the defect is approximated as a hydrogen atom in the dielectric medium of the semiconductor [9]. Thus, the doping atoms are ionized at room temperature (RT) and the free carriers take part in the conduction band or valence band for n-type and p-type semiconductors, respectively decreasing the resistivity of the material. Sometimes, shallow levels are defined by their energy difference between the defect energy and the corresponding band edge, which is in the order of a few thermal energy units kT of 25 meV at RT, where k represents the Boltzmann constant and T the temperature. As the impurities become chemically more different from the matrix as it is known for foreign atoms and crystal defects, the crystal potential is disturbed to a larger extent and defect states far from the band edges will form. The potential of deep levels is much more localized around the defect resulting in deeper ground state in the middle of the band gap. Such states remain at roughly the same energy even if the band edges move away from or toward the states during alloying. Here, the energy difference between the defect energy and the corresponding band edges is much bigger than kT . Deep levels interact more effectively with free carriers of both types than shallow levels, caused by the increased probability of interaction between carriers and defect states as the state departs from the band edges. While shallow states are generally introduced intentionally during doping of semiconductor materials, deep defect states are often responsible for degradation of semiconductor device performance and yield. They impact forward recombination currents, reverse generation/leakage currents and non-radiative carrier lifetimes of devices, because it is of great importance to control and understand deep level defects [3, 9, 14]. Hence, they are explained in more detail in this chapter.

The need for energy for carriers to overcome the semiconductor band gap and contribute to

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the charge current is reduced by the presence of deep levels caused by splitting the direct band-to-band event into an energetic more favorable two-part process. Depending on the position of deep levels in the band gap and their properties, deep levels may show different interactions with free carriers as shown in Fig. 1.2. A deep level may act as generation center when the carrier density is below its equilibrium value as is the case in the space-charge-region (scr) of reverse-biased p-n junctions and metal-oxide-semiconductor (MOS) capacitors or sufficient energy is provided externally to create electron-hole pairs e.g. by temperature or light. If there exist an excess of carriers in the semiconductor, the deep level may act as recombination center for electron-hole pairs. Defect levels with energies of half the semiconductor band gap, close to the intrinsic energy level, have similar electron and hole emission and capture rates and are called G-R center. In contrast, for defect states with defect levels closer to the band edges one of the emission rates may dominate so that the emission of electrons is increased for centers located in the upper half of the band gap, whereas the emission of holes is the dominant process for centers in the lower half of the band gap. These levels are then called traps. In other words, traps interact with only one of the semiconductor bands, whereas G-R centers interact with both bands via capture and emission processes. In case of high electric fields, electrons can also tunnel through the band gap from the top of the valence band to the bottom of the conduction band by using the deep level as intermediate step, also known as trap-assisted tunneling (TAT). Thus, the carrier generation rate at large electric fields is enhanced by deep level defects.

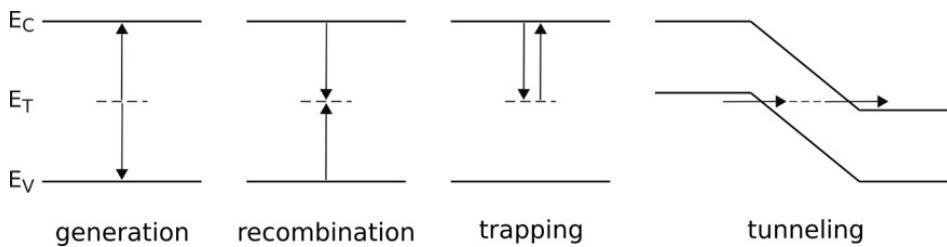


Figure 1.2: Possible interactions of deep levels with the semiconductor bands after [14]

Figure 1.3 shows the four possible processes how electrons and holes can recombine through a trap in the semiconductor band gap. Traps may exist in one of two charge states, either occupied by an electron or a hole. For donors, the trap is neutral if occupied by an electron and positively charged when occupied by a hole. In case of acceptors, the trap is neutral if occupied by a hole and negatively charged by occupation with an electron. There are also different charge configurations possible if two charges of same type are trapped. In the case of Fig. 1.3, the trap will either have a neutral or negative charge state (acceptor) depending on the occupation by a hole or electron, respectively. The neutral trap can either capture an electron from the conduction band (Fig. 1.3a), characterized by the capture coefficient c_n to recombine with the hole in the trap, or the trap emits the hole to the valence band with a hole emission coefficient e_p (Fig. 1.3b) where it can recombine with an electron. In the latter case, an electron will remain in the trap and changes the charge state. If the trap is initially filled with an electron, it can emit the electron back to the conduction band represented by the electron emission coefficient e_n (Fig. 1.3c) and is then free to move by leaving behind a

hole in the trap, or a hole from the valence band is captured with capture coefficient c_p (Fig. 1.3d) and recombine with the electron in the trap.

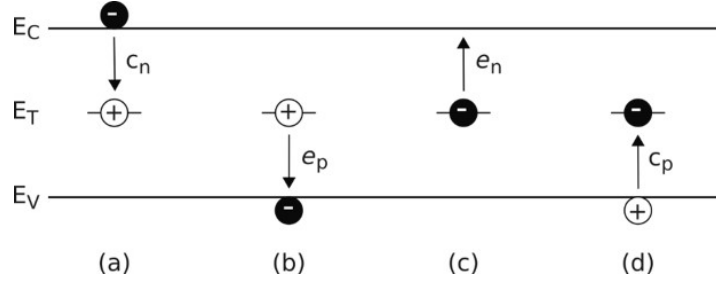


Figure 1.3: Possible processes of recombination via traps: (a) electron capture, (b) hole emission, (c) electron emission and (d) hole capture after [3, 15].

A common way to physically describe the statistics of the processes shown in Fig. 1.3 is based on the Shockley-Read-Hall (SRH) theory [15, 16]. Besides the radiative recombination of carriers from both bands by emitting a photon and the non-radiative Auger recombination in which the excess energy is transferred to a third carrier, the SRH recombination is one of the most relevant processes in semiconductor device operations. The SRH theory describes the steady-state recombination process of electrons and holes through the mechanism of a single-level trapping [17]. Here, the trap is defined by its energy level position E_T in the band gap, the number of traps per unit volume N_T that contribute to the process, n as number of electrons in the conduction band and p number of holes in the valence band, introduced by shallow dopant atoms. For each process schematically drawn in Fig. 1.3, a relation for the corresponding rates R of capture and emission can be expressed [15].

The rate for capturing an electron R_{cn} is proportional to c_n , the average probability per unit time with which an electron can be captured by an empty trap depending on the thermal velocity of the electron v_{thn} and the capture cross-section of the trap σ_n , which describes the probability that an electron is captured by the trap in a certain volume:

$$c_n = v_{thn}\sigma_n \quad (1.1)$$

Capture cross-sections may differ on a large scale depending on the charge state of the trap. A trap featuring a repulsive charge in relation to the majority carriers of the host material has a smaller capture cross-section than a trap that is attractively or neutrally charged; capture cross-sections for neutral traps are approximately in the order of 10^{-15} cm². Additionally, R_{cn} depends on the number of electrons available in the conduction band n and the probability of empty trap states that are ready for occupation by an electron $(1 - f)$. The probability that a trap state is occupied by an electron f is determined by the Fermi-Dirac statistics and depends on the separation between E_T and the Fermi level E_F :

$$f = \frac{1}{1 + \exp(E_T - E_F/kT)} \quad (1.2)$$

$$R_{cn} = v_{thn}\sigma_n n N_T (1 - f) \quad (1.3)$$

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The rate of electron emission from the trap level to the conduction band R_{e_n} is proportional to the number of traps that are occupied by an electron ($N_T f$) and e_n that represents how many electrons per second are emitted from electron-occupied traps:

$$R_{e_n} = e_n N_T f \quad (1.4)$$

The rate for capturing holes from the valence band depends on c_p , again representing the thermal velocity of holes v_{thp} and the hole capture cross-section σ_p , the number of holes in the valence band p and the occupation of traps with electrons ($N_T f$) that are needed for recombination with the captured holes:

$$R_{c_p} = v_{thp} \sigma_p p N_T f \quad (1.5)$$

Lastly, the rate for hole emission is given by eq. 1.6 and is proportional to e_p , the number of holes that are emitted from hole-occupied traps similar to e_n and $N_T(1 - f)$, the number of traps that are occupied by a hole, which can be emitted:

$$R_{e_p} = e_p N_T (1 - f) \quad (1.6)$$

In thermal equilibrium, the net rates of capture and emission processes of either electrons or holes are balanced at each time ($np = n_i^2$):

$$R_{c_n} = R_{e_n}; R_{c_p} = R_{e_p} \quad (1.7)$$

Using eq. 1.3 and 1.4 for electron capture and emission processes, a relationship between e_n and c_n in dependence of the distance between the trap level energy E_T and the intrinsic energy level E_i , can be derived by:

$$v_{thn} \sigma_n n N_T (1 - f) = e_n N_T f \quad (1.8)$$

$$n = n_i \exp \frac{E_F - E_i}{kT}$$

$$v_{thn} \sigma_n n_i \exp \frac{E_F - E_i}{kT} \exp \frac{E_T - E_F}{kT} = e_n \quad (1.9)$$

$$e_n = v_{thn} \sigma_n n_i \exp \frac{E_T - E_i}{kT} \quad (1.10)$$

Similar expression can be derived for the coefficient of hole emission e_p :

$$e_p = v_{thp} \sigma_p n_i \exp \frac{E_i - E_T}{kT} \quad (1.11)$$

It naturally follows from eq. 1.10 and 1.11 that if the trap level coincides with the intrinsic level, the emission rates of electrons and holes are equal. Whereas, if $E_T - E_i$ increases the trap level is closer to the conduction band and consequently the emission of electron e_n is favored while e_p is more improbable. In contrast, the trap is closer to the valence band if $E_i - E_T$ becomes positive, making the emission of holes easier by obstructing the emission of

electrons.

Any deviations from equilibrium condition $np \neq n_i^2$, leads to a constant net recombination rate U_{SRH} to restore the equilibrium. U_{SRH} is defined by Shockley-Read-Hall as [18]:

$$U_{SRH} = \frac{\sigma_n \sigma_p v_{th} (np - n_i^2) N_T}{\sigma_n [n + n_i \exp \frac{E_T - E_i}{kT}] + \sigma_p [p + n_i \exp \frac{E_T - E_i}{kT}]} \quad (1.12)$$

Under steady-state conditions the rate equations 1.3-1.6 are still valid, at least for the low-level injection condition and the net recombination is defined as the difference between captured and emitted carriers:

$$U_{SRH} = R_{c_n} - R_{e_n} = R_{c_p} - R_{e_p} \quad (1.13)$$

$$U_{SRH} = v_{thn} \sigma_n n N_T (1 - f) - e_n N_T f = v_{thp} \sigma_p p N_T f - e_p N_T (1 - f) \quad (1.14)$$

By using the expression for e_n , e_p and making the assumption of equal velocities and capture cross-sections of electrons and holes ($v_{thn} \sigma_n = v_{thp} \sigma_p = v_{th} \sigma$), eq. 1.14 reduces to:

$$v_{th} \sigma n N_T (1 - f) - v_{th} \sigma n_i \exp \frac{E_T - E_i}{kT} N_T f = v_{th} \sigma p N_T n_i \exp \frac{E_i - E_T}{kT} N_T (1 - f) \quad (1.15)$$

$$n(1 - f) - n_i \exp \frac{E_T - E_i}{kT} f = p f - n_i \exp \frac{E_i - E_T}{kT} (1 - f) \quad (1.16)$$

$$n + n_i \exp \frac{E_T - E_i}{kT} = f [n + p + n_i (\exp \frac{E_T - E_i}{kT} + \exp \frac{E_i - E_T}{kT})] \quad (1.17)$$

$$n + n_i \exp \frac{E_T - E_i}{kT} = f [n + p + 2n_i \cosh \frac{E_T - E_i}{kT}] \quad (1.18)$$

Finishing up with the expressions for the probabilities of occupation of trap states by electrons or holes:

$$f = \frac{n + n_i \exp \frac{E_i - E_T}{kt}}{n + p + 2n_i \cosh \frac{E_T - E_i}{kT}} \quad (1.19)$$

$$1 - f = \frac{p + n_i \exp \frac{E_T - E_i}{kt}}{n + p + 2n_i \cosh \frac{E_T - E_i}{kT}} \quad (1.20)$$

Inserting the equations for the occupation probabilities (eq. 1.19, 1.20) into the equation for the net recombination U_{SRH} of electrons lead to:

$$U_{SRH} = R_{c_n} - R_{e_n} = v_{thn} \sigma_n n N_T (1 - f) - e_n N_T f = v_{th} \sigma p N_T (n(1 - f) - n_i \exp \frac{E_T - E_i}{kT} f) \quad (1.21)$$

$$U_{SRH} = v_{th} \sigma p N_T \frac{n(p + n_i \exp \frac{E_T - E_i}{kT} - n_i \exp \frac{E_T - E_i}{kT} n + n_i \exp \frac{E_T - E_i}{kT} - n_i \exp \frac{E_T - E_i}{kT} f)}{n + p + 2n_i \cosh \frac{E_T - E_i}{kT}} \quad (1.22)$$

$$U_{SRH} = v_{th} \sigma p N_T \frac{np - n_i^2}{n + p + 2n_i \cosh \frac{E_T - E_i}{kT}} \quad (1.23)$$

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As can be seen from eq. 1.23, the net recombination rate due to traps is proportional to the term $np - n_i^2$. If this term is greater than zero ($np > n_i^2$) then U_{SRH} is dominated by recombination and if the term becomes negative ($np < n_i^2$) then U_{SRH} is dominated by generation processes. In addition, U_{SRH} depends on the trap level position by the hyperbolic cosine and, therefore, it exists a maximum value of when the trap level is at mid-gap position $E_T = E_i$ exists. Furthermore, the minority carrier lifetime τ is given by [15]:

$$\tau = \frac{1}{c_n N_T} = \frac{1}{\sigma v_{th} N_T} \quad (1.24)$$

Here, τ_p yields the minority carrier (holes) lifetime in n-type semiconductors and τ_n the minority carrier (electrons) lifetime in p-type material. So that the equation for the net recombination rate also can be demonstrated as:

$$U_{SRH} = \frac{np - n_i^2}{[(n + n_1)\tau_p + (p + p_1)\tau_n]} \quad (1.25)$$

$$n_1 = N_C \exp \frac{E_T - E_C}{kT} \quad p_1 = N_V \exp \frac{E_V - E_T}{kT} \quad (1.26)$$

The corresponding depth of deep level states for certain impurities and crystal defects shows a correlation with the behavior of chemical bonding in semiconductor materials. Experimental investigations showed that for semiconductor materials with almost exclusively covalent bonds like in elemental silicon, point defects lead to non-bonding states in the energy gap at roughly the position of the molecular orbital energy, which could be located directly at mid-gap position, as shown in Fig. 1.4 [9]. In contrast, in compound semiconductors the molecular orbitals are separated in energy known as the chemical splitting and therefore initially closer to the band edges. Consequently, non-bonding defect states are closer to the band edges as the chemical splitting increases. For example, vacancy and antisite defects introduce shallower defect level states in III-V semiconductor alloys than in elemental group IV semiconductors. This circumstance, among other factors may be taken into account when discussing the decreased sensitivity of semiconductor materials with higher chemical splitting to the presence of crystal defects such as dislocations and grain boundaries [9].

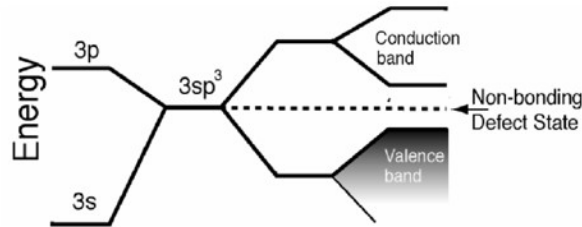


Figure 1.4: Non-bonding orbital resulting from a vacancy defect in silicon [9].

1.2.2 Extended Defects

Extended defects break the symmetry of the crystal lattice in semiconductor materials, similar to point defects as mentioned above. This leads to a local modification of the electron energy bands and localized levels or bands may be introduced in the forbidden bandgap. Whereas grain boundaries play an important role in the operation of polycrystalline semiconductor

devices like in polycrystalline solar cells, dislocations are one the most common extended defects in novel materials and device technologies based on hetero-epitaxy. For instance, it was shown in the past that an increasing amount of dislocation density in germanium (Ge) decreases the room-temperature minority carrier lifetime, as it is illustrated in Fig. 1.5 [19]. The electrical activity of dislocations by acting as traps or generation-recombination centers were also found in other semiconductor materials. A detailed explanation on the electronic properties of extended defects in semiconductors can be found by Holt and Yacobi [10].

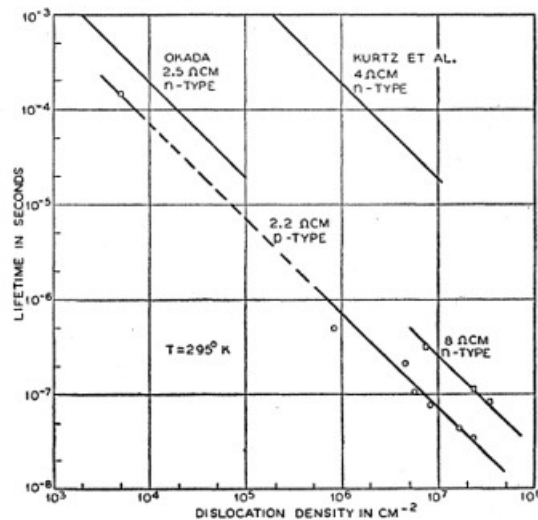


Figure 1.5: Dependence of room-temperature minority carrier lifetime and dislocation density in germanium [19].

In the past, the electrical activity of dislocations was studied on samples that are plastically deformed to introduce dislocations intentionally. This raised different presumptions of how dislocations may affect the electronic structure of group IV semiconductor materials. The three most accepted mechanisms include (1) shallow trap states that are pulled out of the conduction band by the elastic strain field around the dislocation, (2) the theory of dangling bonds in the dislocation core resulting in near mid-gap G-R levels and (3) the agglomeration of point defects near the dislocation that modifies the energy levels inside the bandgap. They are explained in more detail in the following:

(1) The strain fields around dislocations lead to deformation potentials of the electron energy bands of semiconductor materials due to altering the distance between lattice atoms [20]. Here, the separation of electronic states will be different and shallow states may be pulled down from the band edges into the forbidden energy band gap. Such shallow states may act as traps and allow carrier generation and recombination resulting in possible electrical noise [10].

(2) Previously, it was assumed that the core of dislocations in the diamond crystal structure featuring an edge component consists of dangling bonds ending up in space [21]. These dangling bonds can be considered as covalent sp^3 bonding orbitals, containing a single electron that is not bound to a second atom having energies between the bonding orbitals that correspond to valence band states and the anti-bonding states that correspond to conduction band. The wave functions of adjacent dangling bonds may overlap to form a one-dimensional band of states.

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Thus, such dangling bonds could give rise to a continuous band of states that is normally half-filled leading to strong electrical effects in semiconductor materials [21]. If each atom along the dislocation core features a broken dangling bond, the spacing between them c equals the Burgers vector b . Therefore, a general relation of the spacing between dangling bonds c can be expressed as a function of the Burgers vector b and α , the angle between l and b [21]:

$$c = 0.866b \frac{1}{\sin \alpha} \quad (1.27)$$

From eq. 1.27 it can be seen that a minimum spacing c and therefore a maximum number of dangling bonds are found in edge dislocations ($\alpha = 90^\circ$). The model of Read (see Fig. 1.6) suggests discrete acceptor levels due to dangling bonds, rather than a band of states in n-type Ge [22]. Here, the acceptor states trap electrons because they are below the Fermi level to bond with the single dangling electrons. Here, the energy of the bond electron is less than a single free electron in the conduction band but still higher than an electron in a complete bonding state (ϕ_2). In consequence, the material becomes less n-type, indicated by the energy potential ϕ_B around the dislocation in Fig. 1.6. The trapping of majority carriers creates an electrically charged dislocation line. The negative charge Q of the dislocation line is screened by a positive space charge cylinder in the surrounding of the dislocation with radius r_d . Including the occupation function f for the traps occupied by a second electron, the density of donor atoms in n-type material N_D and the elemental charge q , the line charge is given by [22]:

$$Q = \pi r_d^2 q N_D = q \frac{f}{c} \quad (1.28)$$

The occupation fraction of the acceptor states determines their energy position in the band gap and is only in the range of a few percent ($\leq 10\%$) at room temperature due to a repulsion between trapped and free carriers (potential barrier) [10]. Charged dislocations may attract minority carriers influencing their lifetime to a large extent. In plastically deformed materials with a diamond lattice structure like Si and Ge, far fewer dislocation dangling bond-like states are found than the expected number of dangling bonds in a dislocation core. This is probably caused by the energy-reducing rearrangement of dangling bonds per unit length [23]. It is more likely that dangling bonds only occur at disturbances along the dislocation line like jogs and kinks [10]. Jogs represents parts of the dislocation line that are outside the original slip plane and if these parts are normal to the main dislocation direction in addition, they are called kinks.

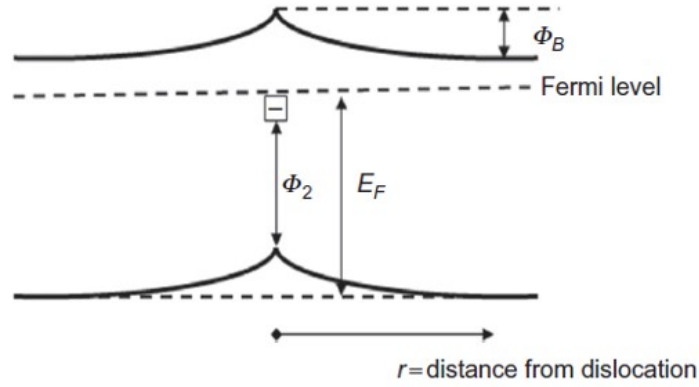


Figure 1.6: Electrical effects of dislocations based on Read model [24].

In addition to the model of Read, there exists the one-dimensional dangling bond band model of Schröter [25]. It deals with a half-filled narrow band of energy states along the dislocation line direction in the forbidden band gap rather than with sharp acceptor levels. It modifies the assumption of a space charge cylinder by including also free carriers that screen the charges of dangling bonds. The charge of the dislocation depends then on the position of the Fermi level E_F and the dislocation bands E_T . Here, the dangling bond levels, occupied by one electron can either accept electrons if $E_F > E_T$ (acceptor like) or are occupied by a second electron if $E_F < E_T$ (donor like). Additionally, E_F determines the occupation limit of this band [24]. Whereas the model of Read [22] is the fundamental assumption to treat a dislocation electrically, including the line charge along dislocation and the corresponding space charge cylinder, the model of Schröter [25] is more acceptable for theoretical treatments, estimating the type of charge in relation to the position of E_F by yielding a better agreement for a wide range of materials [10].

(3) In addition to dangling bonds, jogs and kinks that are intrinsic to dislocations attract impurity atoms and native point defects by elastic and electrostatic interactions at long range fields and by chemical bonding in the dislocation core, respectively. This leads to an irregular distribution and agglomeration of point defects near the dislocations. The segregation of mobile impurity atoms and point defects around dislocations is characterized by the Cottrell atmosphere [26]. Further, attracted impurities, point defects and/or doping atoms may strongly influence the defect states of the dislocations. It was studied experimentally that dislocations in Si show high electrical activity when decorated with heavy metal contaminations [10]. The agglomerated density of point defects leads to a localization of the extended core wave function and the assumed energy spectrum of states appears then as localized deep defect states [27]. Hence, the attracted point defects remain in position as residuals behind dislocations when they move on their glide planes [10]. However, the shallow states pulled down from the band edges due to the presence of strain fields around dislocations are not affected by the point defect decoration.

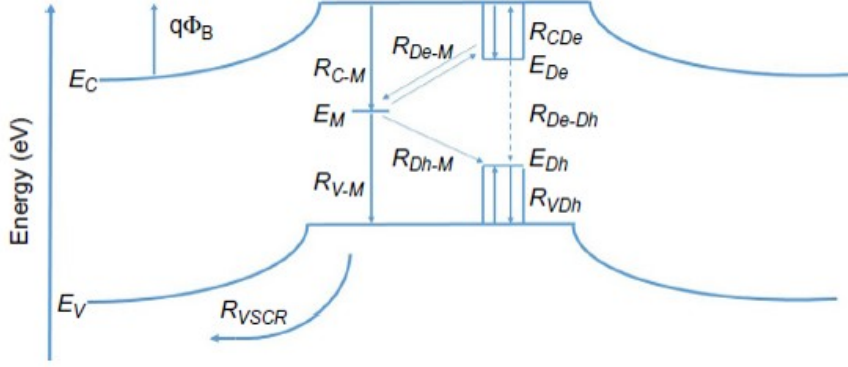


Figure 1.7: Recombination activity at dislocations [28].

In conclusion, dislocations introduce electronic states in the band gap due to dangling bonds, their strain fields or attracted point defects. These states will affect the electronic properties of semiconductor devices by contributing to non-radiative recombination processes and effecting the free carrier density as well as the mobility. It is shown that the electronic states of dislocations are strongly influenced by their interaction with point defects [27].

The strain-field induced shallow levels and the point defect related deep levels will exchange carriers by generation-recombination processes as schematically shown in Fig. 1.7 [28]. The carriers can either be captured or emitted by the shallow states split off from the valence band and conduction band, having energies of E_{Dh} and E_{De} , respectively. This intrinsic recombination is characterized by the recombination rates R_{VDh} and R_{CDe} . Based on the shallow states, the band gap appears smaller at the dislocations and the carrier exchange can take place via the recombination rate R_{De-Dh} , see Fig. 1.7. An additional path for recombination exists if point defects, which are collected in the strain field around the dislocation, introduce localized deep energy states E_M at mid-gap position. Here, the carrier exchange with the valence and conduction band is indicated by the recombination rates R_{V-M} and R_{C-M} , respectively. A lower activation energy is needed for the transition between the intrinsic shallow states and the extrinsic mid-gap levels, resulting in recombination rates R_{Dh-M} and R_{De-M} .

The interaction between impurities, native point defects and intrinsic dislocation energy states plays an important role in determining the electrical and optical effects of dislocations and grain boundaries. Therefore, diverse material compositions and growth techniques in Si heteroepitaxy deliver several combinations of this interaction ending up in divergent electrical activity of dislocations in hetero-integrated alloys on Si as can be seen from the wide range of reported data on the electrical activity of dislocations [10, 27]. Although some defect-related problems disappear due to improved growth procedures and fabrication processes even without being studied extensively or well understood, it is still important to study the electrical effects of dislocations while new materials and device technologies are developed. Especially in hetero-integration of group IV alloys on Si, the formation of extended defects due to crystal growth is an unavoidable issue caused by the large lattice mismatch between the active layers and the Si substrate, so that the study of the electrical activity of defects is important for novel device designs and theoretical simulations.

1.3 Basic devices for electrical characterization

Basic electronic devices such as Schottky diodes, p-n junction diodes and MOS capacitors are of great importance in electronic applications as well as in analyzing the electrical properties of semiconductor materials. The application of semiconductor devices ranges among others from unipolar devices, bipolar devices to photonic devices including heterojunction bipolar transistors (HBTs), junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), charge-coupled devices (CCD), light-emitting diodes (LEDs), semiconductor lasers, photodetectors, and solar cells. Most of them are based on the above-mentioned basic device structures and with their aid the electrical material quality can be determined. Important parameters for assessing the electrical properties of semiconductors are the type of carriers, their density and mobility, bulk defect density, generation lifetime, interface quality, contact and other parasitic resistances, etc.

This chapter describes the fundamental physics of some of the common basic devices that are used to determine the electrical activity of defects in semiconductor heterostructures in this work.

1.3.1 The p-n junction diode

The p-n junction diode is one of the most common representatives of bipolar devices in the semiconductor industry and is the basic structure of solar cells, light-emitting diodes, diode lasers and is present in all types of transistors. A p-n junction is built by bringing a p-doped and n-doped semiconductor into contact. Here, the electrical transport takes place through the movement of electrons and holes as majority carriers in n-type and p-type material, respectively. The diode character of a p-n junction is expressed by the rectifying behavior of the current-voltage (I-V) characteristics, where a significant conduction can only occur in the forward direction. An ideal I-V behavior is plotted in Fig. 1.8 [18]. As the p-n junction theory provides the fundamental physics of semiconductor devices, this section deals with the most important equations and their derivations. A detailed review of the physical nature of p-n junction diodes is given in the books by Sze [18] and Ibach & Lüth [29] from which the following equations are derived.

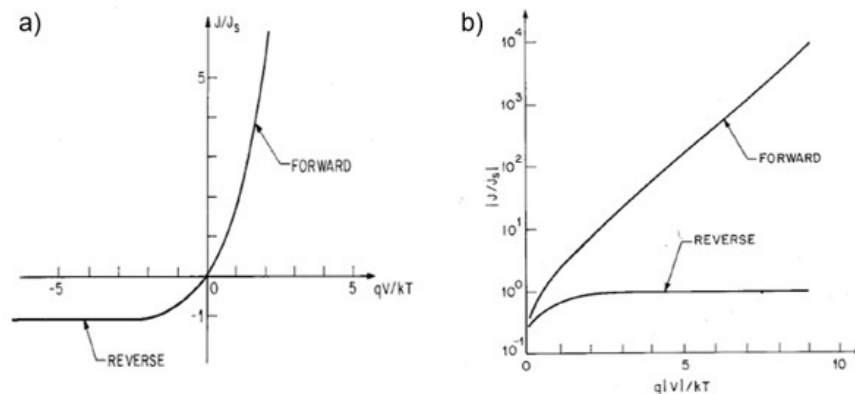


Figure 1.8: Ideal current-voltage characteristics on (a) linear and (b) semi-logarithmic scale [18].

1. Introduction

In the following, an abrupt p-n junction in thermal equilibrium is considered in which a sharp change in impurity concentration from acceptor (N_A) to donor (N_D) impurities takes place as is schematically shown in Fig. 1.9(a). If $N_A \gg N_D$, then one obtains a one-sided abrupt junction here a $p^+ - n$ junction for example. In thermal equilibrium, no external potential is applied to the junction and no current flow. Based on the current-density equation for semiconductor device operation, which consists of a drift component caused by the existing electric field E and a diffusion component related to the carrier concentration gradient ($\partial n/\partial x$ or $\partial p/\partial x$), including the Einstein relationship between the diffusion coefficient D and the mobility μ , ($D_n = \frac{kT}{q}\mu_n$), we can determine for the electron and hole current densities J_n and J_p , respectively:

$$J_n = q\mu_n \left(nE + \frac{kT}{q} + \frac{\partial n}{\partial x} \right) = \mu_n n \frac{\partial E_F}{\partial x} = 0 \quad (1.29)$$

$$J_p = q\mu_p \left(pE + \frac{kT}{q} + \frac{\partial p}{\partial x} \right) = \mu_p p \frac{\partial E_F}{\partial x} = 0 \quad (1.30)$$

Here, q is the elementary charge. A zero net electron J_n and hole current J_p requires a constant Fermi level throughout the junction:

$$\frac{\partial E_F}{\partial x} = 0 \quad (1.31)$$

Equation 1.31 is achieved in thermal equilibrium by building a diffusion potential, also called built-in potential V_{bi} (see Fig. 1.9b):

$$qV_{bi} = E_g - (qV_n + qV_p) = kT \ln \left(\frac{N_C N_V}{n_i^2} \right) - \left[kT \ln \left(\frac{N_C}{n_{n0}} \right) + kT \ln \left(\frac{N_V}{p_{p0}} \right) \right] \quad (1.32)$$

$$qV_{bi} = kT \ln \left(\frac{n_{n0} p_{p0}}{n_i^2} \right) \approx kT \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

including the energy band gap E_g , V_n and V_p as the potential in either the n- or p-region of the junction and N_C and N_V as effective density of states in conduction and valence band. At equilibrium, the electron and hole concentration in the n-side $n_{n0} n_{p0}$ and p-side $p_{n0} p_{p0}$ equals the intrinsic carrier concentration squared n_i^2 . Hence, V_{bi} can be expressed as:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{p_{p0}}{p_{n0}} \right) = \frac{kT}{q} \ln \left(\frac{n_{n0}}{n_{p0}} \right) \quad (1.33)$$

Eq. 1.33 depicts the relationship between the electron and hole densities on either side of the junction:

$$n_{p0} = n_{n0} \exp \left(-\frac{qV_{bi}}{kT} \right) \quad (1.34)$$

$$p_{n0} = p_{p0} \exp \left(-\frac{qV_{bi}}{kT} \right)$$

The electric field in the neutral regions of the semiconductor must be zero in thermal equilibrium. Therefore, the total negative charge per unit area in the p side ($N_A x_p$) must be equal to the total positive charge per unit area in the n side ($N_D x_n$). Considering the approximation of an

abrupt p-n junction, the solution of the Poisson equation reveals:

$$-\frac{\partial^2 V}{\partial x^2} \equiv \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon_s} = \frac{q}{\epsilon_s} [p(x) - n(x) + N_D^+(x) - N_A^-(x)] \quad (1.35)$$

$$-\frac{\partial^2 V}{\partial x^2} \approx \frac{q}{\epsilon_s} N_D \quad \text{for } 0 < x \leq x_n \quad \text{and} \quad -\frac{\partial^2 V}{\partial x^2} \approx -\frac{q}{\epsilon_s} N_A \quad \text{for } -x_p \leq x < 0$$

with $\rho(x)$ as charge density, dielectric constant of the semiconductor material ϵ_s , N_D^+ and N_A^- as ionized donor and acceptor densities respectively, and x_n and x_p as edges of the depletion layer. By integrating the Poisson's equation, we obtain the electric field $E(x)$:

$$E(x) = \frac{qN_D(x - x_n)}{\epsilon_s} \quad \text{and} \quad E(x) = \frac{qN_A(x + x_p)}{\epsilon_s} \quad (1.36)$$

As shown in Fig. 1.9(c), the maximum electric field present at the junction interface ($x = 0$) is given by:

$$|E_m| = \frac{qN_D x_n}{\epsilon_s} = \frac{qN_A x_p}{\epsilon_s} \quad (1.37)$$

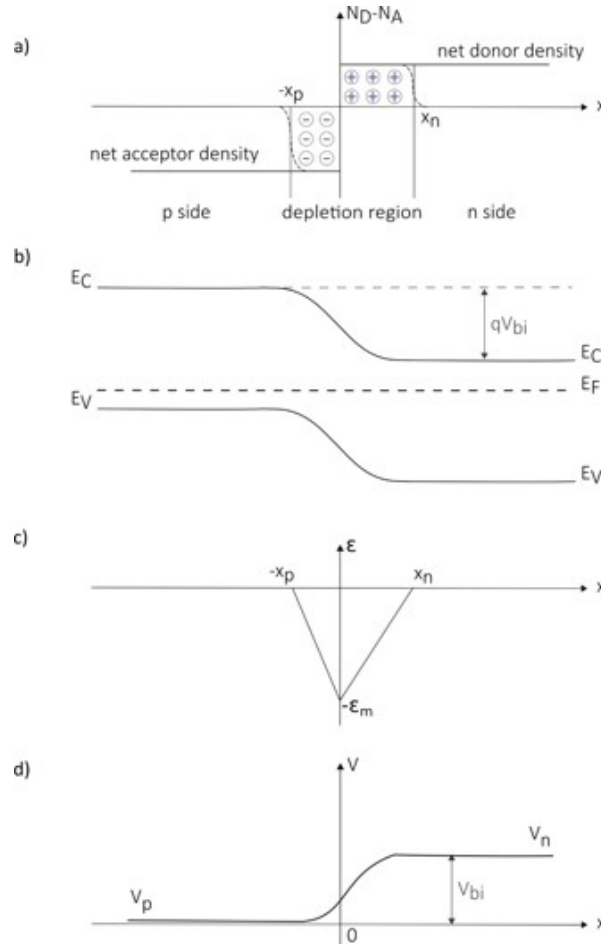


Figure 1.9: Schematic presentation of (a) the carrier distribution, (b) the band diagram, (c) the electric field and (d) the potential at an abrupt p-n junction after [18].

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Integrating Poisson's equation once again, the potential distribution $V(x)$ as well as the built-in potential V_{bi} can be revealed as shown in Fig. 1.9(d):

$$V(x) = E_m \left(x - \frac{x^2}{2w_d} \right) \quad (1.38)$$

$$V_{bi} = \frac{1}{2} E_m w_d = \frac{1}{2} E_m (x_n + x_p) \quad (1.39)$$

Combining eq. 1.37 and 1.39 yields the expression for the total depletion width w_d for a two-sided abrupt p-n junction:

$$w_d = \sqrt{\frac{2\epsilon_s}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi}} \quad (1.40)$$

For a one-sided abrupt junction, eq. 1.40 reduces to:

$$w_d = \sqrt{\frac{2\epsilon_s V_{bi}}{q N_{A/D}}} \quad (1.41)$$

As shown in Fig. 1.9(a), two majority-carrier distribution tails appear on each side of the junction caused by the difference in true carrier distribution and impurity concentration. Taking into account a correction factor of $2kT/q$ for both distribution tails, that is the dipole moment of the error contribution, a more accurate result for w_d can be obtained from eq. 1.35, where V_{bi} is replaced by $(V_{bi} - 2kT/q)$:

$$w_d = \sqrt{\frac{2\epsilon_s}{q N_{A/D}} \left(V_{bi} - \frac{2kT}{q} \right)} = L_D \sqrt{2(\beta V_{bi} - 2)} \quad (1.42)$$

Here, L_D is the Debye length in which a charge imbalance is neutralized by majority carriers under steady-state or equilibrium conditions:

$$L_d \equiv \sqrt{\frac{\epsilon_s kT}{q^2 N_{A/D}}} \quad (1.43)$$

In the following paragraph the current-voltage behavior of p-n junctions is discussed according to ref. [18]. The fundamental theory of the I-V characteristics of semiconductor diodes was established for the first time by William B. Shockley in 1949 [30]. The ideal I-V characteristics are based on the following basic assumptions: (1) validation of the abrupt depletion-layer approximation, where a dipole layer is confined by abrupt boundaries and the outer regions of the semiconductor appear electrical neutral; (2) the Boltzmann relations are valid throughout the depletion layer, see eq. 1.44 for n-type and eq. 1.45 for p-type semiconductor material; (3) the condition of low injection is fulfilled, which means that injected minority carriers are insignificant compared to majority carrier densities and (4) there exists no generation current in the depletion region as well as J_n and J_p being constant.

$$E_F - E_i = kT \ln \left(\frac{n_{n0}}{n_i} \right) \quad (1.44)$$

$$E_i - E_F = kT \ln \left(\frac{p p_0}{n_i} \right) \quad (1.45)$$

Starting from the Boltzmann relation, the pn product at thermal equilibrium equals n_i^2 and can be written as:

$$n = n_i \exp \left(\frac{E_F - E_i}{kT} \right) \equiv n_i \exp \left[\frac{q\psi - \phi}{kT} \right] \quad (1.46)$$

$$p = p_i \exp \left(\frac{E_i - E_F}{kT} \right) \equiv n_i \exp \left[\frac{q\phi - \psi}{kT} \right] \quad (1.47)$$

Here, E_i is the intrinsic and E_F the Fermi level and ψ and ϕ the corresponding potentials ($\psi \equiv -E_i/q$; $\phi \equiv -E_F/q$) respectively. By applying an external voltage, the minority-carrier densities in both regions change and the Fermi level of the valence and conduction band start to differ from one another, so that $np = n_i^2$ is no longer valid. Instead, quasi-Fermi levels ϕ_n and ϕ_p for electrons and holes respectively, should be taken into account:

$$n = n_i \exp \left[\frac{q(\psi - \phi_n)}{kT} \right] \quad (1.48)$$

$$p = n_i \exp \left[\frac{q(\phi_p - \psi)}{kT} \right] \quad (1.49)$$

By rearranging eq. 1.48 and 1.49, we obtain the quasi-Fermi levels for electrons and holes and the pn product becomes:

$$\phi_n = \psi - \frac{kT}{q} \ln \left(\frac{n}{n_i} \right) \quad \phi_p = \psi + \frac{kT}{q} \ln \left(\frac{p}{n_i} \right) \quad (1.50)$$

$$pn = n_i^2 \exp \left[\frac{q(\phi_p - \phi_n)}{kT} \right] \quad (1.51)$$

Following eq. 1.51, the pn product becomes bigger than n_i^2 , if $\phi_p - \phi_n > 0$ (forward bias) leading to a recombination of the excess carriers that results in a conduction of current. For reverse biases, $\phi_p - \phi_n < 0$ and $pn < n_i^2$ forcing a generation of carriers to return to equilibrium conditions. Reflecting equation 1.1 and 1.2 of this chapter, eq. 1.23 and the fact that the electric field equals the difference in the intrinsic potentials ($E \equiv -\nabla\psi$), the electron and hole current densities become:

$$J_n = q\mu_n \left(nE + \frac{kT}{q} \nabla n \right) = q\mu_n n (-\nabla\psi) + q\mu_n \frac{kT}{q} \left[\frac{qn}{kT} (\nabla\psi - \nabla\phi_n) \right] = -q\mu_n n \nabla\phi_n \quad (1.52)$$

$$J_p = q\mu_p \left(pE + \frac{kT}{q} \nabla p \right) = q\mu_p p (-\nabla\psi) + q\mu_p \frac{kT}{q} \left[\frac{qp}{kT} (\nabla\phi_p - \nabla\psi) \right] = -q\mu_p p \nabla\phi_p \quad (1.53)$$

Thus, J_n and J_p are proportional to the gradients of the quasi-Fermi levels. The electrostatic potential difference across a p-n junction is given by:

$$V = \phi_p - \phi_n \quad (1.54)$$

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Combining eq. 1.51 and 1.54 provides the most important boundary conditions for the ideal current-voltage equation including the actual electron and hole densities at the depletion layer edges on the p side ($x = -x_p$) and n side ($x = x_n$) respectively:

$$n_p = \frac{n_i^2}{p_p} \exp\left(\frac{qV}{kT}\right) = n_{p0} \exp\left(\frac{qV}{kT}\right) \quad (1.55)$$

$$p_n = \frac{n_i^2}{n_p} \exp\left(\frac{qV}{kT}\right) = p_{n0} \exp\left(\frac{qV}{kT}\right) \quad (1.56)$$

The continuity equations predict for the steady state condition:

$$-U + \mu_n E \frac{\partial n_n}{\partial x} + \mu_n n_n \frac{\partial \epsilon}{\partial x} + D_n \frac{\partial^2 n_n}{\partial x^2} = 0 \quad (1.57)$$

$$-U + \mu_p E \frac{\partial p_n}{\partial x} + \mu_p p_n \frac{\partial \epsilon}{\partial x} + D_p \frac{\partial^2 p_n}{\partial x^2} = 0 \quad (1.58)$$

with U as net recombination rate. Considering the charge neutrality ($n_n - n_{n0}$) \approx ($p_n - p_{n0}$), eq.1.58 can be transformed into:

$$-\frac{p_n - p_{n0}}{\tau_a} + D_a \frac{\partial^2 p_n}{\partial x^2} - \frac{n_n - p_n}{\mu_p + \frac{p_n}{\mu_n}} \frac{E \partial p_n}{\partial x} = 0 \quad (1.59)$$

where D_a is the ambipolar diffusion coefficient and τ_a the ambipolar lifetime:

$$D_a = \frac{n_n + p_n}{n_n/D_p + p_n/D_n} \quad \tau_a = \frac{p_n - p_{n0}}{U} = \frac{n_n - n_{n0}}{U} \quad (1.60)$$

Considering the low-injection assumption ($p_n \ll n_n \approx n_{n0}$) in an n-type semiconductor, eq. 1.59 reduces to:

$$-\frac{p_n - p_{n0}}{\tau_p} - \mu_p E \frac{\partial p_n}{\partial x} + D_p \frac{\partial^2 p_n}{\partial x^2} = 0 \quad (1.61)$$

Eq. 1.61 reduces further when no electric field exists in the neutral region of a p-n junction to:

$$\frac{\partial^2 p_n}{\partial x^2} - \frac{p_n - p_{n0}}{D_p \tau_p} = 0 \quad (1.62)$$

The solution of eq. 1.62 under consideration of the boundary conditions already derived above (eq. 1.56) and $p_n(x = \infty) = p_{n0}$ gives:

$$p_n - p_{n0} = p_{n0} e^{\frac{qV}{kT} - 1} e^{-\frac{(x-x_n)}{\sqrt{D_p \tau_p}}} \quad (1.63)$$

Leading to the current density formula at the depletion layer boundary ($x = x_n$):

$$J_p = -qD_p \frac{\partial p_n}{\partial x} \Big|_{x_n} = \frac{qD_p p_{n0}}{L_p} \left(e^{qV/kT} - 1 \right) \quad (1.64)$$

$$J_n = -qD_n \frac{\partial n_p}{\partial x} \Big|_{-x_p} = \frac{qD_n n_{p0}}{L_n} \left(e^{qV/kT} - 1 \right) \quad (1.65)$$

The total current density is given by the sum of J_n and J_p , which is the Shockley equation [30] known as the ideal diode law:

$$J = J_p + J_n = J_s \left(e^{\frac{qV}{kT}} - 1 \right) \quad \text{with} \quad J_s = \frac{qD_p p_{n0}}{\sqrt{D_p \tau_p}} + \frac{qD_n n_{p0}}{\sqrt{D_n \tau_n}} \quad (1.66)$$

Here, J_s is the saturation current density due to minority carriers at which the current saturates in the reverse biased direction. For a one-sided abrupt junction (e.g., $p_{n0} \leq n_{p0}$), one term can be neglected. The exponential term of eq. 1.66 includes the electrostatic energy caused by the external applied voltage. It is assumed that the applied voltage drops only across the space-charge region and not across the quasi-neutral regions on the p or n sides. The saturation current shows a temperature dependent behavior. The quantities D , p/n and τ are all temperature-dependent and if the ratio D/τ is proportional to T^γ , where γ is a constant, then:

$$J_s \simeq \frac{qD_p p_{n0}}{\sqrt{D_p \tau_p}} \simeq q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i}{N_D} \sim \left[T^3 \exp -\frac{E_g}{kT} \right] T^{\frac{\gamma}{2}} = T^{(3+\frac{\gamma}{2})} \exp -\frac{E_g}{kT} \quad (1.67)$$

The temperature dependence of the first term ($T^{(3+\gamma/2)}$) is neglectable compared with the exponential term ($-E_g/kT$), so that the slope of a J_s vs $1/T$ plot is determined by the energy band gap E_g . In reverse direction, where J is approximately J_s , the current will increase with temperature as $\exp(-E_g/kT)$, whereas in forward direction J is proportional to $J_s e^{qV/kT}$, the current will increase approximately as $\exp[-(E_g - qV)/kT]$.

There are potential factors that may lead to departures from the ideal diode equation (eq. 1.66):

- Surface effects are not considered, but for planar junctions the surface leakage currents are generally much smaller than the generation currents in the depletion region. Therefore, it will not be taken into account further here.
- Reaching the high-injection condition even at low forward biases may lead to junction breakdown.
- Besides the generation and recombination of carriers, further tunnel processes between states in the forbidden bandgap is not considered.
- If the current increases rapidly, the voltage drop due to potential series resistance R_S increases too and therefore should be added to the voltage drop across the junction. Including R_S the diode equation becomes:

$$I = I_s \left(e^{q(V-IR_S)/kT} - 1 \right) \quad (1.68)$$

- Generation and recombination processes (see 1.1) in the depletion layer will influence the ideal static and dynamic characteristics of a p-n junction.

Defect-related generation-recombination centers result in an additional current component. Under reverse-bias conditions, the reduction in carrier concentration ($pn < n_i^2$) leads to the emission of carriers and an additional generation current J_{gen} . Whereas at forward bias

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($pn > n_i^2$) the capture of carrier is the dominant recombination-generation process in the depletion region, producing a recombination current J_{rec} component in addition to the diffusion current [18]. Based on the net generation rate U_{SRH} (eq. 1.12) the current related generation in the depletion region is then given by:

$$J_{gen} = \int_0^{w_d} q|U_{SRH}| dx \simeq q|U_{SRH}|W = \frac{qn_i w_d}{\tau_g} \quad (1.69)$$

with τ_g the generation lifetime, the average duration of time to generate an electron-hole pair. The sum of the diffusion component in the neutral region of a p-n junction and the generation current (eq. 1.69) inside the depletion region can be written as the total reverse current density J_R (for $p_{n0} \gg n_{p0}$ and $|V| > 3kT/q$):

$$J_R = q\sqrt{\frac{D_p}{\tau_p} \frac{n_i^2}{N_D}} + \frac{qn_i W}{\tau_e} \quad (1.70)$$

As J_R depends on the intrinsic carrier concentration to an unequal extent, the diffusion component will dominate at room temperature in semiconductors with large values of n_i , such as germanium, following the ideal Shockley equation, while the generation current component may dominate in materials with smaller n_i like silicon. However, at sufficient high temperature the diffusion current will be the dominant reverse current component as n_i increases with temperature.

Assuming a mid-gap trap level ($E_i = E_T$) featuring the maximum value of the net recombination rate U_{SRH} , the current component related to the recombination of carriers J_{rec} in the depletion region at forward bias is thus [18]:

$$J_{rec} = \int_0^{w_d} qU dx \equiv \frac{qw_d}{2} \sigma v_{th} N_T n_i \exp \frac{qV}{2kT} \quad (1.71)$$

Similar to J_{gen} in reverse bias, J_{rec} at forward bias is proportional to n_i , too. Furthermore, the total forward current J_F can be expressed by the sum of the diffusion current component and the recombination current component, for $p_{n0} \gg n_{p0}$ and $V > kT/q$:

$$J_F = q\sqrt{\frac{D_p}{\tau_p} \frac{n_i^2}{N_D}} \exp \frac{qV}{kT} + \frac{qw_d}{2} \sigma v_{th} N_T n_i \exp \frac{qV}{kT} \quad (1.72)$$

Eq. 1.72 can in general be correlated to experimental results as:

$$J_F \approx \exp \frac{qV}{nkT} \quad (1.73)$$

Here, n represents the quality factor that equals 1 for an ideal diode where the diffusion current dominates and approaches the value of 2 when the recombination current component starts to dominate [18].

1.3.2 Metal-insulator-semiconductor (MIS) capacitor

In Metal-insulator-semiconductor (MIS) capacitors, the insulator acts as dielectric between a metal contact and a semiconductor material, similar to a parallel plate capacitor. In case

of using an oxide as insulator, the system is commonly known as metal-oxide-semiconductor (MOS) capacitors. For the sake of simplicity, the term MOS capacitors will be consistently used in this section. MOS capacitors are the most common and useful device for studying semiconductor surfaces [18]. Although MOS capacitors are not a frequently used device itself, they are the fundamental structure in MOS-based transistors (e.g. MOS-field-effect-transistors), which are one of the most widely applied semiconductor devices. A typical MOS capacitor is sketched in Fig. 1.10 and consists of a semiconductor substrate representing a variable capacitance C_{sc} , an oxide such as SiO_2 of thickness d_{ox} having a fixed capacitance C_{ox} and a metal contact referred as gate [18, 31]. Hence, the MOS-structure can be assumed as a serial connection of C_{sc} and C_{ox} . The applied gate voltage V_g is positive when the metal contact is positively biased with respect to the ohmic contact on the backside of the semiconductor substrate and negative when the metal contact is negatively biased.

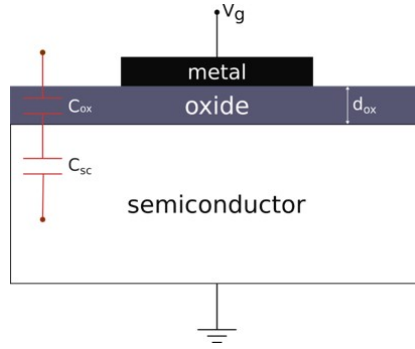


Figure 1.10: MOS capacitor after after [31].

The electronic properties of the MOS system will be described by means of the energy band diagram. Here, the course of the valence band E_V , conduction band E_C , Fermi level E_F and intrinsic level E_i is presented in dependence of the space coordinate x . When there is no applied bias, a MOS capacitor is defined by a zero work-function difference Φ_{ms} between the metal work function Φ_m and the semiconductor work function Φ_s [18]:

$$\phi_{ms} \equiv \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} - \phi_B \right) = 0 \quad \text{for } n\text{-type} \quad (1.74)$$

$$\phi_{ms} \equiv \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} + \phi_B \right) = 0 \quad \text{for } p\text{-type} \quad (1.75)$$

where χ is the semiconductor electron affinity, E_g the band gap and ϕ_B the potential difference between E_F and E_i in the bulk. This case is shown in Fig. 1.11 and is called a flat-band condition, where the energy bands E_C and E_V are flat. In equilibrium condition, no external forces effect the free carrier concentration $p(x)$ and $n(x)$ and they equal the equilibrium carrier concentration p_0 and n_0 respectively. A real flat-band condition can only be fulfilled in uniformly doped semiconductors as they exhibit a location-independent difference of $E_F - E_i$. In non-uniform doped semiconductors, the flat-band condition equals the point in which the electric field at the surface vanishes $E_s = 0$ and we have a zero-crossing point of the integral of semiconductor space charges. The applied voltage is called flat-band voltage V_{fb} [18, 31, 32].

1. Introduction

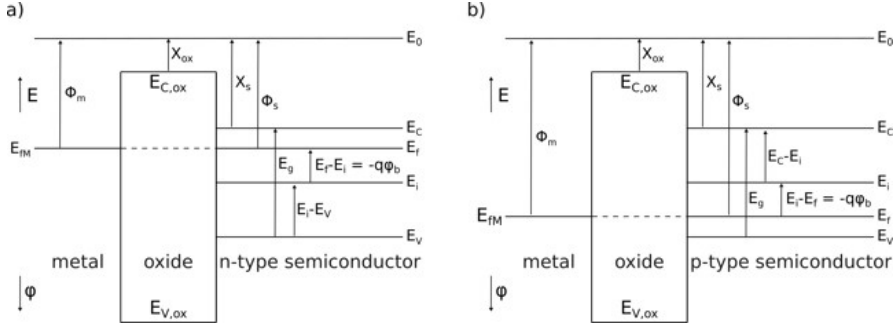


Figure 1.11: Band Diagram of an (a) n-MOS and (b) p-MOS capacitor after [18, 32].

When biasing an ideal MOS diode with positive or negative voltages, there may exist three different modes of operation. For better clarity, all three cases of operation are discussed for p-type semiconductors but can be equally applied to n-type semiconductors as well.

When a negative voltage is applied to the gate ($V_g < 0$), the bands E_V , E_C and E_i bend upwards, whereas E_F remains constant as no current flows in the structure for an ideal MOS diode. As shown in Fig. 1.6(a) the valence band becomes closer to the Fermi level near the semiconductor-oxide interface than in the bulk, which causes an *accumulation* of majority carriers (holes) at the surface (see Fig. 1.12b). Based on the condition that electron and hole densities are much smaller than the corresponding densities of states N_C and N_V the free carrier density $p(x)$ can be described by the energy difference $E_F - E_V$:

$$p(x) = N_V \exp \left(-\frac{E_F - E_V}{kT} \right) \quad (1.76)$$

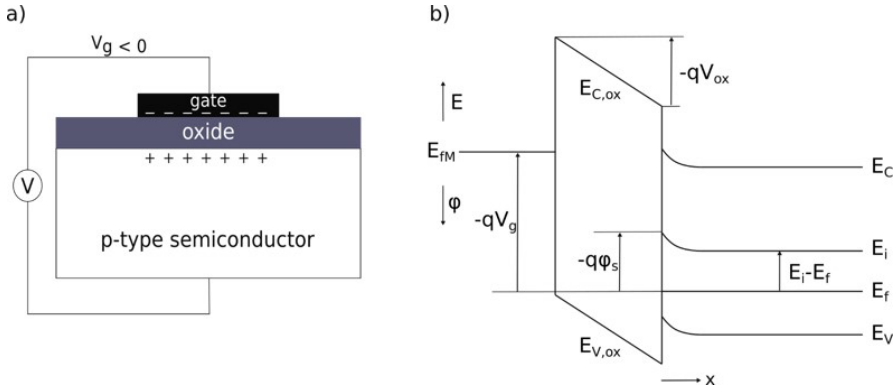


Figure 1.12: Accumulation case of a MOS capacitor represented in (a) band diagram and (b) device sketch after [31, 32].

When a small positive voltage is applied to the gate ($V_g > 0$), the case of depletion is reached. Here, the energy bands bend downwards and increase the energy difference $E_F - E_V$ as shown in Fig. 1.13(b). Therefore, the majority carriers are depleted and a space charge region (scr) forms (see Fig. 1.13a). With the potential $\phi(x) = (E_F - E_i)/q$, ϕ_b , the band bending $\psi(x) = \phi(x) - \phi_b$ and the temperature voltage $u_T = kT/q$, the location-dependent carrier density can be written as:

$$p(x) = n_i \exp \left(-\frac{\phi(x)}{u_T} \right) \quad (1.77)$$

$$p(x) = p_0 \exp \frac{-\psi(x)}{u_T} \quad \text{with} \quad p_0 = n_i \exp \frac{-\phi_b}{u_T} \quad (1.78)$$

whereas in the bulk $n = n_0$, $p = p_0$ and $\phi(x) = \phi_b$. At the semiconductor-oxide interface ϕ becomes the surface potential ϕ_S and ψ the surface band bending ψ_S .

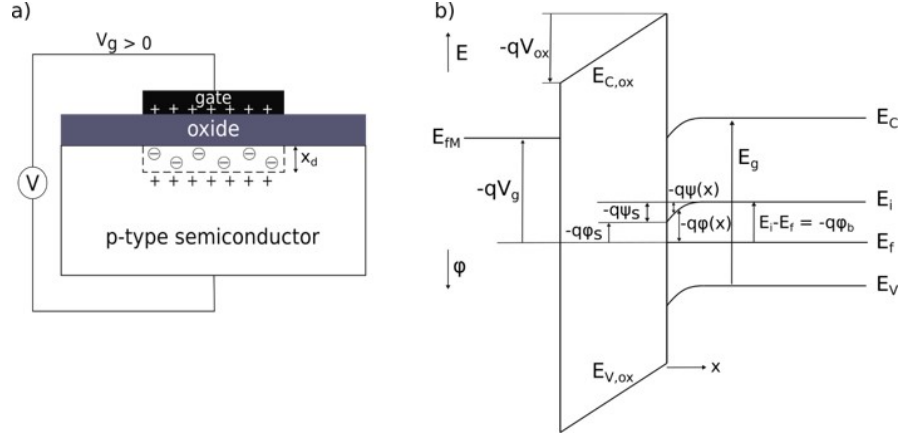


Figure 1.13: Depletion case of a MOS capacitor represented in (a) band diagram and (b) device sketch after [31, 32].

By further increasing the gate voltage, the bands bend even more downward and at some V_g , E_i will cross over E_f at the semiconductor-oxide interface and the surface is no longer in depletion but at the threshold of inversion (V_{th}) (Fig. 1.14). Inversion means that the type of conduction is inverted in the region below the surface, here from p-type to n-type. At this point the number of minority carriers (electrons) at the surface is now larger than that of majority carriers (holes).

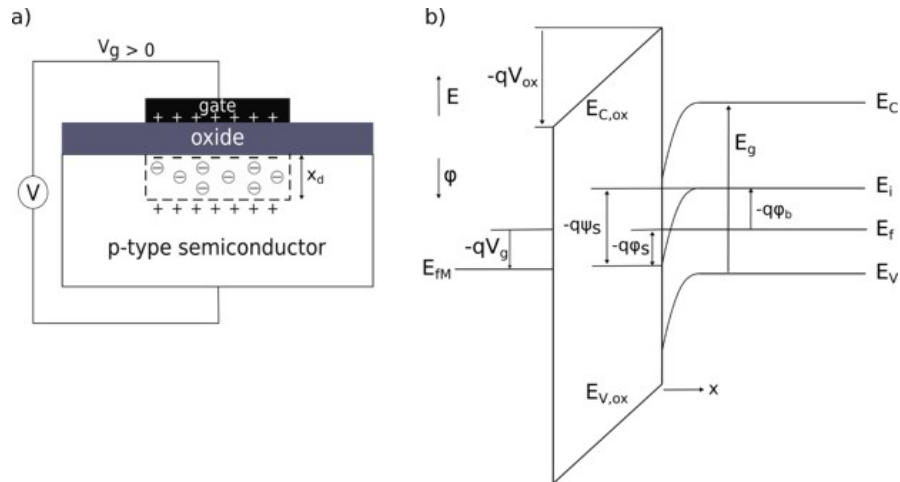


Figure 1.14: Inversion case of a MOS capacitor represented in (a) band diagram and (b) device sketch after [31, 32].

Based on the band diagrams in Fig. 1.12-1.14 the gate voltage drop on the whole MOS system can be described by [32]:

$$-qV_g + \phi_M = -qV_{ox} + \chi_s + (E_C - E_i) - q\psi_s + (E_i - E_f) \quad (1.79)$$

1. Introduction

$$V_g = V_{ox} + \psi_s + \frac{\phi_{MS}}{q} \quad (1.80)$$

The voltage drop on the oxide V_{ox} can be determined by solving the Poisson's equation, which describes the relation between the space charge and the potential (see eq. 1.35) resulting in the integral of the space charge between the semiconductor-oxide interface and d_{ox} :

$$Q_{ox} = - \int_0^{-d_{ox}} \rho(x) dx \quad (1.81)$$

$$\text{with focus of charge } \bar{x}_{ox} : \quad \bar{x}_{ox} = \frac{\int_0^{-d_{ox}} x \rho(x) dx}{\int_0^{-d_{ox}} \rho(x) dx} \quad (1.82)$$

The potential difference and thus the voltage drop on the oxide side with E_{ox} as electric field at the semiconductor-oxide interface is equal to:

$$V_{ox} = \phi|_{x=-d_{ox}} - \phi|_{x=0} \quad (1.83)$$

$$V_{ox} = - \frac{d_{ox} Q_{ox}}{\epsilon_{ox}} \left(1 + \frac{\bar{x}_{ox}}{d_{ox}} \right) + E_{ox} d_{ox} \quad (1.84)$$

Based on the continuity of the electric displacement field ($D \equiv \epsilon_0 E$) at the semiconductor-oxide interface and following Gauss's law, the electric displacement field at the surface becomes:

$$\epsilon_{ox} E_{ox} = -Q_{sc} \quad (1.85)$$

Considering the area-based oxide capacitance $C_{ox} = \epsilon_{ox}/d_{ox}$ the voltage drop at the oxide can be written as:

$$V_{ox} = - \frac{1}{C_{ox}} \left(Q_{ox} \left(1 + \frac{\bar{x}_{ox}}{d_{ox}} \right) + Q_{sc} \right) \quad (1.86)$$

$$\text{with } Q_{sc} = - \int_0^{\infty} \rho(x) dx \quad (1.87)$$

Here, Q_{sc} is the semiconductor charge and Q_{ox} is the oxide charge equal to eq. 1.81. As it becomes obvious in eq. 1.86, the voltage drop on the oxide depends on the oxide charges itself as well as on the charges in the semiconductor material. Hence, the total gate voltage drop in the MOS system reduces to [32]:

$$V_g = \psi_s + \frac{\phi_{MS}}{q} - \frac{1}{C_{ox}} \left(Q_{ox} \left(1 + \frac{\bar{x}_{ox}}{d_{ox}} \right) + Q_{sc} \right) \quad (1.88)$$

Further on, the separate components of both Q_{ox} and Q_{sc} will be introduced. The oxide charges are not necessarily relevant for the operation of MOS based devices, but they influence the C-V characteristic and therefore should be taken into account. A detailed review of the defects in gate dielectrics can be found elsewhere [33]. The following equations are taken from ref. [32]. Q_{ox} consists of the following components:

$$Q_{ox} = Q_f + Q_{ot} + Q_m + Q_{it} \quad (1.89)$$

Fixed oxide charges Q_f are localized near the oxide-semiconductor interface and attributed to structural defects near the interface such as dangling bonds. The density of Q_f (N_f) depends on the crystal orientation of the semiconductor and the oxidation process. As expressed in eq. 1.70, Q_f show no dependence on the surface potential nor the electric field in the oxide and can therefore be considered as immobile positive charges close to the oxide-semiconductor interface. Q_f lead to a shift of measured C-V curves on the voltage axis to negative values.

$$Q_f = - \int_{-d_{ox}}^0 N_f(x) dx \quad (1.90)$$

Oxide trapped charges Q_{ot} caused by defects in the bulk oxide that lead to traps in the forbidden band interacting with both bands E_V and E_C , because they have a donator and an acceptor portion $D_{ot,d}$ and $D_{ot,a}$ respectively. Free carriers can be trapped in those states due to an electric field or diffusion. The probability of occupation is expressed by f_0 . Since Q_{ot} have long capture and emission time constants, they are called slow traps. During C-V measurements, Q_{ot} lead to a hysteresis on the voltage axis when different voltage ramp rates are used. They can be avoided by choosing pulsed C-V measurement techniques and measuring at low temperatures.

$$Q_{ot} = q \int_{-d_{ox}}^0 \int_{E_{V,ox}}^{E_{C,ox}} (D_{ot,d}(x)(1 - f_0) - D_{ot,a}(x)f_0) dE dx \quad (1.91)$$

Mobile ionic charges Q_m evoked by alkali ion impurities in the oxide like Na^+ , K^+ and Li^+ or OH^- and O_2^- ions. The movement of these ions can take place at high temperatures and sufficiently high electric fields resulting in a long-term drift of the threshold voltage. Nowadays, Q_m is usually no longer an issue because of good quality oxides.

$$Q_m = q \int_{-d_{ox}}^0 N_m(x) dx \quad (1.92)$$

Interface trapped charges Q_{it} caused by defects created due to the break in the lattice periodicity at the semiconductor-oxide interface. Q_{it} possess a portion of acceptors and donators and is determined by the integration of these portion densities $N_{it,a}$ and $N_{it,d}$ respectively, by considering the rate of occupation f_0 along the oxide bandgap. Such rechargeable interface traps may exchange carriers with the band edges of the semiconductor and accordingly build up a spectrum of states in the bandgap of the semiconductor.

$$Q_{it} = q \int_{-d_{ox}}^0 \int_{E_{V,ox}}^{E_{C,ox}} (D_{it,d}(x)(1 - f_0) - D_{it,a}(x)f_0) dE dx \quad (1.93)$$

Apart from Q_f and Q_{it} being localized in the insulator, they are attributed to interface states caused by their focus of charge close to the oxide-semiconductor interface. Therefore, Q_f and Q_{it} have a major impact on the semiconductor C-V characteristic. The main charges localized in the semiconductor Q_{sc} that act as countercharge to the gate side are:

$$Q_{sc} = Q_d + Q_{inv} + Q_{bt} \quad (1.94)$$

1. Introduction

The *depletion charge* Q_d includes the majority carrier charge Q_{maj} and the location independent impurity charge Q_N caused by the dopants, e.g. negatively charged acceptors or positively charged donors. In accumulation Q_N is negligible compared to the majority carrier charge, whereas in the space charge region Q_{maj} can be ignored. By reason of the location-independent behavior of Q_N , a change in Q_d is caused solely by the change in Q_{maj} at the edge of the space charge region ($dQ_d = dQ_{maj}$). The depth extension of Q_d into the semiconductor bulk is called depletion depth x_d .

$$Q_d = Q_{maj} + Q_N \quad (1.95)$$

$$Q_{maj} = q \int_0^\infty p(x) dx \quad (1.96)$$

$$Q_N = -q \int_0^\infty N_A/N_D dx \quad (1.97)$$

At a certain extension of x_d electron-hole pairs are generated by thermal generation. Here, the majority carriers flow off through the back contact to the top gate and enhance the gate voltage, whereas the generated minority carriers are attracted by the semiconductor-oxide interface due to the electric field. At a certain concentration of minority carriers at the surface, an inversion of the type of conduction take place forming the *minority carrier charge* Q_{inv} (electrons $n(x)$ in case of a p-type semiconductor).

$$Q_{inv} = -q \int_0^\infty n(x) dx \quad (1.98)$$

Bulk trapped charges Q_{bt} are caused by defects in the semiconductor (acceptor and/or donor states), which are generation/recombination centers of electron-hole pairs. These Q_{bt} are composed of densities of donator and acceptor states in the semiconductor $D_{bt,d}$ and $D_{bt,a}$ respectively, and the corresponding probability of occupation f_0 :

$$Q_{bt} = q \int_0^\infty \int_{E_V}^{E_C} (D_{bt,d}(x)(1 - f_0) - D_{bt,a}(x)f_0) dE dx \quad (1.99)$$

1.4 Electrical characterization techniques

Besides structural investigations of defects downgrading the quality of new semiconductor materials, the extensive characterization of their electrical properties is of equal importance, e.g. for semiconducting device design, improvement and simulation. To detect impurities either charged or neutral that introduce defect levels inside the semiconductor band gap interacting with free carriers, any technique that considers charged species is suitable. Among numerous material and device characterization techniques that can be utilized to identify the electrical impact of unintentionally induced defects (see reference [3]), the techniques applied in this work are described in this chapter. In addition to the theoretical principle of each technique, the tools used are introduced here.

1.4.1 Current-voltage measurements

Current-voltage (I-V) measurements are used on the one hand for evaluation of device characteristics like breakdown voltages in semiconductor diodes and transistors to avoid any damage of the devices. On the other hand, I-V measurements can be used to gain information on the transport of carriers in semiconductor materials. As introduced in section I.2 and I.3, the interaction of free carriers with defects acting as recombination centers or traps will impact the current flow to a certain extent and I-V measurements are, therefore, useful to probe the electrical activity of defects in semiconductor devices.

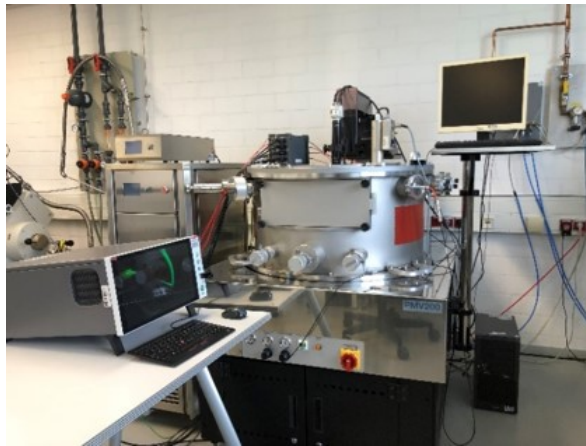


Figure 1.15: Setup for I-V-T measurements at IHP.

In I-V measurements, a voltage is sourced to a device under test (DUT) and the corresponding current flowing through the device is measured. The I-V analysis reported in this thesis was performed in a low-vacuum PMV200 probe station by FormFactor connected with a Keithley 4200A-SCS parameter analyzer that is shown in Fig. 10. Here, source measure unit (SMUs) instruments include a dc (direct current) power source that applies either a constant voltage ($\pm 210\text{V}$) or a constant current ($\pm 100\text{mA}$) to the DUT and measures voltage and/or current simultaneously by an integrated multimeter. The attached temperature system by ATT Systems for heating and cooling allowed temperature-dependent I-V measurements (I-V-T) in the range of -60°C to 200°C .

1.4.2 Capacitance-voltage measurements

Capacitance-voltage (C-V) measurements have a long tradition in determining electrical properties of semiconductor materials and devices like doping concentrations, threshold voltages and oxide thicknesses [3]. Semiconductor devices that are able to build up a depletion region featuring no free charges, e.g. Schottky diodes, p-n junction diodes or MOS capacitors are suitable for C-V characterization because they are able to behave like a capacitor. The capacitance of such devices contains information about ionized donors, acceptors, and electrically active defects inside the depletion region.

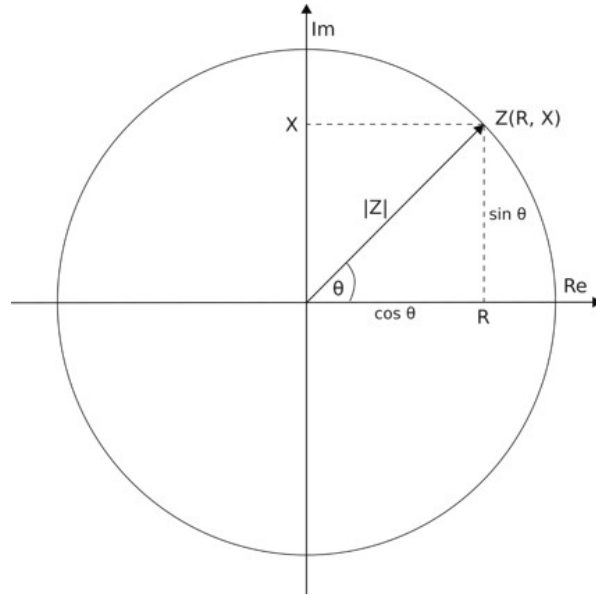


Figure 1.16: Graphical representation of the complex impedance Z on a unit circle containing a resistance part R on the real axis (Re) and a reactance part X on the imaginary axis (Im).

Capacitances itself are typically measured by capacitance-meters (C -meter) or LCR -meter (inductance L , capacitance C and resistance R) that in principle are based on impedance measurements. The impedance of a semiconductor device is generally defined as the impairment for the flow of an alternating current (ac) through it when a voltage is applied at a given frequency [34]. As shown in Fig. 1.16, the complex impedance Z consists of a resistance R and a reactance X that correspond to the real and imaginary part respectively. Here, the impedance can be expressed as rectangular coordinates by the sum of the real and imaginary part by:

$$\bar{Z} = Re(\bar{Z}) + Im(\bar{Z}) = R + jX \quad (1.100)$$

According to Fig. 1.16, the magnitude $|\bar{Z}|$ and direction θ of the vectored impedance can also be expressed in the polar form:

$$\bar{Z} e^{i\theta} = \bar{Z} \cos \theta + \bar{Z} j \sin \theta \quad (1.101)$$

Both types of coordinates can be transferred into each other through:

$$R = |\bar{Z}| \cos \theta \quad X = |\bar{Z}| \sin \theta \quad (1.102)$$

$$|\bar{Z}| = \sqrt{R^2 + X^2} \quad \theta = \tan^{-1} \frac{X}{R} \quad (1.103)$$

Here, the reactance can take two forms, the inductive reactance X_L and the capacitive reactance X_C :

$$X_L = 2\pi fL = \omega L \quad X_C = \frac{1}{2\pi fC} = \frac{1}{\omega C} \quad (1.104)$$

As can be seen from eq. 1.104, the reactance is a frequency-dependent (f) quantity that can be related to the angular frequency ω of a sinusoidal signal. A phase angle of 90° reveals a maximum capacitive reactance and a minimum resistance (see eq. 1.102), which allows a correct measurement of the capacitance. The quality factor Q is a measure for semiconductor devices to behave as ideal reactance, it describes the ratio between reactance and resistance and is sometimes referred to as dissipation factor D :

$$Q = \frac{X_C}{R} = \frac{1}{R\omega C} = \frac{1}{\tan \theta} = \frac{1}{D} \quad (1.105)$$

During common C-V measurements, a small ac voltage signal in the mV range is applied to the DUT and the impedance is determined by measuring the resulting ac current, ac voltage and phase angle (θ) between them. The applied ac voltage signal is superimposed on a dc voltage that is swept in time across the DUT. The sweep in dc voltage enables the extension of the depletion region. A basic measurement setup for such C-V characterization, including all connections is shown in Fig. 1.17.

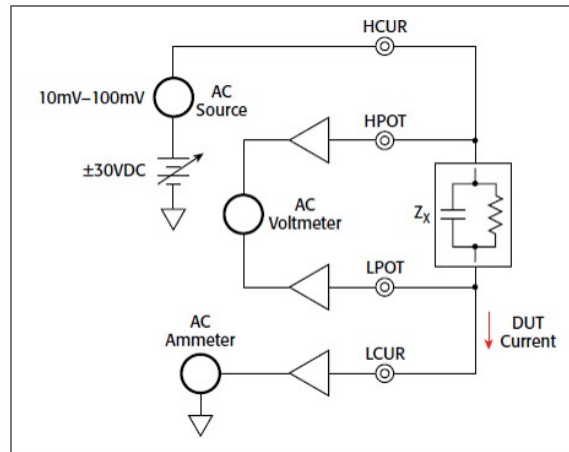


Figure 1.17: Basic setup for C-V measurements [35].

The complex electrical response of a DUT can be conventionally modeled based on the relation between the resistance (real part) and the capacitive reactance (imaginary part). Therefore, the assumption on the internal physical structure of the DUT will be expressed by either a series or a parallel equivalent electrical circuit. Fig. 1.18 (a) shows an impedance modeled by a RC series circuit and the parallel representation of the RC combination is shown in Fig. 1.18 (b).

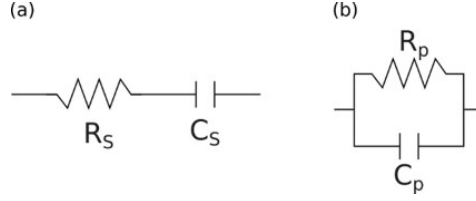


Figure 1.18: Sketch of a (a) series and (b) parallel connection of an equivalent RC circuit.

Whereas the expression of the series combination of R and X_C is similar to eq. 1.100, the equation for the parallel combination is given by:

$$Z_{series} = R + jX_C \quad Z_{parallel} = \frac{1}{\frac{1}{R} + \frac{1}{jX_C}} \quad (1.106)$$

In some cases, the reciprocal of the impedance is expressed as the complex admittance Y including the real conductance G and imaginary susceptance B given by:

$$Y = \frac{1}{Z} = G + jB \quad (1.107)$$

$$\text{with } G = \frac{1}{R} \quad B = \frac{1}{X_C}$$

Therefore, the components of the parallel equivalent circuit of Fig. 1.18 are sometimes given by the capacitance C_p and the conductance G_p .

The C-V measurements performed in this thesis are carried out with the setup shown in Fig. 1.15 and the DLTS tool that will be explained in the next section. Both tools are using the overall concept explained in this section.

1.4.3 Deep level transient spectroscopy

Like C-V characterization, deep level transient spectroscopy (DLTS) is based on space-charge measurements of basic semiconductor devices that are able to build up a space charge region (scr). It is part of spectroscopic methods because each defect level gives rise to a particular peak as a function of temperature. Here, deep level parameters like the energy position E_T , concentration N_T and capture cross-section σ can be extracted from junction capacitance transients that are caused by relaxation processes of defect charge states in the scr. In contrast, DLTS does not provide chemical or structural information of the studied defect levels, which is compensated by investigating devices of known defect content or correlation with other spectroscopic or microscopic techniques [14]. However, the DLTS method is one of the most sensitive techniques to characterize deep level defects. Defect densities N_T in the range of 4 to 6 orders of magnitude smaller than the doping density N_{dop} can be resolved ($10^{-4} \leq N_T/N_{dop} \leq 10^{-6}$) [3].

The working principle of DLTS includes the modification of the charge states of deep levels by applying voltage pulses and is mainly divided into three steps:

1. As from the reverse bias V_R condition, the scr of the measured device contains no free carriers and the trap levels are empty within the depletion region of width $w_d(V_R)$ (see eq.

1.41) resulting in a constant capacitance. This starting point of a DLTS measurement is represented as an example for a one-sided abrupt n^+p junction in Fig. 1.19 (a).

2. By applying a pulse voltage V_P for a certain time t_p , the depletion region width reduces to $w_d(V_P)$, see Fig. 1.19 (b). Free carriers are then available between $w_d(V_R)$ and $w_d(V_P)$ that will be captured by empty trap levels with energies E_T . This capture process follows the rate equations derived in section I.2.1. After a certain t_p , all traps with a density N_T are filled in the probed depletion region.
3. After pulsing, the bias is returned to the applied reverse voltage V_R of step 1. Again, the scr is empty of free carriers, which respond rapidly to the change in bias, while the majority carriers trapped in the defect levels will be emitted following the corresponding emission constants (see section I.2.1). It should be noted that in the case of the n^+p junction from Fig. 1.19, the trapped holes compensate the negative charge of the immobile ionized acceptors in the scr, resulting in a space charge density of $-q(N_A + N_T)$. Compared to the steady-state values from step 1, the depletion region width is larger, and the capacitance is smaller at the reverse bias V_R after pulse. The thermal emission of trapped charges from defect levels cause a time dependent change in w_d and therefore in capacitance, the so-called capacitance transient [14].

The obtained capacitance transient $C(t)$ can be treated by different procedures. In *conventional DLTS* methods, it is assumed that the capacitance transient $C(t)$ follows an exponential time-dependence including the temperature-dependent emission time constant τ_e [3]:

$$C(t) = C_0 \left[1 - \frac{N_T(0)}{2N_{D/A}} \exp\left(-\frac{t}{\tau_e}\right) \right] \quad \tau_e = \frac{\exp\left(\frac{E_C - E_T}{kT}\right)}{\gamma_n \sigma_n T^2} = \frac{1}{e} \quad (1.108)$$

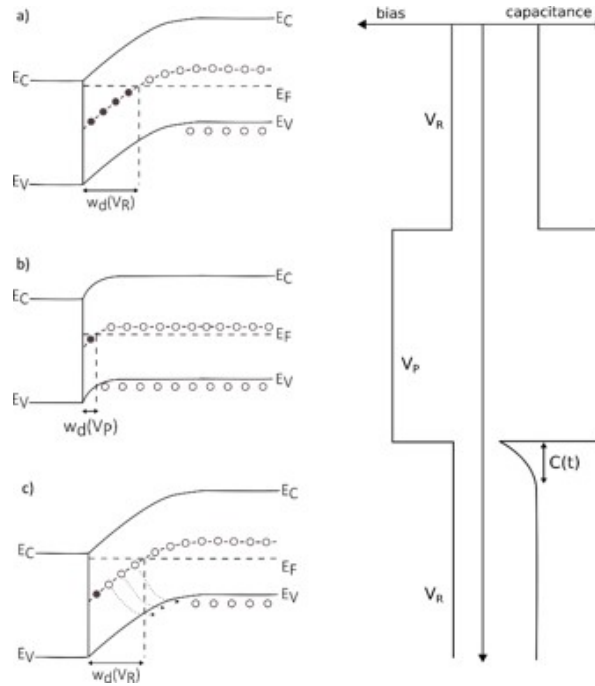


Figure 1.19: Working principle of DLTS on an one-sided n^+p junction for (a) at V_R , (b) during V_P , (c) hole emission from trap and a sketch of the applied bias and corresponding capacitance responds after [14]

1. Introduction

The emission time constant is the inverse of the emission constants for either electrons (eq. 1.10) or holes (eq. 1.11). The difference in capacitance ΔC is measured at two given times t_1 and t_2 after the end of pulse (boxcar approach by [36]):

$$\Delta C = C(t_1) - C(t_2) \quad (1.109)$$

Based on eq. 1.108, ΔC changes by varying the temperature and shows a maximum at T_{max} . At T_{max} , the decay rate of carriers from the trap level (τ_e) is identical with the rate window T_w of a boxcar integrator or the frequency of a lock-in amplifier (rate window concept) and produces the so-called the DLTS peak, see Fig. 1.20 [3]. The relation between τ_e and t_1, t_2 is then given by:

$$\tau_e(T_{max}) = T_w = \frac{t_2 - t_1}{\ln \frac{t_2}{t_1}} \quad (1.110)$$

Performing several temperature scans featuring different pairs of t_1 and t_2 , a set of $\tau_e(T)$ data can be obtained without storing the waveform of the capacitance transient itself, from which the defect parameter can be obtained via an Arrhenius plot of $\ln(\tau_e T^2)$ versus $1/T$. The activation energy of the trap level E_T with respect to E_V for p-type semiconductors and E_C for n-type materials results from the slope of the linear least-squares fit, and the intercept includes the majority capture cross section σ [14]. The trap concentration can be revealed from the peak maximum C [36]:

$$N_T = 2 \frac{\Delta C}{C} N_{dop} \quad (1.111)$$

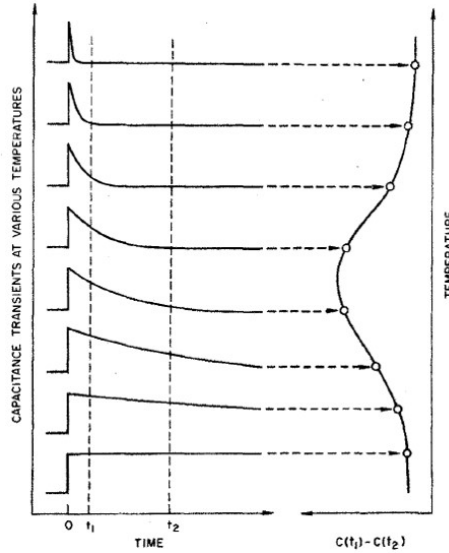


Figure 1.20: Temperature dependent capacitance transients creating the DLTS peak [36]

The limit in energy resolution of separate peaks and therefore deep levels of several units of kT as well as the time-consuming simultaneous filtering in conventional DLTS can be overcome by using *digital DLTS* methods. Here, the capacitance transients (waveform) are recorded in a certain time window T_w (period width), then digitized and stored as a whole and treated by signal processing functions to generate the typical DLTS spectrum. The DLTS spectra shown in this thesis are created by a Fourier transform algorithm that converts a time-dependent

continuous function $f(t)$ into a frequency-dependent complex function $F(i\omega)$ (DLTFS) [37]. With a digital system, the capacitance transient $f(t)$ is divided into N discrete equidistance points with a sampling interval Δt ($T_w = N\Delta t$). At each discrete point in time $t_k = k\Delta t$ the corresponding function values $f_k = f(k\Delta t)$ are recorded and the numerical Fourier transformation ($t \rightarrow k\Delta t$ and $f(t) \rightarrow f_k$) is performed [38]:

$$F_n = \sum_{k=0}^{N-1} f_k \exp \frac{-2\pi ink}{N} \quad (1.112)$$

$$f_k = \frac{1}{N} \sum_{n=0}^{N-1} F_n \exp \frac{-2\pi ink}{N} \quad (1.113)$$

Eq. 1.112 describes the transformation of a discrete value n from a complex time-dependent function into the corresponding spectrum of frequency. Eq. 1.113 explains the inverse discrete Fourier transformation, in which a discrete value is reconstructed from its frequency spectrum. Based on the emission kinetics, a certain time dependence of the transient is assumed to reconstruct the curve characteristic of simple and multiple exponential decays. A Fourier series is developed from this complex periodic function and its continuous (analytical) coefficients a_n and b_n are determined by integration:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t) \quad (1.114)$$

$$a_n = \frac{2}{T_w} \int_0^{T_w} f(t) \cos(n\omega_0 t) dt \quad (1.115)$$

$$b_n = \frac{2}{T_w} \int_0^{T_w} f(t) \sin(n\omega_0 t) dt \quad (1.116)$$

The transition to N discrete measurement points results in the discrete (numerical) Fourier coefficients c_n^D that are identical to F_n including N as a factor:

$$c_n^D = \frac{1}{N} \sum_{k=0}^{N-1} f_k \exp \frac{-2\pi ink}{N} \quad (1.117)$$

$$F_n = N c_n^D \quad (1.118)$$

Considering the relationship between discrete and continuous c_n Fourier coefficients ($c_n^D = \sum_{j=-\infty}^{\infty} c_n + jN$), $f(t)$ can be exactly reconstructed by finite discrete coefficients from a Fourier series:

$$f(t) = \sum_{n=0}^{N-1} c_n^D \exp \frac{-2\pi int}{T_w} \quad (1.119)$$

As each of the determined coefficient contains information of the transient, certain ratios of them are typical for different signal forms. During this evaluation, only lower orders (n) of continuous and discrete Fourier coefficients are considered because their difference and deviation from analytical values are smaller compared to higher order coefficients. In the following, the exponential law of time, the most frequently applied time dependencies and

1. Introduction

their Fourier coefficients are represented. A detailed overview of additional laws of time can be found in Ref. [38]. While in conventional DLTS methods the starting point of the time scale is defined at the end of the filling pulse, the starting point in DLTFs is determined by the beginning of the transient measurement and the end of filling process is then $-t_0$.

Real exponential law of time with the amplitude A , an offset B , the time constant τ and the time at the end of the charging pulse $-t_0$ [37]:

$$f(t) = A \exp\left[-\frac{t+t_0}{\tau}\right] + B \quad (1.120)$$

The real coefficients are given by:

$$a_0 = \frac{2A}{T_w} \exp\left[-\frac{t_0}{\tau}\right] \left(1 - \exp\left[-\frac{T_w}{\tau}\right]\right) \tau + 2B \quad (1.121)$$

$$a_n = \frac{2A}{T_w} \exp\left[-\frac{t_0}{\tau}\right] \left(1 - \exp\left[-\frac{T_w}{\tau}\right]\right) \frac{1/\tau}{(1/\tau^2) + n^2\omega_0^2} \quad (\text{cosine coefficient}) \quad (1.122)$$

$$b_n = \frac{2A}{T_w} \exp\left[-\frac{t_0}{\tau}\right] \left(1 - \exp\left[-\frac{T_w}{\tau}\right]\right) \frac{n\omega_0}{(1/\tau^2) + n^2\omega_0^2} \quad (\text{sine coefficient}) \quad (1.123)$$

For a real exponential law of time, particular relations between two cosine or sine coefficients have to be fulfilled [37]:

- a) $a_2 < a_1 < 4a_2$
- b) $b_2/2 < b_1 < 2b_2$
- c) $\frac{b_1 a_2}{a_1 b_2} = \frac{1}{2}$

The amplitude A of the DLTFs peak can be calculated from each coefficient in eqs. 1.122 and 1.123 and corresponds to the concentration of defect levels. For example, it is shown for the sine coefficients here:

$$A = \frac{T_w}{2} b_n \frac{\exp\left[\frac{t_0}{\tau}\right] \frac{1/\tau^2 + n^2\omega^2}{n\omega}}{\left[1 - \exp\left[-\frac{T_w}{\tau}\right]\right]} \quad (1.124)$$

The time constant is calculated from the ratio of two coefficients of different order (a_n, a_k or b_n, b_k) or the sine and cosine coefficients of the same order (a_n, b_n), so that there is no source of error due to the temperature dependence of the amplitude [37]:

$$\tau(a_n, a_k) = \frac{1}{\omega} \sqrt{\frac{a_n - a_k}{k^2 a_k - n^2 a_n}} \quad (1.125)$$

$$\tau(b_n, b_k) = \frac{1}{\omega} \sqrt{\frac{k b_n - n b_k}{k^2 n b_k - n^2 k b_n}} \quad (1.126)$$

$$\tau(a_n, b_n) = \frac{1}{n\omega} \frac{b_n}{a_n} \quad (1.127)$$

Since the time constant and amplitude can immediately be calculated from the Fourier coefficients, the optimal period width T_w to the corresponding capacitance transient can be adjusted at each temperature by a software (PhysTech GmbH). This increases the measurement

accuracy and noise suppression [37]. Instead of using the ratio of the Fourier coefficients for evaluating the emission time constant, the maxima of the Fourier temperature curves can also be evaluated to obtain Arrhenius plots similar to the conventional DLTS method.

Apart from the way of analyzing the capacitance transient, there are modifications of the basic DLTS principle in order to improve the measurement accuracy and parameter extraction [14]. Table 1.1 lists the most frequently represented variations of DLTS by explaining the refinements and showing the advantages compared to the conventional DLTS method and by mentioning the adapted usage.

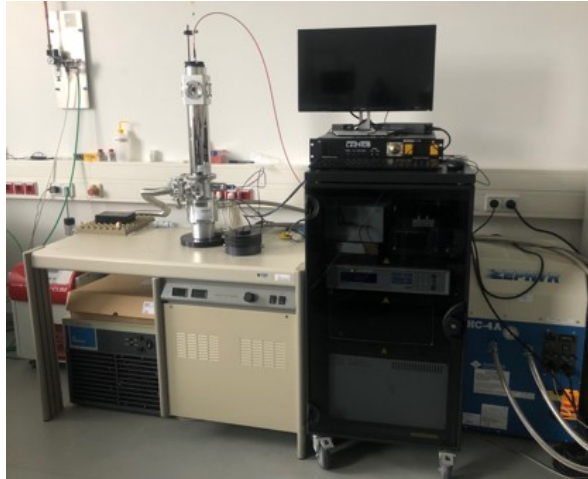


Figure 1.21: DLTS set up used in this work.

Fig. 1.21 shows a picture of the DLTS system (DL8000 and FT 1230 HERA by PhysTech) used in this thesis. While the DL8000 is connected to a liquid nitrogen cryostat (20-300K), the FT 1230 system is coupled to a Janis closed-loop liquid He cryostat (10-800K), enabling measurements of wide-bandgap materials.

The electronics of the systems includes a Boonton LCR bridge (72B for DL8000 and 7200 for FT 1230), transient recorder, signal amplifier, anti-aliasing filter (1Hz-75kHz), bias and pulse source ($\pm 20\text{V}$ and 100V option). A fast pulse (trigger) generator by Agilent and an optical excitation source are connected to the FT 1230 in addition.

Technique	Refinement	Advantage	Adapted for
Isothermal DLTS	<ul style="list-style-type: none"> • C(t) is measured at a fixed T • DLTS amplitude is extracted by applying different pulse durations t_p 	<ul style="list-style-type: none"> • Direct measure of capture cross section σ improves accuracy • Possible T dependence of σ can be estimated • Trap filling kinetics can be visualized • Exact determination of T during measurement 	<ul style="list-style-type: none"> • Distinction between repulsive and neutral or attractive defect centers due to thermal activity of σ • Distinction between point (exponential trap filling) and extended (logarithmic trap filling) defects
Constant-Capacitance (CC) DLTS	<ul style="list-style-type: none"> • C is kept constant during carrier emission by controlling V_R with a feed-back loop • Here, time dependent voltage contains the trap level information 	<ul style="list-style-type: none"> • Provide narrow spatial resolution (energy window) by determining the difference between spectra of two different bias pulses • Valid for any ratio of N_T/N_{dop}, because w_d is held constant and resulting ΔV is directly proportional to the change in scr charge 	<ul style="list-style-type: none"> • Accurate determination of defect level and carrier density profiles • More accurate measurements of samples featuring high trap densities • Suitable for interface-trapped charge measurements
Laplace DLTS	<ul style="list-style-type: none"> • C(t) is measured at a fixed T and analyzed numerically by Laplace transformation to generate spectra 	<ul style="list-style-type: none"> • All components of broad DLTS peaks can be resolved • Energy resolution in the order of up to 0.1 meV 	<ul style="list-style-type: none"> • Investigation of multiple defect levels that are only closely spaced

Table 1.1: Common modifications of basic DLTS measurement principle after [3, 14].

2

Electrical activity of threading dislocations in Ge-rich SiGe heterostructures

2.1 Scientific background

2.1.1 Ge and Ge-rich SiGe-based heterostructures integrated on Si(001)

Germanium (Ge) is a group IV elemental semiconductor that has played an important role in device applications for decades: the first transistor was made of bulk Ge in 1947, which is probably the basis of our present semiconductor industry. While Silicon (Si) has become the most prevalent semiconductor material in the meantime, the properties of Ge such as a high electron ($3900 \text{ cm}^2/\text{Vs}$ [7]) and hole ($1900 \text{ cm}^2/\text{Vs}$ [7]) mobility continue to make the material interesting for device applications. Since the lack of high-quality native oxides of Ge was overcome by introducing high-k dielectrics, Ge can now be used as alternative channel material for high-performance metal-oxide-semiconductor field-effect transistors (MOSFETs) [7]. Furthermore, strain in Ge can modify the band structure, enabling a transition from indirect to direct bandgap material, thus lasing in the mid-infrared region become possible in strained Ge layers [4, 39]. In addition, strain leads to a boost in carrier mobility and device performance. Here, compressive uniaxial stress enhances the hole mobility in p-type transistors [40, 41]. Based on the chemical similarity to Si, both are of the cubic diamond structure featuring covalent bonds, the growth of Ge on Si and their alloys are predestined for strain engineering and bandgap tuning. Accordingly, the use of Ge and Ge-rich SiGe alloys as active material enables, among others, the fabrication of high-speed photodetectors [39] and THz quantum cascade lasers (QCL) [42, 43]. Based on large spin-orbit coupling and long spin lifetimes, Ge and Ge-rich SiGe alloys are emerging as a promising material for semiconductor based qubits [44] and spintronic devices [45] for quantum technology. Hence Ge and Ge-rich silicon-germanium (SiGe) alloys are promising candidates for the

fabrication of novel devices in the field of photonics and optoelectronics. Additionally, Ge and its alloys with Si are compatible to the commonly implemented complementary metal-oxide-semiconductor (CMOS) technology. However, a CMOS-compatible fabrication of Ge-based heterostructures requires the integration on (001)-oriented Si substrates. Owing to the large lattice mismatch between Ge and Si (4.2%) and the difference in thermal expansion coefficients, mechanical stress builds up during crystal growth. In order to adjust the strain and thus the electron- and/or hole-energy band profiles of the active layers a full plastic relaxation of some of the layers is needed. For Ge-rich SiGe/Ge heterostructures, this is commonly achieved by realizing a reverse graded SiGe virtual substrate (RGVS) on Si substrates. Here, a relaxed Ge buffer is first deposited on the Si substrate followed by a gradual decrease of the Ge content in the subsequently grown layers. These RGVS promote the full relaxation of the lattice by formation of misfit dislocations (MD), while minimizing the density of threading dislocations (TD) [46, 47].

While misfit dislocations are located at hetero-interfaces, TDs extend from the heterointerface running through the entire heterostructure up to the free surface of the crystal. As such, it is obvious that TDs can be an important issue for device performance, especially for vertical device designs. The origin and propagation of these TDs depend strongly on the chosen range in composition and layer thicknesses of the SiGe/Ge heterostructure as well as the process conditions of their fabrication. It is then of paramount importance to clarify the electrical activity of TDs in novel Ge-rich SiGe heterostructures according to their device applications. Therefore, an in-depth understanding of the electrical activity of TDs is necessary and will support device development and the assessment of device performance.

2.1.2 Electrical activity of TDs in Ge and Ge-rich SiGe-based heterostructures

Early studies on the electrical activity of extended defects have been performed on plastically deformed high purity Ge bulk crystals. These studies pointed to the formation of TD-related one-dimensional (1D) bands of shallow states, which split off from the valence and conduction band, most likely related to stress fields associated with dislocations [24, 28]. In case of Ge(Si) layers integrated on Si substrates, it is important to investigate the impact of grown-in dislocations associated with strain relaxation. Here, a network of dislocations forms especially at the Ge/Si heterointerface featuring defect states that impact the generation-recombination properties i.e. as source of junction leakage currents and reduced carrier lifetimes [48].

Reported leakage currents in p-n junctions depend on the Ge content as the bandgap shrinks with increasing Ge content and increases proportionally with the amount of threading dislocation density (TDD) [49, 50] for low Ge content SiGe alloys, while the leakage current becomes independent of the TDD below a threshold value of $\approx 10^7 \text{ cm}^{-2}$ [41]. In contrast, leakage currents in thick relaxed epitaxial Ge-rich SiGe and Ge layers are not proportional to the TDD, which points rather to other processing-induced defects and mechanisms of leakage. Recombination lifetimes in small-scale Ge p-n junctions without TDs amounts to the order of $1 \mu\text{s}$, while the presence of TDs leads to a large decrease [48]. A post-deposition thermal anneal leads to a reduction in TDD of approximately one order of magnitude caused by the movement and annihilation of threading arms. Nevertheless, the corresponding leakage

currents decrease only by a factor of 2-3 that cannot be explained by the reduction of TDs alone, but is rather associated with a removal of point defect clusters in the material [41, 50]. In addition, investigated source/drain junctions showed leakage currents dominated by the implantation conditions of high phosphorus doping rather than by TDs [41].

Information on defect states of grown-in dislocations in Ge bulk crystals has in the past been obtained from DLTS measurements. Here, different energy bands are revealed and attributed to the presence of dislocations [51, 52]. In p-type Ge crystals, two bands of defects states have been found centered at $E_V + 0.025$ eV and 0.1 eV attributed to the strain field surrounding 60° dislocations, while a third band at $E_C - 0.09$ eV correlated to screw dislocations can only be found in n-type Ge [52]. Less work is reported on TD related defect states in hetero-epitaxial layers integrated on Si substrates. Bulk and interface states related to TDs are often assessed by MOS capacitors fabricated on Ge-on-Si samples [48]. Here, an increase in interface state density D_{it} has been observed by increasing the number of TDs in p-type Ge epitaxially grown on Si [48, 53]. In addition, hole traps featuring a mid-gap activation energy of $E_V + 0.29$ eV and a hole capture cross-section σ_p of 1×10^{-15} cm² have been found in p-type Ge layers [48]. Such mid-gap traps have been attributed to an agglomeration of point defects trapped in the strain field around dislocations [48]. Dislocations without point defect clusters in their strain fields are referred to clean or undecorated and it is assumed that in p-type material a one-dimensional band of shallow states close to the valence band edge arises with the maximum level at $E_V + 0.15$ eV and a small σ_p of 1×10^{-19} cm² [48].

Previous investigations of the electrical activity of TDs were carried out on devices featuring TDDs in the range of $10^7 - 10^{10}$ cm⁻² [41, 48, 49] and the variation of TDD was limited to a post-growth anneal treatment. For reasonable thicknesses of epi layers (1.5-2.0 μ m) the reported minimum TDD achievable by high temperature annealing is in the order of 10^7 cm⁻² [41]. However, device physics as well as device design requirements push towards a further reduction in TDD, making it crucial to obtain a quantitative understanding of the impact of TDs on device performance particularly in the low density regime of $10^5 - 10^7$ cm⁻² TDs.

The basic concept of introducing the topic in this section has been published in [54].

2.2 Investigated heterostructures – probability of tuning the TDD

The investigated $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures in this chapter serve as RGVS for a CMOS-compatible integration of n-type Ge/SiGe THz QCL structures on Si [42, 43, 55]. A detailed understanding of the electrical activity of TDs that originate in the reverse graded buffer and propagate into the active laser region (quantum wells) enables a more precise theoretical simulation of the designed QCL devices and an estimation of potential losses during the injection process.

By means of a beneficial second interface in the reverse graded buffer technique used for the integration of Ge-rich SiGe heterostructures on Si(001) it becomes possible to tune the TDD in $\text{Si}_{0.06}\text{Ge}_{0.94}$ layers in a wide range from 10^9 cm^{-2} to 10^6 cm^{-2} , as reported in [56]. As can be seen in Fig. 2.1, an increase of the Ge buffer thickness (red squares) results in a decreasing TDD [57]. Here, the full relaxation of the thick Ge epi-layers prevent the extension of existing misfit segments at the Ge/Si interface, while the probability of interaction between two TDs having opposite Burger's vectors is enhanced during the extended growth time, leading to mutual annihilation [56]. Since the number of annihilation events declines with lower TDDs, the geometrical effect is becoming increasingly ineffective with increasing Ge layer thickness and a limit of saturation above $4 \mu\text{m}$ of 7×10^6 TDs per cm^{-2} is observed [56]. However, the growth of a subsequent Ge-rich SiGe layer (blue dots in Fig. 2.1) leads to a further reduction of TDD resulting in a minimum TDD of $1.7 \times 10^6 \text{ cm}^{-2}$ for a thickness of $7 \mu\text{m}$ for the whole $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructure. Theoretical simulations revealed that the subsequent strained Ge-rich SiGe reverse-graded layer provides additional mobility of the TDs causing further bending at the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ interface in order to degrade the excess strain in the $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer [56]. This bending of threading arms enhances the probability of annihilation even if the TDD is below the geometrical limit [56]. An increase of $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer thickness on equal Ge/Si virtual substrates (VS) only results in a small reduction of TDD from $3.3 \times 10^7 \text{ cm}^{-2}$ down to $2.7 \times 10^7 \text{ cm}^{-2}$ [56]. In addition, a high temperature annealing step at 700°C or 800°C does not result in further reduction of the TDD [56].

Since material physics as well as practical considerations such as fabrication cost can be expected to impose limits on a further reduction of the TDD, it is particularly important to obtain a quantitative understanding of the impact of TDs on device performance in the above-mentioned low-density regime.

The $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ heterostructures that are subject of this analysis were grown in IHP's cleanroom on 200 mm diameter Si(001) wafers in a commercial ASM Epsilon 2000 reduced pressure chemical vapor deposition reactor at a pressure of 80 Torr. After wet chemical cleaning of the substrate and a prebake in a hydrogen (H_2) atmosphere in order to remove the native oxide, a 100 nm-thick seed Ge layer was grown at 350°C using a germane-nitrogen gas mixture. After the seed layer formation, variable thickness and fully relaxed Ge buffers were grown without intentionally doping at a temperature of 550°C providing the basis for tuning the TDD. On top of the Ge/Si(001) VS, a $1.2 \mu\text{m}$ thick $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer was deposited at 550°C . The epilayers are of intrinsic character in order to exclude unintentional interaction with dopant atoms or introducing processing-induced defects e.g. by implantation. More details on

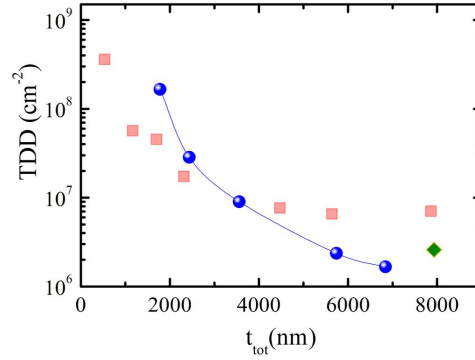


Figure 2.1: TDD as a function of the total heterostructure thickness t_{tot} for Ge/Si(001) (red squares) and $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ (blue dots) heterostructures. The green marker shows the impact of an additional Ge/SiGe heterointerface [56].

the deposition process can be found in Ref. [56].

According to Fig. 2.1, the heterostructures investigated in this thesis feature Ge buffer thicknesses between $0.7\mu\text{m}$ and $4.5\mu\text{m}$ and, consequently, TDDs ranging from $1 \times 10^9 \text{ cm}^{-2}$ to $3 \times 10^6 \text{ cm}^{-2}$. The TDDs of the corresponding $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ heterostructures are estimated to use the common approach of defect etching (etch pit count). Here, a calibrated Secco etch solution [58] composed of alkali dichromate ($\text{K}_2\text{Cr}_2\text{O}_7$) and hydrofluoric acid (HF) diluted in distilled water (H_2O) is used to etch the surface with an etch rate that is increased at the location of disturbances of the crystal lattice like dislocations since the interatomic bonds are weaker than in defect-free crystal parts. The observed dislocation etch pits were imaged by a Zeiss Merlin scanning electron microscope (SEM) and counted over a surface area of $55 \mu\text{m}^2$. Fig. 2.2 exemplarily presents the SEM images of observed etch pits on $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ heterostructures featuring TDDs of a) $3 \times 10^6 \text{ cm}^{-2}$, b) $9 \times 10^6 \text{ cm}^{-2}$ and c) $2 \times 10^7 \text{ cm}^{-2}$.

Based on the above introduced reverse graded buffer technique, the electrical activity of TDs

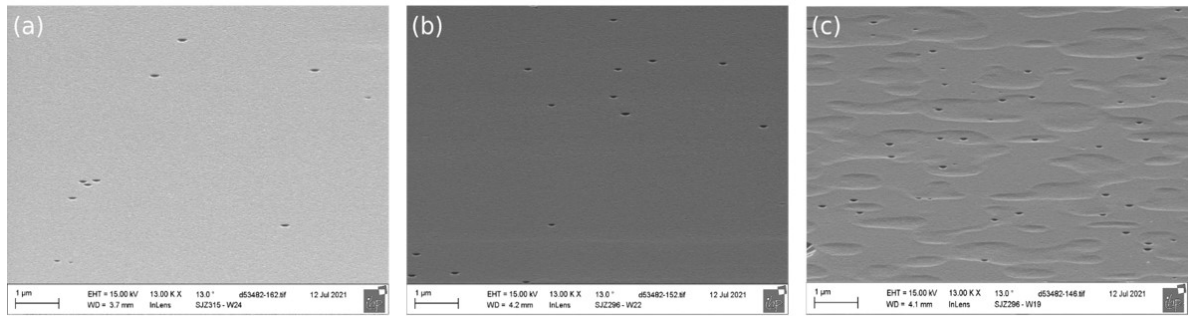


Figure 2.2: Etch pits observed on $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures featuring TDDs of a) $3 \times 10^6 \text{ cm}^{-2}$, b) $9 \times 10^6 \text{ cm}^{-2}$ and c) $2 \times 10^7 \text{ cm}^{-2}$.

in the top $\text{Si}_{0.06}\text{Ge}_{0.94}$ epilayers can be investigated under consideration of equal thicknesses ($1.2 \mu\text{m}$) and degree of plastic relaxation ($R = 106\%$ [56]). Even if the TDD and, therefore the degree of plastic relaxation is usually not uniform over the whole epi layer thickness caused by annihilation processes during growth, the use of a beneficial (second) $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ interface enables the growth of homogenous Ge-rich SiGe epilayers only distinguished by their TDD. Related scanning transmission electron microscopy (STEM) images of the same three samples shown in Fig. 2.2 are presented in Fig. 2.3. Here, the position where the two relaxation

2. Electrical activity of threading dislocations in Ge-rich SiGe heterostructures

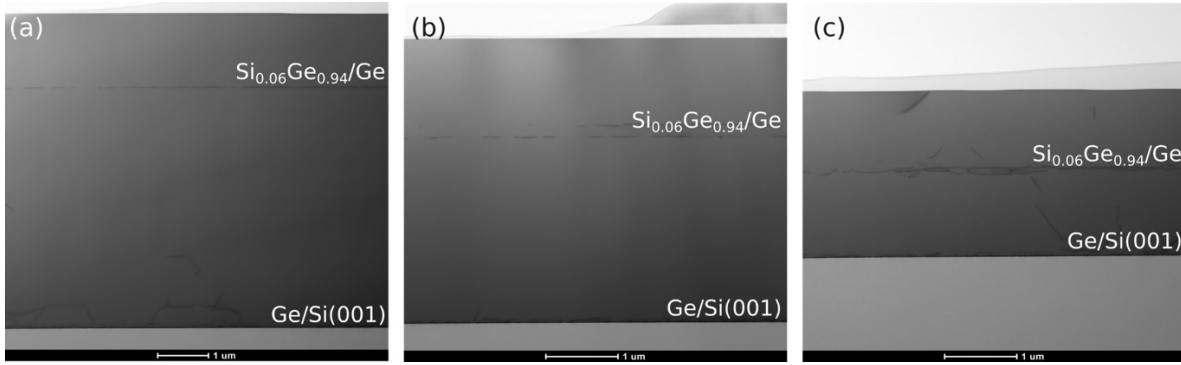


Figure 2.3: STEM images of investigated samples featuring TDDs of a) $3 \times 10^6 \text{ cm}^{-2}$, b) $9 \times 10^6 \text{ cm}^{-2}$ and c) $2 \times 10^7 \text{ cm}^{-2}$.

processes take place is illustrated in the complete heterostacked sample, at the Ge/Si(001) and Si_{0.06}Ge_{0.94}/Ge interface. Here, an agglomeration of dislocations becomes visible. Figure 2.4 enables a closer look at the defective interfaces. While the dislocations at the bottom interface extend far into the Ge buffer, it seems that most of the dislocations are pinned at the second interface. It should be noted here, that the areas above the defective interfaces are not free of defects, but with decreasing TDD it becomes more difficult to observe them in the size-limited section of a TEM lamella as is possible in higher TDD samples where TDs run through the whole heterostructure (see Fig. 2.4(c)).

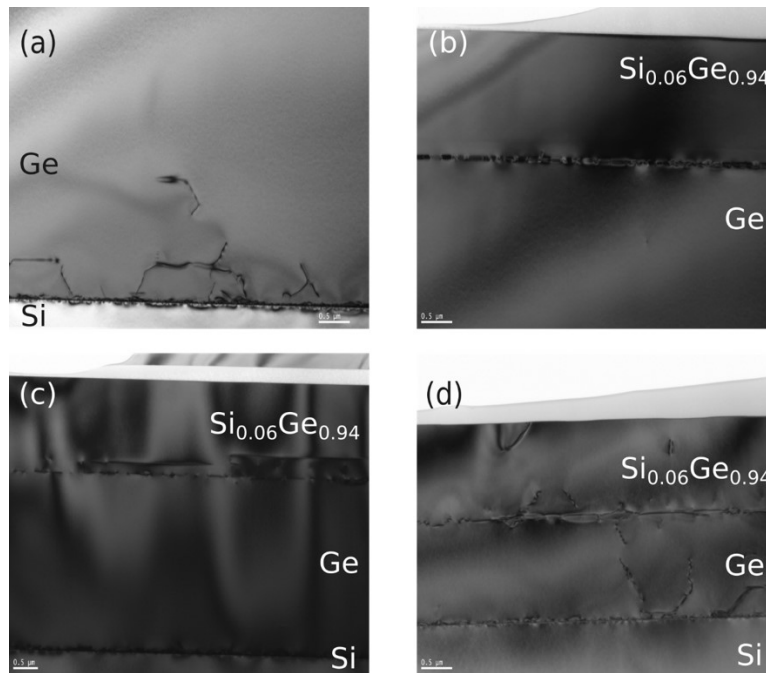


Figure 2.4: Defective interfaces of investigated heterostructures featuring different Ge buffer thicknesses: a) and b) $4.5 \mu\text{m}$, c) $2.3 \mu\text{m}$ and d) $1.2 \mu\text{m}$.

Parts of the content of this section has been published in [54]. The investigated samples were grown by the co-author O. Skibitzki and Y. Yamamoto in IHPs fabrication pilot line and the TEM images were taken by my colleague M.A. Schubert.

2.3 TDD dependent Si_{0.06}Ge_{0.94}/Ge p-n⁺ junction diode characteristics

The development of a Si_{0.06}Ge_{0.94} dummy structure, which is close to the real VS system of n-type Ge/SiGe THz QCL structures integrated on Si, while simultaneously being suitable for electrical measurements, provides the basis for studying the influence of grown-in TDs on the vertical transport mechanisms along the TD direction. Therefore, the as-grown Si_{0.06}Ge_{0.94}/Ge/Si heterostructures are slightly modified, as shown in Fig. 2.5. These heterostructures are grown on standard Czochralski Si wafers of (001) crystal orientation that are boron (B)-doped, featuring a resistivity of 5-22 Ωcm. The Ge buffer thickness is varied in order to tune the TDD in the subsequent Si_{0.06}Ge_{0.94} buffer layers, while keeping their thickness and degree of relaxation constant as explained in the previous chapter. By introducing a 150nm thick highly phosphorous (P)-doped Si_{0.06}Ge_{0.94} layer in the order of $1 \times 10^{19} \text{ cm}^{-3}$, the vertical n⁺-p homojunction diode is formed between the n-doped and the 1.2 μm thick nominally intrinsic (i)-Si_{0.06}Ge_{0.94} layers caused by a lightly p-type doping of the intrinsic layer. This p-doping has been verified by preceding lateral Hall effect measurements, pointing to a p-type conductivity of the studied intrinsic material. An effective hole density that is averaged over the intrinsic region is estimated in the 10^{15} - 10^{16} cm^{-3} range. Such p-type conduction of nominally undoped Ge-based material is in agreement with previously published literature on Ge-rich SiGe layers [59, 60], germanium-tin (GeSn) films grown on Ge substrates [61] and plastically deformed Ge bulk materials [62]. However, the origin of this p-type conduction is still under discussion in literature and is generally attributed to acceptor-like defect states caused by plastic deformation and/or strain relaxation [59, 62].

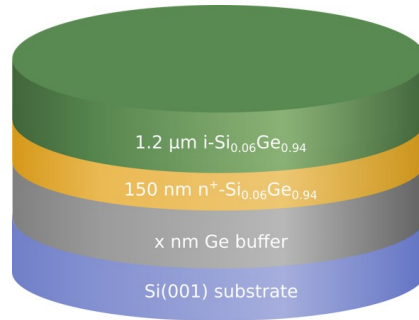


Figure 2.5: Sketch of the Si_{0.06}Ge_{0.94} dummy structures used for electrical characterization.

The investigated diodes were fabricated at the University of Glasgow (UGLA), a project partner of the European Union's Horizon 2020 research and innovation program under Grant Agreement No. 766719 (FLASH). Hall effect measurement results were performed at IHP and provided by Dr. W. Seifert. The Comsol Multiphysics simulation data were carried out by the co-author Dr. C.L. Manganeli. Secondary ion mass spectroscopy measurements were performed by IHP's offline-characterization team. I carried out the I-V and C-V measurements and analyzed the data. The majority of the results in this section has been published in [54].

2.3.1 Device fabrication

Vertical mesa-structured devices were fabricated out of the heterostructures as shown in Fig. 2.6, using standard optical lithography at UGLA. To create the buried p-n⁺ homojunction, a 150 nm thick highly n-doped Si_{0.06}Ge_{0.94} layer ($1 \times 10^{19} \text{ cm}^{-3}$) is grown on top of the Ge buffer, using silane and germane as reactant gases as well as phosphine as dopant gas, before the 1.2 μm thick intrinsic Si_{0.06}Ge_{0.94} layer is deposited. While the Ge buffer layer thickness is varied to tune the TDD, the i-Si_{0.06}Ge_{0.94} film thickness is similar in all devices (see Fig.2.5).

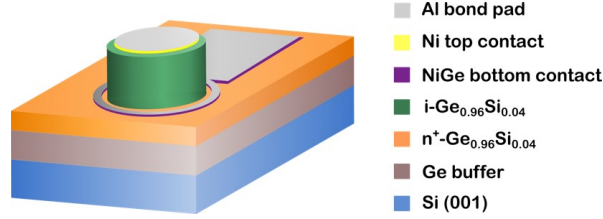


Figure 2.6: Sketch of the fabricated devices [54].

Secondary ion mass spectroscopy (SIMS) results show that the dopant concentrations (P, B) are below the limit of detection (lod) in the intrinsic region and the in-diffusion length of P towards the surface is less than 5 nm/decade, thus allowing the formation of sharp buried homojunctions. The corresponding SIMS profiles can be seen in Fig. 2.7 for heterostructures featuring TDDs of $3 \times 10^6 \text{ cm}^{-2}$, $9 \times 10^6 \text{ cm}^{-2}$ and $2 \times 10^7 \text{ cm}^{-2}$. Here, the Si and P concentration is measured by an 11 kV cesium ion source, while the B concentration is extracted by a 7 kV oxygen ion source. The dashed lines show the P and B signal, while the full lines represent the Si content in Fig. 2.7.

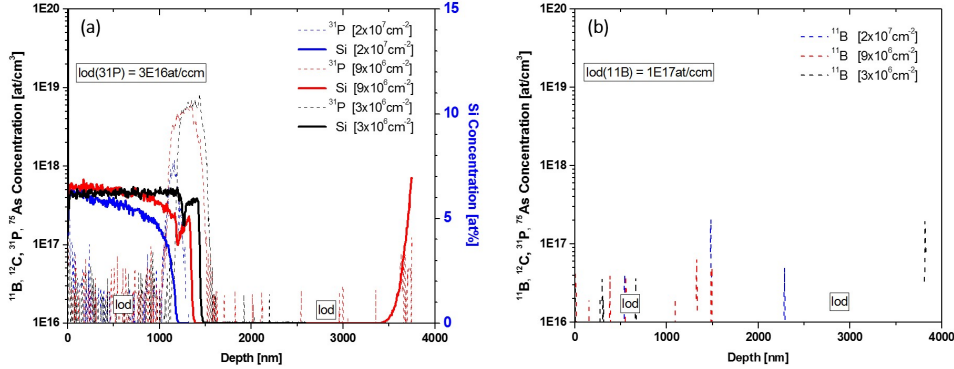


Figure 2.7: SIMS profiles of three samples featuring different TDDs measured with (a) 11 kV cesium and (b) 7kV oxygen ion source.

By means of a lift-off process, a 50 nm thick nickel (Ni) layer as a top metal contact was evaporated on top of the intrinsic Si_{0.06}Ge_{0.94} layers for defining the diode area. Subsequently, the remaining SiGe material was etched by inductively coupled plasma (ICP) mesa-etching, by using a gas mixture of sulfur hexafluoride and octafluorocyclobutan (SF₆/C₄F₈) [63]. A ring-shaped ohmic bottom contact (lift-off) around the residual material of the intrinsic Si_{0.06}Ge_{0.94} layer (green cylinder in Fig.2.6) connected to a bigger bond pad were formed on the highly n-doped Si_{0.06}Ge_{0.94} layer. Here, two approaches are adopted to form ohmic contacts. The first set of samples initially possessed a silver-antimony (Ag-Sb) metal alloy containing 1% of

Sb that was annealed at 400°C to produce an ohmic contact [64]. In the latter device set a Ni metal was deposited and annealed at 330 °C for 30 s to form NiGe [65]. This was followed by a deposition of a 500 nm titanium-aluminum (Ti-Al) protection layer on top of all metal contacts to accommodate the measurement needle probe.

The characteristics of both ohmic contacts were evaluated by measuring the contact resistance R_C using the circular transmission line method (CTLM) with test structures that are simultaneously fabricated during contact preparation on the n⁺- Si_{0.06}Ge_{0.94} layer. As shown in Fig. 2.8(a) the CTLM test structure consist of a circular inner region of diameter L , a conducting outer region (marked in purple) and the changing gap size d between them. In the measured CTLM test structures, d varies between 20 and 55 μm . The total resistance R_T is measured by applying a bias between the circular and the outer contact area and measuring the flowing current and plotted against the spacing d (see Fig. 2.8(b)) [3]. The R_T is then given by [3]:

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T)C \quad \text{with} \quad C = \frac{L}{d} \ln\left(1 + \frac{d}{L}\right) \quad (2.1)$$

where C is the correction factor, R_{sh} the sheet resistance of the material below the contact and L_T the transfer length including the specific contact resistivity ρ_c ($L_T = \sqrt{\rho_c/R_{sh}}$).

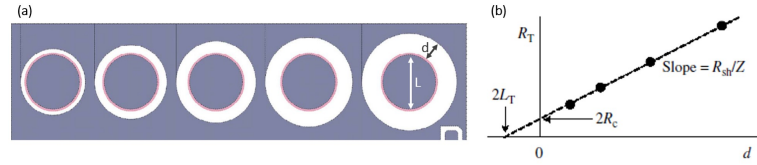


Figure 2.8: (a) Circular contact resistance test structure and (b) schematic of total resistance as a function of contact spacing [3].

Fig. 2.9 shows the measured R_T for bottom contacts of both generations on the highly n-doped Si_{0.06}Ge_{0.94} contact layer. As can be seen here, the correction of the measured data by factor C is necessary to obtain a linear fit, otherwise ρ_c will be underestimated. According to the procedure indicated in Fig. 2.8(b), average R_C and L_T values of Ag-Sb contacts are estimated from the plot in Fig. 2.9 (a) of approximately 8 Ω and 5 μm , respectively. In addition, the specific contact resistivity ρ_c for Ag-Sb contacts is calculated as $3.8 \times 10^{-7} \Omega\text{cm}^2$. NiGe contacts of generation 2 show an average R_C and L_T of 16 Ω and 36 μm respectively, while the specific contact resistivity ρ_c is calculated to $2.9 \times 10^{-5} \Omega\text{cm}^2$.

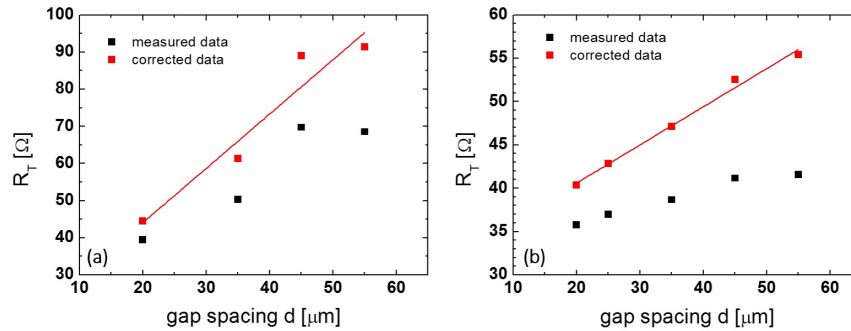


Figure 2.9: Plot of the total resistance as a function of gap spacing for the CTLM test structures of generation (a) 1 and (b) 2 before and after data correction.

2. Electrical activity of threading dislocations in Ge-rich SiGe heterostructures

The size of the diodes varies in four different sets of devices featuring increasing diameters ($250\mu\text{m}$, $500\mu\text{m}$, $750\mu\text{m}$ and $1000\mu\text{m}$) and three different gap spacings ($10\mu\text{m}$, $25\mu\text{m}$ and $50\mu\text{m}$) between the outer ring bottom contact and the inner mesa. The different diode sizes allow for the distinction between different geometrical current components as it will be shown in the next sections. The layout of these devices is sketched in Fig. 2.10, showing one single device enlarged as inset.

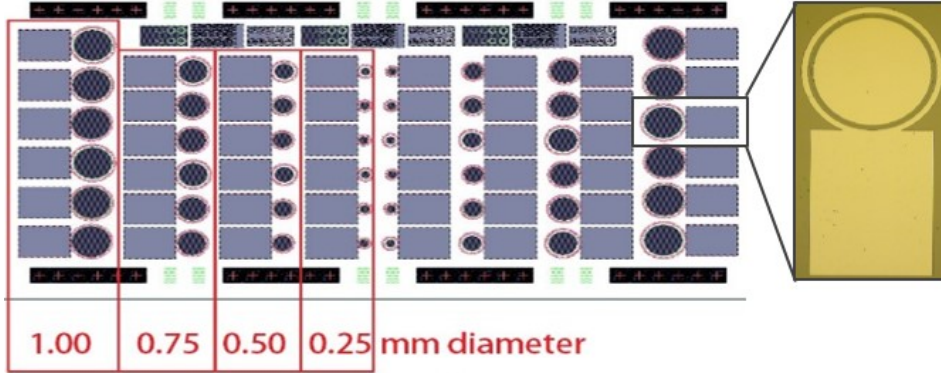


Figure 2.10: Device layout used in this work.

A simulated electrical profile of the studied device structure at 0V is displayed in Fig. 2.11 in which only Ge is assumed as material for simplicity. Here, a p-doping of $1 \times 10^{16} \text{ cm}^{-3}$ and a thickness of $1.5 \mu\text{m}$ are assumed for the $i\text{-Si}_{0.06}\text{Ge}_{0.94}$ layer as well as a Schottky barrier height of 0.49 eV for the top Ni contact and an ideal ohmic contact to the $n^+\text{-Si}_{0.06}\text{Ge}_{0.94}$ layer. In combination with the n^+ -doped layer underneath, it becomes obvious that the formed buried $p\text{-}n^+$ homojunction is the dominant junction compared to the negligible barrier formation at the top metal contact. Due to a barrier height of Ni that is similar to the conduction band energy of Ge, the depletion layer is very thin. Consequently, the presented results are relative to the one-sided $p\text{-}n^+$ homojunction formed between n -doped and intrinsic doped $\text{Si}_{0.06}\text{Ge}_{0.94}$ layers. Owing to the high n -doping of the bottom $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer, the depletion layer predominantly extends into the $i\text{-Si}_{0.06}\text{Ge}_{0.94}$ layer. As such, the vertical transport along TD direction can be probed exclusively in the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer, thus avoiding any possible interactions with dopant atoms.

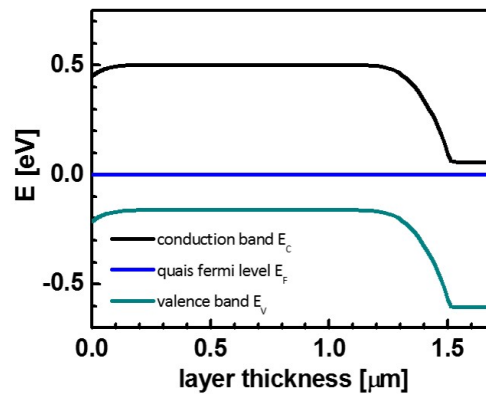


Figure 2.11: Device layout used in this work.

generation	sample	Ge buffer thickness	TDD
1	W21	0.53 μm	$2 \times 10^8 \text{ cm}^{-2}$
	W19	1.15 μm	$2 \times 10^7 \text{ cm}^{-2}$
	W22	2.30 μm	$9 \times 10^6 \text{ cm}^{-2}$
2	W19	1.15 μm	$2 \times 10^7 \text{ cm}^{-2}$
	W22	2.30 μm	$9 \times 10^6 \text{ cm}^{-2}$
	W24	4.40 μm	$3 \times 10^6 \text{ cm}^{-2}$

Table 2.1: Sample sets for generation 1 and 2 featuring ohmic contacts of Ag-Sb and NiGe respectively.

Table 2.1 displays the two investigated sets of samples that were prepared at UGLA including the corresponding Ge buffer thickness and the TDDs measured by Secco etching. All device generations are fabricated from the same material (W19-W24). Generation 1 devices feature ohmic contacts composed of Ag-Sb and ranging in TDD from 2×10^8 to $9 \times 10^6 \text{ cm}^{-2}$, while the ohmic contacts in generation 2 devices are made of NiGe and the investigated TDD range is 2×10^7 to $3 \times 10^6 \text{ cm}^{-2}$.

2.3.2 Room temperature I-V characteristics

In order to evaluate the quality of the fabricated devices, the scalability between current and contact area is reviewed. Therefore, the diodes were connected according to Fig. 2.12, i.e., a bias is applied between the top and bottom metal contacts and the current is measured. Following this measurement configuration the investigated junctions conduct current when positively biased (forward direction) and the current flow are suppressed at negative bias (reverse region) as can be seen in all of the following I-V plots. Thus, the p-type doping of intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ can also be demonstrated by the formation of a buried p-n⁺ homojunction marked by the dotted circle in Fig. 2.12 and its measured I-V characteristics.

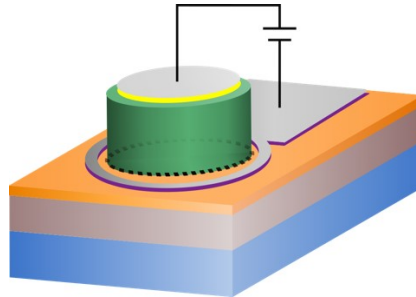


Figure 2.12: Measurement configuration on devices sketched in Fig. 2.6.

The following I-V measurements in this section were performed at room temperature (300K). The bias dependent current density (J-V) plots of all samples featuring different TDDs from generation 1 are presented in Fig. 2.13. Here, the available diode sizes are compared for each sample. Although only one J-V curve per diode size is shown, all diodes are tested and

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provide similar J-V behavior. It becomes obvious that the current density values do not scale with contact areas neither in the forward nor the reverse bias region. Furthermore, repeated measurements of the same device, show inconsistencies over time. This points towards a suspectable choice of contacts. Therefore, a second generation of devices were fabricated using NiGe instead of Ag-Sb as ohmic contact. As the difference in J-V curves becomes less significant at TDD values of $2 \times 10^7 \text{ cm}^{-2}$ and the rectifying behavior of the diodes seems to vanish (see Fig. 2.13(b-c)), the device series of the second generation were limited to TDD values of $2 \times 10^7 \text{ cm}^{-2}$ and expanded to lower values.

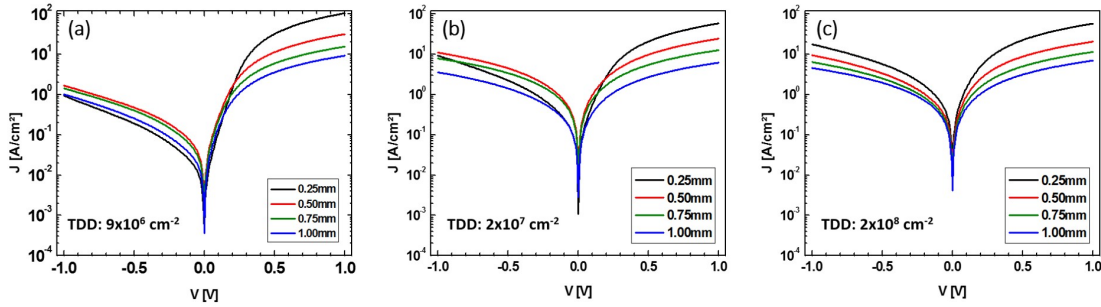


Figure 2.13: Measurement configuration on devices sketched in Fig. 2.6.

In Fig. 2.14, the obtained J-V characteristic of the two fabricated generations of the same sample (W22) are compared using either Ag-Sb or NiGe as ohmic bottom contacts. While the J-V curves obtained on Ag-Sb-based devices presented in Fig. 2.14(a) do not apparently scale with the diode area, devices featuring NiGe-based ohmic contacts (see Fig. 2.14(b)) show a reliable scalability of current flow in a certain range of applied voltages. Moreover, devices with NiGe contacts feature reduced reverse bias current densities and an enhanced rectification as compared to AgSb contacted devices. This contrast of the scalability could be related to an Ag-Sb in-diffusion into the diode structures which may impact the electrical behavior of the investigated diodes or to oxidation issues altering their ohmic behavior. For this reason, the subsequent analysis is performed using devices which have the CMOS-compatible NiGe ohmic contact system [65].

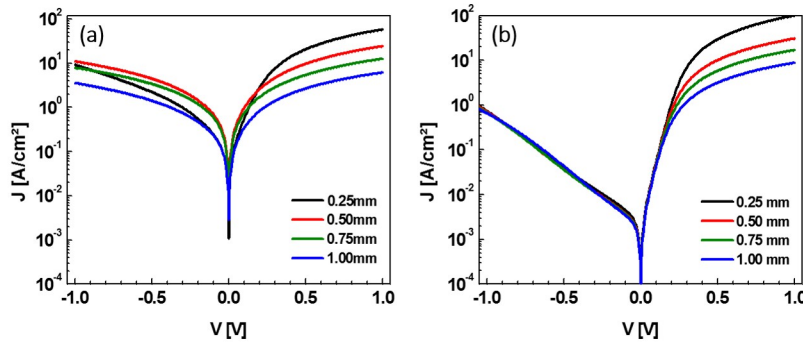


Figure 2.14: J-V characteristics of devices fabricated on sample features highest TDD ($2 \times 10^7 \text{ cm}^{-2}$) using (a) Ag-Sb and (b) NiGe as ohmic bottom contact material.

Fig. 2.15 shows the J-V characteristics of all used diode sizes of samples from generation 2, characterized by TDDs of $3 \times 10^6 \text{ cm}^{-2}$, $9 \times 10^6 \text{ cm}^{-2}$ and $2 \times 10^7 \text{ cm}^{-2}$. Up to a certain current

level of 0.1-1 A/cm², all measured devices featuring a Ge buffer thickness up to 2.3 μm and, therefore, a TDD down to 9x10⁶ cm⁻², show an ideal scalability of current density with diode size (Fig. 2.15(b-c)), which is found to be a robust outcome for all devices on both samples. Beyond this current level, a decreasing current density for increasing diameter of the diode is observed, both under forward and reverse bias. It should be noted that the bias range in which J scales with the area is smaller in samples that have a higher TDD. As described below, the deviation of current scalability at larger applied biases is related to the effect of series resistance R_S that must be considered in the voltage drop across the junction. In contrast, the sample featuring the lowest TDD of 3x10⁶ cm⁻² shows no ideal scalability of current density with contact area (see Fig. 2.15(a)). More particularly, a large distribution of results with only a limited number of scaling devices is found. Therefore, an extensive statistical analysis of the J-V characteristics of all available devices was performed.

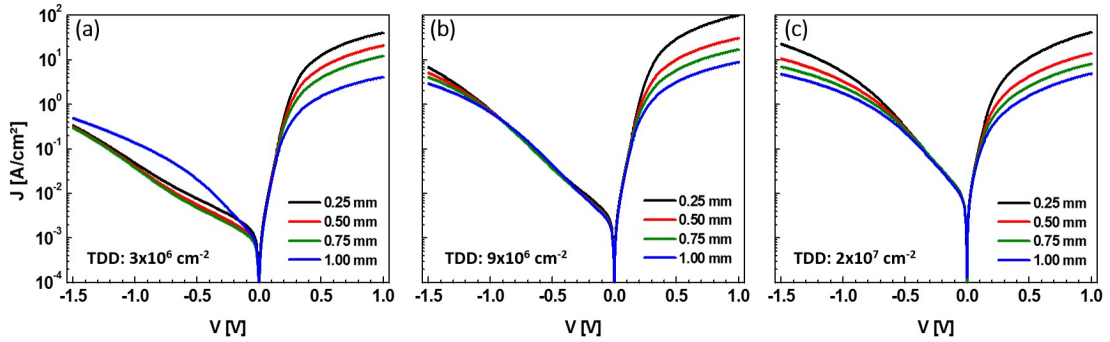


Figure 2.15: J-V characteristics of generation 2 samples featuring Ge buffer thickness of (a) 4.40 μm, (b) 2.30 μm and (c) 1.15 μm.

While almost no variation of the J-V curves is observed in the smallest diameter diodes (0.25 mm, Fig. 2.16(a)), the fluctuation seems to increase with increasing device diameters (Fig. 2.16(b-d)). In case of 1.00 mm devices, just view devices follow the expected scaling (Fig. 2.16(d)). In order to understand the reason of this puzzling result, the measured devices are imaged using optical microscopy. Fig. 2.17 (a) shows an exemplarily optical image of the measured 0.50 mm devices. Here, the presence of “cracks” become clearly visible on the surface.

The observed cracks are equally found on fabricated devices and as-grown material (see Fig. 2.17(b)) and, therefore can be attributed to the release of thermal stress acquired by the growth of such thick samples, including 4.40 μm of Ge buffer and 1.40 μm $\text{Si}_{0.06}\text{Ge}_{0.94}$ layers. By examining the whole wafer, an uneven distribution of these cracks is monitored where large areas of the wafer are completely crack-free. It should be noted here that cracks were only observed in W24 that features the thickest Ge buffer layer and, consequently, suffers the highest thermal stress of the compared sample set. Next, the presence of cracks of the fabricated samples is correlated with the scalability of J-V curves obtained from the imaged devices. The diodes hosting cracks in the top-contact region, as the one indicated by the red arrow in fig 2.17, do not show a scaled J-V curve and the presence of cracks seems to reduce the yield of the fabricated devices. The cracks on the top contact that are accordingly present

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in the diode itself may be a favorable current path inducing high leakage and, consequently, a loss in the device scalability with contact area.

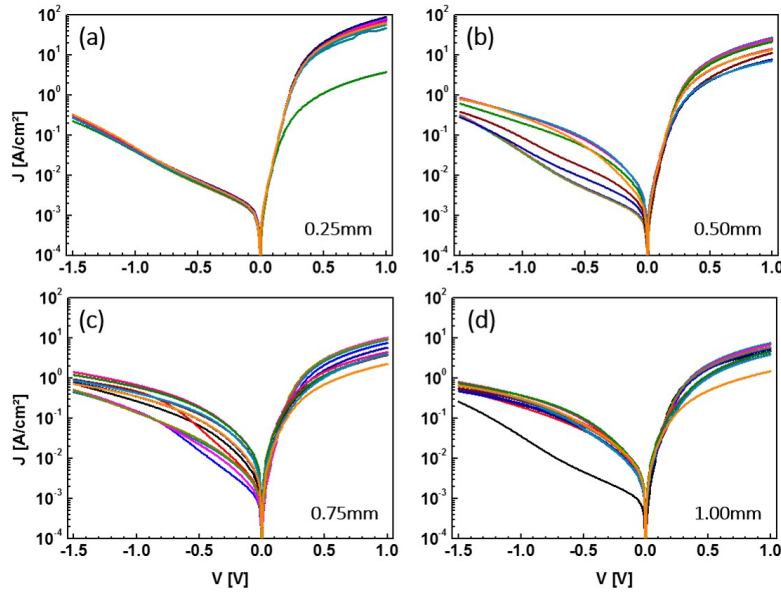


Figure 2.16: J-V data scattering of (a) 0.25 mm, (b) 0.50 mm, (c) 0.75 mm and (d) 1.00 mm devices fabricated on sample featuring lowest TDD and thickest Ge buffer.

In contrast, the J-V characteristics of crack-free devices scale with the contact area without exception. Thus, only the data derived from devices without cracks leads to a scalability of the J-V characteristics for diodes of different sizes (see Fig. 2.18). In comparison to samples featuring higher TDDs (Fig. 2.15(b-c)), the current scalability as function of device areas is observed for an even a wider voltage range. Therefore, only scalable devices will be used for further investigations.

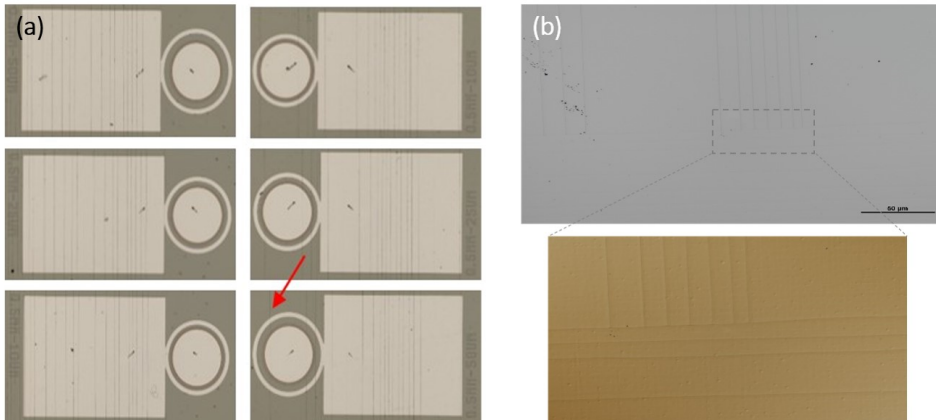


Figure 2.17: Optical microscopy images of W24 showing cracks on (a) 0.50 mm fabricated devices and (b) as-grown material.

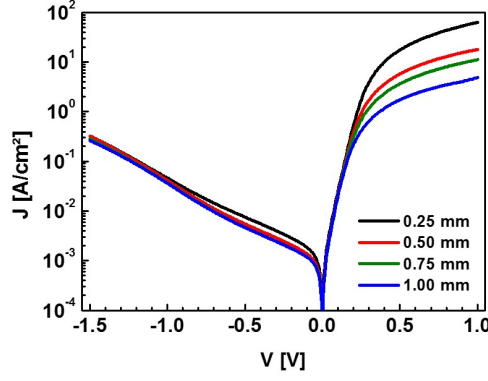


Figure 2.18: Scalability of J-V characteristics on diodes fabricated on sample W24.

There is a potential voltage drop due to the diode's series resistance (to which e.g. specific contact resistivities contribute) that must be considered in the measured voltage drop across the junction. In order to get rid of the unintentional voltage drop caused by R_S that is connected in series to the p-n⁺ junction diode as it is sketched in Fig. 2.19, the I-V data must be corrected. Therefore, the external R_S is determined following the modified ideal Shockley diode equation (eq. 1.68 of chapter 1) to decouple its effect from each measured I-V data. By means of $dV/d(\ln(I))$ vs I plots, R_S can be estimated from the slope and the intercept with the y-axis yields the ideality factor η of the diodes:

$$\frac{dV}{d(\ln I)} = R_S I + \frac{\eta k T}{q} \quad (2.2)$$

Fig. 2.20 shows the diode J-V characteristics of all three investigated samples featuring different TDDs where R_S is excluded. As suggested earlier, the deviation from current scalability with increasing bias can be attributed to the presence of an unintentional voltage drop due to R_S , since the J-V characteristics after data correction are fully scalable over the whole bias range. At positive voltages, the diode is biased in forward direction and, consequently, conducts current so that the whole voltage drop arises from the series resistance. Therefore, the diode J-V curves can be determined in just a small forward voltage range. However, exceeding a certain current density, that seems to depend on the amount of included TDs, the series resistance seems to dominate the voltage drop across the junction and no reasonable diode J-V data can be estimated (see Fig.2.20).

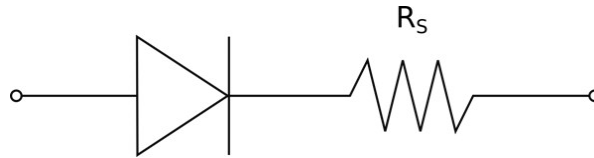


Figure 2.19: Equivalent circuit of p-n junction and series resistance R_S .

As will be discussed below, the diode leakage current increases with TDD and, therefore, the point at which R_S dominates the J-V characteristic starts at lower reverse biases for samples with higher TDD. Similarly, the voltage drop across the junction becomes dominated by R_S at lower applied biases of both signs when the diode size increases. Here, the leakage currents through TDs scales with the diode size, as bigger mesas contain more TDs in total than the

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smaller contacts leading to a domination of R_S at lower reverse biases.

For the following investigations of the TDD dependent I-V characteristics only data that is scalable and corrected for R_S is used.

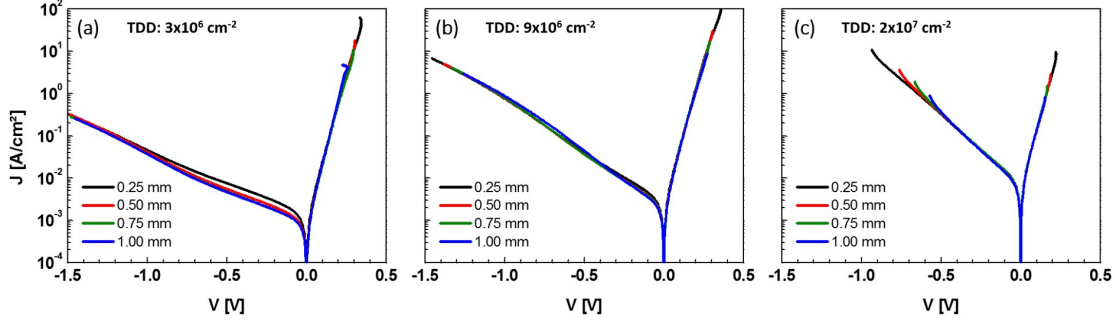


Figure 2.20: J-V characteristics corrected for R_S of generation 2 samples featuring Ge buffer thickness of (a) $4.40 \mu\text{m}$, (b) $2.30 \mu\text{m}$ and (c) $1.15 \mu\text{m}$.

Fig. 2.21 shows the J-V characteristics at 25°C of the three devices of generation 2 with identical geometries and mesa diameters of 0.25 mm , classified by their TDDs. The forward characteristics of the diodes do not represent a major difference, while in the reverse bias regime (V_R) an increase of more than two orders of magnitude in the current density can be observed for an increase in TDDs by just one order of magnitude.

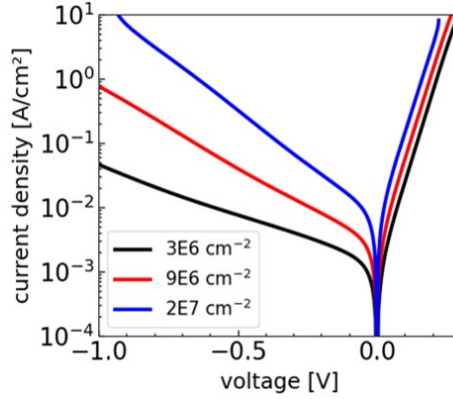


Figure 2.21: Comparison of J-V characteristics of investigated $p\text{-}n^+$ homojunctions featuring different TDDs [54].

The forward I-V characteristics are analyzed in order to extract the diode ideality factor η according to the ideal diode equation:

$$I = I_0 \left[\exp \frac{q(V - IR_S)}{\eta kT} \right] \quad (2.3)$$

Fig. 2.22 displays the TDD dependent ideality factor η evaluated from the slope of the linear square fit of the natural logarithm of the current for all investigated diode sizes. Averaging over all diodes the ideality factors of the studied $p\text{-}n$ junction diodes (Fig. 2.24(a)) are in the range of 1.17, 1.23, and 1.43 for samples of $3 \times 10^6 \text{ cm}^{-2}$, $9 \times 10^6 \text{ cm}^{-2}$, and $2 \times 10^7 \text{ cm}^{-2}$ TDD, respectively. The TDD dependent increase in η point towards a rising portion of the

recombination current component characterized by an ideality factor of 2, while an ideal diode with $\eta=1$ is dominated by the diffusion current.

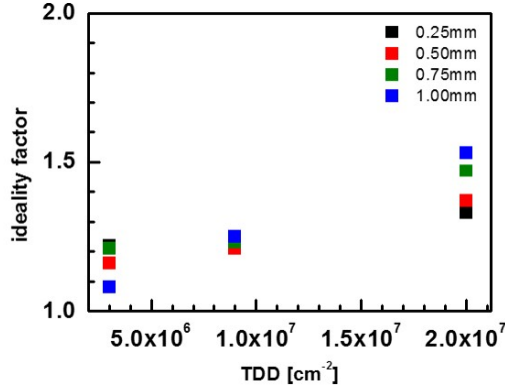


Figure 2.22: TDD dependent ideality factor for all investigated diode sizes.

The measured currents (I_{meas}) in the reverse bias regime ($I_R(V_R)$) consist of various leakage current components, i.e., an area (A)-proportional component J_A originating from the bulk of the diode, an edge component J_P originating from the diode periphery (P), a corner contribution J_C where C is the number of corners and a possible parasitic contribution I_{par} coming from the system and device itself [66]:

$$I_{meas} = I_R(V_R) = AJ_A + PJ_P + CJ_C + I_{par} \quad (2.4)$$

As a consequence of the circular diode design the leakage current contribution from corners can be omitted. Additionally, based on previous exclusion of R_S as well as the assumption that there are no further parasitics in the setup we used, the parasitic current contribution is also excluded. Thus, the leakage currents (I_{leak}) can be written as the sum of the contributing J_A and J_P and, therefore, eq. 2.4 reduces to:

$$I_{leak} = AJ_A + PJ_P \quad (2.5)$$

The separation of the geometrical current components is based on the scalable I-V measurements carried out on the available diodes featuring four different perimeter to area P/A ratios. The current components J_A and J_P were separated using a linear fit of I_{leak}/A vs P/A plots at certain reverse voltages in 0.1V steps for $|V| \geq 0.1V$ and 0.025 V steps for $|V| \leq 0.1V$. Here, the slope corresponds to J_P and the intercept with y-axis is attributed to J_A [66]. The estimated J_A and J_P contributions of the analyzed samples from generation 2 are presented in Fig. 2.23. The area current density (Fig. 2.23(a)) shows a clear dependence on the number of TDs, while the perimeter current density (Fig. 2.23(b)) is almost identical for the three samples featuring different TDDs. The almost constant peripheral leakage current, proving a high reproducibility of the fabricated devices, originates from the surface electron-hole pair generation at the diode perimeter. However, the increase in leakage current density is mainly caused by the area component compared to the perimeter one. Therefore, isolating the diode area current density provides a measure to extract the TDD related diode leakage current in the investigated intrinsic Si_{0.06}Ge_{0.94} layer.

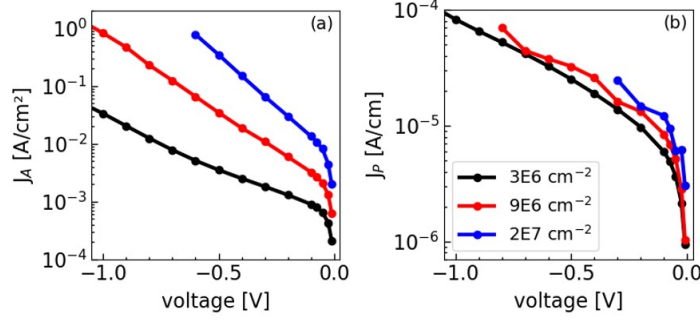


Figure 2.23: TDD dependent current densities vs applied reverse bias at 25°C for (a) area and (b) perimeter contribution [54].

The significant impact of TDD on the diode reverse leakage currents was previously simulated by considering shunt effects of threading dislocations in Si and Ge [67, 68]. Here, an additional shunt resistance parallel to the p-n junction diode is assumed as sketched in the inset of Fig. 2.24 [68]. The total shunt resistance R of the investigated 0.25 mm diodes was determined by the slope of the linear reverse region of the area current component [67]. Fig. 2.24 shows the TDD dependent resistance R (black data points) in a logarithmic scale ranging from $2.2 \times 10^{-6} \Omega$ to $7.4 \times 10^{-5} \Omega$ for the lowest and highest TDD investigated in this study, respectively. By means of the diode geometry and the corresponding TDD, the specific resistivity of an individual TD ρ_{TD} can be estimated [67, 68]. As indicated in Fig. 2.24 (blue data points), the specific resistivity per TD ρ_{TD} in intrinsic Si_{0.06}Ge_{0.94} appears in the range of $10^{-8} \Omega\text{cm}$, which is similar to values reported for ρ_{TD} in Si [68]. Such low specific resistivity points towards a confirmation of the assumption that TDs may act as parasitic shunt channels in rectifying devices by increasing the leakage currents and thus deteriorating the device performances. However, the specific resistivity per TD shows an enhancement of approximately 20% when increasing the TDD by almost one order of magnitude. This non-linear variation in ρ_{TD} with changing TDD indicates the presence of an additional impact on the conductivity of TD rather than just their density. A saturating agglomeration of other defects like metal contaminations or vacancies at the dislocation lines could influence their conductivity accordingly.

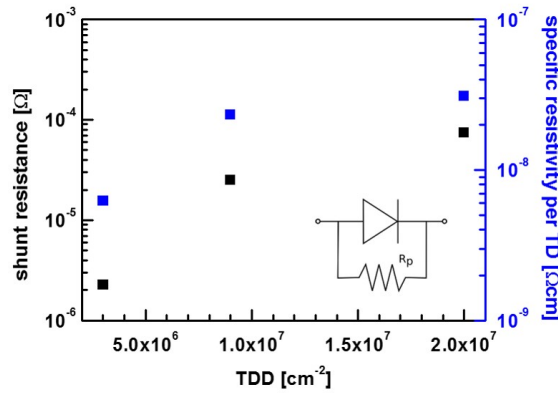


Figure 2.24: Calculated parallel shunt resistance as sketched in the inset of 0.25 mm diodes and specific resistivity per single TD.

The TDD dependence of the diode area leakage currents is investigated by plotting the estimated J_A versus TDD at every V_R up to a value of -0.6 V. According to Fig. 2.25 (a), the

J_A versus TDD plot reveals a stronger than linear dependence. The relationship between J_A and TDD was modeled using a power law [36]:

$$J_A \approx \alpha TDD^\beta \quad (2.6)$$

where β represents the fitted exponent of the power law (eq. 2.6) and α the pre-factor. Here, a super-linear increase of leakage currents with TDD is observed with $\beta(V_R)$ values always greater than 1. Fig. 2.25(b) shows the resulting exponent β as a function of reverse bias including the error bars caused by the fitting procedure. The super-linear dependence is different from what is observed in Si-rich Si_{1-x}Ge_x layers ($x < 0.3$), where a linear relation between leakage currents and TDDs has been reported [69]. Even when extrapolating the β values to zero applied bias it will be still greater than 1. Additionally, the increase in β with higher (V_R) suggests an electric field dependence of the leakage currents and, therefore, of the carrier generation, as will be discussed in the following. Similarly to pure Ge, the rather small bandgap of the studied Si_{0.06}Ge_{0.94} layers (0.67eV at 300K) can enhance tunnel processes of carriers through the bandgap in the presence of a strong electric field [70].

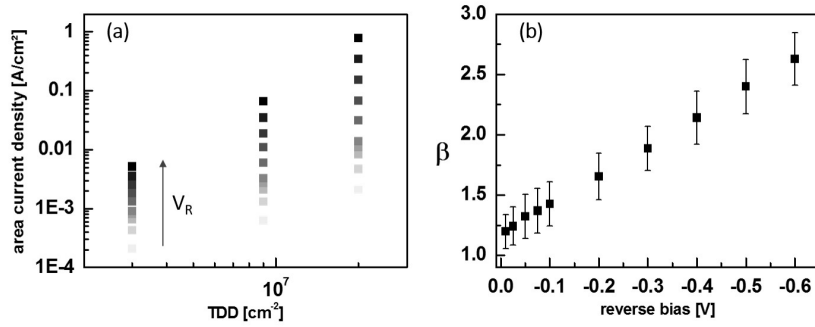


Figure 2.25: Super linear increase in J_A with TDD depending on V_R illustrated by (a) J_A vs TDD and (b) exponent β of the power law vs V_R plot.

The reverse area current density depends only on the diode area and, therefore, the included TDs, can be split up further into physical current components [71]. According to the Shockley-Read-Hall theory (see chapter 1.2.1) [15, 72], the reverse current of an abrupt one-sided p-n⁺ junction comprises a diffusion current (J_{diff}) and a generation current (J_{gen}) contribution caused by generation processes in the semiconductor neutral region, diffusing to the space charge region and inside the space charge region, respectively. Therefore, J_A can be written as [73, 74]:

$$J_A = J_{diff} + J_{gen} = \frac{qn_i^2 D}{N_{dop} L} + \frac{qn_i w_d}{\tau_g} \quad (2.7)$$

where q is the elementary charge and n_i the intrinsic carrier concentration. Here, the diffusion current depends on the doping density N_{dop} and the recombination lifetime τ_r , which is a function of the diffusion coefficient D and diffusion length L ($L \equiv \sqrt{D\tau_r}$ [18]), while the generation current depends on the depletion width w_d and the generation lifetime τ_g [75]. According to ref. [76], both physical current contributions can be extracted by plotting the current density as a function of the depletion depth ($J - w_d$) as is sketched in Fig. 2.26(a), since eq. 2.7 predicts a generation leakage current proportional to the depletion width [76,

77]. Here, the diffusion part is obtained from a linear extrapolation to the zero depletion width while the generation component is given by the slope [76]. Fig. 2.26(b) demonstrates the J_A versus w_d plot for the three investigated samples featuring different TDD. For each applied reverse bias, the corresponding J_A and w_d values are plotted, whereby w_d is measured by C-V measurements that are examined in more detail in section 3.4 of this chapter. Here, the increase of J_A is found to be stronger than the proportional relation between J_{gen} and depletion region width predicted by eq. 2.7. This super-linear increase in J_A with w_d also points towards a field enhancement of the leakage current [71, 78].

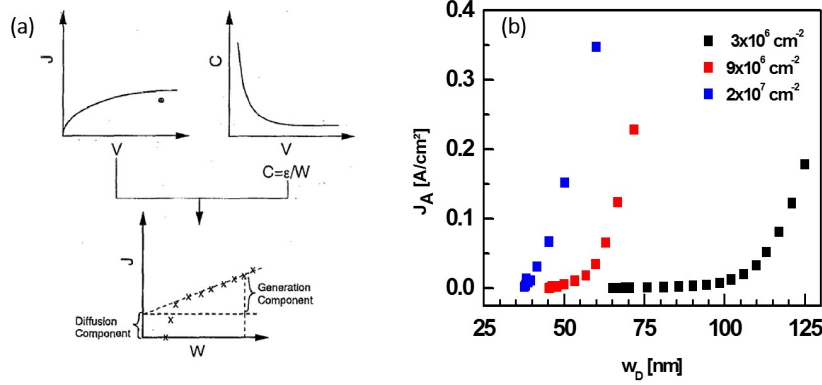


Figure 2.26: J-W plot as (a) schematic presentation of the method [76] and (b) measured rise in J_A with increasing w_d after [54].

Such electric field-enhanced generation rates Γ of charge carriers are considered to be important when the maximum electric field at the junction reaches values in the range of 10^5 - 10^6 V/cm [71]. It should be noted here that w_d extends from the top of the n^+ - into the i-Si_{0.06}Ge_{0.94} layer, which is only 150 nm apart from the defective SiGe/Ge heterointerface. Close to the diode junction interface, a positive charge density of 2×10^{17} , 5×10^{17} , and 7×10^{17} cm⁻³ for samples featuring TDD of 3×10^6 , 9×10^6 , and 2×10^7 cm⁻², respectively has been measured by C-V profiling (see section II.3.4) respectively. Based on the measured carrier densities, the initial maximum electric field F_{max} at zero applied bias is simulated using Comsol Multiphysics and is in the range of 105 V/cm promoting an electric field-enhanced generation. Here, F_{max} shows a duplication from approximately 1.5×10^5 to 3×10^5 V/cm in the range of TDDs investigated here. The higher TDDs seem to result in an increased electric field at the junction probably caused by a higher N_A and a narrower depletion width. This increase in the electric field and the narrowing of w_d can be responsible for an increase in the field dependent generation current contribution with increasing TDD and, therefore, the total diode leakage current (see Fig. 2.23(a)). In addition, such high electric fields play a key role in tunnel-related transport mechanisms like trap-assisted tunneling (TAT) or band-to-band (BTB) tunneling [79]. While the direct tunneling of free carriers from the top of the valence band to the bottom of the conduction band (BTB) is independent from defect levels, trap-assisted tunnel processes are based on deep defect states inside the band gap. The discussed modes of carrier transport processes are schematically shown in Fig. 2.27. Based on the TDD dependence of the electric field at the junction, BTB tunneling may also be influenced by the presence of TDs even if it does not depend explicitly on defect levels (E_T) [79]. Similar field enhanced tunnel mechanisms, such as TAT and BTB tunneling, have also been observed previously in Ge p-i-n photodetectors

[80], p⁺-n Ge junctions for MOSFETs [77], strained SiGe source/drain junctions [81] and Ge pFET junctions [82] and are related to the lower band gap of Ge-based materials compared to Si.

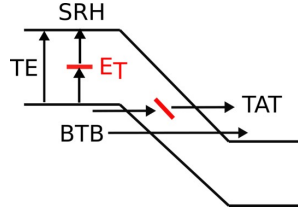


Figure 2.27: Schematic picture of carrier transport processes with and without a defect trap level E_T including thermal emission (TE), Shockley-Read-Hall generation (SRH), trap-assisted tunneling (TAT) and band-to-band tunneling (BTB).

As the area current density shows a stronger increase of the applied bias than predicted by the simple SRH generation mechanism, the distinction between the physical components becomes more complex. However, the area leakage current density J_A including field-enhanced generation mechanisms like TAT can be described by following the model of Hurkx [79], who introduces the position-dependent electric field enhancement factor $\Gamma(x)$ [81]:

$$J_A \approx q[1 + \Gamma(x)]U_{SRH}(x)w_d \quad (2.8)$$

The SRH generation rate U_{SRH} is characterized by deep traps in the depletion region and can be described by $U_{SRH} \approx qn_i/\tau_g$ [81]. The derivative of the area current density with respect to the depletion width dJ_A/dw_d is assumed to be a viable tool for a qualitative assessment of the TDD dependent generation leakage current in consideration of an electric field amplification. Fig. 2.28 (a) shows the dJ_A/dw_d plots for the three investigated samples, which differ in TDD versus the applied reverse bias that is proportional to the maximum electric field at the junction. The minimum of dJ_A/dw_d is associated with the lowest electric field at the junction and is therefore $\Gamma(x)$ considered to be minimal. Therefore, the estimated TDD dependent minima of dJ_A/dw_d are qualitatively compared and illustrated in Fig. 2.28 (b). With respect to the lowest TDD ($3 \times 10^6 \text{ cm}^{-2}$), the generation rates (dJ_A/dw_d) in the other two investigated samples are increased by factor 1.7 and 9.6 for TDD values growing by factor 3 ($9 \times 10^6 \text{ cm}^{-2}$) and 6.7 ($2 \times 10^7 \text{ cm}^{-2}$), respectively.

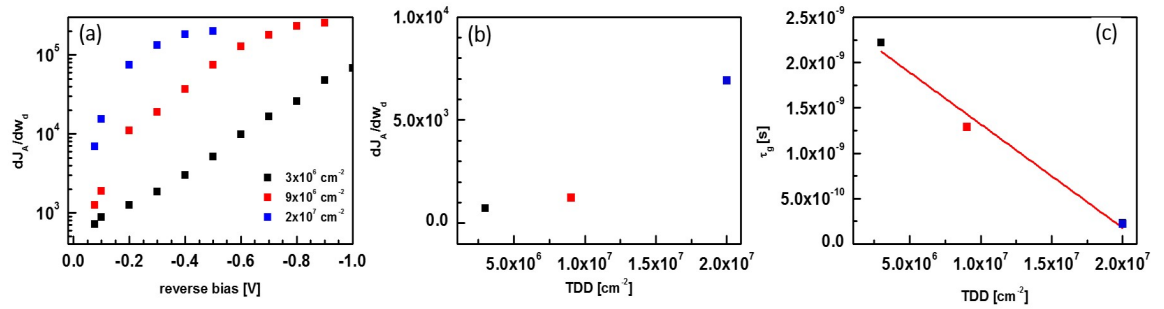


Figure 2.28: (a) dJ_A/dw_d plot, (b) TDD-dependent minimum of dJ_A/dw_d plot at lowest electric field and (c) corresponding generation lifetime.

By considering the simplified estimation procedure, a nearly linear dependence of the electric field independent leakage generation rate on TDD becomes apparent in the investigated samples. By applying eq. 2.8 and using the relation of $U_{SRH} \approx qn_i/\tau_g$, the generation lifetime τ_g can be estimated as follows, assuming the intrinsic carrier concentration of Ge to be $n_i = 2 \times 10^{13} \text{ cm}^{-3}$:

$$\tau_g \approx \frac{qn_i}{dJ_A/dw_d} \quad (2.9)$$

The calculated generation lifetimes are plotted in Fig. 2.28 (c) for the three different TDDs investigated in this work. As one might expect from the TDD dependent increase in leakage currents, lifetimes decrease with increasing TDD, confirming the degradation of the electrical quality of intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ heterostructures due to the presence of TD. Here, carrier lifetimes serve as a measure of electrical quality for semiconductor materials since they include the interaction of free carriers with defect related trapping and G-R centers. A linear fit of the three data points as indicated in Fig. 2.28 (c) enables the description of a relation between the generation lifetime τ_g and the threading dislocation density TDD in the investigated diodes:

$$\tau_g(TDD) \approx 2.4622 \cdot 10^{-9} - 1.1423 \cdot 10^{-16} TDD \quad (2.10)$$

From eq. 2.10 it becomes apparent that an optimal τ_g of 2.4622×10^{-9} s could be expected if the studied $\text{i-Si}_{0.06}\text{Ge}_{0.94}$ layer features no threading dislocations. As a guideline, TDDs in the range of 10^7 cm^{-2} may halve the generation lifetime in investigated devices, which results in a marked deterioration of the electrical quality of such heterostructures e.g. in terms of leakage currents as discussed above. If TDD can be tuned to the low 10^6 cm^{-2} range the impact on τ_g can be restricted to less than 10 percent. A further reduction in TDD would not have the same significant effect of improvement in electrical quality as the reduction from the $\geq 10^7 \text{ cm}^{-2}$ to 10^6 cm^{-2} range. Comparing with literature, one finds a big variation across the range of reported generation lifetimes for Ge substrates between 3×10^{-8} s and 5×10^{-4} s, depending on fabrication process and resistivity [83]. For relaxed Ge epi layers on Si, τ_g is stated as 1×10^{-6} s and 10^{-14} s for dislocation-free material and inside the dislocation core, respectively [48]. However, τ_g estimated in this work is averaged over the entire diode area, which may explain the value in between τ_g of dislocation-free Ge material and inside the dislocation core. In addition, the electric field is still non-negligible so that τ_g is reduced by TAT or other field-dependent generation mechanisms to a certain extent [48].

Although it might not be possible to estimate the recombination lifetime τ_r from the reverse diode characteristics in the investigated devices due to the influence of the electric field enhanced generation, τ_r can also be calculated from the forward current characteristics [84, 85]. Here, the forward current density J_F is extrapolated to zero bias J_{F0} , which is given as a first-order approximation for an abrupt $n^+ \text{-p}$ junction by [84]:

$$J_{F0} \approx q \sqrt{\frac{D_n n_i^2}{\tau_r N_A}} \quad (2.11)$$

Following the correction procedure described in ref. [84] for perimeter effects and the diode ideality, τ_r can be calculated in a more accurate way. Therefore, the area component J_{F0}^A of the forward current intercept J_{F0} is extracted in a similar way as for the geometrical leakage

current components by J_{F0} vs P/A plots. In addition, the forward current I_F can be assumed to consist of a recombination (I_{rec}) and diffusion component (I_{diff}), based on the SRH theory [84]:

$$I_F = I_{rec} + I_{diff} = I_{rec0} \exp \frac{qV}{2kT} + I_{diff0} \exp \frac{qV}{kT} \approx I_{F0} \exp \frac{qV}{nkT} \quad (2.12)$$

$$I_{rec} \approx I_{diff} \frac{n-1}{1-0.5n} \quad (2.13)$$

Differentiating eq. 2.12 with respect to the voltage leads to the ideality dependent ratio between I_{rec} and I_{diff} (eq. 2.13), from which the bulk diffusion component of the forward current intercept J_{F0}^{diff} can be extracted [84]:

$$J_{F0}^{diff} \approx \frac{0.5n}{1-0.5n} J_{F0}^A \quad (2.14)$$

Considering the ideality factors of the investigated diodes as discussed above and eq. 2.13, ratios between I_{rec} and I_{diff} are estimated to be 0.4, 0.6 and 1.5 for diodes featuring TDDs of 3×10^6 , 9×10^6 , and 2×10^7 cm⁻², respectively. A I_{rec}/I_{diff} ratio smaller than 1 points towards a diffusion-dominated forward current, as is the case for the two diodes with lower TDDs, while the recombination forward current is dominant for I_{rec}/I_{diff} ratios greater than 1, as observable for the diode with the highest TDD. The increase of the recombination component with increasing TDD and the dominance of the recombination current in diodes featuring TDDs of 2×10^7 cm⁻² could be related to a TDD-dependent rise of the existing trap density or to the increased electric field at the junction, especially at the low forward bias at which J_{F0} is estimated. Based on the TDD dependent increase in electric fields present at the junction that is related to the increased carrier density calculated from C-V characteristics, as has already been observed in the analysis of the reverse diode characteristics, a combination of both the increase in trap level density and electric field with TDD may be responsible for a growing portion of recombination current. Using the corrected forward current intercept J_{F0}^{diff} , values for τ_r are estimated based on eq. 1.11 assuming $D_n \approx 100$ cm²s⁻¹ and $n_i = 2 \times 10^{13}$ cm⁻³ of Ge, and listed in table 2.2. Using the above estimated generation lifetime τ_g from the reverse I-V characteristic, the energy level E_T of included trapping centers can be calculated from the relationship between τ_g and τ_r according to [85]:

$$\tau_g \approx \tau_r \exp \frac{|E_T - E_i|}{kT} \quad (2.15)$$

The generation lifetime as well as the estimated defect energy level E_T are also listed in table 2.2. As can be seen from table 2.2, the recombination lifetime decreases faster with TDD than the generation lifetime resulting in an increasing ratio of τ_g/τ_r . Therefore, the defect level energy shows a TDD dependence, too, as it is located almost at mid-gap ($E_i \pm 0.04eV$) for the lowest TDD and shifts towards the band edges with increasing number of TDs. As described in chapter 1, the interaction of free carriers with both band edges is most effective if the defect level is located at E_i , as the defect levels are closer to one band edge, the interaction between them is multiplied in contrast to the interaction with the opposite band edge. Here, the TD-related G-R centers that clearly increase the diode leakage currents and that are determined by the ratio of lifetimes are located at $E_V + 0.29eV$, $E_V + 0.22eV$ and $E_V + 0.17eV$

2. Electrical activity of threading dislocations in Ge-rich SiGe heterostructures

or $E_C - 0.29\text{eV}$, $E_C - 0.22\text{eV}$ and $E_C - 0.17\text{ eV}$ for samples featuring TDDs of 3×10^6 , 9×10^6 , and $2 \times 10^7\text{ cm}^{-2}$, respectively. Assuming the TDs related G-R centers act as acceptor-like states, which may trap valence band electrons of the nominal intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ and leaving an excess of holes behind, this could be a possible explanation for the found p-type conductivity. The increase in p-type conductivity (estimated by C-V measurements) could be related to a rising number of acceptor-like states with increasing TDD that consequently trap more electrons. The electrostatic repulsion between trapped carriers may hinder a linear occupation behavior of these acceptor-like states resulting in a non-linear relationship between p-type conductivity as well as leakage current density and TDD, as is shown above and in section 2.3.4. However, the shift in E_T to the band edges with increasing TDD could point to an occupation dependency of these defect states with the number of TDs as it determines the energy position in the band gap [10].

TDD	τ_g	τ_r	E_T
$3 \times 10^6\text{ cm}^{-2}$	$2.2 \times 10^{-9}\text{ s}$	$4.4 \times 10^{-10}\text{ s}$	$E_i \pm 0.04\text{ eV}$
$9 \times 10^6\text{ cm}^{-2}$	$1.3 \times 10^{-9}\text{ s}$	$1.6 \times 10^{-11}\text{ s}$	$E_i \pm 0.11\text{ eV}$
$2 \times 10^7\text{ cm}^{-2}$	$2.3 \times 10^{-10}\text{ s}$	$2.63 \times 10^{-13}\text{ s}$	$E_i \pm 0.16\text{ eV}$

Table 2.2: Estimated values of generation lifetime τ_g , recombination lifetime τ_r and energy level E_T with respect to $E_i \approx 0.33\text{ eV}$.

Keeping in mind the three mechanisms of how dislocations may affect the electronic structure of group IV semiconductor materials (see section 1.2.2), the defect levels found to be at mid-gap position tend to indicate the presence of deep G-R centers rather than shallow trap states pulled down from the band edges due to strain fields. From the estimated value of E_T it is not apparent if the TD related defect levels are sharp or consist of a narrow band of states. To distinguish between them and to perform a more appropriate analysis of the TD related defect levels, DLTS is to be the preferred measurement (see section 2.4).

It should be noted here that the evaluation of carrier lifetimes by I-V characteristic is clearly influenced by the presence of electric-field enhanced generation processes. Additionally, an influence of the lifetimes by attracted minority carriers on charged dislocation lines cannot be excluded. However, the defect level energy E_T is calculated from the ratio between generation and recombination lifetime and, therefore, is not dependent on individual values for τ_g and τ_r . Assuming a comparable impact of the electric field at small reverse and small forward biases (close to the junction interface) where both carrier lifetimes are estimated, the values for E_T in table 2.2 are reasonable assumptions for TD related defect level positions inside the $\text{Si}_{0.06}\text{Ge}_{0.94}$ bandgap.

2.3.3 Activation energies of TDD dependent leakage currents

As already discussed in the previous section, the strongest impact of TDD on the diode I-V characteristics is caused by dislocations. In order to assess the dominant leakage current mechanism along TDs in i- $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructures, the temperature-dependent reverse J-V diode characteristics were measured at temperatures ranging from 210 K to 475 K and are represented in Fig. 2.29. The change in temperature of the J-V curves is visualized by colors ranging from blue (210 K) to red (475 K). All measured curves are corrected by the series resistance R_S which is determined for each separate temperature. As shown in Fig. 2.29, the largest temperature dependence of the leakage current is present for small reverse biases and diminishes strongly with the higher applied reverse bias, pointing to the action of rather weak temperature-dependent mechanisms, such as tunneling of charge carriers at high electric fields ($|V_R| \gg 0$).

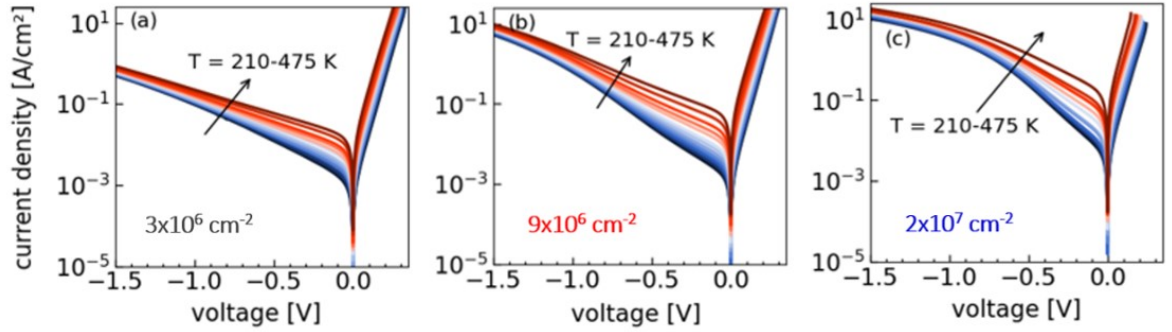


Figure 2.29: Temperature-dependent J-V characteristics ranging from 210 K to 475 K of studied samples of generation 2 featuring TDDs of (a) $3 \times 10^6 \text{ cm}^{-2}$, (b) $9 \times 10^6 \text{ cm}^{-2}$ and (c) $2 \times 10^7 \text{ cm}^{-2}$ after [54].

The activation energy E_A of the TD-dependent diode leakage currents can be estimated by applying an Arrhenius plot at different values of V_R [70]. Here, a graphical representation of the inverse temperature dependence of the natural logarithm of J_R enables the calculation of E_A from its slope. It should be noted that the predictable activation energies E_A of the leakage current are a product of all contributing transport mechanisms. Fig. 2.30 shows the $\ln(J_R)$ vs $1/kT$ plots for different reverse biases in 0.025 V steps for $|V| \leq 0.1$ V and 0.1 V steps for $|V| \geq 0.1$ V. For all three samples, three similar temperature regimes are identified: 1) $T > 100^\circ\text{C}$, 2) $25^\circ\text{C} < T < 100^\circ\text{C}$ and 3) $T < 25^\circ\text{C}$, which are characterized by different slopes of the semi-logarithmic plot as indicated in Fig. 2.30.

1) The estimated activation energies E_A for temperatures above 100°C are plotted in Fig. 2.31(a) and are in the range of approximately half the $\text{Si}_{0.06}\text{Ge}_{0.94}$ bandgap ($E_g/2 \approx 0.33$ eV) at low V_R for all three samples studied. Leakage current activation energies in the middle of the bandgap suggest a carrier generation via deep traps according to the SRH mechanism as the second term of eq. (2.7) shows a dependency of the SRH generation rate on n_i . Consequently, the thermal activation energy of a SRH generation corresponds to half the bandgap energy E_g according to:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \quad (2.16)$$

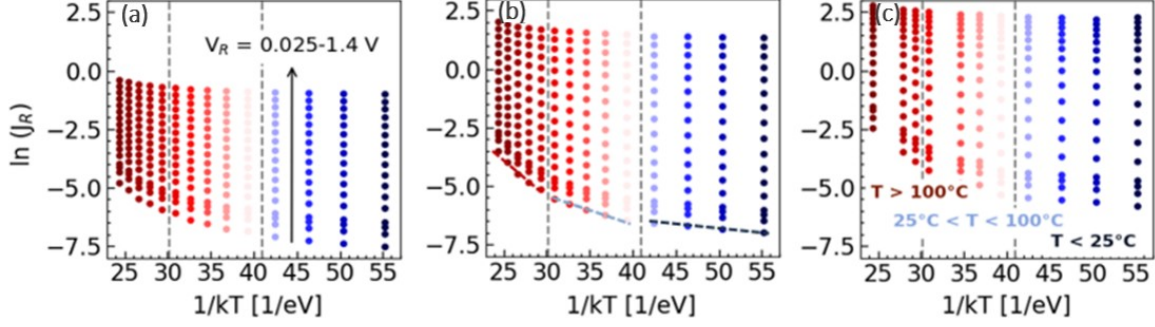


Figure 2.30: Arrhenius plots of reverse current densities at varying V_R of generation 2 samples featuring TDDs of (a) $3 \times 10^6 \text{ cm}^{-2}$, (b) $9 \times 10^6 \text{ cm}^{-2}$ and (c) $2 \times 10^7 \text{ cm}^{-2}$ after [54].

The presence of these deep traps near mid-gap may be related to the presence of TDs, as such traps have been found in plastically deformed or heteroepitaxial n-type Ge layers, where they are attributed to the presence of point defect clusters trapped in the strain field of TDs [48]. Since no implantation processes were carried out during sample preparation, one can argue that these point defects should be related to growth induced defects such as vacancy complexes, which have been reported to show a strong recombination activity in Si when dislocations are present in the material [86, 87]. It should also be noted that for the sample featuring the minimal TDD, the E_A is slightly lower than those of the other two samples with higher TDDs, pointing towards a reduced influence of the SRH generation mechanism. This is in line with the interpretation above, since at lower TDDs the emergence of point defect clusters in the strain field of TDs is reduced. For applied reverse voltages less than -1.0 V, the estimated E_A are below 0.1 eV suggesting BTB tunneling as the dominant leakage contribution in this region probably caused by an increasing electric field present at the probed junction. High electric fields may increase the corresponding band bending and/or lower the barrier for carrier generation through different field-assisted mechanisms, which will result in an enhanced tunneling current [80, 81]. The reduction of E_A with an increasing applied bias is found in all devices (see Fig. 2.31).

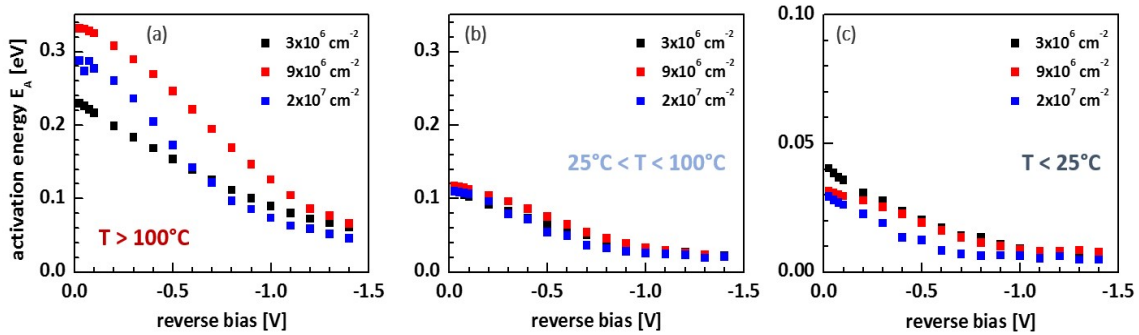


Figure 2.31: Associated E_A for the three defined temperature ranges of generation 2 samples featuring (a) $3 \times 10^6 \text{ cm}^{-2}$, (b) $9 \times 10^6 \text{ cm}^{-2}$ and (c) $2 \times 10^7 \text{ cm}^{-2}$ in dependence of the applied bias after [54].

By reducing the temperature, a decrease in E_A becomes apparent from Fig. 2.31(b-c), which indicates a major contribution of field dependent generation mechanisms like TAT in this material. For TAT, the SRH generation is increased by the field enhancement factor, which in

turn decreases exponentially with rising temperature [70]. It has previously been argued that TAT becomes the dominant mechanism of leakage currents for activation energies between $E_g/2$ and 0.1 eV in Ge based junctions, which are similar to the devices investigated here [70].

2) In the intermediate temperature range $25^\circ\text{C} < T < 100^\circ\text{C}$, E_A is similarly close to 0.1 eV at low V_R in all three samples and, therefore, it can be concluded that TAT is the dominant type of transport here. The tunneling via traps may become possible by the defect centers induced in the structures during the relaxed heteroepitaxial growth and the high electric fields present at the homojunction.

3) For temperatures below 25°C , the estimated E_A are far below 0.1 eV, and thus likely related to BTB tunneling without interaction with any defect levels as indicated in Fig. 2.27. The occurrence of BTB tunneling is similar to results obtained from samples with higher dislocation densities [70, 74]. As suggested in Ref. [28], a possible local reduction of the bandgap energy due to the strain field around a TD may lead to an enhanced BTB tunneling. Additionally, high strain fields around the TDs may have a significant impact on local bandgap narrowing, as it has been reported for Si-rich SiGe layers [81] that will encourage tunneling.

2.3.4 Room temperature C-V characteristics

In this section capacitance-voltage (C-V) measurements have been used to assess the defect-induced carrier concentration. All C-V measurements were performed on the generation 2 sample set described in section 2.3.1. In order to carry out reliable capacitance measurements, the potential influence of the contacts on the measured capacitance is evaluated. Therefore, it is assumed that the measured capacitance C_{meas} consists of the capacitance coming from the diode itself C_{diode} and possible parasitic capacitances through the contacts $C_{contact}$ that are connected in series according to:

$$\frac{1}{C_{measured}} = \frac{1}{C_{diode}} + \frac{1}{C_{topcontact}} + \frac{1}{C_{bottomcontact}} \quad (2.17)$$

Fig. 2.32(a) presents the corresponding test procedures to determine the real diode capacitance. In panel (b) of Fig. 2.32, the observed capacitances on sample W22 (medium TDD) in the common measuring arrangement C_{meas} and for only the top C_{top} and bottom contact C_{bottom} are plotted. By rearranging eq. 2.17, C_{diode} can be estimated and is compared with the measured capacitance in Fig. 2.32(c). The conformity of C_{meas} and C_{diode} makes a data correction for parasitic capacitances caused by the contacts unnecessary.

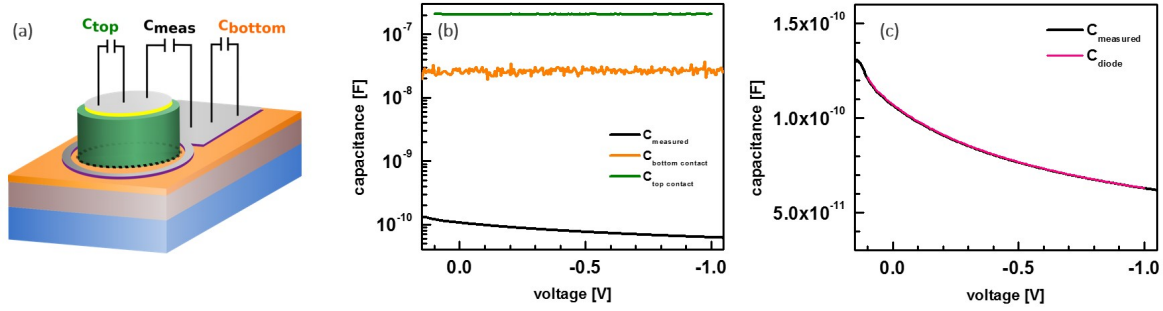


Figure 2.32: Influence of parasitic capacitances coming from the contacts, (a) sketch of measurement procedure, (b) measured capacitances and (c) comparison of measured and diode capacitance.

In addition, values of the impedance Z and its phase angle θ , from which the capacitive reactance X_C is extracted (see chapter 1.4.2) are considered to check the influence of the leakage currents observed in the paragraphs above. The leakage can influence the equivalent resistance R and may overwhelm the capacitive reactance. The behavior of the studied n^+ - p junction as ideal capacitor can be reviewed with the quality factor Q , the ratio between the reactance of the capacitor X_C and its series resistance R_s . Therefore, Q is given at the operating frequency ω by:

$$Q = \frac{\text{Reactance}}{\text{Resistance}} = \frac{X_C}{R_s} = \frac{1}{\omega C_s R_s} \quad (2.18)$$

As generally applies, Q values above 10 are reasonable ratios between X_C and R for a reliable capacitance measurement. The quality factors as functions of TDD are shown in Fig. 2.33. Their absolute values decrease with TDD. The voltage regime in which the ratio between resistance and capacitive reactance is reasonable for capacitance measurements decreases also with TDD, which is related to the increasing leakage through TDs observed in paragraph 3.2 of this chapter. However, diodes featuring the highest TDD of $2 \times 10^7 \text{ cm}^{-2}$ have a maximum Q factor of 7.6 that implies a limit of leakage and, therefore amount of TDD to measure reasonable capacitances in the investigated n^+ - p junction diodes. Similar to the Q factor, the recorded amplitude and phase values displayed an ideal capacitor behavior with declining amplitude and an angle of almost -90° up to a certain bias. It can be added here that no parasitic impedance caused by the device or system is observed.

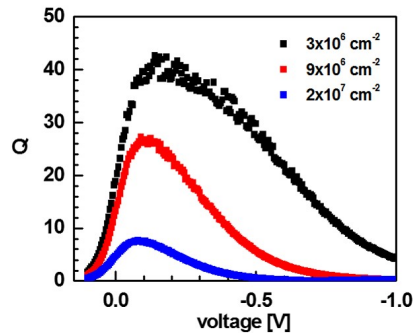


Figure 2.33: TDD dependent quality factor Q

In C-V measurements, high leakage currents can be treated as lossy capacitors that are represented by a capacitance C_p and a high shunt resistance R_p connected in parallel. Both extractable capacitances, C_s and C_p are compared in Fig. 2.34 for all three samples featuring different TDD. As already indicated by the Q factor, C_s and C_p are only similar in a limited voltage regime that shrinks with increasing TDD. Nevertheless, parallel representation of the R_C circuit shows reasonable capacitance values over a broader voltage range than the series configuration, especially for samples having the highest TDD of $2 \times 10^7 \text{ cm}^{-2}$ and leakage (Fig. 2.34(c)). Therefore, the system integrated parallel circuit model is used here to evaluate the capacitance of the samples in the bias regime where $Q = \omega C_p R_p \geq 10$ excluding devices featuring highest TDD, here the small bias regime with maximum Q values is considered.

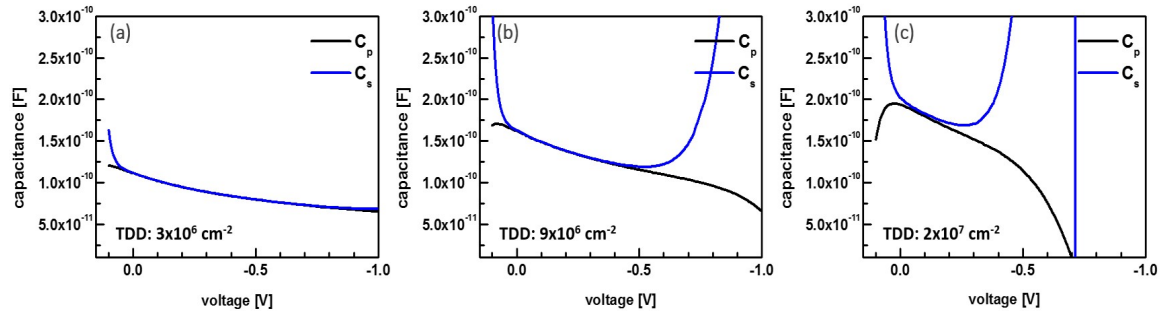


Figure 2.34: Comparison of diode capacitance measured in series or parallel configuration of samples featuring (a) $3 \times 10^6 \text{ cm}^{-2}$, (b) $9 \times 10^6 \text{ cm}^{-2}$ and (c) $2 \times 10^7 \text{ cm}^{-2}$.

In addition, the frequency dependence of the capacitance is evaluated in order to ensure the dominance of X_C against a potential series resistance. Since X_C is a frequency dependent quantity in contrast to R , the measured capacitance (dominating X_C) should remain constant when changing the measurement frequency. Indeed, the C-V characteristics are identical at different measurement frequencies ranging from 10 kHz - 1 MHz up to a certain reverse bias (see fig 2.35) excluding the impact of an additional series resistance. The reverse voltage at which the capacitance becomes inhomogeneous can be correlated to the voltage where a change in voltage drop was observed in J-V measurements highlighted in section 2.3.2.

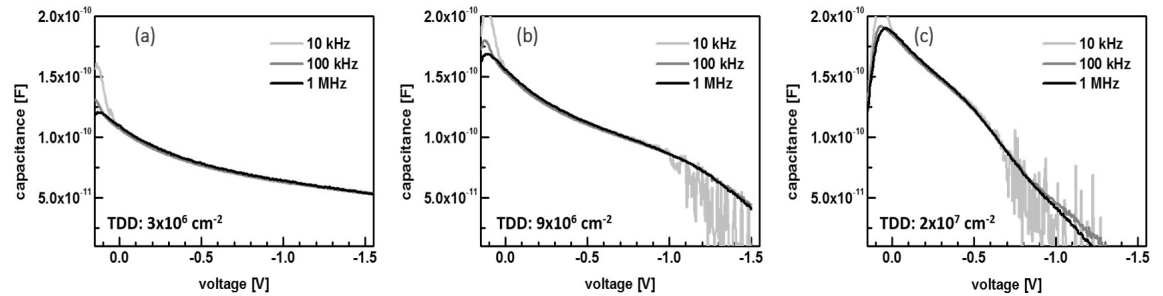


Figure 2.35: Frequency dependent C-V measurements of samples featuring (a) $3 \times 10^6 \text{ cm}^{-2}$, (b) $9 \times 10^6 \text{ cm}^{-2}$ and (c) $2 \times 10^7 \text{ cm}^{-2}$.

Finally, the doping density is estimated by means of C-V analyses, using a 1 MHz ac voltage frequency with 20 mV modulation amplitude. Here, the capacitance of the reverse-biased

junction, which is considered as a parallel plate capacitor is given by [3]:

$$C = \frac{A\epsilon_0\epsilon_s}{w_d(x)} \quad (2.19)$$

The corresponding doping density of p-type material $N_A(x)$ is obtained by the slope ($d(1/C^2)/dV$) of a $1/C^2$ -V plot as represented in Fig. 2.36(a) according to [3]:

$$N_A(x) = \frac{2}{q\epsilon_0\epsilon_s A^2 \frac{d(1/C^2)}{dV}} \quad (2.20)$$

Fig 2.36(b) shows the extracted doping concentration profile and corresponding depletion depths w_d . The large scattering of $N_A(x)$ values (see Fig. 2.36(b)) can be explained by the fact that the slope of the $1/C^2$ -V plot is estimated numerically for each data point. If the slope is estimated graphically by a linear fit of the $1/C^2$ plot, a constant doping concentration can be estimated in the reasonable bias regime indicated by corresponding lines in Fig. 2.36(b). It is recalled here that the depletion region extends into the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer starting from the buried p-n⁺ heterojunction that is at 150 nm distance from the defective heterointerface between the Ge buffer and the $\text{Si}_{0.06}\text{Ge}_{0.94}$ epi layer featuring a network of misfit dislocations.

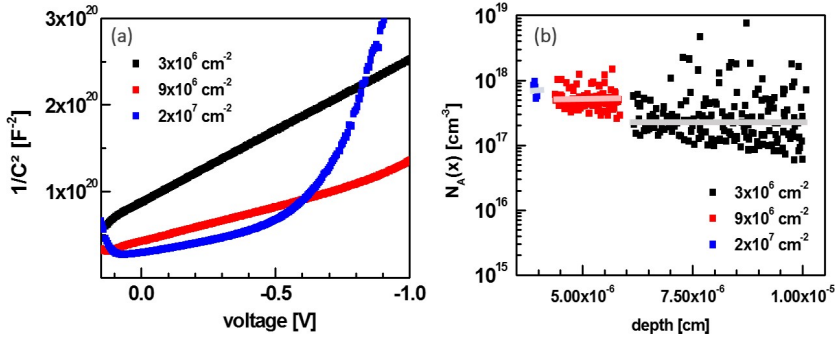


Figure 2.36: Reliable C-V measurements yields the (a) corresponding $1/C^2$ -V plots that are used to estimate (c) the carrier concentration in the reasonable voltage range.

From the intercept of the $1/C^2$ plot with the voltage axis, the built-in potential V_{bi} of the studied n⁺-p junction diodes can be estimated by a linear curve fit in the corresponding bias regimes [3]. The TDD dependent built-in potentials are also shown in table 2.3. The obtained values of V_{bi} at + 0.53 V are in line with reported built-in potentials of approximately + 0.55 V for one-sided abrupt n⁺-p junctions featuring similar background doping densities in Ge [18]. Here, V_{bi} increases by 0.5 V when the background doping of the lightly impurity doped p-side increases from 10^{17} cm^{-3} to 10^{18} cm^{-3} [18]. Such an increase could not be observed in the studied devices. The less optimal capacitance measurement of the sample featuring the highest TDD marked by the lower Q factor may result in a greater error in estimating V_{bi} , which could explain the missing trend.

TDD	V_{bi}	$N(x)$	w_d
$3 \times 10^6 \text{ cm}^{-2}$	0.525 V	$2.21 \times 10^{17} \text{ cm}^{-3}$	60 - 100 nm
$9 \times 10^6 \text{ cm}^{-2}$	0.529 V	$4.56 \times 10^{17} \text{ cm}^{-3}$	45 - 60 nm
$2 \times 10^7 \text{ cm}^{-2}$	0.514 V	$6.08 \times 10^{17} \text{ cm}^{-3}$	40 nm

Table 2.3: Estimated values of carrier concentration $N(x)$ in the certain depletion depth range w_d .

For the lowest TDD sample a constant doping density of $2.21 \times 10^{17} \text{ cm}^{-3}$ is estimated up to a depth of 100 nm from the p-n⁺ junction. The doping concentration increases up to $4.56 \times 10^{17} \text{ cm}^{-3}$ and $6.08 \times 10^{17} \text{ cm}^{-3}$ for samples having TDD of $9 \times 10^6 \text{ cm}^{-2}$ and $2 \times 10^7 \text{ cm}^{-2}$ respectively, in the accessible region of 60 nm and 40 nm close to the interface. These high doping densities close to the Si_{0.06}Ge_{0.94} junction interface may be related to the network of threading as well as misfit dislocations that are present in the neighborhood of the bottom interface. By increasing the Ge buffer thickness and consequently lowering the TDD, the extent of such a defective interface seems to be reduced, as reflected by the lower doping density. Due to the high amount of doping close to the interface and the increasing leakage currents at higher reverse voltages, the depth of information is limited to the bottom interface of the intrinsic Si_{0.06}Ge_{0.94} layer. It will be of paramount interest to characterize the complete intrinsic Si_{0.06}Ge_{0.94} layer towards the sample free surface, which will be the starting point for further layer integration like superlattices for THz lasing devices [42] or device processing steps to fabricate Ge-based MOSFETs [7]. From Hall-effect measurements it is observed that the doping density decreases in the upper part of the intrinsic Si_{0.06}Ge_{0.94} layer, possibly caused by dislocation annihilation at the initial step of layer growth [56].

The limited range in which reliable capacitances can be measured prevents a further analysis by DLTS in order to evaluate properties of the included defect states caused by the high leakage currents in the studied n⁺-p junction diodes.

2.4 TD related defect states in $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ MOS capacitors

To investigate the electrical active defect states related to TDs in Ge-rich SiGe heterostructures, capacitance-based measurements are beneficial because all charges are considered. As discussed in paragraph 3.4 of the previous section, the fabricated n^+ -p junction diodes are not appropriate for advanced capacitance measurements like DLTS because of high leakage currents present in the investigated devices. In order to overcome these high leakage currents, MOS capacitor devices are designed to allow for high quality capacitance measurements that are mandatory for a DLTS study. The grown $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ MOS structures are sketched in Fig. 2.37. Again, the heterostructures are grown on standard Czochralski Si(001) wafers that are boron (B)-doped. The medium Ge buffer thickness of $1.15 \mu\text{m}$ is chosen resulting in a TDD of $2 \times 10^7 \text{ cm}^{-2}$ in the subsequent $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer, while keeping their thickness ($1.5 \mu\text{m}$) and degree of relaxation (106 %) constant. The growth procedure of the heterostructures is as outlined in section 2.2. In addition, a thick silicon oxide (SiO_2) layer is deposited on top of the intrinsic SiGe/Ge buffer as dielectric in the studied MOS capacitors. The increased oxide thickness compared to common MOS transistor designs ($5\text{-}10 \mu\text{m}$) serves as barrier for possible leakage currents through the oxide as will be discussed below. The native oxide on the $\text{Si}_{0.06}\text{Ge}_{0.94}$ surface is removed by a dip in diluted hydrofluoric acid (HF), which is simultaneously the starting point for the oxide deposition.

In this subsection, the fabrication of the investigated MOS capacitors is described as well as its eligibility for capacitance-based measurements. Based on this, the evaluation of the defect-related effective carrier concentration in the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer is revealed by C-V measurements and the properties of the corresponding defect states are investigated by DLTS.

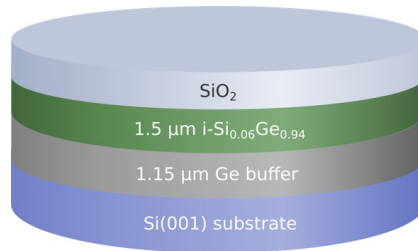


Figure 2.37: Sketch of the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures including the SiO_2 layer used for electrical characterization.

I developed the device design. The investigated samples were grown by my colleagues O. Skibitzki, Y. Yamamoto and M. Lisker in IHPs 200 mm pilot line. I fabricated the metal contacts on samples of generation 3, performed the measurements and analyzed the data. Some of the results of this section have been published in [88].

2.4.1 Device fabrication

In order to create MOS capacitor devices, two approaches are applied, facing two types of silicon oxides as dielectric medium, fabricated in different ways. The first set of MOS capacitors (generation 3) features a 50 nm thick undoped silicon glass (USG), which is deposited by sub atmospheric (SA) chemical vapor deposition using tetraethylorthosilicate (TEOS) as precursor. In addition, a standard Si substrate with a resistivity of 5-22 Ωcm is used for the heteroepitaxy. Subsequently, 20 nm thick Ni contacts were evaporated through a shadow mask on top of the SiO_2 layer in an Edwards Auto 306 vacuum metallization chamber by resistance evaporation resulting in gate areas of $A = 4.07 \times 10^{-3} \text{ cm}^2$. Here, a Ni wire was placed into a tungsten spiral that was heated by passing a large current through it. It followed a deposition of a 150 nm Al by sputtering via argon plasma using a power of 300 W to protect the Ni contact during the measurements.

The second set of MOS capacitors, called generation 4, consists of a 60 nm thick SiO_2 deposited by high density plasma chemical vapor deposition (HDP-CVD) at 300 $^\circ\text{C}$ using an Applied Materials Centura cluster tool. Furthermore, a low resistivity Si substrate of 0.008-0.012 Ωcm was applied in order to minimize the series resistance R_S in the MOS configuration to ensure high quality factors Q providing the basis for HF-capacitance measurements with adequate accuracy. As top metal gate contact a 500 nm thick Al layer was sputtered at 2 kW on top of the gate dielectric in IHPs cleanroom, that have an area of $A = 8.20 \times 10^{-3} \text{ cm}^2$. Table 4 displays the investigated set of samples including the corresponding substrate doping, Ge buffer thickness, TDD and applied SiO_2 .

generation	Si substrate	Ge buffer thickness	TDD	SiO_2
3	5-22 Ωcm	1.15 μm	$2 \times 10^7 \text{ cm}^{-2}$	50 nm SA-USG
4	0.008-0.012 Ωcm	1.15 μm	$2 \times 10^7 \text{ cm}^{-2}$	60 nm HDP-CVD

Table 2.4: MOS sample sets called generation 3 and 4.

In order to provide a better contact to the Si backside, the native oxide layer is scratched and an indium-gallium (InGa) eutectic solution is applied to form a good ohmic contact. The final device structure and the measurement arrangement is sketched in Fig. 2.38.

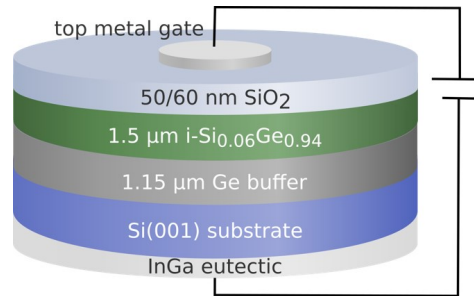


Figure 2.38: Sketch of the fabricated MOS capacitors including the measurement configuration.

In contrast to the studied n^+ -p junction diodes, here the whole heterostructure can be probed from top to the bottom. The advantage is that the space charge region will extend from

the oxide interface into the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer enabling an investigation of the entire epi-film thickness. Additionally, this measurement arrangement allows to also probe the Ge buffer by choosing the appropriate bias regime. Moreover, no implantation procedure is applied during growth so that residual background doping due to dopant atoms commonly used during fabrication can be excluded.

2.4.2 MOS capacitor ideality

First of all, the ideality of the fabricated MOS capacitors is the basis for studying the TD related defect states. A MOS capacitor is essentially determined by the serial connection between C_{sc} and C_{ox} . The semiconductor capacitance C_{sc} is determined by charges in the semiconductor material according to eq. 1.94 of the introduction chapter, also including the defect-dependent bulk trapped charges Q_{bt} . In contrast, the oxide capacitance C_{ox} depends on the oxide quality involving defect charges inside the oxide and near the oxide-semiconductor interface Q_{ox} as illustrated by eq. 1.89 of chapter 1. Although, the oxide characteristic is not necessarily required to investigate trapped charges inside the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ heterostructures caused by threading dislocations, oxide charges will influence the C-V characteristics as they contribute to the total gate voltage drop in the MOS system.

To provide a better understanding, the influence of fixed oxide charges Q_f and interface trapped charges Q_{it} on ideal p-type MOS C-V curves (solid line) will be briefly discussed and is illustrated in Fig. 2.39. If positive fixed charges are present in the oxide a shift to negative bias is a common observation in C-V curves as indicated in Fig. 2.39(a) [18]. Here, a lot of immobile positive charges are located close to the oxide-semiconductor interface, which can probably be attributed to structural defects in the applied oxide. Interface trapped charges cause a flattening of the slope of the C-V curves in the depletion range as shown in Fig. 2.39(b). The charges at the oxide-semiconductor interface needs to be recharged before the semiconductor can be depleted, so that Q_{it} forces an additional voltage for similar portion of depletion in the semiconductor, which is expressed by a stretch-out of the capacitance along the voltage axis [18].

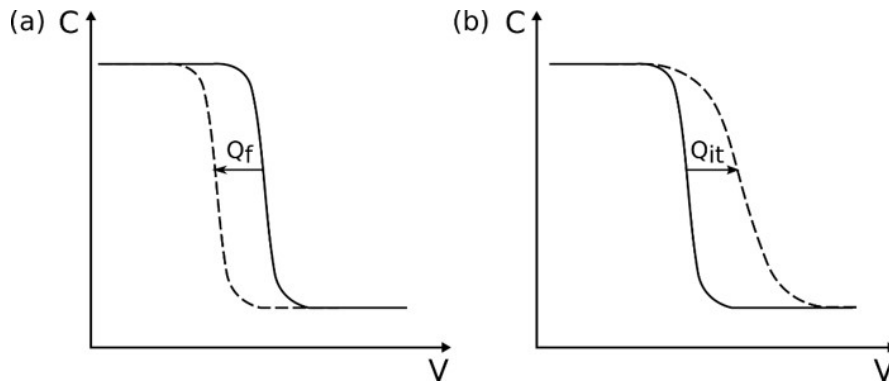


Figure 2.39: Influence of (a) fixed oxide charges Q_f and (b) interface trapped charges Q_{it} on an ideal MOS C-V curve of a p-type semiconductor indicated by dotted lines after [18].

In the following, the two different oxides from generation 3 and 4 are compared with respect to the MOS capacitor ideality. Here, the grown $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructure is identical for both samples to be compared, only the applied SiO_2 is differently processed. All data is

acquired by the DLTS FT1230 HERA system from PhysTech working at 1 MHz, where the temperature is varied between 50 K and 300 K.

First, the leakage currents through the oxide layer are measured by applying a voltage at the gate contact of similar range as used for further characterization. Fig. 2.40 shows the room temperature I-V characteristics of samples from generation 3 and 4 featuring a 50 nm thick SA-USG SiO₂ and a 60 nm thick HDP-CVD SiO₂, respectively. The oxide used for generation 3 shows a 1-3 orders of magnitude higher leakage current reaching values of 4 μA/cm² at accumulation (-10 V) and depletion (±10 V). In contrast, the leakage current through the oxide of generation 4 is at a constantly low level of 50 nA/cm². Thus, MOS capacitors fabricated with a 60 nm thick HDP-CVD SiO₂ on top of the Si_{0.06}Ge_{0.94}/Ge stack provide a less leaky device structure for capacitance measurements. The reduced leakage enables a more accurate way of measuring the parallel semiconductor capacitance as the parallel resistance is increased (see eq. 1.106 of chapter 1).

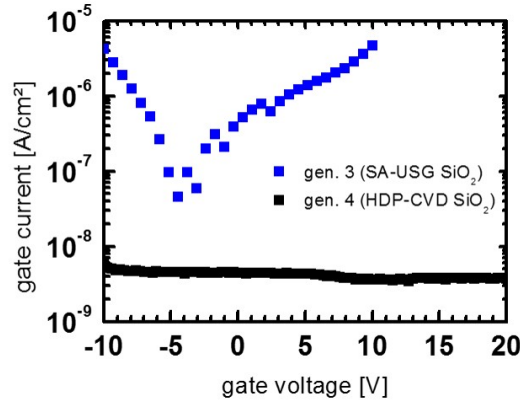


Figure 2.40: I-V curves of the studied MOS capacitors of generation 3 and 4 featuring different fabricated gate oxides at RT.

The corresponding temperature-dependent C-V characteristics of the MOS devices from generation 3 and 4 are shown in Fig. 2.41 a) and b) respectively. It becomes obvious that the oxide capacitance in accumulation (negative applied voltage) changes with temperature for MOS capacitors from generation 3, while C_{ox} is constant over the full temperature regime for MOS capacitors from generation 4. Based on the nominal oxide thickness d_{ox} of 50 nm (gen. 3) and 60 nm (gen. 4), the gate areas of each generation, the permittivity of the vacuum $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm and the relative permittivity of SiO₂ $\epsilon_{ox} = 3.9$, the theoretical oxide capacitance can be calculated according to eq. 2.22:

$$C_{ox} = \frac{A\epsilon_0\epsilon_{ox}}{d_{ox}} \quad (2.21)$$

This results in a theoretical C_{ox} of 280 pF for MOS capacitors of generation 3 and a C_{ox} of 470 pF for generation 4 devices. As can be seen from Fig. 2.41 a), the measured C_{ox} values are quite different from the theoretically calculated one. At 300 K, the measured C_{ox} of approximately 240 pF is the closest to a theoretical C_{ox} of 280 pF. Since eq. 2.22 does not contain temperature-dependent quantities, no change in C_{ox} should be observable in the measured temperature range. However, deviation from the calculated C_{ox} at lower temperatures is observed, which may indicate multiple recharging processes inside the oxide

itself that influence the measured C-V characteristics to a large extent as can be seen in Fig. 2.41 a). In contrast, the measured C_{ox} values of 470 pF at each temperature of MOS capacitor from generation 4 matches exactly with the theoretical calculated C_{ox} value (470 pF). The good correspondence of the C_{ox} values offers optimal conditions for determining the semiconductor capacitance from the measured gate capacitance of the fabricated MOS capacitors.

In addition, the C-V curves in Fig. 2.41 (a) are shifted on the voltage axis towards negative voltages compared to C-V curves in Fig. 2.41 (b). According to Fig. 2.39 (a), such shifts to negative biases indicate a higher amount of fixed oxide charges located close to the SiO_2 - $\text{Si}_{0.06}\text{Ge}_{0.94}$ interface that are probably caused by structural defects of the deposited SA-USG oxide. These immobile positive oxide charges may be responsible for the deviation from C_{ox} . Furthermore, the above-described stretch-out of capacitance along the voltage axis is observed in C-V curves from generation 3 compared to the curves of generation 4, especially for curves at lower temperatures. This additional voltage needed for a similar portion of depletion in the semiconductor is caused by the break in lattice periodicity at the $\text{Si}_{0.06}\text{Ge}_{0.94}$ -oxide interface giving rise to interface trapped charges. Consequently, the SA-USG SiO_2 exhibit more interface trapped charges than the SiO_2 deposited by HDP-CVD on the used $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructure. Based on the Ge-like surface, the introduced density of states mainly caused by dangling bonds will be, however, be higher compared to the optimized Si- SiO_2 MOS system.

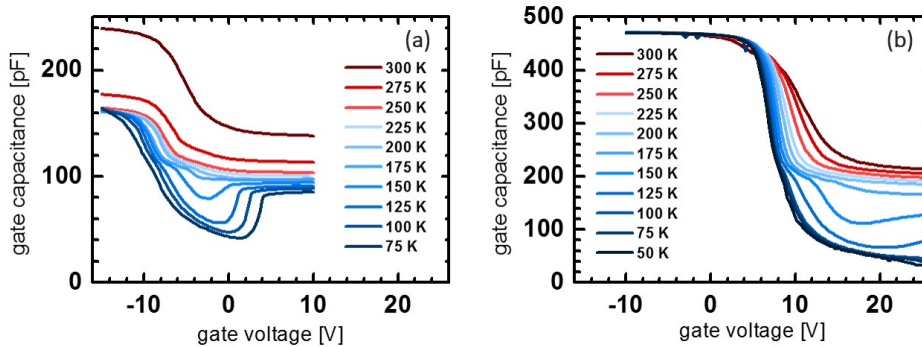


Figure 2.41: Temperature dependent HF C-V curves of (a) generation 3 and (b) generation 4 fabricated MOS capacitors.

A further indicator of the MOS capacitor ideality is the quality factor Q describing the ratio between reactance and resistance in a semiconductor device (see chapter 1). The quality factor at 300 K and 75 K of the measured MOS capacitors from generation 3 and 4 are illustrated in Fig. 2.42. For samples from generation 3, the quality factors are quite low ($Q \leq 5$) at both temperatures. However, the quality factors of samples from generation 4 are above 10 at accumulation, indicating a dominant reactance in the capacitance measurement. Although, Q decreases at the onset of depletion at room temperature, Q increases rapidly when the temperature is reduced. The improved quality of the MOS capacitors from generation 4 maybe on the one hand related to the better oxide quality, and on the other hand to the higher doping of the Si substrate that reduces the series resistance in the MOS configuration during capacitance measurements.

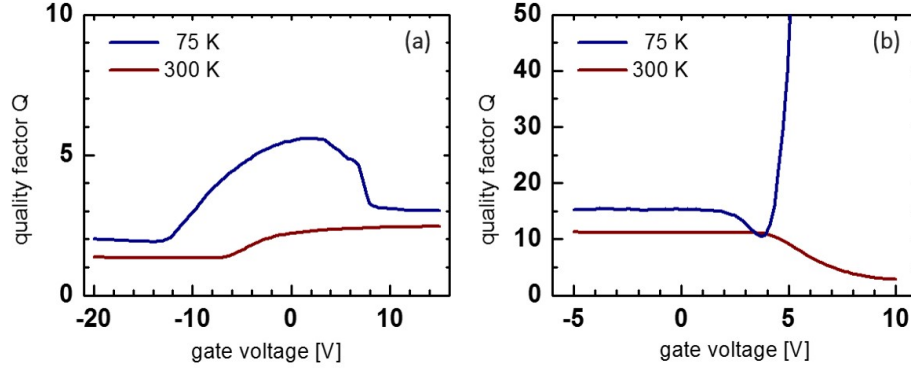


Figure 2.42: Quality factors at 300 K and 75 K of MOS capacitors of (a) generation 3 and (b) generation 4.

In conclusion, the HDP-CVD SiO_2 used in generation 4 MOS capacitors shows better quality in terms of less leakage through the oxide and reduced fixed oxide charges as well as interface trapped charges compared to the SA-USG SiO_2 applied in generation 3 devices. By using HDP-CVD deposition, interdiffusion of Si and Ge can be avoided based on the low growth temperature and no need for additional thermal treatment. In addition, no extra Si layer is needed to form SiO_2 by thermal oxidation. Such HDP oxides also showed good qualities in previous studies on Si substrates. The defective oxide of generation 3 capacitors affects the C-V characteristics to a large extent. Moreover, the reduced resistivity of the Si substrate utilized in generation 4 results in an improvement of the quality factor. Therefore, it is concluded that the HDP-CVD SiO_2 is better suited for the fabrication of good quality MOS capacitors needed for reliable capacitance measurements in order to evaluate the TDD-related carrier densities as well as defect states. Consequently, only MOS capacitors from generation 4 are used in the following analysis.

2.4.3 Residual p-type doping in intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructures

In order to estimate the defect related active carrier concentration in the as-grown intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures capacitance-voltage measurements are applied and will be discussed in this subsection.

First, the measured C-V curves confirm previous observations that the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ layers show a p-type conductivity. This has been concluded as a result of an accumulation behavior of the MOS capacitors at the negative gate voltages as can be seen in Fig. 2.43. Here, majority carriers (holes) are attracted below the oxide and the capacitance in accumulation is only caused by C_{ox} . This behavior is typical for p-type semiconductors because holes are the majority carriers. Such residual p-type conductivity is in line with previously observed studies on similar Ge-rich SiGe layers [59, 60] as well as in GeSn films grown on Ge substrates [61, 89] and plastically deformed Ge bulk materials [62] as already discussed in section 2.3.2. Although, this p-type conduction of intrinsic Ge-based materials is commonly attributed to acceptor-like defect states caused by plastic deformation and/or strain relaxation, its origin is still under discussion in recent literature [59, 62].

Fig. 2.43 shows the temperature dependent C-V characteristics of MOS capacitors of generation 4 in two different modes. In Fig. 2.43(a) the commonly applied high-frequency (HF) capacitance

is measured with an AC frequency of 1 MHz. The observed difference in HF capacitance between higher and lower temperatures in the depletion regime is associated with a contribution of minority carriers to the total charge consideration. These minority carriers may originate from electron-hole pairs generated at deep defect centers in the space charge region. In the process of generation, holes will flow to the substrate back contact forced by the electric field and do not contribute to the overall charge distribution, but electrons will gather at the oxide interface below the gate and build up an inversion layer. In fact, the extension of the depletion region into the semiconductor is hindered by the counteracting inversion charges that is expressed by higher capacitance values at equal gate voltages (see Fig. 2.43(a)). Although the small signal frequency of 1 MHz should be sufficiently fast to avoid inversion processes, traps with very short time constants may be nonetheless able to follow the small signal frequency of the HF capacitance measurement.

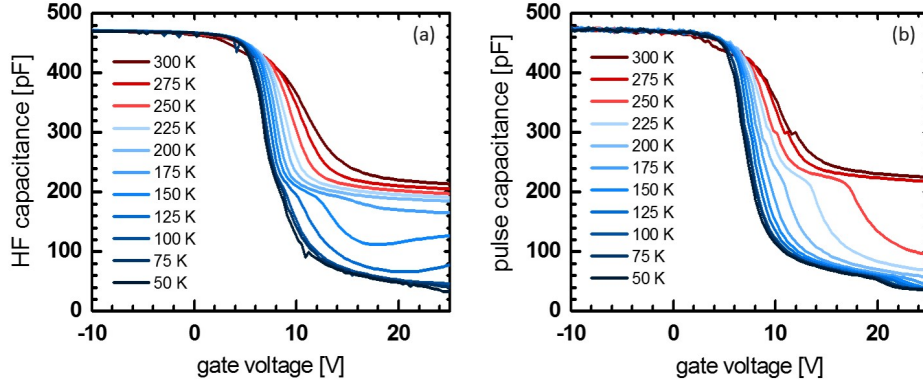


Figure 2.43: Temperature dependent C-V characteristics of MOS capacitors of generation 4 measured in (a) high-frequency and (b) pulsed mode.

In order to eliminate any inversion processes a pulse capacitance is measured instead of a HF capacitance. Here, the MOS capacitor is held in accumulation and then pulsed to the certain reverse bias values for 100 μ s to measure the capacitance in depletion. With such measurement procedure, inversion processes in MOS capacitors can be prevented and the doping concentration can be calculated more precisely. However, the temperature-depend pulse C-V characteristic in Fig. 2.43(b) still shows a contribution of inversion for temperatures above 200 K as the expansion of the space charge region is hindered in the reverse bias regime. The included traps inside the $\text{Si}_{0.06}\text{Ge}_{0.94}$ /Ge heterostructure may be able to respond to the short bias pulse at an elevated temperature but are unable to respond at a lower temperature since the emission time constants of deep traps increase with decreasing temperatures [90]. Nevertheless, by measuring the pulse capacitance, it is possible to obtain real C-V characteristics without an impact on inversion charges up to higher temperatures compared to the HF capacitance. The potential dependent depletion width x_d is calculated according to eq. ?? including the semiconductor capacitance C_{SC} , the gate area A , the vacuum permittivity ϵ_0 and an assumed ϵ_s of 15.93 for the $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer estimated by Vegard's law:

$$x_d = \frac{\epsilon_0 \epsilon_s A}{C_{sc}} \quad (2.22)$$

Accordingly, the depletion width equivalent to the information depth extends from the oxide-semiconductor interface into the Si_{0.06}Ge_{0.94}/Ge heterostructure as represented in Fig. 44. Thus, it becomes possible to deplete the whole Si_{0.06}Ge_{0.94} layer of 1500 nm and the first 500 nm of the Ge buffer at lower temperatures by applying a maximum reverse bias of 20 V.

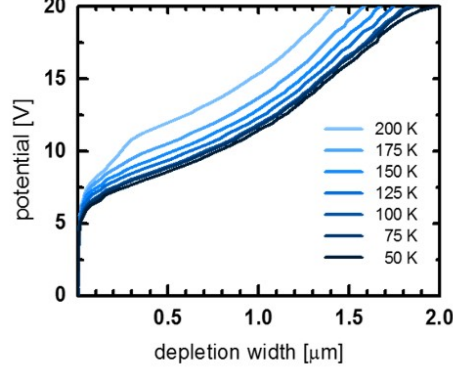


Figure 2.44: Temperature dependent depletion width extracted from the pulse capacitance mode after [88].

Based on the pulse C-V characteristics the carrier density profiles at temperatures below 200 K are calculated from the slope of a $1/C^2$ -V plot [3]. Here, the depletion dependent majority carrier concentration $N(x_d)$ of the MOS capacitor is estimated by:

$$N(x_d) = \frac{2}{q\epsilon_0\epsilon_s A^2 \frac{d(1/C^2)}{dV}} \quad (2.23)$$

where q is the elemental charge, ϵ_0 and ϵ_s as permittivity of vacuum and an the Si_{0.06}Ge_{0.94} layer, respectively, A is the gate and $d(1/C^2)/dV$ the slope of the $1/C^2$ plot. The corresponding temperature dependent majority carrier densities as a function of depletion width are shown in Fig. 2.45(a).

The increased carrier concentration in the first 300 nm from the top surface is considered erroneous due to Debye length limitation [3]. The Debye length (see eq. 1.43 of chapter 1) sets a limit to the spatial resolution of the measured majority carrier profile, since a charge imbalance is neutralized by majority carriers under equilibrium conditions within this range [3]. Equation 2.23 is based on the depletion approximation assuming no mobile carriers in the space charge region. While it is true for larger reverse biases, mobile carriers cannot be neglected for small surface potentials in MOS capacitors. It is reported that doping density profile determinations from pulse C-V measurements lead to errors for surface potentials below 0.1 V ($2-3 L_D$) for the SiO₂-Si material system [3]. Neglecting the increase in carrier concentration at the top surface, a constant majority carrier density of approximately $5 \times 10^{15} \text{ cm}^{-3}$ of the nominal intrinsic Si_{0.06}Ge_{0.94} layer is extracted from eq. 2.23. For temperatures below 100 K, it becomes possible to additionally extend the space charge region into the equally intrinsic Ge buffer layer below the Si_{0.06}Ge_{0.94} layer. Here, the carrier concentration decreases down to $1 \times 10^{15} \text{ cm}^{-3}$ after overcoming the defective Si_{0.06}Ge_{0.94}/Ge heterointerface at a depth of 1500 nm.

The existence of a free hole concentration ($p = N_{A^-} - N_{D^+}$) including ionized acceptors N_{A^-} and compensating donors N_{D^+} in the nominally intrinsic Si_{0.06}Ge_{0.94}/Ge layers might

be related to deep acceptor-like defect states inside the semiconductor bandgap [89]. In consequence of the hetero integration on Si and the absence of any dopants, the included TDs can be a reasonable direct or indirect source of the observed defect states. The almost constant ($5\text{-}7 \times 10^{15} \text{ cm}^{-3}$) majority carrier density in the $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer in a temperature regime between 50 K and 200 K (see Fig. 2.45(b)) suggests a full occupation of the included acceptor states.

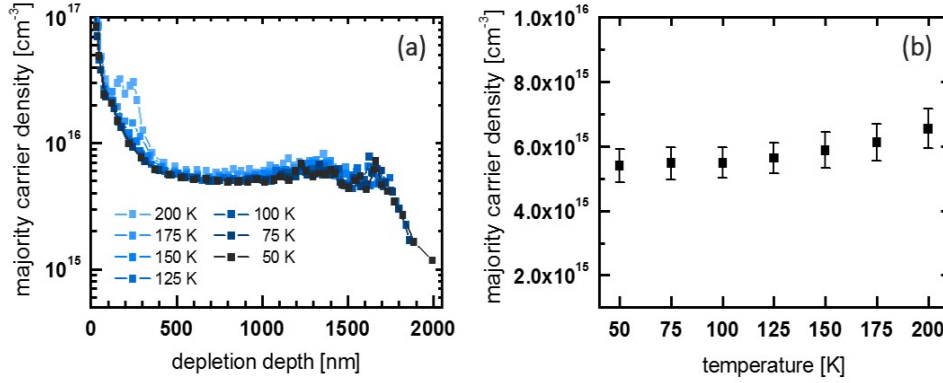


Figure 2.45: Majority carrier density estimated from pulse C-V data of (a) the full information depth using a maximum V_R of 20 V and (b) only the $\text{Si}_{0.06}\text{Ge}_{0.94}$ epilayer [88].

While acceptor-like defect states are commonly reported as source of the observed effective background hole concentration in comparable intrinsic Ge-based materials [59, 62], it is difficult to compare the extracted density values because of a lack of recent literature. The revealed effective background carrier concentration in the mid 10^{15} cm^{-3} range (50 K-200 K) in intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}(001)$ heterostructure can be merely compared to a hole concentration of $2 \times 10^{16} \text{ cm}^{-3}$ at RT in $\text{Ge}_{0.922}\text{Sn}_{0.078}$ epitaxial layers grown on n-Ge substrates [61], a free carrier concentration of $2\text{-}3 \times 10^{17} \text{ cm}^{-3}$ in p-type $\text{GeSn}/\text{Ge}/\text{Si}(001)$ MOS capacitor [89] and a hole density that increases from 10^{16} to 10^{18} with increasing Ge content ($>40\%$) in SiGe films grown on SOI substrates [60].

2.4.4 TD related defect states revealed by DLTS

On the basis of a successful fabrication of good quality MOS capacitors from the investigated $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures DLTS can be applied to study the included defect states. The findings will be discussed in this subsection. In consequence of the hetero integration of Ge-based material on Si and the absence of any doping processes, the included TDs are assumed as a reasonable direct or indirect source of the present defect states.

As described in the introduction chapter, DLTS implies a temperature dependent high-frequency junction capacitance measurement [36]. Traps located in the space charge region are discharged by applying a reverse bias and filled up with majority carriers when a pulse voltage is applied. Switching back to the reverse bias condition causes a time-dependent emission of carriers out of the traps characterized by a change in capacitance. These capacitance transients are recorded and analyzed in order to describe deep traps in semiconductors [36].

For the DLTS temperature scan shown in Fig. 2.46, a reverse voltage V_R of 20 V and a filling pulse voltage V_p of 0 V were applied at the gate of the MOS capacitor. For these bias

conditions, the space charge region extends from the oxide interface up to a maximum of $2 \mu\text{m}$ into the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostack (see Fig. 2.44). The voltage pulse was applied for a duration t_p of $100 \mu\text{s}$, which is commonly sufficient to fill all the traps with free carriers. The capacitance transient was recorded within a period width T_w of 20.48 ms . The transient is digitalized by the measurement software afterwards and a Fourier transform is applied. Here, the first sine coefficient b_1 of the measured capacitance transient is used to all following evaluations, which is an equivalent to the standard DLTS rate window [3].

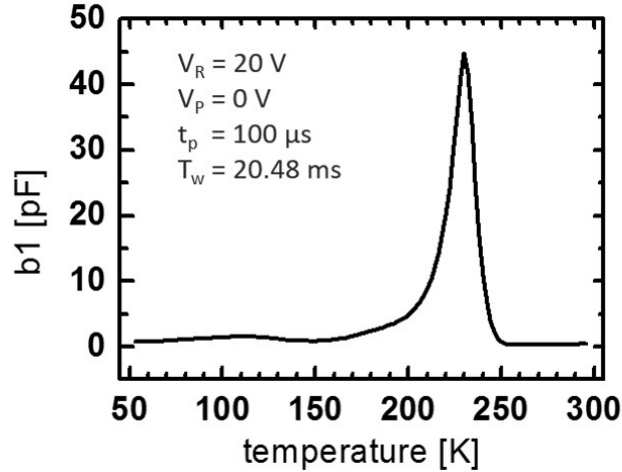


Figure 2.46: DLTS temp scan of $\text{SiO}_2/\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructure showing the first sine coefficient b_1 of the Fourier transform of the measured capacitance transient [88].

One dominant hole trap is found in the DLTS spectra of Fig. 2.46. According to the peak appearing at a temperature of 225 K , it is associated with a thermal activation energy E_T of the carrier emission rate from the bulk trap of 0.325 eV above the valence band E_V estimated by an Arrhenius plot as shown in Fig. 2.47. The corresponding hole capture cross section σ is calculated to $8.69 \times 10^{-17} \text{ cm}^2$, which is in the same order of deep levels found in other Ge/Si heterostructures [70, 91].

Arrhenius plots contain the natural logarithm of the emission time constant τ plotted against the reverse temperature $1/T$. The emission time constants of the observed emission process can be extracted from the maximum of the dC versus T plots that are evaluated by using several correlation functions at every measured transient. The slope of such Arrhenius plots gives the trap level energy and intercept determines the capture cross section of the measured trap.

Assuming a similar bandgap for the $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer like pure Ge (0.66 eV), the observed defect level ($E_V + 0.325 \text{ eV}$) is located at mid-gap position and, therefore, an attractive trapping center for free carriers and/or an effective generation-recombination (G-R) center. This will impact the active carrier concentration in final devices built, using similar Ge -rich SiGe/Ge heterostructures as discussed in the previous section.

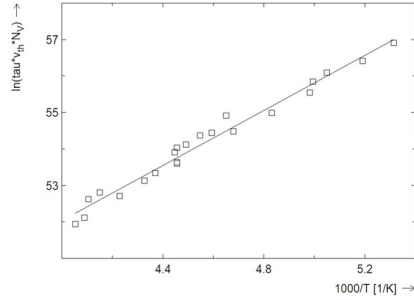


Figure 2.47: Arrhenius plot of the data acquired from Fig. 2.46 including the natural logarithm of the time constant τ and the inverse temperature $1/T$.

The DLTS temperature scan is repeated by changing the filling pulse time t_p , while all other parameters are kept constant. All data is acquired in one temperature sweep. As shown in Fig. 2.48 the observed dominant hole trap is constant in temperature and intensity down to a filling pulse time of $10 \mu\text{s}$. The intensity is decreased when t_p is $1 \mu\text{s}$. Since the intensity of the DLTS peak is correlated to the trap density, a constant peak height with changing t_p points towards a complete occupation of the trap for t_p longer than $10 \mu\text{s}$. This is good agreement with the almost constant background carrier concentration of the intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ layer revealed in the previous subsection. A full occupation is characteristic for point-like defects inducing localized energy levels in the bandgap that can completely be filled with carriers after a certain time. In contrast, extended defects would show a capture behavior that is mutually affected by the band-like states creating a Coulombic potential barrier [89, 92].

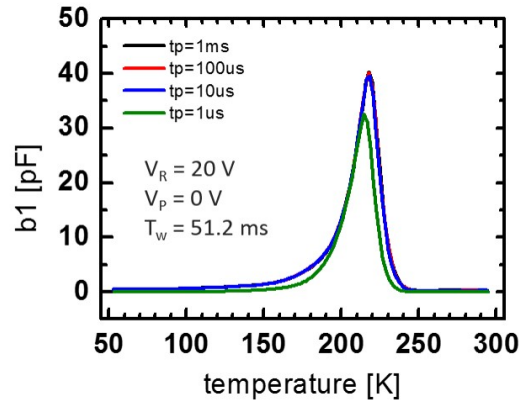


Figure 2.48: DLTS temperature scan of $\text{SiO}_2/\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructure including a variation of the filling pulse time t_p .

For further characterization of the observed defect level the carrier trapping kinetics were recorded in order to distinguish between point and extended defects as origin of the observed defect state [89]. While point defects show a saturating capture behavior of free carriers with increasing pulse time t_p , extended defects exhibit a logarithmic trap filling [89, 92]. The responsible band-like states in extended defects e.g. active defect sites in a dislocation line hinders the continuous carrier trapping at adjacent sites by creating a Coulombic potential barrier [89].

The effect of filling pulse time t_p on hole trapping at the peak temperature of spectra in Fig. 2.46 (225 K) suggests both point and extended defect character as shown in Fig. 2.49. After a continuous trapping of carriers up to $10 \mu\text{s}$, a saturation of the DLTS signal takes place, since

the single localized point defect levels can be filled only up to a complete occupation [89, 92]. However, the DLTS signal is still increasing, with a lesser rate of increase when longer filling pulses are applied as shown in the inset of Fig. 2.49, pointing towards an extended defect character. As reported by Schröter et al. [93], defect states associated with dislocation can be localized when interacting with point defects or of band-like character if the dislocations are clean. Here, either the exchange of carriers with the band edges are favored by emission and capture processes (localized) or the internal equilibrium rate within the defect states are more likely (band-like) [92]. Accordingly, the observed acceptor-type bulk defects located at $E_V + 0.325$ eV may be correlated with native point defects introduced during the epitaxial growth of the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructure, which accumulate in the long range strain field around TDs (Cottrell atmosphere [10]) [24, 60, 67, 70, 93, 94, 95]. A possible candidate for these native point defects are vacancies since they create acceptors in Ge crystals and can easily form during epitaxial growth [62].

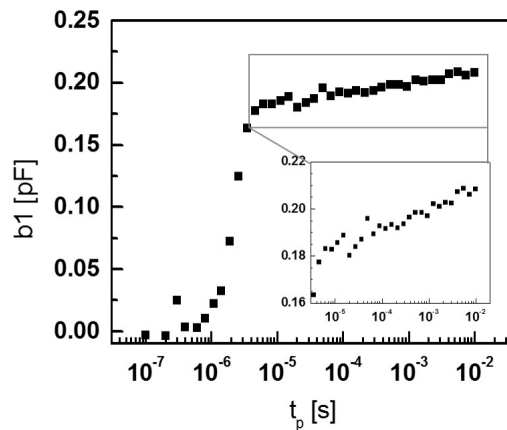


Figure 2.49: Isothermal DLT spectra of the observed hole trap at 225 K based on filling pulse time t_p [88].

According to the DLTS theory [36], an isothermal period scan, where the period width T_w is varied, is an equivalent to the common temperature scan. Both are constructed from the Fourier transform of the capacitance transient and can be used to further characterize the included defect states [89]. Such isothermal period scans are performed at the peak temperature of 225 K by changing the duration in which the capacitance transient is recorded (T_w) and are presented in Fig. 2.50. By increasing the filling pulse voltage V_p from +6 V to 0 V (Fig. 2.50(a)), the peak is distorted towards higher period width T_w and, therefore, higher temperatures, indicating multiple states are present. Here, more traps are being filled farther away from the band edges with increasing V_p [89]. Similarly, when the filling pulse time t_p is increased as shown in Fig. 2.50(b) the peak slightly moves to higher temperatures. Assuming the thermal activation of band-like states based on threading dislocations would be weighted towards states farther from the valence band with increasing temperatures and thus longer t_p [89]. Therefore, shorter filling pulse times t_p only populate lower energy states and by increasing t_p higher states can be filled up with majority holes leading to a shift to higher temperatures or rather higher T_w (see Fig. 2.50(b)) [89].

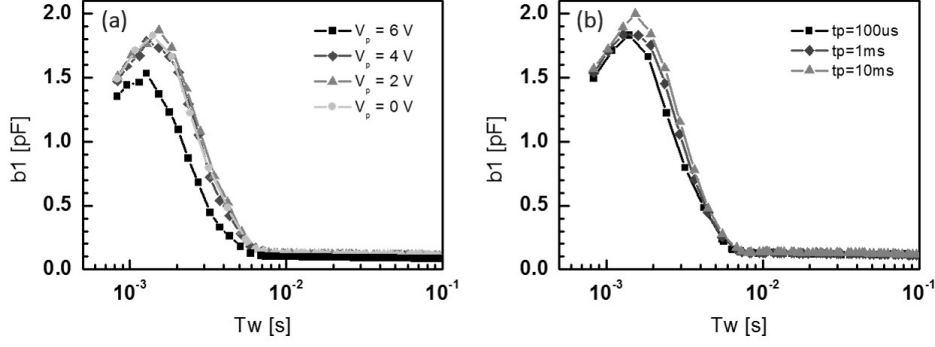


Figure 2.50: Isothermal period scans at peak temperature of 225 K showing a variation of (a) the filling pulse height V_p and (b) the filling pulse time t_p .

The apparent activation energy of 0.325 eV confirms that the observed states are present closer to midgap position. While as-grown dislocations and dislocation networks introduced by plastic deformation in bulk Ge are assigned to shallow one dimensional energy bands split off from the valence and conduction band [24, 52, 95], threading dislocations based on plastic relaxation in Ge heterostructures integrated on Si(001) give rise to deeper defect states inside the Ge bandgap. Such deep defect states may indicate an impurity decoration along the dislocation line or point defect clusters left behind dislocation movement [70]. Two hole traps at $E_V + 0.156$ eV and $E_V + 0.183$ eV have been ascribed to TDs in Ge/Si photodiodes [91], one dominant hole trap located at $E_V + 0.15$ eV is observed in strained $\text{Ge}_{0.93}\text{Sn}_{0.07}/\text{Ge}/\text{Si}$ heterostructures where it is attributed to clean TDs based on the sole logarithmic trap filling kinetics [89], band-like states with an apparent activation energy of 0.291 eV are correlated to dislocations in unintentionally doped GeSn epitaxial layers on Ge-on-Si substrates and acceptor states are found in Ge junctions selectively grown in STI Si substrates located at $E_C - 0.33$ -0.4 eV [70].

2.5 Conclusion

I investigated the electrical activity of grown-in threading dislocations in Ge-rich SiGe/Ge heterostructures integrated on Si(001) substrates. The probability of tuning the threading dislocation density from 10^9 cm^{-2} down to 10^6 cm^{-2} by keeping composition, degree of strain relaxation and thickness constant, serves here as a unique opportunity for isolating the impact of TDs in the investigated heterostructures [56]. Furthermore, the investigation of grown-in TDs in intrinsic material allows for avoiding the integration of additional deformation-induced defects and the interaction with processing-induced defects originating e.g. from dopant implantation, respectively. In order to assess electrical properties of threading dislocations I developed two different device structures, p-n⁺ junction diodes and MOS capacitors, both operating in vertical orientation along the grown-in TD direction in the Si_{0.06}Ge_{0.94}/Ge heterostructure. Because of the careful and complex data processing in terms of excluding the influence of series resistances, separating the TD related area current component and choosing a reliable range for measuring the capacitance I was able to probe exclusively the TDD dependent diode I-V and C-V characteristics. Moreover, due to a consideration of the MOS device ideality I selected a suitable device for subsequent capacitance based defect evaluation for a given TDD by C-V profiling and deep level transient spectroscopy.

I demonstrated the p-type conductivity of intrinsically grown Si_{0.06}Ge_{0.94} layers by (1) the validated formation of a buried p-n⁺ junction when a phosphorous-doped Si_{0.06}Ge_{0.94} layer is introduced in the heterostack and (2) the accumulation at negative applied biases in the measured C-V characteristics of the fabricated MOS capacitors, which was confirmed by supportive Hall-effect measurements and electrical profile simulations with finite element simulation by Comsol Multiphysics. This reaffirms previous work that also observed p-type conduction of similar intrinsic Ge-based material [59, 60, 61, 62].

By probing the rectification of the fabricated p-n⁺ junction diodes, I revealed parasitic shunt channels along TDs based on the low specific resistivity of single TD in the range of $10^{-8} \text{ } \Omega\text{cm}$, which is comparable with values found for TDs in Si [67, 68]. The variation of the estimated resistivity per TD within the investigated samples indicates the presence of additional effects on the conductivity rather than merely the TDD. In this connection, possible effects are the saturating agglomeration of point defects like metal contaminations or vacancies at the dislocation line.

In addition, I outlined a detailed picture of the threading dislocation related leakage currents in rectifying devices and, therefore, carrier generation via threading dislocation related defects. I found a power law dependence of diode leakage currents with TDD, which differs from a previous reported linear dependency in Si-rich SiGe heterostructures [69]. I correlated this super-linear relation to an electric field dependent generation current contribution probably reinforced by the smaller band gap energy of pure Ge (0.66 eV) compared to Si (1.17 eV). By investigating the temperature dependence of the leakage currents I could identify trap-assisted tunneling via TD-induced defect states as the dominant transport mechanism at room temperature. At lower temperatures and at high electric fields, direct band-to-band tunneling without direct interaction with defect levels becomes the dominating type of transport. Nevertheless, the TDD dependent increase in free carrier concentration and, therefore, the

electric field present at the junction linked the BTB tunneling to the presence of TDs in $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures. Leakage currents related to emission from mid-gap traps by the Shockley-Read-Hall (SRH) generation is observed at higher temperatures (>100 °C). Here, I observed a reduced contribution of SRH generation in the studied $\text{Si}_{0.06}\text{Ge}_{0.94}$ material, featuring the minimal TDD ($3 \times 10^7 \text{ cm}^{-2}$), which I attribute to a reduction in point defect clusters trapped in the threading dislocation strain fields. In general, reducing the TDD leads to a strong reduction in area leakage currents, but my investigation also points towards an interplay between threading dislocations and additional point defect clusters as the origin of the leakage currents.

Furthermore, I used the I-V diode characteristic to estimate the TDD dependent carrier lifetimes of generation and recombination in order to classify the electrical quality of intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructures. I found an almost linear dependence on the generation lifetime with TDD calculated from the leakage generation rate that is corrected for the field-enhancement factor. The generation lifetimes decreased with rising TDD proving the degradation of the electrical layer quality due to the presence of TDs. As a guideline, TDDs in the range of 10^7 cm^{-2} halved the generation lifetime resulting in a marked deterioration in terms of leakage currents, while if the TDD can be tuned to the low 10^6 cm^{-2} range the deterioration of τ_g can be restricted within 10%. A maximal lifetime of $2 \times 10^{-9} \text{ s}$ can be expected by interpolating the observed dependency if the studied material does not contain any threading dislocations. Based on the relation between generation and recombination lifetime, I give an estimation for the energy level of included defect centers. For the minimal TDD ($3 \times 10^6 \text{ cm}^{-2}$), I extracted a level located at mid-gap ($E_i \pm 0.04 \text{ eV}$) that shifts towards the band edges with an increasing number of TDs. This points towards the presence of TD related deep G-R centers, which clearly enhance leakage currents rather than shallow trap states pulled down from the band edges due to TD strain fields. The TDD dependent shift in defect level energy position also indicates a possible occupation dependency of a band of defect states as it was assumed for the specific resistivity of single threading dislocations. By analyzing the diode characteristic it was, however, not apparent whether the TD related defect levels are sharp or consist of a narrow band of states.

Capacitance based measurements needed to be performed to further characterize the included defect states. Therefore, I developed MOS capacitors to eliminate the parasitic leakage currents, which hindered reasonable capacitance measurements in the studied p-n⁺ junction devices. Comparing two different approaches for fabricating MOS capacitors on the $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ heterostructure featuring a TDD of $2 \times 10^7 \text{ cm}^{-2}$ revealed the HDP-CVD SiO_2 as a good candidate for an insulating oxide layer. The low leakage current through the oxide of less than 50 nA/cm^2 , the higher quality factors for capacitance measurements, the matching values of measured and theoretical calculated C_{ox} values as well as the lesser influence of fixed oxide and interface charges motivated the choice of the HDP-CVD SiO_2 .

With C-V measurements at the fabricated MOS capacitors it became possible to probe the whole $\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}$ heterostructure, with the exclusion of a near surface region. Here, the carrier concentration is examined along the growth direction of the heterostructure. An effective carrier concentration of $5\text{-}6 \times 10^{15} \text{ cm}^{-3}$ could be revealed in the nominally intrinsic $\text{Si}_{0.06}\text{Ge}_{0.94}$ epitaxial layer in a temperature range between 50 K and 200 K. In addition, a

background hole concentration of $1 \times 10^{15} \text{ cm}^{-3}$ was observed for the Ge buffer underneath in a similar temperature regime.

Defect states included in the $\text{SiO}_2/\text{Si}_{0.06}\text{Ge}_{0.94}/\text{Ge}/\text{Si}$ MOS capacitors were probed using DLTS. One dominant hole trap is found at mid-gap position ($E_V + 0.325 \text{ eV}$), that is linked to acceptor-like point defects. However, investigations on hole trapping kinetics at the peak temperature (225 K) revealed both, point and extended defect character. Furthermore, isothermal period scans at 225 K also point towards band-like states that show a thermal activation weighting towards states father away from the valence band with increasing temperatures. This may associate the observed defect level at mid-gap with point defects that are trapped in the strain field around threading dislocations.

Overall, these results provide an extensive overview of the electrical activity of threading dislocations in Ge-rich $\text{SiGe}/\text{Ge}/\text{Si}(001)$ heterostructures and offer a valuable complement for existing studies in Ge bulk material and Si-rich SiGe materials.

2.6 Outlook

In this work I have investigated two different device structures in order to contribute new scientific knowledge on the electrical activity of threading dislocations in Ge-rich SiGe/Ge/Si(001) heterostructures. In the following I would like to outline potential improvements of the investigated devices and ideas for additional device structures that can be used to tackle this problem, using different approaches. Future work on the buried p-n⁺ junction diodes might include a decrease in phosphorous-doping of the bottom contact layer that will result in a reduced maximum electric field at the probed homojunction. Here, the extraction of the generation and diffusion current components and, therefore, a more precise estimation of generation lifetimes will be facilitated by a lower impact of high electric fields. The reduction of the n-doping will influence the ohmic contact formation. A trade-off between lowering the electric fields and ohmic contact resistance will have to be made here by choosing the proper phosphorous doping.

An additional possibility to measure generation parameters would be the use of three-terminal gate-controlled diodes [3]. The combination of a p-n junction diode with a MOS capacitor allows the separation of three generation regions: the diode space charge region, the MOS capacitor space charge region and the depleted surface below the gate [3]. From the sum of all three generation current contributions the generation lifetimes can be extracted from the total current that is measured at the p-n junction by varying the gate voltage at the MOS capacitor. To further improve the MOS capacitor one could apply an additional annealing in hydrogen atmosphere to saturate dangling bonds at the Si_{0.06}Ge_{0.94}/SiO₂ interface, which will lead to a reduction in D_{it} . Moreover, a reduction of the oxide thickness implied a reduction of the necessary maximal voltage in order to deplete the semiconductor. This would decrease the electric field present in the MOS capacitor, possibly also influencing the defect level emission. Again, a trade-off needs to be made between leakage through the oxide and minimizing the thickness.

A significant contribution to the picture of the electrical activity of threading dislocations in Ge-rich SiGe/Ge/Si(001) heterostructures could be delivered by investigating more MOS capacitor samples featuring different TDDs in a similar way. This will provide information about the TDD dependent background carrier concentrations over the full layer thickness. Additionally, the observed hole trap could be correlated to the amount of threading dislocations in the material and conclusions could be drawn on the origin and population of the included defect states.

In addition, an evaluation of the TDD dependent Hall mobility is planned. A first attempt has been made on samples used for p-n⁺ diode fabrication, but the high n-type doping of the layer below the intrinsic Si_{0.06}Ge_{0.94} led to a parasitic current flow in this bottom layer, which is evidenced by sheet resistance measurements on as-grown samples. A decrease of this n-doping will solve this problem and produce functional Hall bars as it was shown in the past on samples featuring equal TDDs. Based on the lateral direction of current flow in Hall effect measurements, the impact of threading dislocations on devices working perpendicular to their growth direction can be studied, for example carrier scattering at threading dislocations.

3

Defect related vertical breakdown in AlGaN/GaN HEMTs integrated on Si(111)

3.1 Scientific background

3.1.1 AlGaN/GaN HEMTs integrated on Si(111)

Gallium nitride (GaN) is a promising wide bandgap III-V compound semiconductor material for versatile applications in the field of short wavelength optoelectronics [96, 97, 98] and high frequency / high power electronics [99]. The direct bandgap of 3.39 eV at 300 K enables the operation of light emitting diodes (LED), laser (light amplification by stimulated emission of radiation) diodes and UV detectors at wavelengths of 365 nm [100]. In combination with other group III nitride semiconductor compounds like indium nitride (InN) (0.78 eV) and aluminum nitride (AlN) (6.2 eV) the entire visible spectral range can be covered.

In addition, GaN offers high electric breakdown voltages, thermal stability and conductivity, which makes it suitable as channel material for high-electron-mobility transistors (HEMTs) permitting high power operation [99]. Here, the combination with AlGaN offers a promising platform based on the formation of a two-dimensional electron gas (2DEG) featuring extremely high electron mobilities ($\approx 2000 \text{ cm}^2/\text{Vs}$), thanks to piezoelectric and spontaneous polarization effects in AlGaN [101, 102]. The polarization induces an electric field in the AlGaN barrier and promotes the accumulation of electrons from the GaN layer at the AlGaN/GaN interface, leaving behind positive space charges [102]. Since the Fermi level of GaN is lower than that of AlGaN, the electrons will flow from AlGaN into GaN and form a 2DEG exhibiting high sheet carrier concentrations of up to $2 \times 10^{13} \text{ cm}^{-2}$ suitable as conductive channel [101]. Strong polarization induced electric fields lead to an increase in the sheet carrier concentration and a stronger confinement of the 2DEG [101]. In undoped material, the free electrons are thought to originate from donor-like states at the AlGaN surface, which donate electrons into the

conduction band when the Fermi level crosses the donor state level [102]. Power devices based on AlGa_xN/GaN HEMTs offer faster switching speeds with higher breakdown voltages and lower on-resistances than traditional Si-based power chips and, therefore, are considered as preferable material system for power convertors in automotive, information technology and power supply industries [99].

Conventionally, AlGa_xN/GaN heterostructures are grown on foreign substrates like silicon carbide (SiC) or sapphire (Al₂O₃) but they are very cost-intensive, insulating in nature and not available in large size. In contrast, Si substrates provide a cost-effective and wafer-scale alternative to bulk GaN as well as SiC and Al₂O₃ substrates. The monolithic integration of AlGa_xN/GaN heterostructures on Si substrates encourages a CMOS-compatible process and enables the fusion of optoelectronics or high power electronic devices with Si-based electronics [103]. Here, the use of (111)-oriented Si substrates made it possible to mimic the hexagonal crystal structure of wurtzite GaN semiconductors. However, several technological challenges for fabrication must be considered. These include, among others, melt-back etching that is initiated if Ga comes in contact with Si [102, 104], a significant mismatch between GaN and Si in lattice constant (-17%) that leads to strain-induced plastic deformation incorporating a high number of misfit and threading dislocations ($\geq 10^8 \text{ cm}^{-2}$ [105]), and a coefficient of thermal expansion (CTE) (54%) promoting wafer bowing as well as the formation of cracks during cooling down from growth temperature to room temperature (RT) [103, 105] and diffusion of Si into growing GaN layers or Ga into Si substrate, which leads to n- and p-doping, respectively. In order to overcome the above-mentioned technological challenges and fabricate high-quality AlGa_xN/GaN heterostructures on Si(111), intermediate AlN nucleation layers and Al_xGa_{1-x}N buffer structures are applied. The epitaxial layer stacks of common AlGa_xN/GaN heterostructures integrated on Si(111) are sketched in fig. 3.1(a). A nucleation layer of AlN deposited on the Si(111) substrate initiates the growth, preventing possible melt-back etching and suppressing unintentional in-diffusion of Ga or Si [99]. In addition, the lattice mismatch between GaN and Si can be reduced down to 2.5% between AlN and GaN [105]. A prior deposition of a few monolayers of Al can act as barrier for the unintentional formation of amorphous silicon nitride (SiN) on the substrate surface [103]. The subsequent deposition of various buffer schemes is applied to induce compressive stresses compensating the tensile strain that originates during cooling down from growth temperature to room temperature. In combination with thick Si substrates (1 mm), these strain relief buffers are able to prevent the formation of cracks and reduce wafer bowing respectively, resulting in flat wafers with thick GaN and a high wafer yield [99, 106]. The two most successful approaches include the step-graded AlGa_xN buffer as well as superlattices of AlGa_xN/GaN or AlN/GaN that are demonstrated in fig. 3.1(b) and (c), respectively [99]. The ternary compound system of Al_xGa_{1-x}N applied in a graded manner by decreasing the Al content step-wise in separate layers gradually compensates the thermal and lattice mismatch between Si or AlN and GaN respectively [106]. A further advantage of AlGa_xN buffers is the increase in the series resistance providing good electrical isolation from the substrate [103]. Moreover, AlGa_xN/GaN or AlN/GaN strained-layer superlattices are applied to induce the required compressive strain in order to integrate high quality GaN on Si(111) [99, 100, 103]. A superlattice-based buffer

contributes to a reduction of dislocations, since the annihilation of dislocations is encouraged by their bending at the superlattice interfaces [103].

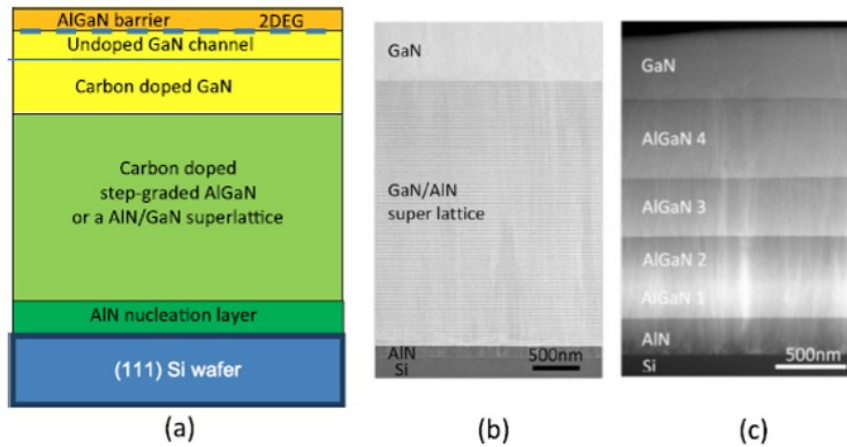


Figure 3.1: (a) Schematic cross-section of typical AlGaIn/GaN-on-Si HEMTs and TEM images of the two common buffer schemes (b) GaN/AlN superlattices and (c) step graded AlGaIn layers [99].

3.1.2 Vertical breakdown in AlGaIn/GaN-on-Si HEMTs

The maximum output power of GaN-based HEMTs is mainly determined by the high breakdown fields (> 4 MV/cm [107]), enabling the fabrication of power electronic devices with breakdown voltages in the order of 1.5-1.9 kV, depending on the gate-drain spacing, the strain compensating buffer thickness and applied substrate [108]. Fig. 3.2 ranks the breakdown field of GaN related to other semiconductor materials as a function of their bandgap energies, highlighting the benefits of using GaN-based HEMTs [109]. Here, breakdown describes the rapid increase in drain current during the off-state if the applied drain voltages exceed a critical value, which may result in device failures [108].

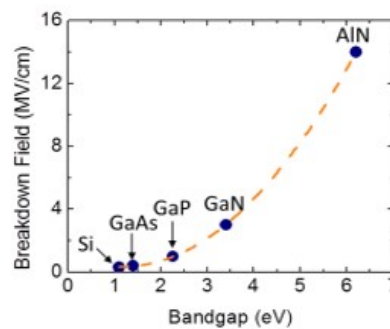


Figure 3.2: Breakdown fields of semiconductor materials [109].

However, the breakdown behavior of AlGaIn/GaN HEMTs integrated on Si substrates (AlGaIn/GaN-on-Si HEMTs) remains below theoretical expectations. For example, reported breakdown voltages of 600 V of AlGaIn/GaN-on-Si HEMTs are much lower than that of comparable AlGaIn/GaN HEMT structures grown on SiC (1.9 kV) featuring a similar total epi-layer thicknesses of about $2 \mu\text{m}$ [107, 110]. Consequently, for high power/high voltage applications of AlGaIn/GaN-on-Si HEMTs the physical origin and responsible mechanisms of the reduced breakdown needs to be understood in order to propose technological solutions

3. Defect related vertical breakdown in AlGa_N/Ga_N HEMTs integrated on Si(111)

or improvements to increase the device robustness [108]. There are different breakdown mechanisms discussed in literature, but in general three main leakage paths in AlGa_N/Ga_N-on-Si HEMTs are identified (see fig. 3.3): (1) through the Ga_N channel layer, where no substrate currents and/or relevant concentrations of electrons in the buffer are found; (2) through the upper AlGa_N buffer layer, when electrons become present due to higher drain voltages, resulting in slow reduction of the 2DEG confinement properties; (3) through the whole heterostructure just before the breakdown of the device takes place, when electrons might be injected from the substrate directly into the drain region caused by the full depletion of the buffer [107].

Nevertheless, it is suggested that the vertical top-to-substrate leakage ultimately limits the maximum breakdown voltages in AlGa_N/Ga_N-on-Si HEMTs [15,16]. According to literature, an accumulation of holes in the Ga_N buffer/transition layer and the injection of electrons from Si substrate contributes to the forward top-to-substrate bias breakdown, whereas impact ionization in the buffer dominates the reverse bias breakdown [110, 111].

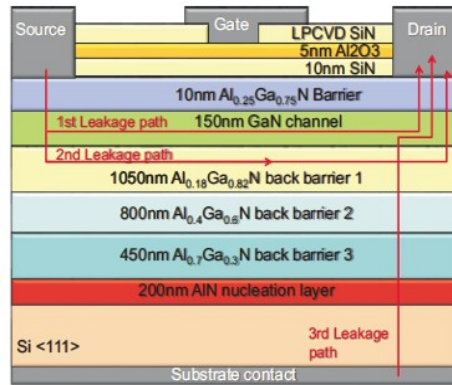


Figure 3.3: Three main leakage paths in AlGa_N/Ga_N-on-Si HEMTs reported in literature [107].

Several attempts have been made to improve the isolation of the Ga_N layer and the buffer below the 2DEG channel in order to reduce the leakage paths mentioned above. By introducing carbon (C) or iron (Fe) atoms, the resistivity of the buffer layer can be increased and short-channel drain leakage can be suppressed while the breakdown voltage increases [99]. In addition, Fe and C act as deep acceptors in AlGa_N/Ga_N alloys, which compensates the background donor doping in the intrinsic heterostructure for residual impurities like oxygen or silicon to a certain extent [111]. A rise in AlGa_N/Ga_N buffer thickness can also be applied to decrease the top-to-substrate leakage currents, since the breakdown field of the Si substrate is ten times lower than in Ga_N, making the AlN/Si interface and Si substrate more conductive compared to the high resistivity AlGa_N/Ga_N buffer [99, 112]. For example, the vertical buffer breakdown voltage at 1 $\mu\text{A}/\text{mm}^2$ is about 200 V for a 3.2 μm thick buffer, which can be increased to up to 650 V when the buffer thickness is raised to 5.5 μm [99]. This illustrates yet again that the nominally insulating AlGa_N/Ga_N buffer layers are actually electrically active and need similar efforts for optimization as the upper barrier and channel region when integrating on Si substrates [99]. Here it became apparent that the Si substrate is of special interest, considering the fact that the breakdown voltage of AlGa_N/Ga_N-on-Si HEMTs could be enhanced when the Si substrate is removed after deposition [110, 112]. In general, the vertical breakdown in AlGa_N/Ga_N-on-Si HEMTs is often correlated to the quality of the AlN nucleation layer and

its interface to the Si substrate [113]. Therefore, it is of particular interest to investigate the electrical active defects that are introduced by the growth of AlN on Si as starting layer for subsequent deposition of the AlGa_N/Ga_N heterostructure.

Previous investigations showed that the substrate resistivity is modified at the interface during growth of the AlN seed layer [114, 115, 116]. Here, near mid-gap hole traps are introduced by a significant in-diffusion of Al atoms into the Si substrate [114, 115, 116]. Acting as efficient G-R centers, these traps may force the build-up of an inversion layer at the AlN/Si interface, which is correlated with a reduction of the vertical breakdown voltage in AlGa_N/Ga_N-on-Si power devices by providing an excess of electrons [117, 118, 119, 120]. In literature, two main types of hole traps are found: (1) bulk traps near mid-gap position and (2) a distribution of states at the AlN/Si(111) interface [114, 115, 116, 117]. Here, the nature of the observed bulk traps varied with substrate resistivity. While they show an extended defect character for highly p-doped Si substrates, they display a point defect character in lower p-doped substrates [117]. An in-situ anneal of these defects, mimicking the thermal budget of further AlGa_N/Ga_N integration, leads to a further in-diffusion of Al into the Si substrate and an agglomeration of the included hole traps into clusters [114]. However, the epitaxial quality of the AlN layer and the AlN/Si interface as well as the damage on the Si substrate is strongly influenced by the AlN growth conditions [114]. It is therefore of special importance to evaluate the implications of the AlN seed layer formation on the AlN/Si material system in order to reveal possible physical origins of the vertical top-to-substrate breakdown in AlGa_N/Ga_N-on-Si HEMTs.

3.2 Investigated AlN/Si(111) heterostructures

The investigated AlN/Si(111) heterostructures in this chapter were epitaxially grown by metal-organic chemical-vapor deposition (MOCVD) on 6-inch Si(111) wafer by Siltronic AG, which serve as initial growth step for integrating GaN heterostructures on Si substrates. Prior to growth, the Si substrate were thermally cleaned inside the MOCVD reactor in order to remove residuals as well as the native oxide. For the final AlN growth trimethylaluminium (TMA) and ammonia (NH₃) were used as group III and V precursors respectively by utilizing hydrogen and nitrogen as carrier gases.

As mentioned above, the Al in-diffusion into the Si substrate causes defects at the AlN/Si interface as well as inside the Si substrate. Several attempts have been made to improve the AlN/Si interface by reducing the Al in-diffusion into the Si substrate and controlling the crystal quality of the initial AlN layer [121, 122, 123]. For example, variation of the substrate temperature during AlN growth, changing the Al/N flux ratio or introducing a thin Al wetting layer without supplying nitrogen, where also the temperature dependence of the TMA preflow was investigated [121, 122, 123]. In this study, a low temperature growth step during the initial AlN growth is investigated in order to reduce the in-diffusion and accordingly, the defect formation. Here, three samples of 200 nm thickness were provided for comparison integrated on similar boron doped (p-type) Si(111) substrates with resistivity of 5-20 Ωcm. Again, the (111) orientation of the Si substrate encourages the growth of wurtzite hexagonal AlN layers, resulting in good crystal quality nitride heterostructures [121]. The reference sample was grown homogeneously at above 1000 °C (sample A), whereas sample B and C were grown using a two step method including a thin layer < 50 nm at two different lower temperatures below 1000 °C on top of Si, followed by the residual growth at higher temperature > 1020 °C. The investigated set of samples is described in table 3.1.

set	sample	substrate resisitvity	AlN thickness	growth T	low T step
1	A	5-22 Ωcm	200 nm	> 1000 °C	non
	B	5-22 Ωcm	200 nm	> 1020 °C	< 50 nm @ < 1000 °C
	C	5-22 Ωcm	200 nm	> 1020 °C	< 50 nm @ < 900 °C

Table 3.1: Sample set of AlN/Si(111) heterostructures.

3.3 AlN/Si MIS capacitors

Based on the wide bandgap of 6.2 eV, AlN can be assumed as insulator and, therefore, the AlN/Si heterostructure behaves like a metal-insulator-semiconductor (MIS) capacitor when an additional metal gate is deposited [114, 115, 116, 117]. In the present study, fabricated MIS capacitors on samples described in the previous paragraph are characterized in terms of capacitance-based measurements to examine the electrical activity of defects inside the Si substrate and at the AlN/Si interface introduced by the AlN growth.

The investigated heterostructures in this chapter were grown at Siltronic AG whereas the MIS capacitors were fabricated at IHP by me. Transmission electron microscopic and secondary electron microscopic images were taken by M.A. Schubert and David Stolarek, respectively. I carried out the C-V and DLTS measurements and analyzed the data.

3.3.1 Device fabrication

The three provided 6-inch wafers from Siltronic AG were divided into 1.5 x 1.5 cm pieces by an in-house wafer sawing machine. Then, the metal gate contacts were fabricated on the AlN layers in IHPs vacuum coater (Edwards Auto 306), exhibiting a base pressure of 8×10^6 mbar created by a turbomolecular pumping system. Evaporation of a bilayer metal structure with approx. 20 nm nickel (Ni) and 100 nm gold (Au) was realized by resistive heating of a tungsten spiral and an aluminum boat, respectively. The gate contacts were formed through a shadow mask resulting in contact sized 1.3 mm in diameter [115]. On the backside, appropriate ohmic contacts were formed by manually scratching off the native oxide layer and applying an indium-gallium (InGa) eutectic film to the Si substrate. The final device cross-section of the fabricated MIS devices and the measurement arrangement are illustrated in fig. 3.4.

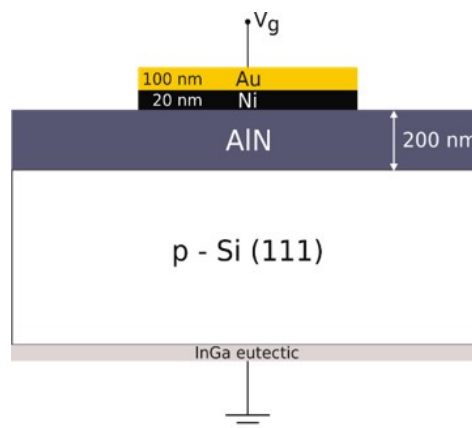


Figure 3.4: Schematic AlN/Si(111) MIS device and its measurement configuration.

3.3.2 Al in-diffusion determined by C-V characteristics

Based on the p-type doping of the Si substrate, an in-diffusion of group III Al atoms will enhance the substrate doping concentration because of Al acting as additional p-type dopant. Therefore, examining the doping concentration by capacitance-voltage (C-V) measurements

allows the assessment of the amount of Al in-diffusion depending on different growth procedures or sample configurations [114]. For comparison, C-V curves of all three samples are measured in high-frequency (HF) and in pulse mode at 1 MHz as illustrated in fig. 3.5 (a) and (b), respectively. Measuring the capacitance in HF mode excludes the contribution of minority carriers in the total charge consideration, since their generation rates are slower than the frequency of the applied signal. Nevertheless, defect states at the insulator-semiconductor interface can be very fast by changing their charge state rapidly according to the frequency of the applied signal. Here, changes in the applied bias and therefore the surface potential, move the semiconductor Fermi level above or below the interface states that are dispersed along the band gap by changing their occupancy. This results in an additional capacitance C_{it} in parallel to the depletion capacitance of the semiconductor C_{sc} , which has to be considered in the gate voltage drop of the MIS system. Therefore, possible charging effects of interface states at the AlN/Si interface may contribute to the measured capacitance and create steps in the measured capacitance as observed at approx. 10 V in fig. 3.5(a). In contrast, such steps that represent a change in the slope of the C-V curve could also indicate a change in substrate doping as discussed in the previous chapter. In order to minimize the contribution of C_{it} in the investigated MIS capacitors, the capacitance is measured in pulse mode, where bias pulses instead of a constant change in bias are applied (see fig. 3.5(b)). As a result, the steps in capacitance measurements observed at approx. 10 V are shifted to lower voltages in all measured devices of sample B and C. Sample A does not show any step in pulsed bias mode.

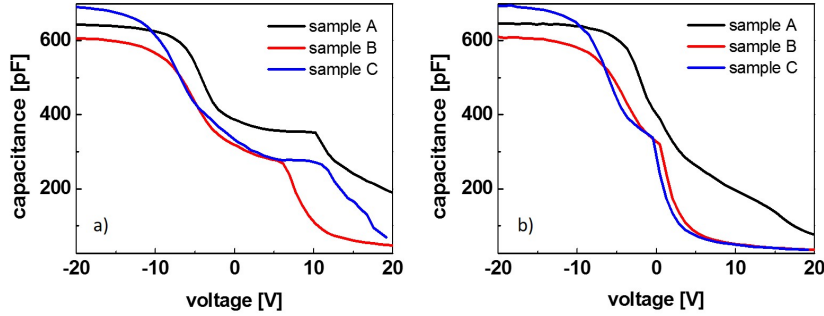


Figure 3.5: C-V measurements of investigated MIS capacitors at RT in (a) HF and (b) pulsed mode.

For calculating the shallow doping concentration of the silicon substrate, two approaches are considered. The first one uses the maximum-minimum capacitance method (C_{max}/C_{min}), where the doping density N_A can be determined by measuring the maximum HF capacitance in strong accumulation ($C_{ox} = C_{max}$) and the minimum HF capacitance in strong inversion ($C_{inv} = C_{min}$) [3]:

$$N_A = \frac{4\Phi_F}{q\epsilon_0\epsilon_{ox}A^2} \frac{R^2 C_{ox}^2}{(1-R)^2} \quad (3.1)$$

With $R = C_{min}/C_{max}$ and $2\Phi_F = 2(kT/q)\ln(N_A/n_i)$ being a transcendental equation that needs to be solved numerically. The advantage of this technique is that potential interface traps are no longer an issue [3]. Estimated doping densities by the C_{max}/C_{min} technique are an average value over the total space-charge-region width. The extracted doping densities of

the studied Si substrates depending on the AlN growth procedure are $9.69 \times 10^{15} \text{ cm}^{-3}$ (sample A), $8.57 \times 10^{15} \text{ cm}^{-3}$ (sample B), $1.13 \times 10^{16} \text{ cm}^{-3}$ (sample C) and listed in table 3.2.

set	sample	growth T	low T step	calculated doping
1	A	> 1000 °C	non	$9.69 \times 10^{15} \text{ cm}^{-3}$
	B	> 1020 °C	< 50 nm @ < 1000 °C	$8.57 \times 10^{15} \text{ cm}^{-3}$
	C	> 1020 °C	< 50 nm @ < 900 °C	$1.13 \times 10^{16} \text{ cm}^{-3}$

Table 3.2: Estimated doping densities of Si substrate by the C_{max}/C_{min} method.

Furthermore, the depletion dependent doping profile $N_A(x_d)$ is calculated by using the data of the pulsed capacitance via the slope of the $1/C^2$ versus voltage relationship [3]:

$$N_A(x_d) = \frac{2}{q\epsilon_0\epsilon_{ox}A^2 \frac{d(1/C^2)}{dV}} \quad (3.2)$$

It should be noted that for eq. 3.2 the semiconductor capacitance is required, which was extracted from the measured capacitance C_{meas} and the oxide/insulator capacitance C_{ox} by:

$$\frac{1}{C_{sc}} = \frac{1}{C_{meas}} - \frac{1}{C_{ox}} \quad (3.3)$$

The corresponding depletion depth x_d into the Si substrate starting from the AlN/Si interface is estimated by [3]:

$$x_d = \frac{\epsilon_0\epsilon_{sc}A}{C_{sc}} \quad (3.4)$$

For eq. 3.4 a gate area of $1.33 \times 10^{-2} \text{ cm}^2$ and a permittivity for Si of 11.7 are applied. Subsequently, the extracted doping profiles of the Si substrates are plotted in fig. 3.6 for comparison.

By means of the doping densities estimated with the C_{max}/C_{min} technique (table 3.2), no clear trend could be observed considering the different growth procedures of AlN. However, the doping densities (high 10^{15} cm^{-3} range) seem to be increased compared to the initial resistivity (5-20 Ωcm) of the Si substrates predicting a p-type (boron) doping in the order of $1 \times 10^{15} \text{ cm}^{-3}$. This is in line with literature, where an increase in p-doping of the Si substrate is observed due to Al in-diffusion [114, 117]. Although additional annealing treatments are reported to lead to a further in-diffusion of Al [114], the average doping concentration in the probed region of approx. 2 μm below the AlN/Si interface does not change to a big extent when a low temperature step either at < 900 °C nor < 1000 °C is applied. One reason for the minor difference in doping concentration may be related to the changes in measured C_{ox} values (see fig. 3.4) impacting the C_{max}/C_{min} ratio. Assuming an AlN thickness of 200 nm, an insulator capacitance C_{ox} of 500 pF can be expected. The observable deviation from the theoretical C_{ox} value could be related to a deviating thickness of the AlN layer or to the AlN quality as insulator itself, since defects in gate dielectrics can influence the C-V characteristics as discussed in the previous chapter [33].

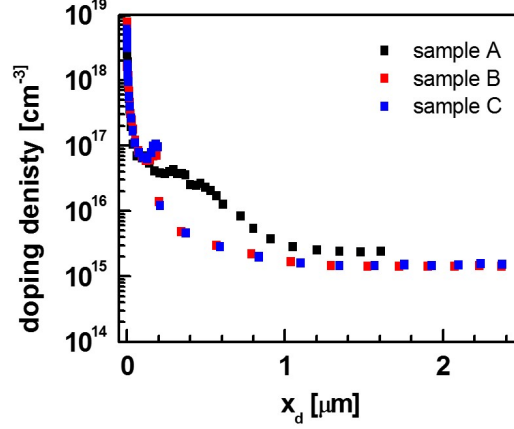


Figure 3.6: Extracted doping density profiles of the Si substrates by $1/C^2$ technique.

In contrast, the doping concentration profiles shown in fig. 3.6 indicate differences in the investigated samples featuring altered thermal budgets. It should be noted here, that the apparent increase in doping density at the AlN/Si interface ($x_d = 0 \mu\text{m}$) is related to the limited validation of the depletion approximation, which assumes zero mobile carriers in the space-charge region [3]. In contrast, at surface potentials below 0.1 V majority carriers cannot be neglected, which results in such erroneous doping concentration calculation near the AlN/Si interface [3]. Apart from the surface, the amount of Al in-diffusion can be evaluated using this approach. In all three samples, the initial doping of the Si substrate of $1 \times 10^{15} \text{ cm}^{-3}$ is measured with a depth from approx. $1 \mu\text{m}$ from the AlN/Si interface, similar to what was observed in literature for equal growth temperatures [114]. However, the bulk doping concentration of sample A without a low temperature step is slightly higher than in sample B and C, as illustrated by a smaller depletion depth x_d when similar bias is applied (+20 V). A strongly increased p-type doping, probably caused by the in-diffusion of Al, can be observed within the first $1 \mu\text{m}$, whereas sample A shows an enhanced constant doping in the mid 10^{16} cm^{-3} range up to $0.5 \mu\text{m}$. Although samples B and C that exhibit low temperature growth steps show a higher peak of increased doping of 10^{17} cm^{-3} , the depth where in-diffusion significantly affects the doping is limited to the first $0.2 \mu\text{m}$. This means that the affected region below the AlN/Si interface is more than halved compared to sample A without low temperature step. According to an exponential temperature dependence on the dopant specific diffusion coefficient [124], a decreased thermal budget at the beginning of the AlN growth may reduce the diffusion length of Al in Si. Additionally, this low temperature step seems to prevent a subsequent in-diffusion of Al even if the temperature is raised during the following growth of the residual 200 nm AlN layer. This contrasts with a further in-diffusion of Al during a subsequent annealing step at initial growth temperature reported in literature [114]. Furthermore, the low temperature growth step may minimize the decomposition of Ga and/or GaN deposited on the reactor wall, which is a further source of p-type doping [103]. Finally, there is no clear difference observable between sample B ($< 50 \text{ nm} < 1000 \text{ }^\circ\text{C}$) and C ($< 50 \text{ nm} < 900 \text{ }^\circ\text{C}$), pointing towards a successful reduction of Al in-diffusion already by decreasing the initial growth temperature below $1000 \text{ }^\circ\text{C}$.

For comparison, an AlN layer similar to sample A with a growth temperature of $> 1000 \text{ }^\circ\text{C}$ without a low temperature step was grown on a n-doped Si substrate of equal resistivity (10

Ωcm). Here, the possible Al in-diffusion may counteract the phosphorous doping of the Si substrate instead of enhancing the p-doping like in sample A-C. Indeed, the C-V curves in fig. 3.7(a) do not show a step in capacitance related to a peak in substrate doping. However, the high-frequency C-V curve shows a plateau in depletion (negative bias) since the inversion charges (holes in n-type material) below the gate prevent further extension of the space charge region into the Si substrate. By measuring the capacitance in a pulsed way, the inversion charges can be suppressed, and the space charge region extends beyond the threshold of the HF curve. By extracting the doping density profile as discussed above, the impact of similarly grown AlN layers on Si substrates featuring different types of doping (A: p-doping; D: n-doping) can be observed and is illustrated in fig. 3.7(b). In contrast to an enhanced p-type doping, the n-doping of the Si substrate is not influenced by the Al in-diffusion. Beyond the AlN/Si interface, the number of phosphorous dopants is in line with the provided resistivity and correlated doping concentration in the order of $1 \times 10^{15} \text{ cm}^{-3}$. The spike in doping density at approx. $1 \mu\text{m}$ could be related to the onset of inversion indicated by the start of deviation between HF and pulsed C-V curve at -3 V that may influences the calculation of the doping density in this point. On the contrary, this peak is similar to the depth where the Al in-diffusion causes an increased p-type doping in sample A and, therefore, may be an indication for the limit of Al in-diffusion.

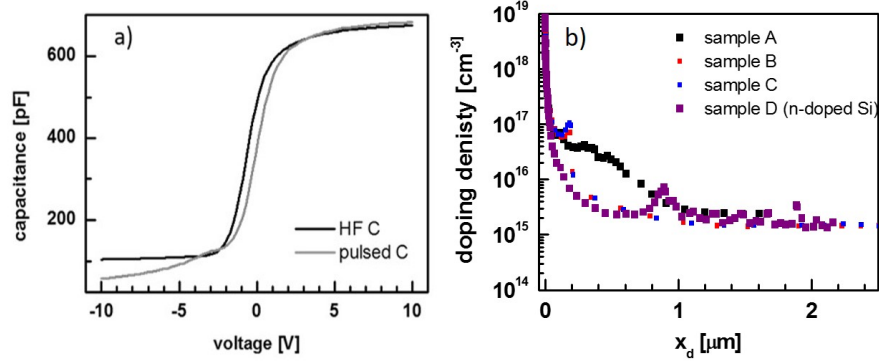


Figure 3.7: (a) C-V curves and (b) extracted doping density profile of the n-doped Si substrate by $1/C^2$ technique.

3.3.3 Defect properties characterized by DLTS

Based on the behavior of the performed DLTS measurements, only majority carrier traps will be detected, and therefore the reported activation energies E_A are related to the maximum of the valence band edge (E_V) in the studied p-type Si substrates.

As a starting point, frequency scans at room temperature were performed. Here, the DLTS amplitude is plotted as a function of the sampling period T_w , the time interval in which the decay in capacitance is recorded and analyzed. Fig. 3.8 shows the room temperature frequency scans of the investigated samples A-C featuring different AlN growth procedures. During the measurement, the MIS capacitors are held in depletion at a reverse bias V_R of 4 V and then pulsed towards accumulation in three steps ($V_P = -6 \text{ V}, -4 \text{ V}, 1 \text{ V}$) by using a pulse time t_p of $100 \mu\text{s}$ in order to fill the included trap levels. Subsequently, the applied bias is reduced to V_R again and the capacitance transient is evaluated. In all three plots a majority-carrier

peak is observable, indicating a hole trap in the Si substrate [115, 116]. Additionally, the peak increases with rising pulse height ($V_R - V_P$), while its position remains almost constant, typical for hole traps in Si [115]. As the peak height correlates with the trap concentration, the included number of traps seems to increase by introducing a low temperature step in the beginning of AlN growth and by reducing the temperature of this step. A similar trend is observed in literature where a post-growth anneal at higher temperatures removes part of deep hole traps measured in the as-grown samples [115]. Furthermore, the position of the peak maximum shifts towards longer sampling periods when a low temperature growth step is introduced, indicating a varying trap position within the Si bandgap.

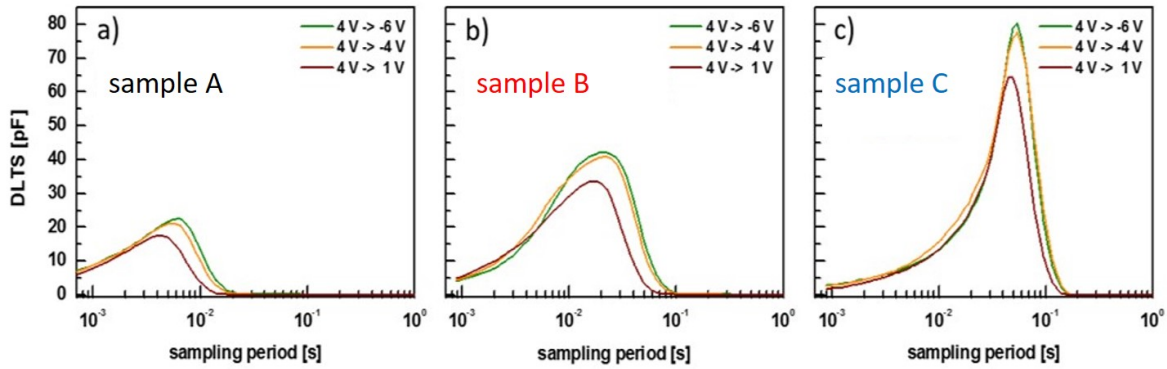


Figure 3.8: Frequency scan at room temperature of (a) sample A, (b) sample B and (c) sample C.

In order to determine suitable pulse conditions for a complete trap filling, the DLTS amplitude is monitored as a function of pulse duration t_p of the applied bias at room temperature [114, 115]. The trap filling kinetics of the three studied samples are shown in fig. 3.9. Similar for all three cases, the DLTS amplitude does not seem to saturate at a certain pulse duration t_p and, therefore, no complete filling of the included trap levels can be expected. As a consequence, the subsequently estimated trap concentrations from the temperature scan DLTS spectra will be underestimated [115]. Extended defects are known for a non-saturating trap-filling behavior, since they exhibit band-like states in the bandgap where the complete trap occupation is hindered by the columbic interaction between the trapped carriers. This might suggest an extended behavior of the introduced trap levels in the p-Si substrate. A similar increase of the DLTS amplitude with logarithmic pulse duration t_p of these traps was observed in literature on comparable AlN/Si MIS capacitors [114, 115]. Accordingly, pulse durations of 1 ms are chosen for the following temperature dependent DLTS investigations.

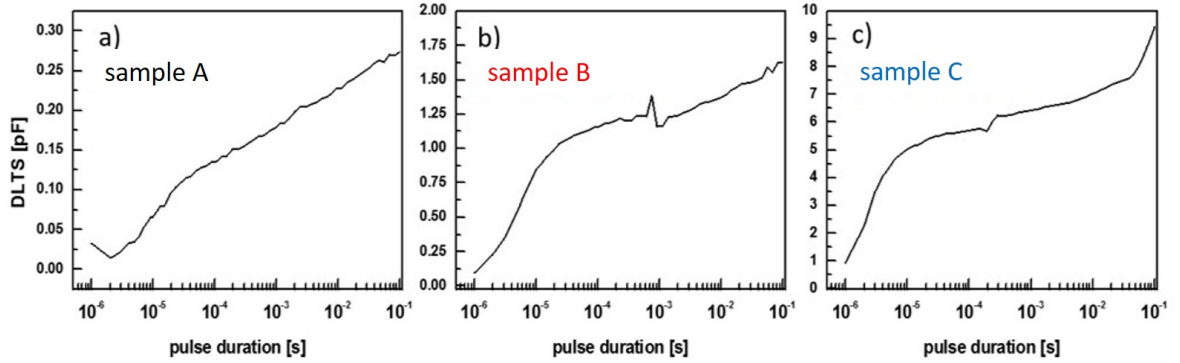


Figure 3.9: DLTS amplitude in dependence of filling pulse duration t_p at room temperature for (a) sample A, (b) sample B and (c) sample C.

In order to characterize the included traps, temperature scans are performed by ramping from 75 K to 320 K, using several bias pulse conditions similar to the frequency scans from fig. 3.8 at room temperature. Here, a filling pulse time t_p of 1 ms and a typical sampling period T_w of 512 ms were applied, which also defines the emission rate time constant τ_0 [115]. The DLTS spectra of the three investigated samples are shown in fig. 3.10. Similar to reported data in literature, one clear hole trap featuring a peak at around 250 K can be observed in all investigated samples [115, 116]. According to the peak height, the trap concentration increases when the temperature of the low temperature growth step is reduced, confirming the trend observed in the frequency scans of fig. 3.8. To distinguish between traps at the AlN/Si interface and in the bulk Si depletion region, the behavior of the peak amplitude as a function of the pulse height ($V_R - V_P$) is monitored [125]. While pulse voltages of -6 V and -4 V probe traps within the Si bandgap together with states at the AlN/Si interface, smaller pulse voltages like +1 V probe only traps in the Si bulk. In accordance with the reverse and maximum pulse voltage, a Si depletion region in the range of 1-30 μm from the AlN/Si interface is explored. Comparing the different pulse conditions, the main peak position does not change with pulse height, while the broad shoulder at the low temperature side reduces in amplitude for pulses only in the Si depletion region, indicating interface states (AlN/Si) as its origin [115, 125]. In the DLTS spectra of sample B and C featuring a low temperature growth step, the broad interface-states related shoulder is reduced in comparison to sample A, grown continuously at high temperature. Therefore, less thermal budget in the beginning of the AlN growth seems to improve the AlN/Si interface quality in terms of a reduced amount of interface states. The high density of deep-level defects present in the near interface region and the observed interface states could be one reason for the early breakdown of GaN-based power devices integrated on Si(111) [115].

The apparent activation energy E_A and capture cross-section σ_p of the measured hole traps are estimated from Arrhenius plots. Here, the emission time constant is calculated from the peak maximum of several coefficients versus temperature plots with equal period width [37, 38].

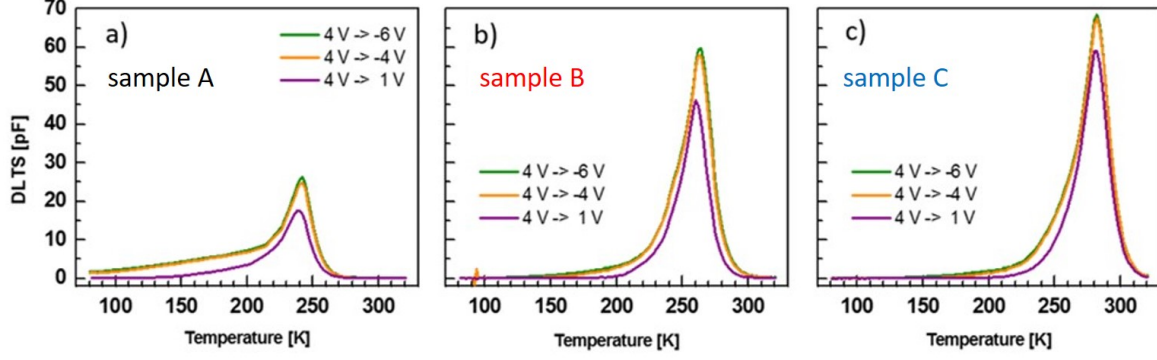


Figure 3.10: Temperature scan DLTS of different bias pulses for (a) sample A, (b) sample B and (c) sample C.

The estimated parameters for samples A-C are listed in table 3.3. The activation energies of the observed hole trap are around mid-gap position of all three samples, whereby their exact position tends to depend on the thermal budget, as already indicated by frequency scans at room temperature in fig. 3.8. While the hole trap in sample A, exhibiting a constant thermal budget above 1000 °C, shows an activation energy of 0.44 eV above the valence band edge, the hole traps are located at 0.46 eV and 0.63 eV when a low temperature step is applied at < 1000 °C and < 900 °C, respectively. A similar behavior is found for the measured capture cross-sections. For the bulk defect in sample A and B capture cross-sections of $5 \times 10^{-17} \text{ cm}^{-2}$ and $2 \times 10^{-17} \text{ cm}^{-2}$ are derived, respectively. With a capture cross section of $4 \times 10^{-15} \text{ cm}^{-2}$, the hole trap in sample C, featuring the lowest temperature step, is more attractive in trapping free holes than in sample A and B. The corresponding trap concentrations, also listed in table 3.3, are in the order of 10^{16} cm^{-3} for sample A and 10^{15} cm^{-3} for sample B and C. But, as mentioned above, these values will be underestimated and should be considered as a lower limit for a filling pulse time of 1 ms, since no complete trap filling could be observed.

sample	low T step	activation energy	hole capture	trap density
		E_A	cross section σ_p	N_T
A	non	0.435 eV	$4.75 \times 10^{-17} \text{ cm}^{-2}$	$5.75 \times 10^{16} \text{ cm}^{-3}$
B	< 50 nm @ < 1000 °C	0.455 eV	$1.63 \times 10^{-17} \text{ cm}^{-2}$	$3.42 \times 10^{15} \text{ cm}^{-3}$
C	< 50 nm @ < 900 °C	0.629 eV	$4.38 \times 10^{-15} \text{ cm}^{-2}$	$4.16 \times 10^{16} \text{ cm}^{-3}$

Table 3.3: Trap parameter evaluated from Arrhenius plots of emission time constant vs $1/T$.

Although the hole trap parameters are characterized by temperature dependent DLTS measurements, their origin is open to discussion. According to the diffusion mechanism of impurity atoms, in-diffused Al atoms may force kick-out events of Si atoms from lattice sites by creating self-interstitial point defects [115, 124]. Assuming a formation of these point defects during cooling down from AlN growth temperature, a clustering may take place to release the high thermal stress, which builds up when the temperature decreases [115]. Hence, the observed trap level at mid-gap in this work can be attributed to clusters of point defects that are large enough to behave like extended defects [115]. Similar observations were made in

DLTS studies of Si ion-implanted Si, where Si interstitial (Si_i) clusters are correlated with a hole trap at $E_V + 0.50$ eV, exhibiting a logarithmic rather than exponential capture kinetics [35]. By increasing the ion flux and annealing temperature, a transition from point defects to defect clusters and extended defects was noticed [126]. In addition, Si self-interstitials are able to replace substitutional boron dopants by forming interstitial boron (B_i), which tends to generate boron-interstitial clusters (BICs), since the interstitial boron atoms are highly mobile [115]. Moreover, it is reported that complexes of Al and oxygen (Al-O) create hole traps in the range of 0.38 - 0.5 eV above E_V , which are believed to reduce the minority-carrier lifetime in Al-doped Si [114, 127]. As a result of altering activation energies as well as hole capture cross-sections determined in the investigated samples with and without a low temperature-growth step of various temperatures, the responsible defects could be of a different nature.

3.3.4 Structural limitations

As indicated in the previous sections, the electrical characterization of MIS structures by C-V and DLTS is very sensitive to the device properties themselves, including the insulator and interface quality. Structural investigations of the AlN/Si structures by secondary electron microscopy (SEM) showed an agglomeration of pits on the AlN surface, which may run through the whole AlN layer, indicating a columnar growth of this layer. The top-view SEM images are displayed in fig. 3.11. Here, the pits on the AlN surface become denser and increase in size by introducing the low-temperature growth step and also by reducing the temperature of this step. According to literature, an AlN seed layer grown at low temperatures results in non-stoichiometric composition and a higher density of imperfections in the layer [103]. This could be responsible for measuring different values of the insulator capacitance, where charges inside the insulator have to be considered, too. Further, surface pits are favorable to current flow, probably resulting in parasitic leakage [128] and, therefore a low parallel resistance component that may dominate the impedance of the capacitor.

In addition, the consideration of the quality factor in the investigated MIS devices limits the range of Si resistivity that can be measured in a proper way. Here, the total series resistance of the structure including the AlN layer as dielectric and the Si substrate must be considered. By using high resistivity samples, the series resistance becomes too high, resulting in insufficient quality factors. Similar problems appear when low resistivity substrates are used for investigation, since only a certain number of free carriers can be depleted. Literature studies have shown that the variation within a wafer of vertical-direction breakdown voltages in GaN-on-Si HEMTs correlates with the AlN nucleation layer growth conditions and decreases as the pit density and their maximum size decrease [113]. The comparison of low and high temperature growth showed an optimal surface morphology at a growth temperature of the AlN nucleation layer at 1030 °C featuring reduced vertical breakdown voltages of GaN-on-Si high power devices [128].

3. Defect related vertical breakdown in AlGa_N/Ga_N HEMTs integrated on Si(111)

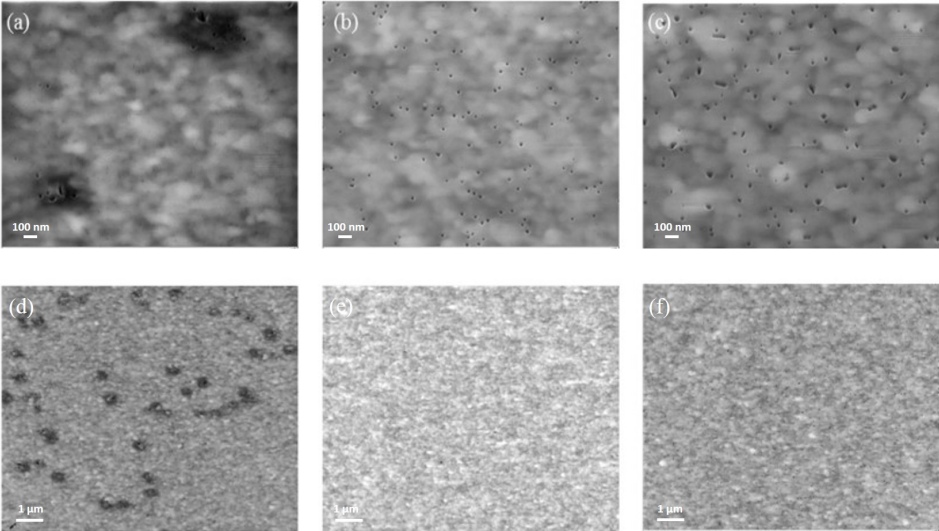


Figure 3.11: Top-view SEM images in two different magnifications of (a) sample A, (b) sample B and (c) sample C.

3.4 Conclusion

I investigated the impact of a low temperature growth step during the initial AlN growth for GaN-on-Si HEMT structures. Two different temperatures for this growth step prior to the final growth temperature were probed and compared to a commonly applied continuous high growth temperature. In order to examine the electrical active defects, AlN/Si MIS capacitors were fabricated and characterized by C-V and DLTS measurements.

The investigated AlN/Si MIS capacitors show a bulk hole trap inside the Si substrate at midgap position and interface states at the AlN/Si interface as already observed in literature [114, 115, 116, 117]. The hole traps are supposed to be related to either self-interstitial clusters or Al complexes that are both efficient G-R centers, based on their position at mid-gap [114, 115]. These G-R centers in the Si substrate as well as the generation at the surface through interface states can contribute to parasitic leakage currents in GaN HEMTs and, are therefore a potential source for early vertical breakdown when those devices are integrated on Si substrates [128, 113].

The insertion of a low-temperature growth step of either < 1000 °C or < 900 °C prevents a deeper in-diffusion of Al atoms into the Si substrate, while in the vicinity of the AlN/Si interface a slightly higher amount of additional p-doping is found than in the sample grown without a low temperature step. Furthermore, the density of deep bulk traps appears to be higher in samples featuring a low temperature growth step. In contrast, the signal coming from surface states at the AlN/Si interface in DLTS spectra decreases when a low temperature growth step is applied, in contrast to AlN layers grown at continuous high temperatures. In addition, growing AlN with a low temperature step of < 900 °C reduces the hole capture cross-section by two orders of magnitude, therefore it may be concluded that these traps are not as efficient as layers grown at higher temperatures.

However, the columnar growth of AlN on Si(111) results in MIS devices, showing a considerable amount of leakage currents through the insulator. Such leaky devices lead to low quality factors in capacitance-based measurements, and it might therefore be deduced that the fabricated MIS capacitors are not ideal for electrical characterization. Nonetheless, based on the insulating behavior of the wide-bandgap material AlN, no other device structure can be applied to comprehensively study electrical active defects that contribute to vertical breakdowns in GaN-on-Si HEMTs.

3.5 Outlook

In order to assess the impact of the low temperature growth step of the AlN nucleation layer investigated in this work on final AlGaIn/GaN HEMT devices integrated on Si, a correlation with corresponding breakdown voltages would be beneficial. Therefore, a subsequent growth of the AlGaIn buffer and the AlGaIn/GaN active material will be needed as well as the fabrication of an ohmic electrode on top for measuring the vertical leakage current through the whole heterostructure.

In addition, making changes to the Si substrate may help to identify the defects responsible for the observed deep traps in the Si substrate. In order to artificially increase the Si self-interstitial point defects responsible for Si_i and B_i cluster formation, the Si substrate could be treated by ion implantation prior to the AlN nucleation layer deposition. To verify Al-O complexes as origin, different qualities of the Si substrate in terms of oxygen contamination could be applied, for instance by comparing Si substrates made by Czochralski or float-zone. Then, reasonable assumptions about the defect origin could be made by making comparisons of the defect properties measured in this work and in additional samples fabricated on the modified Si substrates with similar AlN nucleation layers to those in this study.

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