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Radiation-Tolerant All-Digital Clock Generators for High Energy Physics

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PhD Thesis

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Dissertation presented in partial fulfillment of the requirements for the degree of Doctor of Engineering Technology (PhD) to the Arenberg Doctoral School at KU Leuven.

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Abstract

Eine Zusammenfassung in deutscher Sprache findet sich im nächsten Abschnitt.
The main focus of the presented research is the development and experimental study of radiation-tolerant clock generation circuits intended for applications in high energy physics (HEP). Clock synthesis and the synchronization of systems on the scale of large experimental detectors is an important aspect of their successful implementation and a necessity for achieving their anticipated performance. Both current and next generation electronics for high energy physics impose significantly tighter requirements on clock generation and distribution, motivating further developments in this area to increase reliability and performance. Even though the adoption of highly scaled CMOS technology nodes generally tends to increase the radiation tolerance of electronics, this scaling comes at the cost of introducing a number of challenges into the circuit design process.

Following an introduction of the necessary background and relevant references, the thesis reviews the requirements of existing and emerging systems with regards to radiation-tolerant clock generation. To characterize clock generation circuits and adequately assess their conformity with the identified requirements in radiation tests, a number of methods and instrumentation setups are developed and characterized. The presented approaches combine aspects of digital programmable logic, analog circuit design and and digital signal processing concepts to overcome major limitations of the state of the art in single-event effects testing.

To address the manifold design challenges arising with the adoption of deep submicron CMOS nodes, in particular their aggressive supply voltage scaling, the design and implementation of radiation-tolerant all-digital phase-locked loop (PLL) and clock and data recovery (CDR) circuits is explored in this thesis. The main challenges of reduced voltage swing and limited signal-to-noise ratio are overcome in these circuits by digital representation of traditionally analog quantities, and the use of digital signal processing over analog circuit techniques. These circuits also promise large opportunities to improve the radiation tolerance of clock generator implementations, and hence this thesis

devises the design of a radiation-tolerant all-digital PLL and CDR circuit compatible with contemporary systems requirements of high energy physics (HEP) electronics. Using extensive radiation testing, the sensitivity of the implemented circuits is studied and mitigation strategies for the identified shortcomings are discussed. In total, three such all-digital phase-locked loop (ADPLL) circuits are developed and tested in the form of macro blocks targeting typical applications in frontend application specific integrated circuits (ASICs) for high energy physics. The circuits demonstrate jitter performance, power efficiency and radiation tolerance comparable or improved with respect to the currently used conventional PLL circuits. They further significantly reduce the required circuit area, even though an extensive radiation hardening approach based on triple modular redundancy (TMR) is adopted.

As a final aspect, the improved testing instrumentation and methodology developed within this thesis is applied to uncover a previously unrecognized radiation sensitivity in a conventional, radiation-hardened clock generator circuit. The planar on-chip inductor used within the integrated LC oscillator is identified as the circuit component responsible for this sensitivity through a number of dedicated experiments. Two-photon laser testing, heavy ion and proton irradiation tests are performed to further study and characterize the nature of the discovered sensitivity. The experimental results suggest that energy deposition, most likely within the dielectric materials surrounding the inductor wiring, temporarily alters the impedance of on-chip inductors. This stimulates transient frequency errors with long recovery times in the LC oscillator circuit. The practical manifestation of this effect in typical high energy physics radiation environments is studied using a proton irradiation test, where a mitigation strategy is experimentally validated. A significant reduction of the impact of this sensitivity is demonstrated by increasing the PLL bandwidth of the clock generator circuit. To help conclusively identifying the underlying mechanism responsible for the sensitivity within the inductor itself, further research opportunities are suggested.

Zusammenfassung

Die vorgelegte Dissertation befasst sich mit der Entwicklung und der experimentellen Untersuchung strahlungstoleranter und hochzuverlässiger Takterzeugungsschaltungen für Anwendungen in der Hochenergiephysik. Die Sychronisation von Komponenten und Systemen im Maßstab großer Detektorexperimente mithilfe solcher Schaltungen ist von zentraler Bedeutung für deren erfolgreiche Implementierung und das Erreichen der spezifizierten Leistungsparameter. Die Konzeption von aktuellen sowie zukünftigen Detektorgenerationen erfordern das Erreichen von zunehmend strikteren Anforderungen an Takterzeugung und -verteilung. Dies motiviert im Kern die vorgestellte Forschungsarbeit, die darauf abzielt, die Zuverlässigkeit und Leistungsfähigkeit solcher Schaltungen weiter zu erhöhen. Obwohl die zunehmende Verwendung neuer, fortschrittlicher CMOS-Prozesse in diesem Anwendungsbereich einerseits die Resistenz integrierter Schaltungen gegenüber kumulativen Effekten ionisierender Strahlung und damit deren Langzeitzuverlässigkeit signifikant verbessert, so bringen diese Prozesstechnologien auch eine Zahl neuer Herausforderungen für den Entwicklungsprozess mit sich, mit denen sich diese Arbeit konfrontiert sieht.

Nach einer Einführung einiger Grundlagen sowie relevanten Literaturstellen beschäftigt sich der erste Teil der Arbeit mit der Zusammenfassung und Einordnung von Anforderungen aktueller und zukünftiger Detektor- und Datenkommunikationssysteme für Teilchenphysikexperimente. Aus diesen werden konkrete Anforderungen für integrierte Schaltungen zum Zwecke der Takterzeugung und -verteilung in diesen Anwendungsbereichen abgeleitet. In diesem ersten Teil der Arbeit werden zudem drei komplementäre Methoden und Instrumentationskonzepte für Charakterisierungs- und Qualifikationsaufgaben solcher Schaltungen vorgestellt, um die Einhaltung der durch die Anwendung gegebenen Anforderungen in Strahlungstests zu überprüfen. Die drei präsentierten Konzepte entstanden dazu mit dem Ziel, bestehende Beschränkungen des aktuellen Standes der Technik aufzuheben. Die dazu verfolgten Ansätze kombinieren Aspekte aus den Bereichen flexibel programmierbarer Logikschaltungen, analoger Schaltungsentwicklung und digitaler Signalverarbeitung.

Eine der größten Herausforderungen für analoge integrierte Schaltungen in

hochintegrierten CMOS-Prozesstechnologien stellt deren aggressive Reduzierung der Versorgungsspannung dar. Diese begrenzt beispielsweise den nutzbaren Signalspannungsbereich, was im Ergebnis zur Verringerung des erreichbaren Signal-Rausch-Abstandes in analogen Schaltungen führt. Als Ansatz zur Bewältigung dieser und weiterer Herausforderungen beschäftigt sich diese Arbeit als zweiten Schwerpunkt mit der Entwicklung von strahlungstoleranten, vollständig digital implementierten Phasenregelschleifen (*engl.* all-digital PLL) für Anwendungen in Beschleunigerexperimenten. Digital implementierte Phasenregelschleifen umgehen diese für analoge Schaltungen großen Einschränkungen systematisch durch die Wandlung und Repräsentation konventionell analoger Größen wie Spannungen und Strömen durch digitale Signale. Die digitale Umsetzung traditionell mit analogen Schaltungen implementierter Funktionalität ermöglicht das Verfolgen von neuen, vielversprechenden Ansätzen zur Strahlungshärtung von Takterzeugungsschaltungen. Auf der Basis dieses aussichtsreichen Eigenschaftenraums präsentiert diese Arbeit ein Konzept zur Implementierung von strahlungstoleranten Phasenregelschleifen für Takterzeugungs- (PLL) sowie Takt- und Datenrückgewinnungsaufgaben (CDR). Die drei aus diesem Konzept entwickelten Testschaltungen sind so ausgelegt, dass sie dem Anforderungsprofil typischer Front-End-Schaltkreise entsprechen und daher einen guten Vergleichspunkt zu aktuell verfügbaren Lösungen bieten können. Durch ausführliche Strahlungstests und mithilfe der zuvor entwickelten Messtechnik wird die erreichte Resistenz gegenüber Strahlungseffekten konkret bewertet und die Ursachen für die Restempfindlichkeit der getesteten Schaltungen diskutiert. Alle drei Schaltungen demonstrieren dabei in der Praxis mit konventionellen, strahlungstoleranten Phasenregelschleifen vergleichbare Taktqualität und Energieeffizienz sowie hohe Toleranz gegenüber kumulativen sowie transienten Strahlungseffekten. Durch die optimale Nutzung der Eigenschaften moderner CMOS-Technologien bieten die vorgestellten Schaltungen jedoch den zusätzlichen Vorteil, dass die für die Implementierung notwendige Chipfläche deutlich reduziert wird, selbst wenn umfangreiche Maßnahmen zur Erhöhung der Strahlungstoleranz auf der Basis dreifach modularer Redundanz (*engl.* triple modular redundancy, TMR) in allen digitalen Schaltungsteilen umgesetzt werden.

Als letzten Aspekt beschäftigt sich die Arbeit mit einer neuartigen Klasse von transienten Strahlungseffekten in Takterzeugungsschaltungen. Der erstmalige Nachweis sowie das Erkennen der praktischen Relevanz dieses Strahlungseffektes für Systeme mit hohen Genauigkeitsanforderungen wurde dabei erst durch die im ersten Teil der Arbeit durchgeführte Entwicklung verbesserter Messverfahren ermöglicht. On-Chip-Induktivitäten wurden hierbei als strahlungsempfindliche Schaltungskomponente innerhalb eines LC-Oszillators identifiziert. Mithilfe von Experimenten an Laser- und Schwerionenbeschleunigeranlagen wurden Untersuchungen zur Charakterisierung dieses Strahlungseffektes durchgeführt. Mithilfe dieser konnte gezeigt werden, dass die Deposition von Energie innerhalb der emp-

findlichen Komponente zu einer temporären Änderung ihrer Impedanz führt, was die Schwingfrequenz des untersuchten Oszillators messbar beeinflusst. Während primär eine metallische Struktur für die Herstellung solcher Induktivitäten verwendet wird, legen die Ergebnisse der durchgeführten Tests nahe, dass der beobachtete Effekt seinen Ursprung in den dielektrisch wirksamen Materialien in der direkten Umgebung dieser Struktur hat. Die praktische Relevanz dieses Effektes in einer für Hochenergiephysik repräsentativen Strahlungsumgebung wurde weiterhin mithilfe eines Strahlentests mit Protonenstrahlung untersucht. Als eine wirksame Maßnahme zur Unterdrückung des untersuchten Effektes auf ein akzeptables Maß wurde dabei die Erhöhung der Schleifenbandbreite der in der Takterzeugerschaltung verwendeten Phasenregelschleife identifiziert. Abschließend werden zu diesem Themenschwerpunkt weitere zu untersuchende Aspekte herausgearbeitet, mithile derer eine vollständige Erklärung des beobachteten Strahlungseffektes und der ihm zu Grunde liegenden Mechanismen im Bereich der Halbleiterphysik angestrebt wird.

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Contents

List of Abbreviations

ΣΔM	sigma-delta modulator
ADC	analog-to-digital converter
ADPLL	all-digital phase-locked loop
AM	amplitude modulation
API	application programming interface
ASIC	application specific integrated circuit
BBADPLL	bang-bang all-digital phase locked loop
BBPD	bang-bang phase detector
BBPLL	bang-bang phase locked loop
BEOL	back-end of line
C^2MOS	clocked-CMOS
CDR	clock and data recovery
CERN	Conseil Européen pour la Recherche Nucléaire
CML	current-mode logic
CMOS	complementary metal oxide semiconductor
CP	charge pump
CVD	chemical vapor deposition
DAC	digital-to-analog converter
DAQ	data acquisition
DC	direct current
DCO	digitally controlled oscillator
DCRO	digitally controlled ring oscillator
DD	displacement damage
DICE	double interlocked cell
DLF	digital loop filter

DLL	delay-locked loop
DMM	digital multimeter
DNL	differential nonlinearity
DSO	digital storage oscilloscope
DSP	digital signal processing
DTC	digital-to-time converter
DUT	device under test
EDA	electronic design automation
EHP	electron-hole pair
ELT	enclosed layout transistor
FDIR	fault detection, isolation, and recovery
FIR	finite impulse response
FM	frequency modulation
FOM	figure of merit
FPGA	field-programmable gate array
FTW	frequency tuning word
FWHM	full width half maximum
HDL	hardware description language
HEP	high energy physics
HGCal	High Granularity Calorimeter
HGTD	High Granularity Timing Detector
HL-LHC	High Luminosity Large Hadron Collider
I/O	input/output
I^2C	Inter-Integrated Circuit
IF	intermediate frequency
INL	integral nonlinearity
IP	intellectual property
ISF	impulse sensitivity function
LET	linear energy transfer
LF	loop filter
LGAD	low gain avalanche detector
LHC	Large Hadron Collider
LO	local oscillator
lpGBT	Low Power Gigabit Transceiver
LSB	least significant bit

MBU	multi-bit upset
MOM	metal-oxide-metal
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field effect transistor
MSB	most significant bit
MTD	MIP Timing Detector
NMF	noise modulating function
NOCG	non-overlapping clock generator
NRZ	non-return-to-zero
OC	Optical Carrier
P&R	place and route
PAM	pulse-amplitude modulation
PCB	printed circuit board
PFD	phase-frequency detector
PGS	patterned ground shield
PI	proportional-integral
PLL	phase-locked loop
PM	phase modulation
PPA	power-performance-area
PVT	process, voltage and temperature
RDUC	resistively decoupled unit cell
RF	radio frequency
RHBD	radiation-hardened-by-design
RTL	register-transfer level
SDR	software-defined radio
SEE	single-event effect
SEFT	single-event frequency transient
SEL	single-event latch-up
SEPT	single-event phase transient
SET	single-event transient
SEU	single-event upset
SNR	signal-to-noise ratio
SONET	Synchronous Optical Networking
SPICE	Simulation Program with Integrated Circuit Emphasis

STA	static timing analysis
STI	shallow trench isolation
TDC	time-to-digital converter
TID	total ionizing dose
TMR	triple modular redundancy
ToA	time of arrival
ToT	time over threshold
TPA	two-photon absorption
TTC	timing, trigger and control
USB	Univeral Serial Bus
VCO	voltage-controlled oscillator
VOLK	Vector Optimized Library of Kernels

Chapter 1

Introduction

In a world increasingly dominated by digital electronics, the importance of clock generation and conditioning circuits has increased rapidly over the past decades. Almost any imaginable contemporary development follows the design trends of adopting more advanced CMOS design nodes, which allows digital circuits to operate at higher speeds. This increase in operation frequency continues to drive the performance requirements for the clock generation and conditioning circuits forming the heart of most digital circuits. As mainstream commercial applications continue to push the envelope, specialized applications tend to adapt and follow the same technology trends. This thesis is concerned with clock generation circuits in the domain of harsh environments containing ionizing radiation, in particular high energy physics experiments. This first chapter will introduce some of the challenges faced by these circuits when operating in adverse conditions, with a particular focus on radiation environments.

1.1 Clock Synthesis in Harsh Environments

Due to the central role of clock synthesis and conditioning in the majority of electronics systems, clock synthesizer circuits have also found their way into the harshest environments. The adverse conditions of such environments are not limited to the radiation effects that are central to the work in this thesis, but instead might be mechanical stress, vibrations, extreme temperatures, strong magnetic fields, electromagnetic interference or very high or low ambient pressure. Common to any such application is an increased demand for high operational reliability of circuits, either due to criticality of correct operation or because of limited serviceability of the involved components. Perhaps the most well-known example of such an environment is found in the domain of spaceflight. In addition to being exposed to wildly varying environmental conditions (extreme

vibrations during spacecraft launch, large temperature swings depending on solar exposure, operation in the vacuum of space), circuits also need to deal with an adverse radiation environment. Since reliable clock signal generation is crucial for correct operation of high-speed digital and radio frequency (RF) circuits, high reliability of any circuitry involved in the clock generation process is important. The inability to service malfunctioning spacecraft at vast distances from Earth additionally introduces constraints on the autonomy of such circuits, such as a need for automated fault detection, isolation, and recovery (FDIR) techniques. None of these challenges are unique to spaceflight, but can be found in a number of terrestrial applications as well.

Recent years saw an emergence of high-speed optical communications standards for on-satellite data links in the form of SpaceFibre [1]. At the same time, the carrier frequency and bandwidth of RF and millimeter wave communications links continues to increase, creating demand for reliable high performance clock synthesizers in the form of PLL and CDR circuits. These developments illustrate the gradual adoption of advanced technological developments in applications with demanding operational environments.

1.2 Clock Generator Circuits for HEP Experiments

This thesis focuses on the application domain of high energy physics particle collider experiments. Since at least the beginning of the Large Hadron Collider (LHC) era, such facilities have evolved into large experimental complexes. One particularity of these complex systems is their highly synchronous nature: In order to reliably attribute individual observed physics events to a given particle bunch crossing in a traceable manner, the experiments, their detectors, as well as their individual subdetectors require precise synchronization to a common clock source also driving the accelerator operations. In practice, this synchronization is accomplished through multiple layers of timing and data distribution networks involving PLL and CDR circuits [2, 3, 4]. In the LHC, the most significant timing signal in this regard is the bunch crossing clock of approximately 40.079 MHz. This signal, as the name suggests, establishes the time base for collisions of particle bunches in any of the interaction regions of the accelerator. A conceptual representation of the clock and data distribution architecture typical for LHC experiments is shown in Figure 1.1. Accelerator timing information is provided from the LHC machine to a central location in each experiment using the TTCmi (timing, trigger and control (TTC) machine interface). Timing information and trigger data are distributed from this point to the individual subdetectors using optical links. From there, recovered clock signals are often further distributed, potentially through a number of additional hierarchical layers before finally

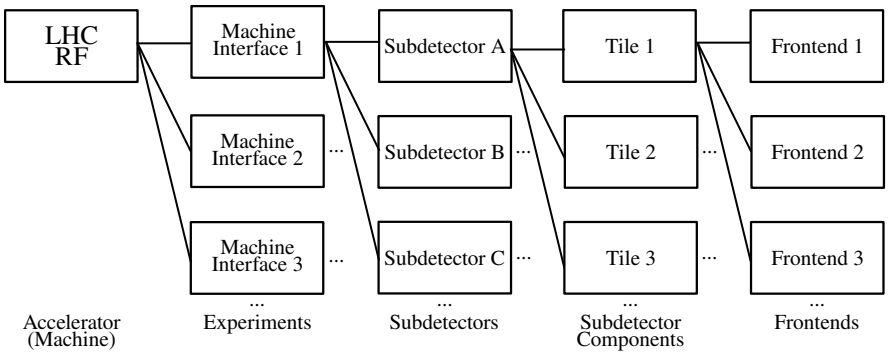


Figure 1.1: Clock distribution architecture in high energy physics experimental complexes.

reaching a number of front-end ASICs. Synchronicity of the timing information provided to each of the leaf nodes needs to be guaranteed, stable and repeatable, even when distribution distances exceed many kilometers and thousands of such nodes are involved.

The reasons for using clock generator circuits such as PLLs and CDRs to accomplish these synchronization tasks are manifold: Firstly, in multi-level clock distribution networks, signal quality tends to degrade. PLL circuits can, to a certain extent, counteract this tendency by locally generating a replica of a given reference clock. This regenerative approach can eliminate or at least limit the amount of degradation accumulated through multiple layers of distribution. Additionally, integer multiples of the provided bunch crossing clock frequency are required in many systems. Applications for such signals range from the analog-to-digital and time-to-digital conversion processes in detector front-ends to the serialization of detector data at high data rates across optical and electrical data links. PLL-based clock generators are often used in these applications, since they can be designed to include the required frequency multiplication capabilities while providing the necessary synchronization. Lastly, instead of individually distributing clock and data signals from the back-end to the detector front-ends, many systems (including the LHC timing and trigger distribution network) instead distribute timing information and data on one common high-speed serial link. These systems require CDR circuits on the receiving end to once again separate the clock and data information by recovering the timing information embedded in the data stream and then extracting the transmitted data.

The reliability of such circuits is severely challenged by the radiation environment in which they operate: The products resulting from the primary

particle collisions are not confined to the active sensor regions in which they are converted into useful signals. Instead, they also penetrate and interact with the integrated circuits comprising the readout electronics. In these, they become the source of a number of detrimental radiation effects. One one hand, the accumulation of large radiation doses over the extended operation periods of experiments result in significant degradation of electronics performance on timescales of months or years. At the same time, short-lived transient radiation effects can at any time disrupt the correct operation of circuits temporarily. While some applications can tolerate a certain amount of data corruption, the critical role of clock generation circuits necessitates striving for the highest levels of robustness. The correct operation of digital circuits crucially depends on the uninterrupted availability of clock signals with well-defined properties. Even temporary disruptions may have catastrophic consequences, potentially resulting in loss of circuit functionality. Since clock signals are often distributed along multiple levels of system hierarchy, a single clock source might drive hundreds or thousands of downstream circuits. Clocking therefore presents a critical single point of failure in large systems. This criticality continues to hold also on smaller scales. Considering the case of a single integrated circuit used inside a larger system, a single local clock generator circuit is often the root node of all on-chip clock distribution networks, driving thousands of sequential logic cells. This number is only going to increase with the unavoidable adoption of more advanced integrated circuit technologies and the increasing complexity of circuits and systems. Since the challenging radiation environment does fundamentally rule out practical use of commercial circuits, detectors for HEP experiments have for a long time adopted the design of custom, radiation-tolerant ASICs.

1.3 Research Motivation

As evident from the previous discussion, reliable clock synthesis and timing distribution are already key considerations in the design of high performance detectors in HEP. Synchronous clocking architectures are used throughout these systems to drive data converters, data processing circuits and data links. While the systems developed for the upcoming high-luminosity upgrade of the LHC have made tremendous advances in increasing the reliability of clock synthesis and distribution, keeping up with the technological developments as well as the changing physics detector landscape will require continued developments in this field.

One of the most significant developments in this area is the advent of timing detectors. The higher number of simultaneous particle collisions resulting from increased luminosity result in more events to be detected and processed by detectors. To individually resolve and differentiate this increased number of events, detectors are starting to further exploit the time domain. While

previous system generations typically operated with a time resolution not much better than a single bunch-crossing (25 ns), such timing detectors instead aim to discriminate events separated in time by only tens or hundreds of picoseconds within a single bunch crossing [5, 6].

The introduction of these detectors was a key consideration in motivating the need for improvements in the performance of PLL and CDR circuits in recent years. Clearly, future detector generations will strive to further increase this time resolution. At the same time, this exploitation of an additional dimension creates a demand for even higher data rates in the high-speed optical data links connecting detector systems to their processing and storage back-ends [7]. This will undoubtedly cause high-speed optical links to become another key driver for the performance of PLL and CDR circuits operating in the increasingly harsh radiation environment of future collider experiments. Successful adoption of advanced CMOS technologies will be one of the key factors in these developments, promising increased radiation tolerance combined with an increase of speed and design density while also achieving a reduction of power consumption.

Even though the adoption of more advanced CMOS technology nodes comes with many beneficial properties, it also comes at a cost. First and foremost, the associated supply voltage reduction limits the performance of most analog circuits. In mainstream commercial applications, a clear trend of replacing traditionally analog circuits by fully-digital or digitally-assisted architectures has emerged. The domain of frequency synthesizer circuits is significantly affected by this issue and the conception of all-digital architectures for PLL and CDR circuits has strongly influenced modern commercial developments. Leveraging these developments and applying them to the domain of radiation-tolerant electronics is one key aspect motivating the work on this thesis. Their successful adoption will offer a strategy to meet the demands of future HEP detectors by increasing performance while facing the challenges of technology scaling.

1.4 Thesis Objectives

Keeping up with diverse, changing and ever-tightening requirements for clock generation circuits in HEP electronics presented above can be formulated as the main objective of this thesis. Motivated by the various challenges faced by clock synthesis and distribution circuits for future accelerator experiments, three sub-objectives in separate aspects of the field are identified and addressed by the presented work.

Instrumentation for radiation-tolerant clock synthesis circuits

The thesis identifies a clear gap between the requirements of next-generation radiation-tolerant frequency synthesizers and the existing methods and instru-

mentation available for their characterization in radiation tests. The work aims to close this gap by proposing three complementary approaches for detecting, characterizing and researching radiation effects in time processing circuits. Achieving this first objective can be considered a foundational effort for the subsequent research: Aligning the capabilities for detection and characterization of radiation effects with the requirements of current and future circuits is a necessary precondition to establish, and as such makes addressing the identified shortcomings of the state of the art an important aspect of the work.

Radiation-tolerant implementation of all-digital PLL circuits

A second objective is concerned with addressing the challenges posed by adopting increasingly advanced technology nodes for the electronics of HEP experiments. Especially the continuing supply voltage reduction and the associated degradation of analog circuit performance in advanced deep sub-micron CMOS nodes strongly motivate the exploration of all-digital circuit architectures for clock generation. The concept of all-digital PLL circuits as a solution to this issue is well-established in commercial applications, and this thesis explores radiation-tolerant implementations of these circuits. The feasibility of a radiation-tolerant ADPLL compatible with the requirements of contemporary HEP electronics will be demonstrated within this objective. Experimental characterization results of the implemented circuits will be presented, paving the road to widespread adoption in future generations of radiation-tolerant ASICs.

Research of radiation effects in passive integrated circuit structures

The third objective is concerned with an experimental study of a novel radiation response identified in passive structures crucial for the implementation of high frequency oscillator circuits. To obtain a better understanding of this radiation effect, multiple experiments are conducted on conventional and all-digital PLL circuits and the LC oscillators they integrate. The results obtained from these experiments provide the basis for further studies in the domain of semiconductor and insulator radiation effects studies. Thoroughly characterizing the nature of this fundamental sensitivity contributes to the ultimate goal of improving the radiation tolerance of clock synthesizer circuits by enabling the development of adequate mitigation strategies in the future.

1.5 Overview of the Thesis

The structure of the thesis closely follows the objectives set out in the previous section. The following chapter 2 will discuss the background necessary to give the reader an understanding of the subject matter discussed afterwards.

Chapter 3 describes the work on the first objective beginning from the crucial instrumentation requirements for radiation effects qualification of clock generator circuits. It goes on to present the different developed instrumentation setups. Chapter 4 and chapter 5 relate to the second objective. While chapter 4 focuses on the design and simulation of a radiation-tolerant all-digital PLL implementation, chapter 5 presents and discusses the results experimentally obtained using the designed and manufactured circuits. Chapter 6 discusses aspects of the research relevant to the third objective. In this chapter, the different experimental setups and methodologies for characterizing a newly discovered radiation effect in planar on-chip inductors are described and the obtained results are subsequently discussed. Finally, chapter 7 presents a summary of the work as well as major conclusions. This final chapter also contextualizes these results, discusses their impact on current and future developments in HEP electronics and suggests a number of open questions and perspectives for follow-up research in this area.

Chapter 2

Background

This chapter reviews a number of concepts useful in understanding the work presented in this thesis. Since the thesis is concerned with radiation-tolerant implementations of clock generator and frequency synthesizer circuits, this chapter is structured accordingly. First, foundations relating to radiation effects in integrated circuits are summarized. Initially without a particular focus on radiation hardening efforts, some basic concepts regarding frequency synthesis are presented afterwards. Subsequently, a connection between these two subjects is established by reviewing a number of radiation sensitivities in frequency synthesizer circuits. Finally, one of the significant mitigation approaches for one large class of radiation effects in digital circuits is reviewed, to provide the reader with context for the design decisions taken in chapter 4.

2.1 Radiation Effects in Deep-Submicron CMOS Circuits

Integrated circuits manufactured using advanced CMOS fabrication processes currently represent the majority of electronics operating in the radiation environments of particle accelerator facilities such as the LHC. Generally speaking, the effects arising from the interaction of such circuits with particle radiation are usefully classified as either total ionizing dose (TID) effects, displacement damage (DD), or single-event effect (SEE) [8, p. 2]. For the topics discussed in this thesis, only total ionizing dose (TID) and single-event effect (SEE) are relevant and will be briefly summarized below. A discussion of displacement damage (DD) will be omitted, since its effects are dominant only in devices relying on bulk semiconductor properties, such as bipolar transistors or solar cells, but less so in typical CMOS device structures [8, p. 16].

2.1.1 Single-Event Effects

The term single-event effect (SEE) is used to describe radiation effects that originate from the passage of a single ionizing particle through a sensitive region of a microelectronic device [8, p. 16]. Owing to the complexity of potentially affected circuits themselves as well as the variety of mechanisms triggered during the interaction, such events can be extremely varied in nature, and are technically not limited in scope to active CMOS devices.

Most commonly known manifestations of these effects allow for a further distinction between soft and hard SEEs. While soft errors are associated with a temporary loss or corruption of information, events involving a destruction of devices which results in permanent loss of functionality are referred to as hard errors. One circumstance that sometimes complicates this distinction is that certain types of hard errors may only occur in case remedying action (such as removal of the power supply voltage) is not taken before permanent damage of a device occurs as a result of a soft error [8, p. 16].

For modern CMOS technologies and outside of the domain of power electronics, hard SEEs are somewhat less of a concern, since technology-related effects such as latch-up readily occur also outside of radiation environments and are therefore typically already mitigated conceptually to a large extent during the design phase of circuits. Instead, soft SEEs present the largest sensitivity that remains to be acknowledged, characterized and mitigated by the circuit designer. In the design of digital circuits, the most basic manifestation of a SEE is the corruption of a data bit stored inside a memory cell, called a single-event upset (SEU). Single-event transients (SETs) on the other hand describe events manifesting as a temporary deviation of a voltage or current from its nominal value, often as a result of charge collection in a sensitive node following a particle interaction. While SETs can affect both analog and digital circuits, in particular for digital circuits these events also pose a risk of being converted into SEUs. A transient occurring in a combinatorial logic cell may be latched by a following memory element, corrupting the data that was supposed to be stored. Clearly, also more complex logic trees suffer from this type of fault propagation, which may potentially lead to catastrophic malfunction of circuits and systems. Another issue arising from technology scaling is the possibility of a single particle interaction impacting the operation of more than one device or memory cell at the same time, potentially resulting in a multi-bit upset (MBU) event [8, p. 144].

Since complete mitigation of such effects is not always possible (one possible approach and a number of the associated trade-offs will be presented in section 2.4), an important aspect of radiation-tolerant circuit design is the estimation of SEE rates in a given radiation environment. A metric useful for this purpose is the single event effect cross section, denoted by σ. When obtained experimentally, this quantity is defined as the number of observed events during

irradiation divided by the particle fluence with which the device is tested. This cross section, which captures the probability of a single particle triggering a given SEE response in a device, is a function of the energy transferred from the incident particles to the sensitive geometry during its passage. It is thus useful to experimentally determine this cross section for a range of such values. The amount of energy transfer along a particle path is usefully quantified using linear energy transfer (LET), typically expressed in units of $\mathrm{MeV\,cm^2\,mg^{-1}}$. This quantity is calculated from the energy loss per unit length in a target material divided by its density [8, p. 17].

It is often found that the dependence of cross section on linear energy transfer (LET) follows a Weibull cumulative probability distribution. After establishing a good fit between experimental data and such a parametric distribution, the cross section for arbitrary values of LET can be calculated. Based on this data, the rate of events occurring in a given particle environment is readily estimated by determining the cross section of the device at the expected value of LET and multiplication by the expected particle flux [8, p. 18]. This method can also be used to predict the event rate in more complex particle fields, even when the primary particles do not itself produce sufficient ionization, but instead interact only through secondary particles, for example as a result of nuclear interactions. In such environments, the resulting flux and LET distribution from such interactions need to be calculated before the obtained data can be used for prediction of the expected SEE rate. Typically, this process is performed using computational methods such as Monte-Carlo simulations [9, 10]. The demonstrated viability of these methods allows characterizing the SEE sensitivity, and hence the qualification of complex integrated circuits, even when the anticipated radiation environment is not itself available during testing. The described methods for characterization of the SEE sensitivities in circuits are not strictly limited to soft errors. Using the same metrics, cross section estimates for hard errors such as single-event latch-ups (SELs) can be obtained. In contrast to soft errors, they are however more frequently used to ascertain the absence of such events in the foreseen radiation environment during the operational life of the circuit.

2.1.2 Total Ionizing Dose Effects

Total ionizing dose (TID) effects comprise the second relevant class of radiation sensitivity of advanced CMOS integrated circuits. As the name implies, TID quantifies the cumulative amount of energy deposited in a material through processes resulting in ionization. In CMOS devices, ionization results in the creation of defects and a buildup of trapped charge in insulating layers, such as the oxides of metal-oxide-semiconductor structures. As a result of these microscopic changes, the macroscopic device properties of MOSFET devices change. Shifts of the threshold voltage V_{th}, a reduction of transconductance g_m

and an increase of leakage current I_l are typically observed [8, p. 6]. Particularly for older CMOS technologies, the main sensitivity to these effects was located inside the gate dielectric itself. Experimental studies have revealed that a radiation-induced shift of the threshold voltage is proportional to the square of the gate oxide thickness, illustrating the significant improvements obtained through its reduction [11]. Modern CMOS design nodes have consistently reduced the oxide thickness down to the physical limitations, and as such also greatly reduced the TID sensitivity of devices vulnerable to such trapping effects. The limiting factor of advanced technology nodes is now found within auxiliary oxides used for device formation, such as shallow trench isolation (STI) [12]. These oxides are often of lower quality (i.e. they have higher defect concentrations) and can have much larger extent than the gate oxide itself. These oxides tend to form the gate oxide of parasitic MOSFET-like structures, which are irrelevant in devices before irradiation but become the source of parameter shifts as TID accumulates. For example, as trapped charges build up inside these oxides, their threshold voltage shifts significantly and the channel of such parasitic devices can begin conducting current, significantly increasing leakage currents. A popular mitigation strategy for this effect available in most bulk CMOS technologies is the use of enclosed layout transistor (ELT) device geometries, which fully enclose the channel by source and drain regions, such that no parasitic devices involving STI oxides are formed [13].

Crucially, many TID effects in advanced CMOS technologies do not only depend on the temperature during irradiation and annealing (due to the temperature dependence of physical parameters such as carrier mobility), but also strongly depend on the dose rate during irradiation [14]. This confounding factor must be taken into account particularly for accelerated testing, where significantly higher dose rates are used than what would be seen in the final radiation environment. Practically achieving and qualifying for a desired radiation tolerance specification therefore requires a suitable methodology, including appropriate margining, dosimetry and environmental control.

In terms of the circuit-level impact of TID degradation, a number of distinct qualities can be identified. Changes of device characteristics, such as shifts of the threshold voltage, a reduction of drain current capability or the transconductance pose risks to the operating point and small-signal characteristics of analog circuits. Parameters such as the width and length of the channel, the number of gate fingers in segmented devices and the dimensions of adjacent oxides significantly influence the amount of degradation, which may be heavily geometry-dependent [15]. For this reason, circuits that rely on matching between parameters of such devices may degrade more strongly or rapidly during long-term exposure to radiation. Another important concern is the unequal degradation of p-channel and n-channel devices, which can result in further unanticipated shifts of circuit operating points. From the perspective of digital

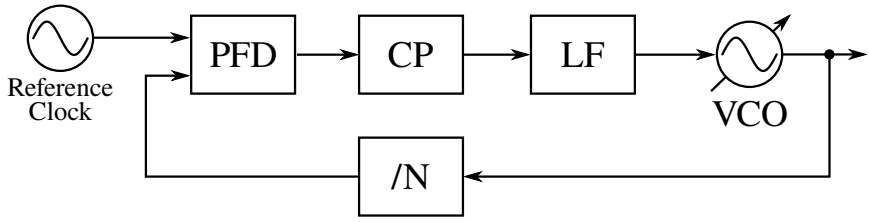


Figure 2.1: Conceptual block diagram of a conventional charge pump PLL

circuit design, a commonly observed impact of TID degradation is a reduction of the maximum operating frequency. As the current capability of devices reduces, the rise times of digital signals deteriorate. In turn, the propagation times of digital logic gates increase, which reduces the available setup margin of digital circuits.

2.2 Phase Locked Loop (PLL) Circuits

PLL circuits are often used to address the ubiquitous problem of synchronization. Fundamentally, a PLL circuit is a feedback system tasked with aligning the phase of a local, frequency-variable oscillator to a reference clock signal. Due to the relationship between frequency and phase of periodic signals, this process also establishes a fixed relation between their frequency. Many variations of these circuits have been proposed for a multitude of tasks, including synchronization, data transmission, modulation and demodulation as well as a variety of sensing applications. Due to their fundamental role as clock generator circuits not only in HEP applications, this section reviews basic concepts of PLL circuits using its most commonly chosen architecture and provides required background for the work on conventional and all-digital PLL circuits presented in the following chapters.

2.2.1 Conventional Charge-Pump PLL

The charge pump (CP) PLL with phase-frequency detector [16] represents the most commonly used circuit in the domain of clock generation and synchronization. Widely studied since the 1970s, this circuit and many of its variants are widely used for tasks including frequency synthesis, modulation and demodulation, skew adjustment as well as clock and data recovery from serial data streams. The CP PLL is technically considered a mixed-signal circuit, since it processes digital clock signals, but internally uses analog current and voltage signals to implement a feedback control system. While some publica-

tions refer to this type of PLL as either a digital or an analog PLL circuit, this thesis will refer to it exclusively as a *conventional PLL* to contrast it against the all-digital PLL circuits that will play a major role in the remainder of the text. A schematic representation of the conventional PLL architecture is shown in figure 2.1. Five main constituents make up the feedback loop: The phase-frequency detector (PFD), one or more charge pump (CP) circuits, the loop filter (LF), a voltage-controlled oscillator (VCO) as well as a feedback divider, stylized by its division ratio N.

The phase-frequency detector (PFD) forms the error detector of the circuit, and in its linear region produces *up* and *down* pulses proportional in length to the instantaneous phase error between the reference and feedback clock signals. These pulses drive one or more tri-state charge pump circuits, which either source or sink a fixed current for the duration of these pulses. This process converts the phase error information into a continuous current signal. This current signal is processed by the loop filter, which is typically implemented as either a passive network or an active filter. The output of the loop filter represents the tuning voltage of the voltage-controlled oscillator (VCO), and as such controls its oscillation frequency in a continuous manner. A frequency divider included inside the feedback path allows the VCO frequency to be a multiple of the reference clock frequency.

This chosen structure has established itself as a beneficial architecture for a variety of reasons. Firstly, the PFD not only provides an ambiguity-free and linear detection gain across a $\pm 360^\circ$ range of phase errors. It also provides wide frequency detection capabilities, which increases the range over which the loop is able to successfully acquire phase lock. The integrator formed by the combination of the CP and the loop filter capacitor increases the open loop transfer function magnitude to extremely high values at low frequencies, which eliminates systematic static phase offsets. Crucially, this property can be obtained even with only a passive loop filter [16], which is beneficial from a power and noise standpoint. The inclusion of a feedback divider gives a PLL the additional advantage of not only providing phase synchronization between a reference clock and its internal oscillator, but also implementing almost arbitrary frequency multiplication capabilities.

2.2.2 All-Digital PLL

While charge pump-based, conventional PLL circuits have been the dominating type of clock generator in integrated circuits for multiple decades, the evolution of CMOS technology scaling makes their implementation increasingly difficult. Supply voltage reduction, increased switching noise coupling from adjacent digital circuit blocks and the absence of many established analog process options are among the many challenges for successful implementation of the high performance analog circuits required in conventional PLLs [17]. Analog

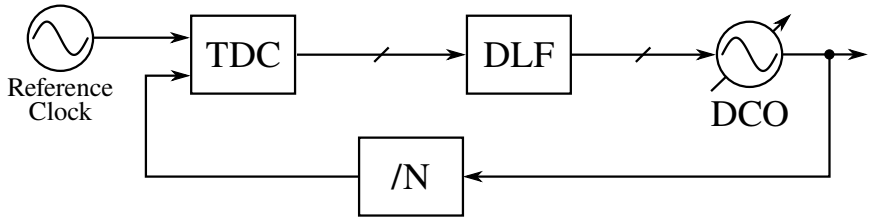


Figure 2.2: Conceptual block diagram of an all-digital PLL.

circuits are also limited in their abilities to provide and incorporate with flexible approaches to calibration or advanced algorithms, such as fast-locking techniques.

The all-digital PLL architecture in contrast represents a key paradigm shift addressing these challenges. This architecture has emerged around the turn of the century, pioneered by the group surrounding R.B. Staszewski [18, 19, 20, 21, 22]. It operates on the basic premise that in highly scaled CMOS technologies, the time resolution of digital signals exceeds the voltage resolution (and signal-to-noise ratio) of analog voltages [22]. It leverages this realization by substituting the major analog building blocks of conventional PLLs by digital equivalents. A straight-forward realization of such an approach is schematically shown in figure 2.2. While bearing structural resemblance to the conventional PLL of figure 2.1, notable changes concern the implementation of these blocks.

Crucially, PLL circuits fundamentally already operate on time domain information in the form of the phase error between two clock signals. Instead of a conversion into the analog current or voltage domain as in the conventional PLL, a time-to-digital converter (TDC) can be employed as the phase error detector. This converts the phase error into digital, quantized information. The following processing inside the loop, conventionally implemented by means of charge pump and active or passive analog filter circuits is performed by a digital loop filter (DLF). As an equivalent to the tuning voltage normally steering the frequency of the VCO, this digital filter produces at its output a frequency tuning word, which instead controls a digitally controlled oscillator (DCO). The time-based processing already inherent to the frequency divider remains unchanged with regards to the conventional PLL.

A number of obvious advantages emerge from this general view on all-digital PLL circuits. Notably, the processing of timing- and noise-critical signals is confined to a smaller number of circuits. The phase information of the digitally controlled oscillator (DCO) and reference clocks need to be retained from the place of their generation, through any dividers and up to the time-to-digital converter (TDC). The conversion of the phase error into a digital word decouples it from the need to retain precise timing information during further processing,

and its digital representation is much less sensitive against interference arising from signal integrity or noise considerations than analog voltage and current signals.

A major disadvantage is however also apparent from this qualitative discussion: Both the conversion and the processing of signals in the digital domain necessitates the representation of continuous quantities (such as phase error) using finite word lengths, implying that quantization is required. In practice, this quantization occurs in two important places, where practical considerations limit the achievable resolution and hence the amount of quantization noise added in the process. The first source of quantization noise is the TDC, which converts a phase difference into a digital word with finite precision. On the other end of the digital signal processing chain, digital frequency control of the DCO can only be implemented with finite granularity. Here, different considerations dictate both high resolution and wide tuning range, resulting in potentially large word widths to fully represent the resulting dynamic range. The design process for all-digital PLLs necessarily adapted to these challenges, and consequently a body of work has emerged, exploring the various theoretical and practical analysis and design aspects of these circuits, examples of which are [22, 23, 24, 25].

2.2.3 Clock and Data Recovery (CDR) Circuits

One natural modification of PLL circuits is their use as synchronizing circuits for serial data links, in which no separate clock signal is transmitted alongside the data information. The purpose of a CDR circuit is therefore the recovery of the clock information inherently included in the data symbol timing information.

Typically, such CDR circuits are structurally very similar to PLL circuits and mostly differ in the choice of error detector they employ. Crucially, suitable error detectors need to cope with the potential absence of transitions (which provide the timing information required to properly adjust the data sampling phase) and the uncertainty of the transmitted data pattern, which may additionally be corrupted by noise. Examples of such phase error detectors are the (linear) Hogge phase detector [26] or the (nonlinear, i.e. bang-bang) Alexander phase detector [27]. After the CDR loop has locked to the incoming serial data stream, the local oscillator phase is aligned with the input data stream, such that its edges can be used to reliably sample and hence recover the transmitted data. In particular for high-speed data links, the quality of this recovered clock signal is of critical importance. Impairments such as sampling jitter arising from random or deterministic sources of noise in the system (which are discussed later) may otherwise result in data errors.

2.2.4 Oscillators for Frequency Synthesizers

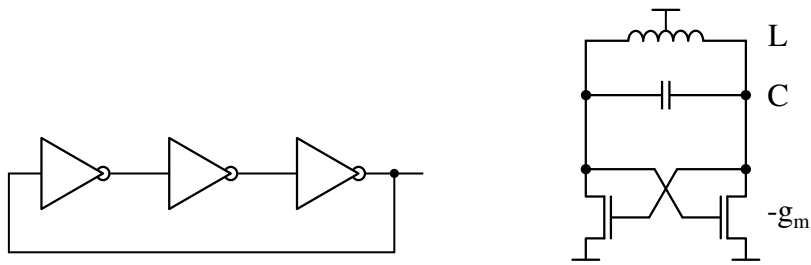
Regardless of the chosen PLL architecture, a number of different oscillator topologies are available for integrated circuit implementations of PLL and CDR circuits. As far as the design of high-speed PLL circuits in the gigahertz-range is concerned, ring oscillators and LC oscillators are the only choices that allow for complete integration on-chip while providing adequate levels of performance.

Ring Oscillators

Ring oscillator circuits are non-tuned circuits in which an oscillation arises from propagation delays. In its most simple form, a closed ring is formed from an odd number of inverting amplifiers, as shown in figure 2.3a. Such a circuit does not possess a stable DC operating point, but instead fulfills the Barkhausen criteria for oscillation [28]: For at least one frequency, the phase shift incurred by passage through the ring is an integer multiple of 180°, which satisfies the phase criterion. Since the amplifiers in principle provide a voltage gain larger than unity, which however reduces as the oscillation waveform increases in amplitude, the amplitude criterion can also be satisfied. Based on this simple model, the oscillation frequency of a ring oscillator composed of N stages with propagation delay t_{D} is given by

$$f_{\mathrm{RO}} = 2Nt_{\mathrm{D}}. \tag{2.1}$$

Ring oscillators lend themselves to high-speed oscillator implementations in CMOS technologies due to the ubiquity and the beneficial scaling properties of inverter circuits. Many variations of this basic circuit concept have been devised, including differential implementations, quadrature oscillators using an integer number of stages, and the use of feed-forward techniques to obtain



(a) Ring oscillator. (b) LC oscillator.

Figure 2.3: Comparison of the two oscillator circuit types relevant for high-speed PLL implementations.

higher oscillation frequencies. Crucially, ring oscillators are often implemented with frequency control mechanisms, making them a suitable choice for PLL circuits. Different tuning schemes can be used, while most commonly frequency control is established by controlling the current of current-starved inverter circuits by means of a bias voltage [29, p. 595]. While high speed ring oscillators can typically be implemented using very little area compared to LC oscillator topologies, they are also associated with drawbacks. The regenerative nature of each stage in the oscillator results in worse noise performance than harmonic oscillators. The strong dependence of their oscillation frequency on the gate delay makes these circuits additionally very sensitive to varying process, voltage and temperature (PVT) conditions and supply noise coupling.

LC Oscillators

LC oscillators make up the second large class of oscillator circuits suitable for integrated high-frequency PLL circuits. Their basic topology is shown in figure 2.3b. These oscillators belong to the class of harmonic oscillator circuits. To first order, their oscillation frequency is determined only by the resonance frequency of the tank circuit formed by a capacitance C and an inductance L, given by

$$f_{\mathrm{LC}} = \frac{1}{2\pi\sqrt{LC}}. \tag{2.2}$$

Since in practice, the energy stored in and transferred between the inductance and the capacitance of the resonant tank is lost through resistive, magnetic and dielectric loss mechanisms, an amplifier is required in these circuits to obtain a sustained oscillation. Since this active amplifier contributes noise to the oscillator and also requires power to replace the energy dissipated by the various loss mechanisms, the best circuit noise performance and lowest power consumption are simultaneously achieved by minimizing these losses, leading to a high tank quality factor Q. In integrated circuits, limits on the achievable quality factor are given primarily by the resistivity of the metallization layers used to implement the inductor and interconnect, however losses in the capacitor dielectrics and losses from eddy currents in the substrate or metallization are also important concerns.

2.2.5 Phase Noise and Jitter

A number of processes inside oscillators are responsible for the generation of voltage and current noise. Examples of these are the thermal noise in the loss resistance of an LC-tank or the various (thermal, flicker, shot, etc.) noise processes in their active devices, forming the delay cell or feedback amplifier. The presence of voltage or current noise on the oscillator waveform necessarily

results in a corresponding modulation of the oscillation phase through AM-PM conversion. In a similar fashion as the voltage or current noise it originates from, phase noise manifests with a certain spectral composition. For this reason, the spectral density of phase noise is often given as a function of the carrier offset frequency and expressed in terms of the amount of phase modulation relative to the carrier frequency.

For some applications, in particular such that do not necessarily rely on the spectral qualities of the underlying phase noise, specifications are more conveniently expressed in terms of timing jitter. The uncertainty of timing events (such as the rising edge transition time of the oscillation waveform) may be summarized succinctly as only its rms or peak-to-peak variation. Due to the varied nature of jitter sources in circuits and systems, a number of further jitter metrics have been introduced, in order to decompose and attribute individual jitter contributions. Among these are the broad distinctions into random and deterministic jitter, while the latter category can be further subdivided into sources that are correlated or uncorrelated to the clock itself.

The amount of time-domain jitter represented by the frequency-domain phase noise spectrum can be calculated by integration of the phase noise spectrum. Typically, a frequency range interesting for the final application is chosen during this integration process. In this way, jitter on timescales not important for system performance can be excluded. This limitation however necessitates using identical phase noise integration boundaries when comparing the jitter performance of different circuits or systems. The integration process is further irreversible, and hence the phase noise spectrum can not be unambiguously derived from time-domain jitter figures [30, p. 146].

In the field of high energy physics, a number of system requirements limit the allowable amount of jitter that can be produced within oscillator and, more generally, clock generator circuits. For the ubiquitous use case of time-to-digital conversion in particle detection applications, jitter limits the achievable precision of time of arrival (ToA) and time over threshold (ToT) measurements. The same is true for analog-to-digital conversion, where excessive jitter on the sampling clock limits the achievable signal-to-noise ratio of digitized signals. In high speed data links, the presence of timing jitter on data signals results in reduced link performance, manifesting as reductions in the link margin, leading to increased bit error rates. As such, phase noise and jitter are the key performance figures by which clock generator circuits discussed in this thesis will be analyzed and compared.

2.2.6 Impulse Sensitivity Function

Specially tailored models for the prediction of phase noise in certain types of oscillators have emerged in the scientific literature in the past. One example is the Leeson phase noise model for resonant oscillators such as the LC oscillator

[31]. Similar models exist also for ring oscillators, such as the one proposed by Weiganth [32]. These models and some of their extensions are thoroughly reviewed in [30]. While these models offer some design insight, oftentimes they can not suggest how improvements in a given circuit can be obtained, or their applicability is limited to a certain oscillator topology and can not be easily extended to more complex circuits. Most importantly, these models fail to explain frequency up- or downconversion of noise, which is a crucial element of low-noise oscillator design.

Based on the modeling of oscillator circuits as linear and time-variant systems, Hajimiri and Lee have proposed a generalized framework useful in the design and analysis of oscillator circuits, called the impulse sensitivity function (ISF) [33, 30]. The ISF itself represents a time-variant impulse response, describing how perturbations in the form of current impulses in arbitrary nodes of an oscillator circuit are converted into a finite amount of excess phase. This insight is useful on its own, since it allows analyzing the susceptibility of oscillator designs to perturbations from internal and external sources. It becomes particularly useful for the prediction of phase noise performance when combined with the concept of the noise modulating function (NMF). The NMF exploits the cyclostationarity of the noise processes in oscillators to describe the envelope of the noise produced within active devices using a periodic function. Their proposed theory further shows that by multiplication of the ISF and the NMF, the effective ISF of an oscillator for a stationary noise process can be obtained. By showing that minimizing the magnitude of this effective sensitivity function also minimizes the phase noise, a convenient and tractable predictor for the noise performance of oscillator designs emerges. A major insight from the modeling approach taken by the ISF is its ability to explain the up-conversion of normally low-frequency noise processes such as flicker noise to the sidebands of the oscillator frequency. Based on a Fourier decomposition of the ISF, an optimization criterion is proposed, which is applicable for arbitrary oscillator topologies. It can be shown that the magnitude of the DC component of the ISF is a direct predictor of the up-conversion efficiency of low-frequency noise. Hence, good flicker noise performance can be obtained through an objective-driven optimization of the ISF for any given oscillator topology.

Compared to the initially discussed traditional models, the proposed impulse sensitivity model has a number of advantages. The first significant advantage is its capability to accurately predict the noise performance of a wide range of oscillator circuits. Additionally, the framework lends itself to a number of different approaches to circuit analysis and designs: The analytical derivation of the ISF is feasible for simple topologies, which provides a large degree of design insight and allows performing architectural trade-offs and comparisons. More complex structures can be analyzed using either numerical methods or using circuit simulations. The ISF also lends itself to an analysis using

circuit simulations due to its simple definition based on quantities readily studied using SPICE simulators, such as node currents and the phase of the oscillation waveform. Since the theoretical framework can be applied directly to arbitrary circuit topologies, the derivation process of the ISF can be automated using commonly used electronic design automation (EDA) tools. This allows performing quantitative comparisons between different practical circuits as well as circuit optimization tasks.

The theoretical framework provided by the ISF has also found applications for other use cases than the optimization of oscillator circuits, in particular in the domain of circuit radiation hardening. Transient radiation effects in CMOS devices are often modeled by current impulses, albeit often with more complex pulse shapes arising from the underlying charge transport phenomena, such as the double-exponential model [34]. Experimental work has shown that the sensitivity of oscillators to transient radiation effects is time-dependent, and periodic sensitivity functions similar to the ones emerging as the ISF can be practically obtained using charge injection using selective laser irradiation of manufactured circuits [35]. This suggests that the developed analysis techniques can be applied to study and improve the radiation tolerance of oscillator circuits, for example using charge injection simulations and experiments.

2.2.7 Dynamic Characteristics

PLL circuits are feedback systems and are therefore characterized by a certain dynamic behavior dictated by the properties of their constituent components. This dynamic behavior can be predicted from the corresponding control system transfer functions. Since practically used loop filter topologies have low-pass characteristics, two important closed-loop transfer functions emerge. The reference transfer function describes the propagation of reference clock dynamics (phase and frequency errors) to the clock output, and is also low-pass in nature. A complementary, high-pass transfer function is found from the VCO input to the PLL output. Its high-pass nature is readily explained by the fact that any steady-state (i.e. low-frequency) frequency error originating in the VCO will be fully compensated by the feedback loop over time, and hence only high frequency components (much shorter than the dominant PLL control time constant) will propagate to the output.

Since the loop transfer function can be readily controlled by appropriate choice of the loop filter transfer function, it becomes the primary design variable for a number of important trade-offs. Since both the reference clock as well as the VCO contribute phase noise to the output of the PLL, an optimal design seeks to balance both contributions, for example to minimize the total PLL jitter. The low-pass-filtered reference clock noise and the VCO noise undergoing high-pass filtering can be made equal contributors to the output clock phase noise with an appropriate choice of the loop bandwidth. For sampled feedback

systems such as the CP-PLL, an upper bound to this bandwidth exists in order to retain stability, which is typically quoted around one tenth of the reference clock frequency unless further analysis is performed. Additional considerations arise from the transient behavior of the feedback loop. Choosing a smaller loop bandwidth also results in longer transient responses from perturbations of the loop, which increases the settling time during the lock-in process or when affected by a perturbation during operation arising from external factors. Its choice therefore also needs to be considered when designing radiation-tolerant systems. Finally, the damping factor ζ (as applied to a second-order system) is a noteworthy design parameter for such PLL circuits. A choice of low damping factors results in oscillations at the loop's natural frequency, which decay only slowly. Such choices also reduce the system phase margin, cause excessive peaking of the loop transfer function, and hence result in jitter peaking, in particular for cascaded systems. Excessively high damping factors on the other hand are a cause of slow settling behavior. Depending on design constraints, good choices are typically found in the vicinity of $\zeta = \sqrt{2}/2$ (critical damping) and above when dictated by jitter peaking requirements.

A final design metric applicable to CDR circuits in particular arises from the discussion above. Depending on the expected dynamics of the data source and transmission channel, systems are often specified in terms of *jitter tolerance*. System specifications using this metric typically specify the minimum amount of sinusoidal phase modulation that needs to be tolerated by the CDR circuit as a function of the modulation frequency, where tolerance is typically given as a maximum bit error rate specification to be achieved under these conditions. The loop filter transfer function must be chosen such that the specified amount of input jitter can be tracked with a phase error small enough to not result in an excessive bit error rate.

2.2.8 Figures of Merit

From the introduction of quantities important for the performance of oscillator circuits above, it is clear that a large number of trade-offs exist in the design of oscillator circuits. Fundamentally to both presented topologies is however a scaling of phase noise performance with the power consumption expended. For this reason, the corresponding figure of merit shown in equation (2.3) is often used to asses the performance of designs. The figure of merit (FOM) of an oscillator circuit oscillating at a frequency of f_{osc} considers the phase noise $\mathrm{PN}_{\mathrm{osc}}$ at an offset frequency f_{offset} from the carrier, as well as the power dissipation P_{osc}.

$$\mathrm{FOM}_{\mathrm{osc}} = -\mathrm{PN}_{\mathrm{osc}}(f_{\mathrm{offset}}) + 20\log_{10}\frac{f_{\mathrm{osc}}}{f_{\mathrm{offset}}} - 10\log_{10}\frac{P_{\mathrm{osc}}}{1\,\mathrm{mW}}. \tag{2.3}$$

Applying this FOM to compare the performance of integrated ring and LC oscillator circuits, typically a discrepancy between 10 and 20 dB is identified. This stark difference in the power that needs to be expended to achieve a given noise performance delineates the different application areas for these two oscillator types. Applications that are area-constrained and have less stringent noise requirements often adopt ring oscillator circuits. When the highest performance is sought after instead, the additional area required for an LC oscillator is often expended to achieve this performance at an acceptable power consumption.

In a similar manner, this fundamental noise-power trade-off also drives the design of the complete frequency synthesizer circuit. A certain amount of power needs to be expended to achieve a certain amount of jitter from the PLL. While in an otherwise noise-free circuit, only the local oscillator contributes to this budget, in practice also all other components of the PLL contribute additional noise which is converted to noise, which can be reduced at the expense of additional power. Again, a suitable FOM provides a basis for comparisons between different architectures, which is formulated in equation (2.4). This FOM considers the standard deviation of the PLL output jitter σ_{PLL} and the circuit power dissipation P_{PLL}.

$$\mathrm{FOM}_{\mathrm{PLL}} = 20\log_{10}\frac{\sigma_{\mathrm{PLL}}}{1\,\mathrm{s}} + 10\log_{10}\frac{P_{\mathrm{PLL}}}{1\,\mathrm{mW}} \tag{2.4}$$

2.3 Radiation Effects in Frequency Synthesizers

Based on the treatment of radiation effects on electronics circuits given in section 2.1, the practical manifestations of different types of radiation effects in CMOS frequency synthesis circuits can be reviewed. Again, their sensitivity to radiation can be meaningfully separated into transient SEE and cumulative TID effects [36]. While a large number of experimental studies on these circuits have been performed in the past, efforts were mostly focused on the conventional charge-pump based PLL architecture, consisting of a linear PFD, CP, loop filter (LF), VCO and a feedback divider, which closes the feedback loop. This section will focus on CMOS implementations of these circuits, and will particularly consider only LC-tank and ring oscillators as the two most common types of VCO topologies presented earlier.

2.3.1 Single-Event Effects

First, considering only single-event effects, a number of shortcomings of the conventional PLL architecture have been reported in the past. The PFD

containing digital storage elements is generally sensitive to SEUs. Even though an upset in the PFD persists for at most one reference clock cycle, it may cause the charge pumps to remain enabled for a significant amount of time. Since these are otherwise (during steady state operation) only active for a very short period each reference clock cycle, this can cause a transfer of large charge quantities into the loop filter, altering the VCO frequency. Such a change will result in an accumulation of significant phase errors and may lead to cycle slips [37, 38]. This sensitivity was shown to be largely mitigated by protection of the PFD using TMR, a technique further described in section 2.4 [37]. A source of sensitivity to SEUs and SETs is similarly present in the feedback divider. Corruption of any of the state registers in the divider results in a phase jump of the feedback clock. This phase error subsequently needs to be corrected by the feedback loop. Again, a mitigation can be found in TMR implementations of the divider [37, 39] or by applying radiation-hardened-by-design (RHBD) techniques, such as double interlocked cell (DICE) implementations for memory elements [40].

Another contributor to SEE sensitivity may be found in the charge pump driving the loop filter [38, 41]. Current-based charge pumps specifically suffer from long recovery times after SETs due to their limited rate of charge evacuation, which again causes large accumulated frequency and resulting phase errors. This sensitivity has been mitigated, for example, by the use of a tri-state voltage charge pump architecture, which reduces the number of sensitive nodes and increases the rate of charge sourcing and sinking [42, 43] at the cost of poor reference-spurs and PVT-sensitive static phase errors. A variety of circuit level mitigation strategies allow suppressing SEE responses from these components in many practical designs. This often leaves the VCO as the remaining, critical component sensitive to SEEs. Depending on the chosen oscillator topology, different mechanisms and sensitivities can be identified.

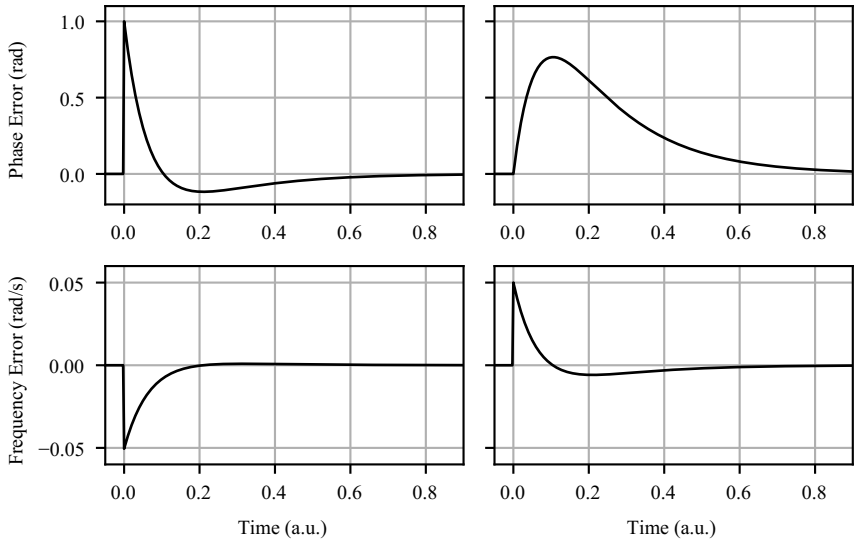
In LC VCOs using cross-coupled differential amplifier topologies, charge collection at the drain node of the connected bias current source is reported to result in a temporary reduction of oscillation amplitude and frequency [44, 45]. This sensitivity can be significantly reduced by the addition of capacitance to this node [44]. A second sensitivity of LC VCOs is often found at their tuning node. Typical MOS varactor tuning architectures were found to be sensitive to charge collection, as reported in [46]. This sensitivity can be largely mitigated by adopting a modified tuning topology [39], which, however, has the drawback of introducing an additional pole at the tuning node of the VCO. The main oscillation nodes are typically quite robust to charge collection, since the amount of oscillating charge in the tank itself is often large, compared to the collected charge at the junctions of the active devices. Additionally, only a small number of device junctions susceptible to charge collection are typically connected to these nodes, and consequentially the sensitive area is limited.

CMOS ring oscillators were found to be susceptible to transient frequency and phase errors [47], missing pulses [48] and stimulation of harmonic oscillation modes [49]. Being composed almost exclusively from active devices with the minimum addition capacitance (in order to achieve high oscillation frequencies), ring oscillator circuits generally exhibit high levels of sensitivity. Since variable-frequency ring oscillator circuits typically exhibit a much larger tuning gain than LC VCOs, the sensitivity to SEEs affecting the tuning node is amplified significantly as well. Some amount of hardening against many of the reported sensitivities has been achieved by measures such as the replication of bias stages [47], duplicating or triplicating larger parts of the oscillator [50, 51] and oscillator stage design methodologies aimed at suppressing the propagation of harmonic modes [49].

Systematization

Upon reviewing the identified sensitivities in PLL circuits, the primary way in which the loop is disturbed by SEEs can be used for refined classification. SEUs and SETs in the PFD, CP and the tuning node of the VCO primarily cause a frequency error of the PLL, and therefore are henceforth referred to as single-event frequency transients (SEFTs). SEEs confined to the oscillating node of the VCO or the feedback divider instead manifest as phase errors, which is why they are referred to as single-event phase transients (SEPTs). This classification is useful, since the dynamics of the feedback loop in response to these two categories can differ considerably.

An illustration of typical behavior of the primary PLL state variables (phase and frequency error) in response to both types of transient errors is seen in figure 2.4. Because any phase errors stimulated during an SEPT are directly observed by the phase detector, the loop is able to immediately react to such disturbances, and the phase error is corrected within a short recovery period. The recovery from frequency errors instead requires an initial accumulation of phase error which can be detected by the phase detector. The response to SEFTs is therefore instead characterized by an initial gradual build-up of phase error, which is then subsequently corrected by the control loop. Hence, the reaction time to frequency errors is significantly larger than that for phase errors. From a control theory perspective, these differences are equivalent to step (SEPT) and ramp (SEFT) error signal introduced at the plant output. Following the reasoning presented in section 2.2.7, an appropriate choice of key loop parameters such as loop bandwidth and damping factor can reduce the susceptibility to radiation effects. Using larger loop bandwidths is often beneficial as the recovery from transient perturbations is accelerated. In particular for SEFTs, increasing the loop bandwidth additionally reduces the amount of phase error build-up, again leading to faster recovery and reduced transient phase errors. In practice however, the loop design may be driven by phase noise or jitter constraints,



(a) SEPT ($\Delta\varphi = 1\,\mathrm{rad}$). (b) SEFT ($\Delta f = 0.05\,\mathrm{rad\,s^{-1}}$).

Figure 2.4: Reaction of a PLL feedback loop to single-event phase and frequency errors. Simulated single-event phase or frequency transients are injected into the loop at $t = 0$.

rendering such choices unavailable. Therefore, a systematic mitigation approach of SEE sensitivities within the loop instead of their suppression is often the preferred choice.

2.3.2 Total Ionizing Dose Effects

With regards to TID effects, the VCO and CP circuits can be identified as the main contributors to performance degradation. The degradation of digital circuits (PFD and feedback divider) in the PLL has no impact on PLL performance, as long as their setup and hold timing requirements continue to be met. One major concern is the degradation of active devices in the charge pump. A reduction of the charge pump current results in a decrease of loop gain, which reduces both the bandwidth and damping of the closed-loop transfer function. When an active loop filter is used, degradation of the implemented amplifier circuits may lead to similar changes in loop dynamics. As long as only passive loop filters are used, the typically chosen resistor and capacitor implementations are often insenstive to TID effects when compared to effects in active devices.

Considering the VCO, different sources of sensitivity can be identified based on the chosen oscillator topology.

LC VCO

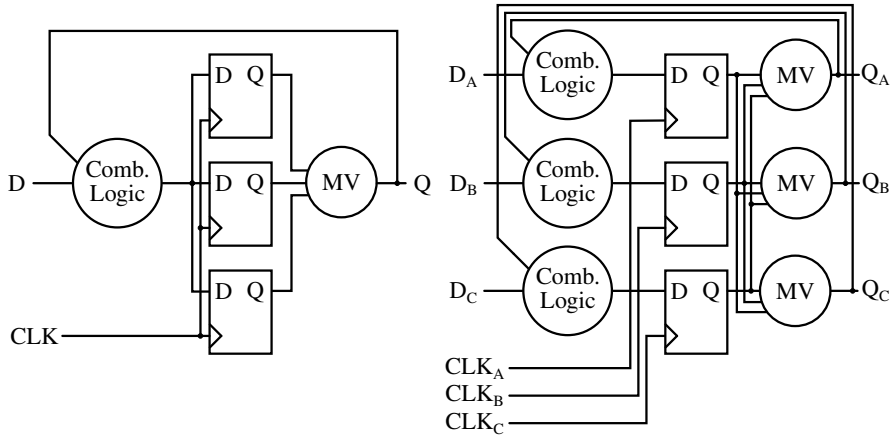
The frequency of LC oscillators is dictated by the inductance and capacitance of the tank. Since these are typically implemented using passive circuit components, they can be considered tolerant to TID effects. One of the dominant degradation mechanisms affecting the devices forming the VCO amplifier is a reduction of their transconductance. This reduces the oscillation amplitude, which, through the presence of voltage-dependent capacitances at the oscillator nodes, is converted into a change of oscillation frequency [46]. Such oscillation frequency shifts are typically limited to within a few percent. Due to the often limited tuning range of LC oscillators, such shifts must nonetheless be accounted for during their design. A suitable mitigation strategy is found in extending the VCO tuning range to enable continuous operation at high doses. Furthermore, the reduced transconductance of the VCO amplifier will eventually result in failure to start or sustain stable oscillation.

Ring VCO

In terms of TID effects in the dose regime above 100 Mrad, the dominant mechanism in sub-micron CMOS ring oscillator circuits is the increase of stage delay [52]. The resulting decrease of oscillation frequency eventually leads to failure of the oscillator to provide the frequency required by the application. When the amount of degradation over the device lifetime can be anticipated, sufficient tuning margin can be foreseen during the design phase. Alternatively, layout techniques such as enclosed layout transistor (ELT) geometries [13] can be used to reduce the amount of TID degradation. Depending on the chosen topology, a severe change of the oscillator tuning gain can occur as the device degrades. This can potentially result in significant deviations from the desired loop dynamics.

2.4 Triple Modular Redundancy

Triple modular redundancy (TMR) has been studied in the general context of computing reliability since the 1950s [53]. Nowadays, it is considered one of the most prominent techniques used to protect digital circuits against SEE in ASICs designs for the LHC. On a basic level, this technique improves the reliability of digital circuits and systems by retaining three replicas of stored data. Even in the presence of corruption of one of the replicas, the original data can be unambiguously recovered using a two-out-of-three majority voting process. Due



(a) Basic TMR (b) Full TMR

Figure 2.5: Comparison of commonly implemented redundancy schemes based on TMR.

to the small set of assumptions made by the technique itself, it can be applied with different levels of granularity. Replication can be implemented at the level of individual data bits, circuits or modules, but also complete devices or whole systems can be implemented redundantly in this way. In the scope of this thesis, the most relevant application is concerned with the implementation at the logic level, where the individual memory elements of a digital circuit are protected by TMR.

In contrast to other RHBD design methodologies, which attempt to increase the reliability of individual combinatorial and sequential logic elements, TMR instead provides systematic hardening even when individual logic cells remain susceptible to SEE. This approach can provide benefits in situations where RHBD methods on the cell-level can not guarantee sufficient protection of single cells in a given circuit radiation environment. With the increasing logic density in advanced CMOS nodes, the implementation of sufficient protection on the cell level can itself significantly increase the required cell area, and hence may not be a favorable option for hardening large circuits [54].

Figure 2.5a illustrates the basic TMR scheme applied to a model of a digital circuit composed of combinatorial and sequential cells. In this basic implementation, only the memory elements are replicated, and a single majority voter is included, which feeds all combinatorial logic and outputs. While the cost in terms of area and power of such an architecture is small, it can also only provide limited protection: While the circuit becomes robust against

SEUs affecting the memory elements themselves, at least two weak points remain unprotected against. Firstly, SETs affecting the majority voter or the combinatorial logic may result in all memory elements latching invalid data. On one hand, this may be unlikely to happen as long as SET pulses are short in relation to the clock period. However, typically the number of cells forming the combinatorial logic and majority voter is significantly larger than that of the sequential elements. Therefore they represent a significantly larger sensitive area, increasing the likelihood of SET-related data corruption. Additionally, all memory elements use a number of common control signals (such as clock and reset inputs), which typically originate from large clock and reset trees. Since these are often shared among many sequential elements in a circuit, SETs within these trees may result in simultaneous corruption of multiple data replicas, invalidating the core assumption of the TMR scheme. Numerous solutions have been devised to address these two architectural shortcomings, typically trading off enhanced circuit protection against an increasing penalty in power and area. Examples of such approaches can be found in [55, 56, 57].

A commonly used variation of TMR offering the largest degree of protection is termed 'full TMR', and implements full redundancy of all circuit elements as shown in figure 2.5b. Notably, this improved version also replicates all combinatorial logic and the majority voters. In this implementation, corruptions from any SETs in the combinatorial logic can be limited to affect a single memory replica. Implementing fully independent clock and reset signals (connected to individual, independent distribution trees) limits the SET sensitivity to only a single data replica. While providing ultimate protection against SEUs and SETs in digital designs, this implementation also clearly comes with the largest associated cost: The required circuit area is increased by more than a factor of three, as additional area is required for the majority voters. The circuit power consumption increases by a similar amount. Especially in high speed digital circuits, TMR might also limit the maximum operation speed of a given circuit: In case an additional majority voter forms part of the critical setup timing arc, its additional gate delay will reduce the achievable circuit performance.

2.4.1 Implementation Considerations

Especially in deep sub-micron CMOS nodes, a number of additional factors need to be considered when TMR schemes are implemented.

Signal Integrity

Implementation of TMR schemes increases the switching activity of digital circuits by multiplying the amount of active logic. Concerns relating to signal integrity can arise from this increased activity and the resulting coupling to other signal nets. Since most switching activity in redundant portions of the

design is additionally correlated, the aggressor potential of this activity may increase notably. While static timing analysis in advanced nodes typically accounts for the impact of signal-to-signal coupling on timing closure, additional mitigation measures such as shielded clock routes might be required to achieve the required level of signal integrity, in particular for high speed designs.

Power Integrity

Another consequence of a threefold increase in periodic switching activity is the associated increase of static and dynamic power dissipation. Since the achievable resistance of power distribution networks is limited by the thickness of metal layers in advanced CMOS processes, the design of on-chip power distribution networks needs to account for higher power consumption, which can require dedicating additional resources to power distribution in order to preserve the required level of power integrity. Especially when situated close to sensitive low-noise circuits, the additional noise may lead to degraded performance. In the case of low-jitter PLL circuits, the level of spurious components in their phase noise spectrum can increase when insufficient isolation through the substrate or the power distribution network is available.

Multi-Bit Upset Sensitivity

Advanced CMOS design nodes achieve a very small size of individual logic cells. This allows for tighter packing of individual memory elements in circuits, but also reduces the amount of critical charge required to induce SETs and SEUs [58]. Since TMR operates based on the assumption of at most a single data replica being corrupted, any simultaneous SEEs affecting multiple memory elements storing replicas of the same data must be avoided. The small cell size and high density increases the probability of such events. In practice, this issue can be mitigated by appropriate cell placement during the physical implementation of a circuit: As long as sufficient spacing between replica storage elements is retained, the probability of a single radiation response corrupting more than one of them at the same time is minimized [59].

Chapter 3

Radiation Test Instrumentation for Frequency Synthesizers

Chapter 1 has introduced the increasing importance of radiation-tolerant clock synthesis and distribution circuits for current and future HEP applications. A full assessment of their susceptibility to radiation effects can often not be obtained from theoretical analysis and simulations alone. Essentially all such circuits require characterization or qualification to be performed using radiation tests. Especially for SEE testing of frequency synthesizers in the constraints of experimental facilities, such as their costly operations and limited availability, a need for specialized test equipment has been identified early on in the development of PLL circuits for space environments [60]. Oftentimes, needs not covered by capabilities of commercially available instrumentation are addressed by custom developments. When comparing the requirements of advanced detectors for HEP with available off-the-shelf and custom instrumentation capabilities, a clear gap can be identified. This chapter aims to close this gap by significantly improving SEE detection and analysis capabilities through the development of different precision instrumentation setups. First, requirements and constraints of current and future systems are analyzed and used to substantiate the requirements of such instrumentation. Following, a survey of the state of the art in the domain of SEE testing for frequency synthesizers is conducted. An advance of this state of art is made by presenting three designed test systems and their capabilities. Their characteristics are compared and supporting information on their applicability to various radiation testing scenarios is given at the end of the chapter.

3.1 Requirements Analysis

Primary requirements for radiation qualification of components such as PLLs, delay-locked loops (DLLs) or CDR circuits can be derived from specifications of contemporary systems foreseen for upgrades of the LHC at CERN. Three main drivers can be identified among these developments. The first one is constituted by timing detectors, such as the ATLAS High Granularity Timing Detector (HGTD), the CMS MIP Timing Detector (MTD) or the CMS High Granularity Calorimeter (HGCal). Common to these detectors is a requirement of a random clock jitter in the range of 5 ps to 15 ps rms at the level of the frontend ASIC [5, 6, 61]. This requirement is, in turn, driven by the timing resolution achievable by the adopted sensors, such as low gain avalanche detectors (LGADs) for the ATLAS HGTD and the CMS MTD. In a similar fashion, clock distribution and synthesis requirements are driven by fast, high resolution analog-to-digital converters (ADCs) that are increasingly employed for precision energy measurements. Sampling clock jitter in the single-picosecond range is required to ensure negligible degradation of the signal-to-noise ratio (SNR) performance of these data converters. A third driver for requirements is the evolution of high speed data links. Systems intended for installation during the High Luminosity LHC upgrade utilize hundreds of serial optical data links at data rates of up to $10\,\mathrm{Gbit\,s^{-1}}$ per link. Excessive random clock jitter as well as SEPTs and SEFTs even at the level of a tenth of a bit period (10 ps) can reduce link margins and result in temporary data corruption or link failure.

Since clock jitter accumulates through the multiple levels of clock synthesis and distribution of a large detector system, specifications for individual circuit components are more stringent than the numbers quoted previously. As an example, the Low Power Gigabit Transceiver (lpGBT), a common ASIC development designed to support the clock distribution requirements of all High Luminosity LHC detectors, is specified to guarantee a 5 ps rms clock jitter performance and in practice offers performance on the 1 ps level [62].

Jitter specifications expressed as solely in terms of an rms value are not fully adequate for assessing radiation tolerance, since the conformity with such a specification depends heavily on the specific operational radiation environment of the circuit. The frequency and magnitude of SEE such as SEPT and SEFT depend on the specific radiation environment, i.e. the particle field composition and the expected particle flux. In the majority of cases, the final radiation environment is not available during circuit qualification. Therefore, predictions for the final radiation environment need to be provided based on data obtained at available irradiation facilities.

Since undetected radiation effects risk compromising the integrity of obtained physics data when not properly accounted for, reliable identification and characterization of radiation sensitivities in circuits is important. At best, undetected

radiation sensitivities may reduce detector performance, for example through an increase of apparent background event rates. At worst, flawed conclusions might be drawn from detector data tainted by unknown radiation responses. It is for this reason that detecting and characterizing radiation-induced SEPT or SEFT of such circuits necessarily requires instrumentation offering resolution down to the level of the random jitter.

The resolution of detectors, the sampling frequency of data converters as well as the data rates of serial communication links will continue to increase to fulfill the challenging requirements of future HEP experiments. It should be anticipated that these developments will be paralleled also in the requirements for clock generation and distribution, as well as the associated test and instrumentation capabilities. These trends further motivate the design of scalable, low jitter measurement instrumentation with picosecond-level single-shot phase resolution and, most importantly, trigger capabilities.

Secondary requirements arise from the aforementioned operational constraints of radiation test facilities suitable for characterization of circuit SEE performance. Such facilities are often particle accelerator facilities or specialized laser test systems, of which only a small number exist worldwide. Consequently, they are costly to access and available for a given experiment only for a limited amount of time. From these constraints, it is clear that instrumentation must be designed to maximize the detection efficiency of the circuit SEE responses. This requires systems optimized for the least possible dead time following a detected event and ideally leads to the development of triggerless readout systems enabling offline event detection, classification and processing. To additionally improve utilization of beam time, setup simplicity and high integration are desirable properties of instrumentation and data acquisition systems. These reduce the installation time required during test campaigns and improve the reproducibility of performance in different physical locations. Additionally, instrumentation approaches enabling close integration with other test system components simplify system-level synchronization, trigger processing and traceability, which are beneficial in assessing the origin and impact of individual single-event effect responses of more complex circuits.

3.2 Review of State of the Art

Radiation effects in time processing circuits have been studied experimentally since at least the 1990s, initially targeting commercial integrated PLL circuits [60]. Various RHBD techniques have since been applied to application specific circuit implementations, and different approaches to experimental instrumentation have been pursued. These can be very broadly classified based on their domain of operation into frequency domain and time domain instrumentation.

3.2.1 Frequency Domain Instrumentation

Periodic modulation of the phase or frequency of a clock signal results in carrier sidebands or spurious tones in the frequency domain. This effect can be leveraged for characterization of circuit radiation responses by comparing the spectra of the circuit in the presence and absence of incident radiation. Since the relationship between properties of the modulation (phase or frequency error) and the resulting spectral components are well-understood, the obtained frequency domain measurements can be used to infer information about the transient radiation response stimulated inside the circuit. A benefit of these methods is that they can be performed using the same commercial test equipment also used for other circuit performance characterization tasks, such as spectrum analyzers. In principle, such instrumentation can achieve very high detection sensitivity, since leveraging the periodic nature of the involved signals allows coherent averaging, suppressing random noise.

In practice however, this approach is limited in its applicability to SEE testing. In all but a few specialized radiation test facilities, the stimulated single-event responses from the circuit under test can not be assumed to occur periodically. Especially in accelerator-based facilities, often a large circuit area is continuously irradiated, and the arrival times and locations of individual particles are not known. Events occur randomly distributed in time, and may therefore produce both very small or very high inter-event times. Additionally, irradiation of different areas of the circuit might stimulate different radiation response signatures. These properties fundamentally violate the initial assumption of a periodic modulation of the signal frequency or phase, and therefore prohibit an unambiguous reconstruction of the transient circuit response. Additionally, individual events can not be separated from one another, which complicates calculations of the circuit cross section. One notable exception to this limitation are laser test facilities, which typically allow for precise positioning of a small laser irradiation spot and can generate laser pulses with a known repetition frequency. With careful experimental design, the periodicity assumption can hold in these facilities and the circuit cross section can instead be obtained by raster scanning of the sensitive circuit area. However, events like PLL unlocks can not be reliably analyzed further using this method due to their chaotic behavior in the circuit state space.

An example of this type of irradiation test setup is reported in [63], where a spectrum analyzer is used to characterize the SEE sensitivity of a PLL circuit. In the cited work, detection criteria for SEE were chosen based on the shift of carrier frequency and the amplitude of spurious spectral components. Periodic charge injection is achieved using a two-photon absorption laser system. No time domain representation of the observed SEE responses are reported based on the experimental results. Instead, the authors use simulations of charge injection into the identified sensitive areas to study the transient circuit response.

3.2.2 Time Domain Instrumentation

In contrast to frequency-domain methods, the more commonly followed approach is the use of time domain SEE detection and characterization. In such tests, the phase or frequency of a clock signal produced by a device under test is obtained directly from the time domain waveform observed at the circuit output. The time domain detection of these methods allow for an unknown arrival time of the stimulated circuit responses and do not rely on any assumptions of periodicity, as is the case for frequency domain methods. The circuit output clock and a reference clock might be directly digitized using a high speed digital storage oscilloscope (DSO), such as in [43]. A challenge associated with this method is that of reliable event detection. Off-the-shelf real-time oscilloscopes typically have one significant limitation in this regard, which is the absence of direct trigger capabilities on the phase relationship of two clock signals. While common voltage-based triggering capabilities can be used to detect transient amplitude fluctuations of the circuit output waveform (and potentially detect loss-of-lock conditions, such as in [43]), obtaining phase information from the digitized waveforms requires further data processing. In many instruments, such advanced trigger processing is often available conceptually, but implemented as a software algorithm. Only after a free-running acquisition has been completed and its data is fully processed can a trigger decision be made and the data stored. This typically comes at the cost of significant dead time of the instrument to relevant events, often exceeding 90 % of the total measurement time. While commercial oscilloscopes are capable of obtaining high resolution phase measurements from time domain waveforms, this limitation makes their application impractical when considering the operational constraints of irradiation facilities.

This limitation has been partially addressed by the development of dedicated real-time phase measurement setups with direct phase trigger capabilities. An example of this technique is reported in [64], which utilizes a field-programmable gate array (FPGA)-based TDC and custom trigger logic for detection of SEPT and SEFT. A remaining issue with this concept is its detection sensitivity. The cited work obtains a single-shot resolution and phase error trigger threshold of 390 ps. This resolution is insufficient to verify conformity with the requirements outlined in section 3.1.

An alternative approach consists of using a trigger signal provided by the irradiation facility itself, indicating the time of incidence of a particle or the injection of an energy pulse into the circuit. This is a popular approach applied with laser irradiation test setups [38, 49, 35]. In particular when the position of irradiation is well controlled and repeatable, this approach is very beneficial. In broadbeam irradiation facilities, where the majority of incident particles will not result in any circuit response at all, this is less beneficial, since most of the trigger events do not contribute useful data. In such cases, direct detection of circuit responses is the preferred solution. However, direct acquisition using off-the-shelf

DSOs is often not practical for clock generator circuits. With typically used beam fluxes of about $1 \times 10^5\,\mathrm{cm}^{-2}$ in heavy ion facilities, for example, direct sampling and trigger processing on clock signals in the gigahertz range is feasible with only a very small number of high-end instruments. Due to the immense popularity of broadbeam irradiation experiments using heavy ions, neutrons or protons to qualify circuits for applications in HEP accelerator environments, the following work focuses on enabling direct detection of phase and frequency transients in the time domain without additional trigger information.

3.3 FPGA-based Phase Measurement System

A natural extension to the TDC based phase measurement scheme implemented in [64] is an improvement of its resolution. The architecture outlined below implements a dead time free measurement system capable of directly triggering on the clock signal phase with a time-domain resolution of less than 100 ps. This is achieved by re-purposing the receivers intended for high-speed communication links, which can nowadays be considered a common peripheral of FPGAs. The system described below was implemented using the Xilinx Virtex 7 FPGAs family, however the implementation can be considered portable to FPGAs of other families and vendors. *The contents of this section have been published in [65].*

3.3.1 Circuit Description

The circuit implementation is shown in figure 3.1. The GTX transceivers available in Virtex 7 FPGAs are configured to operate in 'RX CDR Lock to Reference' mode, in which the CDR circuitry is effectively bypassed and instead the deserializer clock is locked to an externally provided reference clock [66]. When this reference clock is derived from the same clock that is used

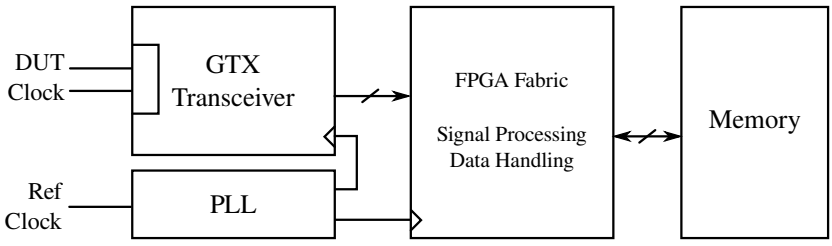


Figure 3.1: Proposed architecture of the proposed FPGA-based phase measurement system.

as a reference for the device under test (DUT), its output clock signal can be sampled with a very high oversampling ratio and fixed phase relationship. If used in this way, the GTX deserializer is effectively being re-purposed as a TDC. Because the GTX deserializer can be operated at data rates up to $10.51\,\mathrm{Gbit\,s^{-1}}$, this mode of operation allows achieving a time bin width better than 100 ps.

Multiple parallel measurement channels can be implemented by using more than one GTX receiver in this configuration. Virtex 7 FPGAs typically offer multiple receivers to be clocked from the same reference clock, allowing synchronous multi-channel measurement systems to be implemented.

3.3.2 Measurement Operation

In the described mode of operation, the GTX core produces deserialized, multi-bit binary data words at a word clock frequency much lower than the deserializer bit rate. Multiple of these data words can be concatenated to capture a full reference clock waveform and the resulting waveform can be transferred into the reference clock domain. The necessary logic required for determination of frequency and phase information is implemented in generic FPGA fabric. This logic only needs to operate at the reference clock period, which makes timing closure straight forward to accomplish. Frequency detection can be realized by counting the number of rising edges in the deserialized data words. Information about the position of the clock signal edges (and therefore information about clock phase) can be obtained by evaluating the location of transitions in the deserialized data word. Many other measurements (such as the presence of glitches in the input clock) can be implemented through simple logic functions similar to the ones described. The implementation of the phase detection logic is illustrated in figure 3.2.

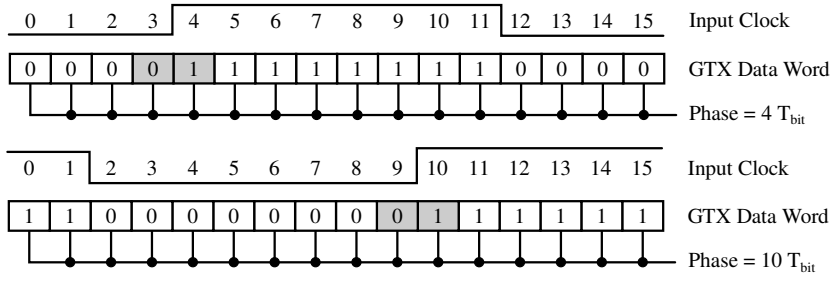


Figure 3.2: Implementation of phase detection operating on deserialized data words. The clock phase is determined by identifying the position of positive transitions in the data word.

The obtained phase information is connected to further processing logic, which implements triggering capabilities and allows storing transient responses of arbitrary length to an on-chip memory. This memory can then be read out for analysis. Additionally, a low-latency trigger signal can be produced at an FPGA output pin, to allow triggering further external instruments, if required. Other applications, such as event counting or time-over-threshold measurements can be implemented this way as well.

3.3.3 Performance Measurements

In order to characterize the measurement performance, the proposed architecture was implemented on a Xilinx Virtex 7 FPGA evaluation platform and one of the integrated GTX receivers was used. The performance of this measurement is determined by the temporal linearity of the deserializer which is used as a differential receiver and TDC.

A DUT reference clock and output clock of 40 MHz were used, from which a GTX reference clock frequency of 320 MHz is synthesized using a PLL integrated in the FPGA. This reference clock is then further used to generate a bit clock of 10.24 GHz for the deserializer. Choosing 10.24 GHz as the deserializer clock frequency has the advantage of being an integer, power-of-two multiple of the chosen reference frequency. This configuration produces 256 deserialized bits per reference clock period (25 ns), which corresponds to a phase resolution of 97.65 ps.

The phase measurement used for characterization of the system was implemented simply by determining the position of a rising edge in the deserialized data word. A triggering system was implemented using a window comparison with configurable window width. A configurable number of phase measurements before and after a trigger event are stored in a dual-port memory for retrieval by the data acquisition (DAQ) system.

Essentially, the DUT clock phase is quantized by means of sampling it with the deserializer bit clock. Similar to quantization processes in the amplitude domain, this time domain quantization is non-ideal and warrants a closer look to better understand the performance of the implemented measurement. For example, deterministic jitter components correlated with the reference clock present on the sampling clock may introduce integral nonlinearity (INL) and differential nonlinearity (DNL) into the measurement. Such nonlinearities can compromise the quality of measurements derived from the digital phase information. Figure 3.3 shows measurements of INL and DNL for the proposed implementation for a complete reference period. These measurements were obtained by advancing the input clock phase in increments of 1 ps. The worst-case INL, corresponding to the largest deviation from a straight-line characteristic of the TDC in the middle of each bin, was found to be approximately 0.05 LSB, while the The maximum DNL is 0.15 LSB. These results are consistent with the

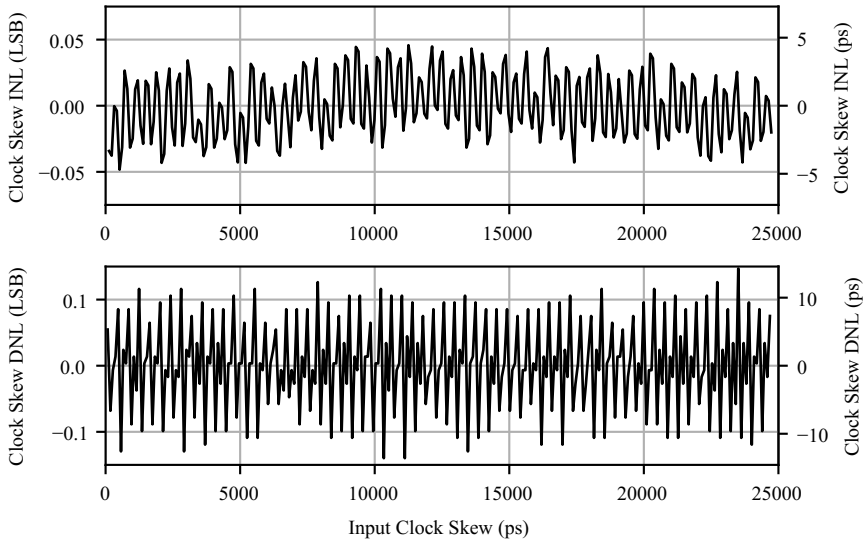


Figure 3.3: INL and DNL measurements of dynamic clock phase estimate.

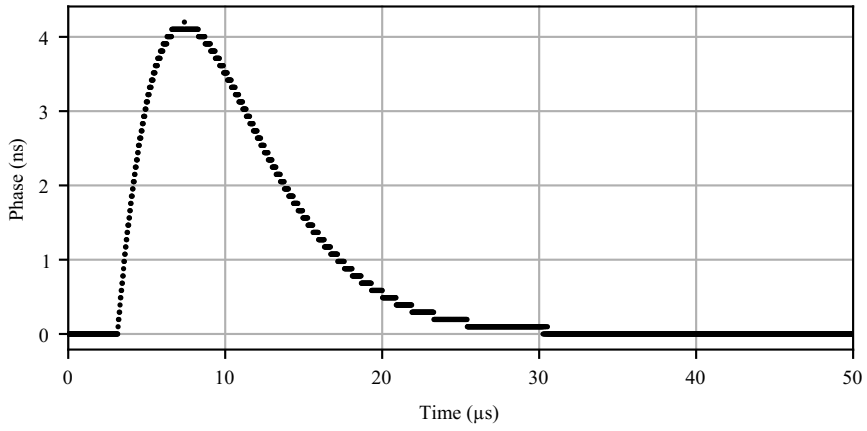


Figure 3.4: Example transient event captured using the implemented measurement concept.

high performance expectations required for adequate performance of the original circuit as a deserializer for high-speed communications. An example transient captured using the implemented method is shown in figure 3.4, highlighting the excellent resolution of this measurement technique.

3.3.4 Summary

A real time clock signal measurement system based on the reuse of high-speed data link receivers available in Xilinx Virtex 7 FPGA has been presented, implemented and characterized. It allows for determination and direct triggering of signal parameters such as frequency and phase as well as the detection of signal glitches in transient measurement applications. Parameter determination, trigger processing and data handling are implemented using generic FPGA fabric, allowing for extensions of the design for more sophisticated measurement tasks and simple integration into larger DAQ systems. An example implementation demonstrated single-shot phase measurement resolution better than 100 ps and dead time free trigger capability on phase transient of this magnitude, which was previously not possible using only off-the-shelf measurement equipment. Multiple channels can be implemented by leveraging multiple high-speed receivers available in the selected FPGA. With the receiver performance improving with recent FPGA generations by moving to data rates upwards of the $10\,\mathrm{Gbit\,s^{-1}}$ presented above, a further improvement in measurement resolution is achievable while utilizing the same measurement concept. As a potential example for further study, the Xilinx Ultrascale+ GTY transceivers supporting non-return-to-zero (NRZ) line rates of $32.75\,\mathrm{Gbit\,s^{-1}}$ can be mentioned.

The described system was used in multiple heavy ion irradiation test campaigns. Its increased detection sensitivity over prior methods enabled the initial discovery of the radiation effect described in chapter 6. Its low-latency trigger generation capabilities were leveraged to obtain sensitivity maps of circuits irradiated using a heavy ion microbeam. These measurements are described in more detail in chapter 6 and highlight the advances made by the presented instrumentation setup.

3.4 Analog Phase Measurement System

A second system was developed with the aim of overcoming the main limitation of DSOs discussed in section 3.2. An analog phase detector circuit was designed, which obtains information about the phase relationship between a reference and DUT clock in the analog domain, and converts this information into a voltage signal. This approach has two main advantages. The bandwidth of the phase information can be limited to significantly below the clock frequency itself. Therefore, the analog-to-digital conversion process can be performed at

significantly lower sample rates, reducing the amount of data to be stored and processed. At the same time, the conversion into a voltage signal re-enables use of the voltage triggering capabilities of commercial DSOs. These can then be used to trigger on radiation-stimulated phase transients directly.

3.4.1 Circuit Description

A block diagram of the proposed analog phase detector device is shown in figure 3.5. The measurement conceptually relies on direct detection of the phase difference between two clock signals. The core phase detection functionality is provided by a commercially available double balanced mixer, the Mini Circuits SYPD-1+. The transfer function of this device is optimized for a wide linear phase detection range, which makes it a suitable candidate for phase measurement applications. Conceptually, its detection range is still limited (to below one half of the input clock period, or 180° of phase shift), but the optimized linearity guarantees a well-defined detection gain within this range. Since its detection gain is amplitude-dependent and highest at large input signal swings, MMIC-based preamplifier stages are implemented at both clock inputs of the device. These additionally present a well-defined impedance to the mixer inputs over a broad frequency range, which is important for obtaining good dynamic mixer performance. The fact that these amplifiers might be driven into saturation by large input signals helps reducing the amplitude dependency of the phase detection gain.

Since not only a DC signal related to the phase difference but also a signal at twice the input frequency is produced at the mixer output, a low pass filter with a cutoff frequency of 10.7 MHz is included in the signal path. A DC calibration output after this filter is available at a front panel connector, which can be used to adjust the static clock phase for maximum detection sensitivity. To

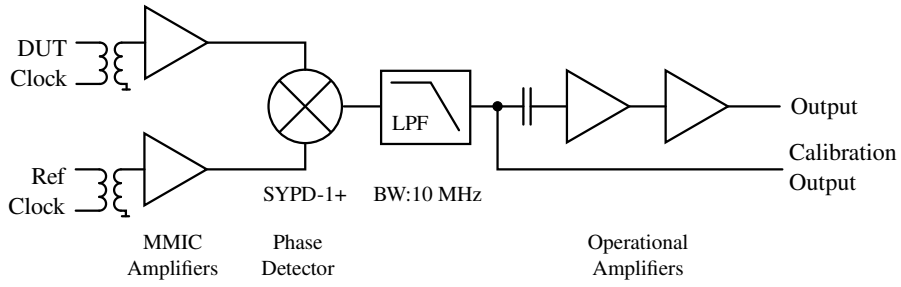


Figure 3.5: Block diagram of the implemented analog phase measurement system. A DC-coupled calibration output is available for field calibration of the amplitude-dependent phase detector gain.

amplify the resulting voltage signal and adequately drive a 50 Ω coaxial cable and oscilloscope input, a two stage amplifier is included following the low pass filter. To avoid amplification of any steady state phase error DC voltage (which would be sensitive to temperature effects and low-frequency wander), the filtered phase detector signal is AC-coupled to the amplifier input. In this manner, a total measurement bandwidth from 300 Hz to 15 MHz can be obtained. The large phase detector gain and the low noise of the operational amplifiers allow the output signal to be dominated by the phase noise of the input clock signals. A photograph of the manufactured device is shown in figure 3.6.

3.4.2 Circuit Characterization

Both the static and the dynamic properties of the developed instrument were characterised experimentally before the circuit was used for irradiation testing. As a first step, the linearity of the phase detector as a function of the input signal amplitude was characterized. Since the amplifier chain of the instrument is AC-coupled and would be readily saturated by large DC offsets, the DC-coupled calibration output of the device was used for this test. The test setup can be seen in figure 3.7. Two signal generators were used to generate differential 80 MHz clock signals with programmable amplitude and phase shift. For each input, amplitudes ranging from 100 mV to 400 mV were characterized. Some results of this static characterization process are seen in figure 3.8. The input amplitude

Figure 3.6: Photograph of the manufactured phase measurement system. Differential clock inputs and single-ended voltage outputs are present on the front side of the device, supply voltage is provided from the back.

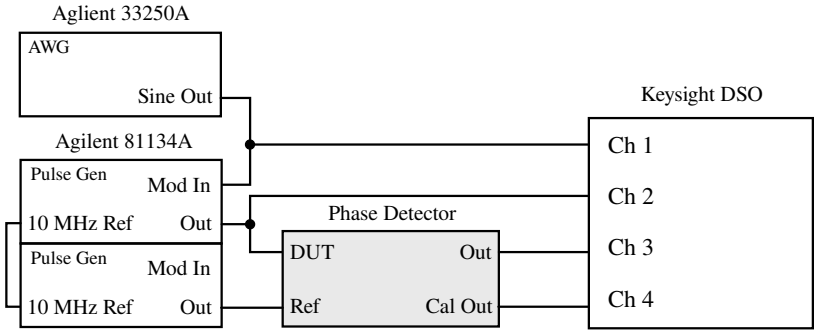


Figure 3.7: Test setup used for characterization of the static transfer function of the phase detector. The characterization process is automated through remote control interfaces of the instruments used.

dependence of the phase detector gain is clearly visible. For input signal swings exceeding 200 mV, the phase detector gain remains within acceptable limits across a ±2 ns phase error, which corresponds to about ±50° of usable range.

After establishing the required signal swing and static phase offset range conditions necessary for proper operation of the circuit, the bandwidth and gain of the circuit across phase modulation frequency was characterized. A clock signal generator is phase-modulated with a known deviation and variable frequency, and the output voltage amplitude is measured before and after the two-stage amplifier in the instrument. This approach allows characterizing the gain of the two-stage amplifier in isolation, which is beneficial for practical use of the instrument. The obtained measurements shown in figure 3.9 confirm the expected bandwidth and gain of the circuit. The noise performance of the measurement system was experimentally validated using two low-jitter clock sources, connected to the inputs of the circuit. The rms voltage noise at the amplifier output was measured using a DSO with sufficient input bandwidth before applying the previously established calibration coefficients. The obtained rms voltage measurement was found consistent with the quadrature combination of the two input jitter values and below 1 ps rms, confirming the noise not to be limited by the instrument itself.

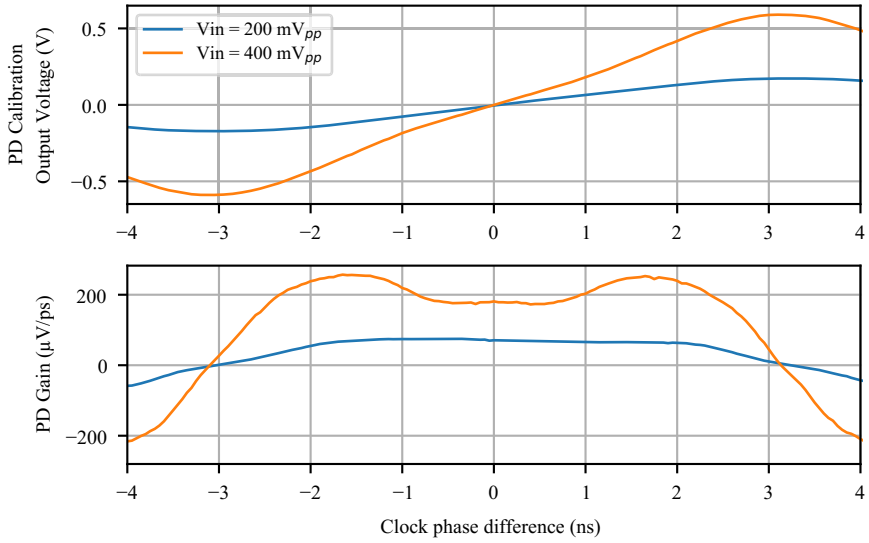


Figure 3.8: Transfer function measurements of the input signal chain for two different signal amplitudes. The phase detector gain is calculated through numerical differentiation of the output voltage measurements along clock phase error.

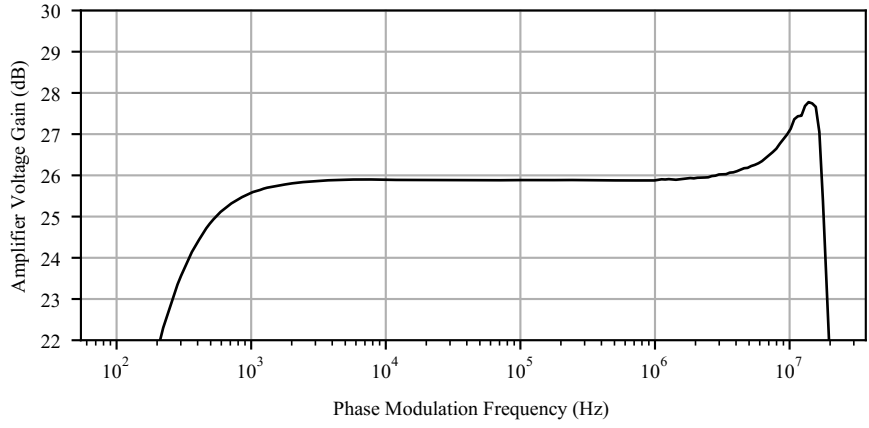


Figure 3.9: Dynamic characteristics of the post-detector voltage amplifier integrated in the phase measurement system. The system achieves a practical measurement bandwidth from 300 Hz to 15 MHz.

3.4.3 Operational Considerations

The anticipated operation of the device is shown conceptually in figure 3.10. The two inputs of the phase detector are connected to the DUT output clock and a reference clock signal, respectively. The output of the phase detector is connected to a DSO for acquisition of transient phase responses. Before beginning the irradiation test, a calibration of the setup is required, which is performed by adjusting the phase of either input signal (reference or DUT output clock signal) until a 0 V output signal at the DC-coupled calibration output of the device is established. This ensures operation around the point of maximum phase detector sensitivity and in the center of its linear region. Since the signal amplitude can be subject to uncertainties in an experimental installation, a simple calibration of the phase detector gain can also be performed. For this, the clock phase is shifted by a small, but known, amount in either direction (using for example cables of different lengths, or a configurable delay line), and the corresponding DC voltage at the calibration output is recorded. The obtained sensitivity can be multiplied by the constant gain of the internal two-stage amplifier to arrive at the system gain in units of $\mathrm{mV\,ps^{-1}}$. Using this system gain, voltage measurements obtained using a DSO can be immediately converted into the equivalent clock signal phase error. The complete calibration procedure can be implemented using only an off-the-shelf digital multimeter (DMM) and was found to be simple and reliable to perform in practice.

3.4.4 Summary

An analog, low-noise phase measurement setup was designed and characterized. Combined with a portable DSO or similar data acquisition system with simple trigger conditioning, transient phase or frequency errors in integrated clock

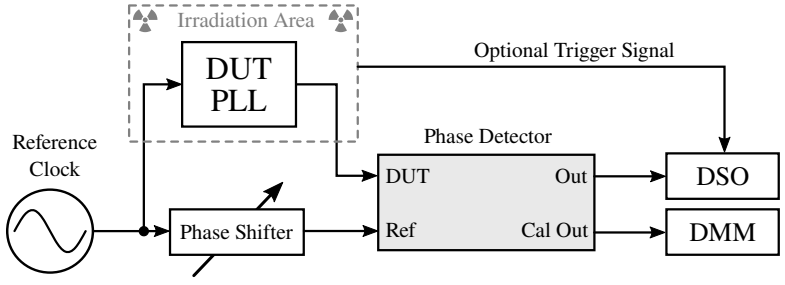


Figure 3.10: Typical operational setup of the phase detector based measurement system. A trigger signal, if provided by the irradiation facility, can be used to control the data acquisition process.

synthesizers can be detected down to the level of the total clock jitter. The system operates independently of any facility-provided trigger information. The significantly reduced bandwidth of the phase information compared with a direct analog-to-digital conversion of the clock waveform was also demonstrated to allow triggerless storage of all obtained voltage data to a storage medium. This allows performing all event detection tasks in post-processing, where the operational time constraints of a test facility are not an issue. More sophisticated signal processing, such as additional filtering or histogramming can also be performed offline in this way. Another interesting application is the generation of low-latency trigger signals using a simple voltage comparator connected to the instrument. This would allow for triggering of other components of the instrumentation setup, and can enable precise time-tagging of any detected event. Additionally, the manufactured device is small and portable, which makes it a low-profile and low-cost addition to volume-constrained test setups.

The developed instrument was used together with a USB oscilloscope during multiple heavy ion irradiation campaigns, where it enabled the characterization of the developed All-Digital PLL circuit described in chapter 5, as well as the research on radiation effects described in chapter 6.

3.5 Digital Phase and Frequency Measurement System

To further extend the SEE characterization capabilities for PLL and oscillator circuits, a third instrumentation system was implemented. Instead of analog implementation of any phase discrimination, this system uses a flexible commercially available RF receiver frontend and fully relies on digital signal processing (DSP) techniques to obtain phase and frequency information of an input signal.

3.5.1 System Description

A block diagram of the developed system is shown in figure 3.11. The hardware component of the system is formed by a Nuand bladeRF software-defined radio (SDR) [67], which integrates a Lime Microsystems LMS6002 RF frontend with integrated data converters [68], an Altera Cyclone IV FPGA as well as a USB3.0 bridge based on the Cypress FX3 chip set. The hardware supports an input frequency range between 300 MHz and 3 GHz, and in its basic configuration offers transparent transfer capabilities of the samples obtained through the on-board ADCs to a host computer. The frontend integrates down-conversion of the RF signal bandwidth to complex baseband, and an integrated frequency synthesizer generates the required in-phase and quadrature local oscillator (LO) signals. The implemented system makes use of this complex baseband

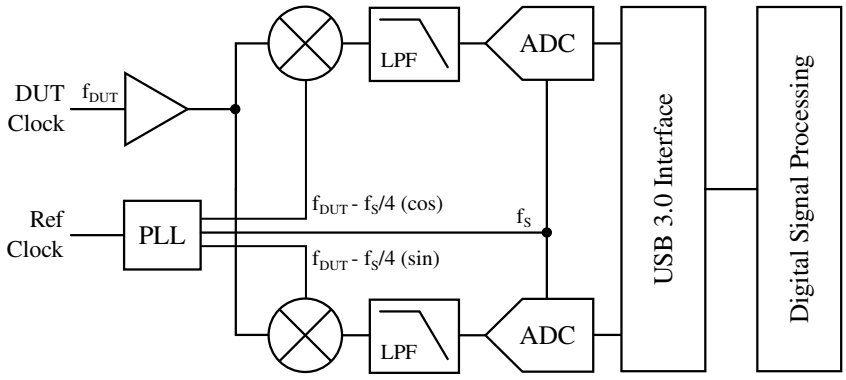


Figure 3.11: Block diagram of the digital phase and frequency measurement system. Most shown functionality is provided by the nuand bladeRF hardware, the desired measurement is implemented as a custom DSP software flow.

signal by implementing signal processing algorithms for phase and frequency measurement on the connected host computer. Since the RF frontend utilizes an integrated CMOS PLL as a local oscillator for down-conversion, the jitter performance of the instrument is limited to the level of its performance. However, since the intended application for this frontend is in the domain of cellular communications, a synthesizer that allows obtaining sub-picosecond rms jitter measurements is available.

An important aspect for implementing a high performance measurement based on this frontend architecture is appropriate frequency planning. The simplest implementation would choose the LO frequency identical to the RF carrier frequency. Following a phase coherent down-conversion, a phase error then directly manifests as a DC component of the baseband outputs, where they can be easily detected. Since the RF frontend is itself a CMOS integrated analog circuit, it is only able to achieve finite suppression of LO leakage and DC offset on its baseband outputs. Additionally, at low frequency, the baseband outputs are affected by $1/f$ noise. Both these issues could severely affect the quality of obtained measurements severely if not sufficiently suppressed. Sufficient suppression can be achieved by frontend calibration, however this comes with the additional complexity of accounting for second order effects, such as temperature and long term stability.

These issues are instead avoided systematically by adopting a low-intermediate frequency (IF) down-conversion approach: The LO frequency is chosen such that the RF carrier is down-converted to an intermediate frequency of $f_S/4$, where f_S is the ADC sampling frequency. This particular choice is advantageous, since

it simplifies the necessary digital signal processing for further down-conversion to DC as described below. At sample rates in the megahertz range, this intermediate frequency is also sufficiently separated from the spectral components around DC, resulting from LO leakage and $1/f$ noise. This allows suppressing these components using low-complexity digital finite impulse response (FIR) filtering.

3.5.2 Digital Signal Processing

The signal processing flow for phase and frequency detection operating on the digitized in-phase and quadrature outputs of the RF down-converter is shown in figure 3.12. The initial processing step implements the down-conversion of the low-IF signal to DC. Due to the advantageous choice of $f_S/4$ as the intermediate frequency, the digital mixing process simplifies to a cyclic multiplication with a sequence of $+1$ and -1, avoiding costly trigonometric operations [69]. Low-pass filtering is implemented in the following stage, to suppress any (now up-converted) DC component. The phase of the RF carrier is obtained using a four-quadrant arctangent operation applied to the quadrature and in-phase components ($\varphi = atan2(Q(k), I(k))$). This function has two important properties as a phase discriminator: The four-quadrant arctangent operation is free from ambiguity across the full 360° range, so phase measurement is possible regardless of the phase relation of the LO and RF input signals. Additionally, the expression is amplitude invariant. The result is a fixed phase detection gain, independent of the RF signal amplitude. Further, no calibration or adjustment of the setup for operation in a certain operation point is required. Direct analysis of the phase

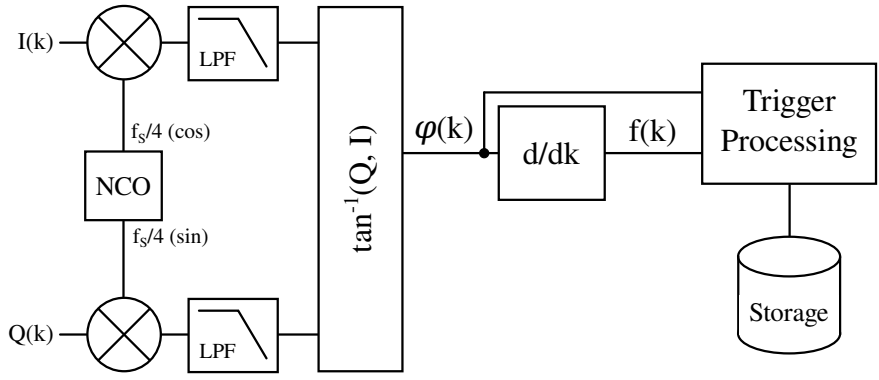


Figure 3.12: Block diagram of the implemented digital signal processing flow. The conceptual computation process for both phase and frequency signals is shown, and triggered or triggerless storage to disk can be implemented.

information including trigger processing can be performed on the obtained phase information at this point. However, due to the linear, ambiguity-free phase detection capabilities of the system, it was also readily extended to perform low-noise frequency measurements. Following the definition of frequency as $f = {}^{d\varphi}/_{dt}$, the time series of phase measurements can be differentiated to obtain a transient frequency measurement. Trigger processing and storage capabilities have been implemented to operate on frequency measurements as well.

To obtain optimal performance, the signal processing chain described above was implemented as a multi-threaded C application, utilizing the Nuand bladeRF C application programming interface (API) as well as the Vector Optimized Library of Kernels (VOLK) library [70] for the required digital signal processing. In this manner, a real-time processing throughput exceeding 20 Msps could be achieved on a customer-grade notebook. This allows the system to be operated during irradiation tests without requiring costly or specialized hardware.

3.5.3 Summary

The implemented test system further increases the flexibility of test setups over the developments presented in the previous sections. High-resolution and low-noise measurements of frequency and phase can be obtained, which makes the system very useful for both the characterization of PLL circuits as well as free-running oscillators. One noteworthy shortcoming of the system as implemented is its inability to generate electrical trigger output signals with low and deterministic latency. All trigger processing is currently performed in software running on a host computer running a non-real-time operating system. Additionally, the RF frontend is connected to this computer through a USB interface, which does not offer real-time guarantees to the application. Since the used hardware already includes an FPGA, a natural extension of this work could implement the digital signal processing within the FPGA fabric, where its latency can be significantly reduced and determinism can be guaranteed.

Nonetheless, the frequency measurement capabilities have been successfully applied in practice during the characterization of radiation responses stimulated in an integrated LC oscillator circuit. The particular challenge of obtaining transient, high-resolution frequency measurements of a free-running oscillator circuit was addressed by the developed instrument and led to important insight into the underlying radiation effect. The corresponding measurements obtained with this system are reported in chapter 6.

3.6 Comparison and Summary

Three different instrumentation options for SEE testing of clock distribution and synthesis circuits have been developed. Table 3.1 shows a comparison of a number of key properties of each system. Incremental improvements in the systems have allowed closing the initially identified gap between existing instrumentation setups and the requirements of future detectors and high speed data links. Practical use of each of the developed systems was demonstrated in multiple irradiation campaigns. The availability of multiple systems with overlapping capabilities gives additional flexibility in choosing the ideal setup for a given irradiation campaign. The various benefits and capabilities of the developed instrumentation systems will become readily apparent in the following chapter 5 and chapter 6, where they are used to characterize manufactured circuits and study radiation effects to a level not accessible with previously existing instrumentation.

Based on their specific characteristics, the following comparative recommendations for the application of the developed systems can be given: In situations where scalability and high integration with a larger test system is important, the FPGA-based system is a very good candidate, as long as the requirements for phase resolution and event detection thresholds are moderate. This system is also able to provide a low-latency trigger signal for other parts of the instrumentation. In situations where the highest resolution and event detection efficiency are required, the analog or digital phase measurement system are the appropriate choice. In situations where the generation of a low-latency trigger signal for other electronics is required, the analog system is more straight-forward to apply, while the digital system can provide a self-contained solution without this capability. For the special case of high-precision measurements of oscillator frequencies without an active phase control loop, the digital measurement system can readily be used in frequency measurement mode.

Instrumentation System	FPGA-based Phase Measurement	Analog Phase Measurement System	Digital Phase and Frequency Measurement System	
Type of Measurement	Phase	Phase	Phase	Frequency
Measurement Principle	TDC	Mixer-based Phase Detection	Downconversion to complex baseband + DSP	
Design Challenge	Digital Circuit Design	Analog Circuit Design	DSP Design and Implementation	
Resolution	100 ps	<1 ps	<1 ps	<1 ppm
Measurement Range	±180°	±50°	±180°	±2 MHz
Sampling Rate	40 MHz	20 MHz	20 MHz	20 MHz
Measurement Bandwidth	0 - 20 MHz	300 Hz - 10 MHz	0 - 5 MHz	0 - 5 MHz
Measurement Limit	Quantization Noise	Device Noise	Internal PLL Jitter	
Event Detection Threshold	±50 ps	±20 ps(1)	±20 ps(1)	±20 ppm(1)
Post-Trigger Dead Time	none	none	none	none

Table 3.1: Comparison of the developed SEE instrumentation systems for frequency synthesizers.

Note 1: Detection threshold limited by peak-to-peak random jitter of DUT and reference clock.

Chapter 4

Radiation-Tolerant All-Digital PLL Design

A need for dedicated radiation-tolerant PLL circuits has emerged in the domain of electronics for HEP experiments at least with the beginning of the LHC era. Essentially all the developments in this domain have adopted conventional charge pump-based architectures, and some examples include [71, 72, 73, 74]. Significant efforts have been made in understanding the radiation sensitivities of these circuits, the development of mitigation strategies and an adoption of more radiation-tolerant circuit topologies [75, 37, 76, 64]. The recently emerging need for low-jitter clock generation circuits for the high speed communication links and high precision timing detectors to be deployed in High Luminosity LHC upgrades have led to the development of LC-VCO-based PLL circuits. These developments represent the current state of the art of radiation hardened frequency synthesizers in the field of HEP [77, 62].

Outside of the domain of radiation-tolerant circuit implementations, the conventional charge-pump based PLL architecture has undergone an evolution into the all-digital phase-locked loop (ADPLL) in order to cope with the challenges of technology scaling and the increasingly digital nature of integrated circuits generally [21]. This digital-intensive approach to PLL design has already proven itself to enable the implementation of phase locked loops within the constraints of even the most advanced CMOS design nodes [78].

Even though many aspects concerning the design, analysis and performance of these all-digital architectures are well-studied [22, 79, 25], there exists only a small body of literature concerned with radiation-tolerant implementations. While the general nature of SEE sensitivities in relevant ADPLLs architectures is understood [80, 81], their characterization has been limited to behavioral simulations and the use of FPGA-based fault injection experiments. A theo-

retical framework useful in analysis and description of these sensitivities has been reported based on these studies [82]. These studies reveal show a focus on the digital components of the ADPLL circuits, namely the phase detector, the digital loop filter (DLF) and the feedback divider. In each of these, sensitivities to SEEs have been analyzed and identified using behavioral models and gate-level implementations. A susceptibility of the to SEPTs and SEFTs of ADPLL circuits is acknowledged and can be associated to the location of injected faults. For components such as the DLF, where information is stored as binary-weighted data words, a further difference in sensitivity corresponding to the weighting of the corrupted data bit is evident. Corruption of bits with little significance is often associated with recoverable fault conditions, such as a temporary phase excursion of the PLL. On the other hand, corrupting bits of high significance was instead found to potentially result in an inability of the circuit to re-acquire phase lock.

Two main shortcomings of the existing studies can be identified: Firstly, the chosen modeling approaches do not discuss structural or circuit-level sensitivities of the DCO. The DCO represent a critical mixed-signal block and fundamentally defines the performance of PLL circuits. As such, further studies on the radiation sensitivities present in different types of DCO circuits are crucial for successful implementations of radiation-tolerant ADPLLs. Secondly, while a number of sensitivities are identified and modeled in the remaining components, no particular emphasis has yet been put on the exploration of mitigation strategies and their applicability to practical circuit implementations. Additionally, no radiation hardened implementations have been presented in the contemporary literature and therefore experimental characterization results of such circuit implementations also remain unavailable.

In an attempt to address these issues, the following chapter is concerned with the design and implementation of a radiation-tolerant ADPLL circuit compatible with the requirements of contemporary and future HEP experiments. This chapter first consolidates a number of further considerations motivating the adoption of radiation-tolerant ADPLL implementations. Appropriate circuit specifications are derived by considering two common use cases and a detailed analysis of their common and specific requirements. The remainder of the chapter presents details of various design aspects, with a particular focus on the relevant radiation hardening considerations.

4.1 Motivation

Chapter 3 has already identified the different developments leading to of a significant tightening of the requirements for PLL circuits. At the same time, the HEP ASIC design community is continuing to exploit the capabilities of more advanced CMOS design nodes for their improved power-performance-area (PPA)

capabilities as well as their significantly better radiation tolerance. While digital circuits generally benefit from this technology scaling, the performance of analog circuits typically deteriorates as a consequence of the supply voltage scaling required to retain reliable circuit operation with reduced gate oxide thicknesses used in advanced technologies. The conventional charge-pump PLL architecture is a prime example of a precision analog circuit suffering from this supply voltage scaling. An underlying premise of all-digital PLL implementations is that in such advanced CMOS nodes, the available signal-to-noise ratio obtained from time-based signal processing exceeds that of its voltage-based equivalents [22], and as such digital implementations can provide performance benefits over their conventional counterparts.

On top of the reduction of circuit performance, the design effort required for analog circuits in these technologies also significantly increases. This is a result of a number of confounding issues: In addition to design difficulties resulting from supply voltage scaling, stricter lithography requirements dictate increasingly constraining design rules, while increased interconnect resistances require careful considerations of parasitics, electromigration and power distribution network integrity issues. In the domain of electronics for HEP, the additional need for verification of requirement-compliant operation in increasingly harsh radiation environments requires further complex considerations on top of these challenges.

When instead considering digital circuits, a significantly different design space is found in advanced nodes: Digital circuits, when described using commonly used hardware description languages (HDLs), possess very high potential for technology portability. A large amount of the new complexities of advanced CMOS nodes are absorbed by automatic place and route (P&R) methodologies provided by advanced EDA tools instead of the circuit designer. Moving to a more advanced technology node is normally associated with an increase of digital circuit performance and a simultaneous reduction in power consumption and area. At the same time, the HEP community has developed similarly automatic methodologies to insert the required protection against radiation effects into digital circuit designs. An example of this is the TMRG tool [83], which partially automates the hardening of RTL circuit descriptions using TMR schemes. Due to the mostly technology-independent description of digital logic, these efforts seamlessly translate to newly adopted technology nodes. The verification of compliance with radiation tolerance requirements for digital circuits can also be considered a technology-agnostic problem: With any given digital circuit being modeled as a combination of sequential and combinatorial logic cells, verification of SET and SEU robustness does not depend on technology-specific information. This implies that automation can be exploited in this domain as well.

Based on these considerations, ADPLLs offer many appealing properties that address the various challenges identified before: Replacing the majority

of sensitive analog circuits by their digital counterparts has the potential of significantly reducing the required design effort, especially when moving towards more advanced design nodes. In these digital components, the established methodologies for systematic radiation hardening and verification of SEE tolerance can be applied automatically. Modern, scalable approaches to verification of these digital designs can be used, increasing the achievable complexity of PLL circuits and in turn their capabilities. As a positive side-effect, the resulting designs can be reused more easily in new developments or different technologies.

The well-established theoretical foundations of all-digital PLL circuits and the existence of a conceptual framework for analysis and mitigation of their radiation sensitivity strongly motivate the exploration of these circuits as a design enabler for future HEP ASIC developments.

4.2 Requirements Analysis

To evaluate the ADPLL concept and its potential for future applications based on a realistic application scenario, two relevant use cases for such a circuit in front-end ASICs have been selected based on the typical TTC architecture adopted in LHC experiments that was introduced in chapter 1.

In current deployments, a typical front-end ASIC represents the receiving end of either a low bit rate ($80\,\mathrm{Mbit\,s^{-1}}$ to $320\,\mathrm{Mbit\,s^{-1}}$) serial data link or a 40 MHz to 320 MHz reference clock. Since these clock or data signals are themselves coherent with the LHC bunch crossing clock, front-end level synchronization to the accelerator facility can be achieved by using appropriate clock recovery techniques. To replace existing systems in this regard, a requirement for operation as either a PLL or a CDR circuit at any of the above-mentioned data rates or clock frequencies can be identified.

Many systems require not only a simple regeneration of a given reference clock frequency, but also the synthesis of multiples of this frequency, for example to enable serialization of data at higher data rates in the uplink direction. Currently deployed front-end systems utilize uplink data rates of up to $1.28\,\mathrm{Gbit\,s^{-1}}$ per link. This establishes the synthesis of clock frequencies up to 1.28 GHz from any of the given input signals as a reasonable requirement for the ADPLL circuit to be designed.

Systems differ in the level of fidelity required of the regenerated and derived clock signals, particularly their jitter performance. A large number of systems require only reliable recovery of the clock signal and the data transmitted over a low-speed serial link, without imposing stringent constraints on total jitter of the obtained signal. Such systems profit from reduced area or power consumption of clock generator circuits. A smaller set of systems additionally require the jitter of the produced clock signals to be significantly lower. Section 3.1 has already summarized some typical requirements of such systems.

Since fundamentally, the PLL output jitter is composed of components of the reference clock and the controlled oscillator, the relevant trade-off space is located in the oscillator and loop filter design: Where higher composite jitter can be tolerated, oscillators with reduced power consumption and performance can be used. In cases where large amounts of jitter are expected on the reference clock, more stringent jitter requirements can be fulfilled only by inclusion of a low-jitter oscillator inside the PLL itself. Together with an appropriate choice of the loop filter transfer function, high frequency components of the reference clock jitter can be suppressed, improving the jitter performance of the PLL output clock signal. Due to the significant PPA trade-offs that these different varying requirements allow, different oscillator topologies are adopted for these different use cases.

Regardless of the required clock quality, a number of common secondary requirements and constraints for PLL circuits operating on the LHC accelerator clocks can be identified. A first requirement is imposed by the dynamics of the clock signal. During the accelerator cycle, the bunch crossing clock frequency changes as the particle energy is increased. This change of frequency is globally propagated to all accelerator and experimental systems, and therefore dictates their required locking range and dynamic input tracking capabilities. The magnitude of this change however, even for heavy ion acceleration cycles in the LHC, remains below 15 ppm. Since the acceleration process is performed over a time scale of minutes, it results in only a very small frequency ramp rate on the order of not more than $25\,\mathrm{ppb\,s^{-1}}$. Another common requirement is tolerance to TID and SEE. The TID tolerance needs to equal or exceed the specifications for all other components typically integrated in the same front-end ASIC. For developments targeting the High Luminosity LHC upgrade, designs of the most demanding inner detector layers have baselined TID specifications between 500 Mrad and 1 Grad accumulated over their multi-year lifetime [84]. Extremely strict SEE tolerance requirements are the consequence of further system level considerations: Most ASICs include only a single PLL or CDR circuit to generate all internal clock signals, and many of them distribute these clocks or derived data signals to further off-chip electronics components. This makes clock generation a potential cause of fault propagation, where a single functional interruption affects many downstream circuits systems. The reliability of clock generator circuits in radiation environments must therefore be maximized, which implies striving for systematic mitigation of SEEs to the largest possible extent.

Based on the identified set of requirements of front-end ASICs applications, the following evaluation approach is pursued. A suitable All-Digital PLL and CDR architecture, accommodating all the common needs of the previously described systems, will be identified. The differences in the required jitter performance for different types of systems are addressed with a study of two

different DCO topologies. A ring oscillator flavor is proposed to satisfy the needs of applications with less stringent jitter requirements, while an LC DCO is included to provide significantly improved jitter performance at the expense of additional circuit area. Aspects of radiation tolerance will be addressed within the DCO design process where appropriate. The designs are further partitioned such that all requirements common to both ADPLL circuits can be fulfilled by a shared set of core digital loop components. For these components, suitable radiation hardening approaches for SEE and TID tolerance will be selected and implemented. The design of all circuits will be performed in a 65 nm bulk CMOS node, which enables comparisons with contemporary developments of conventional PLL designs using the same technology node. To additionally allow fair comparisons between the different designed ADPLLs, the developed circuits will be sized for similar power consumption in typical operation conditions.

4.3 Bang-Bang All-Digital PLL Architecture

In order to propose a suitable architecture for the designed circuit, it is crucial to re-examine the simplified block diagram shown in figure 2.2 in light of the identified requirements. One important architectural consideration is an appropriate choice of TDC architecture.

In PLLs with integer feedback divider ratio in steady-state conditions, the phase error between the reference and feedback clocks will have a zero mean value, with small instantaneous deviations only resulting from random clock jitter. Considering the typically small levels of jitter (on the order of picoseconds) relative to the reference clock period, it becomes apparent that a significant range of any imaginable TDC would be unused, at least in the absence of large perturbations to the loop. From a power standpoint, this dictates reducing the range of the TDC down to the smallest level utilized in steady-state operation. On the other hand, physical limitations on the achievable single-shot resolution of a TDC exist. In the chosen 65 nm process node, typical inverter delays (a reasonable estimate for the bin size of a delay line based TDC) are on the order of 15 ps. This implies, that for typical jitter values on the order of 1 ps rms, its peak-to-peak deviation will only rarely exceed two bins of such a TDC. When operating in this regime, in which the results obtained by the TDC alternate only between two adjacent values, the TDC does not provide useful information on the magnitude of the phase error to the loop. Instead, the two utilized bins are representative only of the sign of the instantaneous phase error. Since a wide range and high resolution TDC is normally a significant contributor to the power dissipation of ADPLL circuits, significant power savings can be achieved when it is replaced by a binary phase detector. One implementation of such a bang-bang phase detector (BBPD) - in fact equivalent to a single-bin delay line TDC - is the D-Flip-Flop, which may be used to sample the state of one

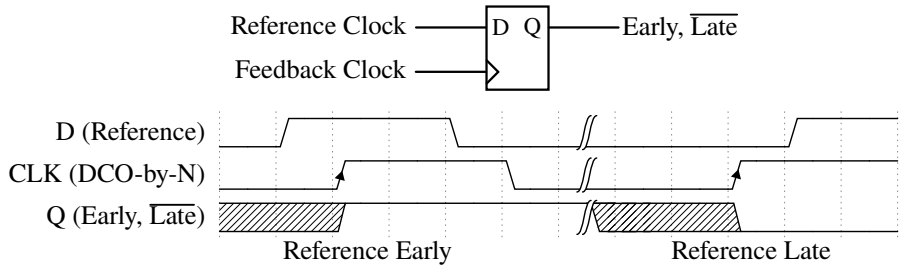


Figure 4.1: Phase detection capabilities of a D-Flip-Flop when configured as a BBPD.

clock at the rising edge of another. This sampled state represents the sign of the phase difference between both clocks, as illustrated in figure 4.1.

The loss of magnitude information to quantization error also transforms the bang-bang all-digital phase locked loop (BBADPLL) into a nonlinear feedback system. Nonlinear PLL circuits have a heritage in conventional PLL design, and are found for example in some CDR systems utilizing binary phase detectors such as the Alexander phase detector [27]. Outside of the domain of ADPLL [79] and CDR applications, BBPDs have also been used in charge-pump based Integer-N PLL circuits [85, 86]. Therefore, the resulting system dynamics are well-studied overall in the literature. The choice of a BBPD nonetheless justifies a number of additional considerations. While alternatives to delay line TDCs exist that achieve better single shot resolution than a typical inverter delay, their implementation may add significant power consumption without notably improving the PLL jitter performance. A better approach, especially when the flexibility offered by digital circuit implementations is available, might be the use of only a BBPD and accepting the resulting system dynamics associated with the nonlinear control system.

Analysis of System Dynamics

The design of such nonlinear feedback systems necessitates a significantly different analysis approach than the one used for designing conventional PLL circuits with linear phase detectors. While TDC-based ADPLL circuits can be designed using analogies to the conventional charge-pump PLL, this is not a generally viable approach for BBADPLLs [23]. While linearization might be possible at certain subsets of operating points using a careful analysis of the effective BBPD gain, the design and sizing process of this type of system often resorts to numerical simulations instead. Ideally, a hybrid approach combining simplified theoretical analyses and numerical studies is used to study the system

dynamics and verify compliance with specifications. An excellent example of this approach, guiding the design process described below, can be found in the works of Da Dalt [25, 79]. The most significant contributor to difficulties in analysis is the variation of the BBPD gain as a function of the input jitter distribution and the dynamics of the PLL. While in a noiseless system, a nonlinear phase detector offers infinite detection gain, the presence of jitter on either clock input reduces the peak gain. When considering large amounts of Gaussian reference clock jitter $\sigma_{t_{\mathrm{jr}}}$ its gain typically follows

$$K_{BBPD} \approx \frac{2}{\sqrt{2\pi}\sigma_{t_{\mathrm{jr}}}} \tag{4.1}$$

as shown in [25, p. 57]. Such a significant variation of the loop gain results in considerable changes of dynamic loop parameters such as bandwidth and damping. In the limit of small reference clock jitter, such approximations additionally become increasingly inaccurate. Further complications arise from the jitter distributions encountered in practical scenarios making an exclusively analytical approach to the study of such nonlinear dynamics infeasible. Instead, a simulation-based approach to the study of these dynamics is essential.

Frequency Detection Capabilities

BBPDs as well as many binary phase detectors for CDR operation do not provide useful error information in the presence of large frequency differences between their inputs. Their lack of inherent frequency detection capabilities reduces the pull-in range of PLL and CDR circuits utilizing such nonlinear phase detectors. To overcome this limitation, additional frequency detection capabilities are required to guarantee reliable circuit operation, particularly during start-up.

Radiation Tolerance Considerations

As outlined earlier, the general nature of SEE sensitivities in all-digital PLL circuits without any applied hardening has been reported in the literature before [81, 80]. These studies show that bang-bang PLL architectures exhibit some inherent robustness due to their use of a nonlinear phase detector. As discussed in section 2.3, linear phase detectors suffer from SEE sensitivities due to their high dynamic range and low detection gain. SEUs can propagate through the loop filter and can result in significant phase errors in the loop. Using a nonlinear BBPD, the phase detector output ideally represents a zero-mean sequence of binary decisions resulting from random timing error at its input. A single decision error due to SEU or SET will therefore not result in any significant phase error accumulating in the loop, and can in practice become entirely indistinguishable from random noise. The cited studies also show that

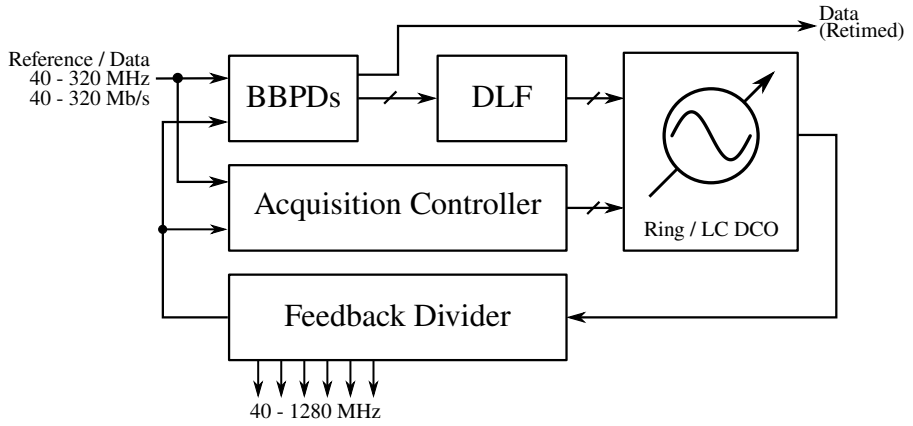


Figure 4.2: Basic architecture of the implemented bang-bang ADPLL and CDR circuit.

further SEE sensitivities exist within the following digital loop components, in particular the DLF. The availability of semiautomatic circuit hardening techniques applicable to the EDA-tool based digital design flow suggests their mitigation using established redundancy insertion methodologies, as will be shown later.

Block-Level Overview

The basic architecture of the BBADPLL circuit emerging from all of the above considerations is shown in figure 4.2. The TDC is replaced by different BBPD options, allowing operation as either a PLL or a CDR circuit. The output of these BBPDs is processed by a digital loop filter, the output of which is applied as a digital frequency tuning word to the DCO. A frequency acquisition controller complements the loop with the required frequency detection capabilities not provided by the BBPDs by implementing a binary open-loop frequency search. As such, it can be disabled after the frequency acquisition process is finished, when feedback control of the PLL is engaged. Following the requirements derived in section 4.2, this architecture anticipates substituting the DCO by either an LC-tank oscillator (LC DCO) or a digitally controlled ring oscillator (DCRO). The following two sections will present the designs for both these oscillator types before describing the design and radiation hardening of the digital loop constituents in more detail.

4.4 Varactorless LC DCO Design

Some of the material covered in this section has been published in [87]. The achievable performance of an LC oscillator with an on-chip tank depends on the selection of an appropriate oscillation frequency. Based on the previously outlined PLL requirements alone, any integer multiple of 1.28 GHz might be considered. One primary driver for this decision is the required value of tank inductance. The large inductance values required to obtain low oscillation frequencies result in increased area requirements and higher resistive losses in the inductor. Lower oscillation frequencies often therefore result in reduced tank quality factors and hence a degraded jitter performance. On the other hand, very high oscillation frequencies and the correspondingly smaller inductance values increase the design sensitivity to layout-dependent parasitics. Additionally, high-speed divider circuits capable of operating at high frequencies become a challenging design aspect and increasingly dominate the power dissipation of the circuit.

Based on these considerations, an LC DCO operating frequency of 2.56 GHz was chosen. When considering the overall area, inductor quality factor and power consumption of the DCO and clock divider circuits, this center frequency provides a suitable trade-off. The chosen frequency is low enough to allow the implementation of even the high-speed divider in the feedback path exclusively using CMOS circuits in the chosen technology. This reduces power consumption and complexity compared to the current-mode logic (CML) implementations often used at higher frequencies, such as for the 5.12 GHz oscillator presented in [39]. The required spiral inductor, while large, still provides an acceptable quality factor.

4.4.1 Circuit Description

A differential oscillator topology using cross-coupled NMOS and PMOS pairs is used, as shown conceptually in figure 4.3. Bias current regulation is provided by an NMOS tail current source. The complementary-cross-coupled pair architecture is chosen not only for the current reuse it provides, but also for its promise of high TID tolerance. In this topology, the voltage swing of the oscillating nodes remains within the limits of the supply voltage. This allows the use of thin-oxide transistors for the cross-coupled pair without reliability concerns. Compared to thin-oxide (core) transistors, the thick-oxide devices required for larger oscillation amplitudes were shown to degrade significantly more strongly with TID in the chosen technology [88].

The maximum oscillation frequency is established by means of a fixed inductor and an appropriate amount of bulk capacitance forming the tank. The required inductance of 1.6 nH is implemented using an on-chip two-turn spiral

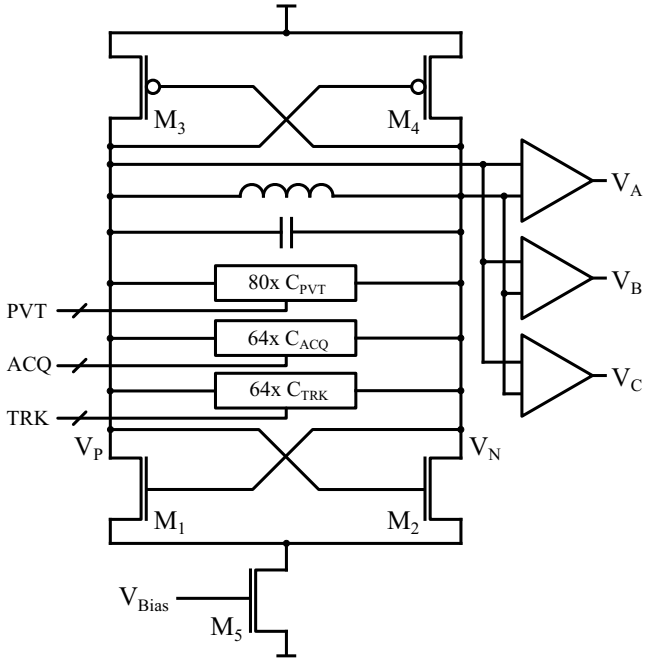


Figure 4.3: Schematic of the digitally controlled LC oscillator with redundant output buffers. Its frequency is controlled using PVT, acquisition (ACQ) and tracking (TRK) banks. Only the tracking bank is used for closed-loop control.

inductor. The bulk capacitance is implemented using interdigitated metal-oxide-metal (MOM) capacitors directly attached to the tank. Digital frequency control is implemented using three distinct banks of switched capacitors, similar in their logical segmentation to DCO designs such as [20]. To cover the expected process and TID-related variations, the DCO design targets a tuning range of 20%. The majority of this range is covered by a coarse PVT bank (C_{PVT}), which is segmented into four binary-weighted LSB cells and four additional thermometric MSB cells. Each cell in this bank is implemented using MOM capacitors and NMOS switches, with the smallest binary cell implementing a 12.5 fF capacitance difference corresponding to a frequency step size of 6.5 MHz at 2.56 GHz. A smaller acquisition bank (C_{ACQ}) implements additional frequency tuning capabilities to ensure optimal frequency centering for closed loop operation. This bank is implemented using 64 thermometric cells. Each unit cell adds 600 aF of capacitance to the tank when enabled, providing a frequency step size of 320 kHz. Both the PVT and the acquisition bank cells are implemented using the bottom-pinning switch architecture presented in [89].

A circuit schematic of this topology is shown in figure 4.4. While its behavior in the on-state is similar to conventional resistive biasing techniques [90] and mostly dictated by the large switch device M_{SW}, this topology offers advantages in the off-state of the cell. By pinning the bottom of the oscillation waveform at nodes $\mathrm{V_A}$ and $\mathrm{V_B}$ at $\mathrm{V_{Bias}}$ - $\mathrm{V_{th,nmos}}$, which can be close to the ground potential, oxide stress of the main switch device is minimized. Additionally, the biasing scheme establishes the exact amount of conductivity of the transistors $\mathrm{M_{PIN}}$ required to compensate any leakage currents from the nodes $\mathrm{V_A}$ and $\mathrm{V_B}$ (through $\mathrm{M_{PD}}$ or $\mathrm{M_{SW}}$), which maximizes the off-state quality factor. Aside from the series switch transistor, minimum-size devices can be used to implement this cell, which minimizes parasitics and area of the cell. A particular area advantage arises from the avoidance of large on-chip resistors, which are required for biasing in the conventional switch topology. For the capacitance $\mathrm{C_{MOM}}$, foundry-provided MOM capacitors are used, which are well-characterized for the range of values required in the PVT and acquisition cells.

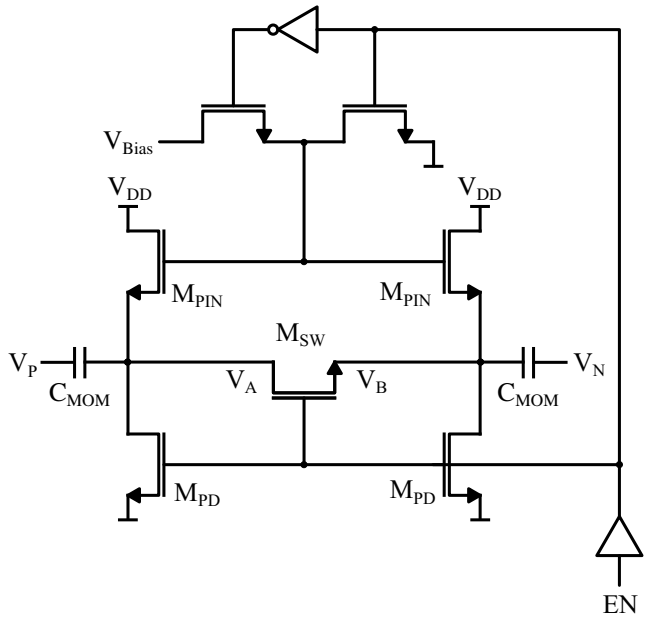


Figure 4.4: Digitally switched capacitor cells with bottom-pinning biasing [89]. When the main switch transistor $\mathrm{M_{SW}}$ is turned off, the NMOS pinning devices $\mathrm{M_{PIN}}$ fix the minimum of the oscillation voltage waveform close to the negative supply potential.

The PVT and acquisition capacitor banks are intended to be configured once during the frequency acquisition process. After their settings are established, closed loop operation solely utilizes the third and smallest capacitor bank, which is henceforth referred to as the tracking bank. To avoid degradation of the good DCO phase noise performance during closed-loop operation and to minimize the production of spurious spectral components, significantly better frequency resolution and linearity is required from this bank. Especially the small required capacitance can not be readily implemented using the capacitor structures characterized and provided by the foundry. To achieve the desired properties, a custom MOM finger capacitor geometry was designed and characterized instead. The conceptual implementation of this cell is shown in figure 4.5.

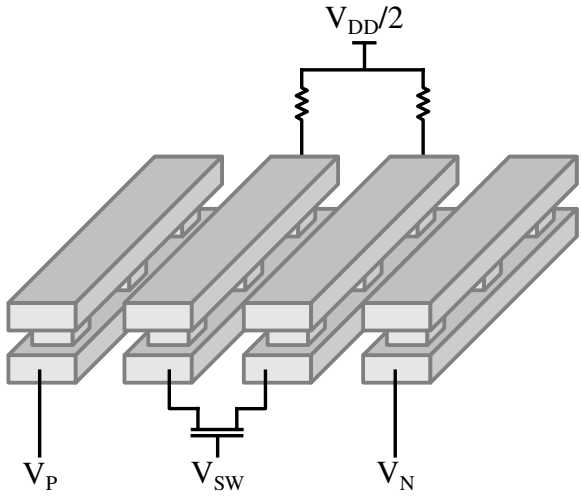


Figure 4.5: Implementation of the custom tracking bank MOM capacitor unit cell. Digital control of the cell capacitance is achieved by electrically connecting the innermost two fingers of the structure using an NMOS switch.

It is composed of four parallel minimum-width metal fingers, stacked across two metallization layers. A grounded poly-silicon shield is implemented below the cell to minimize substrate noise coupling. The two outer metal fingers are connected to the tank oscillation nodes. To digitally modulate the capacitance of this cell, its inner two fingers can be connected electrically using an NMOS switch transistor. This eliminates one of the three finger-to-finger capacitances from the series connection seen from to the tank nodes, and therefore increases the effective capacitance of the cell. Using this arrangement, a very small capacitance difference of about 65 aF can be realized, which provides a 35 kHz

Bank Type	**PVT**	**Acquisition**	**Tracking**
Varactor Type	Foundry MOM	Foundry MOM	Custom MOM
LSB Capacitance	12.5 fF	600 aF	66 aF
Frequency Resolution	6.5 MHz	320 kHz	35 kHz
Number of Cells	8	64	64
Cell Weighting	Binary and Thermometric	Thermometric	Thermometric

Table 4.1: Summary of digital tuning bank design parameters in the designed LC DCO.

frequency resolution of the DCO. Since the switched capacitance is very small, an NMOS transistor close to minimum size is sufficient to obtain good quality factor of such a cell, while also minimizing the amount of parasitics. Even though the mismatch variability of minimum-size devices can be a concern, simulations indicate that the DNL of a bank of such cells is not expected to be significantly degraded. The achieved tuning resolution is sufficiently granular considering the phase noise performance of the oscillator and the adopted sigma-delta modulator ($\Sigma\Delta$M) configuration described later. The performance of the custom capacitor cell was studied using 2.5D electromagnetic simulations, from which an appropriate cell-level S-parameter model was extracted for simulations. To achieve very high tuning linearity, an implementation using 64 unit cells placed in a regular and closely matching layout arrangement is chosen for the tracking bank. Table 4.1 summarizes the characteristics of the three types of capacitor cells foreseen for tuning.

The expected phase noise performance of the full oscillator circuit was determined based on periodic steady-state simulations at the nominal operating frequency. The predicted phase noise performance in nominal operation conditions is shown in figure 4.6. At 1 MHz offset from the 2.56 GHz oscillator frequency, a phase noise of $-123\,\mathrm{dBc\,Hz^{-1}}$ (FOM: $184\,\mathrm{dBc\,Hz^{-1}}$) is obtained in simulations, which is comparable to the currently available LC VCO circuits for radiation tolerant PLLs, such as in the lpGBT ASIC [62, 39]. This level of oscillator performance is sufficient for obtaining sub-picosecond levels of integrated PLL jitter with reference clocks of good quality, in line with the requirements identified earlier.

4.4.2 Discussion of Radiation Hardening Aspects

From a topological point of view, the chosen oscillator architecture is known to offer high radiation tolerance, and has been studied extensively in the past for VCO circuits [77, 63, 91, 92]. One major advantage of the adopted digital

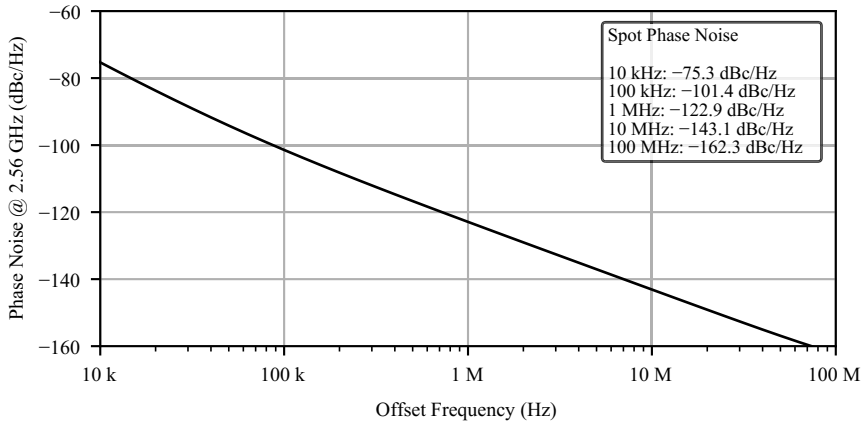


Figure 4.6: Simulated phase noise performance of the designed LC DCO circuit when operating at the nominal design frequency of 2.56 GHz.

tuning approach is the avoidance of MOS varactor devices. Such varactors have also been used in the past to implement digital capacitance control, such as in [22]. However, MOS varactors have been repeatedly identified in the past as components that can be structurally sensitive to SEEs in the context of VCO design [46, 63]. Through their inherent voltage-dependence of the capacitance, these devices also contribute to AM-FM conversion processes. Their omission therefore not only improves power supply rejection and phase noise of the oscillator circuit, but also reduces the sensitivity of the oscillation frequency to its amplitude. Since the oscillation amplitude may change with degradation of the active devices in the oscillator [46], an avoidance of MOS varactors can also be expected to improve TID tolerance by reducing the required oscillator tuning range.

Due to the large amount of charge stored in the LC tank, the oscillation nodes themselves are robust to charge collection resulting from SEE. To retain this robustness in the digital clock signals derived from the oscillating nodes, the DCO is equipped with three replica output buffers. Introducing this redundancy directly at the clock source allows fully hardening all subsequent divider stages and digital logic against SEE using TMR, in a way that is fully insensitive against SETs on the clock distribution network.

4.4.3 Radiation-Tolerant Prescaler Circuit

On the boundary to the digital loop components shared between the different DCO types, 1.28 GHz full-swing clock signals capable of directly driving CMOS

logic must be provided. Since a center frequency of 2.56 GHz was chosen for the LC DCO, a divide-by-two prescaler was designed and integrated with the oscillator. To mitigate SEE susceptibility, this prescaler is protected by adopting a full TMR scheme, including redundant majority voters in its feedback path. To also allow sustaining operation at high levels of TID, the prescaler is implemented using a custom high-speed cell library utilizing ELT devices [13]. Since the critical path of this circuit consists of only a single majority voter gate delay and the setup time of the D-Flip-Flop, the prescaler retains significant margins for TID degradation.

Together with the prescaler circuit, the complete oscillator occupies an area of approximately 0.2 mm^2. The design is predicted to dissipate 7 mW of power at the nominal operation frequency of 2.56 GHz and provides the three required 1.28 GHz clocks at its boundary to the digital loop components.

4.5 Radiation-Tolerant DCRO Design

Some of the material covered in this section has been published in [93]. Being typically composed exclusively from active devices, direct comparisons reveal ring oscillators to show a significantly stronger sensitivity to both SEE as well as TID degradation in radiation environments [46]. Many studies have been concerned with the general subject of radiation effects in ring oscillator circuits [52, 47, 94, 50, 51]. This popularity is in part also a consequence of their widespread use outside of PLL design, for example in process monitoring and data converters. Radiation hardening of digitally controlled ring oscillator (DCRO) circuits has so far not seen any significant treatment in the literature. For this reason, an existing DCRO architecture is evaluated for its radiation tolerance. An improvement to the radiation tolerance of this chosen topology is proposed based on simulations. Finally, two oscillator circuit designs are completed that will allow a study of the obtainable improvement from the implemented hardening measures.

4.5.1 Circuit Description

The basic oscillator circuit topology adopted is the unit cell fill factor DCRO originally presented in [95] which is illustrated in figure 4.7. In this circuit, each oscillator stage is composed of a number of tri-state inverter unit cells of identical size connected in parallel. Individual cells, when enabled, increase the driving strength of a given stage, and hence increase the oscillation frequency. Therefore, the control inputs of individual unit cells are used directly as a thermometric oscillator frequency tuning word (FTW). Since the load of each stage is constant but the driving strength increases proportionally with each additionally enabled unit cell, this DCRO topology achieves linear tuning over

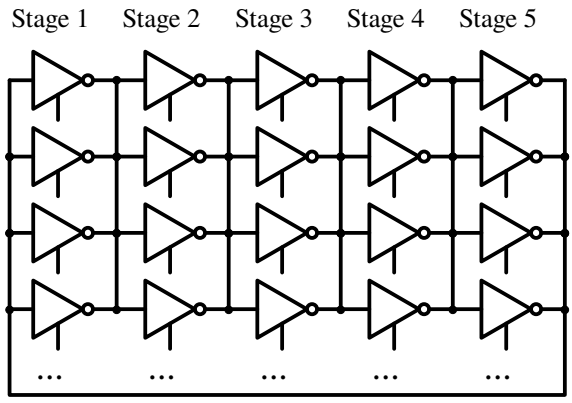


Figure 4.7: Schematic representation of the adopted DCRO topology. Each stage of the oscillator is formed by an array of digitally controlled unit cells connected in parallel.

a wide frequency range, and its tuning characteristic is additionally guaranteed to be monotonic.

Multiple desirable properties for radiation hardness can be expected from this basic architecture: In the context of the large TID degradation expected from ring oscillators, the wide tuning range is beneficial, since it increases the level of TID that can be tolerated before the oscillator becomes too slow to provide the frequency required by the application. The good linearity properties of the tuning characteristic reduce PVT- and radiation-related variations of the loop gain when the DCRO is used as part of an ADPLL circuit.

Advantages in terms of SEE resilience can be expected from the unit cell segmentation of the oscillator. Both the oscillating and tuning nodes are segmented into independent, small devices. This is in contrast to most conventionally used VCO implementations: In voltage-tuned current-starved inverter ring oscillators, the oscillating node of each stage is driven only by a small number of active devices. For this reason, charge collection in these devices can disturb the oscillation waveform and result in significant SEPTs [51]. Also, a single tuning node often simultaneously controls all oscillator stages, which introduces a very high sensitivity to transient responses affecting the frequency control voltage. This makes many voltage-controlled ring oscillator topologies highly susceptible to SEFTs.

The unit cell approach addresses both these problems simultaneously: First, the oscillating node is driven by many small devices in parallel, compared to a small number of large devices contributing to all the charge in the oscillator. Second, the single tuning node present in voltage-tuned oscillators is segmented

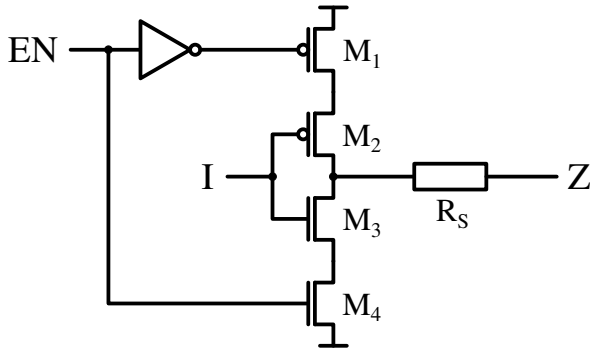


Figure 4.8: Implementation of the resistively decoupled unit cell (RDUC) for improved oscillator SEE tolerance. The output series resistor R_S decouples the individual output cells and reduces the impact of SET inside individual unit cells.

into many independent digital tuning nodes with small individual tuning gain. It can therefore be expected that the presence of SETs on any of the individual tuning bits results in appreciably smaller frequency errors in the oscillator than when a single node with large sensitivity is perturbed.

The basic resistively decoupled unit cell (RDUC) used in the proposed oscillator is shown in figure 4.8. Four MOS devices form a basic tri-state inverter, whose enable signal is used for frequency control of the oscillator. In the originally proposed circuit architecture, the outputs of all cells in a given stage are connected to one another. If the effects of charge collection processes following a particle strike can be confined to remain within a single unit cell, the radiation hardness of this circuit could be further improved significantly. As a measure to better decouple individual unit cells from one another, a series resistor R_S added to the output of each unit cell is proposed. A similar 'resistive averaging' technique has been more commonly used for analog circuit radiation hardening and was applied on a much smaller scale to the bias circuit of a voltage tuned ring oscillator in the past [47]. While charge collection in any of the active devices will still affect the local drain nodes of M_2 and M_3, the SEE current towards the common oscillation node will be limited by the resistor R_S. Therefore, the main oscillation node will be protected by the resistor while the collected excess charge is drained from the local node. The voltage perturbation at the gate nodes of the subsequent stage is therefore reduced and less phase error is stimulated in the oscillator.

An obvious drawback of introducing additional series resistance is a reduction of oscillation frequency, since the unit cell output resistance is increased while

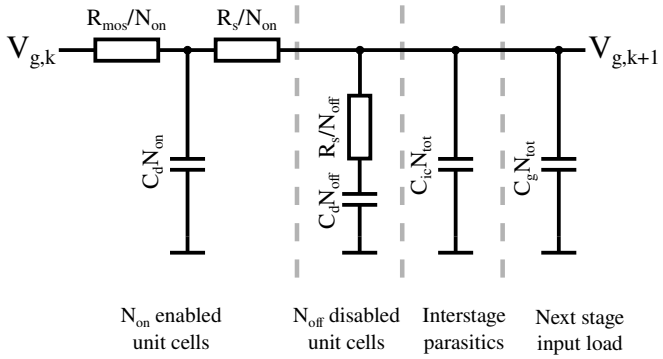


Figure 4.9: Model of one oscillator stage used for Elmore delay based oscillation frequency estimation. Enabled unit cells contribute to an increase of driving current, while disabled cells are assumed to load the common oscillation node with their drain capacitance.

the load capacitance (composed of the input capacitance of the following stage and any interconnect parasitics) is not reduced, but potentially even increased by parasitics associated with the resistor itself. This implies that the reduction of SEE sensitivity can likely be traded off against an oscillation frequency penalty.

4.5.2 Circuit Model

To better understand important design metrics of the fill factor DCRO design as well as the trade-off between the oscillation frequency penalty and the achievable SEE sensitivity improvement, simple models for the circuit will be derived first. Based on these simple models, an optimization is performed to obtain a range of values for the unit cell series resistance balancing both these design aspects.

4.5.3 Oscillation Frequency Estimation

To qualitatively model the oscillation frequency, a simple equivalent circuit for a single oscillator stage based on Elmore delay analysis [96] is proposed. The equivalent RC network for an oscillator stage consisting of N_{tot} parallel RDUCs can be seen in figure 4.9. Each of the N_{on} enabled unit cells contributes an effective parallel channel resistance of R_{mos}. Each cell is further modeled by a lumped drain capacitance C_d before the intentional cell series resistance R_s. The N_{off} disabled unit cells in each stage load the common oscillating node in addition to the N_{tot} gate capacitances C_g of the following stages and the parasitic inter-stage capacitance C_{ic}, which also grows linearly with the number

of unit cells per stage. The resulting propagation delay of the RC network is approximated by:

$$t_{\mathrm{pd}} \approx C_d R_{\mathrm{mos}} + \left(\left(C_{\mathrm{ic}} + C_g\right) N_{\mathrm{tot}} + C_d N_{\mathrm{off}}\right) \left(\frac{R_s}{N_{\mathrm{on}}} + \frac{R_{\mathrm{mos}}}{N_{\mathrm{on}}}\right) \tag{4.2}$$

To simplify the resulting equations, ratio of enabled unit cells per stage is denoted by F (fill factor) and it is assumed that F in each stage is identical.

$$F = N_{on}/N_{\mathrm{tot}} = 1 - \left(N_{\mathrm{off}}/N_{\mathrm{tot}}\right) \tag{4.3}$$

Rearranging equation (4.2) in terms of F, the oscillation frequency of a K-stage ring oscillator is obtained as

$$\begin{aligned} f &= \frac{1}{2K t_{\mathrm{pd}}} \\ &= \frac{F}{2K\left(C_d F + C_{\mathrm{ic}} + C_g + C_d\right) R_s + 2K\left(C_{\mathrm{ic}} + C_g + C_d\right) R_{\mathrm{mos}}}. \end{aligned} \tag{4.4}$$

Already from equation (4.4) it is obvious that for small values of R_s, the oscillation frequency of a given oscillator design depends very linearly on the fill factor F. A small nonlinear contribution is incurred for large R_s, however the contribution of the $C_d F$ term in the denominator to the oscillator frequency remains below 10 % for practical design values. Neglecting this minor nonlinear contribution, the oscillation frequency can be conveniently expressed using

$$f = \frac{F}{2K\left(C_{\mathrm{ic}} + C_g + C_d\right)\left(R_s + R_{\mathrm{mos}}\right)}. \tag{4.5}$$

It is noteworthy that the oscillation frequency is to first order independent of the number of unit cells N_{tot} in the oscillator, since both the driving strength and the load of each stage increase proportionally with each cell. Instead, increasing N_{tot} improves the tuning resolution by providing more granular control over F. While this model is not entirely useful for estimation of the actual design frequency due to difficulties in determination of the included quantities, it adequately models many relevant effects, such as the independence of N_{tot} and the linearity of the tuning curve.

An important consideration is the dependence of the oscillation frequency on the value of R_s relative to R_{mos}. Rearranging equation (4.5) and disregarding constants, this relationship is found to have the form shown in equation (4.6). This qualitative relationship will become relevant in the design optimization performed later, as it allows analyzing the trade-off between oscillation frequency and SEE sensitivity.

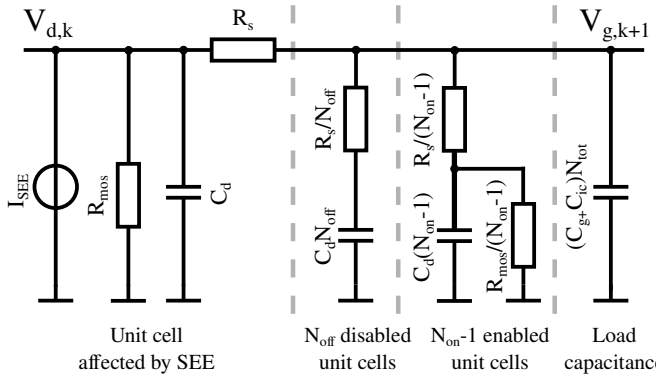


Figure 4.10: Model of one oscillator stage for estimation of the SEE sensitivity. Charge is injected at the drain of an enabled unit cell (shown on the left), while all other unit cells are assumed to be unaffected.

$$f \propto \frac{1}{1 + \frac{R_s}{R_{\mathrm{mos}}}} \tag{4.6}$$

4.5.4 SEE Sensitivity Reduction

As a second step, a model for the SEE sensitivity reduction provided by the addition of R_s to the unit cells is developed. For the following analysis, a charge collection (as a result of irradiation) event at one of the drain junctions connected to R_s, i.e. in M_2 or M_3, is considered. A circuit model for such an event is shown in figure 4.10. This small signal model can give useful insight into the circuit behaviour during irradiation. Following the established treatment of the ISF of oscillator circuits [33], the stimulated voltage disturbance at the (common) gate node of the following ring oscillator stage $V_{\mathrm{g,k+1}}$ is indicative of the resulting phase error of the oscillator at the maximum of the ISF. This quantity can be obtained by deriving the circuit transfer function:

$$H_{\mathrm{SEE}}(s) = \frac{V_{g,k+1}(s)}{I_{\mathrm{SEE}}(s)} \tag{4.7}$$

As a first-order estimate that allows obtaining analytical solutions, a Dirac current impulse can provide a model for charge collection events during irradiation. The transient impulse response $V_{g,k+1}(t)$ is obtained from an inverse Laplace transform of $H_{\mathrm{SEE}}(s)$ for the model in figure 4.10. Qualitative transient

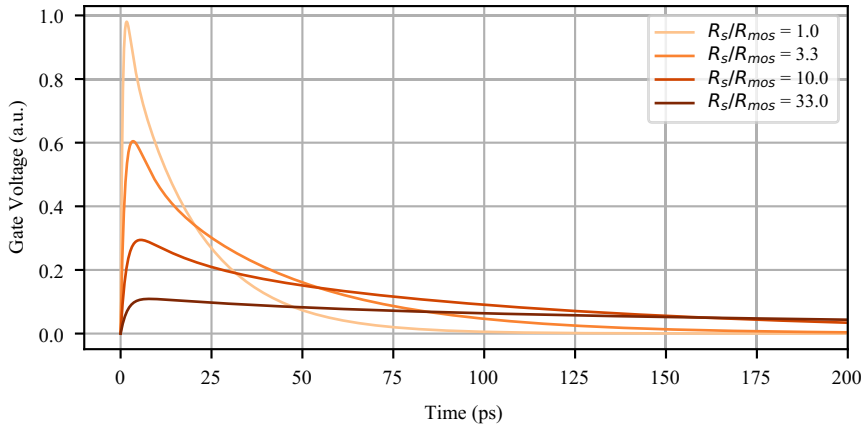


Figure 4.11: Qualitative transient responses of the voltage at one oscillator stage gate node following a current impulse. Responses for different ratios of R_s to R_{mos} are shown, illustrating the lengthening and amplitude reduction of the voltage deviation.

responses obtained for different values of R_s are shown in figure 4.11. It can be seen that as the ratio of R_s to R_{mos} increases, the stimulated voltage transient reduces in amplitude, while at the same time lengthening in duration. In the ring oscillator circuit, this provides two benefits. One on hand, the reduced voltage deviation at the common gate node results in less excess phase being regenerated by the next oscillator stage. On the other hand, the lengthening of the transient response will time-average the response of the SEE across a longer fraction of the period. Since the ISF is typically zero-mean, a significant lengthening across more than half of the oscillation period therefore contributes to a further reduction of the sensitivity.

Since the full transfer function of the circuit shown in figure 4.10 is of fourth order, it provides little insight into the relevant parameters during the design process. To qualitatively assess the primary contributors that determine the peak SEE response generated in the circuit, the obtained transfer function can be simplified by retaining only the first order terms and neglecting any insignificant contributors. Without sacrificing the qualitative behaviour of the peak amplitude, in this way a closed form first order estimate for the peak voltage deviation resulting from an impulse current injection with a charge Q can be obtained.

$$\mathrm{V}_{\mathrm{g,k+1(pk)}} = \frac{Q}{\left(C_{\mathrm{ic}} + C_g + C_d\right) N_{\mathrm{tot}} \left(\frac{R_s}{R_{\mathrm{mos}}} + 2\right)} \tag{4.8}$$

Equation (4.8) provides an insight into the SEE sensitivity of this circuit. Firstly, the sensitivity is inversely proportional to the number of unit cells in the oscillator and their capacitive parasitics. This is an intuitive relation, since the voltage deviation resulting from injection of a fixed charge is inversely proportional to the capacitance it is transferred into, and the load of each stage increases linearly with the number of unit cells. However, it has to be considered that the circuit area (and therefore the area sensitive to radiation) also increases linearly with the number of unit cells. This implies that in a given radiation environment the magnitude of phase errors can be traded-off against their frequency of occurrence.

Secondly, to motivate a choice of R_s, it can be observed that the sensitivity of a given oscillator design with only R_s as the free variable follows the relationship:

$$\mathrm{V}_{\mathrm{max}} \propto \frac{1}{1 + \frac{R_s}{2R_{\mathrm{mos}}}} \tag{4.9}$$

As expected from the foregoing discussion, the sensitivity decreases significantly for values of R_s approaching or exceeding R_{mos}. In this regime, the injected charge stops propagating to the common gate node and is instead dissipated locally within the unit cell.

4.5.5 Design Trade-Off

Since the previous analysis has revealed that the oscillation frequency and SEE sensitivity follow simple relationships of R_s/R_{mos}, it makes sense to at least qualitatively assess the presence of optimal design points for this circuit. A favorable point would provide significant reduction of the SEE sensitivity combined with only an acceptable frequency reduction of the oscillator.

Since the ratios derived in equation (4.6) and equation (4.9) allow analytical optimization and range between zero and one, a suitable loss function can be defined as follows:

$$\lambda = -\,\mathrm{V}_{\mathrm{max}} \cdot (1 - f) \tag{4.10}$$

$$= -\frac{1}{1 + \frac{R_s}{2R_{\mathrm{mos}}}} \cdot \left(1 - \frac{1}{1 + \frac{R_s}{R_{\mathrm{mos}}}}\right) \tag{4.11}$$

$$= -\frac{2R_{\mathrm{mos}}R_s}{{R_s}^2 + 3R_{\mathrm{mos}}R_s + 2{R_{\mathrm{mos}}}^2} \tag{4.12}$$

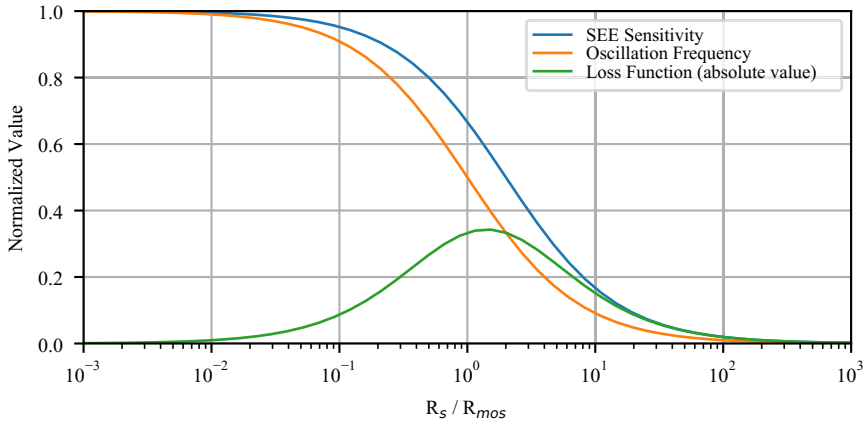


Figure 4.12: Qualitative dependency of oscillation frequency, SEE sensitivity and the loss function chosen for optimization. All quantities are expressed as simple fractions of the ratio between the intentional series resistance and the effective unit cell on-resistance.

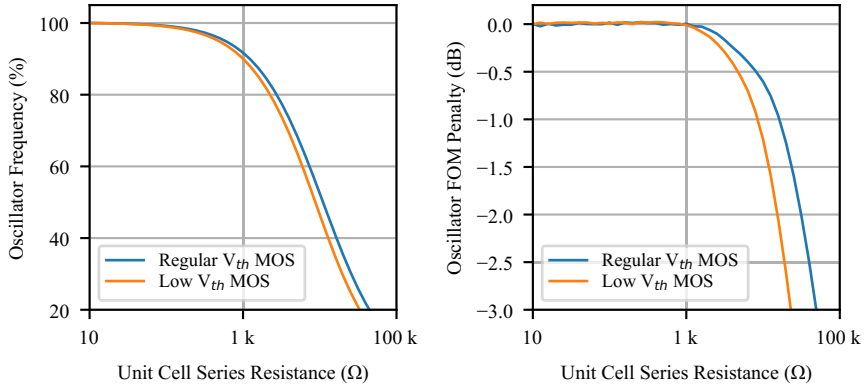
The dependence of the oscillation frequency, SEE sensitivity and the loss function on the ratio R_s/R_{mos} are shown in figure 4.12. The optimum is found by solving for the roots of the first derivative of equation (4.10), and the optimal value for R_s can be shown to be:

$$R_s = \sqrt{2} R_{\mathrm{mos}} \tag{4.13}$$

The identified optimum is rather shallow, so design points in its vicinity may also provide suitable compromises. The practical applicability of this optimization also requires consideration. One conceptual uncertainty of the proposed model lies in the definition of R_{mos}: The ring oscillator being a large-signal circuit by nature, defining a single 'effective' channel resistance has its limitations: Different values for R_{mos} might be appropriate for the analysis of oscillation frequency and SEE sensitivity, which may shift the position of the optimum. Another limitation is in the assumption made by modeling the charge collection event by a Dirac impulse. While this allows retaining mathematical tractability, typical current pulse shapes are more complex and extend over longer timescales approaching the oscillation period of high frequency oscillators.

4.5.6 Design Procedure

In practice, the limitations of the simplified models are of little consequence, since the circuit can be studied well using simulations. Using accurate models for active devices and interconnects, the oscillation frequency of this structure can be precisely estimated. With appropriate models for charge collection events during irradiation, the SEE sensitivity can be quantified in different charge regimes more precisely. An additional consideration for the design trade-off, which can be addressed using simulations, is a potential increase of phase noise resulting from the additional series resistance R_s. To quantify this aspect together with the anticipated improvement in SEE tolerance, a parametric design study is carried out on a practical design. A five stage ring oscillator composed of 100 unit cells per stage is designed in a 65 nm technology. Minimum transistor lengths are selected to maximize the oscillation frequency. Since TID degradation of the maximum drain current of PMOS devices dominates over NMOS devices in the chosen technology [88], the minimum width of PMOS devices is constrained based on their anticipated level of TID. The NMOS device widths are then obtained by determination of the W_P/W_N ratio resulting in a symmetric oscillation waveform, which minimizes the contribution of flicker noise to the oscillator phase noise [97]. Following this sizing, the impact of additional unit cell series resistance on both the oscillation frequency and the oscillator FOM (as defined in equation (2.3)) is obtained using simulations. The results of this analysis are shown in figure 4.13, which compares these dependencies to the initial design.



(a) Oscillator Frequency (b) Oscillator FOM

Figure 4.13: Simulated dependence of the oscillation frequency and oscillator FOM on the unit cell series resistance.

Aspects such as the impact of unequal degradation characteristics of PMOS and NMOS devices under irradiation and its impact on flicker noise upconversion can also be evaluated at this stage. In anticipation of the experimental validation that will be performed later, all simulations are performed for active device flavors with regular and reduced threshold voltage (V_{th}). In line with the intuitions gained from the modeling process, series resistances that are small compared to the unit cell output resistance have insignificant impact on the oscillation frequency. With increasing series resistance, the frequency reduces and the FOM begins to degrade. A noise analysis based on periodic-steady-state simulations was performed, which confirmed that the thermal noise contributions of the added series resistance increasingly dominate the circuit noise. However, up to a frequency reduction of 50 %, the oscillator FOM only reduces by about 1 dB. Therefore, the phase noise performance at a given oscillation frequency is not significantly degraded as long as the frequency reduction can be tolerated or compensated by other means without a penalty in SEE sensitivity, such as the use of low-V_{th} devices or an increased supply voltage.

4.5.7 Radiation Effects Simulations

To enable optimizing the radiation-hardness of this initial design by properly sizing the unit cell series resistor, the achievable reduction of SEE sensitivity is quantified using charge injection simulations. These parametric simulations cover multiple dimensions to adequately assess the circuit sensitivity:

1. As expected from the periodic, time-dependent nature of the impulse sensitivity function of oscillators [33], SET responses of ring oscillator circuits were also shown to be time-dependent [35]. Therefore, charge injections need to be performed at multiple instants along the oscillation period to identify points of maximum sensitivity. In the performed simulations, twenty equidistant points along the oscillation period were evaluated.

2. Because of the previously discussed circuit nonlinearity in the presence of large injected charges, the quantity of injected charge needs to be varied across the range expected from the circuit radiation environment. Charge quantities between 100 fC and 1 pC per transient were used in simulations, which approximately correspond to values stimulated by LETs in the range from 10 MeV mg^{-1} cm^2 to 100 MeV mg^{-1} cm^2 [98].

3. The dynamics of the current waveform used to simulate the charge injection influence the circuit response. To approximate the charge collection process in the chosen 65 nm technology, a double-exponential current pulse model was selected [99]. Time constants of $\tau_r = 15$ ps and $\tau_f = 75$ ps were chosen for the performed simulations. These represent typical values in the chosen technology node, and the ratio of $\tau_f/\tau_r = 5$ is reported to be a

good model for transients occurring in practice [34]. The sensitivity of the studied circuit to variations of these time constants was found to be small, implying that choosing a single value is adequate to reduce the number of simulation dimensions.

As charge is injected at multiple time instants of the oscillation period to account for the time-varying nature of the sensitivity, an individual sensitivity function of the oscillator is obtained for each pair of unit cell resistance and injected charge. A selection of example sensitivity functions obtained with 1 pC of injected charge are shown in figure 4.14. As a proxy for the worst case phase error stimulated by an SEE, the peak value of this sensitivity function is extracted for each parameter combination. These chosen points for sensitivity estimation are highlighted in figure 4.14. This reduction process allows summarizing the dependency of SEE sensitivity across the chosen range of collected charge and unit cell series resistance in figure 4.15.

The obtained results are consistent with the findings obtained using the circuit models: As long as the added series resistance remains small relative to the unit cell output resistance, no reduction of charge injection sensitivity is obtained. Above a threshold resistance the stimulated oscillator phase error begins to reduce significantly. In this region, transients injected at the drain nodes of M_2 and M_3 are reduced at the common gate node, while the excess charge is drained away in the unit cell. Consequently, the propagation of the transient to the next stage of the ring oscillator is reduced, attenuating the resulting phase error stimulated.

While charge injection simulations are always subject to uncertainties due to the simplified current injection model used, they clearly indicate that significant reductions of the oscillator SEE response can be achieved by an appropriate choice of the unit cell series resistance. Suitable design points for a practical oscillator can be identified by combining the results shown in figure 4.13 and figure 4.15. Since the SEE sensitivity improves monotonously with series resistance, the design is constrained by the frequency reduction and FOM penalty that can be tolerated. The area required for the implementation of large resistances in CMOS technologies might also place an upper bound to the resistance.

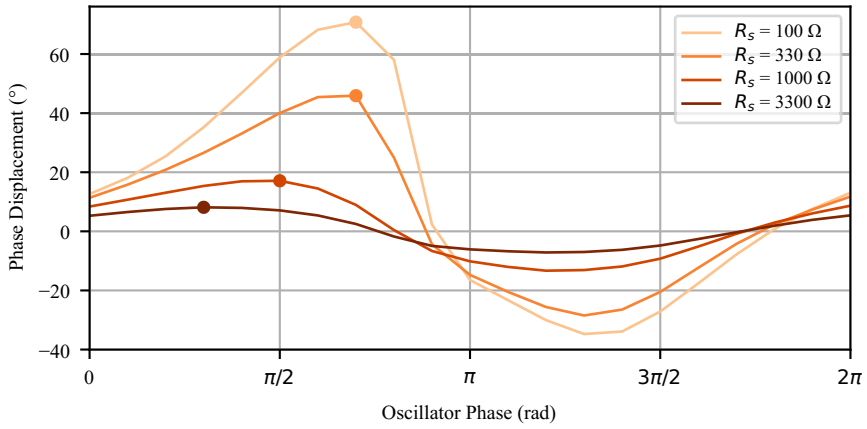
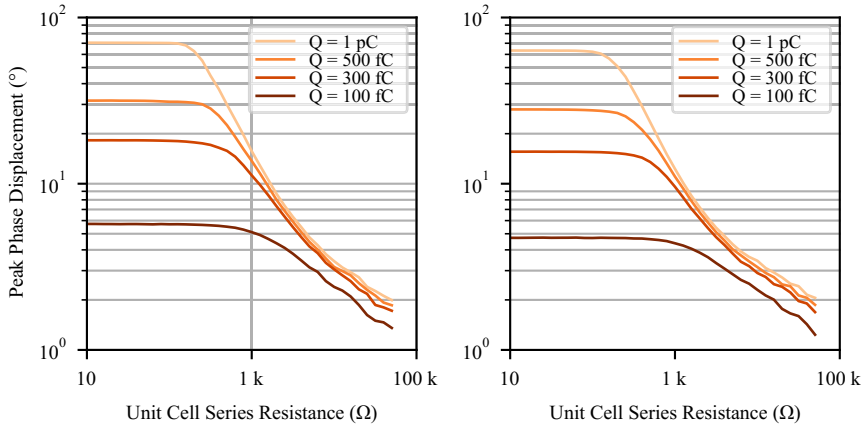


Figure 4.14: Charge injection sensitivity functions obtained in the studied oscillator circuit. The maximum of each periodic sensitivity function is extracted for each simulated resistance value. The shown example data is obtained for 1 pC of injected charge on regular-V_{th} devices. Only the highlighted peak values of each sensitivity function are used in figure 4.15.



(a) Regular-V_{th} devices (b) Low-V_{th} devices

Figure 4.15: Simulated worst-case oscillator phase displacement for different values of unit cell series resistance. Simulations with different injected charge magnitude are performed for comparison. Also shown is the small difference between threshold voltage flavors of devices in the chosen technology.

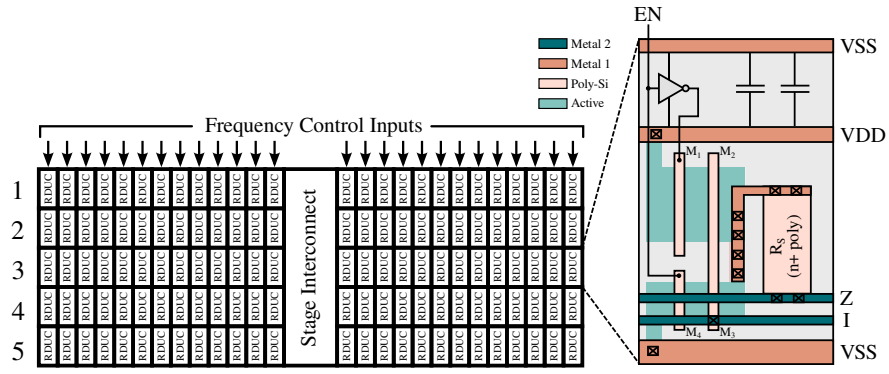


Figure 4.16: Layout organization of the ring oscillator. The inset shows the layout of the abuttable RDUCs. For the design without R_s, the polysilicon resistor is replaced by metal, however the unit cell area is left unchanged.

4.5.8 Designed Oscillator Variants

To validate the findings obtained by simulations and quantify the improvements in SEE sensitivity experimentally within radiation-tolerant ADPLL circuit implementations, two DCROs variants were designed. One of the designed oscillators, serving as a reference design, adopts the original, non-hardened architecture without an additional series resistance. A second design is composed of the proposed RDUCs promising increased radiation tolerance. Both oscillators are sized for an operation frequency of 1.28 GHz using the design procedure outlined in section 4.5.1. The digital frequency tuning range range is sized over process, voltage and temperature corners and also includes a TID degradation margin of approximately 20 %.

To fairly quantify the improvement obtainable using the RDUC approach experimentally, both oscillators need not only to operate at the same frequency, but also using an identical number of unit cells and fill factor. This constraint is fulfilled by compensating for the reduction of oscillation frequency by using active devices with reduced threshold voltage in the RDUC DCRO, while regular V_{th} devices are used in the reference design. The presented charge injection simulations confirm that the V_{th} flavor has very little influence on the SEE-related characteristics of the circuit. A unit cell resistance of 1.7 kΩ is chosen, since it approximately equalizes the oscillation frequency of both oscillators and at the same time promises a significant reduction of the SEE sensitivity based on the preceding simulations. The unit cell resistor is implemented using an unsilicided polysilicon structure, which offers high sheet resistance and therefore occupies little circuit area. The selected resistor implementation increases the

Design	**Non-hardened**	**RDUC DCRO**
Number of Stages	5	
Unit Cells per Stage	96 + 3 output buffers	
Unit Cell Series Resistance (Ω)	0	1700
MOS Threshold Voltage	Standard V_{th}	Low V_{th}
Minimum Frequency (GHz)	0.49	0.49
Maximum Frequency (GHz)	2.07	2.25
Power Dissipation (mW GHz^{-1})	5.7	5.8
Oscillator FOM (dBc Hz^{-1})	162	163
Tuning Step Size (MHz)	4	4.2

Table 4.2: Summary of both DCRO design variants.

unit cell area by about 50 %. Finally, both oscillators are implemented with identical physical layouts apart from the added polysilicon resistor. Crucially, this minimizes differences in charge-sharing interactions among adjacent unit cells, which would otherwise depend on their spacing [100]. The basic design parameters of both oscillators as well as performance figures obtained by post-layout simulations are summarized in table 4.2. The layout organization chosen for both designs is shown in figure 4.16.

Each oscillator occupies an area of 0.012 mm^2, which still makes the design a practical choice for area-constrained applications. Both designs are predicted to dissipate 7 mW of power at the nominal operation frequency of 1.28 GHz. The phase noise obtained from simulations of the architecture is shown in figure 4.17. Similar to the approach chosen for the LC DCO, three redundant output buffers are connected to each of the oscillators to avoid introducing an SET sensitivity at the root of the following clock distribution network. Since the oscillator directly provides the required oscillation frequency of 1.28 GHz, no further prescaler is required.

4.5.9 Tuning Word Segmentation

Due to the chosen architecture, the oscillator offers 480 independent digital inputs to control the oscillation frequency. These correspond to the 96 individual enable lines for each of the five oscillator stages. While these inputs in principle do not dictate any particular segmentation or hierarchy, in practice a similar coarse-fine structure as in the LC DCO is beneficial. In particular for closed-loop control, a thermometric control scheme of the tracking bank is preferred, since it results in an improved linearity. The implementation of a single thermometric encoder for all 480 control bits (corresponding to a binary word length of 9 bit) can however be considered excessive, since only a small fraction of this range would be used during closed-loop operation.

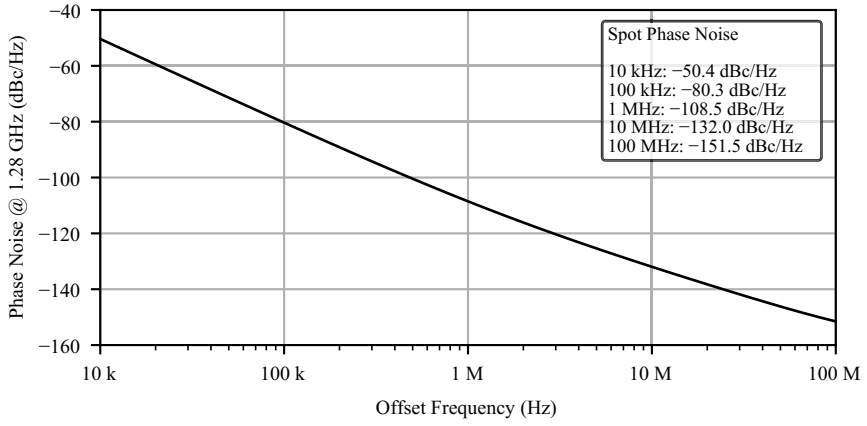


Figure 4.17: Simulated phase noise performance of the proposed DCRO design when operating at the nominal design frequency of 1.28 GHz.

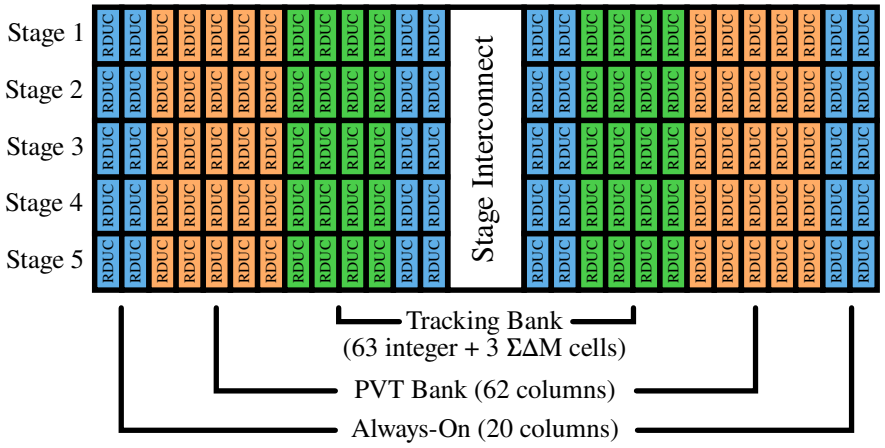


Figure 4.18: Tuning segmentation implemented for hierarchical frequency tuning of the DCRO.

Instead, the tuning inputs were logically segmented as follows. A fixed percentage of stages are electrically configured to be active permanently. This guarantees a certain minimum amount of current to drive the oscillation, alleviating start-up issues caused for example leakage currents when operating with a very small fill factor. For the remaining inputs, a partitioning into two logical banks was performed, which is schematically shown in figure 4.18. A coarse PVT bank was implemented and consists of 64 logical settings. Each of these enables one additional column of five unit cells (one cell per oscillator stage). In this way, one of 64 coarse frequency bands can be selected during the frequency acquisition process. Additionally, a column-wise control scheme keeps the fill factor of each stage approximately the same, which guarantees that similar slew rates are present throughout the oscillator. For fine frequency control during closed-loop operation, 63 individual unit cells in the center of the DCRO are used for the integer component of the tuning word. Three additional unit cells are assigned to the output of the $\Sigma\Delta$M synthesizing the fractional tuning word component. Since a fixed ratio between the PVT and tracking banks is retained regardless of the operation frequency, good centering of the tracking bank can be guaranteed regardless of PVT conditions. To minimize tuning nonlinearity within the configurable stages due to edge-effects, the permanently enabled cells are assigned to locations on the extremities of the oscillator.

4.6 Digital Loop Design

As outlined earlier, the differences in tuning segmentation, achieved frequency resolution and performance of the presented DCO designs need to be accommodated by a common set of digital components forming the core of the ADPLL. The components considered common to all implemented PLL types are the BBPDs, DLF, $\Sigma\Delta$M, feedback divider as well as any required frequency acquisition functionality. Based on the DCO performance figures obtained in section 4.4 and section 4.5, the design of these components can now be refined.

4.6.1 Architecture

A structural representation of the adopted loop structure is shown in figure 4.19. For the loop filter, a proportional-integral (PI) structure is chosen, resulting in a second-order ADPLL. This topology represents a common choice for wireline communications systems, not only among all-digital bang-bang phase locked loop (BBPLL) circuits. Its performance is well-studied, and since no significant higher-order dynamics of the reference clock are expected that could impair the phase tracking capabilities, it is expected to fulfill all identified requirements. To enhance the available frequency tuning resolution of the DCOs, a second order $\Sigma\Delta$M is included between the loop filter output and the DCO tuning

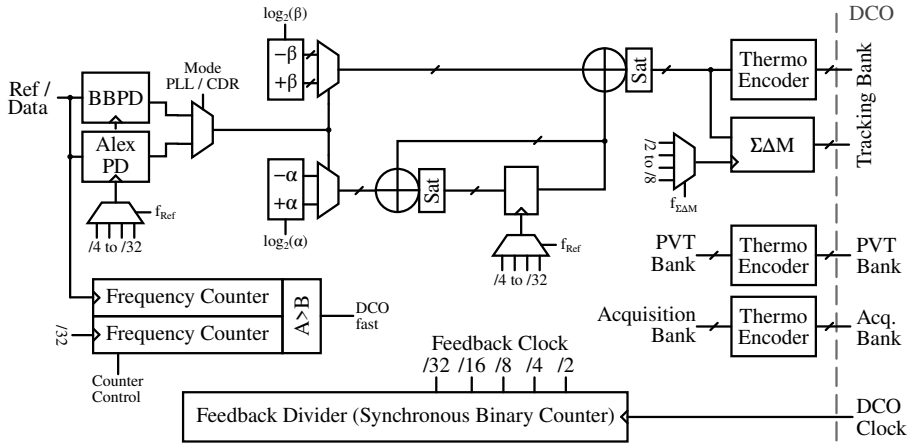


Figure 4.19: Block diagram of the digital components forming the core of the all-digital PLL circuit.

word. In particular for the DCRO, this improved resolution is desirable also for the proportional path of the loop filter to improve the obtainable jitter performance.

The required frequency acquisition functionality is provided by two frequency counters, which can be used to measure and compare the frequencies of the reference and the feedback clock signals. Using a binary search covering the coarse frequency banks available for each DCO, the optimal PVT and acquisition bank configuration can be selected. This process brings the DCO to within the locking range of the BBPD before closed-loop control is engaged. Components used only during acquisition such as the frequency counters are clock-gated during closed-loop operation, eliminating their dynamic power consumption. Particular care is exercised in these components, ensuring that an accumulation of SEUs in registers without an active clock signal can not impact the operation or performance of the PLL.

In devising a clocking architecture for the digital PLL components, the integer-N nature of the loop is leveraged. All clocks used in the circuit with the exception of the external reference clock are derived synchronously from the DCO output inside the feedback divider. To allow supporting the different required options for data rate and reference clock frequency, a number of clocking configuration options are implemented for the forward-path of the loop (BBPD, DLF, ΣΔM). These options can additionally be used to power-scale the design using clock gating, for example by reducing the operation frequency of the ΣΔM. This allows studying available power-performance trade-offs. The

chosen clocking scheme is also beneficial for the timing analysis of the digital circuits during their implementation. The sampling registers within the BBPDs represent the only timing arc between potentially asynchronous clock domains (the reference clock and the DCO-derived clocks) in the design. Timing-critical arcs exist only between synchronous clocks derived from the DCO and can be therefore fully analyzed using static timing analysis (STA) techniques by EDA tools during the implementation phase.

4.6.2 Radiation Hardening Strategy

To obtain the anticipated level of design automation and also achieve technology portability of the developed design, the components described above are in practice implemented using digital design and verification methodologies. As such, their structure, functionality and performance is for the most part defined using hardware description languages instead of device-level schematics. This approach also suggests the use of corresponding and applicable techniques for radiation hardening. The conceptual sensitivities of the digital loop components and the chosen hardening approach against SEE and TID effects are described below.

Single-Event Effects

In the chosen architecture in particular, the DLF presents a critical SEE sensitivity. SEUs may corrupt the frequency error information stored in the loop filter integrator registers, resulting in SEFTs of the PLL [81]. In a similar fashion, the memory elements of the $\Sigma\Delta$M are sensitive to corruption by SEUs, which may also result in the PLL losing lock temporarily and manifesting as either SEPTs or SEFTs when not mitigated. In addition, SEUs or SETs in any control logic of the PLL during operation may trigger potentially catastrophic failure modes. Section 4.2 has already highlighted the role of PLL circuits as a single point of failure of larger systems and the potential impact of SEEs affecting clock signals in digital circuits. Striving for the highest level of protection against these effects essentially dictates the application of systematic hardening techniques against SEE sensitivities to maximize reliability. This goal can be achieved by applying TMR as a structural circuit redundancy technique. Even though the relatively large power and area penalties discussed in section 2.4 are downsides of this technique, it offers many advantages, such as a very high levels of design automation and technology-independent applicability compared to other RHBD methodologies.

Neither the area nor the power penalty represent practical limitations: In terms of area, the gains from omission of any analog loop filter components required only for conventional PLL circuits are most likely to outweigh any potential penalty from a TMR implementation of the digital loop filter. Similarly,

further gains in area and power consumption will be exploited by the adoption of more advanced technology nodes, and other components of the PLL circuit (such as the DCO) can be expected to dominate the circuit area. A TMR-based protection scheme was therefore chosen for all digital PLL components discussed in this section, except for the (inherently insensitive) BBPD. The design automation advantage of the TMR technique over other candidate techniques is obtained through use of the existing TMRG tool [83] developed at CERN. Wherever possible in the design, a full TMR implementation was chosen, which includes redundant implementation of clock and reset trees as well as majority voters, minimizing the circuit sensitivity against SETs. Any specific additional logic required for implementation of the desired redundancy, in particular the triplicated majority voting structures, are also automatically inferred from their RTL description during synthesis. While this leaves the synthesis and physical implementation processes with the largest possible freedom for logic optimization, constraints needed to be carefully applied to avoid merging of any intentionally redundant logic paths. Additional structural checks for such issues have been performed on the netlists after each major implementation stage.

Total Ionizing Dose

Since the properties of any used digital circuits, such as the loop filter transfer function, are fully defined by digital words rather than analog voltages or currents, the loop dynamics remain unaffected by TID degradation until the circuit fails due to violations of setup or hold constraints. This presents a large advantage over conventional PLL designs as long as high functional TID tolerance of the digital circuits is achieved in the first place. The main technique used to enhance the tolerance to TID is the use of conservative setup and hold timing margins during circuit implementation. Based on the reported degradation of digital circuits in the chosen technology [101], setup margins of at least 20 % of the clock period are used throughout the design. Since the most significant effect of TID on digital circuits is the reduction of their maximum operation frequency, this approach allows retaining reliable operation even as gate delays degrade incrementally. Additionally, pessimistic hold margins exceeding the foundry recommendations by a factor of at least two have been used to account for unequal delay degradation of different clocks in inter-domain timing arcs. While the optimization effort required to achieve these tighter margins is absorbed by EDA software, the use of a faster circuit implementation might come with a minor additional power penalty. Timing closure of the design with the above-mentioned constraints was achieved using a 9-track foundry standard cell libraries. If required, even higher margins could be obtained at the expense of additional power consumption through the use of faster, potentially custom-designed standard cell libraries.

4.6.3 Bang-Bang Phase Detectors

The BBPD is a crucial component for system performance, since it converts the timing error between the reference and the feedback clock signals into digital phase error information. From a functional standpoint, the BBPDs are implemented using one or more D flip-flops. Particular scrutiny during the design process of these flip-flops is however warranted, since they operate on sensitive continuous-time quantities, which can be impaired or corrupted by second-order circuit effects. Transistor-level simulations of even such conceptually simple phase detectors are required to allow adequately predicting PLL performance.

One issue affecting the design of bang-bang phase detectors is sampling-time hysteresis [25, p. 96]. This effect can be considered the time-domain equivalent of hysteresis in voltage sense amplifiers. Depending on the previous state of the phase detector, its sampling window may shift in time. In the case of a D-flip-flop being used as a phase detector, this issue alters the the phase difference between the clock and data inputs at which the flip-flop begins latching a different value. Since it is precisely this timing difference that the BBPD is supposed to detect, any such hysteresis is detrimental to its performance as a phase detector. In order to not deteriorate the jitter performance of the PLL, hysteresis must be eliminated systematically or reduced to a level acceptable by the design. Additionally, the transistors forming the sampling latch contribute a design-dependent amount of noise during the sampling process, which (through AM-PM conversion) translates into random sampling jitter. The superposition of both these impairments limits the available phase detection gain and the achievable jitter performance of the PLL.

To establish a performance baseline, a C^2MOS D-flip-flop provided by the foundry standard cell library was evaluated in simulations. The hysteresis of this cell was found to be about 2 ps. Since this level of hysteresis can directly translate into a limit cycle of the DCO phase with a peak-to-peak deviation of the same magnitude, it intrinsically limits the PLL performance to a jitter performance of $^{2\,\mathrm{ps}}/\sqrt{12} \approx 570\,\mathrm{fs}$ rms, even when all other noise sources are neglected. As such, the standard cell flip-flop was considered insufficient for the intended application as a phase detector and two improved CMOS flip-flop designs have been devised. First, a balanced cell-based implementation of a D flip-flop from individual logic gates as in [102, p. 732] was studied. The schematic of the flip-flop is shown in figure 4.20. This implementation was found to provide a post-layout hysteresis of typically 900 fs when implemented using low-V_{th} standard cell gates. As an alternative architecture, a transmission-gate C^2MOS D-flip-flop [103] with an integrated non-overlapping clock generator (NOCG) [104] was implemented and optimized. The schematic of this D-Flip-Flop is shown in figure 4.21. The use of non-overlapping clock signals for the master and slave latches was found to reduce the amount of hysteresis significantly, as suggested in [25, p. 97].

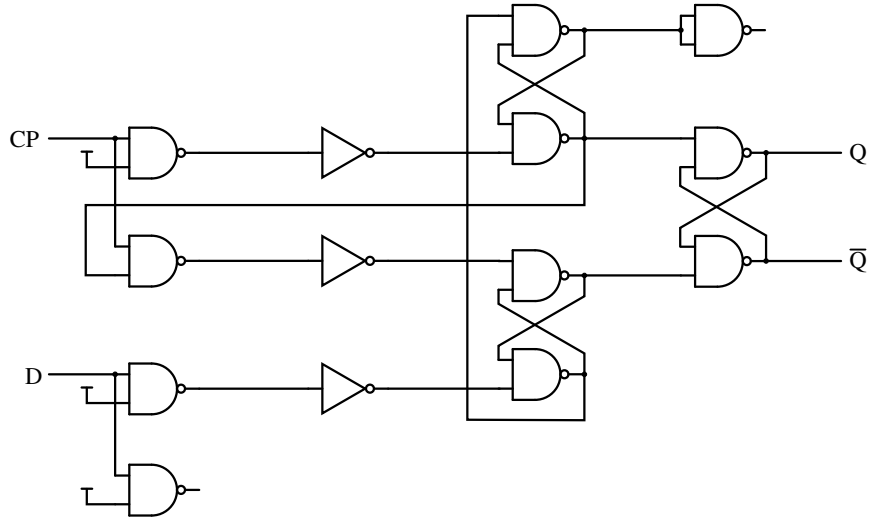


Figure 4.20: Balanced D-Flip-Flop implementation using standard cell gates.

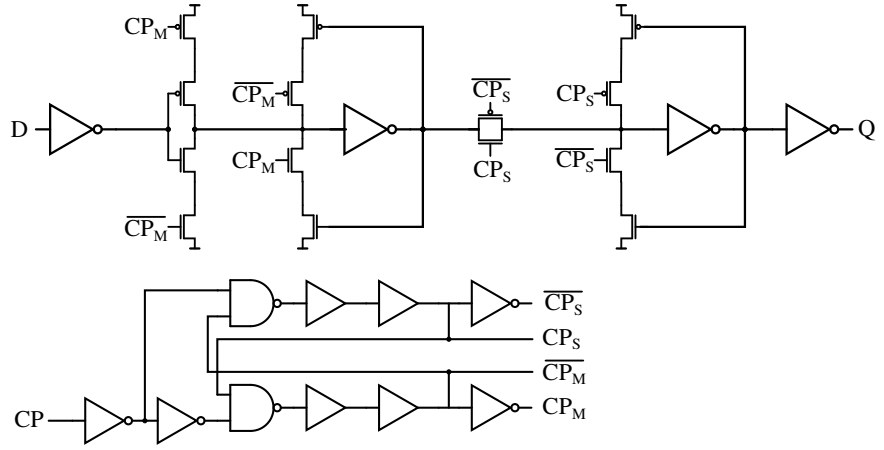


Figure 4.21: Transmission-gate clocked-CMOS (C^2MOS) D-flip-flop implementation with non-overlapping clock generator for hysteresis reduction.

A post-layout hysteresis performance on the level of 275 fs was obtained assuming typical process parameters. Achieving lower levels of hysteresis was found difficult when only single-ended CMOS clock signals are available. Differential sampling latches, such as the ones presented in [105] or [25] can offer significantly better performance in this regard, relying however on the availability of differential clock signals and have thus not been considered here. A remedy for this issue could also be found in a reset of the phase detector flip-flop before each reference clock cycle. This could however require increasing the loop delay, which increases the limit cycle jitter of the PLL.

The obtained post-layout simulation results of the three evaluated phase detector cells are graphically summarized in figure 4.22. The shown results are obtained from transient simulations using noise-free clock signals with device noise enabled. For each value of clock phase difference Δt_{CD} an ensemble of transient simulations is performed, and the probability of the register output settling to either of the possible binary values is shown on the Y-axis. Each of the trajectories is additionally affected by sampling jitter due to device noise. To obtain a measurement of the hysteresis, a separate set of such simulations is performed with the BBPD initially set to zero or one. In the presence of hysteresis, two distinct trajectories emerge, which can be seen for all three evaluated designs.

The achieved hysteresis performance of the optimized BBPD is a significant improvement over the initial baseline cell and considered acceptable for the intended application. An interesting result of this study is that a cell-based

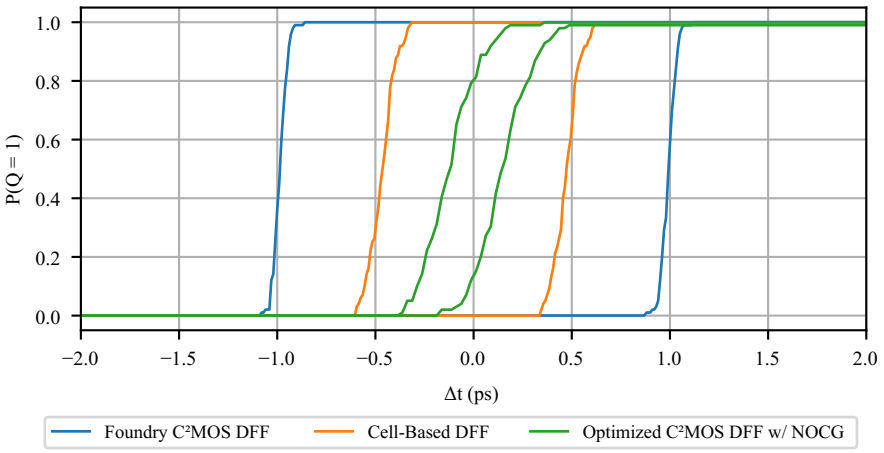


Figure 4.22: Hysteresis and noise performance for three evaluated CMOS BBPD implementations obtained using post-layout simulations.

phase detector with reasonable performance consisting only of library cells is in principle feasible while also outperforming a standard library D-flip-flop. This suggests that such phase detectors could be implemented using a fully digital implementation methodology. However, it shows that phase detector performance must nonetheless be studied using isolated transistor-level simulations whenever low jitter applications are targeted, and secondary issues such as routing parasitics and circuit matching must be carefully considered. Another outcome is that the performance achievable using single-ended clock signalling has practical limits, and that differential signalling for critical clock signals will need to be adopted for more demanding applications in the future to systematically eliminate hysteresis issues.

4.6.4 Clock Dividers

A synchronous counter-based divider is used in the PLL feedback path to derive all required clock signals. Its implementation as a synchronous binary counter circuit lends itself to hardening against SEEs using TMR in the same manner as the other digital loop components. Beneficially for the application at hand, it inherently provides access to intermediate divider stages, which can be used to clock other digital loop components (DLF, $\Sigma\Delta$M, etc.) and to implement the required selection of reference clock frequency or data rate. Further advantages of the synchronous implementation arise from the fact that all flip-flops within the divider are clocked using the common input clock. This not only has the benefit of all intermediate clock signals being inherently phase-aligned, but also avoids the issue of jitter accumulation occurring when using multiple cascaded independent divider stages. The designed divide-by-32 divider includes full TMR protection and is implemented together with the other digital loop components using 9-track foundry standard library cells. The circuit operates with a 1.28 GHz input frequency, meeting the previously discussed setup and hold margins for TID tolerance.

4.6.5 Digital Loop Filter and Sigma-Delta Modulator

The loop filter is implemented as a proportional-integral (PI) structure driven by the single-bit phase error information provided by the BBPDs. Control over the loop transfer function is given by programmability of the loop filter coefficients α and β. The required range of these coefficients to realize all desired transfer functions needs to be determined, since it directly dictates the word lengths required for the data path in the DLF and $\Sigma\Delta$M.

To arrive at an appropriate sizing, a lot of insight can be obtained from the thorough theoretical analysis presented in [25]. A first important consideration is the required available frequency tuning step size and its impact on the expected PLL jitter. Based purely on a simplified analysis of the steady-state behavior of

a noise-free second-order BBPLL, equations 3.22 and 3.23 in [25] (reproduced below) formulate closed-form solutions for the minimum achievable bang-bang jitter. The peak-to-peak jitter of such a system with divider ratio N, DCO period gain K_T, integral gain α and loop delay D can be described as:

$$\Delta t_{pp,opt} = 5.22 N \alpha K_T (1 + D)^2. \tag{4.14}$$

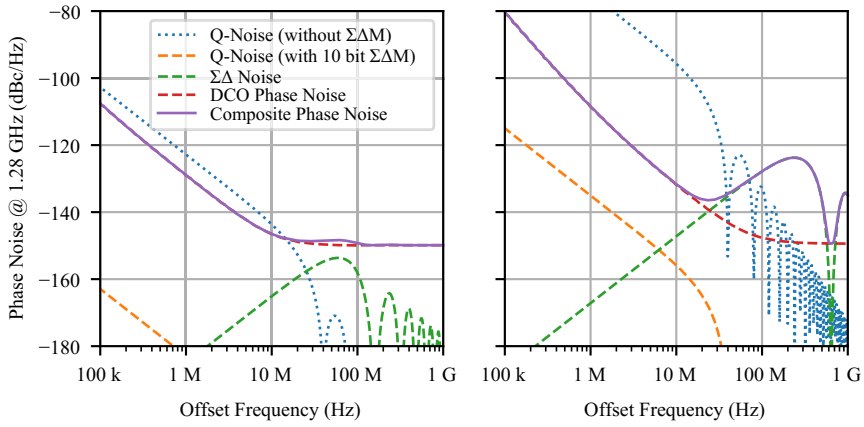
The implemented DCROs offer a frequency resolution of about 4 MHz around their 1280 MHz center frequency, equivalent to a period resolution of 2.43 ps. Even assuming a loop delay of $D = 1$ reference clock cycle and $N = 32$, this resolution (equivalent to $\alpha = 1$) does not result in remotely acceptable levels of closed loop jitter. This strongly motivates the introduction of the ΣΔM to enhance the available resolution. In order to limit the rms contribution of this source of quantization-related jitter to below 1 ps, an integral gain α of better than 2^{-9} is required. This suggests the adoption of a 10 bit word length for the ΣΔM and also dictates the lower bounds for the integral and proportional loop filter constants. The constraint for the optimal proportional gain β can be derived from evaluation of equation 3.22 in [25], which states that:

$$\beta_{opt} = (1.38 + 1.88D)\alpha. \tag{4.15}$$

For the noise-free BBPLL (considering only bang-bang jitter and $D = 1$), this equation suggests an optimal setting for β of around 3 times larger than α. In practice, this value for β will represent a lower bound, since the DCRO with its high intrinsic phase noise will also dictate the use of a large loop bandwidth and therefore larger values of β. For the LC DCO with its much better period resolution (about 4.53 fs at a 2.56 GHz center frequency, i.e. about three orders of magnitude smaller), the required resolution improvement is much less significant and higher values for α can be used if required from other considerations such as the reference tracking capabilities.

With this lower bound established, a refined analysis of useful values for β can be performed. When, as is expected in practice, random jitter is present on both the DCO and reference clocks, optimal performance (in the sense of the lowest composite noise at the output of the PLL) is normally achieved by selecting a loop transfer function resulting in equal contributions from each of the noise sources. While a purely theory-founded derivation of these transfer functions and output noise is feasible as demonstrated by [25], the system behavior can be studied equally well using simulations guided by the intuitions derived in this work.

Constraints on the order, word length and clock frequency of the ΣΔM are imposed by the magnitude of quantization noise in relation to the intrinsic phase noise of the oscillator. In particular for the LC ADPLL with its stringent jitter requirements, reducing the impact of frequency quantization noise to below the phase noise floor of the DCO is desirable, such that its good noise performance



(a) LC DCO (b) DCRO DCO

Figure 4.23: Phase noise spectrum of both proposed DCO circuits including ΣΔM noise shaping and quantization noise.

is not degraded. The noise shaping properties of the ΣΔM allow shifting this quantization noise towards higher frequencies. Since this shaped noise spectrum is weighted by the transfer function of the DCO, a shift to higher frequencies improves the achievable suppression. Figure 4.23 illustrates the expected phase noise composition considering the phase noise profile and tuning resolution of the two studied oscillator designs at an output frequency of 1.28 GHz. The analytical modeling of the quantization-related noise components follows the treatment in [20]. Both designs assume a phase noise floor of $-150\,\mathrm{dBc\,Hz^{-1}}$ and the use of a second order ΣΔM with 10 bit resolution. For the LC DCO, an operation frequency of the ΣΔM of 160 MHz is considered, while 640 MHz is assumed for the DCRO due to its significantly coarser tuning resolution. A frequency of 640 MHz represents the highest reasonably achievable frequency for this modulator configuration in the chosen technology. It can be seen that for both oscillators, the natively available DCO frequency resolution would significantly deteriorate the phase noise performance. In both cases, the quantization noise improvement achieved through ΣΔ modulation falls significantly below the DCO noise in the $1/f^2$ region. In the LC DCO, also the shaped noise components at high offset frequencies remain far below the phase noise floor. For the DCRO (for which the jitter performance of the PLL is less critical), this latter characteristic can not be reasonably achieved: The shaped quantization noise can be expected to dominate the PLL phase noise spectrum at large offset frequencies.

A behavioral system model was implemented by appropriately modeling

the various important components, in particular the tuning resolution and expected phase noise performance of the DCOs, quantization, rounding and truncation effects in the loop filter data path and the order of ΣΔ modulation. An advantage of this approach is the feasibility of including additional sources of imperfection, such as hysteresis and sampling jitter of the BBPD or the dynamics added by the ΣΔM, in the simulations.

Two scenarios representing the boundaries of relevant operation conditions were considered during the sizing simulations, which were evaluated with models for each of the considered DCO types. In the first scenario, random jitter of the reference clock is neglected and only DCO jitter is considered. This scenario is representative of low-input jitter situations in practice. In this configuration, the BBPD gain becomes largest and the optimal bandwidth becomes a trade-off between suppression of DCO phase noise (by increasing the loop bandwidth) and the amount of bang-bang jitter introduced by increasing β. In a second scenario, a very high level of reference clock jitter with Gaussian distribution and a standard deviation of 25 ps is simulated. An optimal loop filter transfer function in this scenario establishes the best possible trade-off between DCO and reference clock jitter. While this large amount of jitter necessarily reduces the effective BBPD gain, a smaller loop bandwidth is sought after in this configuration, such that a larger portion of reference phase noise can be suppressed. Among the different simulated scenarios, the LC DCO ADPLL was found to require larger proportional loop filter gain settings. To achieve the optimal value of total jitter in the simulation scenario with high reference clock noise, values for β of up to 2^2 need to be realized.

With the requirements for the range of α and β as well as the impact of quantization noise in the loop in place, the remainder of the data path can be sized. The implemented loop filter data path uses a word width of 16 bit to represent UQ6.10 fixed point numbers. This chosen normalized fixed point representation is founded in the physical segmentation of the DCO tracking bank: The six most significant bits (MSBs) of these words correspond to integer multiples of the tracking bank unit cell size, while the ten least significant bits (LSBs) are realized using fractional interpolation provided by the ΣΔM. The filter coefficients α and β can be configured to power-of-two values between 2^{-10} and 2^5 times the tracking bank unit cell size, satisfying the identified requirements. Another important factor to consider during the sizing of the ΣΔM word length is the linearity achieved by the tracking bank of the DCO. The ΣΔM can theoretically improve the frequency tuning resolution to any arbitrary precision, with limits set only by the timing closure of arithmetic operations with increasingly bigger word lengths. However, the linearity of the resulting tuning characteristic will be strictly limited by the matching of the individual unit cells. In theory, when using a ΣΔM with a word length of L_{SDM} bits, a worst case DNL of the tracking bank smaller than $2^{-(L_{\mathrm{SDM}}+1)}$ LSB must

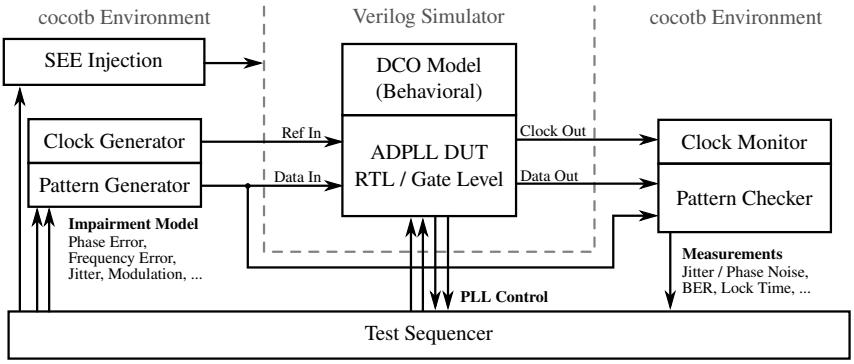


Figure 4.24: Simulation environment used for verification of the ADPLL evaluation test chip.

be achieved to guarantee monotonicity of its resulting characteristic at integer boundaries. In particular for word lengths much larger than the 10 bit chosen in this design, techniques such as dynamic element matching must be considered [22, p. 70].

4.7 Simulation Environment

Specific challenges arise for the verification of a digital PLL architecture with an emphasis on radiation hardening. Again contrasting the design to conventional charge-pump based PLLs, the digital-heavy nature of ADPLL circuits required the adoption of a different approach to simulations and the verification of SEE robustness. The large number of instances making up netlists of synthesized digital circuits is prohibitive to the use of transistor-level circuit simulations. Instead, the majority of simulations for such circuits are performed using on the RTL description or the gate-level netlist of the implemented circuits using event-driven simulators. A dedicated simulation environment was created that enabled not only the extraction of key PLL performance figures (such as locking behavior, loop transfer function, PLL jitter and jitter tolerance), but also satisfies the need to verify its SEE tolerance. The devised verification environment is shown in figure 4.24 and will be described below in more detail.

4.7.1 PLL/CDR Characterization

Transistor-level simulation environments used for the design of conventional PLLs have integrated many of the analyses tools required for complex analyses of time domain signals. Established verification methodologies and simulators

for digital circuits, on the other hand, lack many of these capabilities. The standard libraries offered by hardware description verification languages such as VHDL or Verilog do not offer signal processing related functionality themselves, while also not allowing for straightforward extension of these capabilities. As a solution to this problem, the cocotb verification environment [106] was adopted. This test bench environment natively interfaces event-driven HDL simulators to a Python runtime environment. In this way, any required signal processing algorithms can be implemented with the use of many of the well-established signal processing and analysis packages available in the Python ecosystem. A number of utility classes have been developed to facilitate the simulation of PLL and CDR circuits. On the input side, clock and data generators have been implemented including impairment models for phase and frequency offset, periodic and random phase modulation as well as duty cycle distortion. For instrumentation of the DUT outputs, analysis classes observe the output clock and data signals of the design under test. Using these, properties such as lock time, the output noise spectrum or modulation tolerance can be extracted.

To guarantee accuracy of the performed simulations, appropriate behavioral models for the different DCOs designs were derived from transistor-level simulations. These models accurately model the tuning characteristics of the oscillator, and include simplified models for their phase noise characteristics in the form of white frequency and phase noise with parameters fitting the simulated performance.

4.7.2 SEE Verification

SEE tolerance of all digital circuit components was systematically included in the RTL design in the form of TMR. However, it was found that even minor oversights during implementation (such as excessive optimization or automatic merging of majority voter structures within the EDA-tool-based implementation flow) can inadvertently compromise radiation tolerance. Sufficient protection against SEEs needed to be demonstrated using verification of the gate-level netlist level. This was achieved by extending the developed test environment with complementary SEE verification capabilities. These allow an injection of SETs and SEUs into each instance of the PLL gate-level netlist used during simulations. After the PLL initially completes its frequency acquisition procedure and achieves a locked condition in the presence of SEEs, the clock outputs are instrumented using a virtual clock phase measurement, such that any unexpected excursions from the steady-state value (i.e. SEPTs and SEFTs) can be used as a qualifier for detecting SEE responses. During the performed fault injection campaigns, SEUs and SETs were injected into all memory elements of the design, while only SETs were injected into the output nodes of all combinatorial cells. To achieve sufficient coverage of the full design, a high number of SEEs needed to be simulated. A high injection rate of one SEE

every two reference clock cycles was used to maximize the simulation efficiency, and a coverage of at least 100 SEEs per node in the netlist was targeted. Since the gate level netlist for a single PLL contains on the order of around 10000 standard cell instances, at least one million SEEs were injected per design and operation mode.

4.8 Radiation-Tolerant ADPLL Test Chip

Based on the results obtained in the previous sections, the proposed ADPLL circuits have been implemented and manufactured in a commercial 65 nm bulk CMOS technology. This section summarizes the relevant design details of the test chip. The main aims to be achieved with this test chip are the validation of simulation results as well as the experimental evaluation of the radiation hardness of the implemented circuits.

4.8.1 Chip Architecture

The test chip integrates a total of three ADPLL circuits, which differ only in the type of DCO they integrate. One of the circuits uses the varactorless LC DCO described in section 4.4. The ring DCO circuits presented in section 4.5 are used to implement the two remaining PLL circuits. Both the originally proposed reference DCRO and the improved RDUC DCRO designs are included to allow quantifying the improvement in SEE hardening using a direct comparison experiment.

While the design of the digital loop core controlling each of these three DCOs is largely identical, separate instances are used for each PLL instead of sharing a single one between the three DCOs. This enables simultaneous operation of all circuits, which was considered beneficial especially during the characterization in radiation test facilities. For this reason, each PLL circuit is equipped with dedicated I/O receivers and drivers instead of sharing a set of common I/O pads among the three PLLs. An I^2C-based register interface is used to configure and monitor the three PLL circuits.

4.8.2 Slow Control Interface

An I^2C interface is included in the test chip for control of the I/O circuitry as well as the three included ADPLL circuits. The I^2C slave provides a total of 50 eight-bit registers. For SEE hardening, its control and data path logic as well as the register content itself are protected by self-correcting TMR structures. To minimize on-chip activity and power consumption, the I^2C slave logic is driven by an on-chip ring oscillator, which remains disabled whenever the I^2C bus is idle. Electrically, the I^2C bus is available on 1.2 V CMOS I/Os. A global reset

input with appropriate glitch filtering for SEE protection is also implemented within the control interface.

4.8.3 Hierarchical Implementation Approach

A hierarchical implementation approach was chosen for the test chip with two main goals in mind: It was considered desirable to evaluate the ADPLL circuits in the form of a macro cell. Being available in the form representative of intellectual property (IP) blocks simplifies the integration into designs emerging in the HEP community in the future. Additionally, the design partitioning was chosen such that a limited number of transistor-level simulations of the complete PLL circuit remained feasible at this level. This is beneficial since as a whole, the PLL circuit remains a noise-sensitive circuit component, and circuit characteristics such as power-supply sensitivity and noise coupling can still only be fully studied using this type of simulation. Separated power supply domains are implemented in each PLL for the DCO and the remaining digital logic such as the DLF, $\Sigma\Delta$M, dividers, etc. The rectangular macro blocks containing the LC and DCRO ADPLLs occupy an on-chip area of $0.41\,\mathrm{mm}^2$ and $0.095\,\mathrm{mm}^2$ respectively, illustrating the significant area advantage that the ring oscillator provides, even though the designs were not particularly optimized for area reduction.

The finished PLL macros are integrated into the test chip in a higher hierarchical level during full-chip assembly. At this level also the $\mathrm{I}^2\mathrm{C}$ control interface is implemented and connections to the chip power distribution network and differential I/O drivers and receivers are established.

4.8.4 Physical Implementation

An overview over the layout of the implemented test chip is shown in figure 4.25, and the corresponding photomicrograph is shown in figure 4.26. The three included ADPLL circuits are placed on the right half of the ASIC, and the dedicated I/O and supply voltage bond pads for each PLL are grouped and placed on separate edges of the die to reduce power supply coupling between them. Separate bond pads for two supply voltage rails, a reference clock and data input as well as three configurable differential clock outputs are available on each of the three chip edges dedicated to a PLL. The active area corresponding to each of the three PLL circuits is highlighted using a darker shade, confirming the significant difference between the different DCO topologies. The otherwise unused silicon area of the test chip is filled with on-chip decoupling for each of the different supply voltage domains.

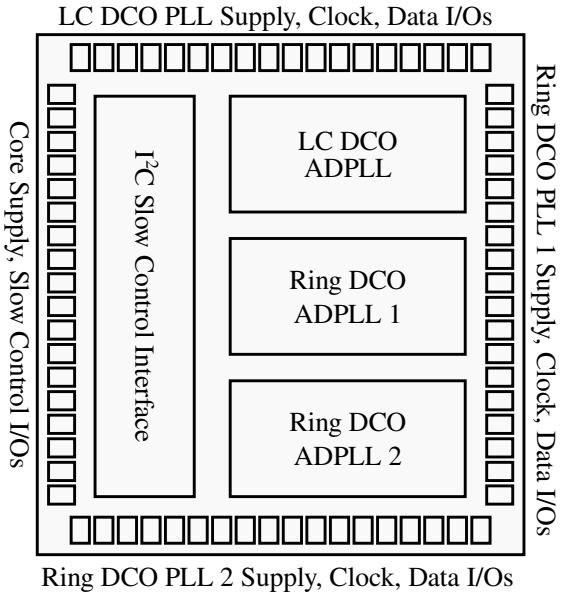


Figure 4.25: Annotated layout of the ADPLL test chip.

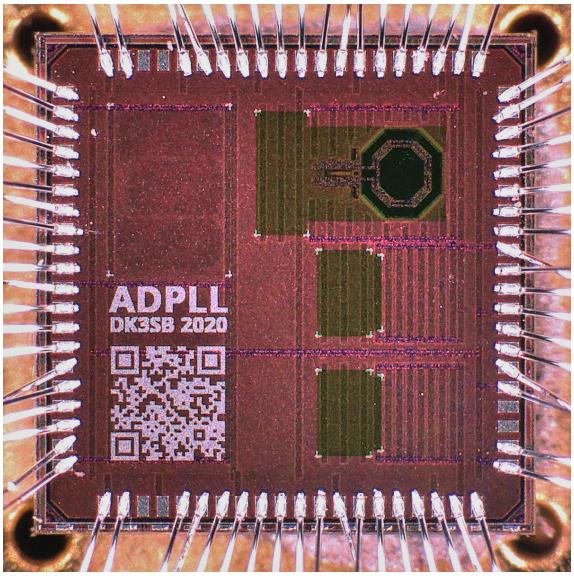


Figure 4.26: Test chip photomicrograph. The three PLL circuits are visible on the right side of the layout. Additional SEE test structures are placed on the left side of the chip.

Chapter 5

Radiation-Tolerant ADPLL Test Chip Characterization

This chapter summarizes the experimental characterization results of the implemented ADPLL clock generator circuits. Similar to the design procedure followed in chapter 4, the performance of the different manufactured DCO designs are characterized first. Following the presentation of these results, relevant aspects of closed-loop PLL performance are presented and discussed and the results compared to the initially identified circuit specifications.

5.1 DCO Characterization

This section presents the open-loop characterization of the three DCO designs integrated in the test chip. The LC DCO is presented individually first, while the obtained characterization results for the two DCRO circuits will be discussed using direct comparisons due to their similarities in most design and performance aspects. The manufactured test chip includes testing functionality that allows overriding any of the digital frequency control setting of the DCO. Without any closed-loop control engaged (i.e. with the tracking bank of the DCO set to a fixed value), the frequency of the free-running DCO was measured using a Keysight 53220A frequency counter. Phase noise measurements are obtained using a Rohde & Schwarz FSWP8 phase measurement test set.

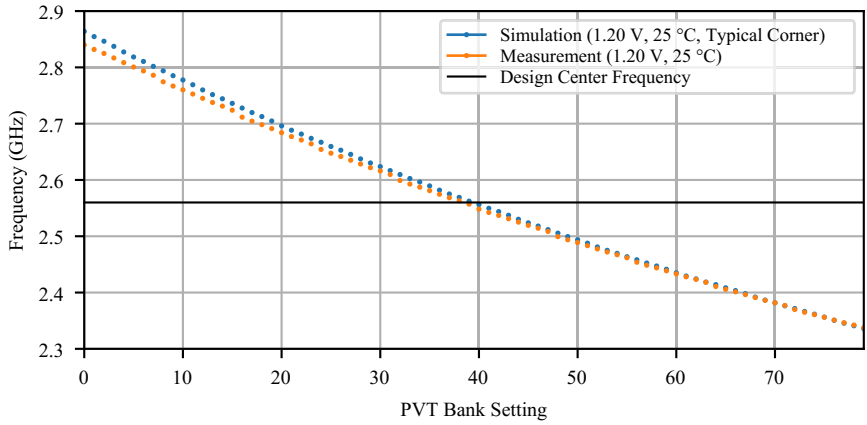


Figure 5.1: Obtained characteristics of the LC DCO PVT bank and comparison with simulations. Measurements were obtained with the remaining banks set to the center of their range.

5.1.1 Varactorless LC DCO

Tuning Range and Linearity

PVT bank: Using mid-range settings for the acquisition and tracking banks, the range and linearity of the tuning provided by the PVT bank cells was measurement. Figure 5.1 shows the obtained measurements of the free running frequency compared to a model extracted from post-layout SPICE simulations in typical PVT conditions. The difference of the measured sample against this simulation is within 1 % across the full tuning range. The tuning was found to be monotonous, and all cells for tuning were found to be functional. Given the dispersion over process corners expected from simulations (±7 %), the measurement can be considered to be in very good agreement. Due to the sensitivity of high-frequency LC oscillators to parasitics, this confirms that all relevant contributors have been adequately taken into account during the design process. The tuning characteristic was similarly found to match simulation results. Using the PVT bank alone, the DCO achieves the specified 20 % tuning range, which comfortably covers all expected process variations, leaving adequate margin for additional TID-induced shifts of the oscillator frequency. Since an overlap between the frequency step size of the PVT bank and the total range of the acquisition bank needs to be guaranteed, the largest frequency difference between adjacent banks was characterized and found to have a value of 12.5 MHz.

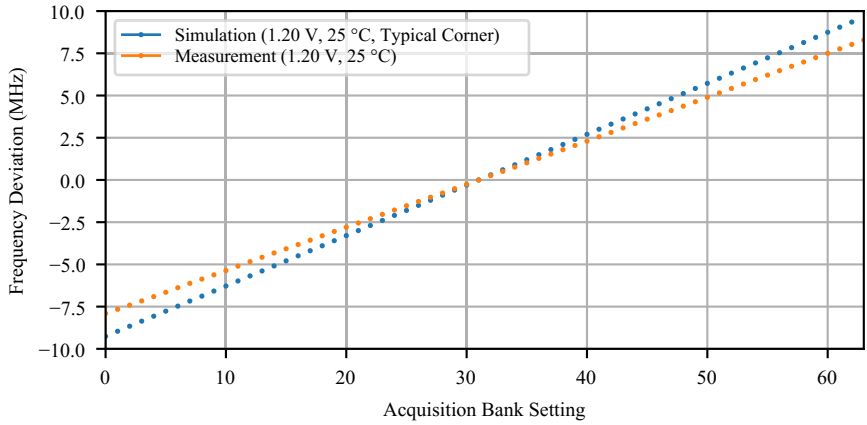


Figure 5.2: Obtained characteristics of the LC DCO acquisition bank and comparison with simulations. A minor difference to the expected unit cell capacitance with regards to the simulations can be seen.

Acquisition Bank: For characterization of the acquisition frequency bank, the PVT bank was configured to the value closest to the intended design frequency of 2.56 GHz. Figure 5.2 shows the tuning behavior obtained using the acquisition bank. Compared to the shown simulation results, the tuning range provided by the acquisition bank is slightly smaller than anticipated. The measured tuning range of the bank is 16 MHz, which still covers the worst case PVT bank step size of 12.5 MHz with sufficient margin. Similarly to the PVT bank, the linearity of this bank is not of primary importance, as the value selected for the acquisition bank remains fixed after the frequency acquisition process of the PLL. Nonetheless, the linearity achieved by the array of thermometric capacitor cells in the acquisition bank was found to be excellent, with the peak DNL not exceeding 0.05 LSB. This gives a positive indication that the cell design does not suffer from underlying issues related to device-matching.

Tracking Bank: The tracking bank, used in closed-loop operation of the PLL, is directly driven by the digital PLL loop filter. The very small differential capacitance provided by the cells of this bank requires additional care during characterization. It was found that the short-term frequency stability performance of the DCO due to thermal effects and low-frequency phase and frequency noise processes does not allow using long measurement intervals. Instead, a differential measurement approach was implemented. Using short individual gate times of 100 ms, the frequency difference between two settings

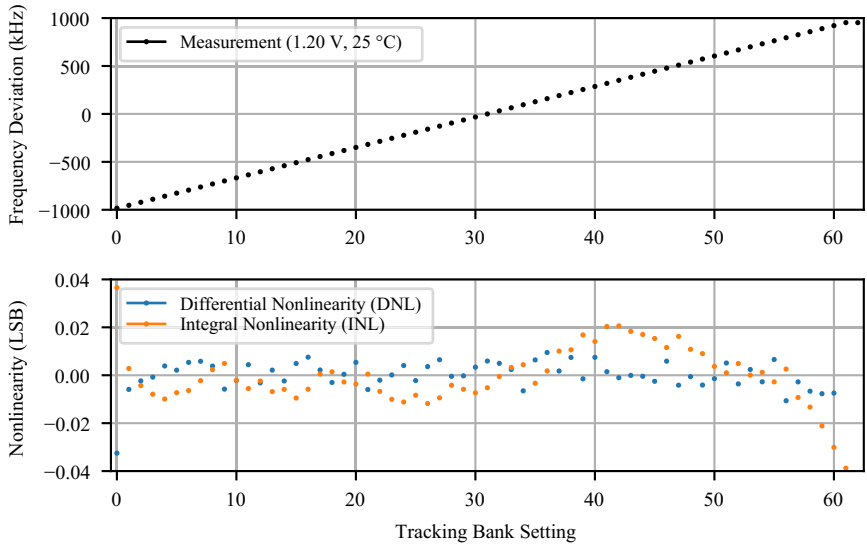


Figure 5.3: Obtained characteristics of the LC DCO tracking bank and linearity measurement results. Outstanding DNL and INL has been achieved with the custom MOM cell design.

of the tracking bank measured in quick succession instead. Since both these frequency measurements are similarly affected by oscillator instabilities, the mean of such difference measurements robustly converges to the true value of the frequency difference between them. During the performed characterization measurements, the mean of 100 such difference measurements was calculated. Following this approach, the measurement uncertainty could be reliably reduced to below 0.001 LSB, and hence significantly lower than the actual nonlinearity of the cells.

Figure 5.3 summarizes the measurements obtained for all available tracking bank settings. The mean step size is found to be 31.75 kHz, or 12.4 ppm. Expressed in terms of equivalent unit cell capacitance, each unit cell offers a capacitance difference of 63.5 aF. Compared to the design value of 66 aF, this small amount of deviation validates the custom design and simulation approach chosen for this cell. The tracking bank was further found to offer a total tuning range of 2 MHz. Since this range is equivalent to four times the step size of the acquisition bank, very good centering of the tracking bank by the frequency acquisition process can be guaranteed. Also shown in figure 5.3 are the derived linearity characterization results for these cells. Exceptional differential nonlinearity performance of about 0.01 LSB rms is found for the

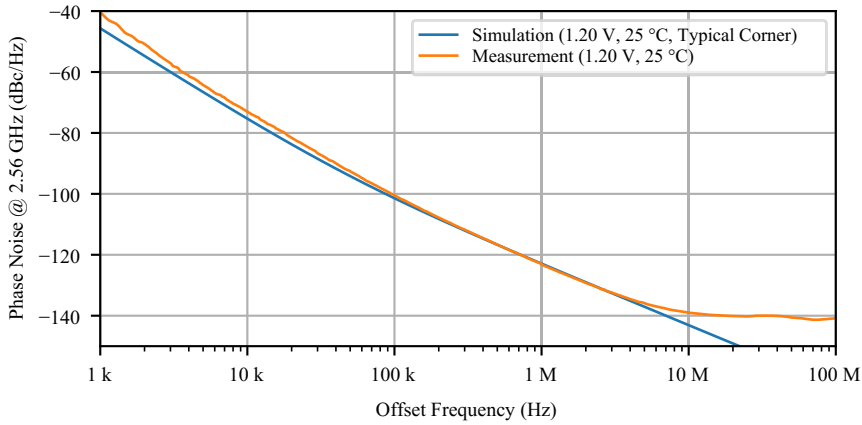


Figure 5.4: Phase noise measurements of the LC DCO.

tracking bank. Only for its first cell, placed on the edge of the bank and without any layout dummy cell adjacent to it, a small edge effect is visible. For all other cells, the mismatch appears to be dominated by random, lithography-related effects. A similarly good peak-to-peak INL of below 0.06 LSB is found, such that no relevant degradation of the PLL closed loop performance is expected as a result of these measurements.

Open-loop phase noise

The open loop phase noise of the LC DCO is characterized using PVT, acquisition and tracking bank configuration settings resulting in oscillation close to its target frequency. Figure 5.4 compares the simulated and measured open-loop phase noise of the DCO. Since the oscillating nodes of the DCO can not be probed directly in-circuit, this measurement is performed at one of the outputs of the divide-by-two prescaler. The shown measurement values are re-normalized to the DCO frequency. Again, very close agreement to the simulated performance is found. The level of close-in phase noise is very slightly increased compared to the simulated performance, which is either a result of limitations in the transistor noise models used during simulations or of power supply noise coupling. Since during PLL operation, much of the close-in phase noise is suppressed, this minor discrepancy is of no practical consequence. Very good agreement of the two phase noise characteristics is found between 100 kHz and 3 MHz, where it is dominated by white frequency noise processes. The wide-band phase noise floor of around $-140\,\mathrm{dBc\,Hz^{-1}}$ above offsets of approximately 10 MHz originates within the on-chip clock distribution network up to

the measurement output pad, which uses only standard library cells instead of dedicated clock buffers optimized for noise performance. The DCO tail current for this measurement was chosen the same as for the simulation result. When reducing the tail current significantly, the wide-band DCO noise floor was found to increase due to reduced drive amplitude reaching the the following buffer and divider stage, up to the point where the divider fails to operate correctly or stable oscillation is no longer achieved. For higher tail currents, the power supply rejection performance was found to worsen, resulting in an increase of phase noise below offset frequencies of about 10 kHz.

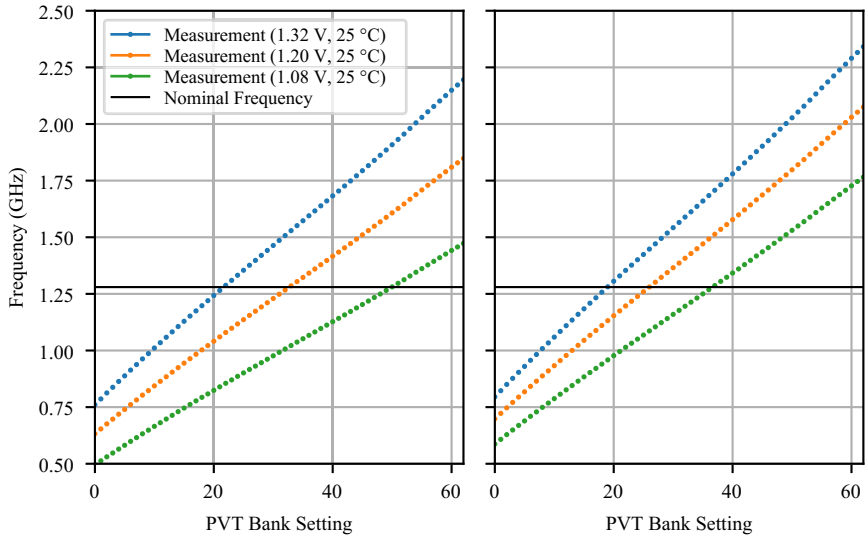
Together with the power consumption of 5.6 mW which was measured in this operating point, a FOM for the LC DCO can be calculated using equation (2.3). With a phase noise of $-123\,\mathrm{dBc\,Hz^{-1}}$ at an offset frequency of 1 MHz, the DCO achieves a FOM of $183.7\,\mathrm{dBc\,Hz^{-1}}$.

5.1.2 Radiation-Tolerant DCROs

Both ring oscillator designs presented in section 4.5 were included in the test chip. Their main difference concerns the tolerance to single-event effects, and to allow adequate comparisons between both, their designs are comparable in as many other aspects as possible. Similar to the characterization of the LC DCO, their tuning range, linearity and phase noise performance were characterized.

Tuning Range and Linearity

PVT Bank: Coarse frequency control of the DCRO frequency is available using a logical PVT bank. Five unit cells (one of each of the five ring oscillator stages) are grouped together to form the individual frequency control steps of this bank. Figure 5.5 summarizes the performed measurements of the free-running oscillation frequency for different settings of this bank. The results for both DCRO designs are shown side-by-side. Since the ring oscillators are additionally subject to much larger variations over supply voltage range than the LC DCO, results are shown for three supply voltage conditions, covering a range of 1.2 V±10 %. Importantly, and in line with the performed simulations, these measurements confirm that the target frequency requirement of 1.28 GHz can be met across the full supply voltage range. As further expected, the SEE-hardened DCRO shows a slightly higher tuning gain, which allows providing a slightly higher oscillation frequency. This practically translates to slightly larger margins for process variation and device degradation resulting from TID. For the lowest characterized supply voltage, margins of 13 % and 37 % are found. The lowest obtainable oscillation frequency is limited by the number of unit cells hard-wired to always remain on. The tuning curves shown in figure 5.5 were obtained with the tracking bank set to mid-range. Since the tracking bank (consisting of 66 cells) covers a range of approximately thirteen PVT bank steps



(a) Unhardened DCRO. (b) Hardened DCRO.

Figure 5.5: DCRO PVT bank characterization results.

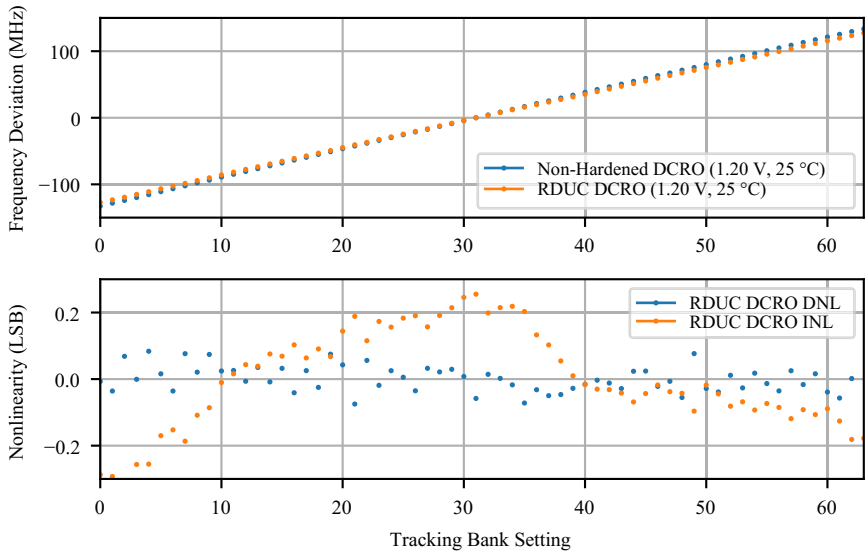


Figure 5.6: DCRO tracking bank characterization results.

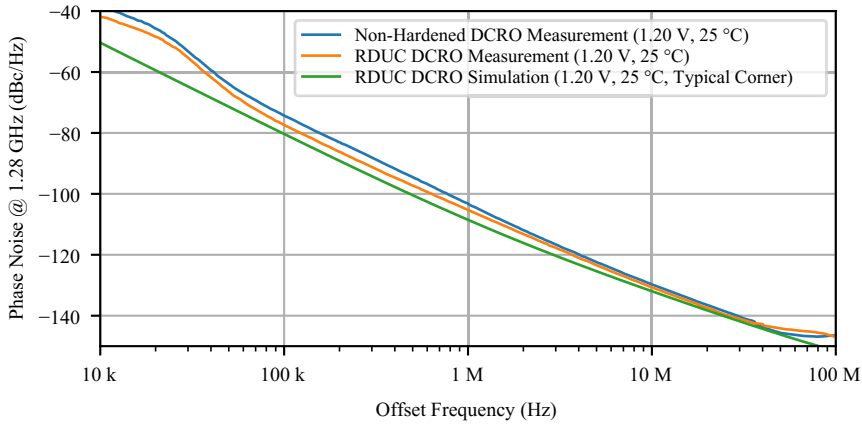


Figure 5.7: Phase noise measurements obtained for the different DCRO designs.

by design, the total tuning range of both oscillators (and hence their margins for PVT and TID) are larger than shown, as long as a partial reduction of the tracking frequency range is accepted.

Tracking Bank: During closed loop control, a smaller bank of thermometric unit cells are used. The tracking bank characteristics of both oscillators around the design center frequency have been measured and are shown superimposed in figure 5.6. In the vicinity of the design frequency, both oscillators offer an essentially identical tuning resolution. A rather large frequency range of about 200 MHz is covered by the tracking bank, which is necessary to account for the relatively large supply voltage sensitivity inherent to the design. Similarly, the linearity performance was found to be very comparable, and as such figure 5.6 omits linearity measurements of the non-hardened DCRO design for clarity. The tracking bank provides a DNL performance of better than 0.05 LSB rms, which is sufficient for the intended application in systems with relaxed jitter and spurious requirements.

5.1.3 Open Loop Phase Noise

The open-loop phase noise was characterized at the nominal design frequency of 1.28 GHz. Figure 5.7 shows measurements of both oscillator flavors compared the simulated phase noise characteristics of the design. Both oscillator types offer qualitatively very comparable phase noise performance, differing only by up to 2 dB to 3 dB across the relevant offset frequency range. The phase

DCO Type	LC DCO	Non-Hardened DCRO	RDUC DCRO
Design Frequency (GHz)	2.56	1.28	1.28
Tuning Range (GHz)$^{(1)}$	2.35 - 2.83	0.75 - 1.45	0.80 - 1.75
Tuning Resolution (kHz)$^{(2)}$	31.7	4200	4000
Power Consumption (mW)	5.6	6.9	7.1
Phase Noise (dBc Hz^{-1})$^{(3)}$	-123	-104	-105
Oscillator FOM (dBc Hz^{-1})	183.7	158	159

Table 5.1: Comparison of obtained design parameters for the different implemented DCOs.

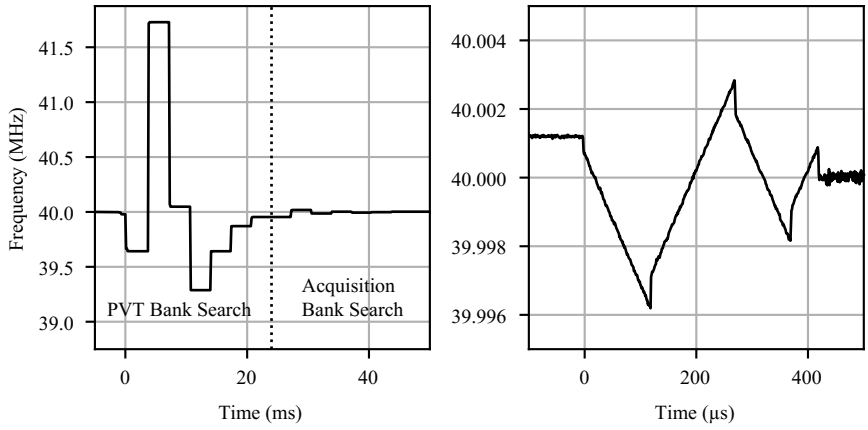
Note 1: Reflects the contiguous frequency range available across 1.2 V±10 % supply voltage variations.
Note 2: Refers to the frequency step size of the tracking bank in vicinity of the design frequency.
Note 3: Phase noise measurements obtained at 1 MHz carrier offset.

noise of both DCO designs are slightly higher than the values predicted in simulations. The rather significant deviation up to offset frequencies of 50 kHz is explained by the high power supply sensitivity of the oscillator design. In this region, noise produced by the off-chip voltage regulator degrades the oscillator noise performance. Likely explanations for the smaller deviations at higher offset frequencies can be found in the noise variability of the minimum-length devices used throughout the oscillator, or in inaccuracies of the device simulation models.

The nominal power dissipation of both oscillators was measured to be 7 mW when operating at the target design frequency of 1.28 GHz. Evaluating equation (2.3) again for a 1 MHz offset frequency at nominal supply voltage conditions, the unhardened DCO achieves a FOM of 158 dBc Hz^{-1}, while the hardened DCO achieves 159 dBc Hz^{-1}.

5.1.4 Summary

Both oscillator types were found to meet their respective design requirements over the full specified supply voltage range. Tuning range, phase noise and power consumption agree well with simulation results. The linearity performance of the tuning banks used for closed-loop operation was found to satisfy the requirements of the respective application scenarios. Finally, the performance characteristics of the two manufactured DCRO designs are found to be very similar, which makes them viable designs for one-to-one comparisons in irradiation experiments. Table 5.1 summarizes and compares the key parameters of the three oscillators.



(a) LC ADPLL frequency acquisition. (b) LC ADPLL phase acquisition.

Figure 5.8: Frequency and phase acquisition transients of the prototype ADPLL.

5.2 PLL Characterization

In the second phase, the performance of the implemented PLL circuits was characterized. Similarly to the previous section, the obtained characterization results are discussed in a comparative manner, based on the differences and similarities between the included DCO flavors. Phase noise and transient frequency measurements were obtained using a Rohde & Schwarz FSWP8 phase noise test set. Reference clock and data generation was implemented using a Keysight 81134A pulse and pattern generator. Additional reference modulation in the form of random phase noise or periodic signals was implemented using a Keysight 33250A arbitrary waveform generator. For jitter tolerance characterization in CDR mode, a Keysight N4903B bit error rate test set was used. Where not specified otherwise, the results presented in this section were obtained in PLL mode of operation, with feedback division ratios configured to lock to a 40 MHz reference clock. Before detailed characterization was performed, all foreseen modes of operation, input reference clock frequencies and bit rates were exercised. For all tested combinations, correct operation and acquisition of phase lock was confirmed. During operation in CDR mode, error-free data recovery was verified by means of bit error rate testing at all supported nominal bit rates.

5.2.1 Frequency Acquisition

To validate the frequency acquisition controller, an externally aided acquisition procedure using the on-chip frequency counters was implemented. This procedure performs binary search over the PVT and, if present, the acquisition banks of the DCOs. The progression of this coarse frequency acquisition process is illustrated in figure 5.8a. Starting from mid-range settings of all frequency control banks, iterative convergence to the optimal center frequency is obtained. It was demonstrated that for the LC ADPLL, this procedure is completed in about 40 ms when using off-chip controls. The DCRO PLLs finish the frequency acquisition process in about 30 ms, since in this oscillator no acquisition bank is used, reducing the number of required search steps. Since the majority of this time is used for I^2C communications, the frequency acquisition time could be reduced by at least one order of magnitude with an on-chip implementation of the same binary search.

5.2.2 Phase Acquisition and Lock Time

Closed-loop feedback control is engaged by initializing the loop filter integrator and disabling the tracking bank override feature used during frequency acquisition. A representative transient measurement of the LC ADPLL frequency following this configuration sequence can be seen in figure 5.8b. Before $t = 0$, a residual open-loop frequency offset after the finished frequency acquisition process is visible. Since this frequency offset is small, phase lock is achieved quickly, and the steady-state frequency, after lock is achieved, equals the 40 MHz reference frequency. The shape of the subsequent phase acquisition transient conforms to expectations. Phase tracking is achieved after about 400 µs for the chosen configuration. For the DCRO ADPLL, locking times are typically at least one order of magnitude shorter than the shown transient because of the larger frequency step size of the DCO, resulting in a much wider phase capture range. Additional measurements performed for both the LC and the DCRO ADPLLs confirmed that the lock-in range of the BBPD is large enough to ensure reliable acquisition of phase lock with arbitrary initial conditions of the tracking bank control word. To further reduce the phase capture time required for the LC ADPLL, gear-shifting techniques for the loop filter gain could be used if required in future applications [107].

5.2.3 Lock-In Range

The frequency range across which successful frequency acquisition and phase lock can be achieved has been characterized over the specified 1.2 V±10 % power supply voltage range. The results obtained in a 40 MHz (nominal) reference clock configuration are shown in table 5.2. The measurement results are in line

PLL Type	Min. Frequency	Max. Frequency
LC ADPLL (LC DCO)	36.5 MHz	44 MHz
DCRO ADPLL 1 (Non-hardened DCRO)	24 MHz	48 MHz
DCRO ADPLL 2 (RDUC DCRO)	25 MHz	58 MHz

Table 5.2: Measurements of prototype ADPLL lock-in range.

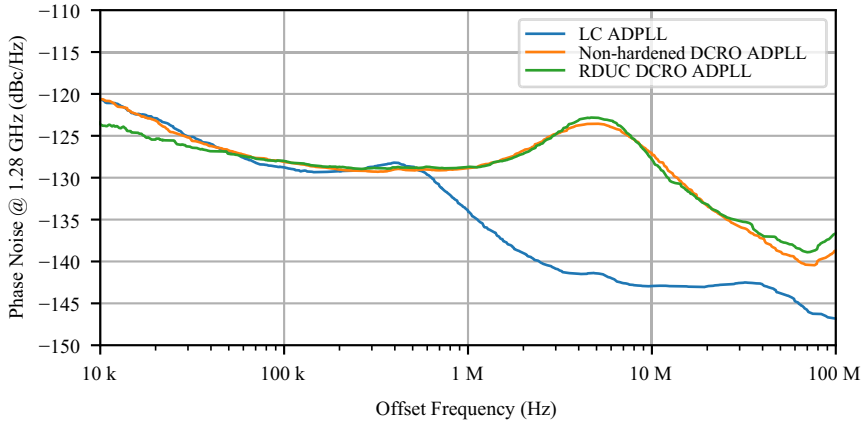


Figure 5.9: Optimal phase noise performance obtained for each of the ADPLL circuits using a low noise reference clock.

with the results obtained during the oscillator characterization process, which confirms that the lock-in range is dictated fully by the frequency acquisition procedure and the limitations of the oscillator tuning range. The measured range greatly exceeds the narrow required lock-in range of LHC applications, demonstrating the required robustness to process and temperature variations as well as margins for TID degradation.

5.2.4 Phase Noise and Jitter Performance

The jitter performance of the three implemented ADPLL circuits was characterized in steady-state conditions. Using a low-jitter (500 fs rms) 320 MHz reference clock, the loop filter configuration was optimized to minimize the integrated jitter produced by the three circuits. In accordance with expectations, this optimum is achieved at the lowest available setting of integral gain for both

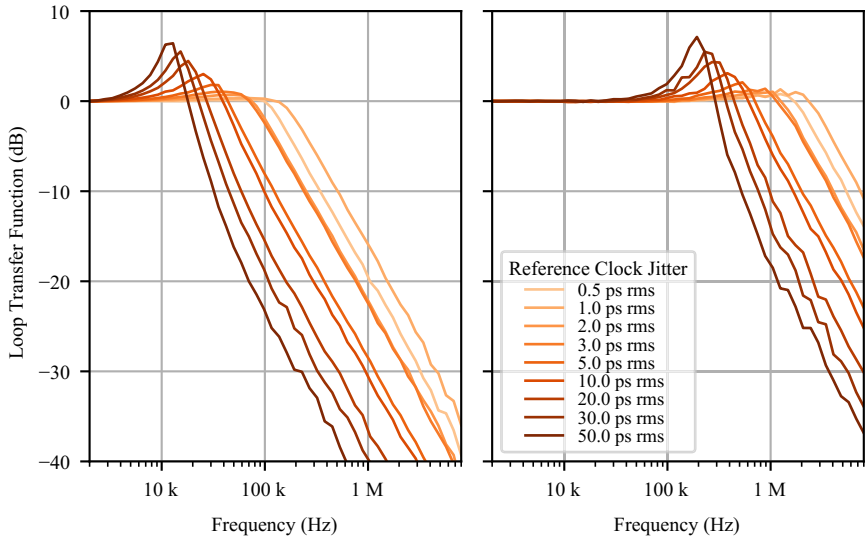
circuits. This condition maximizes the loop phase margin for any given setting of β, which minimizes peaking of the transfer function. A gain of $\alpha = 2^{-9}$ was therefore used when obtaining the presented measurements. For the LC ADPLL, the optimal proportional gain in this configuration was found to be $\beta = 2^{-2}$, while for both DCRO flavors the lowest jitter is achieved at $\beta = 2^{-5}$. The phase noise measurements obtained with these settings are shown in figure 5.9. Within an integration bandwidth from 100 Hz to 100 MHz, an integrated jitter performance of 530 fs and 1.6 ps is achieved for the LC and DCRO ADPLLs respectively. As anticipated from simulations, optimal performance for the DCRO PLLs is achieved using a significantly larger bandwidth due to their larger oscillator phase noise contributions. For this type of oscillator, some amount of jitter peaking can be observed in the optimal configuration. Another notable aspect illustrated in figure 5.9 is the very good agreement of the composite phase noise characteristics between the two types of DCRO ADPLL. This very similar performance obtained using both oscillator versions is crucial for the validity of side-by-side comparison experiments, for example during SEE characterization.

5.2.5 Loop Transfer Function

As outlined earlier, a critical property differentiating nonlinear bang-bang PLLs from their linear counterparts is the dependence of their transfer function on the jitter present at the phase detector. Jitter from both the reference clock as well as the DCO contribute to a change in the phase detector gain and therefore the loop dynamics, which makes accurately predicting loop performance more difficult than when using linear phase detectors. As the target applications require not only stability but also strive for operation close to the point of optimal jitter performance, the dependence of the transfer function on the input jitter is of large importance. For this reason, this relationship was experimentally characterized using the manufactured prototype.

For this measurement, the reference clock signal is phase-modulated using a controlled amount of white noise to obtain a desired level of rms reference clock jitter. The transfer function of the ADPLL is then measured by applying an additional sinusoidal phase modulation to the reference clock signal. By sweeping the frequency of this modulation signal and measuring the amplitude of the resulting spectral component in the PLL output spectrum, the transfer function can be obtained. During this measurement, the level of additional phase modulation on the reference clock must be kept significantly below the level of the random reference clock jitter to not influence the loop dynamics.

The loop filter was configured to optimize the integrated output jitter for an input jitter of 5 ps rms (LC PLL: $\beta = 2^{-1}, \alpha = 2^{-9}$; DCRO PLL: $\beta = 2^{-5}, \alpha = 2^{-9}$). The input jitter is then varied between 0.5 ps to 50 ps and the jitter transfer function is measured. The results of this measurement can



(a) LC ADPLL transfer functions. (b) DCRO ADPLL transfer functions.

Figure 5.10: Reference transfer functions of the ADPLL circuits for different amounts of white reference clock jitter.

be seen in figure 5.10a for the LC oscillator PLL. It was found that the circuit exhibits the expected reference transfer function characteristics. At the initial point (5 ps rms reference jitter), the transfer function shows approximately critical damping and a 20 dB per decade roll-off consistent with the type 2 PLL design. The expected behavior is also observed when the reference clock jitter is varied from this initial point: An increase in reference jitter causes a reduction in loop bandwidth (and vice versa). This is a consequence of the reduced phase detector gain when higher levels of noise are present. For reference clock configurations with very large amounts of reference clock jitter, the transfer function damping factor was found to reduce, down to approximately $\zeta = 0.3$ in the most critical transfer function shown. While problems with instability were not observed during these measurements, such excessively low damping factors are dynamically undesirable and a more appropriate loop filter configuration should be used depending on the expected levels of reference clock jitter. A number of adaptive digital techniques for optimization of the loop transfer function have already been proposed in the literature and could be adopted in future designs if large variations of the reference clock jitter are anticipated. Examples of such schemes can be found in [108, 109, 110]. The

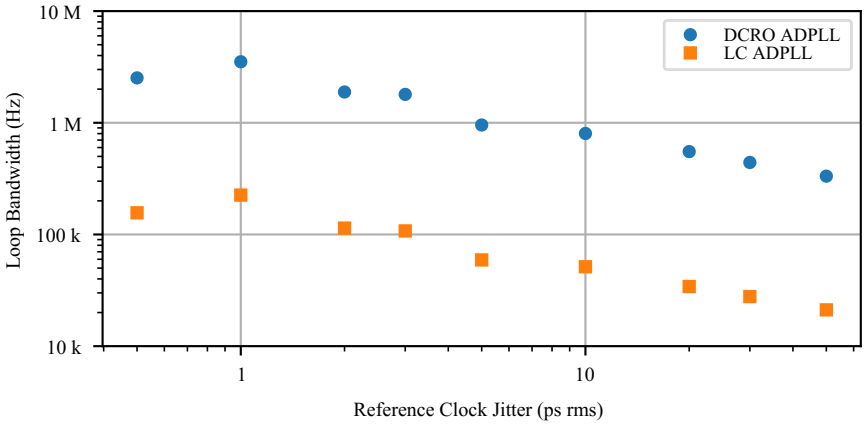
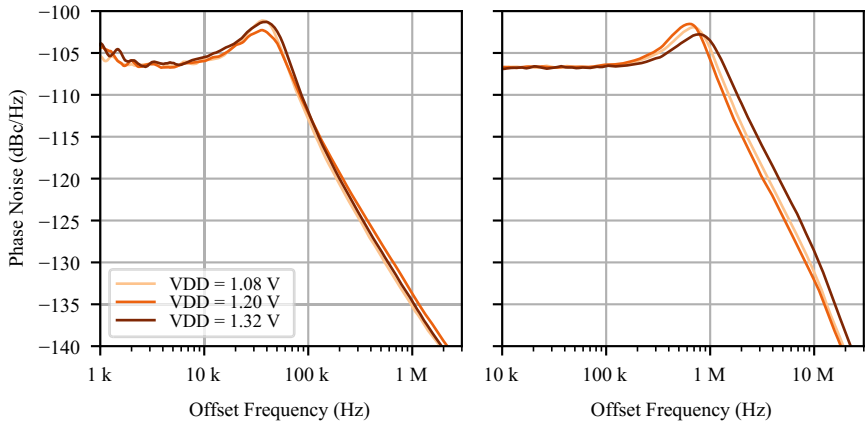


Figure 5.11: Dependence of PLL transfer function bandwidth on reference jitter. The loop bandwidth reduces when the level of reference clock jitter increases, which can be exploited as a beneficial property of this PLL architecture.

same measurement was repeated for the DCRO ADPLL, and the results are shown in figure 5.10b. Due to its higher DCO phase noise, the initial loop bandwidth chosen to minimize the output jitter is larger. However, as expected, the qualitative change in loop dynamics from increased or reduced levels of input jitter is identical to the LC ADPLL. While the large amount of input jitter used during this characterization procedure likely exceeds any value relevant in practice, additional techniques for stabilization of the loop transfer function could be implemented to mitigate this issue [25, pp. 104 sqq.], [109]. Finally, the loop bandwidth was calculated from each of the obtained transfer functions and is shown as a function of the input rms clock jitter for both PLL flavors in figure 5.11.

When considering the application requirements for the implemented circuit, which put more emphasis on the jitter performance than on the dynamic characteristics of the PLL, an interesting realization is that this change in dynamics of the BBPLL can be exploited as a beneficial property: In contrast to the constant bandwidth of PLL circuits with linear phase detectors, the BBPLL tracks the operating point of lowest composite jitter to a certain extent. When the level of reference clock jitter increases during operation, the PLL bandwidth automatically reduces as a consequence. This limits the contribution of the additional reference noise to the output jitter. The associated drawback that was already discussed above is the associated change of damping, which will ultimately limit the range of input jitter across which the PLL can retain



(a) LC ADPLL. (b) DCRO ADPLL.

Figure 5.12: Phase noise of the ADPLL circuits across 1.2 V±10 % supply voltage variations.

stable operation.

5.2.6 Loop Transfer Function Supply Voltage Sensitivity

One highlighted advantage of the ADPLL architecture is the independence of its parameters from process, temperature and supply voltage conditions. The largest remaining sensitivity of the loop dynamics to the supply voltage arises from changes of the DCO tuning gain. From first principles it can reasonably be expected that the LC ADPLL remains less sensitive in this regard than the DCRO ADPLL. The measurements shown in figure 5.12 were obtained by varying the supply voltage while the PLLs are operated with a constant 5 ps rms input jitter reference clock. While the change in loop dynamics was found to be rather limited for both designs, the DCRO ADPLL indeed shows a slightly higher sensitivity. This is consistent with the measurements obtained in figure 5.5, which did highlight some sensitivity of the DCRO tuning gain to the supply voltage.

5.2.7 Reference Jitter Suppression

Especially for the ADPLL flavor based on the LC DCO, providing a low-jitter output clock signal even in the presence of elevated levels of reference clock jitter was an important design requirement. During the design phase, the loop

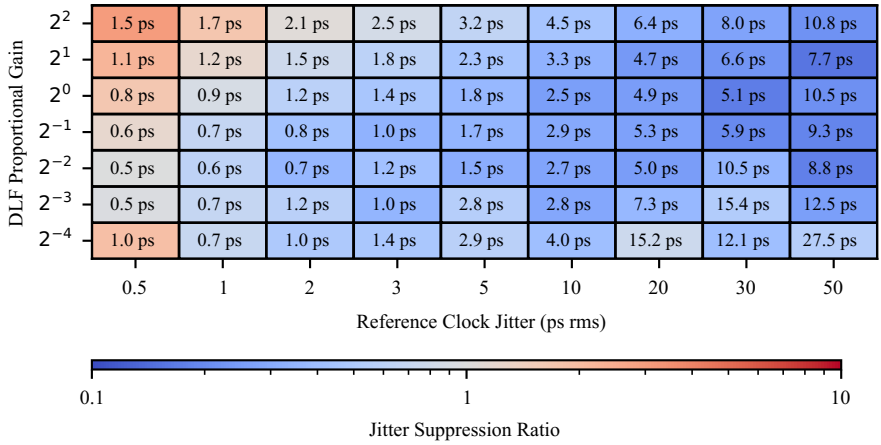


Figure 5.13: Measured LC ADPLL jitter suppression performance. Values in each cell indicate the integrated output jitter of the PLL, while the cell color indicates the ratio between output and input jitter. Lower ratios indicate better noise suppression by the PLL.

filter was sized such that a configuration providing an optimal transfer function could be realized for a wide range of input jitter levels.

This reference jitter suppression capability was evaluated experimentally using a reference clock signal with different, well-defined amounts of jitter. Similar to the previous measurements, the reference clock was phase-modulated using white noise. The jitter of the output clock signal provided by the PLL was obtained by integration of its phase noise spectrum between offset frequencies of 100 Hz and 10 MHz. This measurement is performed for different loop filter β coefficients, obtaining the results shown in figure 5.13.

Since an optimum (i.e. a configuration resulting in lowest composite jitter) can be achieved for any of the chosen input reference jitter values, the noise performance is limited by the DCO itself. For the lowest levels of reference clock jitter, no significant reduction below around 500 fs of integrated jitter can be obtained, and optimal performance is achieved for $\beta = 2^{-2}$. As the amount of input jitter increases, the reduction of phase detector gain leads also to a reduction in bandwidth (as shown previously in section 5.2.5). Since this is beneficial to tracking the jitter optimum, the point of smallest jitter remains relatively close to this initial value. The position of the optimum shifts to higher values of β for larger amounts of input jitter (up to $\beta = 2^1$). An increase in β proves beneficial in these regions since it additionally compensates the reduction in damping factor, and therefore reduces the jitter peaking. Jitter

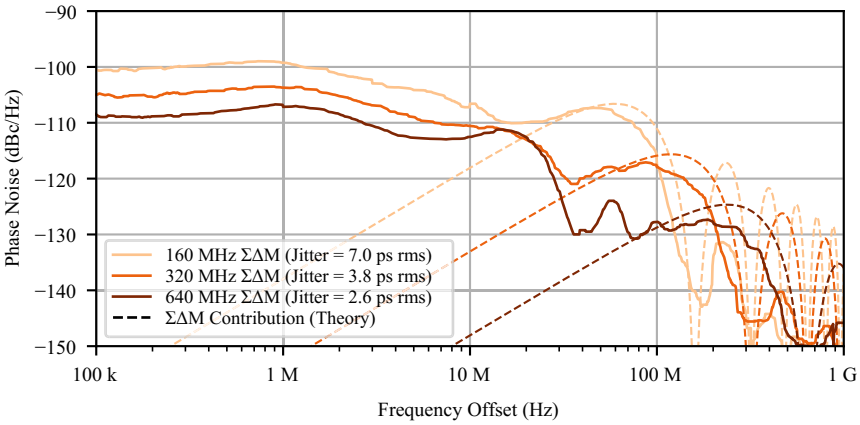


Figure 5.14: Output clock phase noise profiles of the DCRO ADPLL obtained for different operation frequencies of the ΣΔM. This measurement was obtained using a 1.28 GHz output frequency in order to obtain phase noise at offset frequencies up to 1 GHz.

suppression to the level of 5 ps rms can be obtained up to an input jitter of about 30 ps rms. While the obtained measurements using white phase noise provide good indications of jitter filtering capabilities, practical application scenarios may additionally need to consider the spectral composition of the noise present at the input of the PLL.

5.2.8 Sigma-Delta Modulator Clock Frequency

The selection of the clock frequency of the high speed ΣΔM presents an interesting power-performance trade-off, especially for the DCRO ADPLL. In the designed test chip, the ΣΔM can be configured to operate at between 160 MHz and 640 MHz, regardless of the chosen reference clock frequency. Operation at higher frequencies promises an increased suppression of the quantization noise arising from the limited frequency resolution of the DCO. For the LC DCO design with its high intrinsic frequency resolution, this trade-off is of little practical importance since ΣΔM operation at the lowest frequency of 160 MHz already suppresses the quantization noise to below the oscillator phase noise floor. An increase in its operation frequency only increases the power consumption without any material gain of noise performance.

The relatively coarse frequency tuning resolution of the DCRO instead allows trading off integrated jitter performance against power consumption. Measurements of the PLL output clock phase noise for the three available

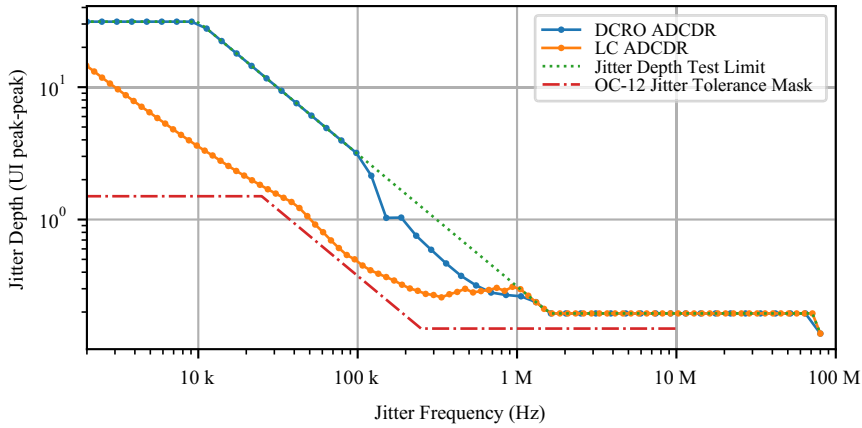


Figure 5.15: Measured jitter tolerance performance of the ADPLL prototype during CDR operation. Both types of CDR circuit meet the requirements set by the SONET OC-12 specifications.

frequency settings of the ΣΔM are shown in figure 5.14. Since the ΣΔM itself however accounts for only a small fraction of the circuit power dissipation, the difference between the 160 MHz and 640 MHz configurations is limited to about 15 % of the total PLL power consumption. Conversely, this fact illustrates that the move to smaller process nodes and the associated reduction of digital circuit power consumption will allow further leveraging this type of trade-off to improve jitter performance by either increasing the order or the operation frequency of the ΣΔM, instead of the tuning resolution of the DCO itself.

5.2.9 CDR Jitter Tolerance

The performance of the implemented CDR circuit was evaluated experimentally using the commonly used jitter tolerance metric. Since no strict specifications for this parameter exist in LHC applications, robustness was evaluated based on one of the commonly used Synchronous Optical Networking (SONET) Optical Carrier (OC) specifications. The OC-12 specification targeting a line rate of about 600 Mbit s^{-1} was used as a reference, since the data rates supported by the CDR are below this value. Experimentally, the jitter tolerance of the circuit was characterized for the highest supported data rate of 320 Mbit s^{-1} using an Agilent N4903B bit error rate test set. In accordance with the OC-12 specification, a sinusoidal phase modulation was applied to the data signal provided to the CDR circuit. The jitter depth in these measurements is defined as the peak-to-peak deviation of this phase modulation from an unperturbed

reference waveform. The measurement results are shown in figure 5.15, and highlight that both ADPLL circuits meet the requirements of this specification. While the original OC-12 specification defines a 1 dB power penalty as a pass criterion for this jitter tolerance test [111], due to the absence of an appropriate electrical channel model a bit error rate limit of 1×10^{-9} was used instead. In the low-frequency region, where jitter tracking is achieved mostly through the loop filter integrator, the DCRO-based CDR offers significantly wider margins due to its much higher integral path gain and its consequentially higher reference tracking capabilities [25, p. 72].

The jitter tolerance of the DCRO ADPLL in particular exceeds the jitter modulation capabilities of the used instrument across most of the measurement frequency range, such that only a lower bound for its jitter tolerance can be given.

5.2.10 Power Consumption

As a final property required to adequately contextualize the performance of the implemented circuits, their power consumption was characterized in the various modes of operation. Generally, the design goal of comparable power consumption of the two developed PLL circuit flavors was achieved: In a given reference configuration (room temperature, 1.2 V supply voltage, 40 MHz reference clock, 640 MHz $\Sigma\Delta$M frequency), the LC and DCRO-based ADPLL circuits dissipate 12 mW and 11.9 mW respectively. Across the various available configuration options (PLL or CDR operation, reference clock frequency, data rate and $\Sigma\Delta$M operation frequency), power dissipation varies between 10.1 mW and 13.4 mW for both flavors. Across the 1.2 V$\pm$10 % supply voltage range, power consumption varies by $\pm$20 %.

5.2.11 Summary

In summary, both designed ADPLL flavors were found to fulfill all functional requirements set out during the design phase and also offer the expected level of performances. The performed experiments have also quantified the impact of differing environmental conditions (using variations of supply voltage and reference clock jitter as a proxy), which indicate that the chosen circuit architecture and implementation is able to satisfy the requirements of HEP applications from a performance standpoint. To further aid the contextualization of these designs by comparisons to other works, both developed flavors of ADPLL can be assessed using the commonly used PLL FOM already presented in section 2.2. Based on equation (2.4), the FOM of the LC PLL is calculated to be -235 dB, while the DCRO PLL offers a FOM of -223 dB. A comparison with selected publications reporting on BBADPLL circuits taken from the scientific literature is shown in table 5.3. While it can be seen that better

Reference	**This Work**		**[112]**	**[113]**	**[109]**	**[114]**	**[95]**
Year	2020		2018	2020	2015	2012	2008
Node (nm)	65		28	28	65	22	65
Reference Freq. (MHz)	40-320		200	500	25	40	500
DCO Freq. (GHz)	2.56	1.28	15.6-18.2	12.8-15.2	2.5	0.3-3.2	4
PLL Type	Int-N		Frac-N	Frac-N	Int-N	Int-N	Int-N
DCO Type	LC	Ring	LC	LC	Ring	Ring	Ring
Jitter (fs)	520	1600	n/a	66	1720	3100	700
Power (mW)	12	12	n/a	19.8	1.72	3.4	17.2
FOM (dB)	-235	-223	-237	-250	-228	-224	-230

Table 5.3: Comparison of the proposed ADPLL circuits with selected publications in the scientific literature.

performance (in terms of power consumption, jitter performance and FOM) have been achieved in the state of the art, the proposed and tested circuit represent the first developments dedicated to an implementation of a radiation-tolerant ADPLL and none of the selected publications include claims about their reliability in radiation environments. With a functional and performance baseline established for the designed ADPLL circuits, the two following sections will quantify the achieved radiation hardness of both these circuits.

5.3 Single-Event Effects Testing

Single-event effects testing has been performed on all three developed ADPLL circuits. Testing was performed at the Heavy Ion Facility of the Cyclotron Research Center in Louvain-La-Neuve, Belgium. This facility provides access to a wide range of particle LET with variable and well-characterized flux, which is essential in obtaining values for the threshold LET and saturation cross section of digital circuits. For such circuits, these values can be used to estimate in-experiment SEU rates in accelerator environments based on expected particle field composition and flux [115].

5.3.1 Test Setup and Experimental Methodology

The test setup utilized for the performed heavy ion irradiation test campaign can be seen in figure 5.16. To assess the reliability of the ADPLLs using metrics relevant for practical operation, the phase of the output clock was chosen as the primary observable during these tests. To obtain the highest detection sensitivity, a low jitter 40 MHz reference clock was provided and the loop transfer

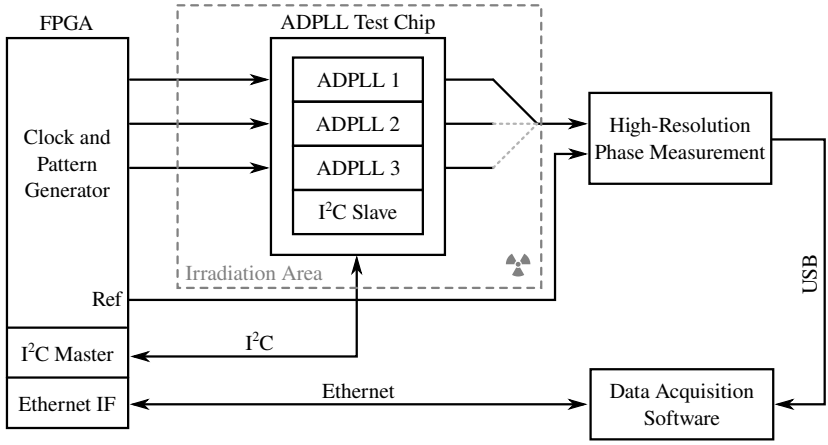


Figure 5.16: Test setup used during heavy ion testing at the CRC Heavy Ion Facility in Louvain-La-Neuve, Belgium.

function was optimized for lowest total jitter. To ensure comparable dynamic behavior of the two DCRO ADPLLs, these were operated with identical loop filter configurations. The clock phase of the ADPLL under test was measured using the analog phase detector setup described in section 3.4. Using this setup, any instantaneous deviation of the phase exceeding the total jitter of the ADPLL could be detected. The following sections discuss the observed SEE sensitivities in both types of ADPLL circuit as well as the relevant differences between the two DCRO flavors. The manufactured test chip was irradiated using six different ions, ranging in $\mathrm{LET_{Si}}$ from $1.3\,\mathrm{MeV\,mg^{-1}\,cm^2}$ to $62.5\,\mathrm{MeV\,mg^{-1}\,cm^2}$. A flux of $1.5 \times 10^4\,\mathrm{s^{-1}\,cm^{-2}}$ (the maximum offered by the facility) and ion incidence normal to the chip surface was used. The different PLL circuits were operated sequentially, and unused PLL circuits were powered down during irradiation. For each of the tested PLL circuits, a fluence of at least $1 \times 10^7\,\mathrm{cm^{-2}}$ was collected with each ion species. Figure 5.17 shows the test chip on its carrier printed circuit board (PCB) installed within the vacuum vessel of the facility.

5.3.2 Experimental Metrics

The heavy ion cross section (in particular as a function of LET) is a useful metric to assess and compare the sensitivity of the tested PLL circuits. However, since the cross section itself only reflects the number of observed events, its absolute value significantly varies with the magnitude and duration of responses that can be detected, which complicates comparisons of different independently tested circuits.

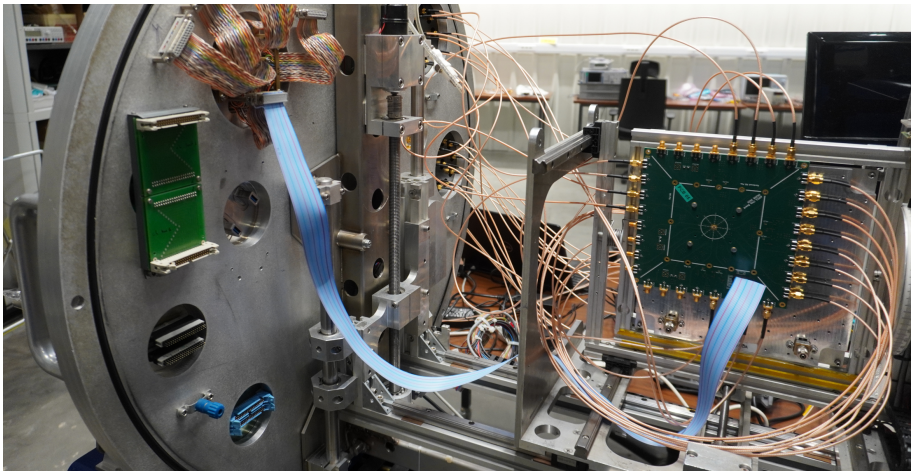


Figure 5.17: ADPLL test chip sample installed in the CRC Heavy Ion Facility vacuum vessel.

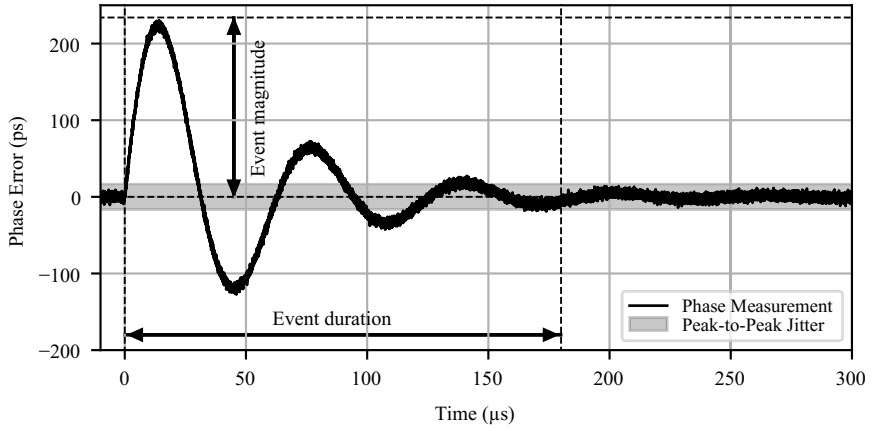


Figure 5.18: Event magnitude and duration metrics used for SEE characterization of the ADPLL circuits. This example transient is shown for illustration purposes only and does not reflect actual circuit performance.

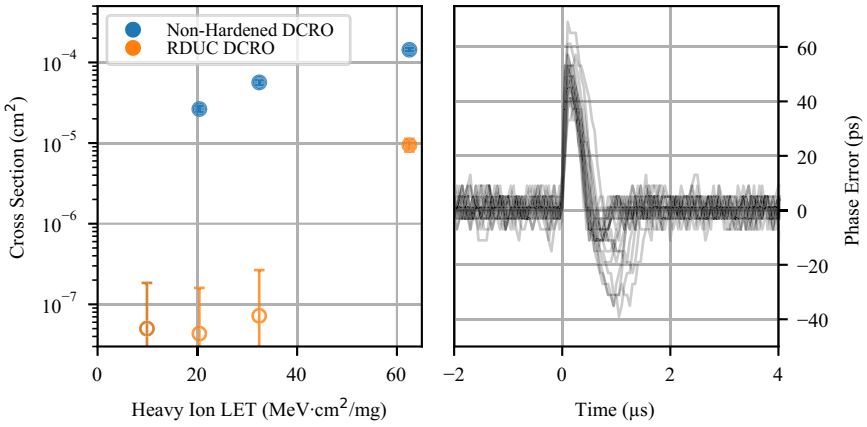
To better understand the SEE sensitivities, all observed circuit responses are characterized using the *event magnitude* and *event duration* as relevant metrics. The *event magnitude* is defined here as the maximum absolute value of phase deviation from its steady-state value during a radiation response. The *event duration* is defined as the time from the first phase excursion outside of the band of values explained by the peak-to-peak jitter, up to the moment of a persistent return into this band, which marks the end of the event. A visual interpretation of these two metrics is shown in figure 5.18. A final useful classification strategy applied is the distinction between SEFT and SEPT outlined in section 2.3. Using these metrics for the classification of all observed events, events can be differentiated and occurrence patterns and distributions of these metrics within each group can be analyzed separately. The utility of applying these metrics are then twofold: To the designer, this classification can guide the attribution of different event classes to different underlying mechanisms and the responsible components within the circuit. For the intended circuit application environment, this information is useful input to computational reliability assessments such as [9]. Results of such an assessment could be the expected rate of events exceeding a certain level of phase error magnitude and duration, or the calculation of mean-time-between-failure and availability metrics.

5.3.3 DCRO ADPLLs

Due to the similarity of the two DCRO ADPLLs and the goal of comparing the two presented oscillator designs, the results obtained with both circuits will be discussed jointly here. For these PLL circuits, the event detection threshold using the described setup was limited by the random PLL jitter of approximately 3 ps rms. Any excursion of the PLL phase from its nominal value of more than 16 ps for longer than 100 ns could be reliably detected and recorded.

Aggregate cross sections corresponding to the total number of detected events, regardless of their duration or magnitude for both circuits are summarized in figure 5.19a together with their 95 % confidence intervals. A significant difference between the two circuits can be observed. Compared against the baseline DCRO design, the RDUC DCRO significantly reduces the circuit cross section and increases the LET threshold. For both circuits, no SEE responses were detected at and below LET values of $9.9\,\mathrm{MeV\,mg^{-1}\,cm^2}$. For the two intermediate values of LET used in the test, a reduction of the cross section by at least two orders of magnitude was achieved. Even at the highest LET of $62.5\,\mathrm{MeV\,mg^{-1}\,cm^2}$, the proposed DCRO still improves the cross section by about 15x. Only at this point responses from the PLL using the improved DCRO design could be detected at all. At values of LET where no circuit responses were observable from a given ADPLL, cross section estimates representing an upper bound and corresponding confidence intervals were calculated following the recommendations in [116].

Only a single type of radiation signature was observed in both DCRO



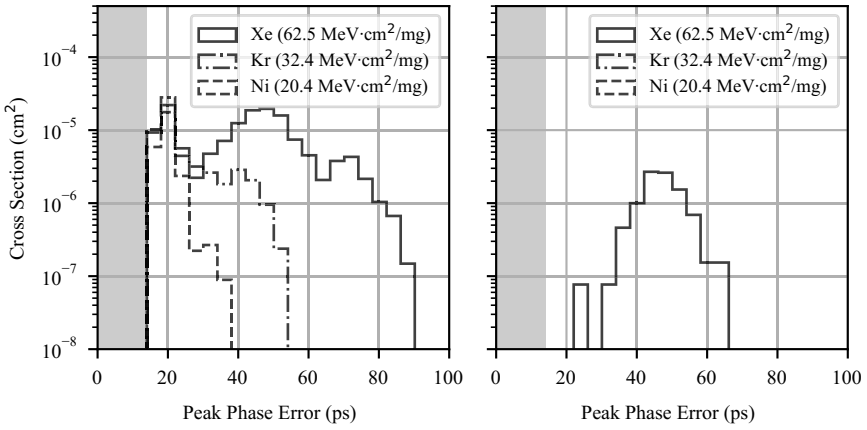
(a) Heavy ion cross section.

(b) Example SEE responses.

Figure 5.19: DCRO PLL heavy ion irradiation results. Unfilled markers in the cross-section plots signify the absence of detected circuit responses. The shown transient responses are obtained at an LET of 63.5 MeV mg^{-1} cm^2.

ADPLLs. These responses were always characterized as small SEPTs of a magnitude below 100 ps. A set of examples outlining the dynamics of this SEE signature is shown in figure 5.19b. All detected events are characterized by a duration in the range of single microseconds due to the fast loop response time.

Since the previously given cross section values do not give insight about the magnitude distribution of these SEE responses, figure 5.20 visualizes the observed distributions of event magnitude for the different ion species. The distribution of response amplitudes is found to be smooth, and expands in magnitude for the baseline DCRO as the LET increases. The largest event magnitudes for this design are in good agreement with the phase excursion estimates obtained during the simulations presented in figure 4.15. These simulations predicted a peak oscillator phase displacement of about 60° for the baseline oscillator design. This corresponds to 120 ps for an oscillation period of 780 ps, only slightly larger than the observed value. These simulations also predicted the observed scaling of the response amplitude with heavy ion LET through an increase of collected charge. In practice, this leads to a modulation of the aggregate cross section as events become too small to be detected towards lower values of LET. For the improved oscillator implementation, it can be seen that the total cross section is reduced significantly and the maximum phase error resulting from an SEE at the highest experimental LET is typically only about 50 ps, with no observed event exceeding 70 ps.



(a) Non-hardened DCRO (b) Proposed RDUC DCRO

Figure 5.20: Distribution of peak phase errors stimulated in the DCRO ADPLL circuits. The shaded region corresponds to the PLL random jitter, inside which SEE responses can not be detected.

A final aspect worth discussing based on the obtained data is whether a part of the observed sensitivity could originate inside the digital loop components. While in principle systematic hardening with TMR was used to mitigate any such SEE sensitivity, oversights during the design and verification process presented in the previous chapter might invalidate this assumption. Based on the magnitude and distribution of observed phase errors during the tests, it can be concluded that this is not likely. Sensitivities within the digital logic of the PLL would be expected to result in phase errors of significantly larger values than what was observed during the experiment. For example, corruptions of memory elements within the DLF or $\Sigma\Delta$M have the potential of resulting in very large phase and frequency errors corresponding to their binary weighting in the digital data words. Similarly, any SEE-related malfunction of the feedback divider circuits would be expected to result in phase jumps of at least 781 ps based on its operation frequency.

In contrast, the magnitude of the observed phase errors appears to follow a continuous distribution, which remains bounded at very small values. It was also found to scale with LET, which is a quality that would not be expected from an origin of these responses within a digital circuit. As a final argument to be made supporting this conclusion, the expected heavy ion cross-section of standard cell library D-flip-flops used in the design is reported in [88, Fig. 21]. At an LET of 9.9 MeV mg^{-1} cm^2, the expected cross section for these cells is still

about 50 % of their saturation value. The complete absence of any observable responses at and below this value of LET during the performed tests makes an explanation involving unprotected digital memory elements very unlikely. It is therefore reasonable to conclude that these responses are instead solely stimulated by charge collection in the oscillator.

In summary, the presented results allow confidently drawing three important conclusions:

1. The systematic hardening approach followed by using TMR in the digital loop components (divider, DLF, $\Sigma\Delta$M) proved successful, and the experimental results agree with the simulations of the digital design components.

2. Very high levels of SEE immunity of the DCRO are achieved by adopting a unit-cell based implementation, which maps naturally to digital schemes used for frequency control of DCOs. Even the reference design without any additional hardening measures already demonstrates excellent tolerance to SEEs.

3. The resistive decoupling scheme using series resistors in each unit cell was confirmed to significantly improve the SEE hardness of the oscillator further, as was expected from the simulations presented in section 4.5.7. This also underlines the validity of the chosen simulation methodology for prediction of oscillator SEE sensitivity.

5.3.4 LC DCO ADPLL

In the second type of ADPLL based on the designed LC DCO, a more varied nature of radiation responses has been observed. The high temporal resolution provided by the utilized instrumentation setup allows clearly separating different types of events and analyzing their origin based on these signatures.

As a first insight into the experimental data, aggregate cross sections based solely on the number of observed events exceeding certain magnitude thresholds are shown in figure 5.21. Among the cuts at different event magnitudes, it can be seen that a large saturation cross section (exceeding $1 \times 10^{-3}\,\mathrm{cm}^2$) exists when events smaller than 200 ps are considered. The cross section reduces sharply for larger magnitude thresholds, implying that larger transients occur much less frequently in practice. This dynamic is illustrated in figure 5.22, where the integrated heavy ion cross section for distinct values of LET is shown as a function of the event magnitude threshold. Here, a pronounced threshold effect is seen for each of the ions with LET at and above $9.9\,\mathrm{MeV\,mg^{-1}\,cm^2}$. The event magnitude at which this threshold is found increases with the heavy ion LET, which suggests that an explanation related to the actual energy deposited appears likely to explain the largest number of circuit responses. Another interesting aspect is the presence of a second class of events with

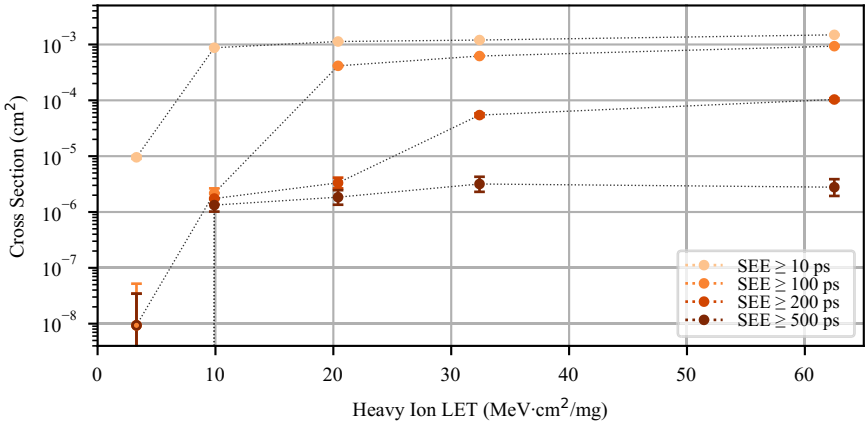


Figure 5.21: Aggregate cross section data obtained with the LC ADPLL. Cross sections for multiple event magnitude cuts are shown. Empty markers signify an absence of detected events. Lines connecting the data points are added only for visual guidance.

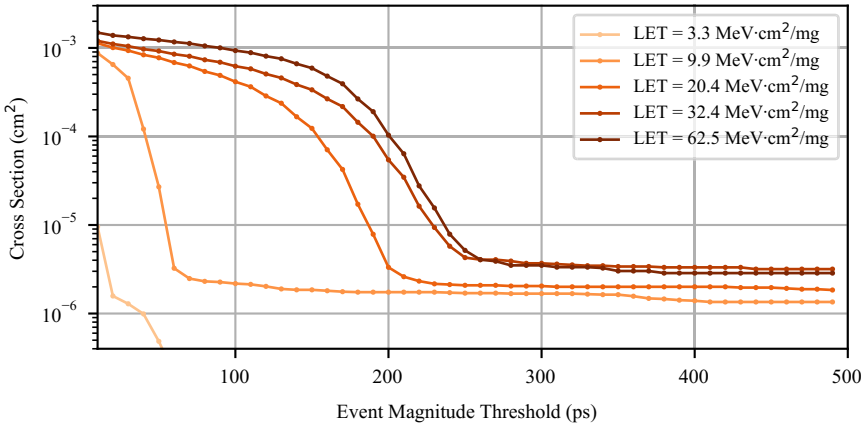


Figure 5.22: LC ADPLL integrated heavy ion cross section as a function of event magnitude threshold. A threshold shift to higher values is observed with larger values of LET.

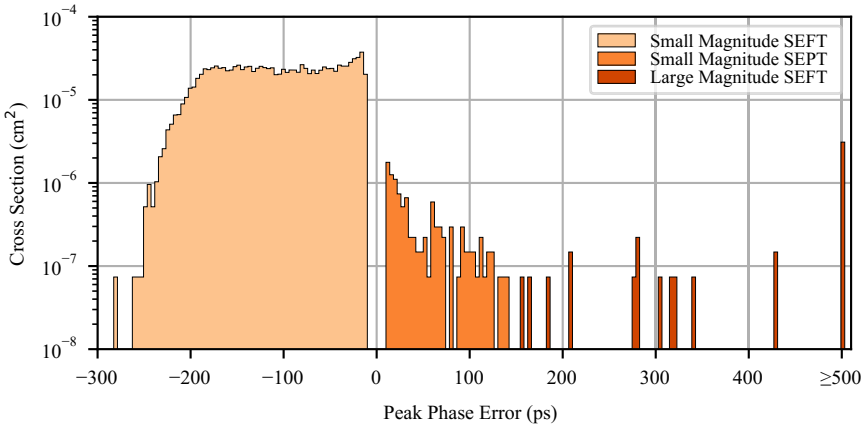


Figure 5.23: Distribution of event magnitudes during irradiation of the LC ADPLL using heavy ions with LET of 32.4 MeV mg^{-1} cm^2. Portions of the magnitude distribution are attributed to the dominating underlying transient event signatures.

magnitudes exceeding 500 ps, with a lower cross section around 3×10^{-5} cm^2. Such large responses are however not observed for the lightest ion with an LET of 3.3 MeV mg^{-1} cm^2.

Finally, figure 5.23 shows the distribution of event magnitudes stimulated by one type of heavy ion in histogram form. Included with this data is a visual classification based on the underlying nature of the PLL transient response responsible for the majority of events in different regions of the histogram. Three relevant event classes were found to emerge from the obtained data, and these are consistently observed across all values of LET. The nature of their underlying sensitivities, including their respective transient response shape and impact on PLL operation will be discussed below. The shown example transients for each of the event classes were obtained at an LET of 32.4 MeV mg^{-1} cm^2.

Small-magnitude SEFT

The first class of events is comprised of small, positive frequency errors. An example of these events is shown in figure 5.24. In these events, a gradual deviation of the phase from its nominal value is observed instead of a sudden discontinuity in the phase, which implies that a frequency error in the oscillator is the responsible mechanism. The oscillator frequency was found to increase with respect to the reference clock frequency during these events. This class of events overwhelmingly dominates the circuit cross section with values exceeding

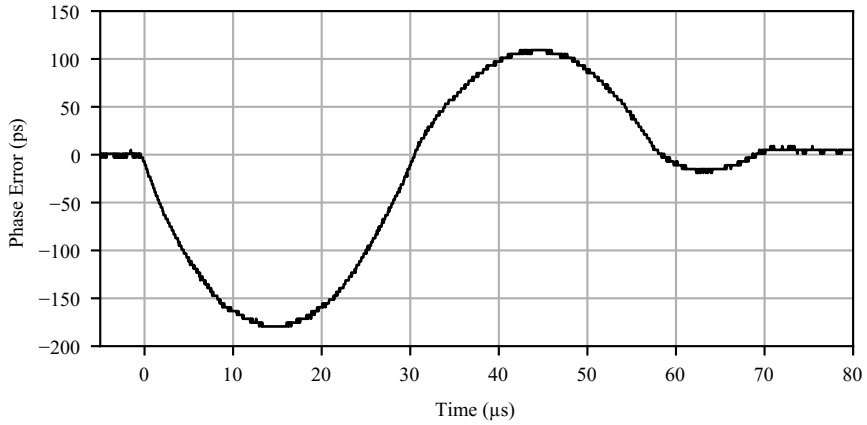


Figure 5.24: Example transient showing a SEFT response of small magnitude in the LC ADPLL.

$1 \times 10^{-3}\,\mathrm{cm}^2$. On the other hand, the magnitude of these events is bounded to approximately 250 ps. The underlying frequency error, which is simulated inside the DCO itself, is found to be at most 25 ppm based on the initial rate of phase error build-up. During similar radiation tests performed on conventional PLL designs, the origin of this effect was identified in the planar on-chip inductor. The nature and mechanism of this sensitivity necessitates a dedicated treatment, also because its impact is not limited to the ADPLL circuit characterized here. For this reason, the discussion of this effect is deferred to chapter 6 of this thesis, where it is discussed in further detail.

Large-magnitude SEFT

The second class of SEE signatures observed exclusively in the LC ADPLL corresponds to larger, but negative DCO frequency errors. The mechanism responsible for the phase errors observed in this class is a temporary reduction of the DCO frequency. An example of observed transients belonging to this class of events is shown in figure 5.25. While these events have a significantly lower saturation cross section (approximately $3 \times 10^{-5}\,\mathrm{cm}^2$) than the inductor-related frequency errors, much larger frequency errors and hence phase errors are stimulated. A wide range of initial frequency errors is observed, ranging from a few tens of ppm to values exceeding 100 ppm for some events. The effect appears to persist on timescales exceeding 20 µs and hence results in the build-up of large amounts of phase error. While the largest observed events exceeded the dynamic range of the used instrumentation, it was possible to

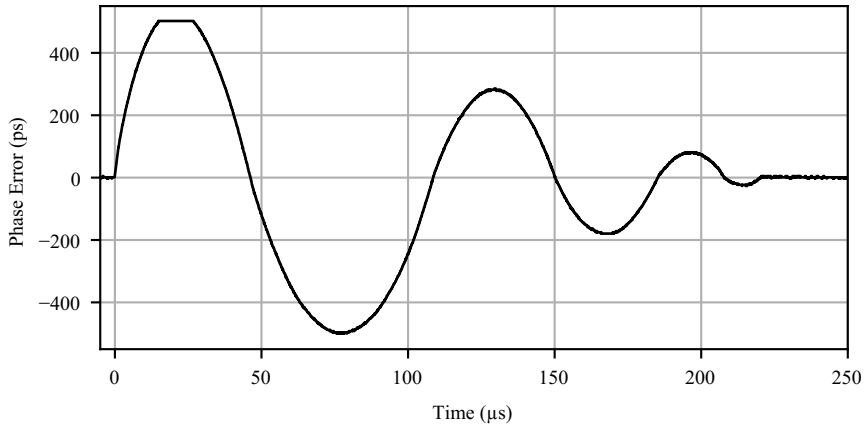


Figure 5.25: Example transient showing a large-magnitude SEFT response of the LC ADPLL. The transient temporarily exceeds the measurement range at $t = 25\,\mu s$.

place bounds on the worst case phase error stimulated. This was done using a parabolic curve fit to the phase error measured within the linear region of the used measurement system. Using this method, the largest phase excursions were estimated to remain below 5 ns. Consequently, larger event durations are observed for these events, with re-acquisition times approaching one millisecond for the largest transients.

The origin of this sensitivity was identified in the bottom-pinning biasing scheme used for the PVT and acquisition banks (see figure 4.4). While the turn-on time of switches M_{SW} and M_{PD} is in the order of one DCO oscillation period, establishing the bottom-pinning bias condition via M_{PIN} was found to require a long settling time, in line with the observed SEE response characteristics. For cells that are disabled during the irradiation, SETs affecting the enable input can temporarily turn on M_{SW} and M_{PD}, which disturbs the established bias condition by swiftly pulling V_A and V_B to ground. While the biasing condition is re-established following this event, the DCO frequency remains temporarily reduced, which results in an accumulation of phase errors in the loop. The sensitivity could be fully reproduced using charge injection SPICE simulations, both in terms of magnitude of the frequency error as well as in its duration. Even though a small number of these events at the highest experimental LET resulted in phase excursions up to 5 ns, no cycle slips of the PLL have been observed during operating with a 40 MHz reference clock frequency. Such high LET events are very unlikely to occur in the radiation environments of the LHC

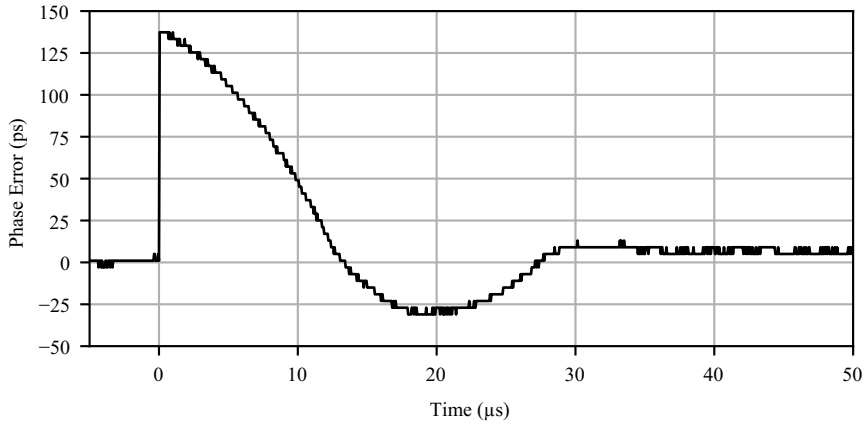


Figure 5.26: Example transient of the small-magnitude SEPT responses observed in the LC ADPLL.

[9]. Nonetheless, this class of SEE can and should be mitigated, for example using a different capacitor switch implementation, such as the one proposed in [90].

Small-magnitude SEPT

The third and final class of events observed in the LC ADPLL consists of small instantaneous phase jumps up to about 200 picoseconds in magnitude. An example transient observed within this class is shown in figure 5.26. Similar to the corresponding class of events in the DCRO ADPLLs, the loop was found to quickly recover from these events without significant overshoot. Since the events appeared to be purely impacting the phase without an associated change of the frequency, these responses are most likely caused by charge collection in either the cross-coupled pair of the oscillator or in the tail current source transistor. This is also evidenced by them never exceeding the DCO oscillation period of 390 ps, making an explanation in any downstream divider an unlikely cause. The saturation cross-section of these events was found to be somewhat below $1 \times 10^{-5}\,\mathrm{cm}^2$, which is compatible with the total area of these devices. An appropriate mitigation strategy for this sensitivity could be the addition of a decoupling network to the drain node of the tail current source transistor [117]. This measure was implemented for the VCO presented in [39], in which no similar radiation signature was observed.

5.3.5 Summary

All three manufactured ADPLL designs were tested for the presence of single-event effect sensitivities using heavy ion irradiation. The chosen DCRO architecture was shown to provide outstanding radiation tolerance, by leveraging the unit-cell-based nature of the circuit. The additionally proposed resistive decoupling approach was shown to further increase radiation tolerance significantly. The high radiation immunity of the ring oscillator ADPLLs also allowed concluding that the digital PLL core components are free from SEE sensitivities. No SEE responses could be identified that originated in the digital loop components (DLF, $\Sigma\Delta$M, feedback divider), highlighting the merits and effectiveness of the systematic SEE hardening methodology applied. Based on this conclusion, the sensitivities observed in the LC ADPLL could all be reliably attributed to components in the LC DCO itself. A sensitivity with concerning magnitude identified in this oscillator could be fully replicated through simulations. An architectural mitigation for this sensitivity was proposed and the obtained findings can be used to improve the radiation tolerance of future iterations of LC DCOs. The experiences gathered during the irradiation experiments provide very high confidence that ADPLL architectures will be able to provide the same or higher levels of SEE hardness than their conventional counterparts in current and future CMOS technology nodes.

One architectural concern can however be identified from the exclusive use of a BBPD. While the lack of phase error magnitude information was found not to limit the jitter performance of the clock generator during steady-state operation, it gives this architecture a disadvantage in presence of SEE in the DCO. The fixed and limited gain of the integral and proportional filter paths increases the recovery time from single-event effects that originate in the DCO, since no control action proportional to the stimulated phase error can be provided. This leads to the accumulation of large phase errors, in particular for SEFT, from which long periods of slewing result. Two natural architectural mitigation strategies could be used to improve the SEE performance further. One solution might be the adoption of gear shifting, temporarily increasing the loop gain when such slewing conditions are detected. Another promising option is the augmentation of the PLL by a coarse TDC with limited dynamic range and power consumption, which could detect SEE-related excursions of the phase and provide an appropriate proportional control response. Both these approaches present attractive extensions of this work in the future.

5.4 Total Ionizing Dose Testing

For the characterization of its TID tolerance, the circuit was irradiated at the CERN X-ray irradiation facility [118]. The test chip bonded to the carrier PCB was thermally connected to a temperature controlled base plate, which allows regulation to a temperature of −10 °C. This temperature is in the range of typical temperatures adopted for future detectors in the harsh radiation environments of the High Luminosity Large Hadron Collider (HL-LHC) and is therefore expected to give a representative estimate of TID tolerance. A dose rate of 8.94 Mrad h^{-1} was used to accumulate a dose of 1.5 Grad over 168 h. The circuit was kept under bias permanently while repeatedly undergoing a characterization measurement routine. In order to validate the tolerance of the ADPLL circuits and their associated DCOs, all tests were performed across a 1.2 V±10 % supply voltage range. As in all preceding tests, the I^2C slow control interface was used for configuration of the ASIC.

The automated test routine was separated into two phases, which can be summarized as *open loop* and *closed loop* tests. During the *open loop* phase, oscillator parameters such as tuning range, linearity, step size and power consumption were characterized, while the *closed loop* test phase was used to confirm whether the acquisition process can be completed as expected and that the circuits correctly obtain phase lock across the full range of specified supply voltages.

5.4.1 Open Loop Performance

Digitally Controlled Ring Oscillators

The oscillation frequency of both designs was monitored. Figure 5.27 shows that, the degradation behavior of both oscillators is very similar. The oscillation frequency degrades with a slope of approximately 1.5 %/100Mrad, which allowed the proposed oscillator design to operate at its design frequency of 1.28 GHz over a 10 % supply voltage range up to 1.5 Grad. Since the oscillation frequency of the proposed RDUC DCRO is determined by the series combination of the MOS channel resistance and the added series resistance R_S, which does not suffer from TID degradation, this design showed a slightly reduced rate of frequency reduction. The initial increase in oscillation frequency by about 5 % is explained by a temporary enhancement of the $I_{d,max}$ of NMOS transistors in the chosen technology [88]. The NMOS threshold voltage is slightly reduced by the fast build-up of oxide-trapped charge, which is compensated by slower interface trap buildup at higher doses [119]. A total dose of 1.5 Grad is the highest reported total dose tolerance a ring oscillator achieves in the current state-of-the-art.

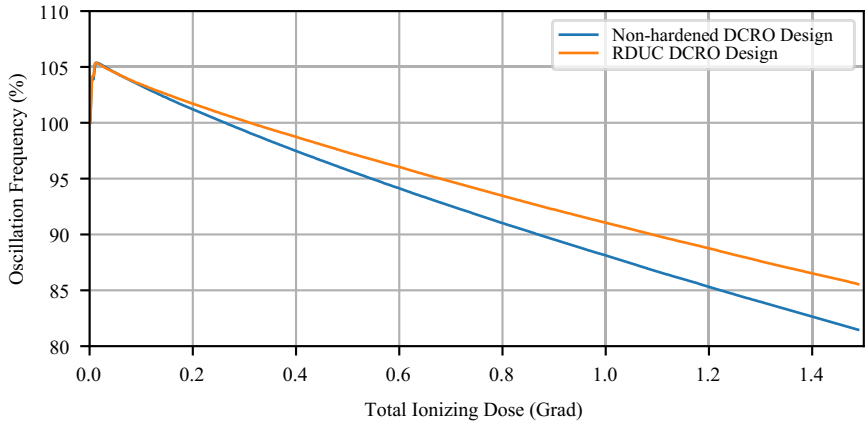


Figure 5.27: Evolution of the DCRO frequency for both manufactured designs during X-ray irradiation. Similar degradation behaviour of both oscillators was observed.

LC DCO

During the irradiation, a consistent increase in the free-running frequency of the LC DCO was observed across all supply voltage and tuning control word settings. The evolution of the oscillation frequency at three different frequency settings is shown in figure 5.28. The worst observed frequency shift remained within 0.8 %, which is small compared to the total tuning range available (20 %). This shift is a result of a change in common mode voltage and oscillation amplitude caused by the radiation-induced reduction in transconductance in the oscillator active devices [46]. Comparing this DCO design to the VCO design adopted in [39], the radiation-induced frequency shift can be found to be significantly reduced. As outlined in section 4.4, the MOS varactors used in VCO designs tend to show a strong amplitude dependence, while the majority of capacitance in this DCO design is contributed by MOM capacitances. The dominant nonlinear capacitance loading the tank in this design is the much smaller junction capacitances of the capacitor bank switches, which explains the reduction in sensitivity. This finding highlights the advantage of a varactorless DCO implementation over VCOs in terms of TID tolerance. Characterization of the digital tuning cells performed during the irradiation did not show any failure of individual cells, nor a degradation of the tuning step size or linearity.

During the irradiation period, the power dissipation of the power domain supplying the LC DCO was found to gradually reduce by about 15% at its nominal design frequency. This reduction is explained by a reduction in transcon-

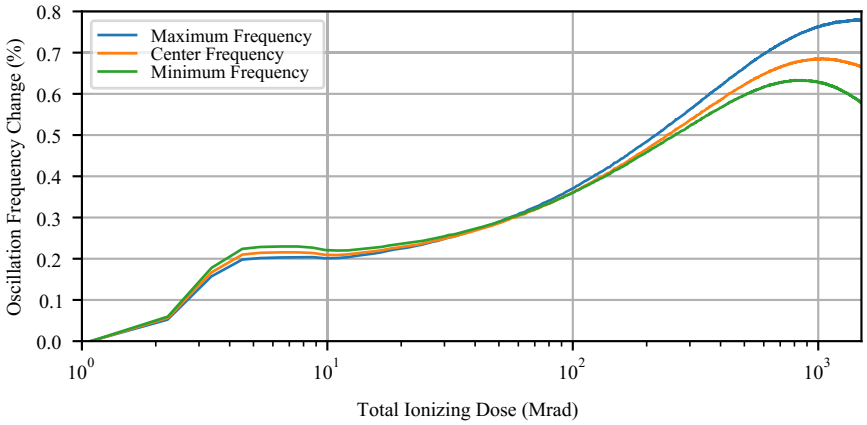


Figure 5.28: Evolution of LC DCO frequency during X-ray irradiation. A consistent frequency increase relative to the pre-irradiation value is seen for different frequency settings of the oscillator.

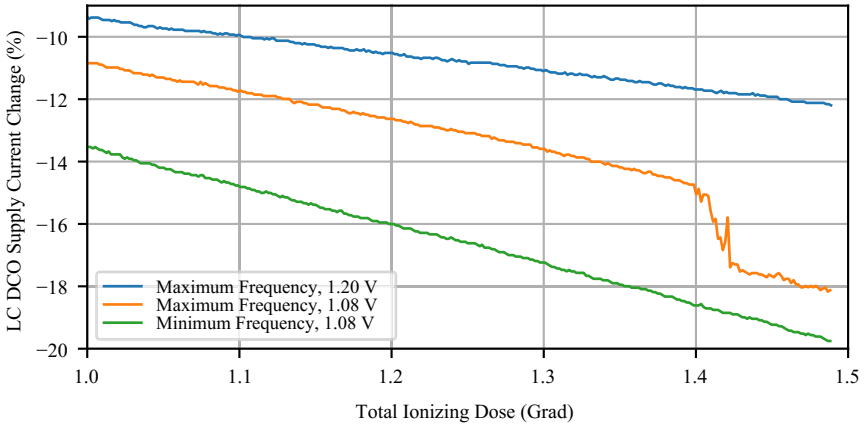


Figure 5.29: Evolution of LC DCO supply domain current during X-ray irradiation for different supply voltage and oscillator frequency settings.

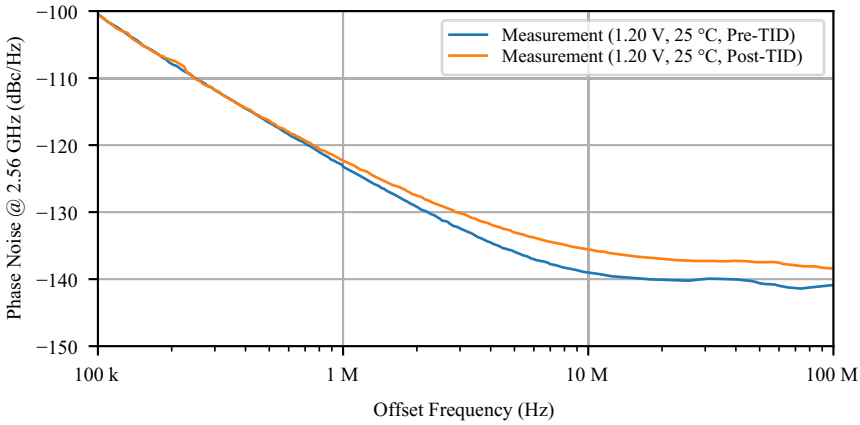


Figure 5.30: LC DCO phase noise measurements before and after X-ray irradiation.

ductance and drain current capability of the active devices in the oscillator [46]. The DCO nonetheless continued operating normally within its complete supply voltage and tuning range up to a dose of 1.4 Grad. At this dose, a discernible drop of current consumption in the power domain supplying the DCO and divide-by-two prescaler was observed. This reduction was observed only at the highest DCO frequency setting at the lower end of the specified supply voltage range. The relevant evolution of the current consumption of this power domain is shown in figure 5.29. As the oscillation of the DCO did not cease at any point and the PLL was still fully operational at that dose, such a behavior can only be explained by a failure of one of the TMR branches of the divide-by-two prescaler. The observation is consistent with the expectation that this circuit would first begin to fail for a combination of low supply voltage and high input frequency.

Finally, figure 5.30 compares the open loop phase noise performance of the oscillator at nominal operating conditions before and after the 1.5 Grad irradiation. A pronounced degradation is observed at offset frequencies above 1 MHz as an increase of the phase noise floor. Since the wide-band noise floor was dominated by the clock distribution network as opposed to the oscillator itself, its increase is most likely also dominated by the degradation of slew rates and an associated increase in jitter added within the clock distribution network.

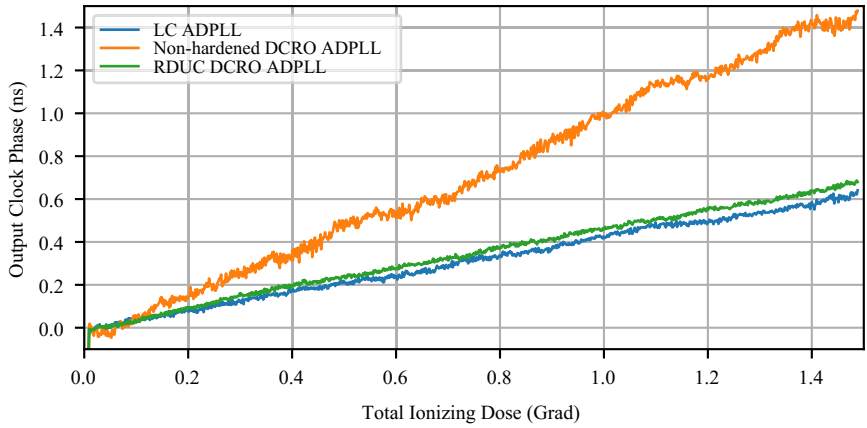


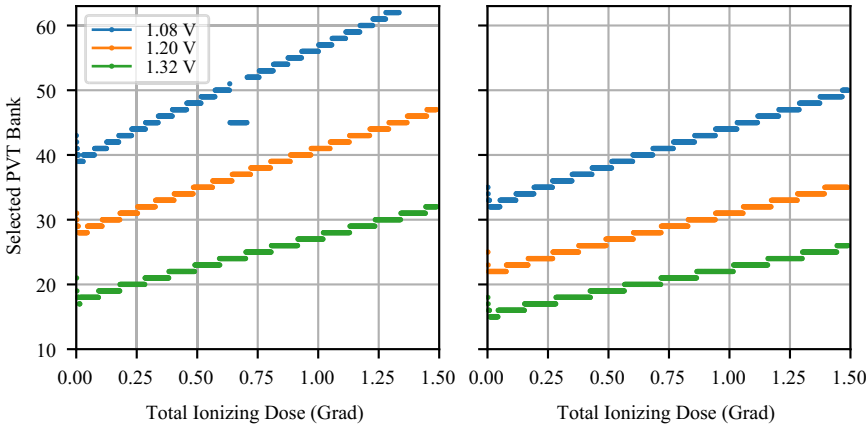
Figure 5.31: Evolution of the output clock phase for all three irradiated PLL circuits.

5.4.2 Closed Loop Performance

Both types of PLL were successfully operated in closed loop during the irradiation process. The evolution of output clock signal phase over the duration of irradiation is shown in figure 5.31, in which each data point is obtained following a 'cold start' of the PLL circuits. This data illustrates that all PLLs are able to provide repeatable phase delay, which only changes slowly as a result of drift of on-chip clock distribution delays. The approximately twice larger slope for one of the PLLs is explained by its location in the center of the test chip, which necessitated the implementation of additional buffering on the reference and clock output paths. The absence of any notable discontinuities confirms that the PLLs operated reliably and were able to unambiguously obtain lock during the irradiation. Two minor failure modes specific to particular characteristics of each of the the oscillator circuits were observed and will be discussed below together with the performance of the individual ADPLLs.

DCRO ADPLLs

Both PLL circuits using ring oscillators were able to successfully track the significant degradation of their oscillation frequency. Figure 5.32 shows the evolution of the selected PVT bank at different supply voltage settings across the irradiation. The selected bank can be seen to increase linearly. It is worth noting that the change observed across TID is essentially as large as the change across supply voltage, further underlines the usefulness of the large linear tuning



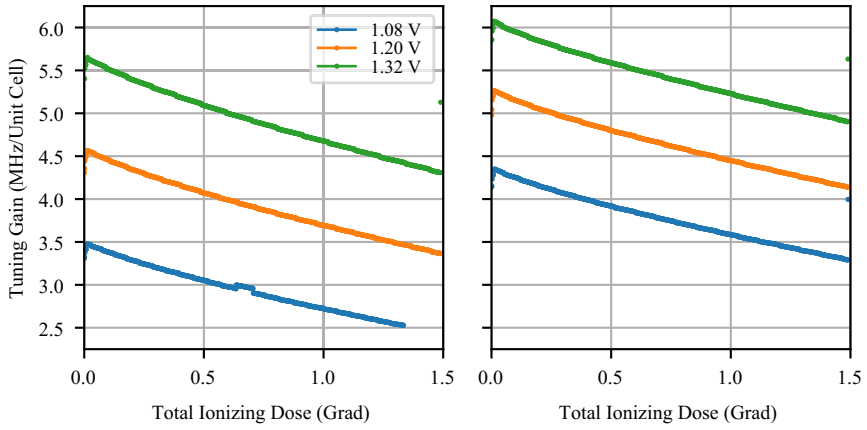
(a) Non-hardened DCRO.

(b) RDUC DCRO.

Figure 5.32: Evolution of the PVT bank selection result for both DCRO ADPLL circuits. A linear increase in the selected bank is seen to compensate for device degradation.

range achieved with this DCRO architecture. Since the non-hardened DCRO flavor had a slightly lower initial center frequency, the TID-induced degradation could not be fully compensated anymore at a dose exceeding 1.3 Grad for the lowest supply voltage, at which point this PLL failed to acquire lock. The discontinuity seen in the data for this oscillator at the lowest supply voltage was the result of a logic error introduced by software modification performed during the irradiation, which was subsequently reverted. It therefore is not indicative of a failure behavior of the DCRO or the acquisition process. Closed loop operation with the RDUC DCRO continued correctly across all supply voltage points until the irradiation was concluded.

Even though the evolution of the loop dynamics was not directly monitored during the irradiation, this aspect can be discussed based on the repeatedly performed oscillator characterization measurements. Figure 5.33 shows the observed evolution of the oscillator tuning gain as a function of TID. This data shows the tuning gain at the selected PVT bank which is closest to the target oscillator frequency. The observed changes across dose are comparable with their differences across the specified supply voltage range. Therefore, changes in the loop dynamics arising over TID from this mechanism can be expected to be similar in magnitude to the data shown in section 5.2.6. As the loop gain is otherwise determined primarily by the digital loop filter, whose coefficients and gain are insensitive to TID, the dynamic behavior of the PLL can be



(a) Non-hardened DCRO.

(b) RDUC DCRO.

Figure 5.33: Evolution of the DCRO tuning gain effective during closed loop operation across the irradiation process.

concluded to be largely unaffected by irradiation. No failures of the DLF, $\Sigma\Delta$M and divide-by-32 feedback divider circuits were observed during the irradiation procedure, implying that the chosen synthesis strategy was adequate to achieve high radiation tolerance in all critical digital components.

LC ADPLL

For the LC ADPLL circuit, similar conclusions can be drawn. Due to the close similarity of all digital loop components shared among both types of PLL, this variant was also able to withstand large amounts of TID and no failures in its digital components were observed. As a result of the very small change in center frequency of the DCO compared to its total tuning range, the frequency acquisition procedure was able to reliably obtain phase lock across the total dose range of the experiment. The evolution of the PVT and acquisition bank selection process during frequency acquisition can be seen in figure 5.34.

Since the DCO frequency is rather insensitive to both supply voltage and TID effects, only three PVT bank settings are required to track the combined change. A jump of approximately 20 acquisition cells is observed whenever the corresponding PVT bank value changes, which is in accordance with the relative sizing performed for these two banks. No locking failures have been observed during the test procedure. The PVT and acquisition banks were able to compensate for the oscillator frequency shift according to expectations and

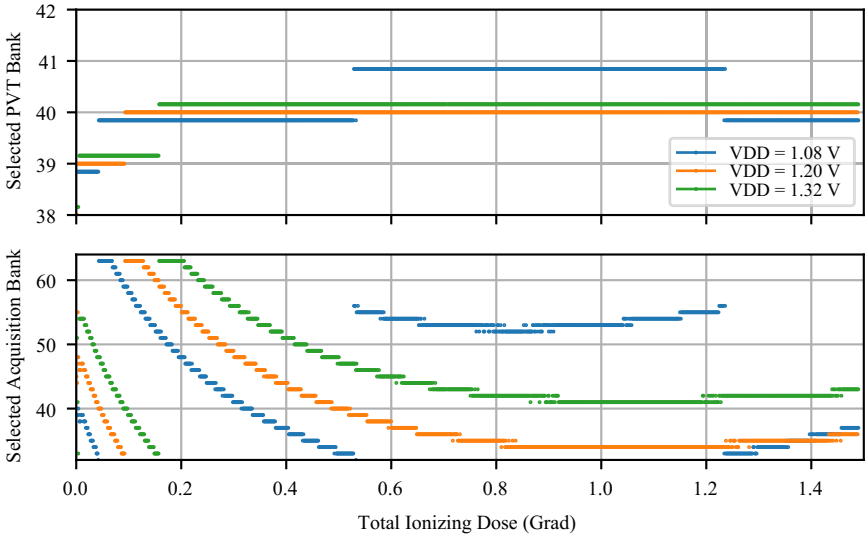


Figure 5.34: Evolution of the selected PVT and acquisition bank for the LC ADPLL circuit during the irradiation. PVT bank data for different supply voltages are vertically staggered for visual clarity.

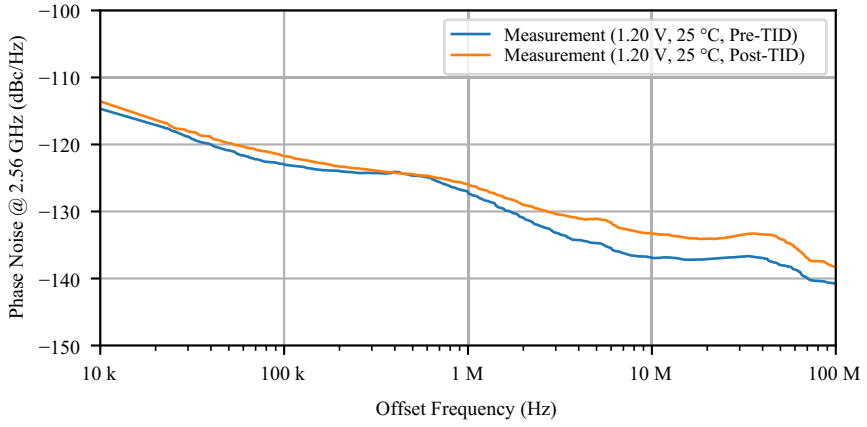


Figure 5.35: Closed loop phase noise of the LC ADPLL using identical configurations before and after the X-ray irradiation process.

the output clock delay with respect to the reference clock remained repeatable across the irradiation.

For the LC ADPLL, the closed loop phase noise before and after the irradiation procedure was measured additionally and the results are shown in figure 5.35. The observed changes are in agreement with the changes in open loop DCO phase noise as the most significant degradation manifests as an increase in phase noise floor. The integrated jitter of the output signal integrated from 100 Hz to 100 MHz increased from 530 fs to 730 fs, and hence remains in the sub-picosecond range, which constitutes only a minor overall degradation.

5.4.3 Summary

Both flavors of ADPLL were shown to provide very high tolerance to TID, and a state-of-the-art radiation tolerance exceeding 1 Grad was demonstrated for all tested circuits. The design methodology adopted for the different circuit components was found to be adequate to achieve these properties. For the LC oscillator, the elimination of varactors has significantly reduced the amount of frequency shift the oscillator experiences with increasing dose. For the ring oscillators, choosing instead an architecture with a large inherent tuning range and good tuning linearity enabled sustained closed-loop operation even at high levels of degradation. Finally, for the digital circuit components, an implementation methodology based on conservative setup and hold margins allowed sustained operation in spite of the high TID levels. It was confirmed that a digital implementation of most of the components dictating the loop transfer function largely decouples their performance from any TID-induced degradation. The variation of loop dynamics over TID is now dominated by relatively minor changes in the DCO tuning gain, in particular for the DCRO flavors.

Chapter 6

Single-Event Effect Responses in Integrated Planar Inductors

This chapter is concerned with experimental investigations into a previously unknown SEE radiation response originating in planar on-chip inductors, which represent a key component used in the design of LC-tank oscillators. *Parts of the material in this chapter have been published in [120].*

6.1 Circuit Description

The measurements described in this chapter have been performed on a radiation-tolerant Integer-N PLL, which was previously presented in [62]. The VCO used in this circuit operates at 5.12 GHz and is locked to a reference clock of 40 MHz during closed loop operation. The LC tank is composed of a 930 pH inductor and 1.04 pF capacitor. It is tuned using MOS varactors (in a radiation hardened configuration [121]), achieving a tuning sensitivity of 500 MHz V^{-1}. More details of the VCO implementation can be found in [39], which utilizes the same VCO as part of a CDR circuit and expands further on the circuit level SEE mitigation techniques implemented, especially with respect to the tuning topology. The loop filter includes a filter capacitor of 56 pF. All digital circuit components (such as the Phase-Frequency-Detector and Feedback Divider) are protected against SEEs using TMR. The analog blocks (CP, LF, VCO) are designed using state-of-the-art radiation hardening techniques, including appropriate sizing and enclosed layout transistors to mitigate SEE and TID effects. A photomicrograph of the complete circuit is shown in figure 6.1.

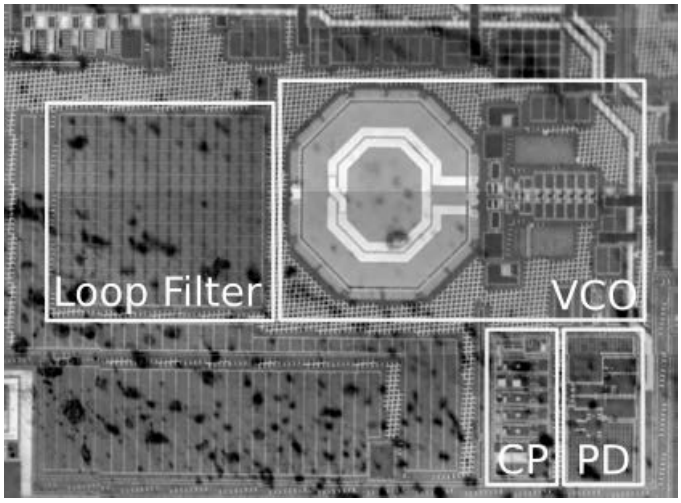


Figure 6.1: Photomicrograph of the PLL/CDR circuit used during irradiation experiments.

The circuit is designed and manufactured in a commercial 65 nm bulk CMOS technology with six metal layers. The two-turn spiral inductor, which will remain the focus of the following discussions, is implemented in the ultra thick top metal layer, plus an underpass at a thick metal level just below. The copper metallization used for the inductor has a thickness of 3.5 µm and a width of 12 µm. The conductor is suspended on inter-level dielectrics at a height of about 4 µm above the silicon substrate. The two turns of the inductor are separated horizontally by a 3 µm gap, which is also filled with an insulating dielectric material. While the lower, thin metal layers in this process utilize low-κ dielectric materials to minimize interconnect parasitics, the upper level metals (which also make up for the majority of vertical geometrical extent in the structure) most likely utilize silicon dioxide (SiO_2) deposited using chemical vapor deposition (CVD) methods. The inductor area is surrounded by a foundry-provided guard ring structure, which minimizes electrical coupling to adjacent structures and improves substrate noise isolation.

Two different versions of the inductor are used in the experiments described below: The version henceforth referred to as 'Inductor A' does not include any additional metal features in the area covered by the inductor, which implies the inductor metal is separated from the silicon substrate only by dielectric layers. A modified version uses the same inductor geometry, but includes a symmetrical patterned ground shield (PGS) on the lowest metal level just above the substrate. This ground shield is connected locally to the guard ring structure as well as

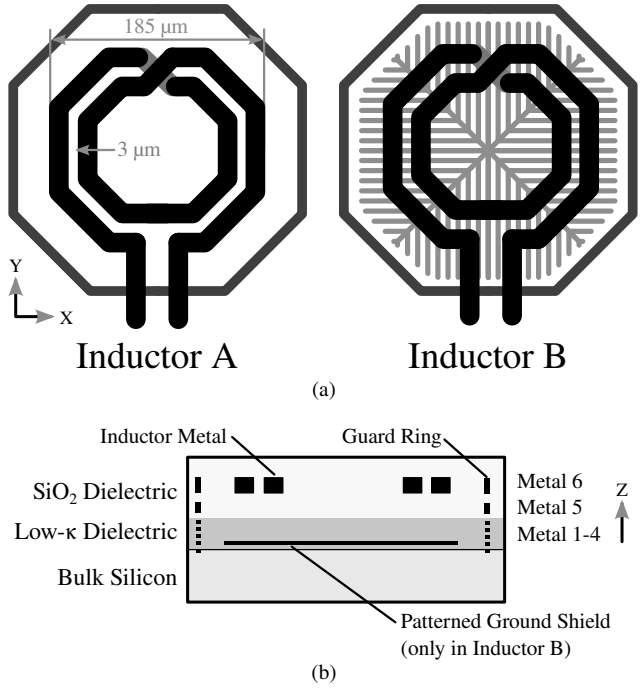


Figure 6.2: (a) Comparison of inductor geometries utilized in tests. In 'Inductor A', the conductor is placed directly above the silicon substrate. In 'Inductor B', a patterned metal ground shield is included on the lowest metal layer above the silicon substrate. (b) Cross section of the sample technology (not to scale).

the ground potential of the VCO circuit. The metal ground shield was included to reduce electrical coupling between the substrate and the inductor, while at the same time not influencing the relevant electrical parameters (inductance and quality factor at the operating frequency) of the inductor itself [122]. This second version is referred to as 'Inductor B' in the remainder of this chapter. Both versions of the inductor geometry are shown side-by-side in figure 6.2, together with an approximate cross section of the geometry.

6.1.1 Discovery of the Radiation Response

Even though the circuit described above includes many circuit-level mitigation measures for known SEE vulnerabilities, an unexpected radiation sensitivity was identified during a heavy ion irradiation test. During this test campaign, the PLL circuit was observed to produce detectable phase deviations from its baseline value, on the order of 200 ps to 300 ps. Since the FPGA-based phase measurement system described in section 3.3 was used during this test, a measurement resolution of only about 100 ps was available. Therefore, only the frequency of occurrence of these events could be reliably characterized and little information about the transient properties of the responses could be obtained.

A heavy ion cross section exceeding $1 \times 10^{-4}\,\mathrm{cm}^2$ for transient phase errors of the PLL circuit was estimated for excursions larger than 200 ps. Since this value is about two orders of magnitude larger than what was expected in terms of sensitive circuit area from previous experiments on similar circuits, further experiments were conducted to identify the origin of this sensitivity.

6.2 Heavy Ion Microbeam Irradiation Experiment

Following the first observation of the radiation response from the described circuit, no single circuit component offered an adequate explanation: The large heavy ion cross section requires the presence of a very large sensitive geometrical area of at least the same order of magnitude on the chip. The broadbeam nature of the used heavy ion facility did not provide any spatial information that could enable localization of this sensitive area. Additionally, the homogeneity of the observed responses made an explanation involving multiple different circuit components unlikely, since these would be more likely to result in a number of different event signatures. While any hypotheses including passive circuit components were considered improbable at this time, only the large on-chip loop filter capacitor and planar inductor approached the geometrical area required from an individual circuit component (compare figure 6.1). To conclusively attribute the circuit radiation response to its corresponding geometrical on-chip

Figure 6.3: PLL circuit sample mounted in the GSI Microbeam facility.

area and therefore identify the responsible circuit element, an experiment at a heavy ion microbeam facility was carried out.

6.2.1 Methodology

Selective irradiation of the circuit was performed using the GSI Heavy Ion Microbeam facility [123]. In contrast to broadbeam irradiation facilities, this facility offers precise positioning capabilities for a heavy ion beam with a full width half maximum (FWHM) of less than 1 µm. Conceptually, the ion beam is scanned across the circuit under test, while a data acquisition system is provided with a trigger signal whenever an SEE response of the circuit is detected by external instrumentation. In this way, a sensitivity map of the circuit under test can be created, which is then overlaid on a photomicrograph.

Using this facility, irradiation was performed with $^{40}Ar^{10+}$ ions ($LET_{Si} = 10.8\,MeV\,mg^{-1}\,cm^2$, range exceeding 100 µm in silicon), sufficient to stimulate the responses observed during the qualification campaign. Figure 6.3 shows the circuit sample mounted in the accelerator beam line. The facility accelerator operates at a fixed bunch frequency of 12.5 Hz and a particle rate of approximately 70 Hz after collimation was achieved. The circuit was scanned in a line-wise fashion at a speed of approximately 1 line/s for regions of interest spanning about 100 µm to 500 µm in each direction. Scans of the same area were performed multiple times in order to obtain a meaningful number of events for the sensitive regions. Particular care was taken to validate the

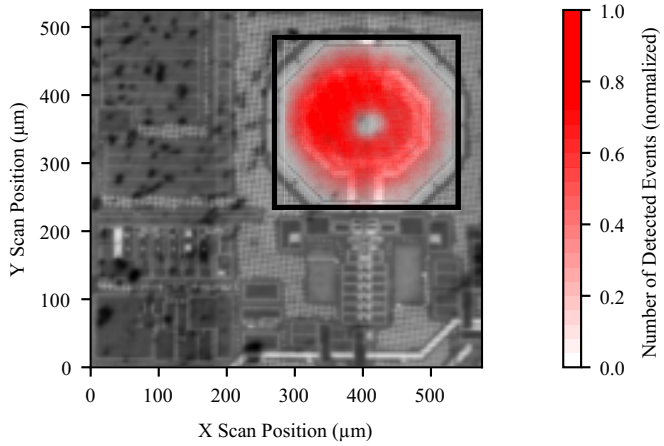


Figure 6.4: Circuit sensitivity map obtained using microbeam irradiation. Color intensity encodes the number of detected responses under irradiation over multiple consecutive raster scans. The rectangular border delimits the scan extent chosen to obtain this data.

relative positioning of the ion beam and the photomicrograph to within 10 µm. A dedicated SEU test structure on the same die placed at a known location relative to the PLL circuit was used for this purpose. The circuit used in this test implements 'Inductor A', which does not include a PGS. Since the device is flip-chip mounted to a carrier board, the sample was irradiated from the back side, i.e. with the particle beam incident on the bulk silicon. To reduce energy loss in the bulk silicon and allow the impinging ions to traverse any potentially sensitive geometry, the substrate was thinned from its original thickness of 250 µm down to 60 µm by grinding and polishing.

During this test, the PLL circuit was operated in closed loop mode locked to a low jitter reference clock. A trigger signal was generated whenever the output clock phase of the PLL deviated from its baseline value by more than 200 ps using the instrumentation setup described in section 3.3. The discriminator threshold was manually trimmed by means of a fine phase adjustment to maximize the detection sensitivity while rejecting events caused by noise. Even though the trigger threshold of this system is nominally 200 ps, its precise value is subject to an uncertainty of ±50 ps (0.5 LSB).

6.2.2 Experimental Results

The complete area of the PLL has been scanned using the heavy ion microbeam. None of the areas containing active devices revealed a sensitivity of the expected

size. While the performed scans initially focused on the on-chip loop filter capacitor, no sensitivity could be identified in this area. A large sensitivity was instead identified in the area occupied by the VCO's main spiral inductor. A detailed scan of only this area has been performed and the number of detected SEE responses from the circuit stored as a function of the beam position during the scan. The resulting sensitivity map of this process is shown in figure 6.4. This visualization clearly highlights an approximately circular sensitive shape concentric with the inductor spiral. The largest sensitivity appears in the vicinity of the wires forming the two inductor turns. In the center of the inductor, the sensitivity appears reduced. The sensitive area highlighted in figure 6.4 was found to be approximately $4 \times 10^{-4}\,\mathrm{cm}^2$. This sensitive area explained solely by a sensitivity in the spiral inductor structure aligns well with the cross section the initial qualification campaign of the circuit had identified.

6.2.3 Discussion

Since the nature of the sensitive geometry was unknown before the test, not all aspects of this campaign could be fully anticipated. While the performed tests provided conclusive evidence concerning the circuit component responsible for the observed sensitivity, the obtained data is affected by a number of issues that complicate further quantitative analysis. A number of these issues are discussed below.

Contribution of Pile-Up

A particularity of the microbeam facility is the operation at a low bunch frequency of 12.5 Hz. While the collimation used to achieve the small beam width reduces the rate of particles on the tested sample significantly, around 70 ions arrive at the sample surface per second. This means that each bunch delivers about five ions to a given position of the microbeam. Since a nominal bunch length of approximately 3 ms were used and single ion counting was not implemented for this experiment, a clear separation of responses from multiple ions could not be guaranteed. As a result, some of the circuit responses used for figure 6.4 are the result of multiple simultaneous ion hits. Since no quantitative information about pulse height or transient duration was obtained however, the only impact in this experiment is an increase of the detection sensitivity.

Microbeam Scan Artifacts

A second issue affecting the data shown in figure 6.4 is the approach adopted for scanning the circuit area. The circuit is scanned in a line-wise fashion at a low speed of approximately one line per second. The facility accelerator operates independently of this scan frequency at a bunch frequency of 12.5 Hz. The

bunched irradiation therefore constitutes a spatial sampling process, and not all positions along the scan lines are covered with equal density. Since the line frequency and the accelerator bunch frequency are not relative multiples, artifacts such as diagonal lines of increased or reduced sensitivity appear in the resulting sensitivity maps. These artifacts change when modifying the scan frequency, which complicates comparisons of measurements obtained with different scan rates and beam deflections. One feature affected by this issue is the 'hole' in the center of the inductor geometry, which did not show the same reduction of sensitivity in all the scans performed. To mitigate scanning artifacts, the collected data is re-binned or low-pass filtered. This process sacrifices resolution and may distort the shape of sensitive area depending on the chosen bin width or filter kernel. As a consequence of these limitations, no attempts were made to extract quantitative information other than the location and area of the sensitive circuit component from the sensitivity map.

6.3 Two-Photon Absorption Laser Irradiation Experiment

Another, more readily available facility offering high spatial resolution irradiation useful for semiconductor testing purposes are two-photon absorption (TPA) laser irradiation facilities [124]. A TPA irradiation of the circuit was performed as a complementary technique to the microbeam experiment. Conceptually, the energy of a single photon at wavelengths used in these tests is below the energy band gap of silicon. Electron-hole pairs in the bulk silicon substrate of semiconductors can be generated only through nonlinear absorption of two coincident photons in the interaction region of a focused laser beam. Since this interaction region is small in both the horizontal and vertical directions, 3D mapping of sensitive regions can be performed with this technique.

6.3.1 Methodology

A PULSCAN PULSYS irradiation system using a 540 fs pulse laser operating at a wavelength of 1550 nm was used. The laser was operated with a 1 kHz pulse repetition rate and pulse energies up to 3 nJ have been used. During the tests, the PLL circuit operated in closed loop, i.e. phase-locked to a low-jitter 40 MHz reference clock.

The circuit samples used in the Microbeam facility (containing 'Inductor A' without a PGS) were reused in this test, which was carried out at the ADVISE RELYlab of KU Leuven. Irradiation was performed through thinned silicon dies from the back side of the circuit. Different areas of the PLL circuit were scanned in a raster-like fashion with programmable speeds, depending on the chosen

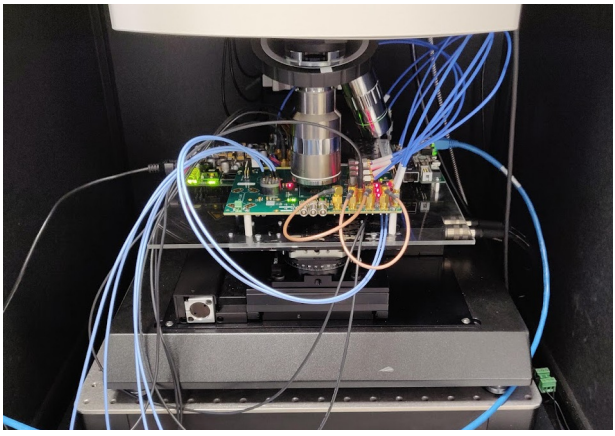


Figure 6.5: PLL circuit sample installed in the PULSCAN TPA laser test system.

pulse repetition rate. A network interface was used to signal the presence of a SEE response to the DAQ system for a given position, which allows creating similar sensitivity maps as obtained through Microbeam heavy ion irradiation. The system is also equipped with a near-infrared camera system, to which the silicon substrate appears transparent. This means that the circuit's active regions as well as metal layers can be imaged together with the laser interaction region, guaranteeing precise positional alignment. A photograph of the tested sample installed in the laser test setup is shown in figure 6.5. During this test, the digital phase measurement system presented in section 3.5 was utilized and a trigger threshold of 50 ps was used for event detection.

6.3.2 Experimental Results

The sensitive depth (Z position) of the active devices in the PLL circuit has been initially established by irradiating active devices connected to a sensitive node with very small area (approximately 1 µm^2) in the PLL charge pump using a pulse energy of 1.5 nJ. Following this setup procedure, selective irradiation of the area occupied by the inductor was performed. The Z position of the laser was scanned at least 10 µm in each direction to account for the possibility of different sensitive depths throughout the geometry, for example as a consequence of insufficient alignment or planarity of the sample. Even though these scans covered different depths in the substrate and the back-end of line (BEOL) dielectrics, they failed to stimulate any detectable responses from the circuit during irradiation of the inductor area. While the initial setup had been performed with pulse energies of about 1.5 nJ to avoid damaging MOS devices,

the pulse energy was increased to 3 nJ in this area, again without being able to stimulate any responses from the circuit. Nonetheless, the full area of the PLL circuit area was scanned but no sensitive areas of comparable cross-section to the Microbeam test were revealed.

6.3.3 Discussion

One important aspect of laser two-photon absorption tests is their capability to stimulate generation of electron-hole pairs only in the silicon substrate, in which the drain and source regions of active devices reside. The 1.12 eV energy band gap of bulk silicon is below the combined energy of two photons (two times 0.7 eV at a wavelength of 1550 nm), which is why non-linear absorption of two coincident photons can stimulate electron-hole pair (EHP) generation. Dielectric materials on the other hand, posses a significantly larger energy band gap, for example 8.9 eV in SiO_2, such that TPA and associated EHP generation does not occur in these materials at available laser wavelengths.

A further consideration important to the discussion of the results is the localized nature of the laser interaction region in which two-photon absorption can occur. The intersecting laser beams are extremely tightly focused in order to maximize the probability of nonlinear interaction of two photons with the bulk silicon. While the spatial interaction probability follows a continuous distribution, its region of highest intensity is confined to a volume likely smaller than $1\,\mu m^3$.

Both of these aspects differ significantly from a traversing heavy ion, which during its passage leaves behind a dense, long trail of ionized atoms. Since the electronic stopping power of the heavy ion species used in the previous tests is essentially identical in Si and SiO_2, EHP generation occurs not only in the bulk silicon but also in the dielectric layers. The observed absence of any radiation response from the circuit area containing the on-chip inductor under laser irradiation could therefore be plausibly explained by two candidate hypotheses. Either the very localized nature of EHP generation from the TPA process is insufficient to generate detectable responses, or the sensitive area is located within the dielectric layers of the circuit, for example in direct vicinity to the inductor conductors suspended above the substrate within SiO_2. Since the microbeam experiment did not provide further information on the underlying radiation response (in terms of its temporal behavior), which could aid in disproving either of these hypotheses, its discussion will be deferred to section 6.6.

6.4 Heavy Ion Broadbeam Irradiation Experiment

The primary shortcoming of the initial heavy ion broadbeam experiment prohibiting a detailed characterization of the sensitivity was insufficient measurement resolution. This shortcoming was mitigated in anticipation of a further experimental campaign by the development of instrumentation offering adequate resolution. These developments were presented in section 3.4 and section 3.5. Using this improved instrumentation, a broadbeam irradiation experiment was carried out at the Heavy Ion Facility of the Cyclotron Resource Centre in Louvain-la-Neuve, Belgium. The main goal of this experiment was the characterization of the sensitivity in terms of its transient behavior and the magnitude of the stimulated responses, especially as a function of the used Heavy Ion $\mathrm{LET_{Si}}$.

6.4.1 Methodology

The circuit was irradiated using six different ions, ranging in $\mathrm{LET_{Si}}$ from $1.3\,\mathrm{MeV\,mg^{-1}\,cm^2}$ to $62.5\,\mathrm{MeV\,mg^{-1}\,cm^2}$. A flux of $1.5 \times 10^4\,\mathrm{s^{-1}\,cm^{-2}}$ (the maximum offered by the facility) was used and a fluence of $1 \times 10^7\,\mathrm{cm^{-2}}$ was collected for each ion. In order to better understand the influence of the path length of heavy ions through the sensitive geometry, irradiation of each ion was performed at three angles (0°, 35° and 50° measured from the normal of the circuit surface).

For this test, a variant of the PLL circuit containing 'Inductor B' with the previously described PGS was utilized. Since this sample utilized wire-bonding instead of being flip-chip mounted, irradiation was performed from the front side of the sample (i.e. with ions incident on the metallization layers first, before traversing the silicon). As front side irradiation is used, no thinning of the samples was required for this experiment. Since the previous tests had localized the sensitive area of the circuit within the VCO itself, the circuit was operated in two distinct modes of operation during this test, which will be described below.

6.4.2 Closed Loop Phase Measurement Results

Similar to the microbeam and TPA laser tests, closed loop irradiation was first performed, during which the PLL control loop was engaged and the VCO remained phase-locked to an external reference clock. This mode was used to allow characterizing the impact of SEE on in-system performance of the circuit and for comparisons with the other experiments. In this mode of operation, the

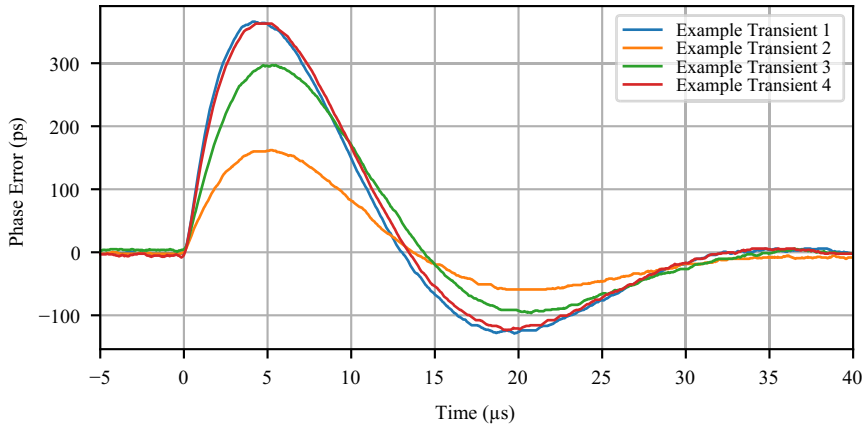


Figure 6.6: Phase transients stimulated by broadbeam irradiation with $^{124}Xe^{35+}$ ions ($LET_{Si} = 62.5\,MeV\,mg^{-1}\,cm^2$). Transients vary in peak amplitude, but are very similar in temporal evolution. After the initial deviation from zero phase error (up to about 5 µs), the transient shape is determined by the active PLL control.

PLL phase error was observed using the transient phase measurement system presented in section 3.4.

Phase deviations of the PLL were again confirmed to be stimulated by heavy ion irradiation of various LET_{Si}. A number of representative examples of these transient responses observed during irradiation with $^{124}Xe^{35+}$ ions ($LET_{Si} = 62.5\,MeV\,mg^{-1}\,cm^2$) are shown in figure 6.6. The shape of the responses reveal that irradiation of the sensitive area primarily results in a deviation of the VCO oscillation frequency (SEFT): Instead of a step-like phase discontinuity (SEPT), this frequency disturbance results in a gradual accumulation of phase error during the first ∼5 µs of the transient response. Subsequently, this accumulated error is corrected by the feedback loop, with the PLL returning to its initial phase value after about 30 µs. This recovery period is entirely dominated by the PLL dynamics and does not necessarily imply the decay of the underlying frequency error stimulated by irradiation. The cross section for the peak phase error exceeding different phase thresholds was calculated from the collected data and is shown in figure 6.7.

Further insight into the dependence of the ion LET_{Si} and angle of incidence can be gained by looking at the distribution of the peak phase error stimulated by irradiation. The resulting distributions for three different ions and three ion incidence angles are shown in figure 6.8. A number of interesting characteristics

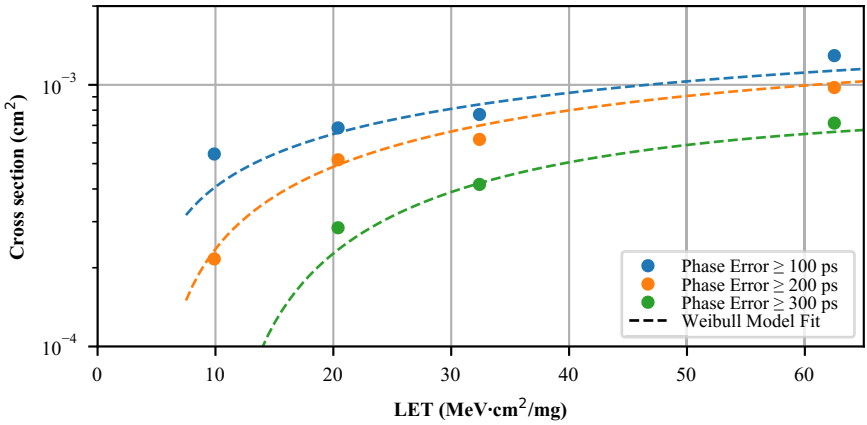


Figure 6.7: Measured cross section during broadbeam heavy ion irradiation for different phase thresholds. Cross sections were obtained by counting the number of events exceeding a given phase excursion threshold for each used ion specimen. The given values are calculated for 0° ion incident angle.

become apparent. Detectable phase excursions ($\geq$50 ps) are stimulated already for low values of $\mathrm{LET_{Si}}$. For higher values of $\mathrm{LET_{Si}}$, the distributions expand towards larger peak values. Another notable feature of the data is the consistent expansion of the distribution towards larger peak values for shallower incident angles of heavy ions. For $\mathrm{LET_{Si}}$ exceeding 30 MeV mg^{-1} cm^2 (not shown in figure 6.8), the peak phase error was found not to significantly increase any further. From the shape of the distributions (which represent the variation of the peak phase error stimulated by each incident ion), it is apparent that the sensitive region does not have either homogeneous or discrete levels of sensitivity, but instead that a continuous range of different phase errors are stimulated.

The responses shown in figure 6.6 also illustrate how the feedback control of the PLL counteracts the buildup of phase error after the oscillator frequency is disturbed by radiation. Since it is however possible that the underlying oscillator frequency errors persist for much longer than the feedback loop response time, the following direct measurements of the oscillator frequency without PLL control feedback become crucial to understand the underlying mechanism.

6.4.3 Open Loop VCO Measurement Results

Additionally, open loop operation of the PLL circuit was performed. In this mode of operation, the feedback control was disabled and the VCO tuning voltage was tied to a fixed voltage in the middle of its tuning range. This mode

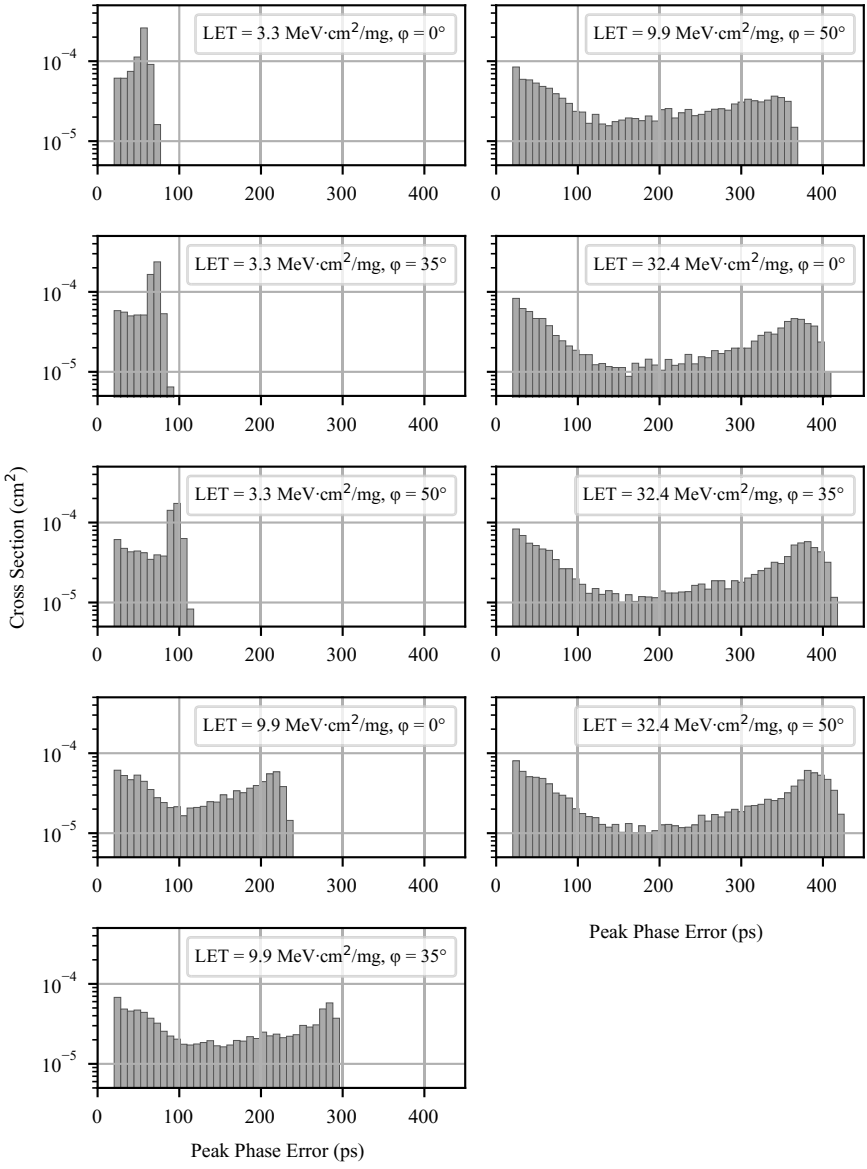


Figure 6.8: Distribution of the peak clock phase error stimulated by heavy ion irradiation. A consistent expansion of the phase error distribution is observed with higher $\mathrm{LET_{Si}}$ and shallower particle incident angles.

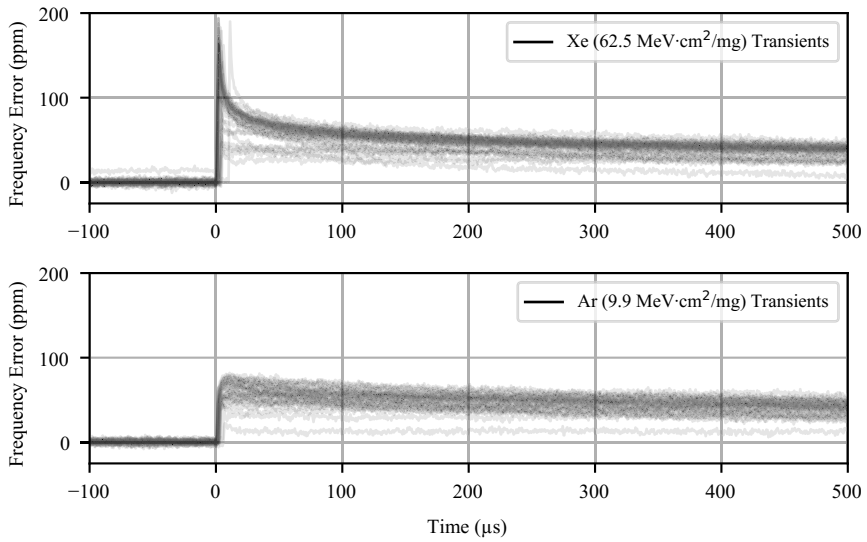


Figure 6.9: Frequency transients stimulated during broadbeam heavy ion irradiation. The response to irradiation with $^{124}Xe^{35+}$ ions is characterized by a pronounced initial frequency step, which quickly decays. This initial response is not observed with $^{36}Ar^{11+}$ ions.

of operation was chosen for two reasons: Firstly, it eliminates any potential contribution of SEE occurring in the reference clock path, phase detector, charge pump and loop filter from interfering with observations. Secondly, it allows observing the evolution of the radiation-induced transients inside the VCO directly, without any of the feedback control loop dynamics being superimposed. In this mode of operation, the frequency of the oscillator is measured using the high-resolution transient frequency measurement system presented in section 3.5.

Transient changes of the open loop frequency were observed for all ion energies used in the test. Figure 6.9 shows a sample of frequency transients collected with $^{124}Xe^{35+}$ and $^{36}Ar^{11+}$ ions. For both ions, the radiation response is characterized by a step-like frequency increase, which then decays back to the initial value. The temporal evolution of the generated frequency error changes significantly for LET_{Si} exceeding $10\,MeV\,mg^{-1}\,cm^2$. For those higher values of LET_{Si}, a sharp peak decaying in a few microseconds appears superimposed on the slow recovery process present also for lower LET_{Si}. Figure 6.10 better visualizes this difference by showing the evolution of frequency error on a logarithmic time axis. Detectable residuals of the effect persist for at least 10 ms after stimulation of the response, with the effect approaching full decay only

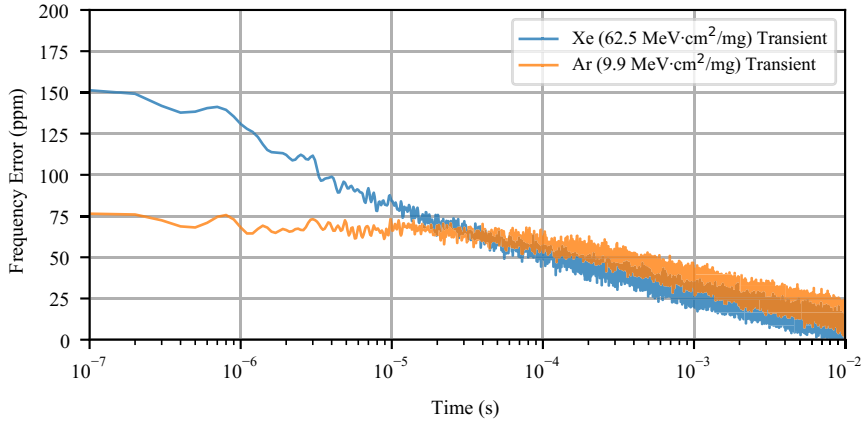


Figure 6.10: Frequency transients stimulated by broadbeam heavy ion irradiation shown on a logarithmic time scale. Detectable residuals of frequency errors were observed to consistently persist into the millisecond timescale.

at around 100 ms. For $\mathrm{LET_{Si}}$ exceeding 10 MeV mg^{-1} cm^2, the frequency error may exceed 50 ppm for up to 100 µs.

Similar to the analysis performed for the stimulated phase error in the closed loop PLL measurements, the distribution of peak frequency errors generated by irradiating the sensitive area can be computed. The distributions produced by two different ions are shown in figure 6.11. In agreement with the measurements obtained for closed loop operation, higher particle $\mathrm{LET_{Si}}$ results in larger peak errors being stimulated. Also notable is the broad, continuous distribution of peak frequency errors, which indicates a non-homogeneous sensitivity of the geometry.

6.4.4 Discussion

Contribution of Pile-Up

In the broadbeam irradiation experiments, the combination of a high ion flux with the long persistence of the radiation effect was observed to occasionally result in pile-up. This manifested as a baseline shift of recorded transients, as a result of a previous radiation response not having fully decayed. Since raw transient data was recorded, this problem could be remedied by using the baseline frequency as an additional qualifier during offline trigger processing. This procedure very efficiently discarded these events and since the proportion of events affected by pile-up was found to be low, their removal has little influence on the reported cross sections.

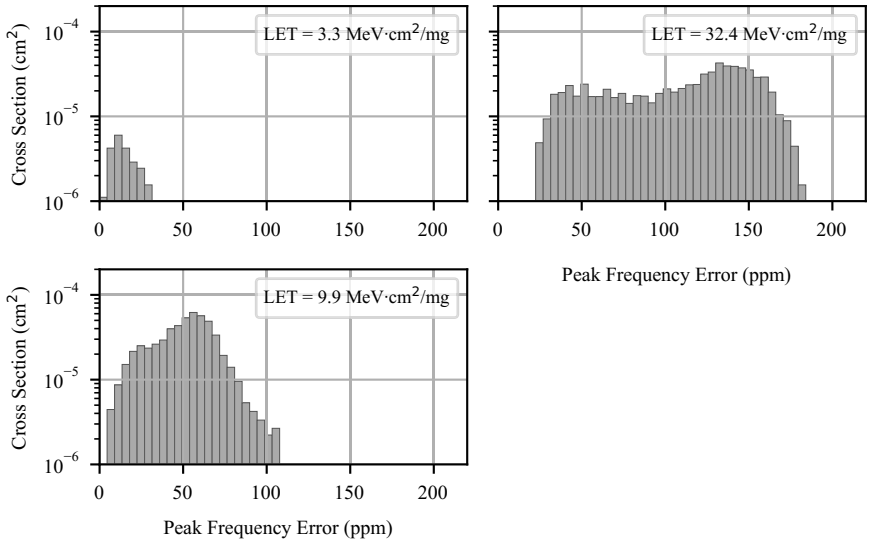


Figure 6.11: Distributions of the peak oscillator frequency error stimulated by broadbeam heavy ion irradiation. A broad distribution of values is stimulated, which expands with increased particle $\mathrm{LET_{Si}}$.

Comparison with Microbeam Irradiation Experiment

In addition to providing valuable insight on the distribution of phase error magnitudes stimulated by irradiation using multiple types of ions and angles, the results obtained from the broadbeam heavy ion experiment can also be discussed in relation to the performed microbeam heavy ion irradiation. First, the obtained cross section measurement can be compared between the two experiments. This comparison has to be performed with the contributions of pile-up in both experiments as well as the experimental differences (front-side vs. back-side irradiation, LET of the used ion species) in mind. The sensitive circuit area estimated from the microbeam experiments is approximately $4 \times 10^{-4}\,\mathrm{cm^2}$. This value agrees well with the data point in figure 6.7 taken at comparable detection threshold (200 ps) and $\mathrm{LET_{Si}}$ ($9.9\,\mathrm{MeV\,cm^2\,mg^{-1}}$), where a cross section of $2 \times 10^{-4}\,\mathrm{cm^2}$ is estimated. Given that the uncertainty of the detection threshold in the microbeam experiment as well as the contribution of pile-up might significantly modulate the first cross section estimate, an agreement to within a factor of two can be considered a good fit.

Also, the non-homogeneous sensitivity of the area shown in figure 6.4 is consistent with the obtained distributions of phase errors shown in figure 6.8:

The broadbeam measurements with increased phase measurement resolution have clearly shown that irradiation of random points inside the sensitive area stimulate a continuum of peak phase error magnitudes. This behavior is reflected also in the magnitude distribution of the underlying frequency errors, which were found to follow a similarly continuous distribution (see figure 6.11).

6.5 Proton Irradiation Experiment

The magnitude of observed transients during heavy ion irradiation experiments revealed a concerning magnitude of these effects, with potentially threatening consequences to the timing detector systems under design for the High Luminosity LHC upgrade. However, a number of issues prohibit performing exact predictions of the magnitude of events in a radiation environment representative of the LHC experiments based on the results obtained with heavy ion irradiation. The most prominent is the lack of a conclusive explanation of the underlying mechanism through which the radiation responses are stimulated, apart from the deposition of energy inherent to the passage of heavy ions. While previous studies concerned with the estimation of SEU rates in LHC particle environments based on heavy ion experiments exist [9, 10], these primarily consider the active devices used to implement digital logic and memory cells. A number of assumptions made in these works are likely incorrect for the sensitivity discussed here, such as their assumption of a small sensitive volume. A straight-forward application of these analyses methods may therefore lead to an incorrect prediction of upset rates in hadron-dominated radiation environments.

However, the cited studies have also identified mono-energetic proton beams with particle energies exceeding 60 MeV a reasonably realistic experimental approximation to many experimental environments, in the sense that these trigger the most important interaction channels in materials typically used in semiconductor devices. For this reason, another irradiation experiment using high-energy protons was conducted.

6.5.1 Methodology

The sensitive PLL circuit was irradiated using 200 MeV protons at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institut (PSI) in Villigen, Switzerland. Since only a small sample (about 25 mm^2) needed to be irradiated, a very high proton flux of $1.4 \times 10^9\,s^{-1}\,cm^{-2}$ could be achieved through beam collimation. The experiment was set up for normal proton incidence and the high-resolution phase measurement system presented in section 3.4 was re-used. Irradiation was performed exclusively during closed loop operation of the circuit and the same data processing as described in section 6.4 was applied to the obtained data. Since the choice of loop bandwidth was identified as a

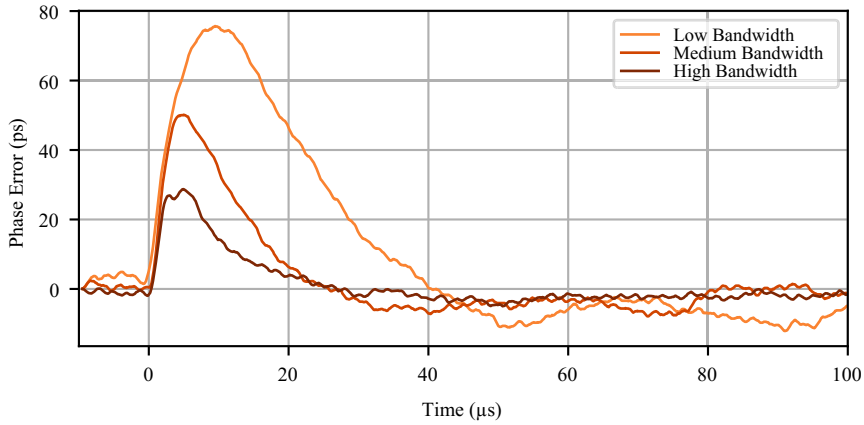


Figure 6.12: Largest observed transient responses under proton irradiation for different loop bandwidth configuration settings.

critical parameter influencing the radiation response amplitude, three different loop filter configuration parameters were studied during this experiment. These will henceforth be referred to as "low", "medium" and "high" bandwidth configurations.

6.5.2 Experimental Results

Radiation responses consistent in temporal behavior with the previously observed transients were detected as long as the beam was present. Transient responses were found to occur at approximately the same rate as during the heavy ion testing, even though a proton flux approximately five orders of magnitude higher was used. The transient responses corresponding to the largest events for each explored bandwidth setting is shown in figure 6.12. As anticipated, a consistent decrease of the peak phase excursion results from an increase of the loop bandwidth. An additionally noteworthy feature is the identical initial slope of the different transient responses. Since this slope is the manifestation of the instantaneous frequency error of the oscillator, this confirms that the underlying mechanism for the transients observed in a proton environment is still the SEFT originating in the spiral inductor.

All detected transient events were again classified according to their peak amplitude, such that their distribution can be analyzed. The distributions for different bandwidth configurations is shown in figure 6.13. The same trend of a contraction of the distributions with an increase in bandwidth is clearly visible.

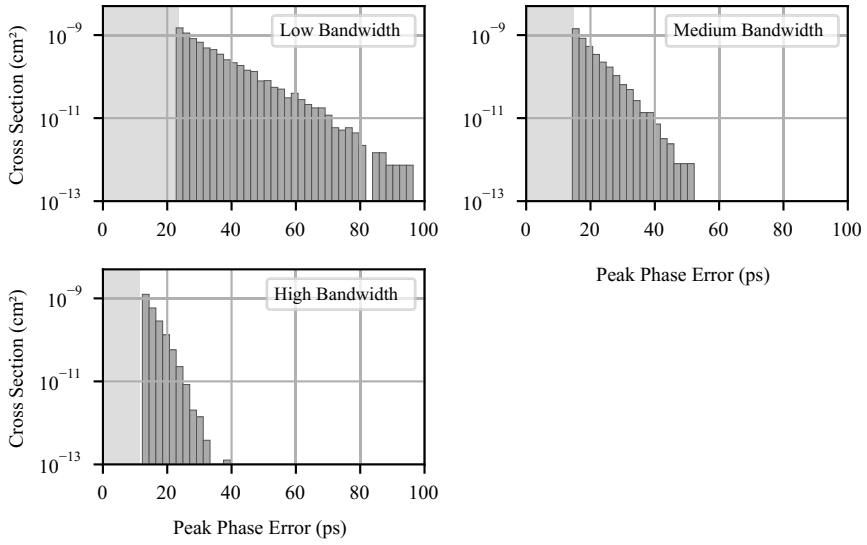


Figure 6.13: Distribution of peak transient phase errors stimulated by proton irradiation for different loop bandwidth configuration settings.

6.5.3 Discussion

Proton Interaction Mechanism

A first interesting aspect is the integrated cross section of observed events, which is approximately five orders of magnitude below the heavy ion cross section. This significant reduction indicates that the direct ionization from energy deposited by protons does not itself result in appreciable phase excursions of the loop. Protons with a kinetic energy of 200 MeV undergo only very little electric stopping in any of the relevant materials and therefore do not cause large amounts of direct ionization. Their LET in Si and SiO_2 is only a few $\mathrm{keV\,cm^2\,mg^{-1}}$, which is much smaller than any of the used heavy ion species in previous tests. The observed difference in cross section is therefore readily explained through nuclear interactions of the protons with atoms in or close to the sensitive geometry [9]. Such nuclear interactions can result in a breakup of nuclei, producing high-energy fragments in the process. These created ions then traverse the sensitive volume with a significantly larger equivalent LET, and in this way stimulate the same mechanisms that are also observed in the heavy ion experiments. The apparent reduction of cross section therefore results therefore from the cross section associated with the interaction of the incident protons and the nuclei of the various materials present in the vicinity of the

sensitive area, and the distribution of the energy deposition that results from these secondaries. The magnitude of the events in proton irradiation further strongly depends on the energy deposited by the fragments. This quantity is not directly related to the proton energy, but instead to the atomic mass of the materials present close to the sensitive volume.

Comparison to Heavy Ion Experiments

To establish a better comparison between the magnitude of events stimulated under heavy ion and proton irradiation, the data obtained in both experiments can be compared. However, as was shown in figure 6.13, the phase excursion magnitude is strongly dependent on the loop dynamics, and therefore further care must be exercised when comparing these different experiments. Unfortunately, different bandwidth configurations were used in the two experiments, which complicates direct comparison attempts. Table 6.1 tabulates the chosen configuration settings, with indicative loop bandwidth values calculated using [125, Eq. 13]. The most similar loop bandwidth setting was used during the low bandwidth proton experiment, where the largest transients approached 100 ps. A comparison with the data shown in figure 6.8 reveals that similar transient amplitudes are seen at a LET of $3.3\,\mathrm{MeV\,cm^2\,mg^{-1}}$, which gives an indication for the amount of energy deposited within the sensitive volume after a proton recoil event. With a better understanding of the sensitive geometry and by which mechanism the energy deposition translates into a frequency error of the oscillator, these results will provide useful information on the expected in-experiment impact of this sensitivity. Also worth discussing is the qualitatively different shape of the transients shown in figure 6.6 and figure 6.12. The transients observed during heavy ion irradiation were characterized by a significantly larger undershoot during the recovery process. This difference is likely the result of a significantly different the transfer function damping used in both experiments. Even though a similar bandwidth was used, table 6.1 shows that a much larger integral charge pump gain was used during the heavy ion irradiation experiment, resulting in reduced phase margin (or a lower loop damping factor, equivalently) during the heavy ion experiment.

6.6 Global Discussion of Experimental Results

A number of incremental and complementary experiments have been described in the previous sections. These have individually confirmed the presence of a sensitivity in the inductor of an LC-tank VCO. A further discussion of the experimental results in relation to one another is warranted in order to strengthen a hypothesis for an underlying mechanism causing this sensitivity.

Experiment	I_{prop} (µA)	R (kΩ)	I_{int} (µA)	BW (rel.)
Broadbeam Heavy Ion	54.6	3.94	43.7	1.0
Proton (Low BW)	16.4	7.88	5.46	0.59
Proton (Medium BW)	27.3	13.1	21.8	1.66
Proton (High BW)	49.1	19.7	49.1	4.5

Table 6.1: Comparison of PLL configuration settings used during heavy ion and proton irradiation experiments.

6.6.1 Role of Silicon and Dielectric Layers

While the interactions of heavy ion irradiation with active devices in silicon integrated circuits are a very widely studied topic, no active devices are present in the sensitive area that could explain the observed sensitivity. Of particularly surprising nature is the long decay time of the effect, which was found experimentally to extend into in the millisecond range, as highlighted in figure 6.10. Studies concerned with the interactions of heavy ions in silicon devices such as [126] make clear that the large charge carrier densities present after ion impact persist for only fractions of nanoseconds, fully reverting to their pre-irradiation value within 10 ns. This makes an explanation of the observed effect involving the generated charge carriers in the bulk silicon substrate implausible. This conclusion is supported by the fact that the PGS included in 'Inductor B' (used during the broadbeam experiment) failed to result in a significant reduction of the sensitivity compared to 'Inductor A' (used during the microbeam experiment). The responses seen from 'Inductor B' would have been expected to be much smaller if the responsible mechanism takes place in the silicon substrate and is therefore shielded from the inductor by the PGS. Even though the differences in experimental setup used in the two tests do not allow precisely quantifying the difference, it can be stated that the stimulated responses share approximately the same magnitude at comparable values of LET.

Another strong indication for an origin in the dielectric materials surrounding the inductor coil is the absence of any circuit responses in the laser TPA experiments: Even though the used pulse energies of 3 nJ produce localized EHP densities in silicon comparable to heavy ions with an LET_{Si} of 50 MeV mg^{-1} cm^2, our experiments failed to detect any phase deviations when irradiating the bulk silicon below the inductor. As discussed in section 6.3.3, laser experiments are unable to stimulate EHP generation in the dielectric layers, due to their significantly larger energy band gap (9.3 eV for SiO_2 [127]). Heavy ions in the

energy regime used in our tests on the other hand possess sufficient stopping power for generation of large densities of EHPs in both Si as well as dielectrics such as SiO_2. These experimental findings lead us to the conclusion that the responsible mechanism is most likely to be found in the dielectric layers above the silicon substrate.

6.6.2 Electrical Properties of the Inductor Geometry

In order to propose a mechanism responsible for the generated frequency errors during irradiation of the spiral inductor, the geometry of the inductor needs to be reviewed in more detail. The planar CMOS inductor used in the structure contains notable geometric features that require appropriate electrical modeling: The small gap between both windings and their proximity to the silicon substrate in combination with the large area covered by the conductors results in large distributed parasitic capacitance of two types: firstly, between the two closely spaced conductors (winding-to-winding capacitance) and secondly between the conductors and the substrate (winding-to-substrate capacitance). At operating frequencies in the GHz range, this implies that the impedance at the inductor terminals is determined by both the inductive components as well as these parasitic capacitances, which capacitively couple sections of the conductor to either the substrate or to other areas of the conductor in adjacent windings. While the overall complex impedance of the structure is indeed inductive, the distributed capacitances (and therefore the dielectric properties of the surrounding materials) play a major role in determining its real and imaginary components.

6.6.3 Proposed Mechanism for Stimulation of Frequency Errors

Since the LET of the heavy ion species used in the performed heavy ion experiments is very similar when considering the Si substrate and the SiO_2 dielectrics as targets, dense tracks of free charge carriers will be created in the dielectric layers surrounding the inductor. The dielectric properties of these layers are determined by their electric polarizability. The presence of free charge carriers and potentially also the excitation of defects through ionization could result in significant changes to the local polarizability of the material, and this may locally alter its complex permittivity. It can therefore be proposed that the complex impedance of the inductor structure is altered as a result of this interaction until these effects subside. This would imply either the recombination, trapping or collection of generated carriers and the return of electrically excited defects to their initial state. A conclusive quantitative analysis of this hypothesis is unfortunately difficult for multiple reasons: One major obstacle is uncertainty about the dielectric materials and their properties

in the CMOS process used in the experiments. Even when assuming that SiO_2 is used in the majority of inter-level-dielectrics, the properties of SiO_2 can vary strongly depending on the chosen method of fabrication. Deposited oxide layers, for example using CVD techniques, are typically characterized by much higher defect concentrations than thermally grown ones. These defects result in changes of quantities relevant to the polarizability, such as the charge carrier mobility and their lifetime. While the effective mobility accounts for the the amount of polarizability change by a given number of free carriers, the carrier lifetime would need to be large enough to explain the experimentally observed timescales. Unfortunately, a large body of fundamental research on these properties of amorphous SiO_2 (e.g. [128] and [129]) uses thermally grown, high purity SiO_2. Free electrons in this type of SiO_2 posses very high mobility, which makes them contribute strongly to the change of polarizability, however they are also characterized by very short lifetimes (on the order of tens of nanoseconds) [128]. Holes, on the other hand, are shown to have much lower mobility but significantly greater lifetimes: The lifetime of holes in amorphous SiO_2 was reported to exceed 100 ms at room temperature [129]. Another consideration here is the electrical excitation of defects in the SiO_2 and their impact on polarizability. While the literature on defects in SiO_2 indicates the presence of such excited states with decay times in the 10 ms range [130], their contribution to changes of the dielectric properties of the material remains to be quantified. Further modeling of the ionization and displacement processes in the dielectrics is required to conclusively attribute the effect to post-irradiation mechanisms inside the dielectric layers. Additionally, different experimental techniques must be considered to better separate different mechanisms, for example using X-ray or deep ultraviolet radiation.

6.6.4 Sensitivity of Radiation Response to Irradiation Angle in Heavy Ion Experiment

The proposed mechanism also offers an explanation for the increase of sensitivity observed with shallower particle incident angles in the broadbeam experiments (compare figure 6.8 and figure 6.11). Even though a large surface area is sensitive to irradiation, the sensitive dielectric volume extends vertically only about 5 µm. Shallower incident angles therefore significantly increase the path length of individual ions through the sensitive material, which results in the generation of more free carriers along their path. These observations are consistent with the hypothesis that the concentration of free charge carriers or excited defects determine the magnitude of the effect, by proportionally altering the dielectric properties of the material.

6.6.5 Relevance of Circuit Time Constants

A concern that needed to be considered throughout the experiment is whether the long persistence time of the observed responses could be explained through time constants present in the circuit itself. Since the experiments have conclusively shown that the effect is stimulated inside the VCO, the number of circuit components in which such a time constant would need to be identified is limited. It is clear that neither the primary time constant formed by the LC-tank (which resonates at 5.12 GHz) nor the bandwidth of the frequency control input of the VCO can be responsible for this effect. The latter, while limited through use of the modified varactor topology, is still in the order of 20 MHz and therefore may only introduce a time constant of the order of nanoseconds. One alternative hypothesis considered is shown here, but was ultimately determined to be insufficient to explain the response time constants.

CMOS VCOs are known to be susceptible to AM-to-FM conversion, for example as a result of nonlinear capacitances in the tank [64]. Long-lasting frequency transients may therefore be expected in case long time constants are important in processes relating to the oscillation amplitude. Following a disturbance of the amplitude, the tank voltage envelope (which may convert into a frequency error) can be described by the exponential given in equation (6.1).

$$\hat{v}_{\mathrm{tank}}(t) = e^{-\frac{t(1-g_m R)}{RC}} \tag{6.1}$$

In this expression, C and R model the tank capacitance and its loss resistance, while g_m represents the transconductance of the active device. As the oscillation amplitude grows, g_m decreases as it nonlinear operation is approached, until the product $g_m R$ is equal to one. This fact makes g_m a function of $\hat{v}_{\mathrm{tank}}$. Due to this relationship, the term $(1 - g_m R)$ slowly approaches zero as the amplitude grows, which in principle leads to an infinitely long time constant for establishing the steady-state oscillation amplitude. However, it was found that in practical circuits, this is without significance compared to the observed responses and this theoretically infinitely long response does not practically emerge during circuit operation. Both in simulations and laboratory experiments, any appreciable transient response of the tank voltage envelope following a step change vanished within a few oscillation periods and no frequency error could be resolved after this time. It can therefore be concluded that the observed response can not be explained by time constants inherent to the circuit.

6.6.6 Novelty of the Observation

Given that SEEs in PLL circuits have been a focus of research for a long time and methods for their characterization have been reported in the scientific literature for at least 25 years [60], an explanation for discovering the described effect only recently needs to be provided. From an analysis of the literature concerned

with radiation effects in PLL and oscillator circuits, it may be concluded that this is a result of at least three separate factors:

Dominance of ring oscillators in relevant studies

A survey of available publications concerned with assessment of single-event effects hardness of PLL and VCO circuits revealed that the overwhelming majority of studies utilize ring oscillator VCOs. Apart from publications of our own research group, irradiation experiments performed with LC oscillators are reported in [63, 131, 132, 133, 134, 135]. Common to all these publications is the exclusive use of laser irradiation techniques for experimental validation. While [63] reports on a sensitivity in the area occupied by the inductor, the sensitivity is attributed to the tuning varactors placed in the same area. The authors specifically refer to the charge collection sensitivity of MOS varactors previously reported by our research group in [121], which can not explain the observations presented here. The remaining literature utilizes a single photon absorption technique and reports sensitivities only during irradiation of active devices present in the LC oscillator. As previously explained, we hypothesize that the circuit responses we describe do not originate in the silicon substrate. Both single- and two photon absorption laser experiments are however unable to stimulate EHP generation in the dielectric layers with their larger energy band gap, which likely explains the absence of earlier discoveries.

Chosen PLL bandwidth

A contributing factor influencing the magnitude of the observed radiation response is the choice of PLL bandwidth. Since the underlying radiation response was found to be a frequency error (as opposed to a phase error), the amount of phase error accumulated in the PLL is strongly dependent on the loop bandwidth. Higher loop bandwidths will result in faster reaction of the control loop and therefore the accumulation of less phase error. As an example, even though the same VCO as described in this article is also used in [62], it is embedded in a high speed CDR loop with a bandwidth of 2 MHz, a factor of 20 higher than in the experiments presented here. Even though heavy ion irradiation will have stimulated the same frequency errors in this VCO, the resulting phase errors were small enough to remain below the detection threshold.

Detection and measurement sensitivity

A final contributor is the use of test equipment with sufficient sensitivity. While our group has tested low-bandwidth LC PLL circuits before, for example in [64], transient phase instrumentation resolution in these experiments has been

far lower than with the techniques applied in this work. While in this previous work the resolution and detection threshold of phase transients was limited to 390 ps, the detection threshold of the setup used in this work is essentially only limited by the clock jitter of the PLL itself, which is below 50 ps peak-to-peak. Other works, such as [63], [131] and [132] utilize spectral analysis methods for detection of phase or frequency errors instead of time-domain measurements. The differences between these types of instrumentation and the implication on experimental work have been discussed in section 3.2. The achievable resolution and noise floor of the methods used in these other works is not trivial to assess, but available information in the publications indicates that detection of effects on the level reported here could have been impossible in the first place due to insufficient sensitivity.

6.6.7 Mitigation of the Sensitivity

The performed experiments, particularly the encouraging results obtained during proton irradiation, suggest that the magnitude of the radiation response can be reduced by a sufficient increase in loop bandwidth. However, it also reveals that the discovered sensitivity is not of purely academic interest, but may actually impact clock synthesizer performance in practical radiation environments. Since the loop bandwidth is an important parameter used to achieve optimal phase noise and spurious performance of a frequency synthesizer, it should ideally remain unconstrained by radiation tolerance considerations. For example, when using better on-chip VCOs, a higher degree of reference clock jitter suppression can be achieved by adopting a smaller reference bandwidth. Such applications will surely be part of future developments in radiation-tolerant frequency synthesis and distribution systems, and therefore a root-cause mitigation of the observed sensitivity must be sought after. As long as the sensitivity of the inductor itself can not be reduced, it appears more appropriate to augment PLL circuits with adaptive control techniques such as gear-shifting [107] to minimize the impact of transient radiation responses.

6.6.8 Impact on All-Digital Frequency Synthesizers

All experimental results presented in this chapter were obtained with a conventional, charge pump-based PLL circuit. However, since the effect was shown to originate in the planar inductor of an LC-tank oscillator, its practical impact is not limited to this particular PLL architecture. As described in section 5.3, a large cross section compatible with the observed effect has also been observed during heavy ion testing of the all-digital frequency synthesizer discussed in chapter 4 and chapter 5. In the LC DCO-based ADPLL circuit, the largest heavy ion cross section by far can be attributed to this sensitivity. While the amount of phase error stimulated by this sensitivity is small in comparison to

other identified sensitivities, it can currently only be mitigated through the choice of different loop filter configuration. As expected from a frequency error, lower phase error is accumulated when the loop gain (and therefore the loop bandwidth) is increased. Since ideally, the choice of loop parameters should remain a free variable in order to optimize jitter performance, further emphasis must be placed on identifying systematic mitigation measures also for ADPLL synthesizers going forward. In this regard, the highly digital nature of ADPLL circuits may offer a substantial advantage for the implementation of suitable mitigation strategies. Since additional monitoring and control functionalities can natively extend the digital loop filter structures and can be implemented within the same, highly automated EDA tool flow, reduced engineering overhead is required compared to custom or mixed-signal implementations of such techniques.

The general comments concerning the limitations of bang-bang phase detectors given in section 5.3 remain valid for this effect as well. The inability of a binary phase detector to quantify the magnitude of an SEE-induced phase error also does not allow implementing a control action proportional to the phase error. This is likely to lengthen the recovery process from a given transient radiation response. The proposed augmentation of the BBADPLL by a low-power TDC dedicated to the detection and reaction to such events would therefore also constitute a viable mitigation strategy concerning this specific sensitivity, and therefore become even more meritable.

6.7 Summary

A previously unreported radiation response affecting inductors manufactured in a commercial 65 nm CMOS process was presented. In a tested PLL circuit, the effect was shown to produce frequency errors resulting in phase excursions large enough to significantly impair circuit performance. The fact that this effect was found to directly impact the performance of a low-jitter PLL circuit underlines the increasing importance of considering SEEs in passive circuit components, which have been traditionally assumed to be insensitive to SEEs when compared to their active counterparts. Multiple experiments were performed to conclusively attribute the observed sensitivity to the inductor used in the LC tank of an oscillator and quantitatively characterize the produced effect. Different hypotheses for the underlying mechanism have been discussed and the experimental results strongly suggest that the observed responses are a result of temporarily altered polarizability or conductivity of the dielectric materials surrounding the inductor metallization. The resulting stimulated change of the complex permittivity alters the impedance of the inductor structure, which in turn changes the resonant frequency of the oscillator temporarily. Direct measurements have shown that this effect persists on timescales exceeding the

10 ms range. This is likely a result of high carrier lifetimes or the long-lived excitation of defects in the dielectric materials. A full quantitative treatment of the observed responses and their underlying mechanisms can not yet be provided. Further experiments and modeling are needed to better understand the origins of the effect. These will be necessary foundations for developing effective mitigation strategies for circuits using on-chip inductors in radiation environments. As the dielectric properties of on-chip materials play a role for a number of other circuit elements than inductors, it appears likely that the presented research also potentially extends into the general domain of RF and mm-wave circuits, as well as capacitor-based ADC and digital-to-analog converter (DAC) architectures.

The discovery of this effect during the work on this thesis has been primarily the result of improvements in the instrumentation for radiation-tolerant frequency synthesizer circuits presented in chapter 3. The performed experiments clearly highlighted that this identified sensitivity is not only present in contemporary radiation-hardened frequency synthesizer circuits, but also that it results in measurable performance impact in relevant radiation environments for high energy physics.

Chapter 7

Conclusions

The work presented in this thesis has addressed a number of important issues in the field of clock generators suitable for applications in harsh environments, such as the radiation environments commonly found in HEP detector systems. Advances to the state of the art were made through the multi-faceted approach to the requirement-driven development of instrumentation, the design of radiation-tolerant all-digital clock generator circuits, and research in the domain of basic radiation effects in passive circuit components.

The thesis has reviewed the state of the art in the domain of radiation-tolerant clock generator circuits together with the requirements of contemporary and future systems in HEP, as well as emerging technology trends in this domain. A lack of instrumentation suitable to reliably validate the compliance of such circuits with system and circuit requirements in radiation tests was identified. This shortcoming was shown to affect even the circuits and systems under consideration for near-future upgrades of the LHC. The identified need was successfully addressed by the development and characterization of a number of dedicated instrumentation techniques. The different proposed systems are tailored to the technical requirements and the diverse operational constraints of the facilities available for radiation testing. Fully delivering on the promise of increased measurement resolution, high detection sensitivity and a reduction of dead time, these developments have provided the basis for the comprehensive experimental evaluation of clock generator circuits performed in subsequent chapters of the thesis.

Their development has also enabled the detection of a previously unacknowledged radiation effect in a passive on-chip inductor structure. Upon irradiation, long-lasting frequency errors were found to be stimulated within the oscillator circuit containing this inductor. The most likely cause of this sensitivity are temporary and reversible changes in the complex permittivity of the dielectric

materials surrounding the inductor coil. The discovery of this sensitivity has already had a significant impact on the radiation effects assessment and qualification strategy employed for a number of HL-LHC ASICs, in particular the lpGBT. Since particularly in the field of RF and millimeter wave circuit design, dielectric material properties become exceedingly important, it appears likely that the relevance of such sensitivities will only increase as electronics for HEP and other harsh radiation environments continue to venture into this domain. While the systems currently being implemented are still able to tolerate this SEE sensitivity by adopting the experimentally validated mitigation strategies, it is clear that sensitivities in passive circuit structures possess the potential to at some point become fundamental limitations to the performance of not only frequency synthesizers, but also other radiation-tolerant high-frequency circuits and the larger systems they are used in.

Another important contribution to the field was made by the development and characterization of all-digital PLL circuits for the implementation of radiation-tolerant clock generators. Research performed on radiation hardening aspects of digitally controlled oscillators highlighted that structural differences between these circuits and their voltage-controlled analog counterparts can be leveraged to obtain higher levels of tolerance to single-event and TID effects. For example, it was demonstrated that digital oscillator tuning schemes can be exploited to significantly reduce the susceptibility of DCO circuits to single-event phase and frequency errors.

Suitable radiation hardening approaches for the digital components (digital loop filter, sigma-delta modulator, feedback dividers, etc.) of ADPLL circuits were also explored. In the proposed ADPLL circuit, full protection against SEEs was achieved by a consistent adoption of TMR in all digital circuit components. Compared with the analog circuits in conventional PLLs, which often require extensive analysis and experimental characterization of their resilience to SEEs, the application of such systematic, provable design hardening techniques can be considered a major paradigm shift. The design automation benefits of these hardening techniques, combined with the technology-agnostic implementation of all-digital PLL circuits using hardware description languages instead of transistor-level schematics will be a key contributor to the successful adoption of advanced CMOS nodes in the HEP community in the near future.

Of particular importance to the work in this domain was therefore also the exploration of a design, implementation and verification methodology which does not only achieve the required performance, but also enables simulation-based verification of the correctness and completeness of the applied radiation hardening strategy during different stages of the design. The devised approach relies heavily on a reusable verification environment enabling simulations of ADPLL circuits on the algorithmic, register transfer and gate level, while also incorporating the required fault injection facilities. This framework has

successfully catered to the needs of functional and performance verification as well as the radiation hardness assurance process without having to resort to more computationally intensive transistor-level or mixed-mode simulations. Due to the excellent scalability of this approach, it will enable the design of more advanced and complex all-digital PLL and CDR circuits in the near future.

Based on the experimentally obtained results with the manufactured test chip, a number of strategies have been suggested to further increase the radiation tolerance and reliability of ADPLL circuits. Clearly, the highly flexible nature of the digital circuits used to implement the PLL data path can be exploited for this purpose. Further, statistics and heuristics of signals in the PLL may be monitored and processed using additional digital logic, which can enable the autonomous optimization of performance as well as fault detection, signalling and correction, similar to the FDIR techniques long established in other domains of digital electronics. Owing to the beneficial power dissipation and scaling trends of digital circuits in advanced CMOS design nodes, such additional complexities can likely be implemented without an excessive penalty in area or power.

In summary, ADPLL circuits were shown to provide an avenue for successful and efficient implementation of both general purpose and high performance frequency synthesizer circuits, while successfully addressing the challenges of technology scaling and radiation environments. It was shown that with the adoption of an all-digital PLL architecture, similar or better levels of radiation tolerance than currently provided by their conventional counterparts can be achieved. The experimental results further suggest that the designed ADPLL circuits can cater in principle not only to the radiation environments of particle accelerators. For example, the achieved level of protection may at the same time be considered sufficient for applications in the domain of spaceflight, where radiation tolerance and reliability are also key aspects of electronics design. The adopted approach of achieving SEE protection using TMR is also considered as a means of yield improvement when using advanced fabrication techniques [136]. Considering on the other hand the identified shortcomings of the tested ADPLL circuits, an observation initially made for conventional PLL circuits was found to remain true. All SEE sensitivities identified in the prototype ADPLLs circuits could be attributed to their respective DCO circuits. Remaining a highly sensitive mixed-signal component even in all-digital PLL circuits, their verification, in particular against SEE-related issues continues to remain a crucial aspect of the design process. Clearly, further advances in the modeling and simulation process of DCOs must be made going forward, such that vulnerabilities can be identified and fully mitigated early in the design cycle.

7.1 Future Work

The performed research has opened avenues for further study and experimentation in the field of radiation-tolerant frequency synthesis. This section summarizes a number of these aspects in each of the respective areas that will provide a meaningful continuation of the presented research.

7.1.1 Radiation Test Instrumentation

A number of flexible instrumentation setups for use during irradiation experiments have been presented. Conceptually, each of these schemes offers extensive flexibility for adaption to needs of specific test facilities, which was one of their main design goals. The biggest challenge for the developed systems will be keeping up with the high performance requirements of radiation-tolerant synthesizers. Further refinements to the concepts established in chapter 3 can be applied in order to optimize their noise performance and integration with test facilities. Especially in the face of the challenging experimental environment that some test facilities provide, further developments may also focus on reducing the susceptibility to interference of experimental setups while retaining or improving their noise performance.

Another aspect requiring future consideration is the detection and classification methods applied to the data obtained with these instrumentation setups. During the analysis of the experimental data presented in chapter 5 and chapter 6, a number of ad-hoc methods and algorithms were used to enable the automated detection, extraction and classification of circuit SEE responses. When presented with the large amounts of data produced by the high-speed and high-resolution instrumentation setups, the robustness and classification accuracy of such ad-hoc methods and algorithms becomes a significant issue, since the amount of available data is simply too large for exhaustive manual processing. This shortcoming provides an opportunity for the application of techniques based on statistical signal properties, template matching or machine learning in the detection and classification process. The domain of RF signal identification can be a source of inspiration, but also the large field of anomaly detection in time series may offer a wealth of applicable techniques. Parallels to other applications in SEE testing can already be identified, such as the recently emerging body of work concerned with SET detection using machine learning techniques [137].

7.1.2 Radiation-Tolerant All-Digital Clock Generators

The ADPLL frequency synthesizer concept has, through its implementation in a test chip and a variety of radiation tests, clearly proven its viability for implementation in future HEP electronics. While this initial design has

demonstrated the feasibility of a systematic radiation hardening approach, it has merely opened the avenue to now fully exploit the system-level advantages these digital architectures can provide. The performance of the BBADPLL architecture can be extended by a variety of techniques to improve performance and reliability: The introduction of adaptive control techniques will allow increasing the SEE-awareness of circuits and systems through the detection of radiation effects and allows for a more appropriate reaction. For example, the inclusion of an auxiliary low-power TDC into the proposed ADPLL circuit has been suggested to improve the response time to currently unavoidable single-event effect sensitivities in the DCO. Fast-locking techniques and adaptive loop filter structures may be leveraged to further reduce the impact of SEEs. Additional monitoring and calibration logic or dynamic supply voltage scaling can allow autonomously adapting circuit parameters to process variations, changing environmental conditions or even TID-induced degradation.

At the same time, the evolution of detector systems and their need for increased data link capacity also clearly show research opportunities for extending the scope covered by radiation-tolerant ADPLL circuits. Implementation of higher data rates will require the adoption of higher order modulations such as pulse-amplitude modulation (PAM), which further drives the need for clock generation at the lowest levels of jitter achievable. Implementing PAM-4 communication links compliant with specifications such as IEEE 802.3cd [138] in accelerator environments will require extending the research on radiation-tolerant clock generator circuits to also cover fractional-N synthesis. Fractional-N synthesis is a field already explored and revolutionized by all-digital architectures in commercial environments, in the form of phase-domain ADPLLs [22]. Their increased complexity compared to integer-N PLLs will require further study of sensitive time-based signal processing blocks such as TDCs and digital-to-time converters (DTCs). Recent feasibility studies also begin to consider the use of millimeter wave wireless communications especially in particle tracking detectors of collider experiments [139]. In such demanding applications, radiation-tolerant on-chip frequency synthesis will naturally also be required.

Finally, interesting trade-offs remain to be explored by taking different approaches to radiation hardening. It can be argued that the power penalty paid by the application of full TMR to all digital PLL components is significant. In systems where temporary disruptions of the circuit functionality can be tolerated as long as they are reliably detected (such that corrective actions can be taken), a fraction of the power required for hardening could likely be expended on detection strategies instead. Such trade-offs may also be made on a block-by-block basis, such that for example the level of redundancy could be reduced in high-speed dividers, as long as adequate detection and fast correction for any radiation-induced corruption can be implemented. As such, the flexible nature of ADPLL circuits presents a wealth of further aspects to be studied as

requirements for applications in HEP experiments of the future emerge.

7.1.3 Radiation Effects in Passive Circuit Elements

From the results presented in chapter 6, it becomes clear that for successful implementation of high performance clock generator circuits targeting harsh radiation environments, considering radiation effects solely in active devices is no longer sufficient. To be able to cope with the tightening requirements for such circuits in the future, a number of further issues need to be addressed. Further fundamental research is required to unambiguously identify the mechanisms responsible for the observed radiation responses in such passive device structures. While the underlying physical phenomena are most likely well understood from an electrodynamics and particle-matter-interaction standpoint, the inter-domain link between that of solid state physics and the electromagnetic properties of structures on the macroscopic level remains to be firmly established. Various opportunities for further study of this sensitivity exist and can be pursued in the form of theoretical analysis, molecular dynamics simulations, as well as in the experimental domain.

Only with a solid understanding of the relevant dynamics can suitable mitigation strategies be proposed and implemented, which will be a key enabling factor in achieving ultimate radiation hardness of circuits based on these materials. Even in the constraints of the fabrication process dictated by commercial CMOS technologies, the inductor geometries themselves can likely be optimized to partially or fully suppress the observed radiation sensitivities. Such mitigation efforts should also be augmented by system-level mitigation strategies: Synergies with the proposed implementation of detection and fast-recovery schemes for ADPLL circuits described above may allow tolerating the presence of such radiation effects, as long as their occurrence can be reliably detected and corrected or at least signaled to downstream detector or upstream data processing systems. While such approaches might be unavoidable in the future and can help making detector systems more intelligent, their introduction also dictates studying the complex trade-offs that come with the resulting increase in system complexity.

On the other hand, the identified sensitivities might also offer opportunities in radiation detection applications. With a firmly established understanding of the underlying sensitivity, geometries that maximize the susceptibility to indicident radiation can be designed. Paired with appropriate readout circuits, such structures could be used to implement or augment particle detection or dosimetry applications.

List of Publications

A number of scientific journal articles and conference proceedings contributions have been prepared during work on the thesis. This appendix lists all relevant contributions that have been published or accepted for publication. Where content of these articles is repeated (verbatim or in modified form) in this thesis, this is indicated below.

S. Biereigel, S. Kulis, P. Moreira, J. Prinzie, P. Leroux, A. Kölpin. **Methods for Clock Signal Characterization using FPGA Resources [65]**
This article presents two concepts for the characterization of clock signal parameters particularly suitable for implementation in FPGAs. One of the two concepts is concerned with the detection of SEE responses on such clock signals. This part of the article relevant to the thesis is included with minor modifications as section 3.3 of this thesis.

S. Biereigel, S. Kulis, P. Leitao, R. Francisco, P. Moreira, P. Leroux, J. Prinzie. **A Low Noise Fault Tolerant Radiation Hardened, 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS [39]**
This paper reports a radiation-tolerant CDR circuit, which has been designed for the lpGBT circuit. Over the previously published conference paper [77], this journal article adds two relevant aspects with relevance to the thesis: Firstly, it provides important details of the oscillator circuit studied in chapter 6. Additionally, the reported SEE testing results have been obtained with the transient instrumentation presented in chapter 3 of this thesis.

S. Biereigel, R. Oliveira Francisco, S. Kulis, P. Vicente Leitao, P. Leroux, P. Moreira, J. Prinzie. **The lpGBT PLL and CDR Architecture, Performance and SEE Robustness [62]**
This conference proceedings article summarizes measurements performed on the lpGBT ASIC foreseen for the High Luminosity LHC upgrade. Similar to the previous publication, it is relevant to the content of this thesis since it reports on

circuit details important for the studies in chapter 6, and SEE characterization results included in this article have been obtained using the instrumentation presented in chapter 3 developed as part of this thesis.

S. Biereigel, S. Kulis, P. Moreira, P. Leroux, J. Prinzie. **Radiation-Tolerant Digitally Controlled Ring Oscillator in 65 nm CMOS [93]**
This journal article results on the findings obtained during research on a radiation-tolerant DCO architecture. The theoretical and design-related aspects of this article are incorporated in section 4.5 and measurements obtained with this structure, both standalone and when integrated into a radiation-tolerant ADPLL are reported in chapter 5.

S. Biereigel, S. Kulis, P. Moreira, A. Kölpin, P. Leroux, J. Prinzie. **Radiation-Tolerant All-Digital PLL and CDR with Varactorless LC DCO in 65 nm CMOS [87]**
This article reports on the development and implementation of a radiation-tolerant ADPLL architecture. The publication summarizes the design process and results obtained with the developed test chip. The article contains a subset of the considerations and results presented in chapter 4 and chapter 5.

S. Biereigel, S. Kulis, P. Leroux, P. Moreira, A. Kölpin, J. Prinzie. **Single-Event Effect Responses of Integrated Planar Inductors in 65 nm CMOS [120]**
This article reports for the first time in the scientific literature on the discovered SEE responses originating in planar inductor structures. Along similar lines of the organization of the thesis, this article focuses on the experimental methodology and results obtained. Since a significant need for follow-up research was identified, neither the article nor this thesis offer a conclusive, proven explanation for the origin of the effect. The contents of the article are included as chapter 6 of this thesis. An additional contribution of this thesis to this chapter is the reporting of results obtained with proton irradiation.

List of Third-Party Contributions

This appendix lists significant third-party contributions to the presented work.

Chapter 1

No third-party contributions.

Chapter 2

No third-party contributions.

Chapter 3

Dr. Szymon Kulis[1] supported the work presented in section 3.4 with the schematic entry and PCB layout of the analog phase measurement system. David Porret[1] has kindly manufactured the enclosure for the finished device shown in figure 3.6.

Chapter 4

Dipan Kar[2] contributed the initial schematic and layout design of the Varactor-less LC DCO presented in section 4.4. The schematic and layout of this design was partially modified according to the requirements of this work. Dr. Szymon Kulis[1] contributed the RTL description for the radiation-tolerant I^2C slave used for control of the manufactured test chip.

Chapter 5

No third-party contributions.

Chapter 6

The circuit used during experiments reported in this study was originally designed by Jeffrey Prinzie[2] [77] for use in the lpGBT ASIC. A test chip containing this circuit used during Broadbeam Heavy Irradiation was provided by the ETROC Team (H. Sun[3,4], D. Gong[4], X. Huang[4], A. T. Liu[4], C. Liu[4], T. T. Liu[5], Q. Sun[5], J. Ye[4], L. Zhang[3,4]). Kay-Obbe Voss[6] has kindly provided access to the Microbeam facility at GSI Darmstadt, Germany. Salvatore Danzeca[1] has kindly provided access to the Proton Irradiation Facility (PIF) at PSI in Villingen, Switzerland.

Chapter 7

No third-party contributions.

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