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PolyData/DataRace — Polymer-Integrated CMOS-Based High-Speed Communication Systems at W-Band

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DOI: 10.26127/BTUOpen-5917

11.1 Introduction

There is an ever increasing demand for higher data rates in wireless consumer communications. Recent communication systems achieve data rates close to the maximum channel capacity. To achieve even higher throughput there are two possibilities: employ massive MIMO techniques or increase the usable bandwidth by adopting higher frequency bands. MIMO is always related to a high signal processing effort, especially if very high data rates are involved. Regarding the carrier shift to higher frequencies, a clear trend is apparent in consumer wireless communication over the last years. For example, common WiFi operates at 2.4 GHz. Meanwhile the standard extends up to 5 GHz and also the 60 GHz band has been adopted. Millimeter wave bands offer much more bandwidth, which makes them very attractive for high data rate wireless communications.

Following the trend towards higher frequencies for higher throughput, the PolyData and DataRace projects aim at a wireless communication system operating at W-band from 75 GHz to 110 GHz and achieving 100 Gbit/s. It is challenging to design millimeter wave systems at reasonable performance because of the required precision for mechanical parts and high electrical requirements for passives. Furthermore, the overall system cost is critical for systems targeting consumer-markets. High precision additive manufacturing using stereolithographic 3D-printing and metalization processes allows batch production of system-in-package designs [417]. This technology enables highly complex systems with low per-unit cost in high-volume production. For the active components, complementary metal-oxide-semiconductor (CMOS) is the technology of choice for cost-sensitive mass-market applications. Using CMOS is advantageous in terms of overall cost and performance when the microwave front-end and digital back-end are integrated on a single chip [418]. CMOS is the only technology that delivers state-of-the-art digital performance according to its heritage. Compared to compound semiconductors, CMOS offers moderate microwave performance. However, as shown in Fig. 11.1, the f_{T} and f_{max} of CMOS transistors increase when further downscaling the gate length. A 40 nm CMOS process offers transistors with f_{T} and f_{max} larger than 200 GHz and is therefore well suited for W-band applications. For gate lengths smaller than 28 nm leakage currents and fields penetrating from source and drain into the channel degrade the transistor performance. Both problems can be overcome with fully-depleted silicon-on-insulator (FDSOI) CMOS processes [420], as illustrated in Fig. 11.2. The transistor is built on a thin insulating buried oxide which decreases the drain- and source-to-substrate capacitances and prevents leakage currents. As a result, a FDSOI process can deliver improved microwave performance compared to the bulk counterpart for a given minimum process gate length.

This chapter is organized as follows. First a general concept and system

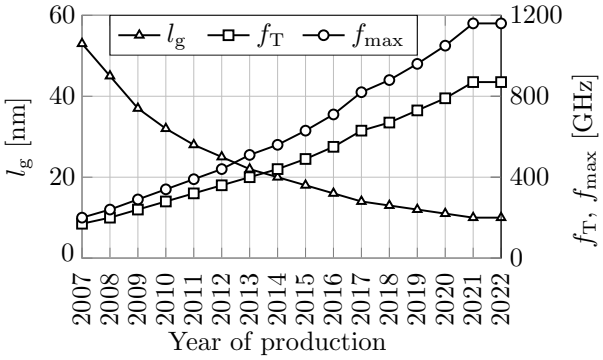


Figure 11.1
Impact of CMOS scaling on f_T and f_{max} according to ITRS roadmap 2007. From [419].

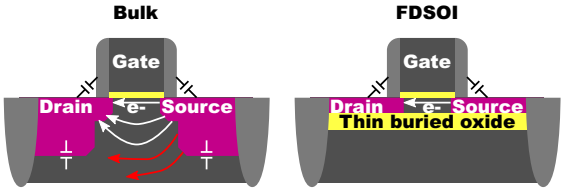


Figure 11.2
Bulk and FDSOI CMOS transistors cross-section.

analysis is given in Section 11.2. Next, in Section 11.3 the front-end and the components it is composed of are described. At last, some conclusions are drawn in Section 11.4.

11.2 Concept and System Analysis

Three different application scenarios for the proposed communication system are identified in [421]. They are summarized in Table 11.1. The first scenario applies to a single wireless link between two devices less than one meter apart from each other. Due to the proximity of the devices, alignment is easy and only a small scan angle is required. The second and third scenario correspond to small rooms like offices and larger rooms like departure lounges, respectively. Here, a wider scanning range is required. The total system data rate is shared by time-domain-multiplexing between multiple users. Two circular polarizations are used. Thus no alignment of two devices on their roll axis is needed. Additionally, the two polarizations offer separate communication channels. This allows to split the total 100 Gbit/s data stream into two 50 Gbit/s streams, which reduces the overall system bandwidth requirements.

Table 11.1
Application scenario requirements proposed in [421]. From [421] © 2014 IEEE

Scenario no.	1	2	3
Maximum distance	1 m	10 m	20 m
Angular range	±15°	±30°	±45°
	Single link	Multi-user	Multi-user

The schematic front-end shown in Fig. 11.3 is assessed in [421]. Only modulation schemes with moderate complexity are considered in order to relax the signal processing requirements. Figure 11.4 shows the signal-to-noise ratio (SNR) needed for a bit-error-rate (BER) below 10^{-3} in a bandwidth of 27 GHz. Binary phase shift keying (BPSK) is not suitable for achieving 100 Gbit/s. Quadrature phase-shift-keying (QPSK) yields 54 Gbit/s at an SNR of 9.8 dB. Using both polarizations, doubles the data rate to more than 100 Gbit/s. With

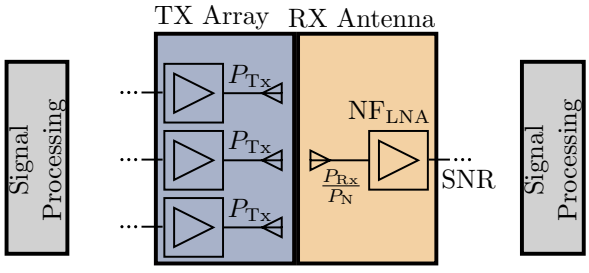


Figure 11.3
Schematic signal processing chain with transmitter and receiver. From [421] © 2014 IEEE

16-quadrature-amplitude-modulation (16QAM) and 16QPSK it is possible to transmit more than 100 Gbit/s per polarization at the cost of a higher SNR. The SNR and assumptions on the performance of the system components [421]

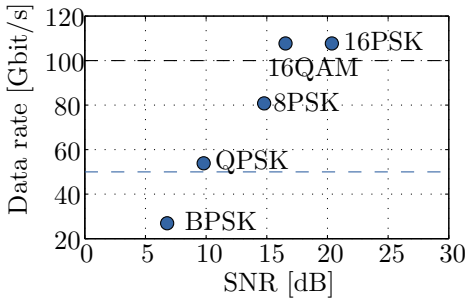


Figure 11.4
Minimum SNR for a BER of 10^{-3}. From [421] © 2014 IEEE

yields the number of elements of the transmit and receive antenna arrays for the different scenarios (see Table 11.2). With QPSK, respectively 2, 10, and

Table 11.2
Required number of array elements for different scenarios and modulation schemes. From [421] © 2014 IEEE

Modulation type	Minimum SNR	TX-elements (RX-elements)		
		Scenario 1	Scenario 2	Scenario 3
QPSK	9.8 dB	2	10 (5)	19 (8)
8PSK	14.8 dB	2	17 (7)	33(11)
16PSK	20.4 dB	4 (3)	32 (11)	63 (17)

19 array elements are needed for the three scenarios to enable data rates in excess of 100 Gbit/s.

11.3 W-Band Front-End

In the considered communication system, the antennas, the polarizers, and other passive components of the transmitter and the receiver are basically very similar. Therefore, the focus here is on the receiver to demonstrate the performance of the approach. Because of its particular features, also the power amplifier (PA) will be considered.

Figure 11.5 presents a schematic of the receiver array. Each antenna element is provided with a polarizer to separate the two circular polarizations into two channels, each of which requires its own receiver chain. The down-converted signals of all array elements with the same polarization are combined in the baseband. The local oscillator (LO) signal is generated and distributed to each receiver at 18.5 GHz to minimize losses. Beam-steering is established through phase shifters in each LO path. On-Chip frequency quadruplers (X4) generate the required 74 GHz LO signals. The intermediate frequency (IF) signals from all channels are collected in two power combiner networks covering the whole 1-to-36 GHz band and then digitized. The two analog-to-digital-converters (ADC) are clocked by the 74 GHz LO signal.

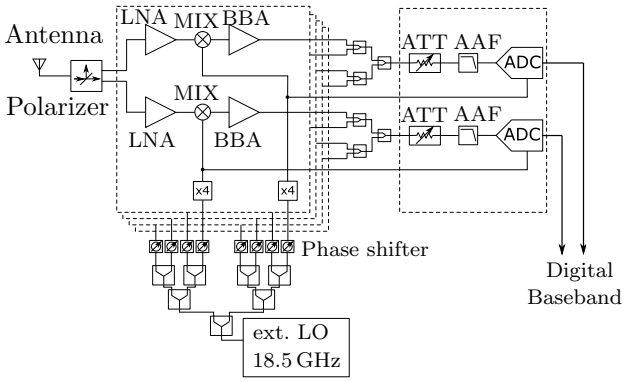


Figure 11.5
Schematic of the receiver with dual-polarized array antennas, an IF power combiner chain, and the ADC.

Figure 11.6 shows the receiver assembly. The antennas and the polarizers are waveguide components. A waveguide-to-microstrip transition is needed to connect the chip. The project DataRace aims at a full W-band single chip receiver for two polarizations. This is possible thanks to the CMOS technology which allows integration of digital and analog circuits on the same chip. This is especially useful for a single element receiver without power combining network.

All microwave circuits on the chip are envisaged as balanced circuits to be

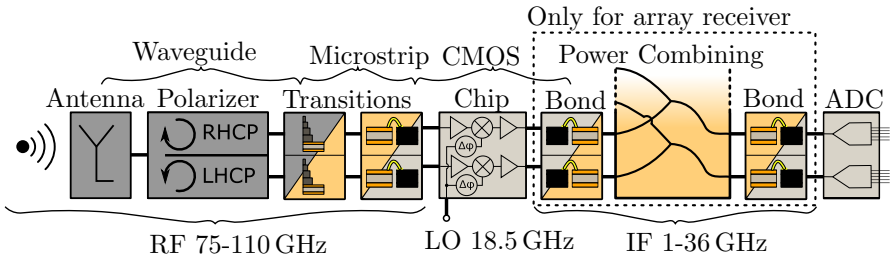


Figure 11.6
Building blocks of the receiver. The power combining network is only required for the receiver arrayand not for a single element receiver.

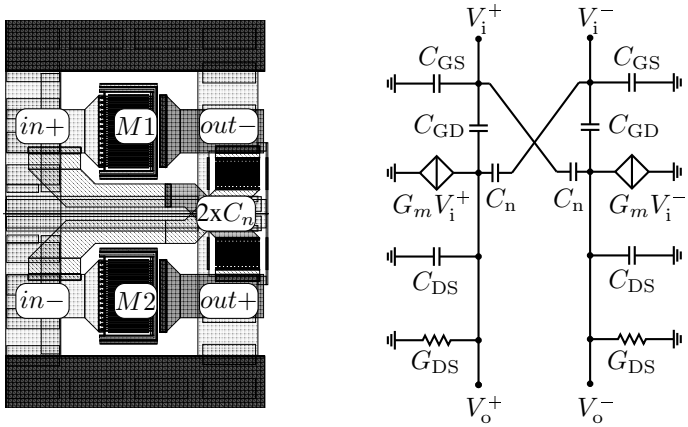
immune to poor source resistances. Furthermore, less bypass capacitance is needed which lowers the consumed chip area. All circuits must operate with a single supply voltage to ease the antenna integration and realize a system-in-package receiver.

11.3.1 Full W-Band CMOS PA

One of the difficulties in designing CMOS PAs at millimeter-wave frequencies is to minimize the destructive effect of parasitic elements on the PA's performance. Especially C_{GD} causes very low reverse isolation and thus lower gain and worse stability. The problem is even more critical for PAs because the transistors are normally very large, such that C_{GD} is also enormous. Therefore, capacitive cross-coupling neutralization is employed to mitigate the effect of C_{GD}. Figure 11.7 illustrates the differential PA core with capacitive cross-coupling neutralization. The cross-coupling capacitors C_{n} connected between the gate and the drain of the opposite transistor act as $-C_{\mathrm{n}}$ and thus can neutralize the effect of C_{GD}. This effect is analytically clarified in [422].

The PA core after neutralization is depicted in Fig. 11.7. Several neutralized PA cores with different transistor dimensions are taken for load-pull simulation in order to determine the PA core with maximum P_{out}. In Fig. 11.8 the maximum P_{out} of different PA cores are shown. It turns out that a PA core with a gate-finger-width W_{F} of 3 µm and 30 gate-fingers delivers the highest output power and is thus further used for the PA output stage.

Figure 11.9 shows the PAE and P_{out} contours in the Smith chart for 80 GHz and 105 GHz which are both close to the corners of W-Band. Fortunately, the optimum load impedances for maximum P_{out} and maximum PAE for both edge frequencies are close together in the Smith chart. Due to the fact that the technology does not provide high-Q capacitors, a transformer is used in order to provide DC-blocking to the load. The resulting load impedance (Z_{load}) at the input of the matching network is plotted in the Smith charts of Fig. 11.9. The upper end of the plotted Z_{load} is related to the lower end of the frequency



(a) (b)

Figure 11.7
(a) Layout of the PA core after neutralization with C_n. (b) Small-signal equivalent circuit. From [423] © 2017 DeGruyter

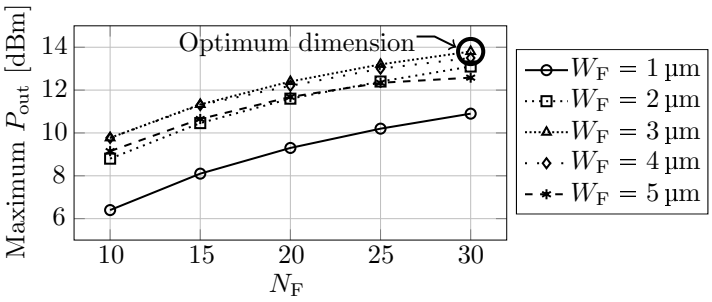


Figure 11.8
Simulation of the maximum P_out of several PA core combinations (W_F, N_F) at 105 GHz. From [423] © 2017 DeGruyter

range from 75 GHz to 110 GHz. Figure 11.10 shows on the left the overall implemented four stage differential PA. The input signal is transformed from single-ended to differential-ended by an on-chip Guanella-transformer (GN). This is followed by three gain-optimized amplifier stages. In order to minimize the losses in the PA power stage, the final transistor is transformer-coupled at the input and output.

The circuit is fabricated in 40 nm CMOS technology with a BEoL (Back-End-of-Line) process of five thin 150 nm and two medium thick 850 nm metals as top layers. A micrograph of the fabricated chip is depicted on the right in Fig. 11.10.

The small-signal gain is illustrated in Fig. 11.11a. From 80 GHz until

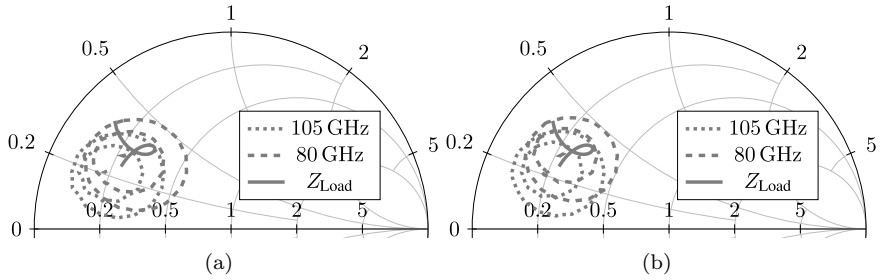


Figure 11.9
Loadpull simulation of PA core with $W_{\text{F}} = 3\,\mu\text{m}$, and $N_{\text{F}} = 30$. (a) P_{out} contours for 80 GHz (12 dBm, 11.5 dBm, 11 dBm) and 105 GHz (12 dBm, 11.5 dBm, 11 dBm). (b) PAE contours for 80 GHz (23 %, 20 %, 18 %) and 105 GHz (16 %, 14 %, 11 %).

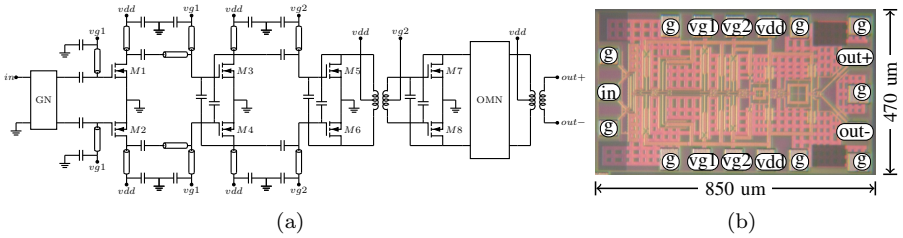


Figure 11.10
(a) Simplified schematic of the overall PA implementation. (b) Micrograph of the fabricated PA chip. From [423] © 2017 DeGruyter

105 GHz the measurements show around 18 dB of gain with a ripple of less than ±1 dB. The measured 3-dB bandwidth is around 30 GHz between 76 GHz and 106 GHz and is in good agreement with simulated S_{21}. The input and output reflection coefficients with measured and simulated data are plotted in Fig. 11.11b. The measured S_{11} remains below −8 dB over the frequency range. It has significantly smaller notches compared to the simulated S_{11} which is not completely understood so far. The measured and simulated S_{22} show values of less than −10 dB over the frequency range. Here, simulation and measurements show an acceptable agreement. Table 11.3 summarizes the performance of the realized PA and moreover compares it to recently published CMOS PAs.

This work shows a good trade-off with respect to P_{out}, BW, and PAE compared to related work of broadband CMOS millimeter-wave PAs. The covered area is larger compared to [424] and [425]. This is due to fact that this work provides a larger bandwidth which requires usually more area consuming matching elements. Due to the fact that only a few W-Band broadband CMOS

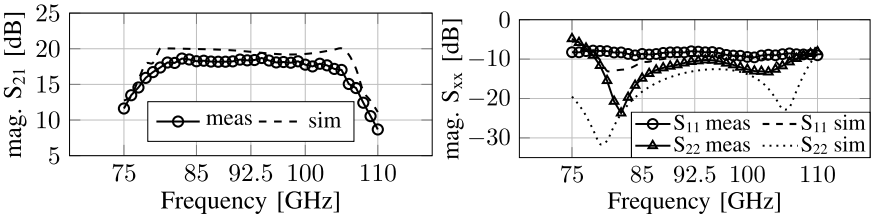


Figure 11.11
(a) Measured and simulated small-signal gain S_{21} over the W-Band. (b) Measured and simulated input and output reflection over the W-Band. From [423] © 2017 DeGruyter

Table 11.3
Performance of comparable state-of-the-art CMOS PAs. From [423] © 2017 DeGruyter

#	Tech [nm]	f_c [GHz]	S_{21} [dB]	BW [GHz]	P_{out} [dBm]	PAE [%]	P_{dc} [mW]	Size [mm^2]
[424]	40	77.8	15.2	15.2	21	20	375	0.19
[425]	65	92.5	12	27	14.8	8.7	n.a.	0.28
[426]	65	93.5	18	33	14	4.5	576	0.57
This work	40	91	18	30	>10	>10	130	0.40

PAs have been published so far, this work is a contribution to this recent field of research.

11.3.2 Antennas and Polarizer

The transmitted signals are received by dual polarized horn antennas. The two circular polarizations are separated by a septum polarizer. This chapter first describes the used septum polarizer with a triangular common port followed by horn antennas with triangular waveguide feed.

11.3.2.1 Advanced Septum Polarizer

Turnstile orthomode transducers allow to discriminate the two polarizations over a large bandwidth [427]. However, even compact realizations [428] are not suited to feed closely spaced array antennas. Septum polarizers, on the other hand, allow for array spacings in the order of the wavelength and have a low structural complexity [429, 430]. This comes at the expense of a rather narrow operating bandwidth.

Generally, the usable frequency band is bound by the cutoff frequencies of

the fundamental and the next higher order mode [431]. Propagating higher order modes affect the polarizer performance. In order to cover the entire W-band with a bandwidth of 37.8 %, the interval between fundamental and higher order mode cutoff is increased by using a triangular waveguide [432]. As depicted in Fig. 11.12 the usable relative bandwidth (URBW) between fundamental and higher order mode cutoff is significantly increased for triangularly shaped waveguides. Commonly square and circular waveguides are used for septum polarizers. Since a certain distance towards fundamental and higher order cutoff is required, the achievable bandwidth is 30 % for square and 25 % for circular waveguides. Using triangular waveguides a bandwidth up to 50 % is possible.

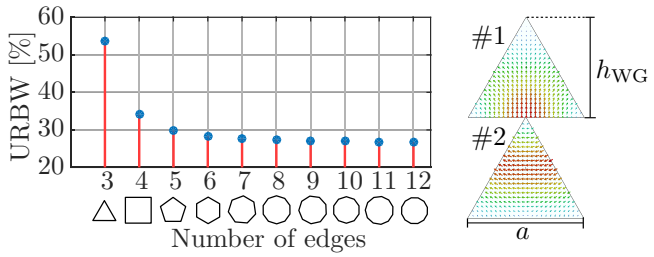


Figure 11.12
Left: Bandwidth for waveguides of different cross sections. Right: Electrical field of fundamental vertical (#1) and horizontal mode (#2) in an equilateral triangular waveguide. From [432] © 2019 IEEE

Quad-ridged waveguides were investigated, too. However they do not solve the fundamental problem of higher order propagating modes. Despite using special symmetries which are hard to implement in an array there is no advantage in bandwidth.

The electrical field distribution of the two fundamental modes in an equilateral triangular waveguide is shown in Fig. 11.12. Because of the predominant orientation of their electrical field, the first and the second mode are labeled vertical and horizontal, respectively.

To construct a septum polarizer, two single-moded waveguides are separated by a septum, which is stepwise removed towards a common dual-mode waveguide. The design goal is an equal amplitude of the two fundamental modes, a phase difference of 90° as well as low reflections and coupling. The impact of the two possibilities for the placement of a septum are analyzed in Fig. 11.13. Two important observations can be made. First, the green marked design space for the septum height h is wider when it is connected to the base. Second, within the design space, the difference in cutoff frequencies and in turn the difference in propagation constants of the two fundamental modes is much larger for the base connected septum. This is important since the different propagation constants ease achieving a 90° phase difference for the

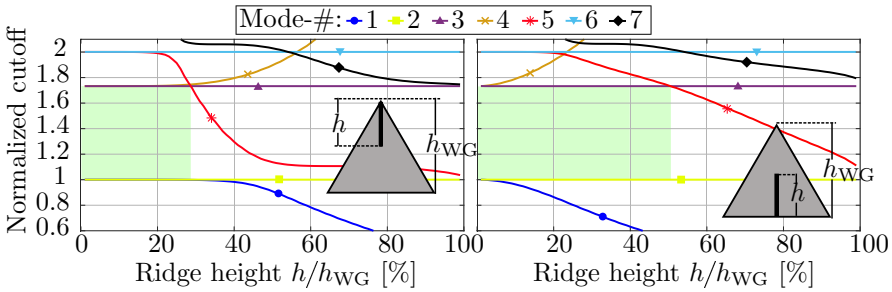


Figure 11.13
Mode spectrum of triangular waveguide with infinitesimally thin ridge connected to a corner (left) and a base (right). Green areas mark dual-mode operation regions for 53.5 % bandwidth. The modes are numbered according to their cutoff frequency in a waveguide without ridge. From [432] © 2019 IEEE

two modes by designing the step lengths properly. Thus the base connection is the preferred choice.

To ease interfacing with other components (e.g. Section 11.3.3.1) the two single-moded feed waveguides are standard WR10. A stepwise transition from rectangular to triangular cross-section is integrated into the septum polarizer, as shown in Fig. 11.14a. The triangular waveguide has a height h_{WG} of 2.54 mm to match the WR10 standard. The resulting cutoff frequencies for the fundamental modes and the next higher order mode are 68.1 GHz and 118 GHz, respectively.

The exact design parameters are obtained by constrained optimization using *CST Studio* and can be found in [432]. The goal is to minimize the axial ratio as well as reflection and coupling coefficients.

The simulation reveals an axial ratio of less than 0.8 dB as well as input reflections and coupling below −15 dB over the whole W-band. To verify the simulated performance the polarizer is manufactured using conventional machining in aluminum as a three part split block. The split block design and the realized parts are shown in Fig. 11.14(b) and (c).

The experimental characterization follows the procedure described in [433]. A *Agilent PNA E8361A* network analyzer with W-Band extensions is used for the measurements. The sinlge mode input ports are numbered ① and ② and the two electrical ports at the common port corresponding to the horizontal and vertical mode ③ and ④. Figure 11.15 reports the measured reflection and coupling coefficients as well as the axial ratio of the circular polarized field at the common port. The measured isolation of the two input ports is better than 17 dB and the return loss exceeds 15 dB over the entire W-Band. Compared to the simulation a good agreement is observed. The frequency dependence of the axial ratio is similar to the simulation. However, the maximum value of 1.3 dB is slightly higher than the simulated 0.8 dB.

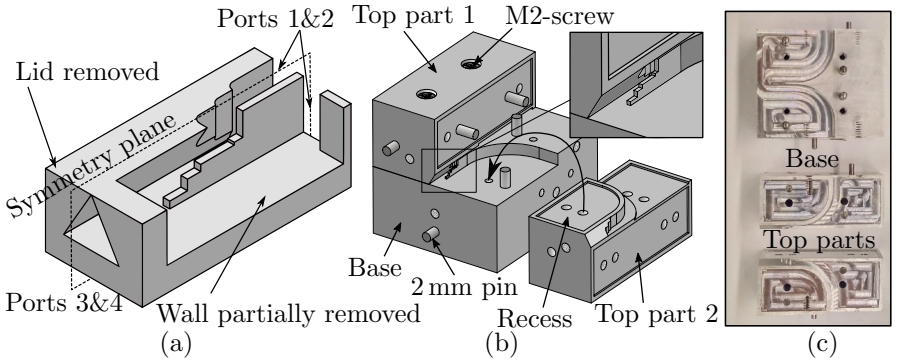


Figure 11.14
(a) Detail view of the designed polarizer model used for simulations. (b) Sketch of the designed split block aluminum polarizer with detail view of the septum. (c) Realized parts made of aluminum blocks. From [432] © 2019 IEEE

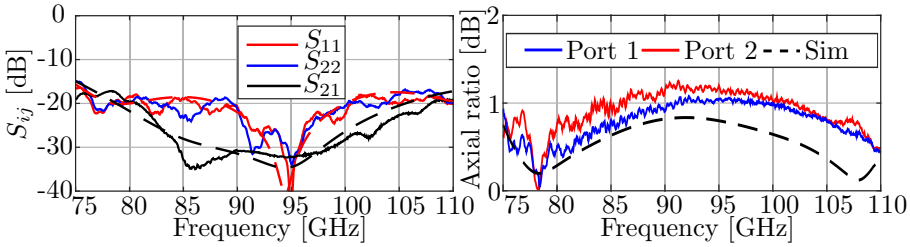


Figure 11.15
Measured (—) and simulated (- - -) reflection coefficients (S_{11}, S_{22}), coupling coefficient (S_{21}) and axial ratio (right). From [432] © 2019 IEEE

As the polarizer is a quite complex structure, it is challenging to achieve the required accuracy with conventional machining like milling. Therefore, the goal is to realize it as a system-in-package by means of advanced polymer 3D printing and metalization. In [432], a frequency scaled version of the polarizer is already realized with a commercially available 3D printer.

11.3.2.2 Horn Antennas with Triangular Feed

The polarizer requires horn antennas with triangular waveguide feed. This cross-section has to be tapered to realize the desired aperture, the shape and the size of which have to be optimized for each of the three application scenarios in Table 11.1. This is part of ongoing research and has yet to be finalized.

11.3.3 Transitions

The receiver integration requires two major transitions. The first one interface the polarizer waveguide and the microstrip line. The second one is needed between the microstrip line and the CMOS chip.

11.3.3.1 Vertical Waveguide-to-Microstrip Transition

For the receiver a tile architecture is chosen. Thus, a vertical connection of waveguide and microstrip line has to be designed. Since the CMOS receiver chip in its final form has differential RF inputs, a differential waveguide-to-microstrip transition ist needed. Known solutions feature a quarter wavelength backside cavity or offer only a narrow bandwidth [434, 435, 436, 437]. The cavity strongly limits the design space, especially for multilayer printed circuit boards (PCB), as needed here the power combining network (Section 11.3.9). The proposed design without cavity offers broadband performance and an intact ground plane. This is achieved by introducing ridges in the waveguide, so that the electrical field of the fundamental waveguide mode is confined between the two ridges and excites the differential mode on the microstrip line. The symmetry prevents common mode excitation.

The transition [438] is shown in Fig. 11.16 with its symmetry plane. Broad-

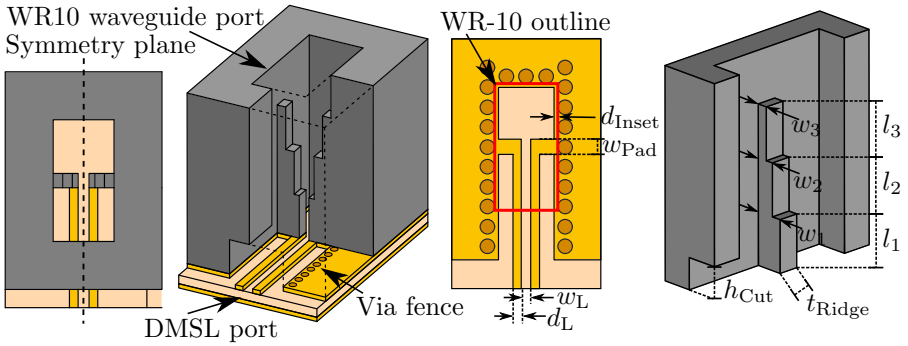


Figure 11.16
Different views on the transition and parameters describing the geometry. The waveguide wall is partially removed for better visibility of the ridges. From [438] © 2019 IEEE

band performance is obtained by stepwise tapering the ridges. Three steps turn out to be a good compromise between size and performance. The ridges match adequately shaped contact pads on the PCB. The contact region is surrounded by a via fence to minimize leakage into the substrate. To avoid shorting the microstrip lines the waveguide is provided with a feedthrough. The geometrical parameters of the transition shown on the right in Fig. 11.16 are preset by a Chebyshev approach and refined by constrained optimization

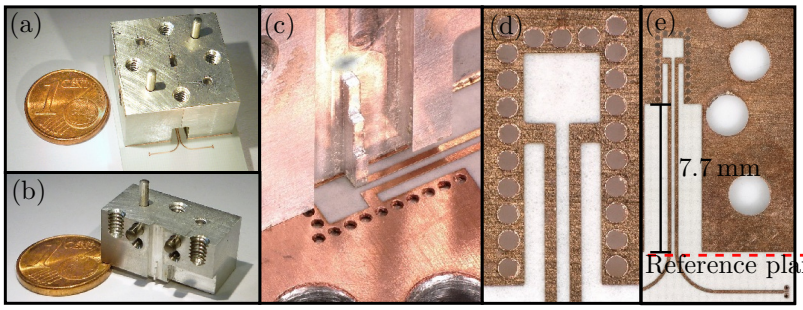


Figure 11.17
Photographs of the manufactured transition and Eurocent for scale. (a) Transition with PCB mounted, (b) waveguide component with ridge, (c) detail view on transition with only one half waveguide mounted, (d) closeup-view of the PCB top side, (e) reference plane used in the measurements indicating a 7.7 mm distance to the transition core. From [438] © 2019 IEEE

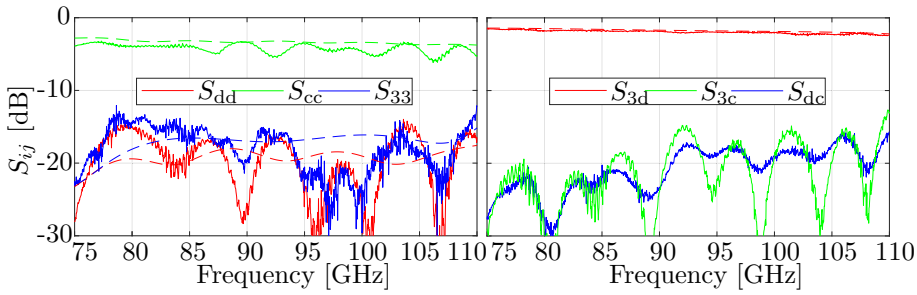


Figure 11.18
Measured (—) and simulated (- - -) modal reflection coefficients (left) and modal transmission parameters (right). From [438] © 2019 IEEE

in *CST Studio Suite*. The landing pad for the ridges is shorted by the via fence. To transform the short to an open in the region between the ridges the starting value for w_1 is a quarter wavelength at the center frequency.

The proposed approach yields a simulated return loss in excess of 15 dB for both the differential and the waveguide port.

The manufactured transition shown in Fig. 11.17 is composed of a 100 µm thick *Rogers 4350B* substrate structured with standard lithographic processes and a two part aluminum split block.

The transition is characterized according to [439] with an *Agilent PNA E8361A* and W-band millimeter wave extensions on a manual probe station. The measured reflection coefficients are given in Fig. 11.18 (left). The two ports of interest are those of the waveguide (3) and of the differential mode on the MSL (d). Both exhibit a return loss better than 13 dB. In the-

ory, the common mode (c) is completely reflected because it can only excite a mode below cutoff in the waveguide.

The modal transmission coefficients in Fig. 11.18 (right) confirm the predicted performance of the transition. The transmission from the differential MSL to the waveguide port is between 1.5 dB and 2.4 dB over the entire W-band. The 7.7 mm long line between the reference plane and the actual transition causes a loss of approximately 1 dB. The measured cross-mode transmission is below −15 dB. In simulation it is zero due to symmetry.

11.3.3.2 Microstrip-to-Chip Transition

A transition is needed to connect the CMOS chip and the MSL. Conventional wire-bonding is used for DC and low frequency interconnects and flip-chip for high frequency connections. The advantages of the former are the good thermal connection to the substrate and the possibility to visually inspect the active chip area and the bonds. This is handy for prototype designs. However, at high frequencies the bond wires introduce a large parasitic reactance, the compensation of which narrows the bandwidth [440]. Flip-chip on the other hand offers wideband performance beyond 100 GHz [441]. Drawbacks are proximity effects, mechanical instability, and difficult heat dissipation.

The transition proposed in Fig. 11.19 combines the advantages of both approaches [442]. An RF-chip is mounted in a cavity on a PCB. Wire-bonds are used to connect the DC and low-frequency pads. For the RF interconnect, a so-called flip-line is used. It consists of a coplanar line section without ground plane shaped to match the pads on the chip and on the PCB. The dimensions

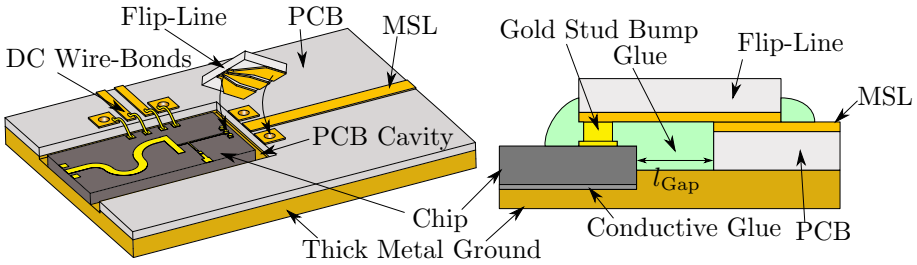


Figure 11.19
Left: 3D view of the proposed transition. The thermally curable glue used to mount the flip-line is not shown. Right: Cross-section of the flip-line interconnect. From [442] © 2020 IEEE

of the flip-line are chosen such that it features a line impedance of approximately 50 Ω. Thus, in contrast to wire-bonds, the length of the interconnect does not affect the performance much. The manufacturing is executed as follows. First the chip is glued into a cavity in the PCB. Gold stud bumps are placed on the chip pads. By precisely controlling the cavity depth the bumps and the PCB pads are at the same height. Next, a thermally curable, non-

conductive glue is applied on the chip and the PCB pads as well as in the gap between both. While the glue is cured, the flip-line is pressed onto the contact pads such that the glue is squeezed away at the contact points. The glue does not only reinforce the interconnect, it also helps tuning the line impedance of the flip line to match 50 Ω due to its permittivity. Figure 11.19 on the right shows the cross section of the established interconnect.

The proposed approach is demonstrated with a CMOS chip mounted on a *Rogers 4350B* PCB. Figure 11.20 shows in (a) and (b) the prepared chip with stud bumps glued on the PCB. The flip-line is depicted in (c) before and in (d) after mounting. The gap between the chip and the PCB is approximately 50 µm wide.

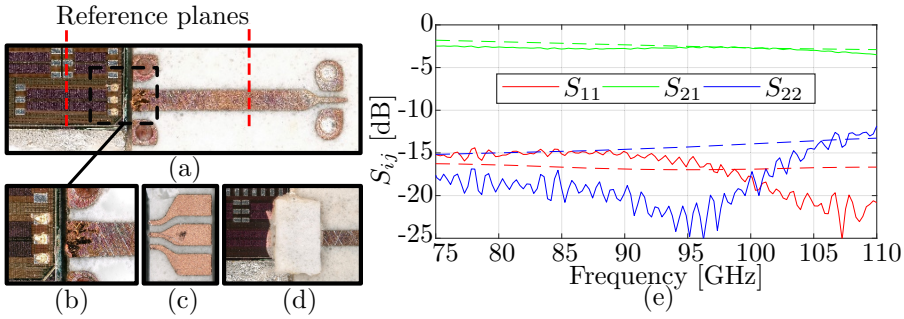


Figure 11.20
Flip-line transition before and after assembly. (a) The chip with stud bumps and line glued in place. (b) Enlarged view on the stud-bumps. Flip-line segment (c) before and (d) after mounting. (e) Measurement response. From [442] © 2020 IEEE

The measured scattering parameters are reported in Fig. 11.20 (e). The insertion loss is between 2.4 dB and 3.4 dB over the entire W-band. Uncertainties regarding the surface roughness and other material parameters as well as manufacturing tolerances explain the deviation between simulation and measurements. The return loss at the chip side (S_{11}) exceeds 14 dB and on the PCB side 12 dB. This is well in agreement with simulation.

11.3.4 Low-Noise Amplifier

The low-noise amplifier (LNA) must have gain and low noise figure (NF) in the W-band from 75 GHz to 110 GHz. For lowest noise figure, the common source (CS) topology is chosen. In the cascode topology an inductance is introduced between the cascode transistors to reduce the NF. However, this only works for narrowband designs and is therefore not applicable for a full W-band LNA [443].

As the design is balanced, the neutralization technique is applied to improve stability and gain of the CS amplifier. Two transistors with neutraliza-

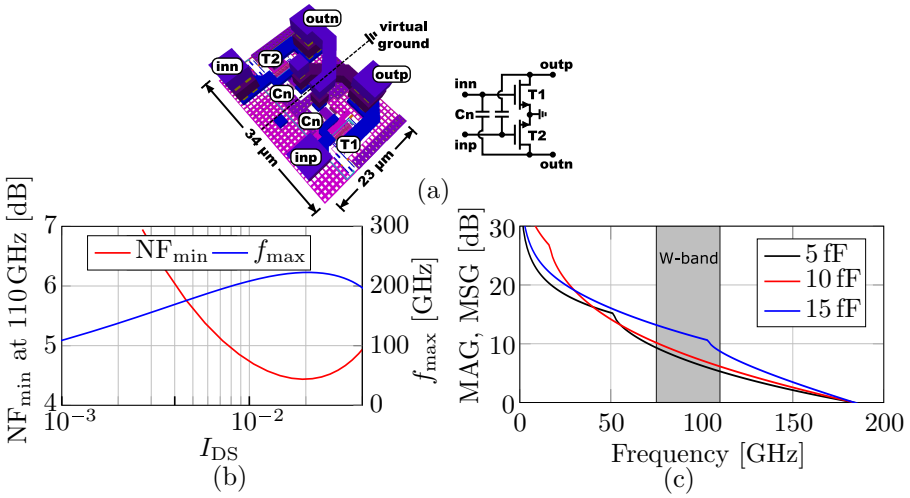
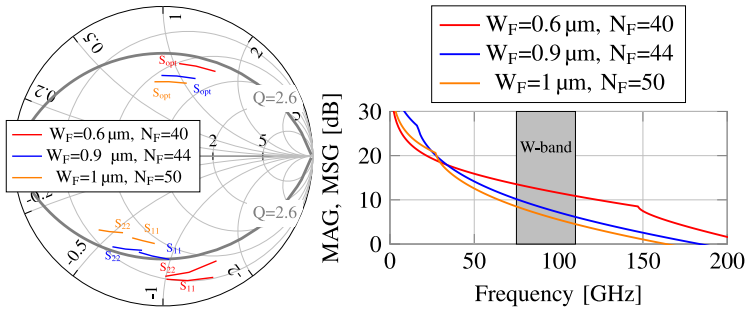


Figure 11.21
(a) 3-dimensional layout and schematic of the neutralized active core. (b) NFmin and f_{max} versus drain current. (c) Impact of the neutralization on stability and gain.

tion capacitances forming the so-called active core have to be optimized for high f_T, f_{max}, and low noise. Figure 11.21(a) depicts the symmetric layout of the active core. The layout uses a two metal layer ground lattice for lowest source resistance and lowest source inductance. All terminals are routed to the ultra-thick top metal layer, so that the active core can be directly connected to passive matching devices. In Fig. 11.21(b), f_{max} and NFmin are plotted versus the drain current. Fortunately, the optimum drain current with respect to noise corresponds to the maximum f_{max} for the active core. Fig. 11.21(c) depicts the maximum available gain (MAG) and maximum stable gain (MSG) for different neutralization capacitances. The 15 fF neutralization shows a high MSG in the W-band which has to be stabilized by an additional lossy device such as a resistor. The 5 fF and 10 fF neutralizations both lead to stable operation in the W-band, whereas the 10 fF has the higher MAG and is thus chosen. The impedances for in- and output, and the optimum noise source impedance must have quality factors smaller than

$$Q_{Imp} = \frac{f_{center}}{BW} = \frac{92.5\,GHz}{35\,GHz} \approx 2.6 \tag{11.1}$$

in order to satisfy the bandwidth requirement. In contrast, a larger transistor has a lower f_T and f_{max} and therefore may be unsuitable for W-band operation. For the LNA design, only minimum length transistors of 18 nm are considered. Degrees of freedom for the transistor are thus the number of gate-fingers (N_F) and the gate-finger width (W_F). Fig. 11.22 shows the



(a) (b)

Figure 11.22
(a) Input, output, and optimum noise source impedances of three different transistor sizes together with Q-circle of 2.6. (b) MAG/MSG of the three transistor sizes.

impedances and the corresponding MAG and MSG. A smaller transistor has higher MAG/MSG due to lower gate capacitances, as clearly seen in Fig. 11.22(b). The transistor with W_F=0.6µm and N_F=40 is not stable in the W-band. Furthermore, the input and output impedances are outside the Q-circle, which means that this transistor can not be matched over the full W-band. A transistor with W_F=1 µm and N_F=50 shows input and output impedances within the Q-circle but around 2 dB less gain than the transistor with W_F=0.9 µm and N_F=44. To achieve a minimum gain of 15 dB in the W band, the LNA must consist of at least three stages. The MAG roll-off in the W-band must be counteracted by frequency selective matching of LNA stages two and three such that a constant overall gain is realized over the W-band. The first stage output impedance is transformed independently of the source matching for low noise and is the source impedance for the second stage. The second stage is bilaterally matched by similar circuits according to the VSWR method discussed in [444]. Therefor, source and load impedance have to be transformed and presented to the second stage. This is why the bilateral matching of the third stage is done by the chosen load mismatch on a constant operating gain circle as explained in [444], which makes the input impedance transformable to be the load impedance to the second stage. The LNA stages are matched with a transmission line network, which is also reused as bias-T diplexer, as shown in the schematic of Fig. 11.23. The DC voltages are connected to the virtual ground nodes, so that no negative impact is expected when long metal wiring is connected to a voltage source. The LNA was fabricated in 22 nm FDSOI CMOS technology with two 3 µm thick copper layers. It occupies an active chip area of 0.35 mm^2 and a total chip area of 0.44 mm^2. The fabricated LNA chip is depicted at the bottom of Fig. 11.23.

As Fig. 11.24(a) shows, the LNA exhibits a simulated gain of 18 dB at 75 GHz and 17 dB at 110 GHz with 1 dB flatness over the W-band. The in-

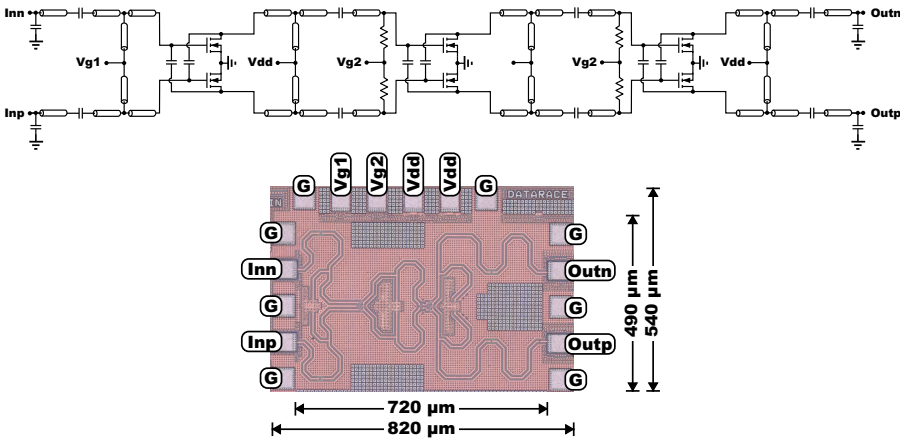


Figure 11.23
Top: Simplified schematic of the LNA. Bottom: Micrograph of the fabricated LNA chip.

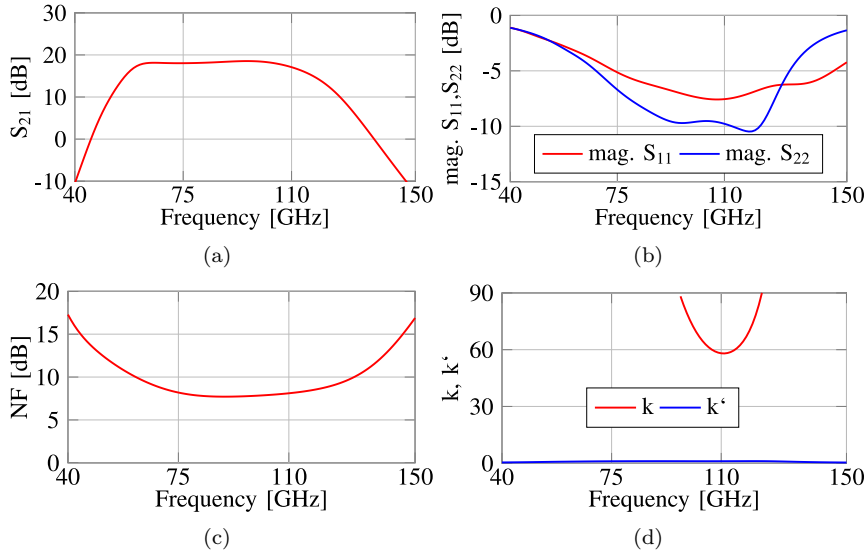


Figure 11.24
Simulated performance of the LNA.

and output matching exceeds 5 dB and the noise figure remains below 9 dB in the W-band, as reported in Fig. 11.24(b) and (c), respectively. Following the stability analysis according to Rollet, the k-factor stays above 1 and the sufficient condition k'¿0 is fulfilled in the entire W-band.

Table 11.4 summarizes the performance of comparable CMOS LNAs. This

Table 11.4
Performance of comparable state-of-the-art CMOS LNAs.

#	Tech [nm]	f_c [GHz]	S_{21} [dB]	BW [GHz]	Flatn [dB]	NF [dB]	P_{dc} [mW]	Size [mm^2]
[445]	28 FDSOI	85	12	64	4	6	38	0.46
[446]	65	99	13.7	22	3	9	45	0.29
This work	22 FDSOI	85	17-18	50	1	9	54	0.44

work is the only balanced design. It shows the highest gain and best gain flatness among the given references. The consumed chip area is comparable with the other wideband design [445].

11.3.5 Resistive Mixer

A mixer is a three-port circuit that employs a non-linear device to convert the RF frequency of 75 GHz to 110 GHz to the IF frequency of 1 GHz to 36 GHz. The non-linear device can be implemented either by varying the transconductance known as the active mixer or by varying the resistance known as a resistive mixer. Since an active mixer has transconductance it usually has less conversion loss than a resistive mixer. Drawback is the added noise of the active devices. A resistive mixer on the other hand uses transistors which are switched between low resistance and high resistance and are therefore fully passive. Matched passive circuits have a noise figure as high as their insertion loss. Phenomena that resistance mixers show higher noise than their insertion loss have been studied and can be explained by LO feedthrough [447]. Since the mixer is balanced at all ports the LO feedthrough can be drastically minimized by improving the symmetry in the circuit layout. In a three-port circuit dummy traces are introduced in order to balance the parasitic capacitances between all ports as shown in [448]. Figure 11.25(a) shows the balanced resistive mixer. The input is transformed to 100 Ω by the matching network consisting of transmission lines. Capacitors and a balanced inductor match the narrow-band LO-port to 100 Ω and are bias-T diplexers at the same time.

Figure 11.25(b) depicts the fabricated mixer chip. The total size of the chip is 0.53x0.49 mm^2. Figure 11.26 shows the results for the resistive mixer. The mixer has a conversion gain of around −8.5 dB over the full W-band with less than 1 dB gain variation. The noise figure is around 9 dB and varies by less than 1 dB over the W-band.

Table 11.5 summarizes comparable CMOS downconversion-mixers for W-band frequencies. The presented mixer exhibits the lowest conversion gain, which is due to the chosen passive approach with no power consumption. It should be noted that [449] evaluates the conversion gain with a fixed IF

Table 11.5
Performance of comparable state-of-the-art CMOS downconversion mixers.

#	Tech [nm]	RF_{in} [GHz]	P_{LO} [dBm]	ConvG [dB]	NF_{SSB} [dB]	P_{dc} [mW]	Size [mm^2]
[449]	65	74-98	5	4	13	n.a.	n.a.
[450]	65	74-78	4	-8	11.3	6	0.42
This work	22 FDSOI	75-110	4	-8.5	9	0	0.26

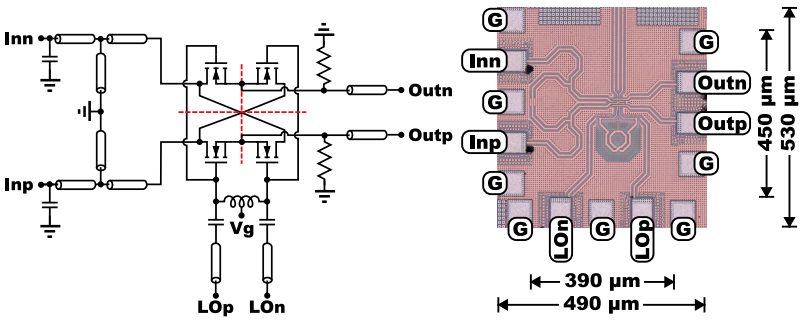
frequency of 1 GHz and includes IF amplification. The noise figure realized in this work is lower as no active devices with additional noise sources are used.

11.3.6 Truly Balanced LO Quadrupler

Minimizing the LO phase noise (PN) is extremely important because it degrades the sensitivity of the DataRace receiver. An empirical expression for PN, Leeson's equation [451], reads

$$L\left(f_{\mathrm{m}}\right) = 10\log\left[\frac{2kT}{P_{\mathrm{sig}}}\left(\frac{f_{\mathrm{c}}}{2Q_{\mathrm{L}}f_{\mathrm{m}}}\right)^{2}\right]. \tag{11.2}$$

With increasing frequency f_{c}, the low Q-factors Q_{L} of the resonator tank lead to an even larger phase noise in oscillator circuits. Therefore, multiplying a LO signal instead of fundamental LO generation is beneficial even though doubling will result in 6 dBc higher PN for instance. A comparison of recent fundamental phased-locked-loops proves this theoretical assumption [452]. In addition, LO distribution in a receiver array is simpler at lower frequency due to lower losses. For this reason, a balanced frequency quadrupler with high efficiency and output power is developed for the DataRace receiver.



(a) (b)

Figure 11.25
Simplified schematic (a) and micrograph of the fabricated mixer chip (b).

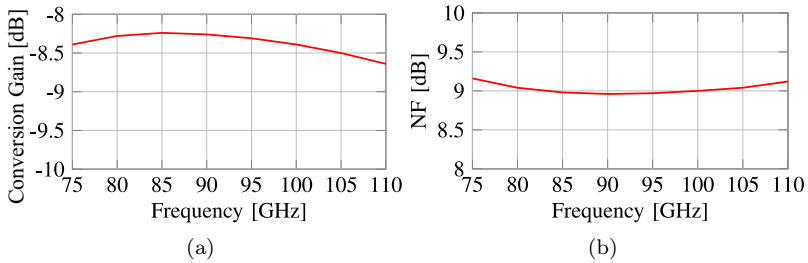


Figure 11.26
Simulated results of the mixer.

Kucharski [453] reports a very efficient way of signal quadrupling by using a stacked Gilbert cell architecture. Due to the thin oxides in scaled CMOS processes, the supply voltages are so low that not more than two transistors can be stacked between the supply rails. Therefore, an approach like the stacked Gilbert cell is not applicable. In scaled CMOS, the signal quadrupling is realized by a cascade of two frequency doublers (FD). One FD concept is the CS circuit with matched second harmonic at the output while the input is matched for fundamental frequency. However, these doublers are unbalanced and show only fair fundamental rejection and output power lower than 0 dBm with low efficiency. Another way of frequency doubling is the usage of a Gilbert cell (GC) fed by two signals of equal frequency at its LO and RF port. This approach suffers from a DC offset at the output and an imbalance due to LO feedthrough. Doublers which appear most in literature are push-push (PP) doublers. PP doublers have been successfully demonstrated at various frequencies, technologies, and with high output power. A PP doubler is inherently balanced at the input and unbalanced at the output. If a balanced input and output is intended, one needs a transformer balun at the output forming a balanced output out of the unbalanced node. In this sense, the doubler is pseudo balanced since it incorporates an unbalanced node. The transformer balun introduces undesired losses.

A PP doubler can be extended to truly balanced operation by adding an identical PP doubler cell and two 3-dB quadrature couplers [454]. In order not to burden the chip area consumption, traditional $\lambda/4$-resonant couplers such as branch-line, or Lange couplers are not considered. Instead of coupled transmission lines the inductive coupling of a transformer is used. Figure 11.27(a) shows the lumped coupler used for the 37 GHz to 74 GHz truly balanced PP doubler design. The coupler for the 18.5 GHz to 37 GHz PP doubler is made similarly. It is a permutation of the one reported in [455]. The design uses a bifilar wound transformer to place the desired ports side by side and introduce less phase imbalance for additional wiring. Figure 11.27(b) shows the insertion loss and the phase difference of the coupler. It exhibits less than 1 dB excess loss and a amplitude imbalance of less than 0.3 dB at 37 GHz.

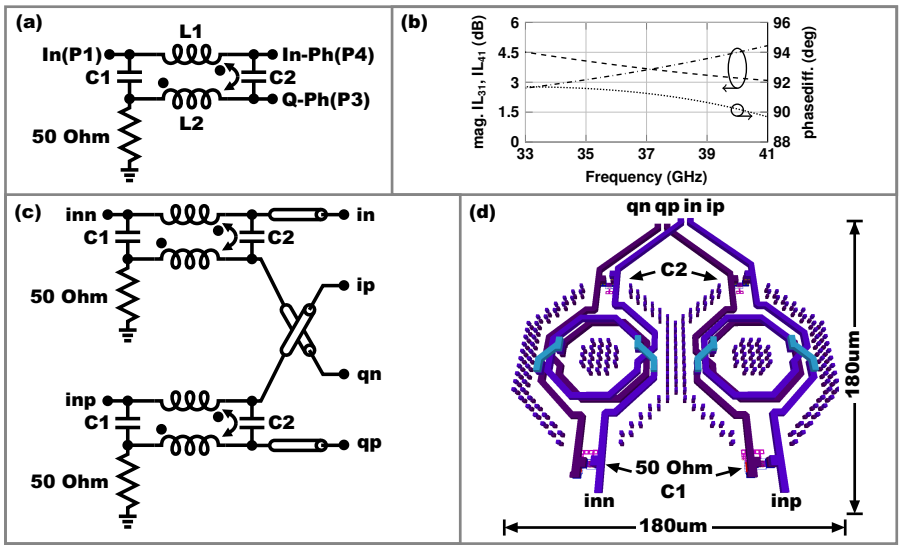


Figure 11.27
(a) Single quadrature coupler for the 37 GHz to 74 GHz truly balanced PP doubler. (b) Simulated insertion loss and phase difference. (c) Coupler network for PP doubler. (d) Layout of the coupler network.

The phase difference is as close as 1.2° to the desired 90° phase difference. Figure 11.27(c), (d) depict the network consisting of two identical couplers. Its size is 0.03 mm^2. The four output wires of same length are guided to the center reaching then the rather small active circuit part.

Figure 11.28(a) displays the active circuit part of the doubler. It consists of two equal PP doubler cells with PP pair and a common-gate transistor. The matching networks are made by balanced inductors instead of transformers, which generally results in lower losses. Figure 11.28(b) shows the layout of the active core. The devices and the wiring are meticulously symmetrical, so that almost no imbalance has to be filtered at the common-gate transistors. The device sizes are determined by a large set of harmonic load- and source-pull simulations and are summarized in Fig. 11.28(c). Figure 11.28(d) shows the P_{out} circles for the active core with and without common-gate transistor (stacked device) as well as the matching of input and output. The optimum load impedance Z_{lopt} is shifted with a common-gate transistor enabling matching by a simple L-section network of inductor and capacitor being simultaneously bias-T diplexer. Furthermore, the maximum P_{out} is increased from 3.2 dBm to 4.3 dBm, which is also underlined by the voltage signals at the summing node and drain node. The schematic of the quadrupler is depicted at the top of Fig. 11.29. It is a cascade of two truly balanced PP doublers. Figure 11.29 shows at the bottom the micrograph of the fabricated quadru-

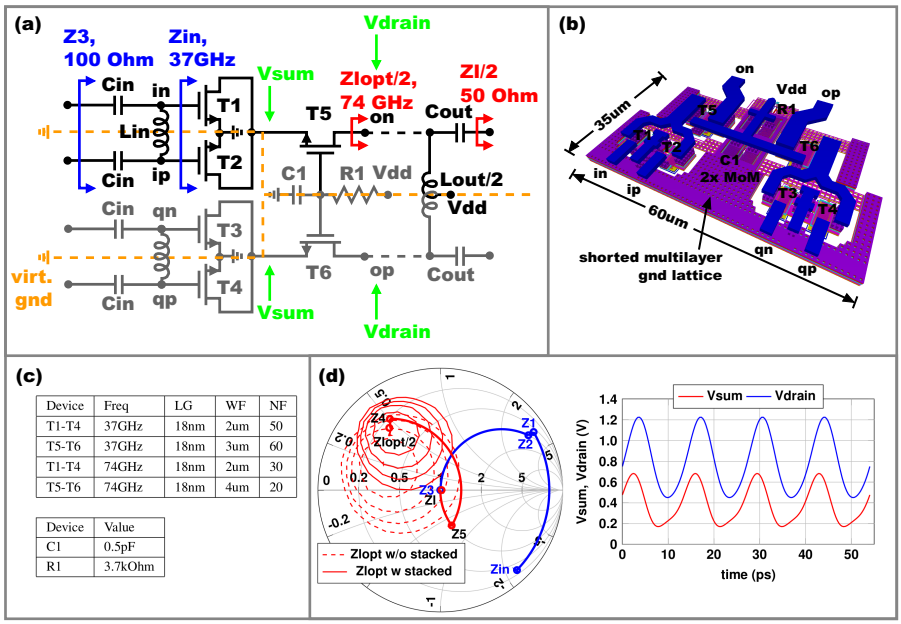


Figure 11.28
(a) Active circuit of the truly balanced PP doubler. (b) Layout of the active core. (c) Chosen device sizes for the active part. (d) Matching of the active core and voltages versus time.

pler chip. The active chip area is around 0.38 mm^2 while the total chip area including all pads is 0.54 mm^2. The quadrupler is characterized as a whole and laser-cutting of the doubler cascade is used to allow the comprehensive characterization of the individual doublers. Figure 11.30(a) shows the second harmonic output power $P_{\mathrm{out},2f_0}$ and the fundamental rejection F_{rej} of both doublers. The 18.5 GHz to 37 GHz doubler delivers around 3.1 dBm of output power at the targeted working point of 0 dBm input power. For the 37 GHz to 74 GHz doubler, the output provides around 5 dBm power at 5 dBm input power, which is the power delivered by the first doubler. Since most multipliers do not have power-added-efficiency (PAE), the multiplier performance metric is the total efficiency and reads

$$\eta_{\mathrm{total}} = \frac{P_{\mathrm{out},nf_0}}{P_{\mathrm{dc}} + P_{\mathrm{in},f_0}} \tag{11.3}$$

Figure 11.30(b) summarizes the DC power consumption and the total efficiency. The latter exceeds 8 % for both doublers at the targeted operating working points. As the doublers are tuned circuits the bandwidth is limited. Figure 11.30(c) shows the second harmonic output power at the chosen operating points versus frequency normalized to the desired output frequencies of

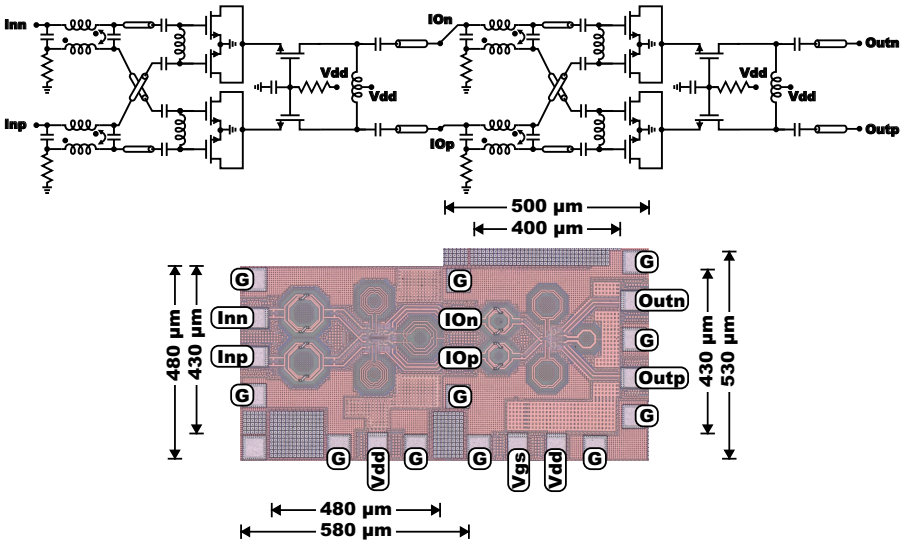


Figure 11.29
Top: Simplified schematic of the quadrupler. Bottom: Micrograph of the fabricated quadrupler chip.

Table 11.6
Performance of comparable state-of-the-art CMOS doublers.

#	Tech [nm]	$2f_0$ [GHz]	G [dB]	F_{rej} [dBc]	$P_{\text{out},2f_0}$ [dBm]	P_{dc} [mW]	η_{total} [%]	Size [mm^2]
[456]	90	46	-1.6	40	-1.6	11.5	5.5	0.63
This work	22 FDSOI	37	3.2	>40	3.2	26.4	7.6	0.21
[457]	65	77	1	19	-4	14	2.7	0.22
This work	22 FDSOI	74	-0.2	>50	4.8	29	9.3	0.17

37 GHz and 74 GHz, respectively. Both doublers exhibit a 3-dB-bandwidth in excess of 15 %. The cascade of both doublers shows a fourth harmonic output power of 3.7 dBm at 0 dBm input power and a total efficiency of more than 3 %, as depicted in Fig. 11.30(d). The fact, that the output power of the doubler cascade is lower compared to the individual doublers, is due to mismatch losses between the doublers.

Table 11.6 lists CMOS doublers for comparison. The 18.5 GHz to 37 GHz doubler shows high gain and second harmonic output power at fair dc power consumption and is thus well suited to be the first stage in a doubler cascade. As second stage, the 37 GHz to 74 GHz doubler has significantly higher output power, total efficiency, and lower chip area compared to [457]. Table 11.7

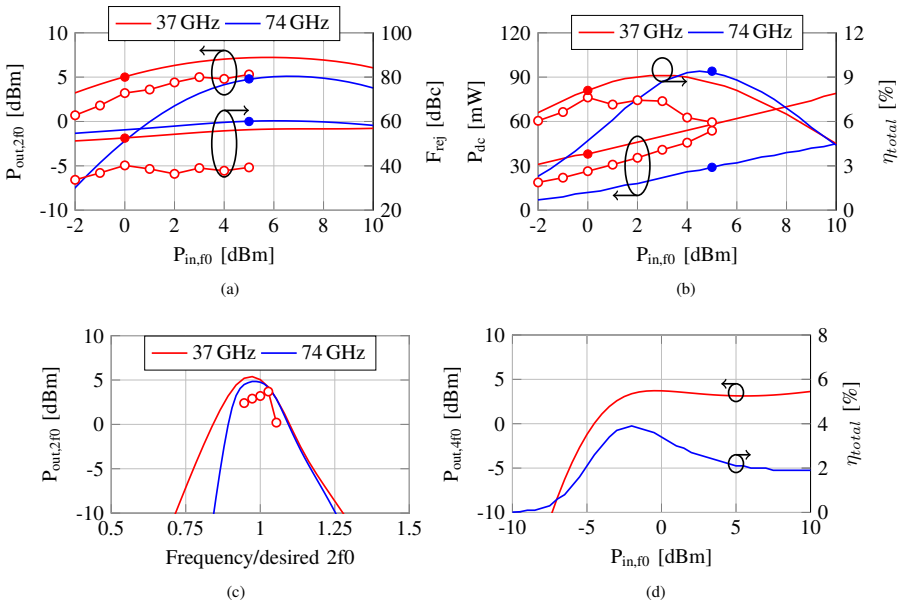


Figure 11.30
Simulated and measured performance of the quadrupler circuit. (a) 2nd harmonic output power $P_{\mathrm{out},2f_0}$ and fundamental rejection F_{rej}. (b) DC power consumption P_{dc} and total efficiency. (c) $P_{\mathrm{out},2f_0}$ versus normalized frequency. (d) 4th harmonic output power $P_{\mathrm{out},4f_0}$ and total efficiency of the quadrupler.

Table 11.7
Performance of comparable state-of-the-art CMOS quadruplers.

#	Tech [nm]	$4f_0$ [GHz]	G [dB]	F_{rej} [dBc]	$P_{\mathrm{out},2f_0}$ [dBm]	P_{dc} [mW]	η_{total} [%]	Size [mm^2]
[458]	90	66	2.3	27	2.3	53.4	3.1	0.34
[459]	65	85.5	-24.3	>30	-14.3	16	<<1	0.34
This work	22 FDSOI	74	3.7	>50	3.7	67	3.4	0.38

confirms the superiority of the proposed quadrupler. Compared to the other CMOS devices in W-band, it exhibits the highest gain, output power, and total efficiency.

11.3.7 Digital Phase-Shifter

To realize the desired beam-steering, the phase-shifters are placed in the LO path. The advantage is that the LO is operated at a low frequency and offers enough power. In addition, the phase-shifter losses do not impair the receiver

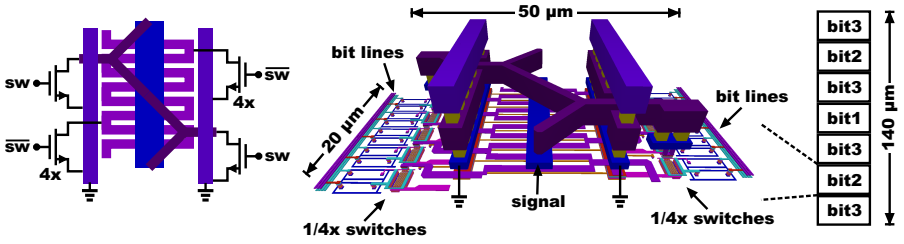


Figure 11.31
Single cell of the digital phase-shifter with three switches for patterned capacitances and one switch for inductance on each side.

path and the NF. An electronic phase-shifter can be made of a switchable LC-network. Here, the signal has to pass transistor switches which is always a source of non-linearities and losses. The 44 GHz implementation reported in [460] shows insertion loss of around 14 dB and makes therefore additional buffer amplifiers inevitable. Another solution uses tunable transmission lines as presented by [461]. If one considers the lossless telegrapher's equations the characteristic impedance Z_0 and the propagation constant β are

$$Z_0 = \sqrt{\frac{L}{C}}, \beta = \frac{1}{\sqrt{LC}}. \tag{11.4}$$

If L and C change by the same factor, Z_0 remains constant. In contrast, β changes, resulting in a phase-shift in a transmission line with constant physical length. Figure 11.31 shows a 20 µm long cell of the tunable transmission line implemented in 22 nm FDSOI. The switches on each side connect either the patterned capacitance (8 switches) or the inductance (2 switches) to ground. The switches with bit lines are at the outer edges such that they do not affect the mm-wave performance of the transmission line. For a 3-bit tunable transmission line the cell must be put in a chain with binary weighted coding as indicated, making it 140 µm long. In Fig. 11.32 reports the insertion loss and the phase shift of a 140 µm long 3-bit tunable transmission line. The high beta case shows 0.25 dB insertion loss and 39° phase shift at 74 GHz, the low beta case 0.32 dB and 33°. The loss of the high beta case is a higher due to the larger loss of the inductive part in the triangular wire. Table 11.8 summarizes the performance of tunable transmission line phase shifters. This work presents the lowest insertion loss and area consumption at the expense of limited phase tuning range.

11.3.8 Balanced Distributed Amplifier

Since the receiver chain provides only a small gain due to the conversion loss of the resistive mixer, an IF-frequency amplifier is essential for good overall receiver performance. The amplifier must offer gain and a low noise figure

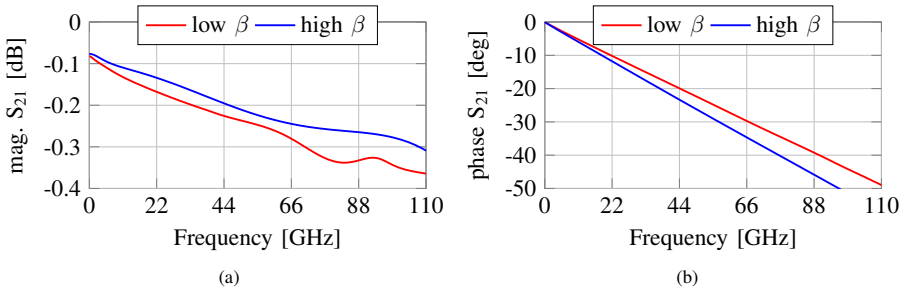


Figure 11.32
Simulated results of a 140 µm tunable transmission line.

Table 11.8
Performance of comparable state-of-the-art phase-shifers.

#	Tech [nm]	f_0 [GHz]	S_{21} [dB]	PShift [deg]	PShift/Loss [deg/dB]	Area [mm^2]
[462]	32 SOI	45	-7.6	-185	24.3	0.099
[461]	45 SOI	45	-3.3	-79	23.9	0.072
This work	22 FDSOI	45	-1.2	-24	20	0.042

from 1 GHz to 36 GHz, i.e., over a relative bandwidth of 190 %. That is why the amplifier is called baseband broadband amplifier (BBA). In general, the bandwidth of an amplifier is mostly limited by the gate and the drain capacitances, which together with the parasitic resistances form a low-pass filter. Amplifiers with 190 % relative bandwidth can only be made if the gate and the drain capacitaces are absorbed in an artificial transmission line, which yields a so-called distributed amplifier (DA).

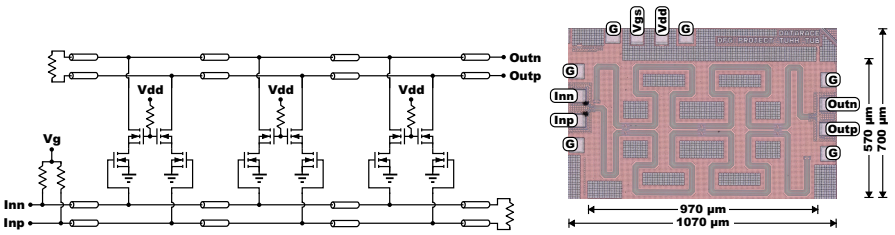


Figure 11.33
(a) Simplified schematic of the BBA. (b) Micrograph of the fabricated DA chip.

Figure 11.33 shows on the left the schematic of the BBA. The circuit uses three balanced cascode gain cells and differential transmission lines. Termina-

tions at the end of the transmission lines are made floating, so that no current occurs like in a shunt termination due to a bias voltage different from ground.

The micrograph of the fabricated BBA is shown on the right in Fig. 11.33. The chip consumes 0.7x1.07 mm^2 of total chip area including all pads. Figure 11.34 shows the simulated results for the BBA. It has more than 11.9 dB of gain from 0 GHz to 40 GHz with less than 2.5 dB of ripple. The return loss at in- and output is larger than 10 dB and the NF is around 5 dB in the band of interest. The Rollet stability analysis indicates that the circuit is stable as $k > 1$ and $k' > 0$. The group delay of the BBA is around 30 ps with less than 6 ps of ripple. Table 11.9 summarizes some state-of-the-art DA. This work reports the highest gain and gain-bandwidth-product (GBW) among the given references. The power consumption is fair and chip area is the largest. This is also due to the fact that this reports the only balanced DA in this comparison.

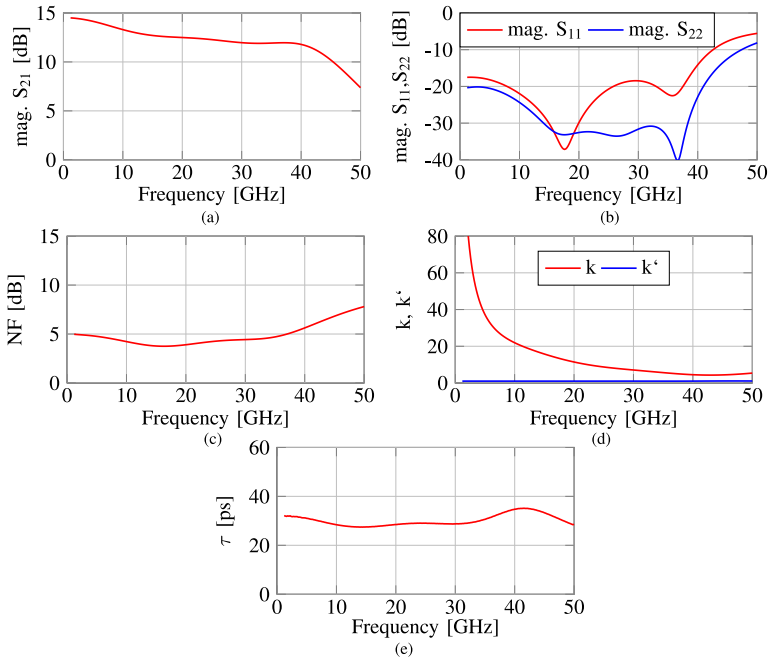


Figure 11.34
Simulated results of the BBA.

11.3.9 Power Combining Network

To ease scalability of the receiver array the power combining network is composed of several 2-to-1 combiners. The anticipated bandwidth the combining network needs to cover is the full IF-band from 1 GHz to 36 GHz. Single-ended power combiners covering almost that bandwidth have been demonstrated in

[465]. Since the CMOS chip output is differential the power combining network also needs to be differential. Such combiners can only be realized with the anticipated bandwidth on multilayer substrates because of the required signal crossings. The need for multilayer substrates also raises the demand for integrated resistors since regular SMD components need to be placed on a top or bottom layer, which reduces the design freedom significantly. Figure 11.35 shows on the left the manufacturing process and on the right an exemplary resistor made of carbon paste, which, without any restrictions, can be integrated in multilayer substrates. Such resistors can be manufactured in a batch

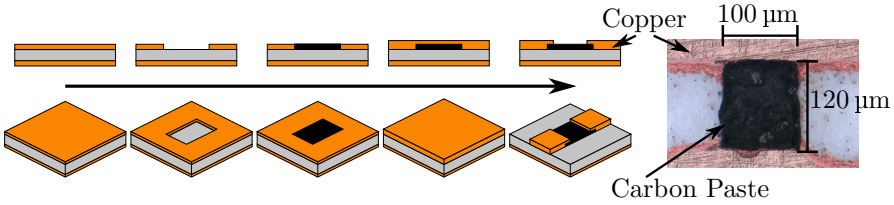


Figure 11.35
Manufacturing process of embedded carbon paste resistors (left) and exemplary resistor (right). From [466] © 2019 IEEE

process involving etching and galvanic plating. The resistance can be adjusted via the length to width ratio or by mixing isolating additives to the carbon paste. Using these resistors, the fully differential power combiner shown in Fig. 11.36 is designed [466]. It basically consists of two stacked single ended power combiners in a multilayer PCB. The in- and outputs are on the top layer. Via transitions distribute the signals to the inner layers. To compensate the different lengths of the vias the stripline of one of the differential conductors takes a detour.

The combiner is manufactured on *Rogers 4003C* and *Rogers 4450F* substrates and laminates. The carbon resistors are made with *Peters SD 2843 HAL* carbon paste. Coaxial connectors provide access to the the network analyzer. Calibration sets the reference planes shown in Fig. 11.37. The size of the power combiner core is only 8.5 mm x 5.8 mm. The measured performance for the differential mode of the power combiner is reported in Fig. 11.38. The

Table 11.9
Performance of comparable state-of-the-art distributed amplifiers.

#	Tech [nm]	BW [GHz]	G [dB]	GBW [GHz]	NF [dB]	P_{1dB} [dBm]	P_{dc} [mW]	Size [mm^2]
[463]	40	30	7	150	4	2	34	0.45
[464]	45 SOI	92	7.5	517	n.a.	n.a.	73.5	0.45
This work	22 FDSOI	40	11.9	620	5	n.a.	61.5	0.75

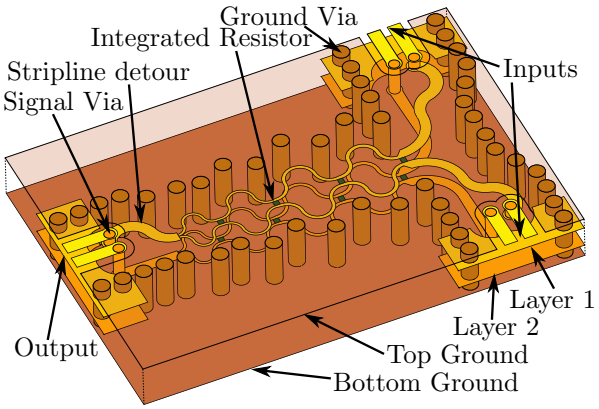


Figure 11.36
Fully differential 2-to-1 power combiner design. Copper layers are shown in different colors to enhance contrast. The dielectric is omitted and the top copper layer is transparent. From [466] © 2019 IEEE

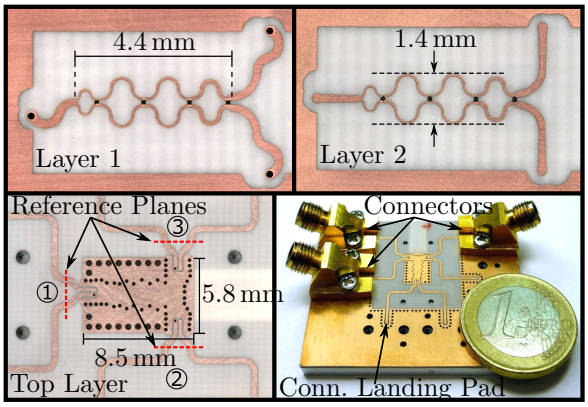


Figure 11.37
Manufactured power combiner. Pictures of layer 1 and layer 2 are taken prior to laminating the two substrates. From [466] © 2019 IEEE

return loss at all ports exceeds 10 dB from 1.5 GHz to 36.5 GHz. The transmission is better than −5.3 dB, which is close to the ideal value of −3 dB. The two input ports are isolated by more than 15 dB above 5 GHz. The complete measured scattering parameters are presented in [466]. As the structure shows only minor asymmetries, the differential-to-common mode suppression is high.

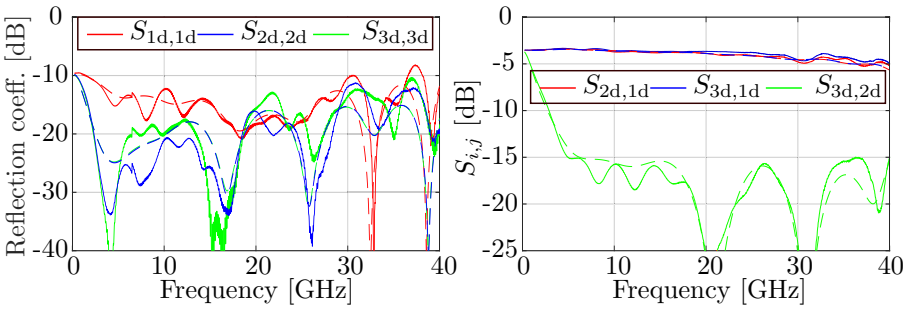


Figure 11.38
Measured performance (—) of the differential power combiner compared to the simulated performance (- - -). Port 1 is the combined output. Ports 2 and 3 are the inputs. The index d denotes the differential mode. From [466] © 2019 IEEE

11.3.10 Time-Interleaved Track-&-Hold

This section presents the design and implementation of an ultra-wideband (bandwidth > 40 GHz) track-and-hold (UWB T&H) with a sampling speed of 18.5 GS/s, which needs to be operated in a 4X-time-interleaved (4X-TI) architecture to get the target sampling rate of 74 GS/s for the ADC. The down-converted signal in the IF band has a bandwidth of 1-36 GHz. Hence, a sampling rate of 74 GS/s is chosen for the IF-to-digital converter. The ENOB target for the ADC including the UWB T&H and a 5-bit flash ADC is more than 4.5 bits. Since a resolution of 5 bits is considered for the ADC, an accuracy of better than 5.5 bits is targeted for the T&H to meet the ENOB target. Assuming a sampling rate of 74 GS/s for the IF-to-digital converter and 5-bit resolution, a receiver output data rate of 370 Gb/s is provided.

Sampling, as the first step in the A/D conversion, is a non-trivial task and the performance of the ADC is often limited by the SFDR or SNR of the front-end T&H specifically at high input frequencies. In order to avoid SFDR drop due to distortion caused by incomplete settling, a certain settling accuracy has to be obtained. This settling requirement correspondingly imposes a constraint on the time constant of the T&H (τ_{TH}). To get a $\leqslant$ LSB/2 settling error for n-bit resolution, the τ_{TH} and consequently $f_{3\,\mathrm{dB,TH}}$ are given by

$$\begin{aligned} e^{-t_s/\tau_{\mathrm{TH}}} &< \frac{1}{2^{n+1}} \\ \tau_{\mathrm{TH}} &< \frac{t_s}{(n+1)ln(2)} \\ f_{3\mathrm{dB,TH}} &= \frac{1}{2\pi\tau_{\mathrm{TH}}}. \end{aligned} \tag{11.5}$$

In Eq. (11.5), t_s is the available settling time for the T&H (acquisition time). Assuming 2/3 of the track phase is available as acquisition time, due to finite

rise and fall times as well as non-overlapping sampling clocks, a settling time of $t_s = \frac{2}{3} \times \frac{T_s}{2} \approx 18\,\text{ps}$ ($f_s = 18.5\,\text{GS/s}$) is available for a 4X-time-interleaved T&H. To meet a 5-bit settling accuracy according to Eq. (11.5), a lower bound is put on the bandwidth of the T&H, which is $f_{3\,\text{dB,TH}} > 40\,\text{GHz}$. Therefore, a bandwidth of higher than 40 GHz is targeted for the 4X-TI sampler. Using a smaller number of time-interleaved lanes increases the input analog bandwidth, makes the time-interleaved mismatch calibration easier and reduces the number of critical clocks. However, a 2X-TI with the same settling accuracy needs a minimum bandwidth of 80 GHz for each sampler due to higher sampling speed per lane (37 GS/s) (reduced acquisition time). Since such a high T&H bandwidth can not be achieved without violating the 5-bit SNR target, a 4X-TI T&H architecture, as depicted in Fig. 11.39, is considered. Each front-end sampling channel is followed by a 5-bit flash ADC to implement a 4X-TI flash ADC. A front-end buffer and a flash buffer, as depicted in Fig. 11.39, are used to reduce the source impedance and decouple the capacitive load of the flash comparator array from the T&H respectively. Apart from the bandwidth requirement, these buffers in the signal path need to meet the target SNDR over the entire Nyquist bandwidth of the 4X-TI ADC ($f_{\text{Nyq}} = 74\,\text{GHz}/2$). Therefore, an elaborated design of the buffers in the signal path proves essential. Two lanes share an input buffer as the clock phases of the respective ADCs are 180° apart from each other. Hence, the number of the required FE input buffers, as the main power consumer of the sampler (42 mW), is reduced to only two buffers saving 84 mW in the 4X-TI implementation. Moreover, the input capacitance of the ADC is reduced by half, which translates into higher input bandwidth resulting in less drive effort and power consumption for the PGA preceding the ADC.

The required quadrature phase clocks for the sampling switches ($\phi_0, ..., \phi_3$), as shown in Fig. 11.40, are generated by a sampling clock-phase generator. It takes a half rate sinusoidal signal ($f_{\text{in}} = 37\,\text{GHz}$) as input and a 2:1 CML frequency divider provides the clock buffers with an in-phase and a quadrature-phase ($V_{\text{I}}, V_{\text{Q}}$) differential signal at 18.5 GHz. The V_{I} and V_{Q} from the CML frequency divider are AC-coupled to the input of the clock buffers to enable common-mode voltage shift. To avoid second rank time interleaving for the ADC, the ADC conversion rate is chosen to be the same as the channel sampling speed ($f_s = 18.5\,\text{GS/s}$). Hence, a 5-bit flash ADC is used, which enables this conversion speed.

A low jitter clock path is a must for sampling at high input frequencies. Otherwise, jitter, as the dominant noise contributor, will limit the total SNR. There are three noise sources contributing to the total SNR in an ADC, which are quantization noise, thermal noise (kT/C) and clock jitter. The SNR due to clock jitter is given as

$$\text{SNR} = -20\log_{10}(2\pi f_{\text{in}}\sigma_{\text{j}}). \tag{11.6}$$

Where f_{in} is the frequency of the sinusoidal input applied to the T&H and σ_{j} is the standard deviation of the sampling clock periodic jitter. As the input

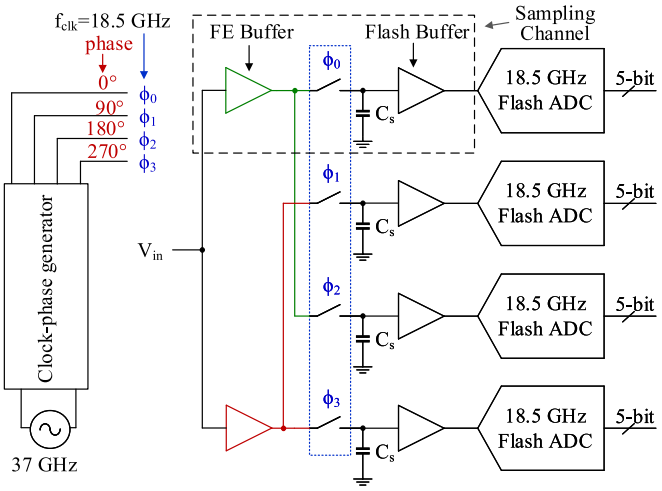


Figure 11.39
Block diagram of the 4X-TI flash with proposed sampling channels. From [467] © 2019 IEEE

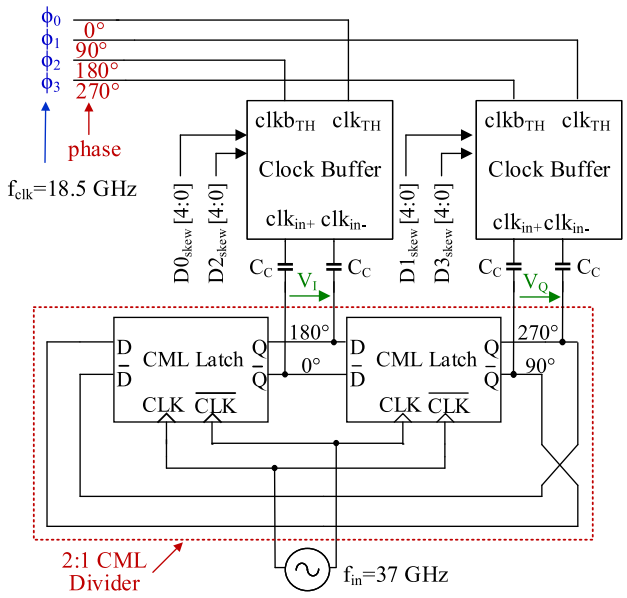


Figure 11.40
Block diagram of the clock-phase generator for the 4X-TI T&H.

frequency increases, the uncertainty of the sampling instant as a result of external or local jitter in the clock path reduces the SNR. Therefore, design of an

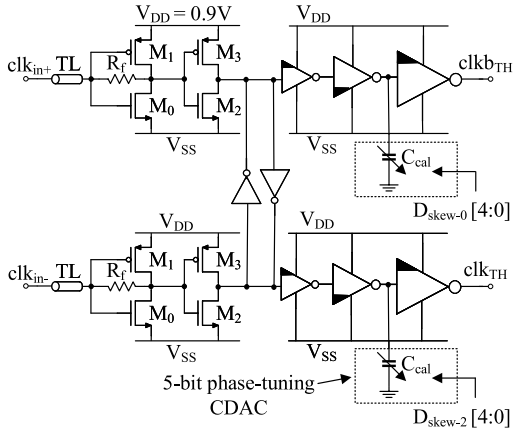


Figure 11.41
Schematic of the clock buffer. From [467] © 2019 IEEE

ultra low jitter clock buffer is crucial for this application ($f_{\mathrm{in-max}} = 37\,\mathrm{GHz}$) in order to reduce the ADC performance loss due to jitter. Schematic of the proposed ultra-low jitter clock buffer is depicted in Fig. 11.41. It uses a 0.9 V supply and converts a sinusoidal input, which is 1.8 $V_{\mathrm{p-p,diff}}$ to a differential clock required for two T&Hs. The transistors M_0 and M_1 form a CMOS amplifier, which is designed for an output DC common-mode voltage of 450 mV ($\frac{V_{\mathrm{DD}}}{2}$). It has a DC gain of 18 dB and a bandwidth of 30 GHz. The amplifier uses a self-biasing scheme employing the resistor R_{f} as a feedback resistor. The amplifier is designed to deliver a differential input impedance of 100 Ω over a frequency range of 18.5 GHz for RF-matching. The cross-coupled inverter sets the crossing point to approximately 450 mV, so that a phase shift of 180° between the complementary clock phases is achieved. The last three inverters are scaled with a fan out of 3 to drive the large sampling switch ($W = 30\,\mu\mathrm{m}$) and since the pMOS sampling switch samples the input on the rising edge, the last three inverters as emphasized in Fig. 11.41 are optimized for a sharp rising edge at the output. Therefore, the first and the last inverters are sized with sharp rising clock edges, while the middle one has fast falling edge. This way, supply and jitter noise effects as well as sample switch offset sensitivity are reduced. The sampling clocks ($\mathrm{clkb_{TH}}$ and $\mathrm{clk_{TH}}$), which can be used for a 2X-TI (TI channels at complementary clock phases) achieve a jitter of $\sigma_{\mathrm{j}} \approx 20\,\mathrm{fs}$ at TT corner, which is extracted from the transient simulation with transient noise and observing the spread of the sampling clock around the sampling point.

A detailed schematic of the track-and-hold building blocks is shown in Fig. 11.42. The input port is differentially 100 Ω-terminated to avoid any reflection. The output port is connected to the flash comparator array. However, this sampler is designed to be implemented within a test chip. Therefore, the

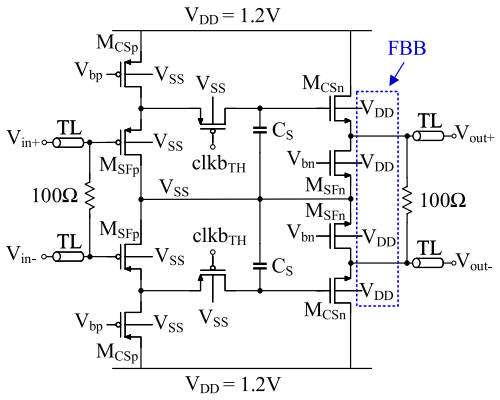


Figure 11.42
Schematic of the sampler with pMOS and nMOS source followers. From [467] © 2019 IEEE

output is also 100 Ω-terminated to match with the resistance of the probes. The FE or input buffer, which is a pMOS source follower (SF) provides a source resistance of 6 Ω and the flash output buffer decouples the load of the flash comparator array from the T&H. The use of two of those buffers guarantees a small enough time constant, which corresponds to a bandwidth of beyond 40 GHz, to meet the dynamic settling requirement of the T&H. Input parasitic capacitance of a SF includes a non-linear and a linear term, which are respectively originated from C_{gd} and C_{gs} of the input devices. Sampling on the input parasitic capacitance of the SF without C_{S} is possible. It results in higher bandwidth and kT/C noise budget is also met without C_{S} However, the obtained linearity is not sufficient. Therefore, a sampling capacitor of $C_{\mathrm{S}} = 30\,\mathrm{fF}$ is added to increase the linearity and achieve better than 36 dB THD, while maintaining a bandwidth of higher than 40 GHz.

A common problem of having several SF buffers in series is the common-mode (CM) voltage shifts limiting the usable signal swing. The first SF shifts the CM from 350 mV at the input to an output CM of approximately 700 mV at TT. The signal swing is 150 mV around the CM voltage (differential input range is $600\,\mathrm{mV_{p-p,diff}}$). As a result, the maximum tolerable CM voltage of the T&H is 750 mV to stay within reliability limits of the pMOS sampling switch. Since no further positive CM shift is possible, the output SF is a nMOS based SF. However, the minimum input CM requirement for the flash comparator array (400 mV) is not met. To solve this issue, forward-body bias (FBB) is applied to the back-gate of $\mathrm{M_{SFn}}$ as shown in Fig. 11.42. Using a supply voltage of $\mathrm{V_{DD}} = 1.2\,\mathrm{V}$ as FBB and thanks to the flipped-well option of the 22FDX process, nMOS threshold voltage is reduced by approximately 100 mV (TT corner) and adequate output CM voltage is achieved. Simulation results given in Table 11.10 show the T&H and output CM voltages across PVT. The

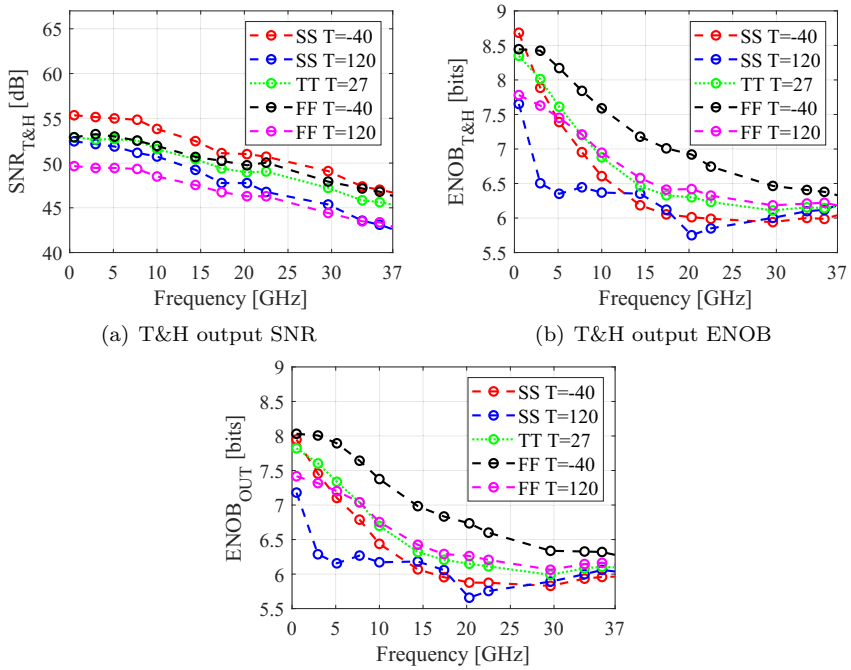
Table 11.10
T&H input bandwidth and CM across PVT. From [467] © 2019 IEEE

Corner	T&H Input BW [GHz]	CM Voltage T&H [mV]	CM Voltage Final Output [mV]
SS Temp = −40 °C	57.2	742	426
SS Temp = 120 °C	40.4	716	427
TT Temp = 27 °C	54	715	413
FF Temp = −40 °C	69.7	714	408
FF Temp = 120 °C	49.7	700	410
SF Temp = −40 °C	65.3	705	394
SF Temp = 120 °C	46.28	680	392
FS Temp = −40 °C	61.6	741	449
FS Temp = 120 °C	44	718	451

transistor M_{SFn} is a super low threshold voltage (SLVT) device. The SLVTs in 22 nm FDSOI use a flipped-well transistor architecture [468], which allows FBB for both SLVTs without any latch-up limitation, demanding a positive and negative body bias for the SLVT nMOS and pMOS respectively.

The complete 18.5 GS/s sampling front-end has been implemented in 22 nm FDSOI and the performance across PVT has been verified using small-signal and transient simulations. The overall T&H input bandwidth at each process corner is given in Table 11.10, achieving a worst-case bandwidth of 40 GHz. The spectral results are extracted from the transient simulation by performing a 256-point FFT on the samples stored on C_S (T&H output) and also at the output of the flash buffer (final output). The input signal is a sinusoidal single-tone swept across frequency. The SNR and ENOB of the T&H vs input frequency are shown respectively in Fig. 11.43 (a) and (b). Figure 11.43 (c) shows the total ENOB at the output of the flash buffer. Simulation results show a performance of better than 6 bits ENOB up to the 4th Nyquist zone of the ADC (f_{in} = 37 GHz). Thanks to FBB the T&H achieves a differential input range of 600 $mV_{p-p,diff}$ while the source-follower based buffers operate from a 1.2 V supply and clock buffer and switches use the standard 0.9 V power supply voltage. The total power consumption of the single-channel sampling front-end is 75 mW including the clock buffer (10 mW). In order to verify the performance on silicon, a test chip including the single-channel T&H has been taped out. Hence, apart from the schematic simulation results, the extracted simulation results for the worst case (f_{in} = 37 GHz , V_{in} = 0 dBFS) is given in Table 11.11. The post-layout simulation results prove a performance of better than 5.4 bits ENOB at Nyquist frequency across PVT.

The final implementation of the 4X-TI T&H requires a 2:1 frequency divider for the quadrature-phase clock generation. The frequency divider as



(a) T&H output SNR

(b) T&H output ENOB

(c) Final output ENOB

Figure 11.43
Spectral results of the T&H and output of the flash buffer (final output) vs input frequency across PVT (input is a sinusoidal single-tone signal at 0 dBFS). From [467] © 2019 IEEE

shown in Fig. 11.40 is composed of two quasi CML latches, which consume 15 mW from the 0.9 V supply. Finally, time-interleaved calibration is required for the sampling phase mismatch of the TI T&Hs. The mismatch is detected using a digital correlation-based estimation [469] and a 5-bit mixed-signal phase correction with capacitive tuning DACs is considered.

11.3.11 Analog-to-Digital Converter

In this section, design of the 18.5 GS/s 5-bit flash Analog-to-Digital Converter (ADC) core is discussed. The required overall conversion rate for the ADC, as discussed in the previous section, is 74 GS/s, which is not possible with a single-channel ADC. Although time interleaving, as the only solution, makes it possible to achieve these conversion rates, the price one has to pay is a reduced ADC input bandwidth and higher design complexity specifically for the calibration. Since the complexity increases with the number of parallel TI

Table 11.11
Spectral results of the single-channel sampling front-end across PVT (Extracted simulation results).

	T&H Output f_{in}=37 GHz, V_{in}=0 dBFS			Final Output f_{in}=37 GHz, V_{in}=0 dBFS		
Corner	SNR [dB]	SFDR [dBc]	ENOB [bits]	SNR [dB]	SFDR [dBc]	ENOB [bits]
SS, Temp=−40 °C	43	36.4	5.6	41.4	35.4	**5.4**
SS, Temp=120 °C	41.1	39.4	5.8	38.5	39.1	**5.6**
TT, Temp=27 °C	42	37.6	5.7	40.5	37	**5.6**
FF, Temp=−40 °C	43.8	38.9	6	42.1	38.7	**5.9**
FF, Temp=120 °C	40.7	39	5.8	39.1	38.3	**5.6**
SF, Temp=−40 °C	43.1	37	5.7	40.8	36.4	**5.5**
SF, Temp=120 °C	41.1	38.6	5.8	39.2	37.5	**5.5**
FS, Temp=−40 °C	43.1	36.5	5.6	41.4	36.4	**5.4**
FS, Temp=120 °C	40.5	39.1	5.8	38.4	37.3	**5.4**

channels, it is desired to keep the number of TI ADCs as low as possible. Consequently, the fastest ADC architecture is adopted. Flash architecture enables the highest conversion rate among the different ADC architectures. Hence, a 4X-TI flash architecture is chosen, which requires a quarter rate conversion speed (18.5 GS/s) for each flash ADC. Since the front-end sampler has also a 4X-TI architecture, there is no need for a second-rank time interleaving, resulting in reduced design complexity.

Flash ADCs are generally categorized as hardware inefficient and power-hungry converter types, since the complexity increases exponentially with the resolution. The comparator array in the flash is typically the main power consumer. To diminish the kickback and dynamic offset in high-frequency comparators and reduce metastability errors, using a preamplifier is usually unavoidable, which makes the highest contribution to the power consumption of the comparator array and consequently the flash ADC. The other large power consumer is the resistive ladder (R-ladder) generating the flash references. The comparator kickback towards the R-ladder depends on the impedance on the reference side. Hence, the R-ladder needs to be low impedance to achieve a sufficiently small settling time constant [470] to meet the required LSB accuracy of the flash reference levels. To overcome this power and performance bottleneck, in this design, a flash ADC architecture employing a comparator active body-biasing technique is proposed [471]. Thanks to the body-biasing options of the 22 nm SOI technology, which will be discussed next, the power consumption of the R-ladder and comparator array is significantly reduced, improving the power efficiency of the flash ADC.

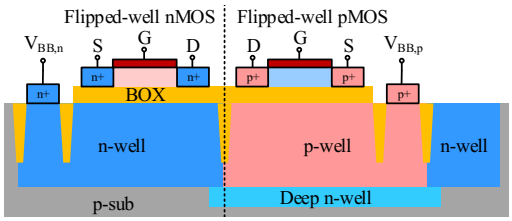


Figure 11.44
Simplified cross section of a SLVT nMOS and pMOS using flipped-well in FDSOI. From [467] © 2019 IEEE

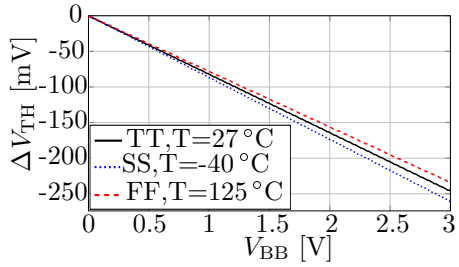


Figure 11.45
Simulation of the body bias voltage altering the SLVT nMOS threshold voltage across process variations (SLVT nMOS uses a flipped-well device architecture. From [472] © 2020 IEEE

Body biasing of MOSFETs in the bulk CMOS process is a widely used technique specifically in the digital design domain. It can be either applied as forward body bias (FBB) to reduce the threshold voltage or reverse body bias (RBB) to increase it. As an example in the field of microprocessors, RBB is employed to reduce the power consumption by reducing the leakage current during the standby mode and FBB is used when a faster device operation is required. As CMOS technologies scale towards deep sub-micron processes, the efficiency of body biasing reduces as well [473]. A respective body-bias efficiency of $\pm 12\,\% V_{\mathrm{TH}}$ is reported in [473] for the 90 nm CMOS process, while it reduces to $\pm 5\,\% V_{\mathrm{TH}}$ for the 40 nm process. As body-biasing efficiency decreases and tolerable body-bias range specifically FBB is strongly limited in the bulk CMOS process, while it is not the case for modern FDSOI technologies. A cross section of a super low threshold voltage (SLVT) nMOS and pMOS of the used FDSOI technology using flipped well (FW) is shown in Fig. 11.44. The device architecture of the depicted SLVTs in FW allows FBB for both SLVTs without any latch-up limitation, which needs a positive and negative body bias V_{BB} for the nMOS and pMOS respectively ($V_{\mathrm{BB,n}} > 0$ and $V_{\mathrm{BB,p}} < 0$). Apart from the constantly decreasing efficiency of the body biasing and its small allowed range in the bulk CMOS process, another issue

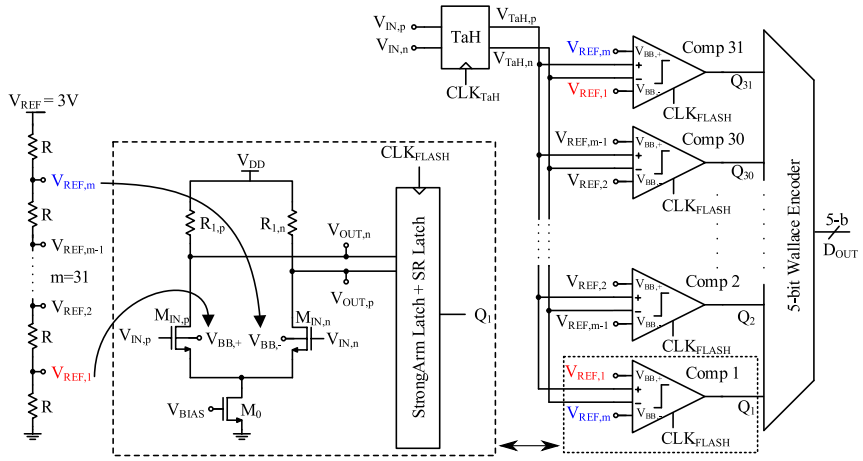


Figure 11.46
Schematic of the flash ADC with body-biased comparator. From [472] © 2020 IEEE

is non-linear junction capacitances C_{DB} and C_{SB}. As the device cross section of the SLVT devices depicted in Fig. 11.44 show, these non-linear junction caps are negligibly small. Hence, linearizing the MOS devices, leaves a linear dependency between the threshold voltage (V_{TH}) and the back-bias voltage (V_{BB}). The threshold voltage of a SLVT nMOS as function of V_{BB} across process corners is depicted in Fig. 11.45. The graph also confirms that V_{TH} changes linearly respective to V_{BB}. As a result, another degree of freedom is gained even for analog designs based on body biasing, which has been the motivation for a different flash comparator design in this work.

The overall architecture of the proposed flash is depicted in Fig. 11.46, which is adopted in a 5-bit 18.5 GS/s flash ADC. The Track-and-Hold (T&H) employs pMOS sampling switches along with a source-follower based input buffer, which operates from a 1.5 V supply enabling a T&H bandwidth of 28 GHz. The T&H is followed by the comparator array. The comparators leverage a body-biased preamplifier, which is the main difference of the proposed work with compared conventional flash ADCs. In a conventional flash architecture, a standard differential-difference amplifier (DDA) is used in each comparator. The DDA requires two differential pairs, one for the actual input signal and the other one for the reference voltages. The differential pair for the reference voltages is impaired by parasitic capacitances (C_{gd}, C_{gs}) causing high-frequency coupling and kickback into the R-ladder. Our proposed technique eliminates the differential pair for the reference voltages therewith the low impedance requirement of the reference ladder to guarantee settling of the R-ladder is alleviated. Moreover, the power consumption of the preamplifier is halved by using a single differential pair. The references from the R-ladder,

as shown in Fig. 11.46, are applied to the back-gate of the preamplifier input devices, generating the actual flash ADC reference levels by altering the input transistor threshold voltages. As discussed earlier, V_{TH} reduces linearly by increasing the V_{BB} as FBB voltage applied to the back-gate of the SLVT nMOS devices. Therefore, considering the linear dependency of the V_{TH} to V_{BB} and applying uniformly-spaced references from the R-ladder to the input transistor back-gate, uniformly-spaced comparator offsets are obtained correspondingly. Therefore, each comparator has a dedicated offset respective to the applied differential FBB, which is the flash reference level in this architecture. Each comparator then compares the differential input from the T&H to its built in offset. The body-biased preamplifier is followed by a standard StrongArm latch as the comparator core and a final S-R latch. A detailed analysis of the StrongArm latch is given in [474]. Finally, the thermometer code is converted to binary using a 5-bit Wallace Tree Encoder.

The flash reference levels are defined by dedicated comparator offsets. As a result, the full-scale range (FSR) of the ADC is actually the difference of the minimum and maximum comparator offsets in the comparator array. Since the R-ladder of the flash is placed between the ground and $V_{\mathrm{ref}} = 3\,\mathrm{V}$, this difference is twice the corresponding V_{TH} change of the input devices for the variation of the back-bias V_{BB} from 0 to V_{ref}, represented as $V_{\mathrm{TH}_{\mathrm{max}}}$ and $V_{\mathrm{TH}_{\mathrm{min}}}$ respectively. The FSR and LSB voltage are therefore calculated as

$$\begin{aligned} \mathrm{FSR} &= 2 \times (V_{\mathrm{TH}_{\mathrm{max}}} - V_{\mathrm{TH}_{\mathrm{min}}}) = 2 \times S_{\mathrm{BB}} \times V_{\mathrm{ref}} \\ \Delta &= \frac{\mathrm{FSR}}{2^n - 1}. \end{aligned} \tag{11.7}$$

Where $S_{\mathrm{BB}} = \frac{\mathrm{d}\,V_{\mathrm{TH}}}{\mathrm{d}\,V_{\mathrm{BB}}}$ is the tuning gain of the V_{TH} respective to V_{BB}. Since the adopted technology provides a threshold voltage tuning gain of $S_{\mathrm{BB}} \approx 85\,\mathrm{mV/V}$. By using a 3 V SC charge-pump as V_{ref}, a nominal full-scale range of approximately $500\,\mathrm{mV_{ppd}}$ is achieved. Variation of the S_{BB} across PVT according to simulation results, affects the ADC full-scale range only by $\pm 7\,\%$. Although the ADC FSR is altered across PVT, only a linear gain error is introduced to the transfer function of the ADC and this gain error can be calibrated out by trimming the 3 V reference. Accuracy of the flash reference levels depends on the matching of the R-ladder and comparator offsets. The resistor mismatch in the reference ladder is typically small [475], The comparator offset on the other hand is the main design challenge in flash ADCs. The offset in the comparators are categorized into three types, which are systematic dynamic and random offset. Systematic offset is predictable and can be remedied by adopting proper circuit design and layout techniques. Dynamic offsets can occur as a result of kickback or memory effect of the comparator core (StrongArm latch). Putting a preamplifier before the StrongArm latch mitigates the dynamic offset. The random offset is a result of process variation during the fabrication and can lead to large DNL/INL errors. Since a preamplifier is used in this design, the major contribution to the random offset is made by the input devices of the preamplifier ($\mathrm{M_{inL}}$, $\mathrm{M_{inR}}$). The variance of

the random offset voltage at the input can be approximated as [476]

$$\sigma^2(V_{\text{off}}) \approx \frac{A^2_{V_{\text{TH}}}}{W \cdot L}. \tag{11.8}$$

Where $A_{V_{\text{TH}}}$ is a process dependent coefficient. and $W \cdot L$ is the area under the gate of the input devices. Therefore, in order to reduce the random offset the size of the input transistors needs to be made larger. However, the penalty is more capacitive load on the T&H resulting in reduced bandwidth or increasing the power consumption. Monte Carlo simulation with $n = 1000$ samples shows a total input referred comparator offset of $\sigma \approx 4.1\,\text{mV}$. To get a fabrication yield of 99.7 %, 3σ needs to be less than 0.5 LSB. Considering $1\,\text{LSB} \approx 15\,\text{mV}$, this condition is met for 1.8σ in the current design. Therefore, the yield is reduced to 92.8 %. In order to bring back the yield without increasing the size of the input transistors, offset calibration is required. Since the random offset is static, foreground calibration methods with lower complexity compared to background calibration can be used. Using a resistive tuning DAC as suggested in [477] for each comparator, the references applied to the back gate of the input devices are trimmed with a resolution of 4-bits within 1 LSB range solving the offset issue.

Simulation results of the single-channel 18.5 GS/s 5-bit flash ADC in 22 nm FDSOI technology reveal a worst case SNDR and SFDR of 28.5 dB and 40 dBc in the first Nyquist zone of the single-channel ADC ($f_s/2$). The FFT plot of the single-tone test at Nyquist is shown in Fig. 11.47(a), while Fig. 11.47(b) shows the SNR and SNDR of the ADC across process corners vs input frequency. The total power consumption of the ADC is 140 mW, including clock buffers (36 mW), comparator array (53 mW), input buffer (49 mW), SC charge pump (2 mW) and resistive divider (24 uW). A comparison of this work with state-of-the-art flash ADCs is also given in Table 11.12.

This single-channel design is extended to a 4X-TI flash for the target 74 GS/s ADC. Hence, the first requirement is providing a bandwidth beyond 37 GHz with enough linearity and SNR up to $f_{\text{in,max}} = 37\,\text{GHz}$ to keep the T&H ENOB better than 5.5 bits across the entire bandwidth of the 4X-TI ADC. To achieve this, the UWB time-interleaved T&H discussed before is used as the front-end sampler driving the comparator arrays of the flash ADCs. Correction of the sample phase mismatch of the time-interleaved ADCs, as discussed in the previous section, is considered for the UWB T&Hs using a 5-bit phase-tuning CDAC. The remaining time-interleaved errors are gain and offset mismatch. The gain mismatch is corrected by trimming the 3 V ADC references with a tuning step of 30 mV (1 % tuning accuracy), which is applied to the R-ladder of the flash and the offset mismatch is digitally post-corrected to keep the offset error less than LSB/2. Finally, a digital encoder is added to the analog front-end of the ADC (74 GS/s 5-bit ADC). The details of the digital encoder required for the bubble-free thermometer-to-binary conversion is covered in the subsequent section.

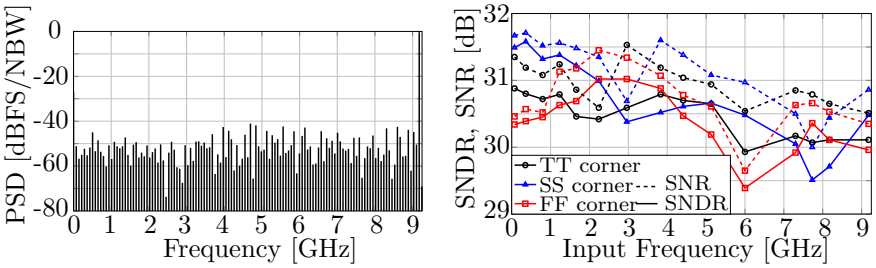


Figure 11.47
(a) 256-point FFT of the single-channel flash ADC (single-tone input amplitude is 0 dBFS, $f_{in} = 9.17$ GHz). (b) SNR and SNDR vs input frequency across process corners (single-tone sinusoidal input is at 0 dBFS and $T = 27\,^{\circ}$C). From [472] © 2020 IEEE

Table 11.12
Comparison of the single-channel 18 GS/s flash ADC with state-of-the-art flash ADCs. From [471] © 2019 IEEE

Reference	[478]	[479]	[480]	[481]	[482]	This Work
Architecture	4X-TI Flash	8X-TI Flash	8X-TI Flash	8X-TI Flash	Flash	Flash
Technology	65nm	65nm	32nm SOI	65nm	SiGe	22nm SOI
Resolution [bit]	6	5	6	6	4	5
SNDR [dB]	28.9	25.1	30.7	28	19.8	28.5
f_S [GS/s]	10	12	20	16	35	18.5
Power [mW]	63.5	81	69.5	435	4500	140
Input Capacitance [pF]	-	1.1	1	1.8	-	0.04
Calibration	yes	yes	yes	yes	no	no

11.3.12 Digital Encoder

The outputs of the flash comparator array (thermometer code) needs to be converted to a 5-bit binary code. Wallace Tree Encoder [483] is one of the widely used encoder architectures for this purpose, which has also the capability of bubble-error correction. Since this encoder has the lowest error rate compared to other encoder architectures [484], a 31-5 Wallace Encoder is considered for this design. The encoder adds the outputs of the comparator array using full and half-adders and evaluates the binary code (counts the number of '1's'). Considering the fast operating speed of the flash ADC in this design, a standard Wallace Encoder can not meet the timing requirements to operate

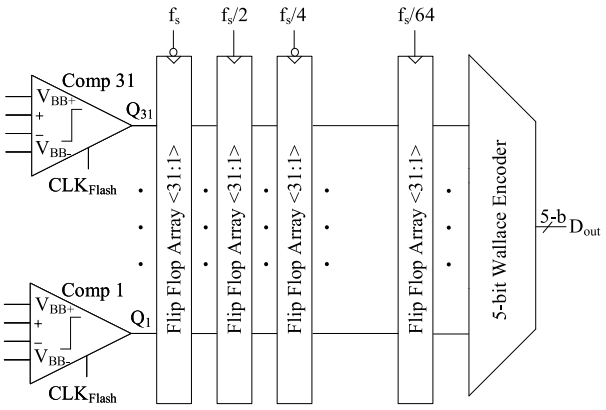


Figure 11.48
Block diagram of the 31-5 encoder using a decimation by 64.

at the full conversion rate of 18.5 GS/s per lane. Therefore, decimation of the output data is considered.

Decimation of the data at the output of an ADC is a commonly used technique specifically for high speed ADC, which reduces the output data rate by taking one from every M samples and ignoring the others (decimation by M). Hence, the ADC can be measured at a reasonably low output data rate although the analog front-end still operates at f_s. The first solution for the 31-5 encoder implementation based on decimation is shown in Fig. 11.48. The outputs of the comparator array are sampled by the first flip flop array operating at f_s. Then the second flip flop array operating at $f_s/2$ takes one every other samples and skips the remaining, which equals a decimation by two. Employing additional decimation stages enables a factor of 64 ($f_s/64 \approx 290$ MHz). Hence, the Wallace Encoder converts the down-sampled outputs to binary at a rate of 290 MHz. The down sampler and the Wallace Encoder are also implemented in 22 nm FDSOI. The clocks are generated by 2:1 CMOS clock divider (ring divider). In order to prevent set up and hold timing violations, one every other flip flop array are negatively edge triggered obviating the need for clock-phase alignment. The high-speed flip flops used for operation from f_s to $f_s/8$ are dynamic flip flops, while the rest are static flip flops to avoid data loss due to leakage. This decimation-based encoder is used for the test chip, which includes a complete single-channel 18.5 GS/s 5-bit flash ADC. Although decimation solves the issue for the measurement of a single-channel ADC, it can not be easily applied to the 4X-TI ADC. Moreover, a full rate digital output needs to be available on-chip as the receiver specification demand. Hence, other solutions such as pipelining, time interleaving and employment of an on-chip SRAM are required for the final encoder implementation.

Pipelining inside the Wallace Encoder is a solution, which can be implemented by breaking the encoding operation into smaller steps and using

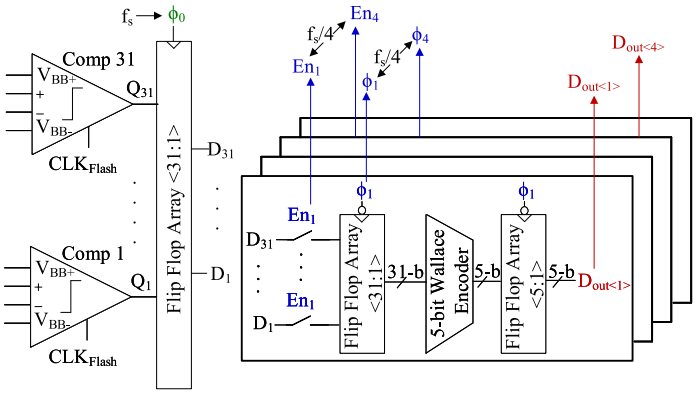


Figure 11.49
Block diagram of the 4X-TI Wallace Encoder.

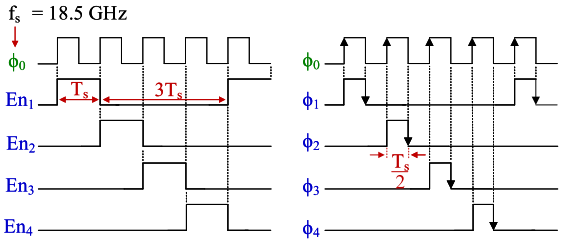


Figure 11.50
Timing diagram of the clocks used for the 4X-TI Wallace Encoder.

pipeline stages for each operation step. Hence, one conversion per clock cycle can be performed and a full rate digital output is obtained. The other solution is time interleaving of the 31-5 encoder. Simulation results of the implemented Wallace Encoder confirmed the feasibility of a 4X-TI encoder, while the timing requirements can not be met for a 2X-TI design. Using each of the aforementioned methods for the full rate digital output, reading out the 5-bit code at the rate of 74 GHz is not possible. Hence, an on-chip memory is used for such high-speed ADCs to store the data, so that the date can be read out off-line. Since it is easier to store the data on the memory at the lower rate of $f_s/4$ (4X-TI) compared to the full rate (pipelining), time-interleaved solution is preferred over pipelining. The block diagram of the 4X-TI Wallace encoder and the required clock phases are depicted in Fig. 11.49 and Fig. 11.50 respectively. As the block diagram of the encoder shows, each encoder lane is multiplexed using the enable signal (En_1 ... En_4). On the falling edge of the ϕ_0, the first flip flop array inside the selected encoder samples the thermometer code from the master flip flop array, which operates at the full speed. Each of the two flip flop arrays before and after the Wallace Encoder use the same

clock. Hence, the encoder has $4T_s$ as the available time for the conversion in the ideal case, which is the period of $\phi_1 \dots \phi_4$. Allocating a timing budget of $T_s = 54\,\text{ps}$ for the setup time of the 5-bit flip flop array and clock-to-Q propagation delay of the flip flop array preceding the encoder, the Wallace Encoder has $3T_s$ time left in the worst case to perform the encoding.

11.4 Conclusion

The DataRace project aims at realizing a wireless communication link at W-band with a throughput of 100 Gbit/s. The given link budget analysis in Section 11.2 confirms the feasibility of such a system and reveals requirements for the array dimensions. The passive components of the RF-front-end have been designed and demonstrators have been realized with conventional manufacturing techniques. The measurements confirm the simulated performance. The active parts of the receiver, i.e., the RF-to-IF converter and the ADC are designed in CMOS. The former has been realized and was partly measured, showing promising results. Also the PA required for the transmitter has been demonstrated in CMOS with outstanding performance.

The last phase of the project is still ongoing. Thus, the complete system has not yet been demonstrated. The next step is to integrate the presented components in a system-in-package receiver and fabricate it with commercially available high precision additive manufacturing process.