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Real100G.RF: A Fully Integrated, Multi-Purpose Radio Front-End for Wireless 100 Gbps

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9.1 Introduction

The main objective of the project, Real100G.RF funded by the special priority program SPP1655 from the German Research Foundation (DFG), is to leverage silicon-based economies-of-scale for a technology breakthrough in wireless multi-gigabit communication above 200 GHz. One of its many promising applications is a short range, high-speed wireless data transmission link with a data rate of up to 100 Gbps, e.g. in a data kiosk where people can download movies on their mobile electronic systems over a short distance in just a few seconds. The advantage of using a high carrier frequency of above 200 GHz is that a moderate relative bandwidth of 10 to 20% yields a high absolute bandwidth of several tens of GHz. Therefore, a wireless transceiver with a massive data rate of up to 100 Gbps can be realized in the physical layer using low-order modulation schemes [350]. This is in line with the recent IEEE standard 802.15.3d-2017 [351]. Additionally, a high carrier frequency of above 200 GHz leads to an ultra-compact transceiver and a moderate relative bandwidth re-

duces the complexity of its baseband circuitry. The challenges involved in this project are broadly classified as follows.

- Realization of wideband millimeter-wave transmitter (Tx) and receiver (Rx) circuit architectures using silicon-germanium (SiGe) technology.
- Realizing a large bandwidth and high efficiency antenna in SiGe technology, which can be directly connected to the Tx/Rx circuit without using space-consuming and lossy interconnects; thus building an ultra-compact radio module.
- Overcoming the limited link budget at millimeter-wave frequencies by implementing a suitable power-combining concept.
- Housing the Tx/Rx module in a robust, compact and efficient millimeter-wave package, which transfers only DC and baseband signals between the Tx/Rx module and the outside world. The package is also responsible for an efficient heat dissipation of the Tx/Rx module.

The project has been worked upon in cooperation between the Institute of Radio Frequency Engineering and Technology (IHE), Karlsruhe Institute of Technology (KIT) and Institute for High Frequency and Communication Technology (IHCT), Bergische Universitat Wuppertal (BUW).

9.1.1 State-of-the-art

During the time of the SPP1655, numerous groups all over the world developed high data-rate wireless communication transceivers at high millimeter-wave frequencies, using a broad range of technologies. This section discusses the state-of-the-art that can be found in the current literature. A key figure of merit (FoM) for these transceivers is the energy efficiency per transmitted bit, normalized to the bridged distance of transmission. This FoM is included in Tab. 9.1, which includes the various work described in this section, along with the achieved data-rates. For the purpose of comparison, the transmitter and receiver chip-sets developed at KIT and BUW are also included.

Current work in III/V technologies includes [352], where 35 nm InP-HEMT based split block modules transmit 96 Gbps at 240 GHz using an 8-PSK modulation scheme and a direct-conversion architecture. Even more recently, a super-heterodyne chip-set in 80 nm InP-HEMT presented in [353] transmits 100 Gbps in 16-QAM.

A 40 nm CMOS transceiver was presented in [354]. A data-rate of 80 Gbps is achieved over a 3 cm distance. The transmitter does not use fundamental power amplifiers, but power-combined, doubler-based modulators at the output. The carrier signal for the direct-conversion receiver is also directly derived from the transmitters output, therefore full-duplex communication is not possible. Two independent 16-QAM, 60 Gbps streams are transmitted with a super-heterodyne transceiver chip in [355]. Here, the data streams are split

into two 17.5 GHz bands, filling the total 35 GHz bandwidth of the W-band. The first is modulated with a 70 GHz carrier generated by a doubler, using low side injection. For the second band, a tripler provides a 105 GHz signal to a mixer using high side injection.

Work in 0.13 µm SiGe can be found in [356], where direct-conversion Tx and Rx with 5 dBi wire bond monopole antennas are placed opposite each other on a probe station and transmit 50 Gbps using BPSK modulation. In [357], an on-chip ×8 multiplier chain generates a 240 GHz carrier for a SiGe Tx and Rx chip-set. With BPSK modulation, 25 Gbps were demonstrated. A directivity of 14 dBi is achieved in this work with on-chip antennas utilizing localized backside etching (LBE) radiating into polyethylene lenses.

As part of SPP1655, exploratory work in an collaboration between IHP and BUW using an advanced SiGe technology with f_T/f_{max} of 350/550 GHz was presented in [358] and [359]. In both, a direct-conversion quadrature transceiver chip-set was developed. With RF amplifiers in both Tx and Rx, 90 Gbps were demonstrated for both 16-QAM and 32-QAM. The 230 GHz carrier for this Tx and Rx was generated by a ×16 multiplier chain. The front-end amplifier of the receiver was omitted in [360] to arrive at a mixer-first architecture, which enabled a data-rate of 100 Gbps in 16-QAM with 17 % error vector magnitude (EVM).

The above mentioned work in III/V or CMOS technologies all use highly directive horn antennas. In the work done in SiGe, meaningful transmission distances were achieved with high directivity, lens-integrated, on-chip antennas. An overview of the antennas used in the described state-of-the-art work and the bridged distances can be found in Tab. 9.2.

9.2 Fully Integrated Millimeter Wave Transceiver Concepts

The silicon-germanium (SiGe) semiconductor technologies used in this project are 'SG13S' and 'SG13G2' from Leibniz-Institute IHP. Both 'SG13S' and 'SG13G2' are 130 nm SiGe technologies, which differ mainly in terms of their transit frequency (f_t) and maximum frequency of oscillation (f_{max}). The f_t of 'SG13S' and 'SG13G2' are 240 GHz and 300 GHz, respectively. The f_{max} of 'SG13S' and 'SG13G2' are 340 GHz and 450 GHz, respectively [180]. Due to such high f_t and f_{max} values, a multitude of active and passive components such as mixer, amplifier, oscillator and coupler can be integrated on a monolithic microwave integrated circuit (MMIC) operating at frequencies beyond 200 GHz. Further, a 100 Gbps wireless transceiver MMIC can be realized by integrating Tx and Rx antennas either on the MMIC substrate (i.e. on-chip) or on a separate substrate (i.e. off-chip). In the later case, the antennas should be integrated with the MMIC using millimeter-wave interconnects

TABLE 9.1
Comparison with the State-of-the-Art

Ref.	Technology f_T/f_{max} (GHz)	Frequency (GHz)	Modulation	Data-rate (Gbps)	P_{DC} (W)	FoM[1] (pJ/bm)
[352]	InP HEMT 35 nm 515/–	240	8-PSK	96	—	—
[353]	InP HEMT 80 nm 300/700	270	16-QAM	100	—	—
[354]	CMOS 40 nm –/–	300	16-QAM	80	1.79	746.6
[355]	CMOS 65 nm –/–	70/105	16-QAM	2·60	0.28[2]	12.5[2]
[356]	SiGe 130 nm 300/450	190	BPSK	50	0.154[2]	500[2]
[357]	SiGe 130 nm 300/500	240	BPSK	25	0.95	253.3
[358]	SiGe 130 nm 350/550	225-255	16-QAM	90	1.96	22
[359]	SiGe 130 nm 350/550	220-260	32-QAM	90	1.96	22
[360]	SiGe 130 nm 350/550	220-255	16-QAM	100	1.41	14

[1] FoM: Figure of merit: P_{DC}/(highest data-rate · free-space-distance).
[2] Without carrier generation circuitry.

(e.g. wirebond or flip-chip interconnect). Consequently, the packaging concepts can be divided under two broad categories, namely System-on-Chip (SoC) and System-in-Package (SiP), respectively. The pros and cons of these two packaging concepts, followed by the choice made in this project are discussed in the following section. The overall cost of a microelectronic system operating at frequencies of hundreds of gigahertz is mainly governed by its package design. The requirements of a robust, compact and efficient package design for a 240 GHz wireless transceiver and the challenges involved in realizing the package are summarized below.

TABLE 9.2
Antennas of the State-of-the-Art

Ref.	Technology f_T/f_{max} (GHz)	Frequency (GHz)	Antenna Type	Antenna Gain (dBi)	Distance (m)
[352]	InP HEMT 35 nm 515/–	240	horn	—	40
[353]	InP HEMT 80 nm 300/700	270	horn	2×50	2.22
[354]	CMOS 40 nm –/–	300	horn	—	0.03
[355]	CMOS 65 nm –/–	70/105	horn	2×23	0.2
[356]	SiGe 130 nm 300/450	190	bond wire monopole	2×5	0.006
[357]	SiGe 130 nm 300/500	240	LBE[1] dipole + plastic lens	2×14	0.15
[358]	SiGe 130 nm 350/550	225-255	single pol. + Si lens	2×26	1
[359]	SiGe 130 nm 350/550	220-260	single pol. + Si lens	2×26	1
[360]	SiGe 130 nm 350/550	220-255	single pol. + Si lens	2×26	1
Sec 9.3	SiGe 130 nm 300/450	220	single pol. power comb. + Si lens	26.8 & 27.1	0.5

[1] localized backside etching.

- An ultra-compact surface-mount technology (SMT) package encapsulating the MMIC and the Tx/Rx antennas is foreseen, which can be directly mounted on a standard printed circuit board (PCB), i.e. a low-cost board with coarse feature size and pitch. The critical millimeter-wave signals are confined within the package; hence only DC and baseband signal (In this case, the baseband signal range up to 30 GHz) are routed through the package onto the PCB.

- The package should dissipate the heat generated by the MMIC, otherwise it could lead to malfunctioning of the sensitive semiconductor circuits or in the worst-case scenario damage them completely.
- An ultra-compact package design implies that the risk of an undesired electromagnetic interference between the various package components is severely high, which in turn could degrade the package performance, e.g. radiation pattern of the Tx/Rx antennas. Therefore full-wave electromagnetic simulations of the active and passive circuits as well as the complete package are necessary for eliminating such risks.

9.2.1 Package Concept

9.2.1.1 System-in-Package (SiP)

An SiP employs off-chip Tx and Rx antennas, which are integrated with the MMIC using millimeter-wave interconnects. An off-chip antenna has the advantage that an antenna substrate can be selected independently, taking into consideration parameters such as dielectric constant, loss tangent and substrate thickness, thus achieving an antenna with a high bandwidth-efficiency product (i.e. an antenna with a large operating bandwidth and a high radiation efficiency). However, there are two key disadvantages associated with off-chip antennas. First, the feature size (e.g. line/space width) required at such high frequencies is in the range of micrometers; hence cost-intensive thin film processes are necessary for manufacturing the antenna. Second, the millimeter-wave interconnects (usually based on wirebond or flip chip technology) between an off-chip antenna and an on-chip amplifier occupy a substantial chip area, since bond pads in a single-ended (e.g. coplanar waveguide) or a differential (e.g. coplanar stripline) configuration are required at the output terminals of the on-chip amplifier (In a Tx MMIC, the antennas are usually driven by a power amplifier, whereas in an Rx MMIC, the antennas are usually followed by a low noise amplifier). Third, the millimeter-wave interconnect results in an insertion loss of a few decibels and their bandwidth is also limited.

9.2.1.2 System-on-Chip (SoC)

An SoC employs on-chip Tx and Rx antennas. Therefore, no millimeter-wave interconnects are required between the MMIC and the antennas; thus saving chip area and avoiding the insertion loss and bandwidth limitation associated with the interconnects. However, on-chip antennas usually suffer from a low bandwidth-efficiency product due to the following reasons. First, the semiconductor substrate on which the antenna is fabricated has a high dielectric constant ($\epsilon_r = 11.9$ for Si), which enhances the undesired surface wave propagation at the cost of the desired space wave propagation, thus lowering the radiation efficiency. Note that special semiconductor processes such as through silicon via and localized backside etching could be used to prevent

surface wave propagation, however such processes significantly increase the manufacturing effort and cost. Moreover, they cause mechanical instabilities in the backend process and are hence not employed in this project. Second, The layer stack of the silicon back end of the line (BEOL) process used in this project is shown in Fig. 9.1. The substrate thickness between the topmost metal layer (TM 2) and the bottom-most metal layer (M 1) is approximately 15 µm. In other words, the antenna-to-ground distance is limited to 15 µm, which again results in a low bandwidth and a poor radiation efficiency. Note that the antenna-to-ground distance can be increased to >100 µm by placing a ground plane reflector below the bulk silicon; however in the absence of through silicon vias, this would be counter-productive since the surface wave power loss will be larger than the radiated power.

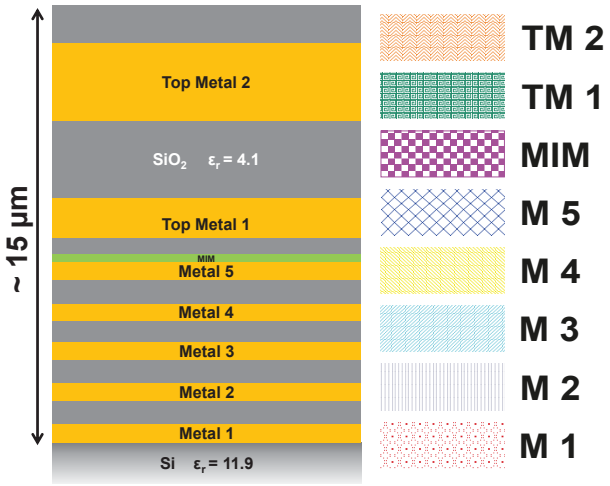


Figure 9.1
Silicon BEOL layer stack. From [361] © 2017 IEEE

9.2.1.3 Integrated Lens Antenna Concept

A modified SoC package concept is used in this project. As mentioned above, the main drawback of a typical on-chip antenna is a low bandwidth-efficiency product, which is countered by using an integrated lens antenna (ILA). An on-chip ILA achieves a high bandwidth-efficiency product based on Eq. 9.1.

$$\frac{P_{\text{rad}}}{P_{\text{total}}} \approx \left(\frac{\epsilon_{\text{r1}}}{\epsilon_{\text{r2}}}\right)^{\frac{3}{2}} \tag{9.1}$$

In Eq. 9.1, P_{rad}, P_{total}, ϵ_{r1} and ϵ_{r2} denote the power radiated by the antenna in upward direction, total power supplied to the antenna, relative permittivity of the medium surrounding the antenna and relative permittivity of

the antenna substrate, respectively. Using this equation for a silicon (Si)-based antenna with air as the surrounding medium, it is found that only 3% of the total power is radiated by the antenna in upward direction. The remaining 97% of the total power remains within the semiconductor substrate. In order to form an on-chip ILA, the backside of the antenna is attached to an Si lens. The lens acts as an extended substrate for the antenna, thereby enhancing its operating bandwidth. Further, the focal point of the lens is aligned with the phase center of the on-chip antenna; consequently, the backside radiation of the on-chip ILA provides an antenna beam with high-gain and narrow-beamwidth [361].

9.2.2 Quad Flat No Lead Type Package Configuration

The ILA-based SoC package design conceptualized for the 240 GHz wireless transceiver is shown in Fig. 9.2. The key design features of this package are as follows [361] [362].

- The 240 GHz transceiver MMIC including on-chip Tx/Rx antennas is attached face down to a hemispherical Si lens, which acts as an extended substrate for the MMIC. The glue used to attach the MMIC to the lens is a commercially available thermally-conductive, electrically-insulating epoxy adhesive, named Polytec TC 430-T. Usually, the dielectric characteristics of commercial epoxy adhesives are only available in the low frequency range of kilohertz or megahertz. In contrast, the dielectric characteristics of Polytec TC 430-T have been characterized in D-Band (i.e. 110 to 170 GHz) [361], as shown later in this chapter.

- An Alumina based redistribution layer (RDL) is attached face down to the Si lens. The RDL enables the routing of DC and baseband signals (up to 30 GHz) from the MMIC to a PCB or vice-versa. Note that the width and pitch of signal lines on a PCB is several orders of magnitude larger than a semiconductor MMIC; therefore the Alumina RDL manufactured using direct laser writing technology enables fanning out of the DC and baseband connections of the MMIC.

- A cavity is cut with high precision in the center of the RDL using laser cutting process. The MMIC is placed within this cavity and directly attached to the Si lens.

- The DC and baseband interconnects between the MMIC and RDL are realized through standard wirebonds. The operating bandwidth of these wirebond interconnects depends on the length of the wirebond interconnect and the type of wirebond used (i.e., ball-wedge, wedge-wedge or ribbon wirebond). This point is further clarified in section 9.5.1.

- An open-cavity quad flat no lead (QFN) package forms the base of the assembly. It includes a lead frame on both sides of the package base (a lead

frame is a series of bond pads placed along the periphery of the package). The lead frames on top and bottom sides of the package are connected by vias. The lead frame on the top is connected to the RDL by means of flip chip bumps, whereas the lead frame on the bottom is soldered to a PCB (The PCB is not shown in Fig. 9.2)

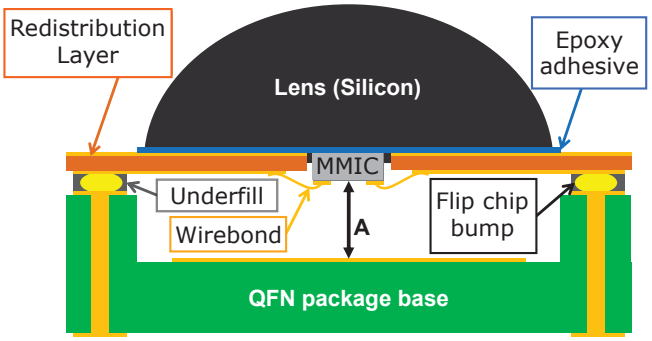


Figure 9.2
Integrated lens antenna based system-on-chip package concept. From [361] © 2017 IEEE

9.2.2.1 Electrical package requirements

As previously described in section 9.2.1.3, the bandwidth-efficiency product of an on-chip ILA used in this project is significantly larger than a typical on-chip antenna. According to the QFN package concept shown in Fig. 9.2, the MMIC (including the on-chip ILA) is glued face down to a Si lens, which acts as an extended substrate for the ILA. In other words, the topside of the on-chip ILA is surrouded by an air cavity of the QFN package base. As per Eq. 9.1, the ILA radiates nearly 97% of the total power through the Si lens (i.e. backside of the ILA) and only 3% of the total power is radiated in the direction of the QFN package base (i.e. topside of the ILA). Although the undesired power radiated towards the QFN package base is significantly smaller than the desired power radiated through the Si lens, the undesired space wave is reflected by the QFN package base and it causes destructive interference with the desired space wave (i.e. space wave radiated through the Si lens). Moreover, the open-cavity QFN includes a large metal pad (5 mm×5 mm) at the center, which not only enhances the reflection of the undesired space wave (i.e. radiated towards the QFN), but it also causes the reflected wave to be 180° out of phase. Note that if the distance between the on-chip ILA and the QFN package base (denoted by 'A' in Fig. 9.2) is equal to a quarter wavelength, then the space wave radiated through the Si lens and the space wave reflected by the QFN package base will

be in-phase; hence leading to a constructive interference. This is verified by means of a simulation-based investigation carried out at a lower frequency of 122 GHz [361]. Four different simulations are performed in which the distance between the on-chip ILA and the QFN (i.e. 'A' in Fig. 9.2) is set up as 100 µm, 300 µm, 700 µm and 1100 µm. The simulated realized gain and the simulated total efficiency of the ILA in each of these four cases is shown in Table 9.3. It is observed that for $A = 100\,\mu m$, the simulated realized gain and the simulated total efficiency are nearly 1 dB and 3% less than the corresponding values for $A = 1100\,\mu m$. Moreover, the maximum value of simulated realized gain is achieved for $A = 700\,\mu m$, which is close to a quarter-wavelength distance at the operating frequency. In addition, the radiation efficiency of the ILA is influenced by the following factors [361].

Table 9.3
Dependency of the simulated total efficiency and the realized gain of ILA on the distance A. From [361] © 2017 IEEE

Distance A	Realized gain dBi	Total efficiency in percent
100 µm	15.5	83.5
300 µm	16.4	86.9
700 µm	16.7	86.4
1100 µm	16.4	88.1

- The impedance mismatch at the boundary of the Si lens and its surrounding medium (i.e. air) causes reflections, which degrade the radiation efficiency of the ILA. This mismatch could be compensated by using a matching layer of quarter-wavelength thickness. The influence of a matching layer has been analyzed in simulation, however in practice no matching layer was used due to manufacturing limitations.
- The adhesive used for attaching the MMIC and RDL to the lens should have a negligible influence on the radiation characteristics of the ILA. For this purpose, the adhesive should have the following characteristics.
  - i It should be electrically insulating in nature.
  - ii It should have a minimum possible bond line thickness, i.e. the adhesive layer required to form a reliable bond between the MMIC and the lens should be as thin as possible.
  - iii Its dielectric characteristics should be known in the desired frequency range, or at least at a sufficiently high frequency so that its influence can be investigated by means of simulation.

The adhesive used for assembling the package is a commercial epoxy adhesive named Polytec TC 430-T. It is a thermally-conductive and electrically-insulating adhesive with a minimum bond line thickness of around 5 µm. Note that minimum bond line thickness of the epoxy adhesives depend on their filler size. Epoxy adhesives with silver filler particles have a minimum bond line thickness of around 50 µm. In contrast, Polytec TC 430-T has Boron nitride filler particles. These filler particles have a flat hexagonal shape, which results in an extremely small bond line thickness of around 5 µm. Further, the dielectric characterization of commercial epoxy adhesives is usually available up to kilohertz or megahertz range. Therefore, the dielectric characterization of Polytec TC 430-T has been carried out at a sufficiently high frequency range of 110 to 170 GHz. The measured relative permittivity and loss tangent of Polytec TC 430-T are shown in Fig. 9.3 [361].

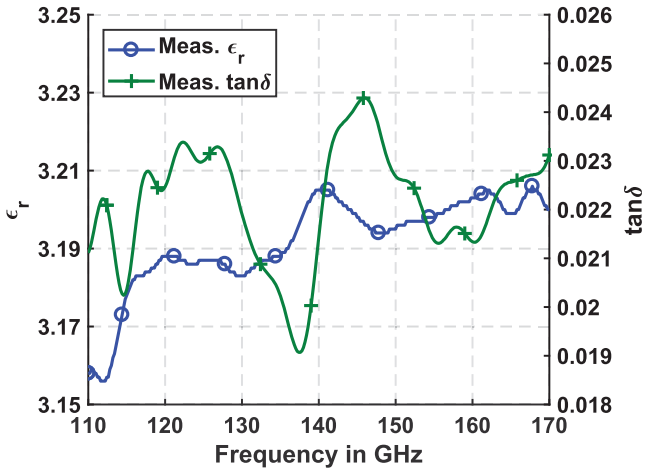


Figure 9.3
Measured dielectric characteristics of epoxy adhesive Polytec TC 430-T. From [361] © 2017 IEEE

9.2.2.2 Mechanical package requirements

The mechanical requirements of the package can be broadly divided into the following points. First, the package should be robust enough to withstand harsh environmental conditions, i.e. it should remain mechanically intact and operate reliably even under conditions such as dust, smoke and high temperature. Second, the QFN package concept is foreseen as a pick-and-place module, i.e. the QFN package can be surface mounted on a standard PCB

using lead free reflow soldering process. Therefore, the various components of the QFN package (e.g. wirebond and flip chip interconnects, MMIC, lens and RDL material, epoxy adhesive) should withstand the maximum temperature involved in a standard PCB production line, i.e. approximately 380 °C. Third, standard manufacturing and assembly techniques should be used in the physical realization of the package, which if necessary can be integrated in an industrial production line. The ILA-based SoC package concept shown in Fig. 9.2 require wirebond interconnects between the MMIC and RDL and flip chip interconnects between the RDL and QFN. In order to form these interconnects, a planar process environment is necessary, which in turn is provided by a lens holder, specially manufactured for this purpose. The steps involved in manufacturing and assembling the package are as follows [361].

- The lens is placed in a specially-fabricated lens holder, which ensures a planar process environment.
- The MMIC is placed face down on the lens such that the lens focal point is aligned with the phase center of the on-chip ILA. The MMIC is attached to the lens using the selected epoxy adhesive.
- The RDL with a cavity is placed face down on the lens such that the MMIC lies at the center of the RDL cavity. The RDL is attached to the lens using the selected epoxy adhesive.
- Wirebond interconnects routing DC and baseband signals between the MMIC and RDL are formed.
- Flip chip bumps are formed on the QFN bond pads (topside).
- An ultrasonic flip chip process is used to attach the QFN to the RDL followed by an underfill process, which enhances the reliability of the flip chip interconnect.

9.2.2.3 Thermal package requirements

The SiGe Tx MMIC used in this work has a power consumption of 2.9 W and its surface area is around 5.6 mm^2. Therefore, the amount of heat flux generated on the MMIC is approximately 518 kW/m^2, which is even higher than the heat flux generated in an Intel Pentium D microprocessor. The maximum operating temperature of a typical semiconductor chip is around 100 °C. However, the goal of this project is to attain a much lower junction temperature, i.e., in the range of 50 to 60 °C, provided the ambient temperature is around 30 °C. The thermal management strategies and the thermal simulations of various package designs is discussed in detail in section 9.5.2. The design features helpful in meeting the thermal requirements of the package are as follows.

- The Si lens not only enhances the radiation efficiency of the on-chip antenna (i.e. ILA concept), but it also acts as an excellent heat sink. The thermal conductivity of Si is 148 W/mK, which is several orders of magnitude larger than the commmonly used lens materials, e.g. Polytetrafluoroethylene (PTFE): 0.25 W/mK.

- The adhesive used to attach the MMIC and RDL to the lens is a thermally-conductive, electrically insulating epoxy named Polytec TC 430-T with Boron Nitride filler particles. The thermal conductivity of Polytec TC 430-T is 0.7 W/mK, which is significantly less than epoxy adhesives with silver filler particles (i.e. approximately 10 W/mK). However, the later could not be used due to two reasons. First, the adhesive should be electrically insulating in nature, otherwise it degrades the radiation characteristics of the ILA. Second, the adhesive layer thickness should be as low as possible in order to lower the overall thermal resistance of the package. This point is further clarified in 9.5.2. The minimum bond line thickness of Polytec TC 430-T is around 5 µm, which is ten times lower than silver-based epoxies.

- The cavity-based RDL used in the ILA-based SoC package concept is made up of Alumina with a thermal conductivity of 30 W/mK, which is significantly higher than other commonly used dielectric substrates, e.g. liquid crystal polymer 0.2 W/mK.

9.3 240 GHz Transceiver Circuits

9.3.1 Transmitter

A block diagram of the transmitter, which was developed in a cooperation between BUW and KIT, can be found in Fig. 9.4. Fig. 9.5 shows a micrograph of the Tx, where the circuit blocks are highlighted. A tunable ×16 multiplier chain generates a carrier frequency between 220 GHz and 240 GHz from an external local oscillator signal (LO). The multiplier chain used in the presented chip-set differs from the initial design presented in [322] and utilized in [360]. Instead of an active balun with 100 mW of DC power consumption, a broadband passive balun is used, which cuts the power consumption of the multiplier chain in half.

A four-stage PA adds drive power to the 16th harmonic coming out of the multiplier chain, which then is split by a differential 90° coupled line hybrid. The output signal of the separate mixers for I and Q-channel up-conversion is first run through pre-amplification PAs. A broadband Gysel power combiner superimposes the separated I and Q-channel signals. Afterwards, the differential output of the combiner is transformed into a single-ended one,

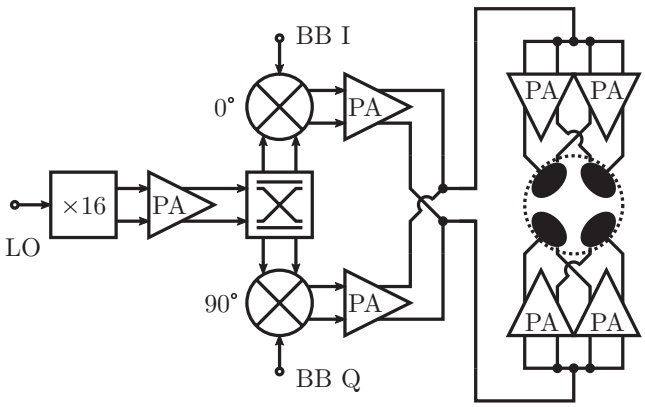


Figure 9.4
Transmitter block diagram.

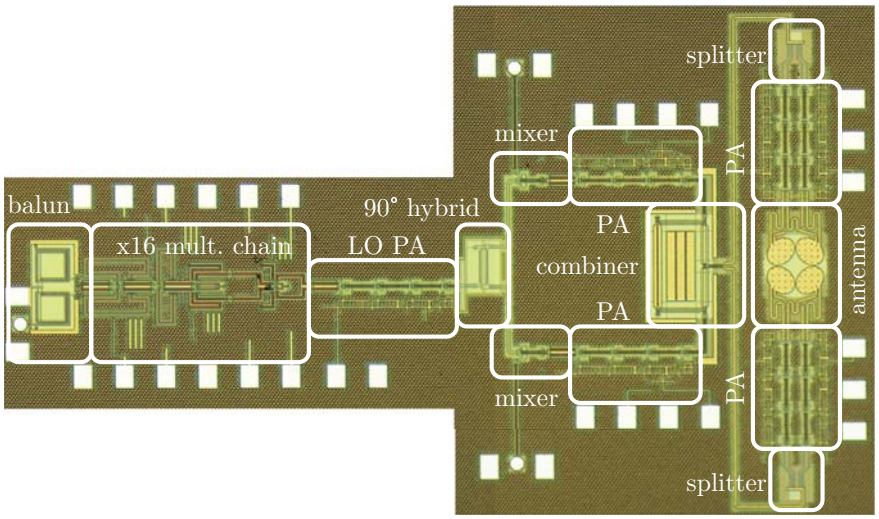


Figure 9.5
Transmitter circuit micrograph. The Tx is (3.12 × 1.8) mm^2 in size.

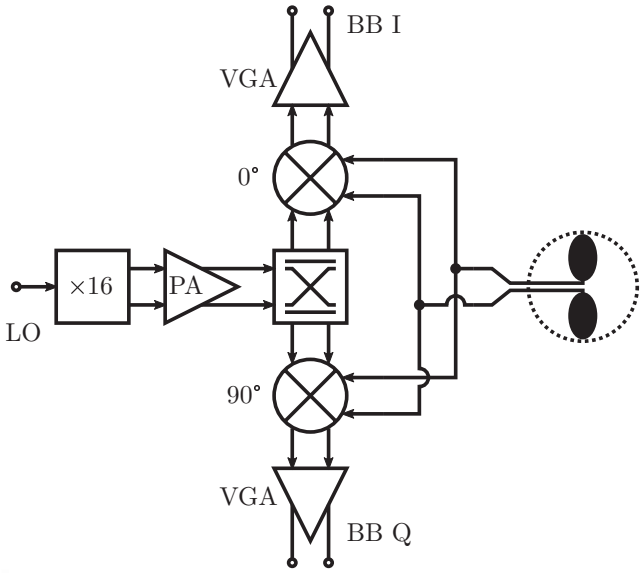


Figure 9.6
Receiver block diagram.

which in turn is then split by distributed power splitters [350]. These have a 50 Ω single-ended input and two 25 Ω differential outputs.

Four power amplifier drive the single polarization, in-air power combining antenna first-presented in [350] and used in a first experiment in [363] for an estimated output power of 10 dBm. Further details on the antenna design can be found in 9.4.2.6.

9.3.2 Receiver

A block diagram of the Rx can be found in Fig. 9.6. Fig. 9.7 shows a micrograph of the Rx, where the circuit blocks are highlighted. The same quadrature carrier generation chain consisting of ×16 multiplier chain, PA and 90° hybrid feeds a quadrature down-conversion mixer with one adjacent variable gain amplifier (VGA) per I or Q-channel.

A design insight was presented in [364], stating that due to the high baseline noise figure of SiGe low noise amplifiers above 200 GHz, a rather narrowband receiver front-end amplifier can be omitted for a wideband mixer-first topology without a severe noise penalty, provided that a high gain, low noise baseband amplifier directly follows. Both mixer and VGA designed for this work are described on the circuit level in 9.3.3.3.

Because the receiver uses a mixer-first architecture, the broadband receive

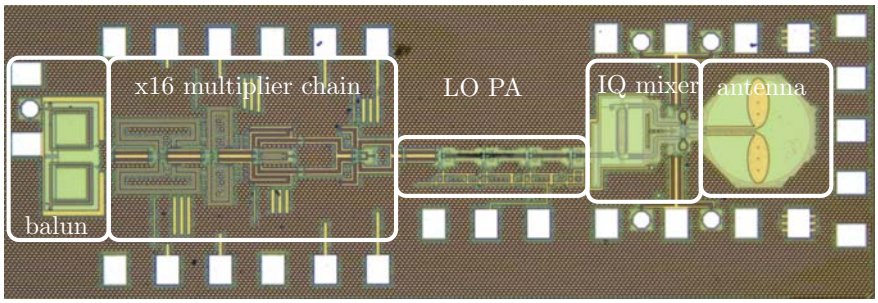


Figure 9.7
Receiver circuit micrograph. The Rx is (0.8 × 2.45) mm^2 in size.

antenna couples directly into the differential RF port of the mixer. The antenna consists of two differentially-fed monopoles, which excites a circular slot in a ground plane. The antenna principle is described in detail in 9.4.

9.3.3 Circuit blocks

9.3.3.1 Up-Conversion Mixer

An up-conversion mixer topology with wide input matching bandwidth, single-ended input but differential output and high linearity was introduced as the micromixer in [365]. Like in the classic Gilbert cell, a switching quad driven by an LO signal is responsible for frequency translation. But instead of a differential pair at the input, a bisymmetric Class-AB input stage provides a single-ended input to the micromixer. With its input resistance equal to $1/g_m$ due to the common-base transistor, the input impedance can be set to a wideband 50 Ω by choosing an appropriate bias current, emitter degeneration and series resistance. Fig. 9.8 presents the circuit schematic.

9.3.3.2 Power Amplifier

The power amplifier [322] is used both after the ×16 multiplier chain for generating drive power for the mixers and as an RF front-end amplifier. It utilizes four stages of a pseudo-differential cascode topology.

A breakout of the RF power amplifier was manufactured. It includes the four stage PA, on-chip Marchand baluns and compensated pads at input and output. Fig. 9.9 shows the measured scattering parameters of the PA. Including balun losses, the peak small signal gain is 13.4 dB at 226.5 GHz with a 3-dB bandwidth of 20 GHz. At center frequency, the simulated input referred P_{1dB} is -9 dBm. The simulated P_{sat} is 5.3 dBm, as shown in Fig. 9.10. The power amplifier draws 98 mA from a 4 V supply.

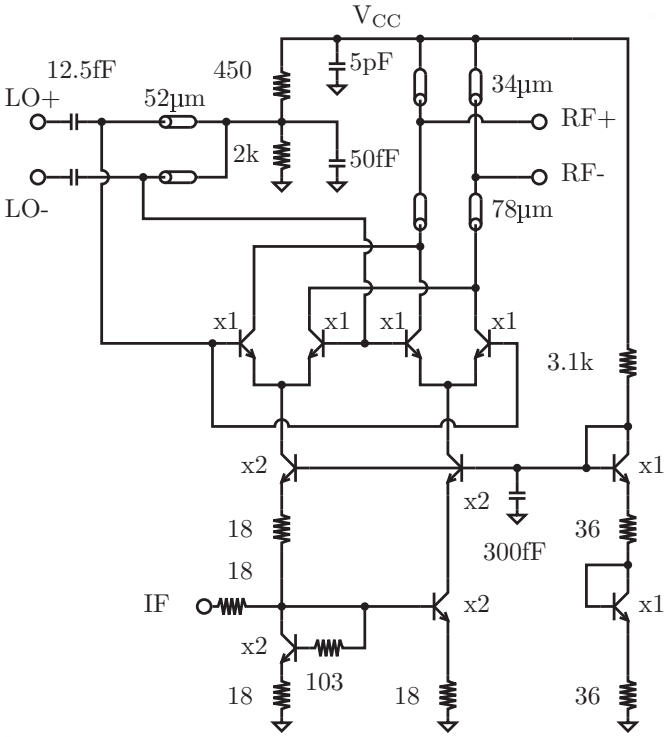


Figure 9.8
Up-conversion micromixer.

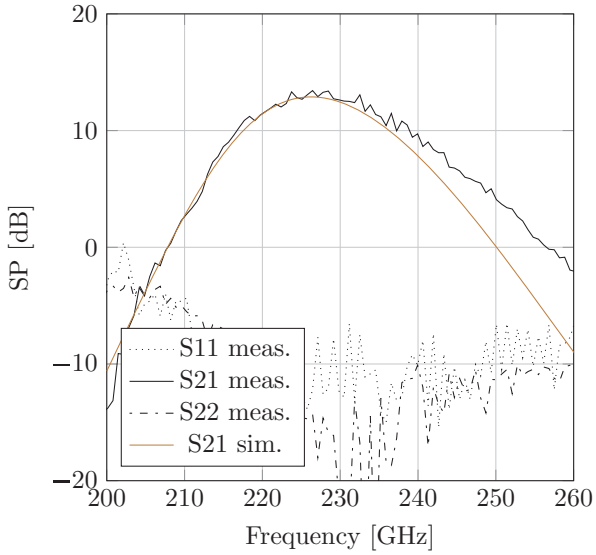


Figure 9.9
Measured and simulated scattering parameters of the front-end PA. From [322]

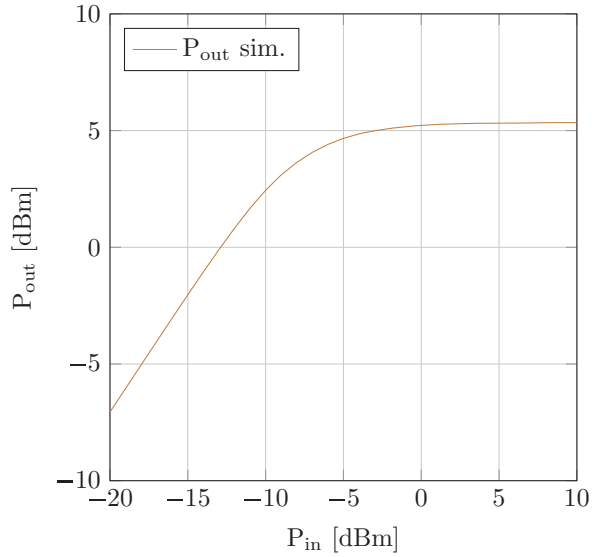


Figure 9.10
Simulated output power at 226 GHz of the front-end PA.

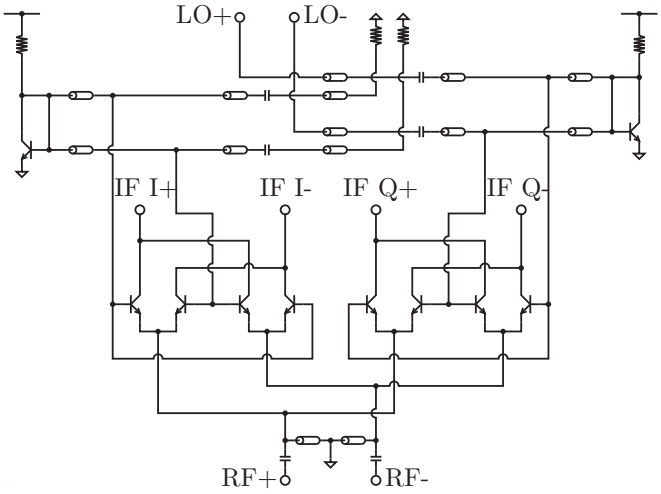


Figure 9.11
Emitter-coupled quadrature down-conversion mixer.

9.3.3.3 Quadrature Down-Conversion Mixer

This receiver uses a mixer-first architecture, with two parallel switching quads driven with a 90° carrier phase offset as shown in Fig. 9.11 for quadrature frequency translation. Low noise Cherry-Hooper transimpedance amplifiers provide baseband gain; their schematic is detailed in Fig. 9.12.

In the mixer, the RF input is emitter coupled to the HBTs. Their DC current has a ground-return path through shunt transmission line stubs in the L-type input matching network. A differential coupled line hybrid splits the carrier signal, to run the two switching quads in quadrature. The base currents of the transistors are generated in a seperate current mirror per switching quad and supplied through shunt stubs in the LO-matching network.

The baseband collector currents generated from the switching quad are fed into the baseband Cherry-Hooper transimpedance amplifier. The first differential pair is biased for low noise operation by a fixed tail current, but also provides a high gain with its 1.4 kΩ load resistors. Part of the output voltage is coupled back to the input through emitter followers, significantly increasing the bandwidth. Another differential pair with small $2\times(0.96\times0.12)\ \mu m^2$ transistors and 50 Ω wideband impedance matching load resistors follows. In its initial state, this differential pair provides further gain. But if a control current, denoted as Ictrl in Fig. 9.12, of up to 500 µA is applied, the devices g_m is reduced. Therefore the last stage provides gain variability. The current mirror configuration for this mechanism was first introduced in [366] as linear-in-dB cell. In this particular variation, a 4:1 bipolar current mirror with β-helper is fed by a reference current from a PMOS current source. The control cur-

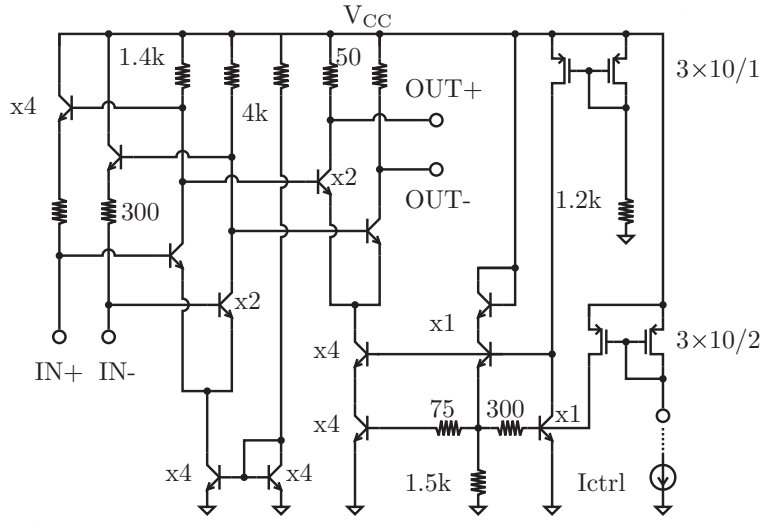


Figure 9.12
Variable gain transimpedance amplifier.

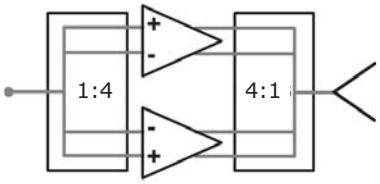
rent introduces an additional voltage drop over the current mirrors resistors, lowering the transistors respective base-emitter voltage and therefore the differential pairs tail current.

9.4 On-Chip Integrated Lens Antennas

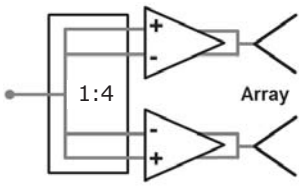
9.4.1 In antenna power combining

The output power of transistor-based power amplifiers operating in millimeter and sub-millimeter wave range is limited due to the reduction in the gate length and emitter area of the transistors. The miniaturization of transistors is on one hand essential for obtaining transit frequencies in hundreds of gigahertz, however, on the other hand, it reduces the current consumption and the breakdown voltage of the transistor-based devices. Consequently, a high Tx output power can be achieved by using the power-combining concepts shown in Fig. 9.13. The drawbacks of the existing power combining concepts, followed by a novel power combining concept introduced in this work and its advantage over the existing concepts are given below [350].

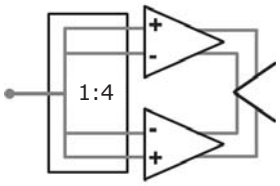
- Power amplifiers in parallel (Fig. 9.13(a)): The main drawback in this concept is that the line losses in a semiconductor BEOL process are signifi-



(a) Power amplifiers in parallel



(b) Power combining in an antenna array



(c) Power combining in a single antenna

Figure 9.13
Power combining concepts. From [350] © 2016 IEEE

cantly high. Hence, the losses incurred by the coupler outweigh the power amplification achieved by operating several power amplifiers in parallel.

- Power combining in an antenna array (Fig. 9.13(b)): In this concept, each antenna of an antenna array is fed by a power amplifier. In order to reduce an undesired coupling between the antennas, a finite spacing is required between the antennas, which requires longer feed lines and a larger chip area for implementation. Additionally, if the antenna array is integrated with a dielectric lens in order to achieve a high gain directional beam, the focal point of the lens is aligned with the array phase center, which creates a beam tilt. The severity of the beam tilt increases with an increasing distance from the lens.

- Power combining in a single antenna (Fig. 9.13(c)): The drawbacks of the abovementioned concepts are overcome by means of a novel power combining concept used in this work. In this concept, the output power of several power amplifiers operating in parallel are combined in a single antenna. Unlike the concept of power amplifiers in parallel, there are no coupler losses incurred by this concept. Further, in contrast with the concept of power combining in an antenna array, the required chip area is substantially smaller and a concentrated phase center is achieved. The later is useful in integrating a dielectric lens with the antenna without creating a beam tilt.

9.4.2 Broadband On-chip Antenna Design

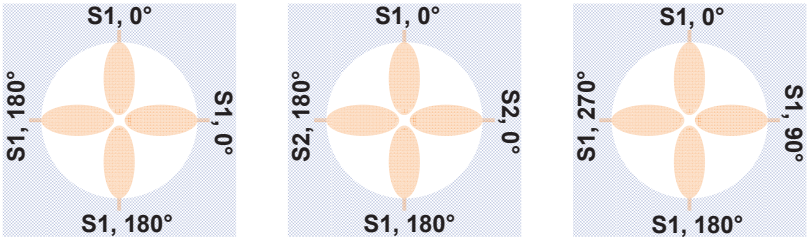
A broadband antenna is implemented in an Si BEOL process consisting of seven metal layers as shown in Fig. 9.1. The topmost and bottom-most metal layers (i.e., TM 2 and M 1) are separated by approximately 15 µm. In other words, the maximum possible antenna-to-ground distance is restricted to 15 µm. The antenna consists of a slot in a ground plane, whose diameter (d) is given by Eq. 9.2, i.e. one half of the guided wavelength.

$$d = \frac{c_0}{2 f_c \epsilon_r} \tag{9.2}$$

In Eq. 9.2, c_0, f_c and ϵ_r denote the speed of light, the lower cutoff frequency of the antenna and the relative permittivity of the antenna substrate, respectively. On using $f_c = 174$ GHz and $\epsilon_r = 11.9$, the slot diameter is calculated as $d = 250$ µm. The slot is excited by using two or more monopoles, which in turn are fed by power amplifiers; thus achieving power combining in the radiating element [350]. The various parameters necessary for designing such an antenna are investigated below.

9.4.2.1 Antenna Polarization

Different antenna polarizations can be realized depending on the relative phase values of the monopoles. The antenna configurations for three different polarizations are shown in Fig. 9.14. In each case, four monopoles are used to realize an antenna polarization, however less or more number of monopoles (e.g. 2 or 8) can be used to realize the same antenna polarization.



(a) Linear polarization (b) Dual-linear polarization (c) Circular polarization

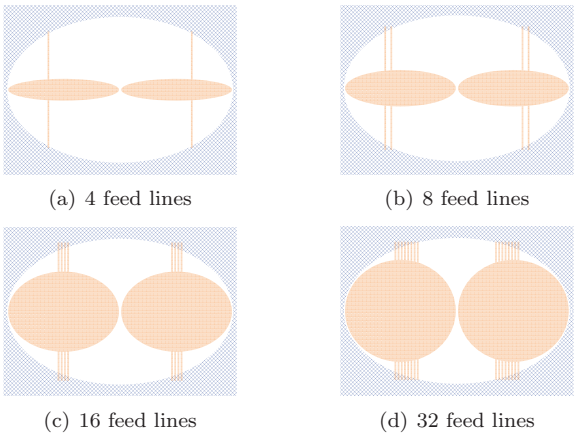
Figure 9.14
Antenna configuration for different polarizations. From [367] © 2017 IEEE

A linear polarization is generated by feeding the four monopoles with a power-split, differential signal S1 (see Fig. 9.14(a)). A dual linear polarization is generated by feeding the four monopoles using two different power-split, differential signals S1 and S2 (see Fig. 9.14(b)). A circular polarization is generated by feeding the four monopoles using a power-split single-ended signal S1, such that the relative phase values of the sub-signals are 0°, 90°, 180° and

270° in clockwise or counter-clockwise direction for left-hand or right-hand circular polarization, respectively (see Fig. 9.14(c)) [367].

9.4.2.2 Power Combining Limit

If each monopole is excited using more number of feed lines, it enhances the amount of power combining that takes place within the radiating element. Since multiple feed lines connected to a monopole act as parallel transmission lines, the input impedance of the antenna decreases; therefore the shape of the monopoles is adjusted (i.e. the monopoles are made broader) in order to achieve an impedance matching between the monopoles and the feed lines. The maximum number of feed lines, which can be connected to a monopole is determined by means of a simulation-based investigation. The simulation model used for this investigation consists of a slot with two monopoles. Four cases are simulated, where each monopole is excited using 4, 8, 16 and 32 feed lines, as shown in Fig. 9.15.



(a) 4 feed lines (b) 8 feed lines

(c) 16 feed lines (d) 32 feed lines

Figure 9.15
Simulation model of the antenna. From [367] © 2017 IEEE

The characteristic impedance of each feed line is same as the output impedance of the power amplfier, i.e. 70 Ω in this simulation. For an initial estimate, the feed lines are connected to ideal 3 dB power dividers and ideal 180° phase shifters. Additionally, the ideal feed network is terminated using 70 Ω waveguide ports. The shape of the monopoles is adjusted so that the simulated return loss is greater than 10 dB in an operating frequency range of 200 to 260 GHz. The resultant total antenna efficiency is shown in Fig. 9.16. It is observed that in the case of 16 feed lines per monopole, the total antenna efficiency shows a degradation of less than 5% over the operating frequency range. Whereas, in the case of 32 feed lines per monopole, the total antenna efficiency shows a substantial degradation over the operating frequency range [367].

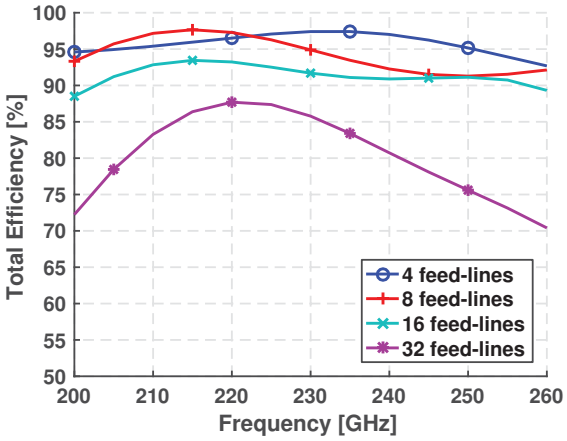


Figure 9.16
Total antenna efficiency for 4, 8, 16 and 32 feed lines per monopole. From [367] © 2017 IEEE

9.4.2.3 Amplitude and Phase Imbalance

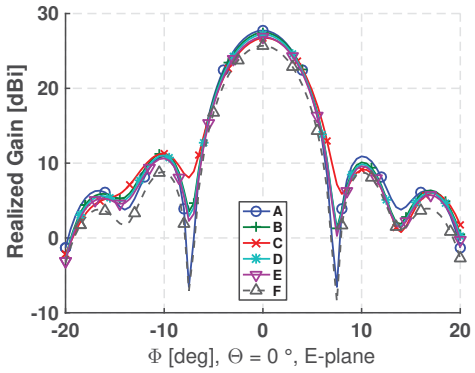
A slot antenna with four monopoles is taken into consideration. Each monopole is fed by two in-phase signal lines with an impedance of 30 Ω per line. The phase between adjacent monopoles is ideally shifted by 180° in order to achieve a linearly-polarized, power-combining antenna. The influence of amplitude and phase imbalance is investigated by simulating six different cases, shown in Table 9.4.

Table 9.4
Phase and amplitude mismatches. From [350] © 2016 IEEE

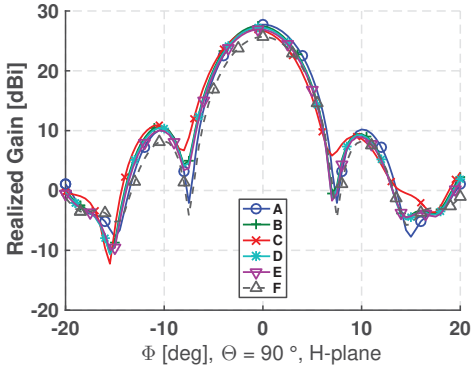
[deg] / [dB]	P1	P2	P3=P4	P5=P6	P7	P8
A	0/0	0/0	180/0	0/0	180/0	180/0
B	20/0	20/0	180/0	0/0	160/0	160/0
C	40/0	40/0	180/0	0/0	140/0	140/0
D	40/0	0/0	180/0	0/0	180/0	140/0
E	20/-3	20/0	180/0	0/0	160/0	160/-3
F	0/-50	0/0	180/0	0/0	180/0	180/-50

In the simulation, the antenna is mounted on a hemispherical Si lens with 12 mm diameter. The resultant radiation pattern and the total antenna effi-

ciency for the ideal case (Case 'A' in Table 9.4) and the deviation cases (Cases 'B' to 'F' in Table 9.4) are shown in Fig. 9.17 and Fig. 9.18, respectively. It is observed that if the phase values of ports 1, 2, 7 and 8 are simultaneously shifted by 20° from the ideal phase value (i.e. Case 'B'), it leads to a 0.5° tilt in the H-plane beam and 0.23 dB degradation in the realized antenna gain. Additionally, if the signal amplitude at ports 1 and 8 is also reduced by 3 dB (i.e. Case 'E'), the realized antenna gain decreases by 1.05 dB. Next, if the phase values of ports 1, 2, 7 and 8 are simultaneously shifted by 40° from the ideal phase value (Case 'C'), it leads to a 0.5° tilt in the E-plane beam and 0.95 dB degradation in the realized antenna gain. Finally, if the signal amplitudes of ports 1 and 2 are reduced by 50 dB (Case 'F'), the realized antenna efficiency degrades by nearly 35% [367].



(a) E-plane



(b) H-plane

Figure 9.17
Simulated radiation pattern at 245 GHz for amplitude and phase distribution shown in Table 9.4. From [350] © 2016 IEEE

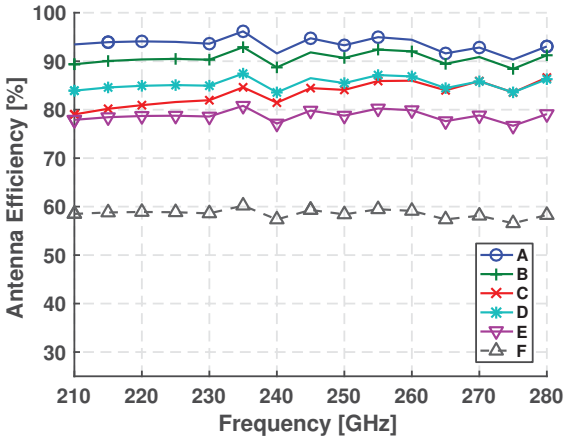


Figure 9.18
Simulated antenna efficiency for amplitude and phase distribution shown in Table 9.4. From [350] © 2016 IEEE

9.4.2.4 Power-Splitter Network: Distributed Transformer

A power-splitter network is required for feeding the monopoles by means of multiple transmission lines in parallel. The power-splitter network should have the following characteristics.

- It should operate over a broad frequency range of 200 to 320 GHz.
- It should provide two pairs of quasi-differential lines (i.e. a pair of microstrip lines with 180° phase difference) as output, since each power-splitter network should feed two monopoles with two feed lines per monopole.
- A single-ended input with a characteristic impedance of 50 Ω in order to facilitate probe-based antenna measurement.
- It should demonstrate different output impedances so that impedance matching can be achieved between the input impedance of the antenna and the output impedance of the power amplifier.

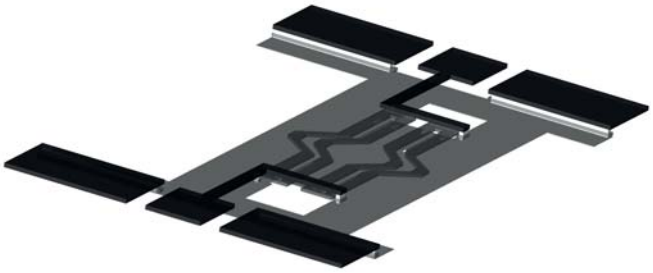
The abovementioned characteristics could be satisfied using a distributed transformer (DT) circuit, introduced in [368]. A DT circuit is small in comparison to the operating wavelength. Moreover, its size does not scale proportionally to the operating wavelength; thus achieving a high relative bandwidth and low losses in comparison to a quarter-wavelength coupler. A DT acts as a 1:1 transformer, whose input and output impedances (Z_{in}, Z_{out}) are related by Eq. 9.3.

$$Z_{\text{out}} = \frac{Z_{\text{in}}}{N} \tag{9.3}$$

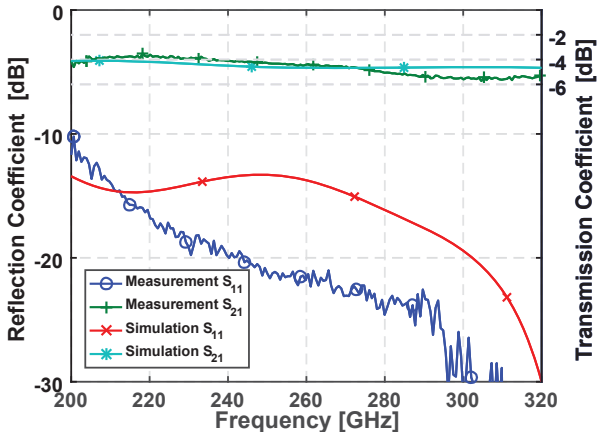
In Eq. 9.3, N denotes the number of output transmission lines. A DT consists of a single input feed line, which is magnetically coupled to N quasi-differential output lines (quasi-differential output lines imply a pair of microstrip lines which show a phase difference of 180° with respect to each other). The magnetic coupling is enabled by means of a rectangular slot in an intermediate ground plane. Further, the input feed line is short circuited at one of its ends and it has an unavoidable intrinsic inductance, which requires a metal-insulator-metal capacitor for its compensation. In this work, two DT based power-splitters with an output impedance of 12.5 Ω and 50 Ω have been realized [350].

DT-based Power-Splitter with 12.5 Ω output: A DT based power-splitter with a 50 Ω coplanar waveguide input and two pairs of quasi-differential outputs is shown in Fig. 9.19(a). Each of the four output lines has an impedance of 12.5 Ω. The output and input impedance values are consistent with Eq. 9.3. The power splitter is designed in a back-to-back configuration in order to enable probe-based measurement. The power splitter has a very small size of 90 µm × 60 µm. The simulation and measurement results of the power splitter in the frequency range of 200 to 320 GHz are shown in Fig. 9.19(b). An excellent agreement is observed between both the results in the entire frequency range. The maximum simulated amplitude and phase imbalance of the power splitter are 0.9 dB and 10°, respectively, which could be attributed to the asymmetric geometry of the power splitter.

DT-based Power-Splitter with 50 Ω output: A DT based power splitter with 50 Ω input and output impedances is designed as shown in Fig. 9.20(a). In other words, the input coplanar waveguide and each of the four quasi-differential output lines have a characteristic impedance of 50 Ω. Unlike the power-splitter shown above, this power splitter shows a transformation ratio of 1:4. The design layout of the power splitter is shown in Fig. 9.20(a). In this design, the orientation of the input microstrip transmission line and a pair of quasi-differential output lines is changed by 90° with respect to the previous design. Similar to the previous design, the input and output lines are magnetically coupled by means of a rectangular slot in an intermediate ground plane. Further, phase-matched meandered lines are added in order to realize a back-to-back configuration. The simulation and measurement results of the power splitter in the frequency range of 200 to 320 GHz are shown in Fig. 9.20(b). An excellent agreement is observed between both the results in the entire frequency range. The maximum simulated amplitude and phase imbalance of the power splitter are 0.7 dB and 4°, respectively. Note that the amplitude and phase imbalance values are better than the previous design due to the symmetrical geometry of the power splitter.



(a) Design layout



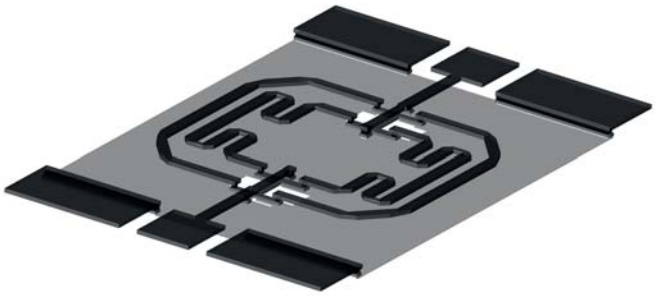
(b) Simulated and measured S parameters

Figure 9.19
DT-based power splitter with two pairs of quasi-differential 12.5 Ω outputs. From [350] © 2016 IEEE

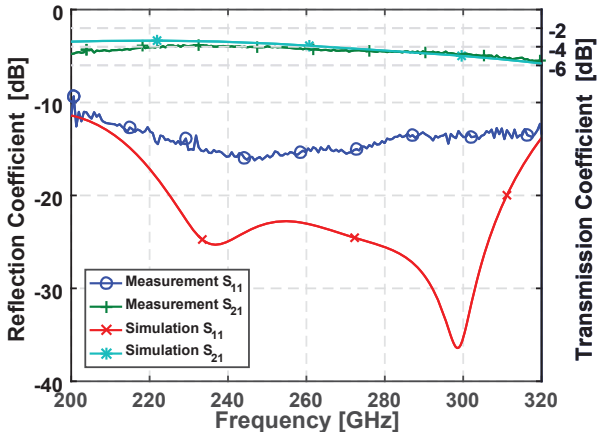
9.4.2.5 Four-Feed Differential Antenna with 6 mm Silicon Lens

Various aspects involved in the proposed broadband on-chip antenna concept have been individually investigated up to this point. These aspects include feeding of monopoles to achieve a desired antenna polarization, maximum number of feed lines per monopole without degrading the antenna efficiency, the influence of amplitude and phase imbalance of monopole feed lines on the antenna efficiency and variants of a DT-based power splitter network. Based on the outcomes of these investigations, a four-feed differential antenna is designed as shown in Fig. 9.21 [350].

It consists of a 250 µm diameter slot (the value of slot diameter is calculated using Eq. 9.2) in a ground plane, excited using four differential-feed monopoles. Each monopole is fed by two in-phase signal lines and the phase be-



(a) Design layout



(b) Simulated and measured S parameters

Figure 9.20
DT-based power splitter with two pairs of quasi-differential 50 Ω outputs. From [350] © 2016 IEEE

tween adjacent monopoles is shifted by 180°; thus forming a linear-polarization power-combining antenna. The microstrip lines used for feeding the monopoles have a characteristic impedance of 50 Ω per line, therefore a DT-based power splitter shown in Fig. 9.20(a) is placed on either side of the antenna. Each DT-based power splitter provides four feed lines in quasi-differential configuration, i.e. eight feed lines in total. Further two out of four quasi-differential feed lines coming out of each DT-based power splitter are crossed so that each monopole is fed by two in-phase lines. Although the extra feed line length required for this cross-connection leads to an additional loss, the additional loss is 1.1 dB less than if the DT-based power splitters shown in Fig. 9.19(a) were used in this antenna. The input microstrip transmission lines of the DT-based power splitters are connected by means of a T-junction. Finally, a spiral Klopfenstein

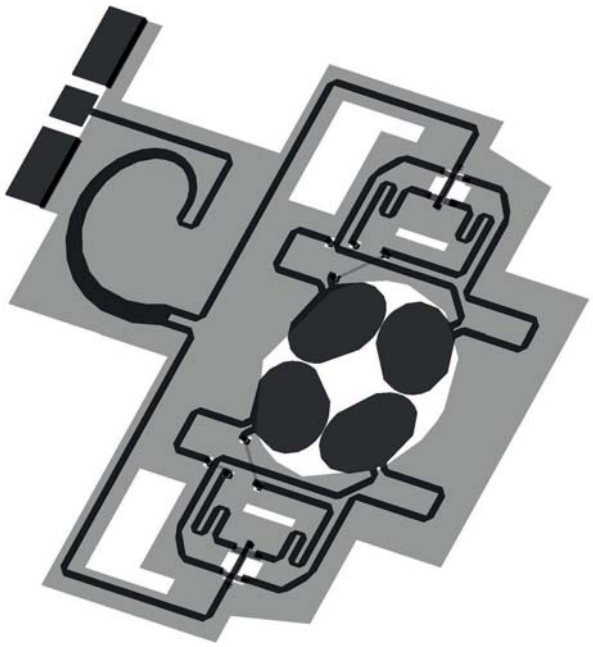
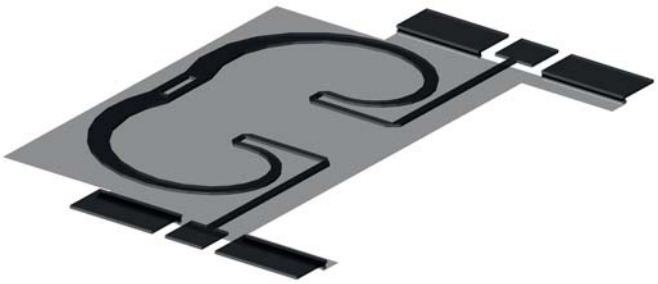


Figure 9.21
Layout of four-feed differential antenna operating from 200 to 320 GHz. From [350] © 2016 IEEE

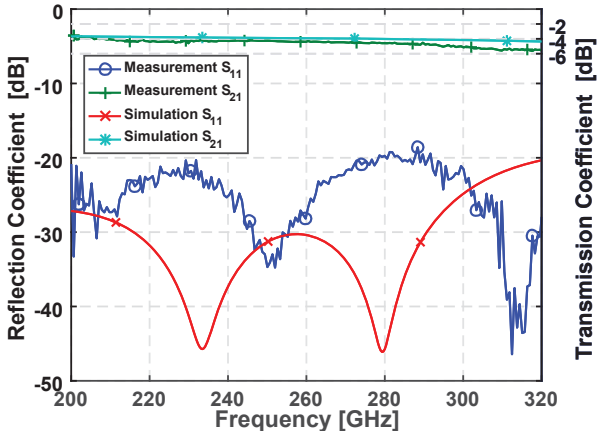
taper is used for matching the impedance between the T-junction and 50 Ω coplanar waveguide pads at the end. The simulation and measurement result of the spiral Klopfenstein taper in a back-to-back configuration is shown in Fig. 9.22.

Its measured return loss and single-ended insertion loss are greater than 20 dB and −2.5 dB, respectively in the operating frequency range of 200 to 320 GHz. A prototype of the four-feed differential antenna is integrated with a hemispherical Si lens of 6 mm diameter. As previously described in section II, a thermally-conductive, electrically-insulating epoxy named Polytec TC 430-T is used to attach the antenna to the Si lens. Since the adhesive has a relatively low relative permittivity of around 3.2 (see Fig. 9.3) and its bond line thickness is of the order of a few micrometers, it has an almost negligible influence on the electrical properties of the on-chip ILA. The simulated and measured reflection coefficient and realized gain of the ILA are shown in Fig. 9.23. A good agreement is observed between the measurement and simulation result. The theoretically-achievable gain of a lens antenna (G) is given by Eq. 9.4.

$$G = \eta \cdot \eta_{\mathrm{L}} \left(\frac{\pi \cdot L_{\mathrm{D}}}{\lambda} \right)^2 \tag{9.4}$$



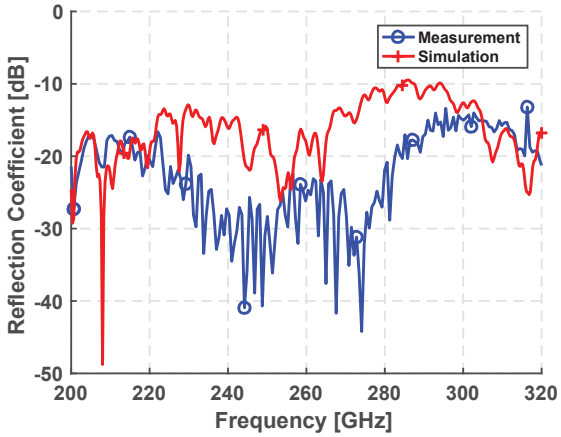
(a) Design layout



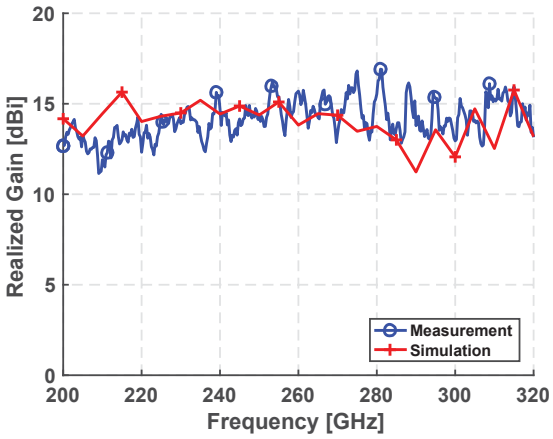
(b) Simulated and measured S parameters

Figure 9.22
Spiral Klopfenstein taper in back-to-back configuration. From [350] © 2016 IEEE

In Eq. 9.4, the parameters η, η_{L}, L_{D} and λ denote the simuated antenna efficiency, lens efficiency, lens diameter and operating wavelength, respectively. Using $L_{\mathrm{D}} = 6\,\mathrm{mm}$, $\eta_{\mathrm{L}} = 80\%$, $\eta = 89\%$, the theoretical gain of a lens antenna is calculated as 22 dBi at 240 GHz. The measurement of the four-feed differential antenna integrated with a hemispherical Si lens of 6 mm diameter shows a realized antenna gain of 15 dBi at 240 GHz (see Fig. 9.23(b)). Therefore, the total loss incurred by the spiral Klopfenstein taper, the microstrip line T-junction, the DT-based power splitters and the quasi-differential feed lines feeding the monopoles is calculated as 7.1 dB. Consequently, an excellent agreement is achieved between the theoretical gain of a lens antenna and the measured realized gain of the four-feed differential antenna integrated with a 6 mm diameter Si lens [350].



(a) Reflection coefficient



(b) Realized antenna gain

Figure 9.23
Measurement and simulation result of four-feed differential antenna with 6 mm diameter hemispherical silicon lens. From [350] © 2016 IEEE

9.4.2.6 Four-Feed Differential Antenna with 12 mm Si Lens and Power Amplifiers

An active antenna is realized by connecting a four-feed differential antenna to four single-stage power amplifiers. The single-stage power amplifier has a pseudo-differential cascode topology and a simulated gain of 5.1 dB. All four amplifiers require a current of 124 mA and a voltage supply of 4 V. Note that the power amplifier mentioned here differ from the one described in section 9.3.3.2. The power amplifier was designed at a center frequency of 240 GHz, however after fabrication, the operating center frequency was found to be shifted to 210 GHz [350]. In order to achieve an impedance matching between the power amplifiers and the four-feed differential antenna, DT-based power splitters with 12.5 Ω quasi-differential feed lines are used for the active antenna. A micrograph of the antenna prototype is shown in Fig. 9.24.

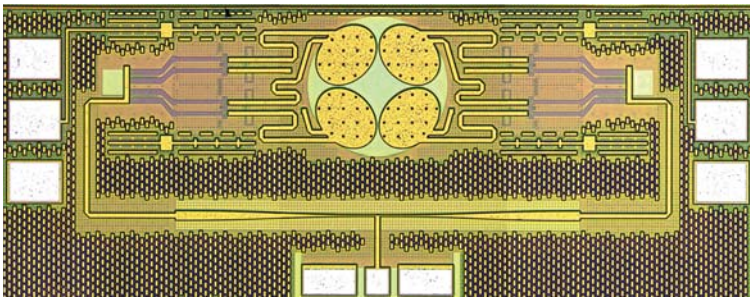


Figure 9.24
Micrograph of the fabricated four-feed differential antenna connected with four differential amplifiers. From [350] © 2016 IEEE

The active antenna prototype is integrated with a hemispherical Si lens of 12 mm diameter. After integrating the lens to the antenna, the RDL containing the DC signals is mounted on one side of the lens surface. The DC signal lines on the RDL are connected to the active antenna by means of standard wirebonds. The other side of the lens surface is kept free in order to enable probe-based antenna measurement. The simulated radiation pattern of the antenna is shown in Fig. 9.25. The measurement and simulation results of the antenna with and without power amplifiers are shown in Fig. 9.26. The antenna simulation is performed by setting up a magnetic symmetry plane, which passes through the center of the coplanar waveguide pads, i.e. only one half of the chip is simulated to save the simulation time and effort. Further, four waveguide ports are used at the input of the four quasi-differential feed lines. These waveguide ports are set up before the feed lines are crossed over. The simulated S parameters of the power amplifiers are included in the simulation. The measured and simulated antenna gain with amplifier are found to be in very good agreement up to 210 GHz. The maximum value of mea-

sured antenna gain is 24.9 dBi at 210 GHz. At frequencies above 210 GHz, the negative slope of the measured antenna gain (with amplifiers) is found to higher than the simulated antenna gain (with amplifiers). This observation is consistent with the fact that the power amplifier was initially designed at a center frequency of 240 GHz, however the center operating frequency of the fabricated power amplifier was found to be 210 GHz. Finally, the amplifier gain is calculated by subtracting the measured active antenna gain (i.e. with amplifiers) from the simulated passive antenna gain (i.e. without amplifiers).

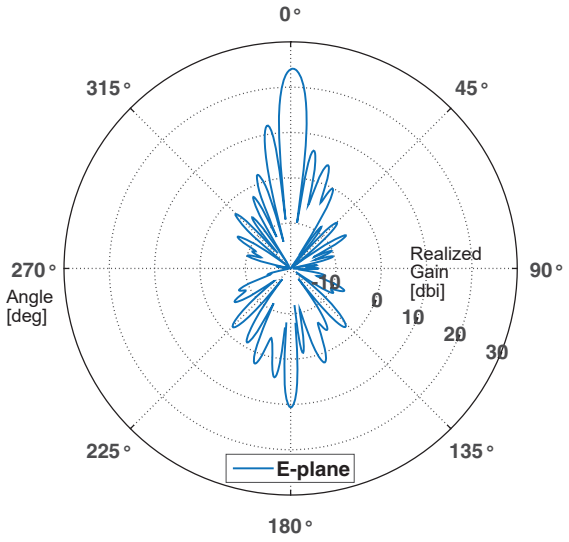
The calculated amplifier gain shows a peak value of 5.1 dB at 210 GHz, which shows an excellent agreement with the corresponding simulated amplifier gain. The deviation between the measured and simulated amplifier gain at frequencies above 210 GHz could be attributed to non-ideal transistor models of the SiGe technology, since the transistors are operating at the upper limit of the transit frequency [350]. Other ILA variants are shown in [369], [370] and [371].

9.5 Packaging of Miniaturized 240 GHz Transceiver Frontend

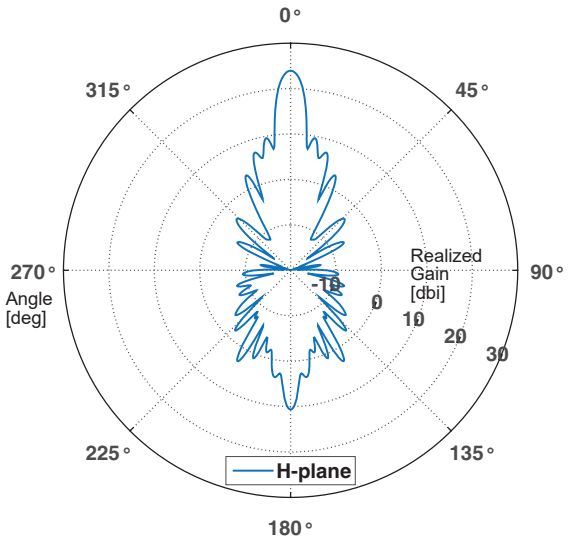
9.5.1 Bandwidth limitations

The two key factors, which limit the baseband bandwidth of the miniaturized 240 GHz transceiver frontend are as follows.

Wirebond interconnect: In the ILA-based SoC package concept shown in Fig. 9.2, the 240 GHz SiGe Tx or Rx MMIC is placed in the middle of an RDL. The chip and RDL are interconnected using 17 µm diameter gold (Au) wirebonds in wedge-wedge configuration. At low frequencies, where the electrical length of a wirebond is much less than the operating wavelength, a wirebond acts as a series inductance and its bond pads act as parallel capacitances; hence a wirebond interconnect acts a low pass filter. As the frequency increases (i.e., the electrical length of a wirebond becomes a significant fraction of the operating wavelength), the parasitic effect associated with a wirebond interconnect increases, leading to undesired resonances. Ideally, the wirebond connecting the chip and RDL should be kept as short as possible. However, the following factors lead to an extension of the wirebond length. First, the dicing limit of the chip and RDL. The dicing limit defines the distance between the bond-pad edge and the chip- or RDL-substrate edge. In this work, the dicing limit of the chip and RDL are 235 µm and 50 µm, respectively. Second, the difference in the height of the chip- and RDL substrate, which in this case is around 430 µm. Third, the loop height and the foot placement of the wirebond

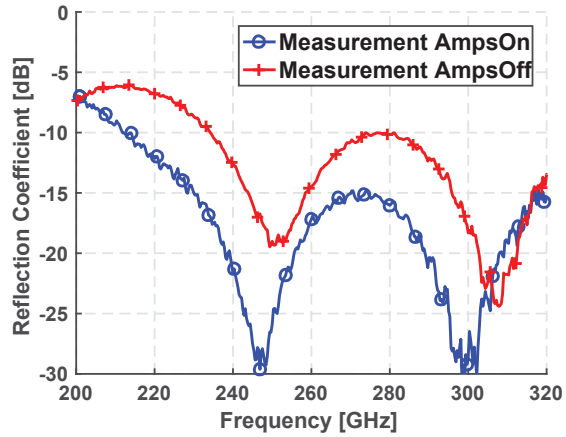


(a) E-plane

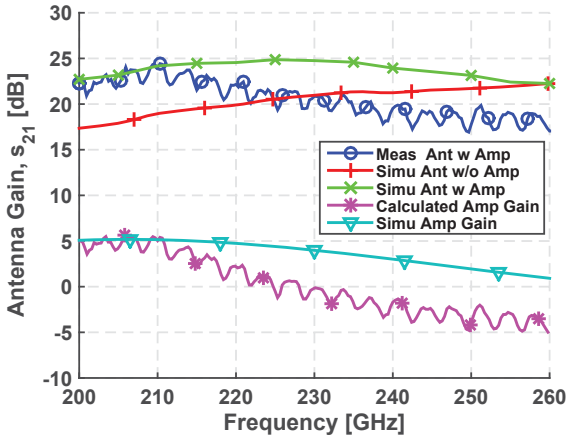


(b) H-plane

Figure 9.25
Simulated radiation pattern of four-feed differential antenna connected integrated with a 12 mm diameter hemispherical silicon lens. From [350]



(a) Reflection coefficient



(b) Realized antenna gain

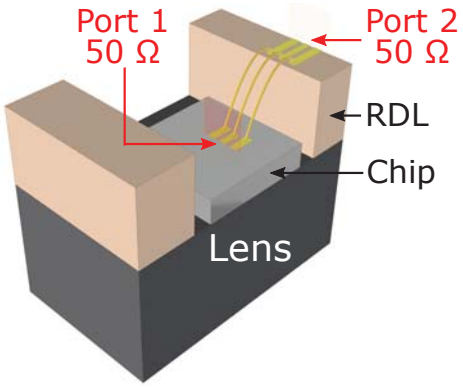
Figure 9.26
Measurement and simulation result of four-feed differential antenna connected with and without four differential amplifiers. The antenna is integrated with a 12 mm diameter hemispherical silicon lens. From [350] © 2016 IEEE

interconnect also contribute to its overall length. Ideally, it is desired that the loop height is kept as small as possible and the wirebond foot is placed as close as possible to the bond-pad edge. In this work, a semi-automatic wirebonding machine is used to achieve a loop height of around 60 µm above the RDL substrate and the wirebond foot is placed at a distance of around 25 µm from the bond-pad edge. Note that these values may vary due to manufacturing tolerances. The abovementioned parameters are used to construct a simulation model of a chip-to-RDL wirebond interconnect as shown in Fig. 9.27(a). The wirebonds are in ground-signal-ground (GSG) configuration. The model is simulated using CST Microwave Studio and the resultant S parameters are shown in Fig. 9.27(b). It is observed that up to 11 GHz, the simulated reflection coefficient (S_{11}, S_{22}) is less than −10 dB and the simulated transmission coefficient (S_{21}, S_{12}) is greater than −0.8 dB. The performance of the wirebond interconnect could be improved by reducing the dicing limit and by reducing the height difference between the chip and the RDL substrate. Additionally, ribbon wirebonds could be used instead of the conventional round wirebonds to improve the bandwidth of the wirebond interconnects. Note that if a ribbon and round wire have a similar cross section area, then the surface area of the ribbon wire is greater than the round wire. Therefore, at higher frequencies, a ribbon wirebond carries larger current (i.e., due to skin effect) than a round wire of similar cross section area. The dimensions of the smallest ribbon wire available are 50 µm × 12.5 µm, which requires bond pads of around 100 µm × 100 µm. Since the bond-pads of the 240 GHz transceiver MMIC have a smaller size of 68 µm × 86 µm, wedge-wedge wirebonds are preferred instead of ribbon wirebonds for manufacturing the package.

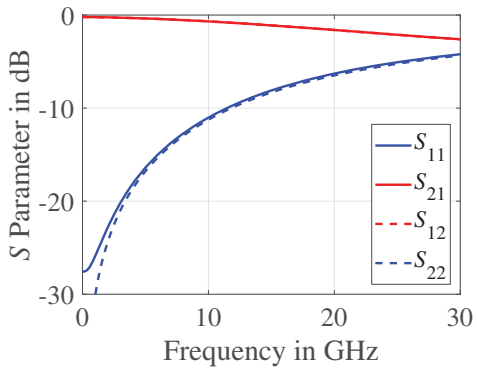
Package height: In the ILA-based SoC package concept described in section 9.2.2, the signals from the RDL are routed to a PCB, via an open-cavity QFN package base. The QFN package base consists of the following components. First, a lead frame on the top- and bottom-side of the QFN. A lead frame consists of a series of bond pads, located on the periphery of the QFN. The top lead frame is connected to the RDL by means of flip chip Au bumps and the bottom lead frame is connected to the PCB by means of solder balls. Second, the top and bottom lead frames are connected by means of vias. Third, an air cavity in the middle of the QFN. The package height plays a crucial role in determining the bandwidth limitation of the overall package. This can be understood from the following points:

i A larger package height implies that the vias connecting the top and bottom lead frames also have a larger height. Since the impedance of these vias is usually less than 50 Ω, they act as an impedance discontinuity between the top and bottom lead frames. Therefore, in order to minimize this impedance discontinuity, the via height should be kept as small as possible i.e., a smaller package height is favorable in terms of bandwidth.

ii As the package height decreases, the air cavity in the middle of the package also decreases in height, which in turn leads to two undesired effects. First,



(a) Simulation model



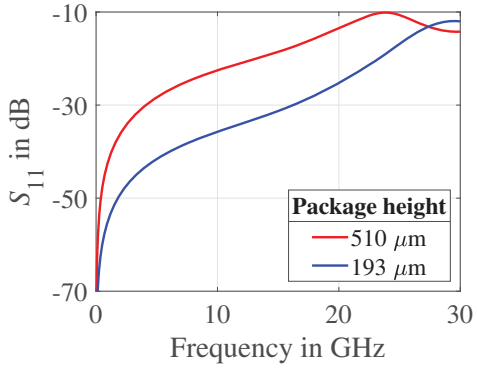
(b) Simulated S parameters

Figure 9.27
Bandwidth limitation due to wirebond interconnect.

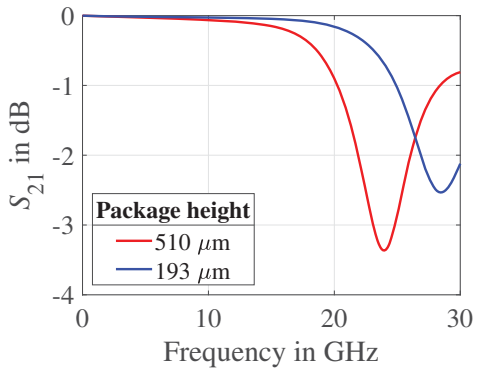
the distance between the on-chip ILA and the QFN package base decreases, which degrades the realized antenna gain and the total antenna efficiency as shown in Table 9.3. Second, the mechanical assembly of the package becomes difficult, since the wirebond interconnects between the chip and the RDL are suspended in the air cavity of the QFN package base.

iii The manufacturability of the QFN package base is taken into consideration. For this purpose, a multilayered technology is required such as low temperature co-fired ceramic (LTCC) technology. A wide variety of LTCC substrates are available, which have excellent electrical, thermal and mechanical characteristics, however LTCC technology has certain manufacturing limitations. Two of these limitations, which are relevant for manufacturing a broadband QFN package base are as follows. First, most of the commercially-available LTCC substrates have a minimum layer thick-

ness of around 100 µm. Second, LTCC modules are manufactured using at least two to three substrate layers. If the LTCC module is too thin (i.e. if the number of LTCC layers are too less), then warpage of LTCC module might occur during its manufacturing process (During the manufacturing process, LTCC modules are sintered at high temperature (800 to 1000 °C) and pressure; hence an LTCC module gets deformed if it is too thin). Third, the smallest possible via diameter that can be realized using standard LTCC technology is limited.



(a) Reflection coefficient S_{11}



(b) Transmission coefficient S_{21}

Figure 9.28
Bandwidth limitation due to package height

Taking the abovementioned points into consideration, sections of two different LTCC-based QFN packages are simulated. One of the simulation models is shown in Fig. 9.28(a). It consists of three 50 Ω GSG bond pads on top- and bottom-side of the LTCC substrate. The bond pads are connected by vias of 175 µm diameter (i.e., via diameter specified by the LTCC manufacturer). The simulation models mainly differ in terms of their package height i.e.,

510 µm and 193 µm. The simulated reflection coefficient (S_{11}) and the simulated transmission coefficient (S_{21}) are shown in Fig. 9.28(a) and Fig. 9.28(b), respectively. It is observed that the package with a height of 510 µm provides a bandwidth of up to 20 GHz and the package with a height of 193 µm provides a higher bandwidth of up to 25 GHz (i.e., S_{11}<−10 dB and S_{21}>−1 dB).

9.5.2 Thermal management

As mentioned previously in 9.2.2.3, the SiGe Tx chip used in this work has a power consumption of 2.9 W and its surface area is around 5.6 mm^2, which generates a heat flux of approximately 518 kW/m^2. The maximum operating temperature of a typical semiconductor chip is around 100 °C. However, the goal of this section is to attain a much lower junction temperature, i.e., in the range of 50 to 60 °C, in order to achieve an optimal performance of the Tx chip. There are two key concepts in thermodynamics, which are essential for thermal management. First, the flow of thermal current is analogous to the flow of electrical current. An electric current flows from higher to lower potential and its flow is hindered by an electrical resistance. Similarly, a thermal current flows from higher to lower temperature and its flow is hindered by a thermal resistance as shown by Eq. 9.5.

$$Q = \frac{\Delta T}{R_{\text{th}}} \tag{9.5}$$

In Eq. 9.5, Q, ΔT and R_{th} denote thermal current (J/s), temperature difference (K) and thermal resistance (K/W), respectively. The second concept is that of thermal resistance, which is given by Eq. 9.6.

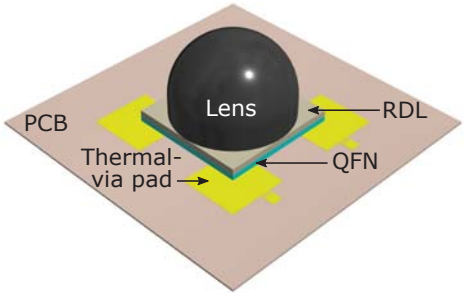
$$R_{\text{th}} = \frac{l}{\lambda A} \tag{9.6}$$

In Eq. 9.6, l, A and λ denote the thermal path length, the cross section area over which the heat is dissipated and the thermal conductivity (W/mK), respectively. Based on these two key concepts, it is clear that an efficient heat dissipation requires the following.

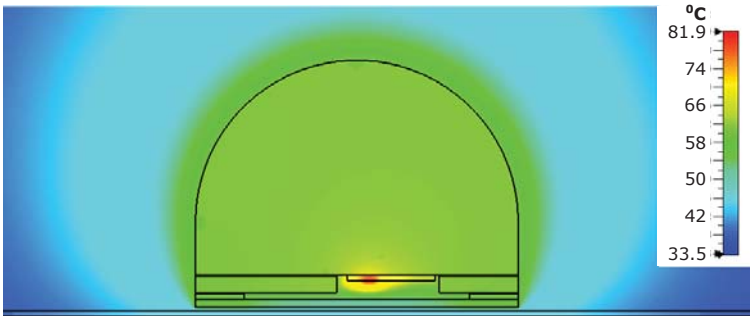
- Reduction of the thermal path length
- Increasing the cross section area
- Using materials with high thermal conductivity

In the ILA-based SoC package concept (see Fig. 9.2), the SiGe MMIC is glued to a Si lens using a thermally-conductive epoxy adhesive named Polytec TC 430-T. The Si lens has a diameter of 12 mm and its thermal conductivity is 148 W/mK, which is less than metals e.g., Cu (385 W/mK), however, it is several orders of magnitude higher than dielectrics e.g., Alumina (30 W/mK). On the other hand, the thermal conductivity of Polytec

TC 430-T is merely 0.7 W/mK. As previously mentioned, the thermal conductivity of Polytec TC 430-T is significantly less than Ag based epoxies, however its bond line thickness (5 µm) is nearly ten times less than Ag based epoxies (50 µm). Therefore, Poyltec TC 430-T helps in reducing the thermal path length between the MMIC (i.e. the heat source) and the Si lens (i.e. the heat sink), which provides a low thermal resistance value. Using Eq. 9.6, the thermal resistance values of the Si lens and the Polytec-based adhesive layer are calculated as $(6\,\text{mm})/[(148\,\text{Wm}^{-1}\text{K}^{-1})(36\pi\,\text{mm}^2)] = 0.36\,\text{K/W}$ and $(5\,\mu\text{m})/[(0.7\,\text{Wm}^{-1}\text{K}^{-1})(36\pi\,\text{mm}^2)] = 0.063\,\text{K/W}$, respectively. It is observed that although the thermal conductivity of Polytec is significantly less than Si, the thermal resistance of the Polytec layer is still five times less than the Si Lens, owing to its minimum bond line thickness of 5 µm. The ILA-based SoC package concept is simulated using the Thermal steady state solver of the CST studio suite software. Further, a cooling concept has been developed for the package. The thermal simulation result of the package with and without using the cooling concept are discussed next.



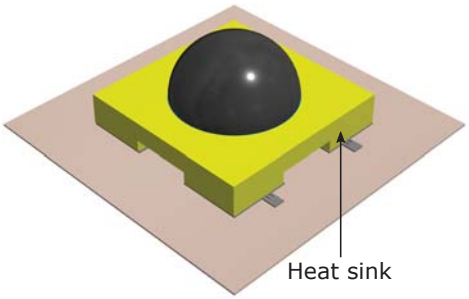
(a) Simulation model



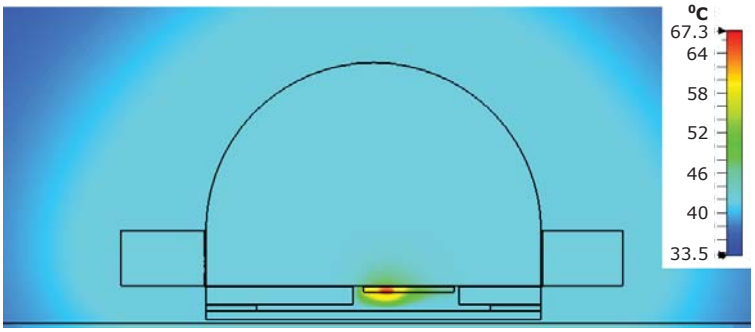
(b) Simulation result

Figure 9.29
Thermal simulation of QFN package without heat sink

A simplified thermal simulation model of the ILA-Based SoC Package using a QFN base is shown in Fig. 9.29(a). The QFN is mounted on a PCB made



(a) Simulation model



(b) Simulation result

Figure 9.30
Thermal simulation of QFN package with heat sink

of Rogers RO4003C substrate, which has a size of 30 mm×30 mm. The PCB includes four thermal-via pads (i.e., each metal pad is backed by dozens of thermal vias), which are soldered to the thermal-via pads of the QFN base. The model is simulated using the thermal steady state solver of the CST studio suite software. The key parameters used in this simulation are as follows: the SiGe Tx MMIC with a power consumption of 2.9 W acts as the heat source, the ambient temperature is specified as 30 °C and open boundary conditions are used. Only conduction and convection are considered as the modes of heat transfer. In terms of conduction, the simulation relies on the thermal conductivity values of the various materials used in the thermal simulation model, which are shown in Table 9.5. In terms of convection, the simulation relies on the convective heat transfer coefficient of the surfaces, which are in direct contact with the surrounding medium (i.e. air). For static air, the convective heat transfer coefficient usually lies in the range of 5 to 10 $W/m^2/K$. The simulated heat distribution along a cross section of the the package is shown in Fig. 9.29(b). It is observed that the maximum chip temperature lies at 81.9 °C and the temperature of the lens is around 65 °C. Note that the

heat is predominantly dissipated through the Si lens. Additionally, a small amount of heat is dissipated through the thermal-via pads, since the path length from the heat source (i.e., the Tx MMIC) to the thermal-via pads is much longer than to the Si lens. A standard low-cost passive heatsink e.g. Aluminum (Al) or Copper (Cu) extruded heatsink with fins, which support natural convection, could be placed beneath the PCB, however this approach will again lead to a much longer thermal path length. Therefore, an Al-based heatsink of dimensions 18 mm×18 mm×3 mm is designed, as shown in the modified thermal simulation model in Fig. 9.30(a). The heatsink is mounted around the QFN base and it is directly connected to the Si Lens by means of a Polytec layer. The simulated heat distribution along a cross section of this model is shown in Fig. 9.30(b). The maximum chip temperature in this case is observed to be 67.3 °C. Hence, the heatsink helps in reducing the chip temperature by nearly 15 °C.

Table 9.5
Thermal conductivity values of materials used in the thermal simulation

Material	Thermal conductivity (W/mK)
Si (MMIC)	148
LTCC CS71 (QFN)	4.6
Alumina (RDL)	30
Au (QFN & RDL)	314
Polytec TC 430-T (Adhesive)	0.7
Solder (QFN-to-PCB interconnect)	64
RO4003C (PCB)	0.64
Cu (PCB)	401
Al (Heatsink)	237

9.5.3 Compact Cube

The usage of an LTCC-based QFN in the proposed ILA-based SoC package concept leads to two major bottlenecks, which are as follows.

- The baseband bandwidth is limited by the height of the LTCC-based QFN, which can be reliably manufactured using a standard LTCC manufacturing process.
- The thermal conductivity of LTCC is relatively low, which leads to a high chip temperature of 81.9 °C. A passive cooling concept is used in the form of an Al heat sink, which reduces the chip temperature to 67.3 °C; however the chip temperature needs to be further reduced in order to achieve the desired transceiver performance.

Taking into account the abovementioned considerations, the ILA-based SoC package concept is modified. The modified package concept is termed as 'Compact Cube' and it is shown in Fig. 9.31.

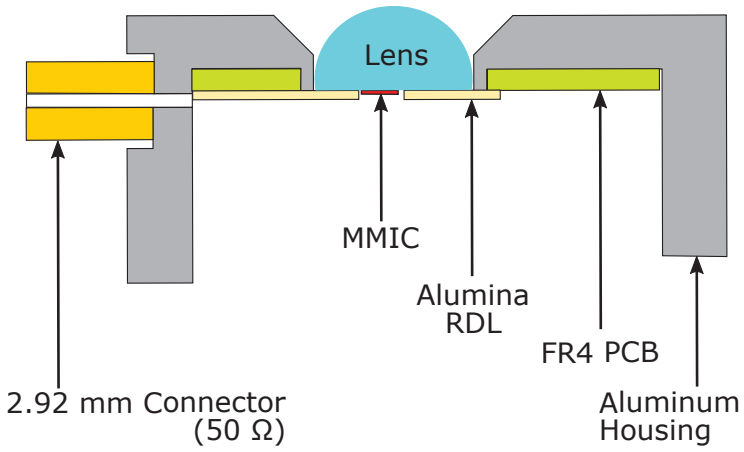


Figure 9.31
Compact cube concept

Similar to the QFN-based package concept (shown in Fig. 9.2), the MMIC including the on-chip antenna is glued face down to a 12 mm diameter Si lens using thermally-conducting, electrically-insulating epoxy adhesive Polytec TC 430-T. The position of the MMIC on the Si lens is precisely controlled such that the focal point of the lens is aligned with the phase center of the on-chip antenna. An Alumina-based RDL with a size of 20 mm × 25 mm and a thickness of 635 µm is used to fan out the DC and baseband signal lines on the MMIC. The Alumina RDL is manufactured using direct laser writing, which provides a high resolution of less than 10 µm. A cavity of size 3.3 mm × 2 mm (i.e. for Tx module) is cut in the middle of the RDL such that the MMIC can be placed within the cavity. Similar to the MMIC, the RDL is also glued to the Si lens using Polytec TC 430-T. Next, the DC and baseband signal lines on the MMIC and RDL are connected using 17 µm diameter Au wirebonds in wedge-wedge configuration. The baseband signal lines on the Alumina RDL are directly routed to 50 Ω 2.92 mm connectors, which are mounted on the walls of an Al metal housing. The less critical DC signal lines are routed to a pin header on an FR4 PCB, which is located beneath the Alumina RDL. Further, the Alumina RDL and the FR4 PCB are connected using soldered Cu wires. The overall size of the Tx compact cube, i.e. the overall size of its Al metal housing is 35 mm × 20 mm × 40 mm. The Tx compact cube is shown in Fig. 9.32.

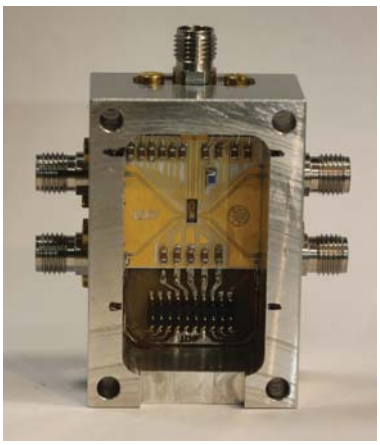
(a) Back view (b) Front view

Figure 9.32
Tx module - compact cube

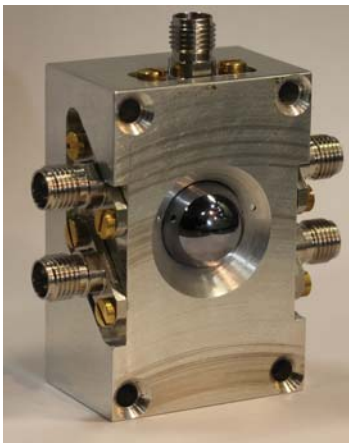
The Rx compact cube shown in Fig. 9.33 is built in the same way as the Tx compact cube. Five 50 Ω 2.92 mm connectors are mounted on the Al metal housing of the Rx compact cube, which are used for routing the differential in phase and quadrature signals and the LO signal. The overall size of the Rx compact cube is 20 mm × 30 mm × 45 mm. The compact cube provides the following benefits in contrast with the QFN-based package concept.

- The baseband signals on the MMIC are routed via 50 Ω coplanar waveguide structures on the Alumina RDL to 50 Ω 2.92 mm connectors. Therefore, unlike the QFN-based package concept, the baseband bandwidth is not limited by the LTCC QFN height. Note that in this case, the baseband bandwidth is only limited due to the wirebonds connecting the MMIC and the Alumina RDL.
- The massive heat flux generated by the Tx MMIC is dealt with in the following ways. First, the thermal conductivity of the Al metal housing is nearly two hundred times larger than the LTCC QFN. Second, the cross section area of the Al metal housing is two to three times larger than the LTCC QFN and the passive heat sink surrounding it (shown in Fig. 9.30(a)).
- An active cooling concept is used to lower the chip temperature. The concept uses a peltier element and a cooling fan, which are mounted on the backside of the Al metal housing.

A communication link measurement using an older version of Tx and Rx compact cubes is shown in [372]



(a) Back view



(b) Front view

Figure 9.33
Rx module - compact cube

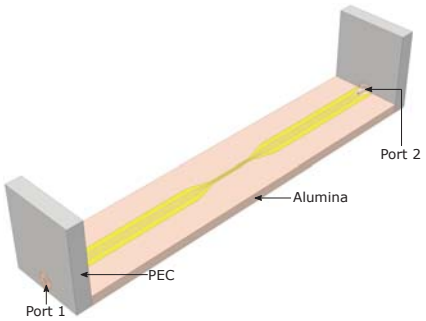
9.5.3.1 Bandwidth of Compact Cube

The baseband bandwidth of the compact cube concept is determined based on the simulation and measurement of a daisy chain shown in Fig. 9.34.

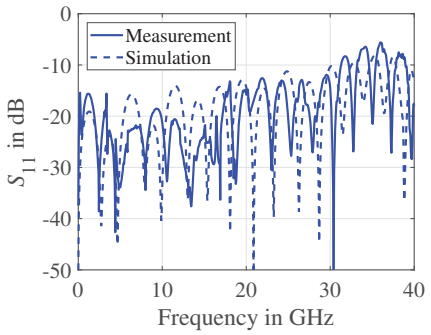
The daisy chain consists of a 50 Ω coplanar waveguide formed on an Alumina substrate of 635 µm thickness. The coplanar waveguide is connected to two 50 Ω 2.92 mm connectors, which are mounted on either side of an Al metal housing. The simulated and measured reflection coefficient (i.e. S_{11}) and transmission coefficient (i.e. S_{21}) of the daisy chain are shown in Fig. 9.34(b) and Fig. 9.34(c), respectively. A very good agreement is observed between the simulation and measurement result. From DC to 30 GHz, the measured $S_{11} < -10$ dB and the measured $S_{21} > -3$ dB (i.e. the single-ended insertion loss is less than 1.5 dB).

9.5.3.2 Active Cooling Concept

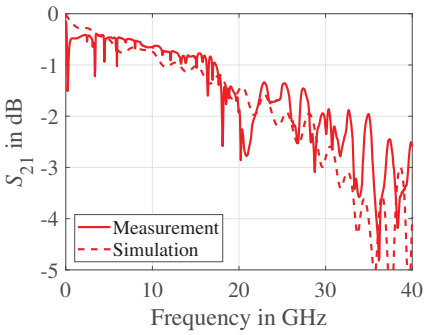
A peltier element based thermoelectric cooling system is used to transport the heat generated by the compact cube to the ambient air. The direction of heat transport depends on the direction of current that flows through the peltier element. In this setup, the compact cube is attached to the 'cold' side (i.e. heat absorption side) of the peltier element. Additionally, a fan is attached to the 'hot' side (i.e., heat dissipation side) of the peltier element. The key parameters of the peltier element used in this setup are shown in Table 9.6. Q_{max} denotes the maximum heat pumping capacity of a peltier element, if the temperature difference between its hot and cold sides is 0 K. The current and



(a) Simulation model



(b) Reflection coefficient S_{11}



(c) Transmission coefficient S_{21}

Figure 9.34
Compact cube daisy chain

voltage associated with the maximum heat pumping capacity are given by I_{max} and V_{max}, respectively. ΔT_{max} is the maximum temperature difference across the peltier element, when no heat is pumped.

Table 9.6
Key parameters of peltier element

Parameter	Value
ΔT_{max}	67 °C
Q_{max}	52 W
I_{max}	4.6 A
V_{max}	15.4 V

Note that the peltier element itself produces a certain amount of heat, which depends on its operating electric current (i.e., $I_p^2 R$). As the operating electric current (I_p) approaches I_{max}, a large amount of heat is generated by the peltier element, which may exceed the heat that needs to be pumped out of the compact cube. In this case, the thermoelectric system would reach a state of thermal runaway and hence become counterproductive. Therefore, the operating electric current of the peltier element is determined in the following manner. A thermal simulation shows that the temperature of the compact cube without any thermoelectric cooling concept is 67 °C. The desired temperature of the compact cube is assumed to be 37 °C; hence a temperature difference of $\Delta T = 30$ K is required between the hot and cold sides of the peltier element (Note that this value is kept much lower than the ΔT_{max} in order to obtain an optimal performance). The required heat pumping capacity is $Q_c = 2.9$ W (i.e. the power consumption of the Tx chip). Further, the operating electric current required for a heat pumping capacity of $Q_c = 0.056 Q_{max}$ and a temperature difference of $\Delta T = 30$ K is given by $I_p = 0.3 I_{max} = 1.3$ A and the operating voltage is 5.4 V. The values of operating current and voltage are obtained from the plots shown in [373]. The heat rejected by the peltier element at this operating point is nearly 3.5 times the heat pumping capacity.

9.6 Transmitter & Receiver Characterization

9.6.1 Transmitter Characterization

9.6.1.1 TX Characterization Setup

The transmitter was characterized using the setup shown in Fig. 9.35. An Agilent E8257D generates the reference LO, which the ×16 multiplier chain translates into the carrier frequency f_c. Another Agilent E8257D signal generator is connected to a single K-connector corresponding to either I or Q-channel

and supplies the baseband signal of frequency f_{BB} with power P_{BB}. A rotational stage is used to align the transmitter polarization to the 19 dBi horn antenna of a 220 GHz to 325 GHz OML mmWave extender module in down-conversion configuration. The transmitter was characterized in its intended direct-conversion function, therefore both lower side-band (LSB) and upper side-band (USB) and the respectively placed second and third harmonic tones were recorded. The pertinent reference frequency for the extender module is chosen to result in an offset frequency of 33 MHz, which is recorded with an Agilent E4440A spectrum analyzer.

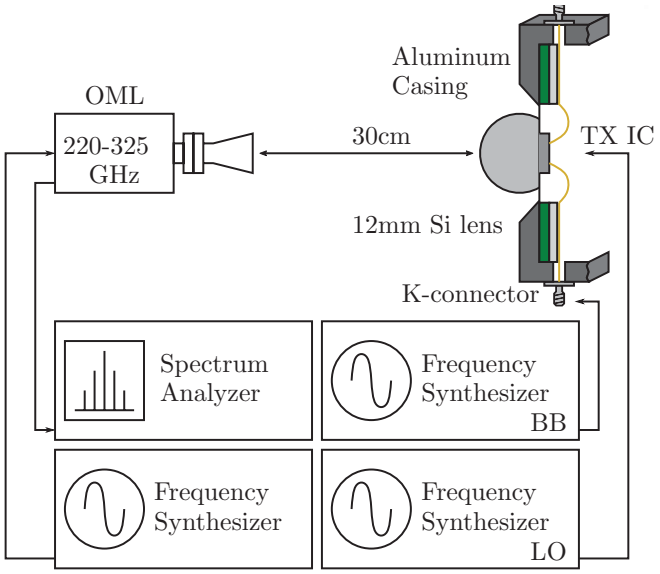


Figure 9.35
Transmitter measurement setup. The Tx is mounted on a rotational stage for the antenna characterization.

9.6.1.2 TX Characterization Results

Fig. 9.36 presents the Tx antenna pattern for a carrier frequency of 220 GHz and 0.5 GHz BB frequency. Additionally, the antenna patterns for carrier frequencies up to 240 GHz were recorded. Each respective realized gain was calculated by integrating over the acquired power density values, while neglecting back radiation. At all measured frequencies, the realized gain stays a constant 26.8 dBi. Note that the realized gain of the Tx antenna shown in Fig. 9.26(b) differs from the measurement value shown here, since the power amplifiers used in these two cases are different.

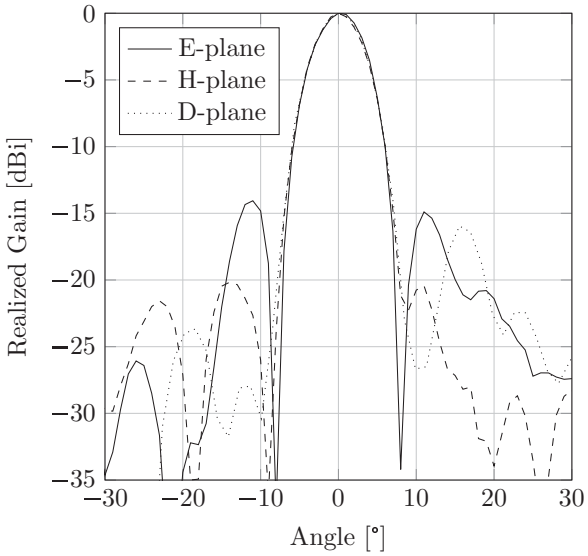


Figure 9.36
Measured antenna pattern of the transmitter

At the center of the main beam, the cross-polar realized gain in the E- and H-plane is XX.X dBi.

The Tx has a linear gain of 33 dB in the USB of the I-channel for an f_c of 220 GHz and an f_{BB} of 0.5 GHz. At -35.2 dBm input power, the 1-dB compression point is reached, where an output power of -3.2 dBm was measured. As Fig. 9.37 shows, the second harmonic is at -30.6 dBm and the third is at -33.1 dBm at this point. The output power saturates at 1.1 dBm.

Fig. 9.38 shows the frequency behaviour in both I and Q-channel at the 1-dB compression point. A total bandwidth of 11.5 GHz was measured, spanning from 217 GHz to 228.5 GHz.

In total, the transmitter consumes 2900 mW of DC power.

9.6.2 Receiver Characterization

9.6.2.1 RX Characterization Setup

The receiver was characterized using the measurement setup depicted in Fig. 9.39. An OML mmWave extender module in transmit mode is placed at 30 cm distance to the fully packaged receive module, which is mounted on a rotational stage for polarization alignment. Similar to the transmitter measurement setup, an Agilent E8257D supplies the LO signal. Phase-matched cables feed the differential baseband output of the receiver into an exter-

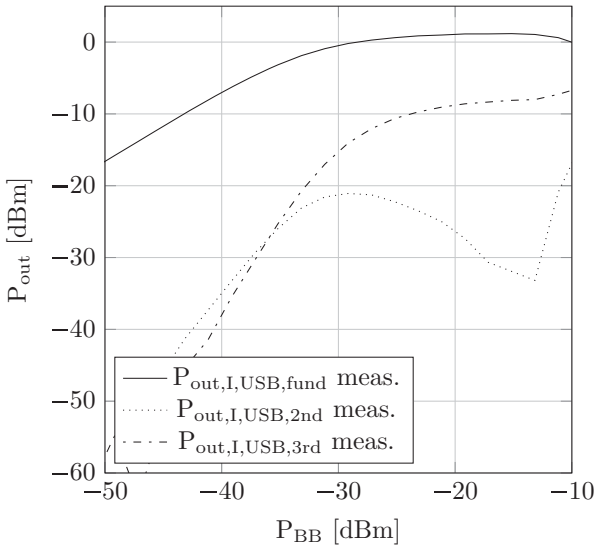


Figure 9.37
Measured and simulated fundamental and harmonic output power vs. input power of the transmitter at 0.5 GHz baseband and 220 GHz carrier frequency.

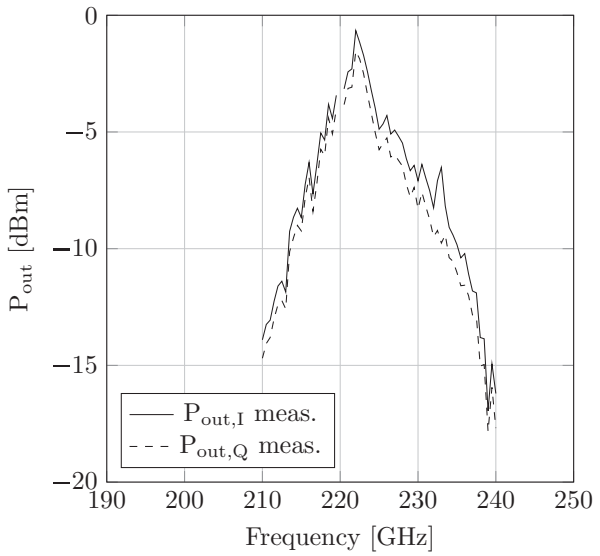


Figure 9.38
Measured and simulated output power of the transmitter over frequency at the 1-dB compression point.

nal Marki broadband balun. An Agilent E4440A spectrum analyzer allows the characterization of the conversion gain up to a baseband frequency of 26.5 GHz.

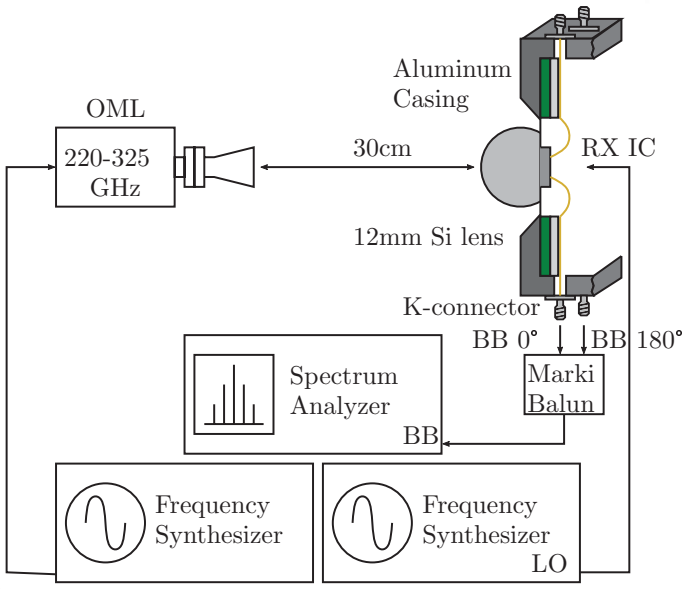


Figure 9.39
Receiver measurement setup. The Rx is mounted on a rotational stage for the antenna characterization.

9.6.2.2 RX Characterization Results

Fig. 9.40 presents the Rx antenna pattern for a carrier frequency of 220 GHz and 33 MHz BB frequency. The realized gain stays at a constant 27.1 dBi over all measured frequencies.

The respective VGA at the output of both I and Q-channel in the Rx compensates the conversion-loss of the mixer first topology with its broadband input-match. In the USB of the I-channel for an f_c of 220 GHz, the Rx shows a linear gain of 1 dB at an f_{BB} of 0.5 GHz and 5 dB at an f_{BB} of 20.5 GHz, see Fig. 9.41. The gain drops by 3-dB at an RF frequency of 245.5 GHz in USB. Characterizing the 3-dB bandwidth in the lower side band was not possible due to the cut-off of the OML module.

Because no noise sources were available, the noise figure of the receiver was calculated using the direct method [374]. Assuming that the input noise floor N_{in} equals the thermal noise at room temperature with -174 dBm/Hz, dividing the output noise N_{out} read off of the spectrum analyzer with the product of conversion gain CG and N_{in} results in the noise figure.

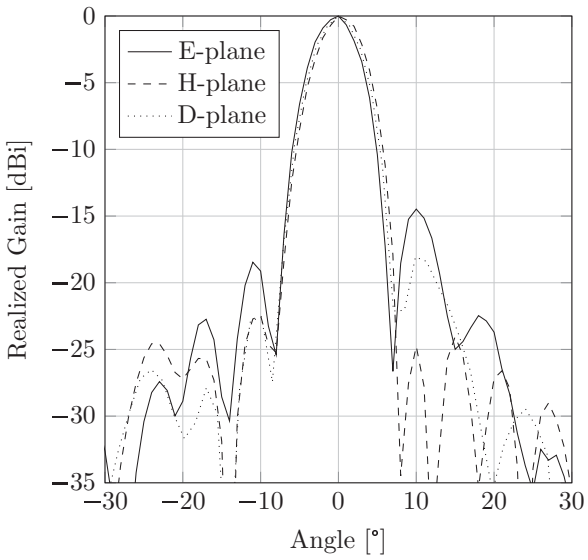


Figure 9.40
Measured antenna pattern of the receiver

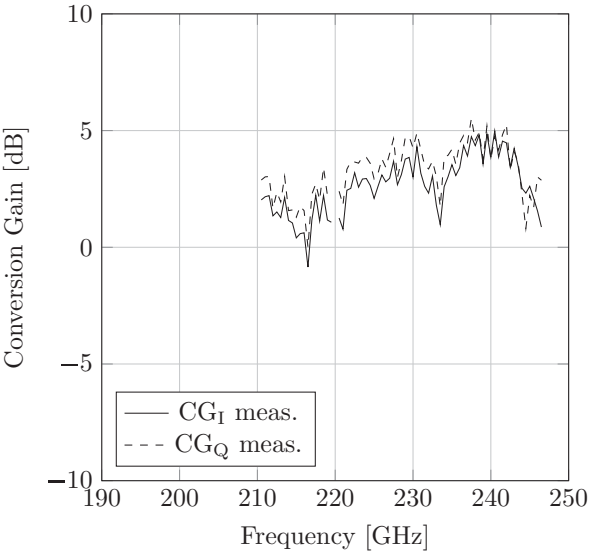


Figure 9.41
Measured and simulated conversion gain of the receiver over frequency

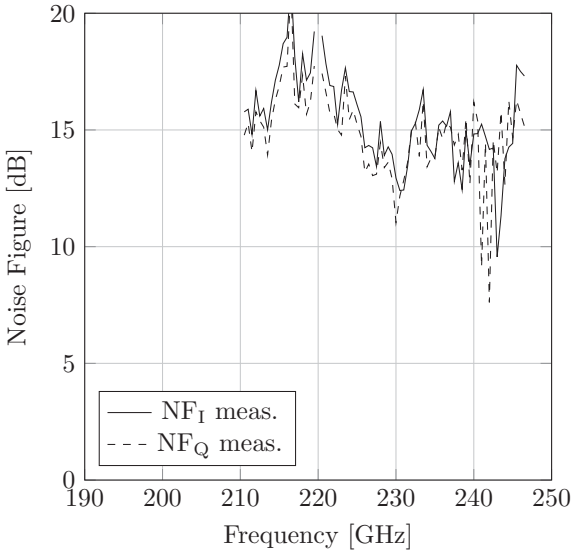


Figure 9.42
Measured and simulated noise figure of the receiver over frequency

$$\mathrm{NF} = 10 \cdot log_{10}\left(\frac{N_{\mathrm{out}}}{\mathrm{CG} \cdot \mathrm{N_{in}}}\right)$$

As can be seen in Fig. 9.42, the noise figure shows an inverse relationship with the measured conversion gain, with an NF of 14.8 dB at the peak gain in the USB.

In total, the receiver consumes 910 mW of DC power.

9.6.3 Communication Demonstration

9.6.3.1 Measurement Setup

The setup used for measuring data-rates is shown in Fig. 9.43. A pair of Tektronix AWG70001A with a sampling rate of 50 GS/s each feed quadrature data streams to the Tx. A pseudo-random bit sequence of order 9 resulting in a stream length of 2^9-1 was pulse-amplitude modulated (PAM) in each of the AWG outputs. A root raised cosine filter with an α between 0.1 and 0.7 was applied to the data stream for pulse shaping to reduce the effective bandwidth of the baseband signal.

The Rx was placed in a 50-cm line-of-sight distance. Its differential output signals run through a set of PSPL5882 broadband amplifiers to improve the SNR at the two Tektronix DPO77002SX high speed oscilloscopes with 100 GS/s each. The captured signal was post-processed using the SignalVu

vector signal analysis software. It analyzes the EVM, constellation and eye diagram in real time and facilitates clock recovery and IQ imbalance correction. An adaptive decision-directed FIR feed-forward equalizer with 51 taps was applied to the received signal. All EVM values shown in this paper refer to the average power of all symbol vectors within the used constellation for normalization [375] and are directly read off the SignalVu oscilloscope software as previously described. No further post processing has been done.

All baseband signals are routed via phase-matched cables. The setup was covered with absorbers to avoid multipath and standing wave effects caused by reflections. An Agilent E8257D signal generator supplies the LO drive for both Tx and Rx, which are phase aligned through external phase shifters and polarization aligned with a rotational stage.

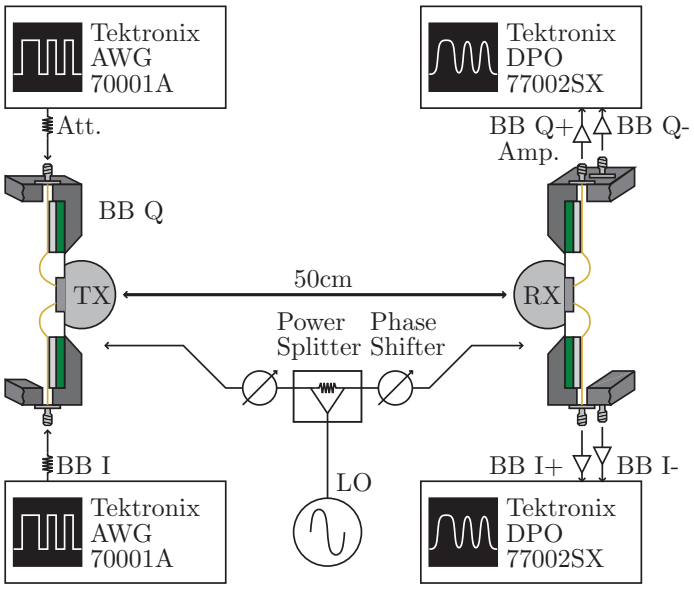


Figure 9.43
Communication measurement setup. The Tx and the Rx are placed at 50 cm distance. They are fed from the same LO and phase aligned through external phase shifters.

9.6.3.2 Measured Results

The tunable ×16 multiplier chain enables placing the carrier at frequencies inside the bandwidth of the PA. The maximum data-rates were found with a 220 GHz carrier. Three different modulation schemes were tested: quadrature phase shift keying (QPSK), quadrature amplitude modulation with 16 symbols (16-QAM) and 32 symbols (32-QAM). In each, increasing data-rates were

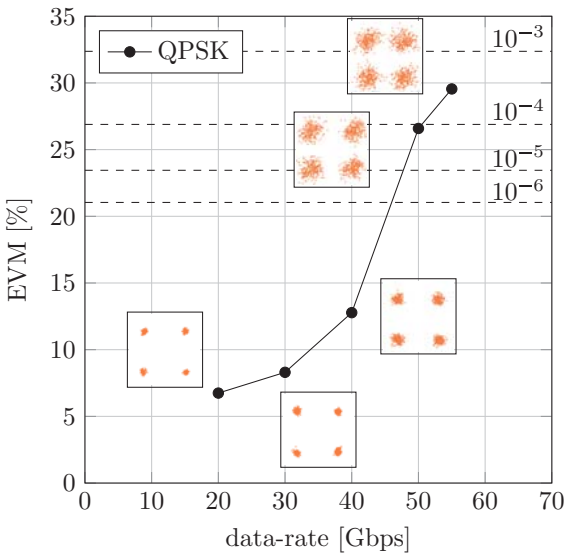


Figure 9.44
Measured EVM for different data-rates using QPSK with a 220 GHz carrier frequency.

applied and the respective EVM was recorded. To evaluate the usability of the presented link in conjunction with error correction algorithms not applied here, but used in real-world applications, an equivalent bit error rate (BER) was calculated from the recorded EVM values. This conversion from EVM to BER is only valid under the assumption that only additive white Gaussian noise (AWGN) is added to the received signal [376]. In reference to [377], where a hard decision-based forward error correction for 100 Gbps transport networks was proposed, the channel input BER should stay below $4.5 \cdot 10^{-3}$, which can be corrected to a nearly optimal output error rate of less than 10^{-15} with 7 % overhead. In the following figures respective to the different modulation schemes, dotted demarcation lines display the channel input BER equivalent to the EVM.

Fig. 9.44 shows the progression of the EVM with increasing data-rate for QPSK modulation, alongside screen-shots of the constellation diagrams taken from the oscilloscope. A maximum of 55 Gbps at an EVM of 29.5 % were measured, while staying below the equivalent 10^{-3} bit error rate.

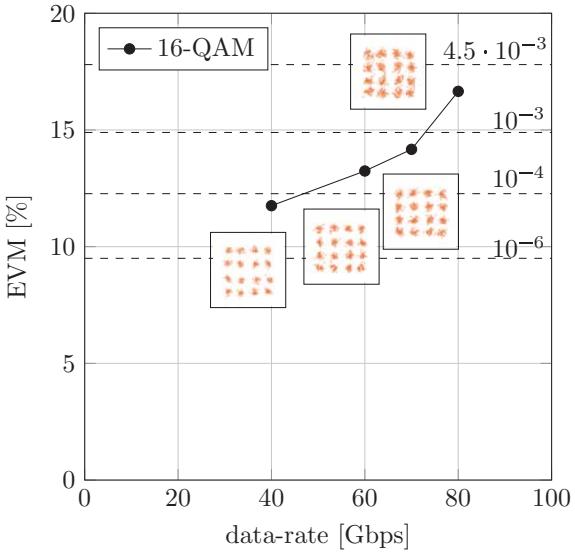


Figure 9.45
Measured EVM for different data-rates using 16-QAM with a 220 GHz carrier frequency.

The absolute maximum data-rate with this link was achieved using 16-QAM, as shown in Fig. 9.45. The maximum data-rate was 80 Gbps at an EVM of 16.6 %.

Fig. 9.46 shows the results for 32-QAM. With 50 Gbps at an EVM of 11.2 %, the equivalent BER is still below the previously discussed practical cut-off of $4.5 \cdot 10^{-3}$.

9.7 Conclusion

The main conclusions drawn during this project are summarized as below.

- The major challenge in transmitter design lies in the combination of an advanced level of power-combining, the necessity of Class-A bias for high linearity and high current densities in the HBTs, which are mandatory to generate power gain near their frequency cut-off.

- In terms of package design, the baseband bandwidth limitation caused by the wirebond interconnects could be extended to tens of gigaghertz if ribbon bonds could be used instead of wedge-wedge wirebonds. For this

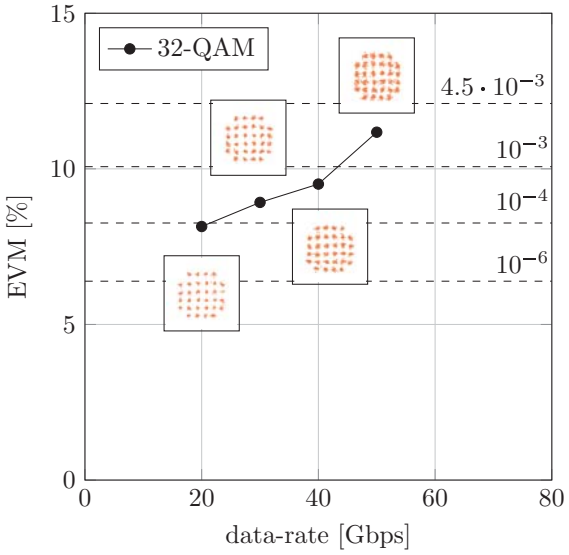


Figure 9.46
Measured EVM for different data-rates using 32-QAM with a 220 GHz carrier frequency.

purpose, the pad size on the Tx/Rx chip should be slightly larger than the current pad size.

- A high performance in-antenna power combining is achieved on the basis of the following factors. First, an ideal impedance matching between the antenna and the power amplifiers. Second, an optimum input impedance of the antenna combined with a maximum output power from the power amplifiers. Third, ensuring a minimum loss while connecting the antenna and the power amplifiers.
- The in-antenna power combining concept provides the highest power combining efficiency, in comparison to the conventional power combiners such as couplers and T-junctions [378].

Acknowledgement

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