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Real100G — Ultrabroadband Wireless Communication at High mm-Wave Frequencies

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7.1 Introduction

Within the SPP 1655 the projects Real100G.RF and Real100G.com cooperated in the research on a 100 Gbps wireless system. The two projects developed a common overall system specification and architecture but investigated different parts of the same wireless system, namely the RF frontend and antennas (Real100G.RF), as well as baseband processing and synchronization (Real100G.com).

The present chapter serves as an introduction to the two projects and focuses on the Real100G overall system specification and architecture. A detailed description of the Real100G.com project and the Real100G.RF project will be given in subsequent chapters.

7.2 Applications and Basic System Architectures for 100Gbps Wireless Communications

Wireless communication links with ultra-high data rates can be used for various short-range to medium-range wireless applications. Among these applications are backhaul/fronthaul links for 5G access points [284], wireless links as a replacement for short-range fiber links on campuses [284] or inside data centers [285], kiosk downloading [286] as well as ultrabroadband wireless chip-to-chip links inside electronic devices (e.g. PCs, Servers) [287]. Additionally, a high-speed data transmission link between a data kiosk and a mobile electronic device could be established as shown in Fig. 7.1 [288], thus enabling high-speed transfer of bandwidth-intensive and delay-sensitive applications such as streaming 4K videos, gaming and voice over IP.

The ambitious goal of 100 Gbps wireless communications can be achieved with quite different wireless system architectures. One possible approach is to use frequency bands in the microwave or lower mm-Wave (e.g. 60 GHz) frequency range with high-order modulation schemes and spatial multiplexing (cf. the projects LP100, maximumMIMO, M4). Spatial multiplexing with

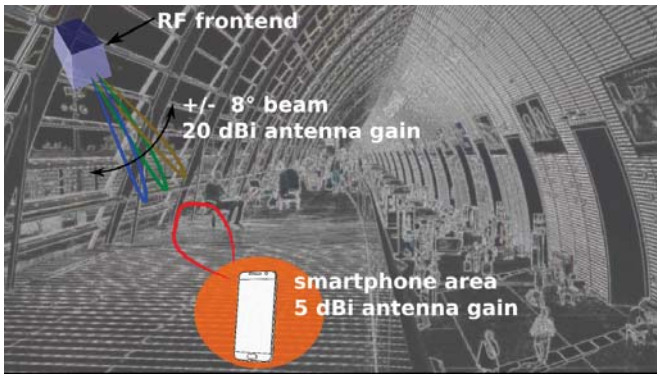

Figure 7.1
A high-speed data transmission link between a data kiosk and a mobile electronic device. From [288] © 2017 IEEE

more or less massive MIMO is needed because the available spectrum in these frequency bands will otherwise not be sufficient for 100 Gbps link capacity.

As an alternative one can use ultra-high carrier frequencies in the high mm-Wave or even sub-mm-Wave ("THz") range in conjunction with ultra-high RF bandwidth well beyond 10 GHz. This is the system approach used in Real100G. In this case 100 Gbps link capacity can be acheived with comparably low spectral efficiency of only a few bits/sHz. Hence an ultra-high carrier frequency and RF bandwidth allow to use low-order modulation schemes and MIMO can be omitted. It should be noted that since antenna size at high mm-Wave frequencies is in the mm-range, too, MIMO systems can be quite compact so that MIMO could still be an option. These advantages, however, are contrasted by the very challenging specifications for the RF frontend and baseband hardware as will be discussed below.

7.3 Definition of Target System Parameters of the Real100G System

7.3.1 Carrier Frequency

For the Real100G wireless system a carrier frequency of 245 GHz was selected. This choice was made for several reasons. Firstly the spectrum above 150 GHz is largely unused besides some radiometric astronomic and satellite-based earth observation applications. Hence large contiguous frequency bands with bandwidths of several 10's of GHz are available and could be used for fu-

ture wireless communication applications [289]. Secondly the ongoing progress in silicon semiconductor technology provides silicon-based transistors (CMOS and Silicon Germanium heterobipolar transistors) which are fast enough to implement RF transmitters and receivers at carrier frequencies above 200 GHz with reasonable performance [290, 291, 292, 293, 294]. Thirdly, the frequency band between 190 and 320 GHz represents a so called "atmospheric window" with only moderate attenuation of radio waves. For clear atmospheric conditions attenuation is lower than 4dB/km, and with fog or under rainy conditions (up to 50 mm/h) attenuation is still better than 20dB/km in the whole frequency band [295].

Regulatory bodies like ITU-R are working on a regulatory framework in this frequency range to define operational requirements for wireless communication links to avoid interference with astronomic and earth observation applications [296]. In addition, recently a new wireless standard operating in the frequency range from 252 GHz to 325 GHz, the IEEE 802.15.3d-2017, has been published [297]. The standard targets data rates up to 100 Gbps. A survey on the worldwide standardization and regulatory activities wrt. wireless communication at frequencies beyond 200 GHz can be found in [289] and shows the relevance of ultrabroadband wireless communications in this frequency range.

7.3.2 Bandwidth and Spectrum Efficiency

The target RF bandwidth of the system should be as high as possible to allow for 100 Gbps while using moderately-complex modulation schemes. For the Real100G system a target RF bandwidth of 40 to 50 GHz was chosen.

The data rate of a wireless link can be calculated to be $DR = BW_{RF} \times SE \times CR$ where DR denotes the data rate, BW_{RF} the RF bandwidth, SE the spectrum efficiency for a given modulation scheme, and CR the code rate. In Table 7.1 various data rates for different spectrum efficiencies and code rates are calculated for an RF bandwidth between 40 and 50 GHz. The calculated values show that with the assumption of realistic code rates in the range between 0.66 and 0.75, 100 Gbps data rate could be achievable with spectrum efficiencies between 3 to 4 b/sHz.

Table 7.1
Exemplary data rates and modulation schemes in 40 to 50 GHz RF bandwidth

DR [Gbps]	$BW_{RF}[GHz]$	SE [b/sHz]	CR	Modulation
105.6	40	4	0.66	16-QAM, 16-PAM
120	40	4	0.75	16-QAM, 16-PAM
99	50	3	0.66	8-PSK, 8-PAM
112.5	50	3	0.75	8-PSK, 8-PAM

The RF bandwidth of 40 to 50 GHz results in a baseband bandwidth of 20 to 25 GHz as shown in Table 7.2. In the case that IQ modulation is used (16-QAM, 8-PSK) this bandwidth is needed for both the inphase- and quadrature-signals. In the case of amplitude modulation (16-PAM, 8-PAM) only one channel with 20 to 25 GHz is required.

Table 7.2
RF bandwidth (BW_{RF}) and baseband bandwidth for inphase rsp. quadrature signals (BW_I rsp. BW_Q) for diff. modulation schemes

$BW_{RF}[GHz]$	Modulation	$BW_I[GHz]$	$BW_Q[GHz]$
40	16-QAM	20	20
40	16-PAM	20	-
50	8-PSK	25	25
50	8-PAM	25	-

7.3.3 Baseband Signal Processing

The high RF bandwidth results in challenging requirements for the baseband signal processing. As explained in section 7.3.2 each baseband channel in transmitter and receiver needs an analog bandwidth of at least 20 to 25 GHz. This extreme bandwidth results in very challenging requirements wrt. bandwidth and sampling rate of the digital-to-analog converters (DACs) in the transmitter and the analog-to-digital converters (ADCs) in the receiver. Furthermore, the digital baseband processor has to process transmit and receive data at very high data rates in real-time. For a 100 Gbps baseband processor it can be expected that coding, modulation, carrier recovery, synchronization, channel estimation, error correction etc. will easily require a compute power of several 10's of TFLOPS.

In a conventional wireless transceiver all the baseband signal processing is done in the digital domain. Compared to digital processing, analog signal processing can be potentially more hardware- and power-efficient. For example, an analog multiplier can be realized with only six transistors, operate at a signal bandwidth of more than 10 GHz, and consume only a few mW of power [298]. The performance of such an analog multiplier corresponds to 20 GFLOPS. On the other hand analog signal processing has some drawbacks compared to digital signal processing as it suffers from nonlinearity and noise and is less precise. In addition not all signal processing functions are equally simple to implement in the analog domain. Hence for analog or mixed-analog/digital signal processing, "analog-friendly" algorithms and modulation techniques are required.

Parallel Spread Spectrum Sequencing (PSSS) is a modulation scheme for wireless and wireline communication which is attractive for mixed-signal pro-

cessing [299, 300]. In [299] an analog PSSS baseband implemented as a Matlab/Simulink model has been used together with 60 GHz radios in a radio link experiment and compared to an OFDM baseband processor. The experiments showed that PSSS achieved a similar performance as an OFDM baseband. Another advantage of mixed-signal PSSS baseband processing is that it allows to reduce the bandwidth of data converters in transmitter and receiver as will be explained below.

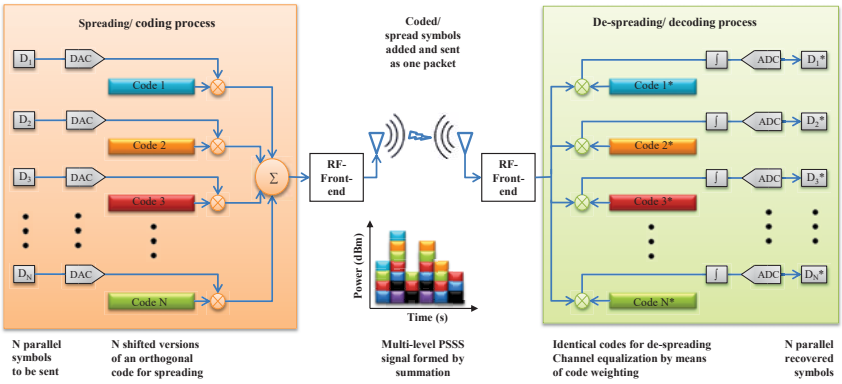

Figure 7.2
Block diagram of the PSSS transmitter (left) and receiver (right) baseband circuit with the proposed mixed-signal architecture. From [301] © 2017 IEEE

In the PSSS transmitter N parallel symbols D_1 to D_N are encoded with N orthogonal codes and summed up to a single quantized PAM-signal. These signals are up-converted to RF, transmitted over the radio channel, and down-converted to baseband. The receiver cross-correlates the PSSS baseband signal with the N PSSS codes and recovers the symbols D_1 to D_N. PSSS is similar to direct-sequence spread spectrum (DSSS) with the difference that PSSS uses DSSS in parallel fashion, by summing several orthogonal DSSS streams in a single wireless link.

The complete spreading-/coding-process in the transmitter and despreading-/decoding-process in the receiver can be implemented efficiently in analog domain using fast analog circuitry, such as analog multipliers, adders, and integrators. In Fig. 7.2, a block diagram of a mixed-signal PSSS transceiver is shown which uses predominantly analog signal processing.

In the mixed-signal PSSS transmitter N parallel symbols D_1 to D_N are first converted to analog signal values by N parallel DACs. Then the analog symbol values are multiplied with N orthogonal codes and summed up to a single quantized PAM-signal, all in the analog domain. These signals are then up-converted to RF, transmitted over the radio channel, and down-converted to baseband. In the receiver the cross-correlation is performed in the analog

domain to recover analog symbols D_1^* to D_N^* which are then converted to the digital domain by means of N parallel ADCs.

Besides the efficient implementation of the analog functions, another important advantage of the mixed-signal implementation of PSSS transceiver is the reduced speed requirements for the data converters. In the mixed-signal PSSS baseband from Figure 7.2 N parallel DACs and ADCs are utilized operating at a sampling frequency equal to symbol rate which is much lower than the bandwidth of the PSSS signal. The implementation of the mixed-signal PSSS transceiver will be described in more detail in the chapter on the project Real100G.com.

7.3.4 Link Budget and Achievable Range

The following link budget calculation shows how to reach the 100 Gbps mark by utilizing moderately-complex modulation schemes. This is enabled by exploiting the huge amount of available spectral bandwidth while limiting the digital signal processing effort, which reduces capital and operating expenses. Based on the spectral efficiency S of the utilized modulation scheme the required symbol rate can be calculated by $f_s = f_b/S$, where f_b denotes the desired data rate. According to Nyquist, the symbol rate theoretically corresponds to the required RF bandwidth. However, this would require an ideal rectangular filtering in frequency domain. Therefore, in practice raised-cosine (RC) pulse shaping filters are used to limit the spectral resources [302]. Depending on the selected roll-off factor $0 \leqslant \alpha \leqslant 1$ of the RC pulse shaping filter the RF bandwidth results to $B_{\mathrm{RF}} = (1+\alpha)f_s$ [303]. Nevertheless, as analog pulse shaping are difficult to design, current communication systems utilize finite impulse response filter in the digital domain [304]. These digital filters require an oversampling of the transmit signal by at least a factor of two to perform a shaping of the input signal [305]. Note that to guarantee a good match between the resulting and the desired filter response the oversampling factor o and the number of filter taps have to be adjusted properly [305]. This oversampling in the digital domain leads to an increase in the sampling rate of the DAC $f_{\mathrm{DAC}} = of_s$, which might be challenging to realize as the symbol rate is already high. Hence, that a pulse shaping filter can be neglected and the sampling rate of the DAC can be set equal to the symbol rate [306]. This corresponds to a roll-off factor of $\alpha = 1$ leading to a RF bandwidth of double the Nyquist bandwidth $B_{\mathrm{RF}} = 2f_s$ [307]. In this case the shape of the output signal is defined by the frequency response of the DAC. As the sampling rate of the DAC might be a limiting factor and due to the large available spectral resources a hardware instead of spectral efficient operation is preferable to reach the 100 Gbps mark. The resulting RF bandwidths and DAC sampling rates for a bit rate of $f_b = 100$ Gbps are listed in Table 7.3 without pulse shaping and in Table 7.3 with pulse shaping considering a RC filter with $o = 2$ and $\alpha = 0.25$.

The calculated values in Table 7.3 show, that to reach the 100 Gbps utiliz-

Table 7.3
RF bandwidth (B_{RF}) and DAC sampling rate for different modulation schemes considering $f_b = 100\,\mathrm{Gbps}$ and no pulse shaping filter.

	BPSK	QPSK	16-QAM	PAM-8	PAM-16 PSSS
S in b/s/Hz	1	2	4	3	4
f_s in GBaud	100	50	25	33.33	25
B_{RF} in GHz	200	100	50	66.67	50
f_{DAC} in GHz	100	50	25	33.33	25

Table 7.4
RF bandwidth (B_{RF}) and DAC sampling rate for different modulation schemes considering $f_b = 100\,\mathrm{Gbps}$ and a digital RC pulse shaping filter with $o = 2$ and $\alpha = 0.25$.

	BPSK	QPSK	16-QAM	PAM-8	PAM-16 PSSS
S in b/s/Hz	1	2	4	3	4
f_s in GBaud	100	50	25	33.33	25
B_{RF} in GHz	125	62.50	31.25	41.67	31.25
f_{DAC} in GHz	200	100	50	66.67	50

ing a modulation schemes with a spectral efficiency of 4 b/s/Hz like 16-QAM or PAM-16 a RF bandwidth of 50 GHz is required. These large RF bandwidths are realistic as shown in [308, 309, 310, 292]. Furthermore, the sampling rate of the DAC is only 25 Gbps. It is important to mention that for the 16-QAM two DACs are required to convert the inphase and quadrature component of the signal, whereas for a PAM-16 signal only one DAC is required. By introducing a RC pulse shaping filter the RF bandwidth can be limited to the cost of a higher DAC sampling rate as shown in Table 7.4.

In the next step the maximum achievable range can be determined for a communications link enabling 100 Gbps. At the transmitter side the radiated power and the antenna gain are the dominant factors determining the achievable range. Especially, power amplifiers at the higher RF region are suffering from technology related low energy efficiencies and output powers [311, 312]. The operation point of the transmit amplifier therefore has to be selected as high as possible regarding the selected modulation scheme. Note that especially for amplitude modulated signals, an operation in the linear region of the amplifier must be ensured, to avoid non-linear distortions of the signal. To assure the linear operation of the amplifier the operation point is selected in the backoff of the 1 dB-compression point of the amplifier decreasing the average transmit power. As a first reference value the average transmit power can be defined as $P_{\mathrm{Tx}}^{\mathrm{dBm}} = P_{\mathrm{Tx,1\,dB}}^{\mathrm{out}} - \mathrm{PAPR}$, where $P_{\mathrm{Tx,1\,dB}}^{\mathrm{out}}$ denotes the 1 dB-output compression point of the transmitter in dBm and the back-off is set equal to the peak-to-average-power-ratio (PAPR) in dB of the selected modulation scheme. For a directional communications link the linear receive power results

to

$$P_{\mathrm{Rx}} = \left(\frac{\lambda}{4\pi r}\right)^2 G_{\mathrm{Rx}} G_{\mathrm{Tx}} P_{\mathrm{Tx}} \tag{7.1}$$

with the free space path loss $\mathrm{FSPL} = (\lambda/(4\pi r))^2$ as well as the transmit and receive antenna gain G_{Tx} and G_{Rx}. Thereby, λ denotes the wavelength of the transmit signal and r the range between the transmitter and receiver. Atmospheric losses can be neglected at this point, as the range is considered to be several meters. To determine the maximum achievable range, the minimum receive power has to be defined. Therefore the required energy per bit to noise power spectral density ratio (E_b/N_0) to guarantee a sufficiently low bit error rate (BER) of 10^{-3} without any error correction is calculated for every modulation scheme [313]. The BER can be reduced to a negligible low value by utilizing forward error correction techniques as presented in [314]. The carrier-to-noise ratio at the receiver is given by $C/N = P_{\mathrm{Rx}}/(kTB_{\mathrm{RF}}F)$, where k denotes the Boltzmann's constant, T is the absolute temperature in Kelvin, and F the noise factor of the receiver [315]. Furthermore, it holds [313]

$$C/N = \frac{f_b}{B_{\mathrm{RF}}}(E_b/N_0) \tag{7.2}$$

for the relation between C/N and E_b/N_0. Using the presented formulas the maximum range results to

$$r_{\max} = \frac{\lambda}{4\pi}\sqrt{\frac{P_{\mathrm{Tx}} G_{\mathrm{Tx}} G_{\mathrm{Rx}}}{f_b (E_b/N_0)_{\min} kTF}} \tag{7.3}$$

for a minimum required $(E_b/N_0)_{\min}$ of the selected modulation scheme. It can be seen that for a larger transmit power, antenna gains, and wavelengths the maximum range can be increased, while for a larger $(E_b/N_0)_{\min}$ and receiver noise the maximum achievable range is decreased. Moreover, the maximum range is theoretically independent of the pulse shaping filter.

Table 7.5 presents the resulting maximum range for different modulation schemes assuming a fixed bit rate of $f_b = 100\,\mathrm{Gbps}$. The higher maximum range for lower order modulation schemes comes at the price of a larger required RF bandwidth. For the 16-QAM a maximum range above 1 m is achieved, considering a moderate 1 dB-output compression point of the transmit amplifier of $P^{\mathrm{out}}_{\mathrm{Tx,1\,dB}} = 0\,\mathrm{dBm}$ and a transmit and receive antenna gain of 25 dBi.

One opportunity to enlarge the maximum range is to increase the antenna gains of the transmitter and receiver. Fig. 7.3 shows the increase in maximum range versus the transmitter and receiver antenna gain for the PAM-16 PSSS modulation. However, by increasing the antenna gain, the half power beam width (HPBW) of the antennas is reduced, requiring a more precise alignment between transmitter and receiver. For Fig. 7.3 the HPBW is approximated assuming a round aperture utilizing the formula $\mathrm{HPBW} \approx \sqrt{35000/G}$ [316,

Table 7.5
Maximum range for different modulation schemes considering $f_b = 100\,\text{Gbps}$, $P^{\text{out}}_{\text{Tx,1 dB}} = 0\,\text{dBm}$, $G_{\text{Tx}} = 25\,\text{dBi}$, $G_{\text{Rx}} = 25\,\text{dBi}$, and $F = 12\,\text{dB}$. For the PSSS a spreading gain of 11.76 dB and an implementation loss of 2.73 dB is assumed.

	BPSK	QPSK	16-QAM	PAM-8	PAM-16 PSSS
S in b/s/Hz	1	2	4	3	4
f_s in GBaud	100	50	25	33.33	25
B_{RF} in GHz	125	62.50	31.25	41.67	31.25
PAPR (linear)	1	1	1.80	2.33	21.18
PAPR in dB	0	0	2.55	3.67	13.26
P_{Tx} in dBm	0	0	-2.55	-3.67	-13.26
$(E_b/N_0)_{\text{min}}$ in dB	6.77	6.77	10.49	14.75	19.35
r_{max} in m	5.4	5.4	2.62	1.41	0.78

317]. The results show that for an antenna gain at the transmitter and receiver of 36 dBi a maximum range of nearly 10 m can be reached. In this case the HPBW is reduced to only 3°, which clearly shows the high demands on the alignment.

7.4 Challenges and Proposed Solutions

7.4.1 PSSS System Architecture

The PSSS transmitter baseband uses orthogonal coding sequences to encode several data symbols in parallel. The encoded chips are added up chip-by-chip to generate the PSSS baseband signal. On the receiver side, local copies of the decoding sequences are generated which are correlated with the incoming PSSS waveform to recover the transmitted symbols. Apart from the basic building blocks mentioned above, several additional functional blocks are required for reliable functioning of the communication link. The proposed general system level architecture of a PSSS based communication system using a Terahertz radio frequency frontend is shown in Fig. 7.4.

The input data stream is packed into frames which contain delimiters, to mark the start and the end of the frame, that enclose the data bits. The data primarily consists of payload data but it may contain some training data for channel equalization. The framed data is digitally modulated into symbols for which the pulse amplitude modulation (PAM) is preferred because it makes the carrier recovery simpler using a Costas loop as explained later. The symbols are arranged in sets of N symbols to encode them in parallel using N shifted versions of a coding sequence. The chip-wise summation of

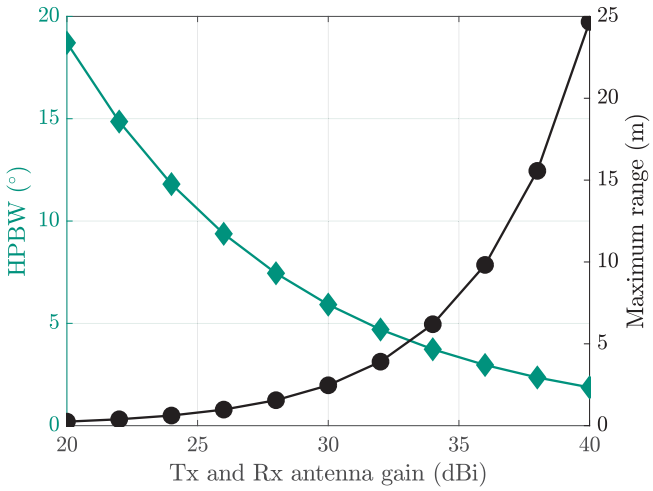

Figure 7.3
Maximum range and HPBW versus the transmitter and receiver antenna gain of the PAM-16 PSSS modulation.

the encoded chips from each data symbol generates the PSSS chips of the PSSS sequence.

On the receiver end, the received PSSS waveform is down-converted and fed to a Costas loop to recover the carrier signal from the received waveform. The Costas loop is preceded by a limiting amplifier to convert the PSSS stream to a BPSK stream with a mean or DC value of 0V. The recovered carrier signal is used as the system clock for the receiver baseband.

During the training phase, the received training data is compared with the ideal computed response. The channel equalization is then performed using matrix operations on the received data. The output of the matrix operations generates the weighting factors for the decoding sequence chips i.e. instead of an additional filter for the channel equalization the decoding sequence chips are weighted to perform the channel equalization. Thus, the data decoding and channel equalization are performed simultaneously.

The output of the integrate and dump correlator (IDC) in Fig. 7.4 is sampled periodically with a period equal to the symbol duration. An analog to digital converter (ADC) is used to convert the sampled value to a digital representation to recover the original symbol. N parallel copies of the IDC and ADC circuits are used to recover N parallelly transmitted symbols simultaneously.

For the case of 100 Gbps, performing some of the baseband signal processing using analog circuits may have advantages in terms of power dissipation, complexity, and cost as compared to the digital baseband circuits. As an example, assuming a baseband bandwidth of 12.5 GHz, a spectral efficiency of 8 bits/s/Hz is required to achieve the target data rate of 100 Gbps. With a

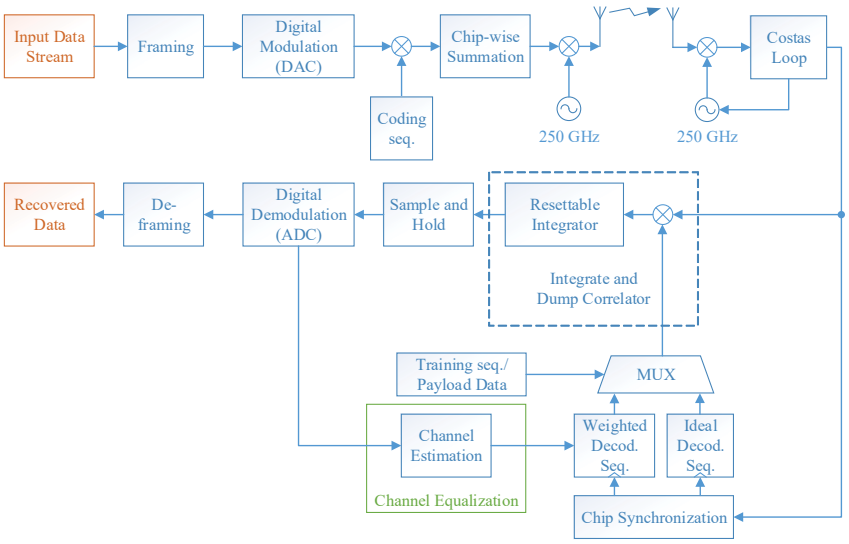

Figure 7.4
Proposed system architecture for PSSS based communication link using a Terahertz radio frequency frontend. From [318] © 2015 IEEE

digital baseband receiver, an ADC with a minimum resolution of 8-bits will be required with an input bandwidth of at least 12.5 GHz and a minimum sampling rate of 25 GS/sec. If a spreading scheme like PSSS is used with a mixed-signal baseband implementation the requirements for the input bandwidth and the sampling rate of the ADC are reduced by a factor equal to the spreading gain of the system which corresponds to the length of the coding sequences used. Using the code length of 15 as an example (as is the case for the mixed-signal PSSS baseband explained in the next chapter), the sampling rate of the ADC will be reduced by a factor of 15 to 1.666 GSa/s. This considerably reduces the design complexity of the ADC.

7.4.1.1 System Parameters for Mixed-Signal PSSS Baseband

The important system parameters for a mixed-signal PSSS baseband are the following: type of coding sequences i.e. m-sequences, Barker codes, etc., polarity of the coding and decoding sequences i.e. (unipolar vs. bipolar codes), length of the coding sequences, system bandwidth, chip rate, bit loading, type of digital modulation used, input and output dynamic range of the correlator circuit, length of the guard interval, and type of data in the guard interval. A detailed discussion about the system parameters of a mixed-signal PSSS baseband for 100 Gbps wireless communication is available in [318], [319].

For a mixed-signal implementation, the code-length directly influences

many of the circuit design parameters. According to the discussion in [318], [319] m-sequences of length 15 are a good choice for the coding sequences because larger coding sequence require greater number of copies of the hardware slices. A bipolar variant of the m-sequences is used for the coding whereas a unipolar variant is used for the decoding. This generates the smallest set for the PSSS amplitude set which eases the requirements for the correlator input and output dynamic range. The chip rate is chosen to be 30 Gcps resulting in a baseband bandwidth requirement of roughly 25 GHz. Using double sideband modulation requires an RF bandwidth of 50 GHz. Such a large contiguous chunk of bandwidth requires the carrier frequency to be in the terahertz range e.g. for the current implementation an RF frontend with a carrier frequency of 250 GHz is considered. 15 data symbols are transmitted in parallel. If a sliced hardware concept is used where each slice corresponds to one symbol of transmitted and received symbol, then a total of 15 slices are required for the over-all system as explained in the next sub-sections of the chapter.

7.4.2 RF Frontend

Realizing an RF frontend at millimeter-wave frequencies above 200 GHz involves several challenges, which can be broadly divided under the following three categories. First, developing an antenna with a high bandwidth-efficiency product. Usually, it is much more difficult to realize such an antenna on chip than off chip. An on-chip antenna is fabricated on a high dielectric constant substrate, which leads to an enhanced surface wave propagation and thus a lower radiation efficiency. This problem could be solved by using processes such as through silicon via and localized backside etching; however they enhance the manufacturing cost and may lead to mechanical instabilities. Second, a high performance chip-to-antenna interconnect. If an off-chip antenna is used, the chip-to-antenna interconnect is realized using wirebond or flip chip technology. Large parasitic effects are associated with these interconnects at such high millimeter-wave frequencies. Although the parasitic effects can be mitigated by designing a symmetric or asymmetric compensation network (A symmetric compensation network is realized both on- and off-chip, where as an asymmetric compensation network is realized only off-chip), this requires extra chip/substrate area and hence extra manufacturing cost. Moreover, the bandwidth of a compensation network is limited ($< 10\%$) and even small manufacturing tolerances in realizing these millimeter-wave interconnects could severly degrade their performance (i.e. reflection and transmission coefficient). In contrast, if an on-chip antenna is used, the chip-to-antenna interconnect is simply realized using planar transmission lines, which have no bandwidth limitation in the desired frequency range. Additionally, it leads to a more compact chip-antenna assembly. Third, a suitable package for the chip-antenna assembly is required. The package acts as an electrical, thermal and mechanical interface between the chip-antenna assembly and the outside world. It is responsible for the following aspects - routing the control signals

to the chip, dissipating the heat generated by the chip, protecting the chip-antenna assembly against environmental hazards and mechanical stress and minimizing electromagnetic interference between various components of the chip-antenna assembly. Based on the abovementioned rationale, an on-chip antenna and hence a system-on-chip (SoC) package architecture is preferred in this work. The radiation efficiency of the on-chip antenna is enhanced by using a novel SoC package concept, where a SiGe chip including the on-chip antenna is mounted on a Silicon lens and the backside radiation of the antenna is used to its best advantage. A detailed description of the package concept is given in Chapter 9.

7.4.3 Receiver Synchronization

A carrier recovery system is required on the receiver end to down-convert the digitally modulated signals coherently. The type of carrier recovery system depends on the type of modulation used and on the RF frequency. For moderate signal bandwidths, a conventional synchronization in the digital domain would suffice, while at higher bandwidth analog synchronization would be more power efficient [320].

In order to make full use of the available RF bandwidth at THz carrier frequencies, Costas loops are a propitious choice due to their operation on the baseband signals. The requirements on the PSSS modulation format would be of the quadrature as in phase-shift keying. The operation at mmW frequencies comes with challenges in the choice of VCO parameters which influences the performance of the synchronizing system.

Since the Costas loop is a linear chain of three cascaded circuit blocks, the small-signal bandwidth of the each individual circuit is chosen to be greater than $1.5 \times R_b$, where R_b is the data rate. As mentioned in Tab. 7.2, the required baseband bandwidth for the complete system is around 25 GHz. Thus for an optimum operation on the baseband signals, the small-signal bandwidth for the individual circuits is chosen to be from DC up to greater than 40 GHz in order to avoiding the low-pass filtering of fast signal transitions [321]. The loop parameters of the Costas loop like the locking time or the loop bandwidth depends on the preamble length. In this work, a preamble signal is a BPSK signal with 33 Gcps chip rate and 10 nsec long. Thus the loop parameters are chosen such that the loop can lock with in this time frame. Once the lock is acquired, the loop should stay in lock position.

7.5 Real100G Overall System Architecture

To synchronize the various research tasks in the project Real100G, a common system architecture has been agreed upon. Based on the discussion of the

individual system level components of the Real100G project, the following architecture of the transmitter and receiver has been defined.

7.5.1 Real100G Transmitter Architecture

The Real100G transmitter architecture is shown in 7.5. The transmitter consists of a TX baseband board and a TX RF frontend soft-board. The transmitter is fundamentally operated through a tunable local oscillator generated by a Gilbert-cell based ×16 multiplier chain. This multiplier chain is fed externally by a 15 GHz signal. Afterwards, the generated 240 GHz signal is amplified by a 3-stage cascade power amplifier [322]. The quadrature signal is provided by a broadband 90° coupler [323]. Two mixers, for in-phase and quadrature (i.e. I and Q) channels respectively, up-convert the baseband signal to the 240 GHz band. The up-converted signals are fed to a 4-stage power amplifier and combined afterward in a Gysel power combiner. The combined IQ signal is then routed to the antenna, split again, amplified and deliver to the antenna. The antenna radiates through the substrate into a high-resistivity hemispherical 12 mm diameter silicon lens. The chip-on-lens assembly is mounted and wire-bonded on the backside of a printed circuit board with a recess to accommodate the chip.

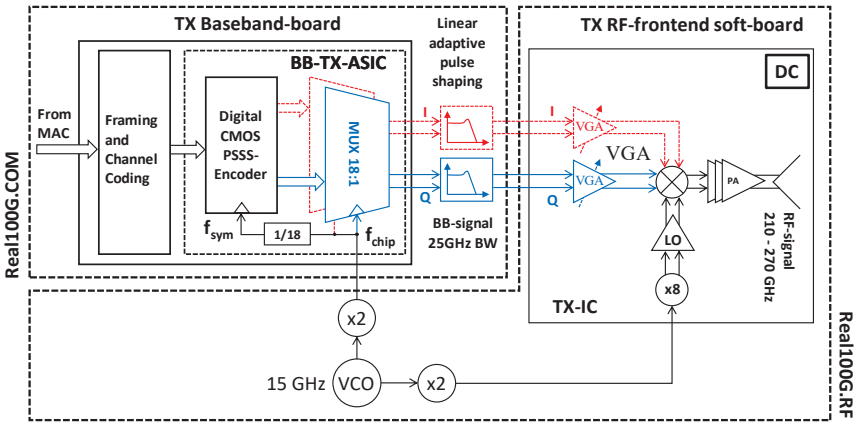

Figure 7.5
Block diagram of the Real100G transmitter circuit showing the interface between the projects Real100G.com and Real100G.RF.

A simple mixed-signal transmitter baseband architecture is described in fig. 7.6. N parallel XOR (exclusive OR) gates are used to encode the N parallel data symbols with individual orthogonal coding sequences simultaneously. Note that each data symbol consists of M-bits where M corresponds to the modulation complexity. The coding sequence generators are clocked with a

frequency of f_{chip}. The *ith* encoded chips of all N data symbols are added up to make the *ith* PSSS chip. The output of the adder circuits are the PSSS chips in digital form. The digital PSSS chips are applied as inputs to digital to analog converters to convert them from digital to analog signals. The resolution of the DACs depends on the modulation complexity M, the number of parallely transmitted symbols N, and the polarity of the coding and decoding sequences. The outputs of the DACs are in the form of current signals. The current mode outputs from the DACs are applied at the inputs of a broadband analog multiplexer (mux). Each of the first N inputs of the mux represents one chip of the PSSS sequence. The last 3 inputs are the cyclic extension chips which are copies of the first 3 PSSS chips. The multiplexer outputs the successive PSSS chips with a clock rate of f_{chip}. The broadband analog output of the multiplexer corresponds to the PSSS signal for the input data symbol set $D_1 - D_N$ plus the 3 cyclic extension chips.

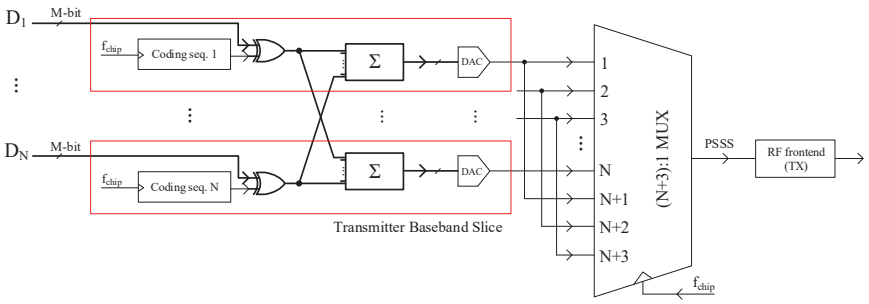

Figure 7.6
Block diagram of the mixed-signal PSSS transmitter baseband circuit. From [319] © 2017 IEEE

7.5.2 Real100G Receiver Architecture

The Real100G receiver architecture is shown in fig. 7.7. The local oscillator signal generation path, including the quadrature signal, and the packaging scheme is analogous to the one described in the transmitter section above. The RF signal is converted to the baseband by a down-conversion in-phase and quadrature mixer. This baseband signal is afterwards amplified by a variable gain amplifier (VGA) before it is delivered to the printed circuit board.

The IQ carrier recovery system follows the receiver front-end as shown in fig. 7.7. In this IQ system, the QPSK Costas loop is used to extract the frequency and the phase information of the received carrier which utilizes the I and Q baseband signals after the down-conversion [324]. The baseband signal inside the Costas loop travels through a power splitter, a limiter and an error dector in order to generate an error signal which reflects the amount

of frequency and phase error. This error signal is used to control a VCO at 10 GHz. The choice of the operating frequency of the VCO is done based on the required LO frequency for the received front-end and the clock frequency for the following baseband system. The VCO output at 10 GHz is up-scaled by a factor of 3 to get 30 GHz signal. The 30 GHz signal is divided and used to drive the LO port of the receiver in one direction and clocking port of the the baseband system in the other direction.

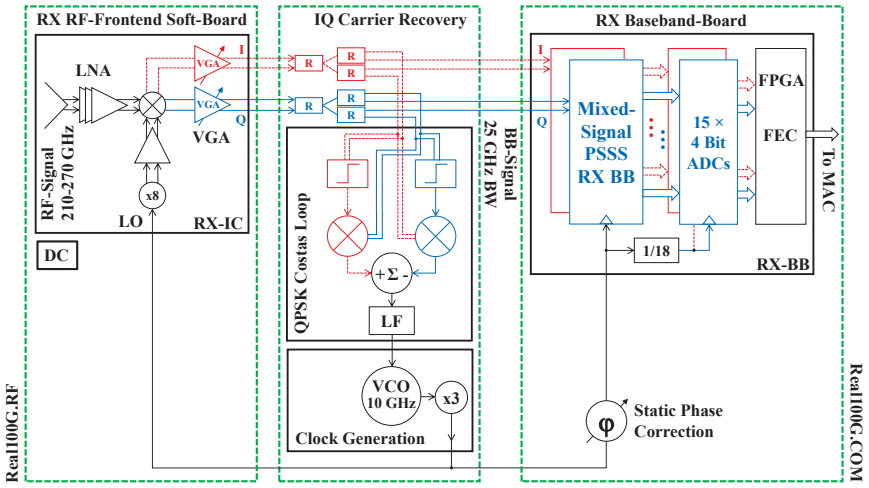

Figure 7.7
Block diagram of the Real100G receiver circuit showing the interface between the projects Real100G.com and Real100G.RF.

The architecture of a mixed-signal receiver baseband is shown in fig. 7.8. The receiver baseband has a sliced architecture where each slice corresponds to the receiver baseband unit circuit that is required to recover one data symbol from the incoming PSSS sequence. The receiver baseband decodes the incoming PSSS stream by multiplying it with a local copy of the original coding sequences or some modified version thereof. A carrier recovery circuit is used to recover the 30 GHz synchronous to the PSSS signal. The recovered clock signal with a frequency of f_{chip} is used to clock the mixed-signal pattern generator circuit which uses an analog mux to select and route the inputs (one-by-one) to the output. The mux has N+3 number of inputs in the form of scalable differential current signals. The first N inputs correspond to the chips of the decoding sequences whereas the last 3 can be filled with zeros since this is the time during which the integrator is reset. The chip-wise product of the PSSS chips with the decoding sequence chips is integrated until all N chips have been multiplied and integrated. The output of the correlator is sampled at the end of the correlation period $T_S{=}N \times T_{chip}$ after which follows

a guard interval of duration $3 \times T_{chip}$ during which the integrator is reset and the output value of the correlator output is sampled using a sample and hold circuit S/H. The reset signal of the integrator and the sampling clock of the S/H circuit is generated by using a one-hot pulse (i.e. 1 followed by all zeros) generation circuit. 3x one-hot pulses are OR-ed to generate the reset signal of the integrator as well as the sampling clock of the S/H circuit. The sampled output of the correlator is converted to a digital form using analog to digital converters (ADCs) which only need to have a sampling rate of $f_S = f_{chip}/(N+3)$. The output resolution of the ADCs is at least equal to the bit loading i.e M-bits. To recover the N transmitted symbols simultaneously at the receiver, N copies of the receiver baseband slice are needed.

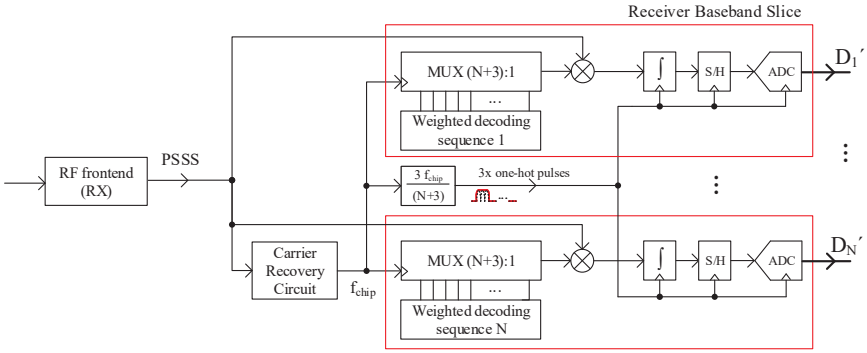

Figure 7.8
Block diagram of the mixed-signal PSSS receiver baseband circuit. From [319]