4

DAAB — On-Chip Integrated Distributed Amplifier and Antenna Systems in Locally-Backside-Etched SiGe BiCMOS for Receivers with Ultra-Large Bandwidth

Paolo Valerio Testa, Corrado Carta, Frank Ellinger

Chair for Circuit Design and Network Theory,
Technische Universität Dresden

Bernhard Klein, Ronny Hahnel, Dirk Plettemeier

Chair for Radio Frequency and Photonics Engineering,
Technische Universität Dresden

CONTENTS

DOI: 10.26127/BTUOpen-5910

4.1 Introduction to the Chapter

This chapter presents the results of the project "On-chip integrated Distributed Amplifier and Antenna systems in locally-backside-etched SiGe BiCMOS for receivers with ultra-large Bandwidth" – DAAB, and of its second phase "On-chip integrated Distributed Amplifier and Antenna systems in SiGe BiCMOS ultra-large Bandwidth Transmitters" – DAAB-Tx . More specifically, these projects investigate novel distributed amplifier and antenna concepts to massively improve the relative bandwidth of wireless receivers and transmitters operating at frequencies above 100 GHz and up to 250 GHz. The projects aim at achieving relative bandwidths up to 50%, corresponding to an improvement of at least a factor of 2 compared to the state-of-art, to pave the way to communications with data rates beyond 100 Gbps. Furthermore, the integration of antennas and active electronics into the same semiconductor die aims at minimizing the interconnection parasitics. The fastest commercially available BiCMOS technology, with a maximum frequency of oscillation (f_{max}) of 450 GHz has been employed for experimental validation. The Chair for Circuit Design and Network Theory (CCN) and the Chair for Radio Frequency and Photonics Engineering (CRF), both from the Technische Universität Dresden, carried out the project. Profound interdisciplinary competencies have been applied, involving – among the others – knowledge in the high-frequency domain and integrated circuits technology.

4.2 Broadband Distributed Amplifiers

In the DAAB and DAAB-Tx projects, integrated circuits for UWB operation in the millimeter-wave band have been demonstrated for integration with on-chip antennas in transceivers. A commercially available 130 nm SiGe BiCMOS process has been used to fabricate the circuit prototypes and to validate the developed designs. State-of-the-art performances have been reached in the field of distributed amplifiers. The major results can be summarized as follow [Testa1-Testa21]:

- A novel gain-cell has been conceived to boost the highest frequency of operation of distributed amplifiers via the compensation of the synthetic-line losses. Experimental demonstration validated the technique with a Traveling-Wave Amplifier (TWA) able to produce 10 dB of gain over a 170 GHz-wide frequency band.
- Two Cascaded Single-Stage Distributed Amplifiers (CSSDAs) have been optimized for low power and high speed. The first requires less than 20 mW to provide 10 dB of gain over a 130 GHz-wide frequency band, while the

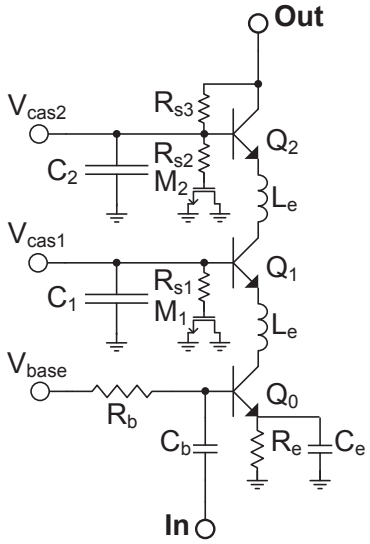


Figure 4.1
Circuit schematic of the G_m-boosted triple-cascode gain-cell developed in the DAAB(-Tx) projects. From [140] © 2015 IEEE

second has been proven functional up to 250 GHz, which is a record result for solid-state SiGe distributed amplifiers.

- The first traveling-wave power combiner and divider capable of operation from the MHz range up to 220 GHz have been demonstrated. The circuits improved the state of the art in terms of maximum frequency of operation and bandwidth by a factor 5.

4.2.1 Traveling-Wave Amplifiers

Within the frame of DAAB and DAAB-Tx projects, a novel gain-cell has been demonstrated to increase the Gain-Bandwidth-Product (GBP) and the maximum frequency of operation of TWAs with respect to conventional approaches based on cascode cells [140]. The conceived cell produces a peak in its equivalent transconductance G_m, which is employed to compensate the synthetic-line losses at high frequency. Fig. 4.1 shows the schematic of the designed cell. The circuit is based on a cascode stage (Q_0 – Q_1), followed by an additional common-base amplifier (Q_2). The resulting gain element will be referred to as *triple cascode* within this manuscript. The three stacked transistors, together with inductive elements, produce a sharp peak in the transconductance of the cell. The inductive elements are realized with the collector-emitter connections between Q_0 – Q_1 and Q_1 – Q_2. The peaking of

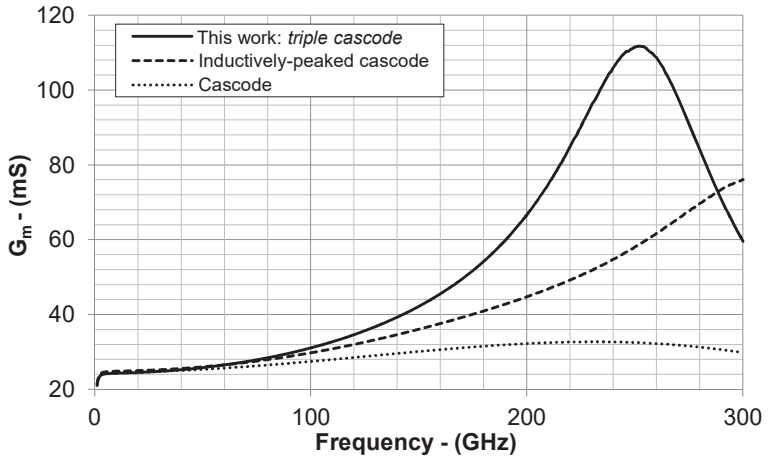


Figure 4.2
Simulated transconductance of the presented triple-cascode cell (Fig. 4.1) against those of conventional and inductively-peaked cascode. The three circuits have same emitter degeneration R_e – C_e, input series capacitor C_b and L_e inductor. I_{CC} and V_{CE} per transistor are also the same. From [140] © 2015 IEEE

cell transconductance is shown in Fig. 4.2, where it is also compared for same technology and bias conditions ($I_{CC} = 6\,\text{mA}$, $V_{CE} = 1.2\,\text{V}$) against those of conventional and inductively-peaked cascode. As illustrated, the G_m of the presented cell has the steepest increment for increasing frequency. Since the TWA gain is proportional to ${G_m}^2$ (eq. (4.1)), its rapid increase has been exploited to compensate the synthetic input losses (eq. (4.2)) improving the bandwidth of the amplifier [141, 142, 143]. TWA power gain is approximated by [143]:

$$G_{TWA} = \left(\frac{nG_mZ_S}{2}\right)^2\left(1-\frac{n\alpha_{in}}{2}\right)^2 \tag{4.1}$$

where n is the number of gain cells, while the expression of the synthetic input-line losses is [143]:

$$\alpha_{in} = 2\pi^2 f^2 C_{in}^2 R_{in} Z_{Sin} \tag{4.2}$$

where f is the frequency. Since the synthetic input-line losses increase with the square of the frequency, α_{in} easily reduces the $-3\,\text{dB}$ upper-corner frequency of TWAs to values smaller than the LC cutoff [141, 142, 143].

Fig. 4.3 shows the schematic of the amplifier, while its micro-photograph is illustrated in Fig. 4.4. The TWA is composed of five gain elements, placed at a distance ℓ of $130\,\mu\text{m}$, which resulted in a total chip area of $0.38\,\text{mm}^2$. The main supply voltage V_{CC} is provided through the output of the amplifier with a bias tee.

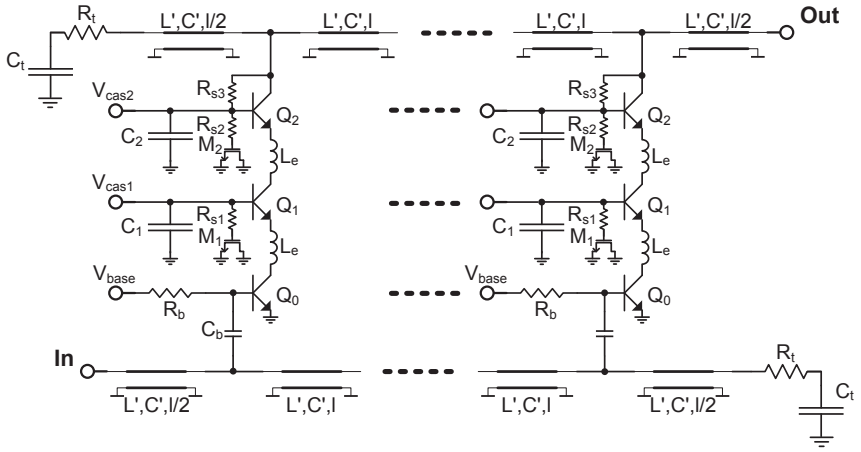


Figure 4.3
Circuit schematic of the designed TWA. From [140] © 2015 IEEE

The presented novel architecture has been tested with a circuit prototype fabricated in the *SG13G2* technology. The nominal f_{max} of the process is 450 GHz, but it reduced to 370 GHz in the tolerance corner of the actual fabrication run. The characterization of the amplifier was performed on-chip with wafer probes when the circuit was biased at $I_{CC} = 30\,mA$ and $V_{CC} = 3.6\,V$. The pad parasitics have been taken into account during the design through electromagnetic simulations. For this reason, they have not been de-embedded from the measurement results. A Vector Network Analyzer (VNA) has been used to measure the S-Parameters. Three different measurement setups characterized the ultra-wide spectrum of amplification: from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. All except the first required the use of extender mixer modules, while the absence of experimental results between 67 GHz and 90 GHz is due to the lack of measurement instrumentation for this band at the time of characterization.

Fig. 4.5 shows the measured S-Parameters and the simulated magnitude of S_{21}. The amplifier provides an average gain of 10 dB with −3 dB corner frequency at 1 GHz and 170 GHz. The resulting GBP is 537 GHz. Fig. 4.5 also shows the gain calculated as in eq. (4.1) with the simulated values of G_m and α_{in}. The absolute value and frequency behavior predict well the measurement results.

Table 4.1 presents a comparison with recently-published single-stage TWAs. At expenses of chip area and power consumption (P_{DC}), the gain can be increased using more gain cells. The following Figure of Merit (FoM)

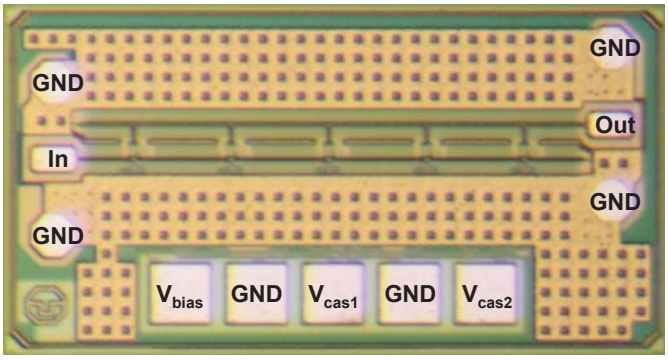


Figure 4.4
Chip micro-photograph of the fabricated TWA. From [140] © 2015 IEEE. The chip dimensions are 0.85 mm×0.45 mm, while the chip area is 0.38 mm^2.

Table 4.1
State of the art of single-stage TWAs. From [140] © 2015 IEEE

FoM	BW [GHz]	Gain [dB]	Technology	GBP [GHz]	Area [mm^2]	P_{DC} [mW]	o1dBCp [dBm]	f_{max} [GHz]	Ref.
N/A	1-180	5	InP HEMT	320	2.1	N/A	N/A	300	[142]
0.51	5-110	11	50 nm InGaAs HEMT	390	1.68	450	7	500	[145]
0.76	dc-95	21	InP DBHT	1065	2.00	700	16	300	[146]
1.10	dc-120	21	InP DBHT	1346	2.00	610	N/A	370	[147]
1.25	dc-52	10	0.13 µm Si CMOS	164	1.56	84	N/A	N/A	[148]
1.47	4-82	7.8	0.12 µm SOI CMOS	201	1.05	130	10	N/A	[149]
1.70	dc-44	3	0.5 µm AlGaAs HEMT	61.5	1	36	0	70	[150]
2.56	5-73	14	90 nm Si CMOS	370	1.72	84	3	200	[151]
3.74	dc-59	8	90 nm Si CMOS	148	0.3	132	12	150	[152]
9.34	15-110	24	0.13 µm SiGe	1500	0.65	247	16	450	[153]
13.8	1-170	10	0.13 µm SiGe	537	0.38	108	7	340	This work

can be used to account for this design trade-off and ease the comparison [144]:

$$FoM = \frac{GBP}{Area \times P_{DC}} \quad [\frac{GHz}{mm^2 \cdot mW}] \tag{4.3}$$

The presented design solution achieves the highest GBP per power consumption and area, as well as the highest reported bandwidth for silicon implementations. The performance improvements presented are enabled by the introduction of a crucial circuit-design innovation: the compensation at high frequencies of the synthetic-line losses with a frequency-dependent increase of the gain-cell transconductance.

4.2.2 Cascaded Single-Stage Distributed Amplifiers

In the last decades different solutions have been reported to minimize or compensate the gain-cell losses [142, 140], which are the primary limiting factor

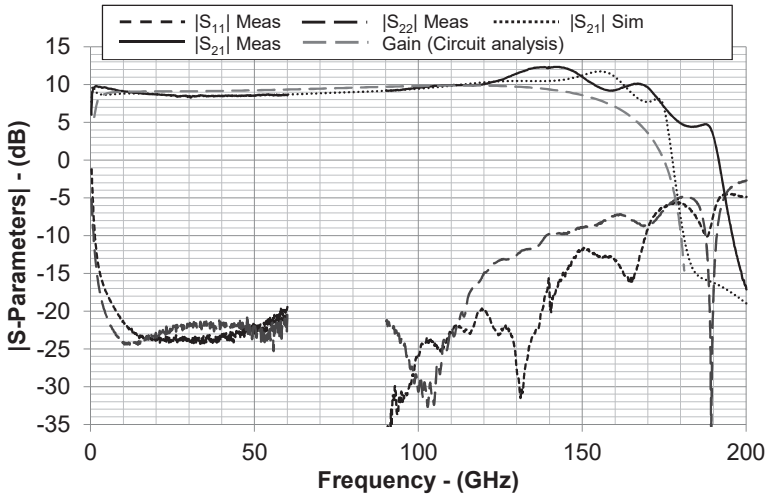


Figure 4.5
Measured S-Parameters of the TWA in Fig. 4.4, and comparison with its simulated —S_{21}—, and power gain as calculated in eq. (4.1) using the simulated values of G_m and α_{in}. From [140] © 2015 IEEE

towards operation at high frequencies of TWAs. However, the most straightforward approach to minimize the impact of the losses is the reduction of the number of cells, as predicted by eq. (4.1). The single-cell configuration is, therefore, the one with the frequency response less penalized by the synthetic losses and, thus, the fastest distributed architecture. On the other hand, using just one gain element results in low amplifier gain. Cascading several single-cell DAs [155, 156] achieves gain levels comparable to TWAs, while still reaching the highest possible frequency of operation for a given cell. Amplifiers with such structure are referred to as Cascaded Single-Stage Distributed Amplifiers (CSSDA) in literature [157, 158, 159, 160, 161, 162, 163, 164, 165]. Fig. 4.6 illustrates their circuit schematic. In the DAAB and DAAB-Tx projects, two CSSDAs optimized for low power or maximum frequency of operation have been fabricated with the *SG13G2* technology to validate the concepts experimentally.

Fig. 4.7 and 4.8 show the schematic and micro-photograph of the CSSDA designed for low power consumption [163]. The circuit consists of four cells based on an inductively-peaked cascode topology. The inductor L_b has been employed for the peaking creating positive feedback at the base terminal of the transistor Q_1. The value of L_b is 6 pH, which is obtained with the parasitic inductance of the interconnections between the base of Q_1 and the bias distribution network. The discussion of this peaking technique is presented in detail in [150]. The S-Parameters measurement for the operation point $I_{CC} = 13\,\text{mA}$ and $V_{CC} = 1.5\,\text{V}$ are shown in Fig. 4.9. For a power consumption of just

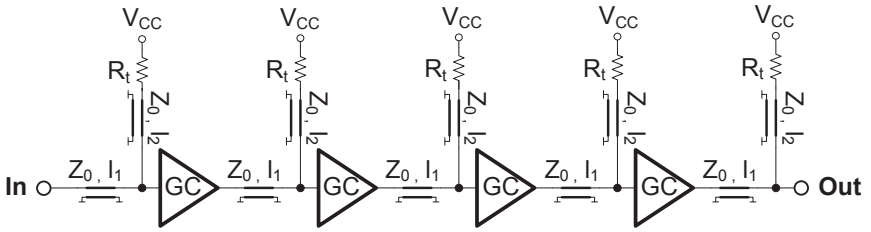


Figure 4.6
CSSDA circuit schematic. The gain-cells are labeled with GC. From [154] © 2016 IEEE

19.5 mW, the CSSDA provides 9.5 dB of gain, over a 130 GHz-wide −3 dB frequency-band which spans from 50 GHz to 180 GHz. The resulting GBP is 388 GHz.

The second CSSDA developed within the project targeted high frequencies of operation, demonstrating a response with a −3 dB upper-corner frequency of 250 GHz [159]. Fig. 4.10 shows the schematic of the CSSDA, while its micro-photograph is illustrated in Fig. 4.11. The circuit consists of four gain cells based on cascode topology. The cell input pole $R_{in}{\cdot}C_{in}$ is one of the factors that limit the CSSDAs operation at high frequencies. The design targeted, therefore, its minimization. A wide transistor Q_0 has been then used to reduce the cell input-resistance R_{in}. The emitter area of the device is $6{\times}0.9{\times}0.07\mu m^2$. Indeed, the larger the emitter area, the bigger is the input capacitances of the cells. C_{in} was then reduced with the C_b capacitor in series with the base of Q_0, as usually done in the capacitive-division technique [142]. The capacitor C_b dc-decoupled also the gain elements. Its value is 125 fF. Fig. 4.12 shows the S-Parameters measurements. They were acquired when the circuit was biased at $I_{CC} = 23$ mA and $V_{CC} = 3.2$ V, resulting in 74 mW of power consumption. In the selected operation point, the amplifier provides a gain of 13 dB with a −3 dB bandwidth of 160 GHz, which spans from 90 GHz to 250 GHz. The resulting GBP is 715 GHz.

Table 4.2 presents a comparison with recently-published CSSDAs in both Silicon and InP technologies. Since the amplifier gain can be increased using more cells at expenses of chip area and power consumption (P_{DC}), the FoM introduced before is here recalled [144]:

$$FoM = \frac{GBP}{Area \times P_{DC}} \quad [\frac{GHz}{mm^2 \cdot mW}] \tag{4.4}$$

The CSSDA optimized for low power achieves the lowest power consumption and the highest figure of merit for CSSDA implementations, confirming that the circuit is well suited at the same time for low power, high speed, and broadband applications. The CSSDA optimized for high-frequency operation

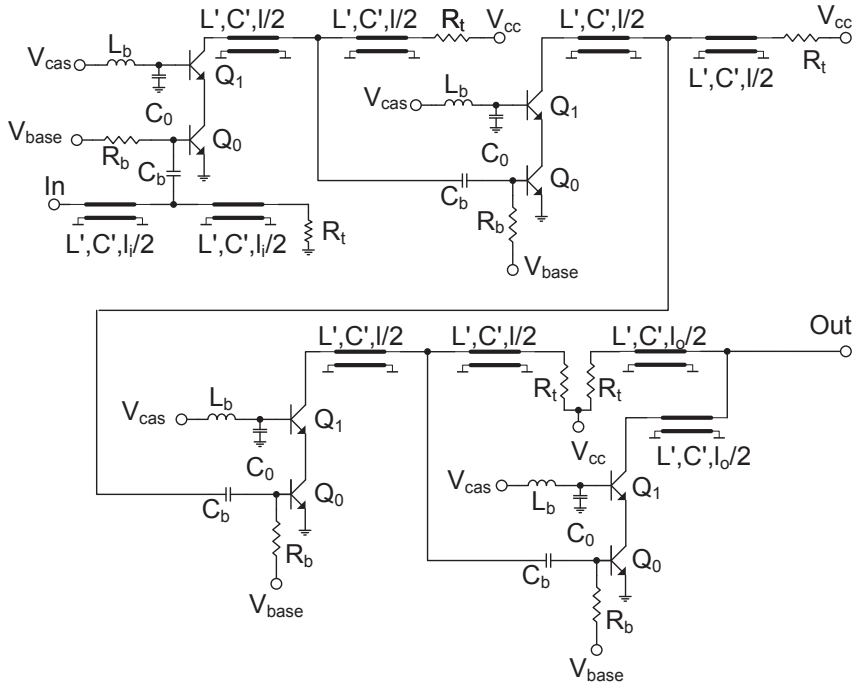


Figure 4.7
Circuit schematic of the CSSDA optimized for low power consumption. From [163] © 2015 IEEE

achieves the highest −3 dB upper frequency, the smallest chip-area, and one of the highest FoM for silicon implementations. These improvements result from the set of presented design solutions, which can help to exploit at best the capabilities of the available integrated circuit technology.

4.2.3 Traveling-Wave Combiners and Dividers

Within the DAAB and DAAB-Tx projects, a Traveling-Wave Combiner (TWC) [166] and a Traveling-Wave Divider [167] (TWD) have been demonstrated. Fig. 4.13 shows the circuit schematic of the developed distributed combiner. The circuit consists of two stages. The first one consists of two TWAs, which share the output line and are used to perform the signal combination. The second section of the circuit is composed of a CSSDA, which is employed to provide high amplification while requiring less chip area and power consumption than TWAs [159, 156, 158, 163].

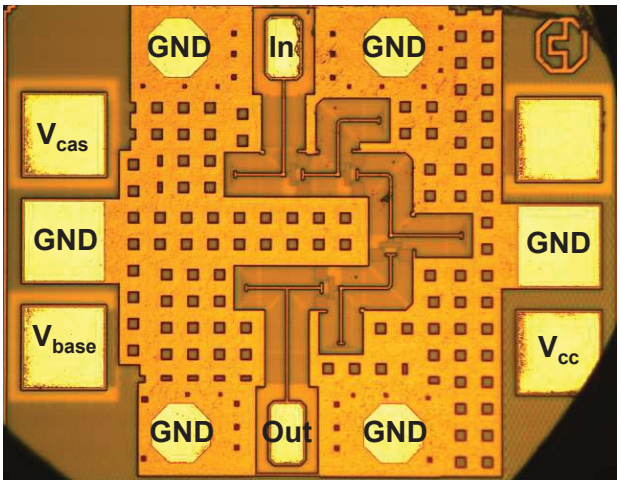


Figure 4.8
Micro-photograph of the CSSDA optimized for low power consumption. The die size is 0.28 mm^2. From [163] © 2015 IEEE

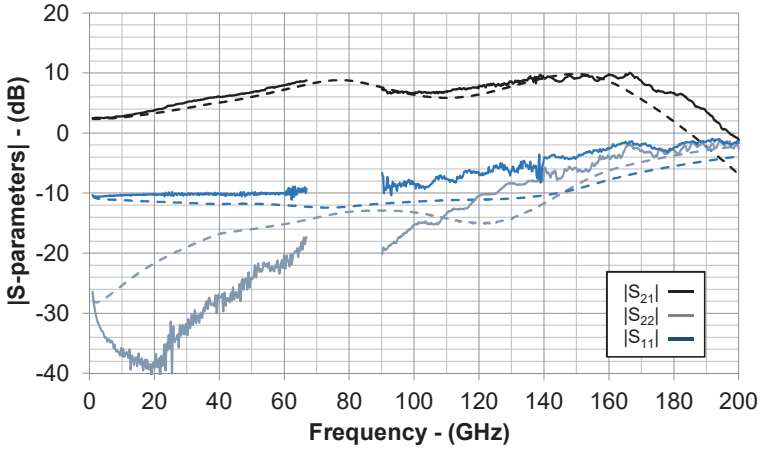


Figure 4.9
Measured (solid) and simulated (dashed) S-Parameters magnitude of the CSSDA in Fig. 4.8 for $I_{CC} = 13$ mA and $V_{CC} = 1.5$ V. From [163] © 2015 IEEE

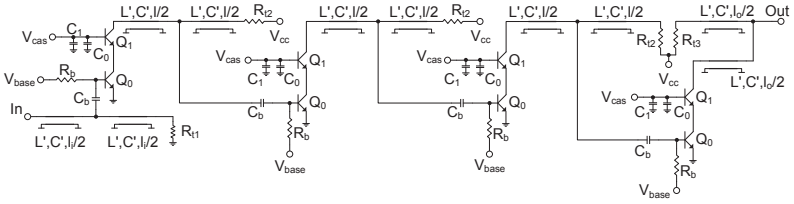


Figure 4.10
Schematic view of the CSSDA optimized for high speed. From [159] © 2015 IEEE

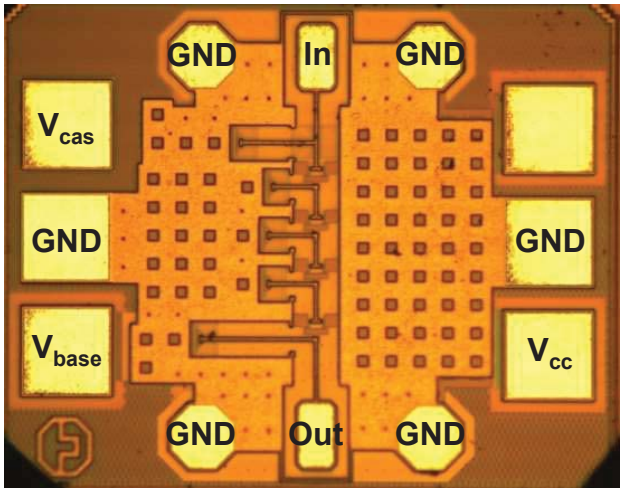


Figure 4.11
Micro-photograph of the CSSDA optimized for high speed. From [159] © 2015 IEEE. The die size is 0.23 mm^2.

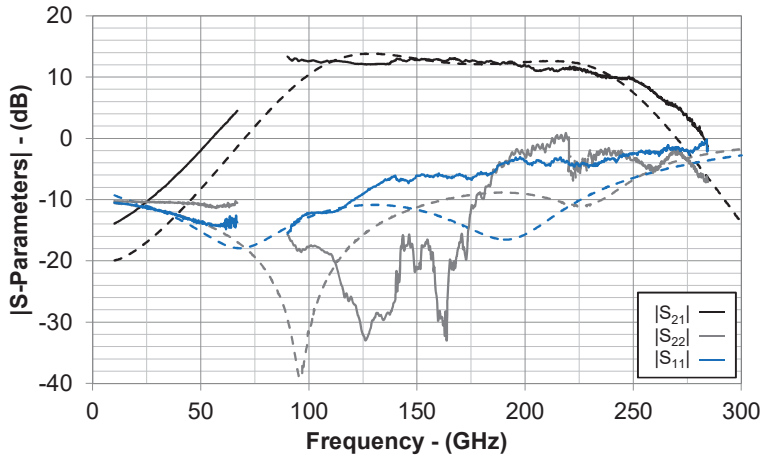


Figure 4.12
Measured (solid) and simulated (dashed) S-Parameters magnitude of the CSSDA in Fig. 4.11 for I_{CC} = 22 mA and V_{CC} = 3.2 V. From [159] © 2015 IEEE

Table 4.2
CSSDAs state of the art. From [163] © 2015 IEEE

P_{DC} [mW]	Area [mm^2]	FoM	BW [GHz]	Gain [dB]	GBP [GHz]	$f_{UP,3dB}$ [GHz]	Technology	Ref.
120	0.72	3.6	70	13	312	70	90 nm CMOS	[164]
90	0.31	28	90	20	800	80	40 nm CMOS	[165]
60	0.36	9.2	25	9	199	25	0.18 µm CMOS	[162]
46	0.54	59	235	16	1480	235	InP DHBT	[158]
74	0.22	46	170	13	760	250	0.13 µm SiGe	CSSDA optimized for High Speed
19.5	0.28	71	130	9.5	388	180	0.13 µm SiGe	CSSDA optimized for Low Power

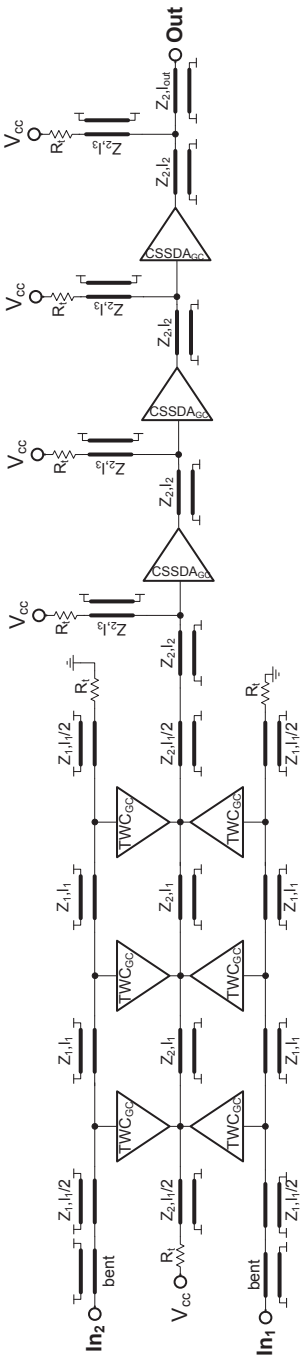


Figure 4.13
Schematic of the distributed combiner designed within the DAAB(-Tx) projects. The TWC and CSSDA gain cells are indicated by TWC_{GC} and $CSSDA_{GC}$ respectively. From [166]

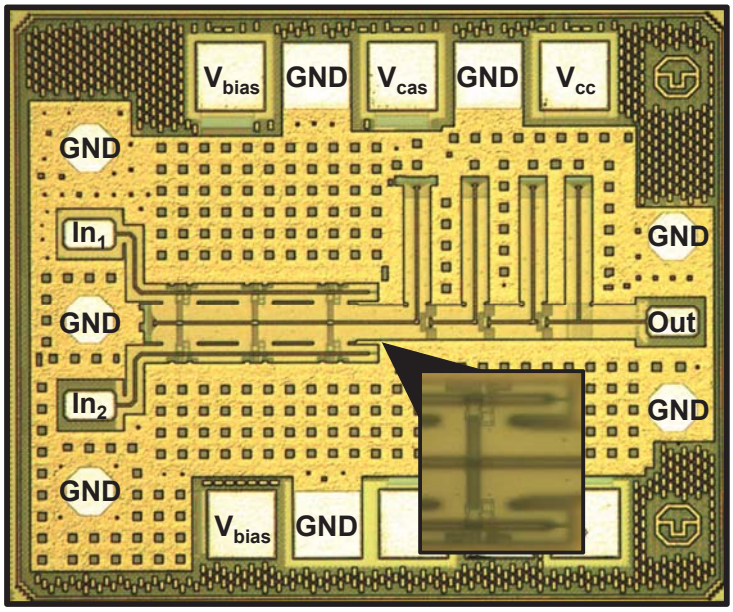


Figure 4.14
Micro-photograph of the fabricated distributed power combiner. From [166] © 2016 IEEE. The chip dimensions are 0.7 mm×0.8 mm, while the chip area is 0.56 mm^2. The TWC gain-cell is illustrated in the inset.

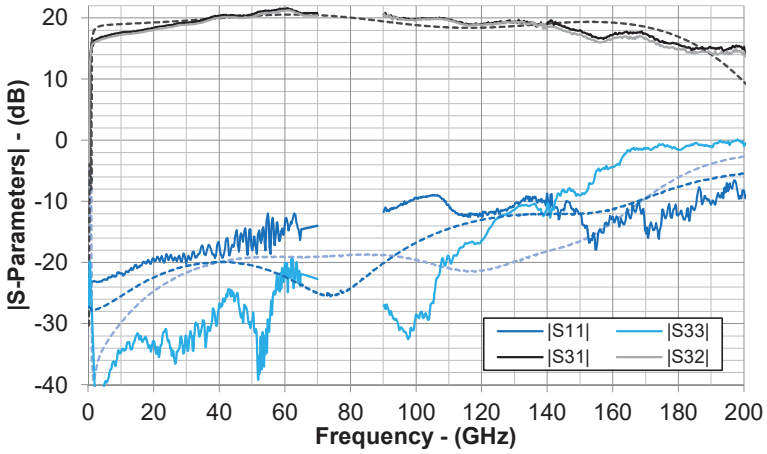


Figure 4.15
Measured (solid) and simulated (dotted) S-Parameters of the combiner in Fig. 4.14. From [166] © 2016 IEEE. The input ports are I and II, while the output is port III.

Table 4.3
State of the art of distributed power combiners. From [166] © 2016 IEEE.

Ref.	**Gain** [dB]	**BW** [GHz]	$\mathbf{P_{DC}}$ [mW]	**Area** [mm^2]	$\mathbf{\Delta t_p}$ [ps/GHz]	**Technology**
[168]	6	1-10.6	15	1	10/10	0.13 µm CMOS
[169]	8	2-8	300	7.59	NA	0.5 µm GaN HEMT
[170]	3	2-18	NA	9	NA	GaAs
[171]	3	4-40	46	1	NA	0.25 µm InP HEMT
This work	20	1-170	203	0.56	10/170	0.13 µm BiCMOS

Fig. 4.14 shows the micro-photograph of the distributed combiner. The total chip area is 0.57 mm^2. The S-Parameter measurements of the combiner are presented in Fig. 4.15. They were acquired when the system was biased at $I_{CC} = 58$ mA and $V_{CC} = 3.5$ V, resulting in 203 mW of power consumption. A VNA was employed for the characterization. In the selected operation point, the circuit provides a gain of 20 dB over the −3 dB bandwidth from 1 GHz to 170 GHz. From 170 GHz to 220 GHz, the gain is still above 15 dB, demonstrating the combiner capabilities with significant gain even at this frequency.

Table 4.3 presents the state of the art of distributed power combiners. The demonstrated circuit shows the highest −3 dB upper frequency $f_{UP,3dB}$, as well as the broadest bandwidth of operation and gain. In detail, $f_{UP,3dB}$ is improved from 40 GHz to more than 200 GHz, which amounts to a factor 5 of advancement. The presented results are supported by the *SG13G2* process, in conjunction with the described design techniques.

Fig. 4.16 shows the complete schematic of the divider. It consists of 12 gain cells connected with on-chip microstrip lines [167]. Their inductance and capacitance per unit-of-length are 0.5 µH/m and 80 pF/m, respectively, which corresponds a characteristic line impedance of 79 Ω. The tapering of the synthetic-line impedance aims at increasing the output power and the maximum frequency of operation, and it is achieved reducing the distance between the cells in the direction of propagation of the input signal. The length of each line is annotated on the circuit schematic in Fig. 4.16.

The initial length *len* of the lines is 100 µm, while the tapering parameter x has been set to 8 µm. Indeed, the tapering is also beneficial for the silicon footprint of the circuit, which is reduced due to the smaller distance between the gain cells.

Fig. 4.17 shows the micro-photograph of the fabricated TWD. The total area of the die is 0.8 mm^2, while the active area of the circuit is 0.1 mm^2. All the measurements presented in this section have been acquired on-chip with bias operation point $I_{CC} = 100$ mA and $V_{CC} = 3$ V. The S-Parameters characterization of the divider was performed with a VNA plus extender modules. Due to the lack of equipment for the differential S-Parameter measurements above 60 GHz, the divider path-gain was measured with a single-ended setup.

Fig. 4.18 shows the S-Parameters of the TWD as measured and simulated. The divider provides a gain with a maximum value of 10 dB and a −3 dB bandwidth from 300 MHz to 180 GHz. The useful frequency band of the component, defined as the band where the gain is above 0 dB, spans from 100 MHz to 200 GHz.

Fig. 4.18 also shows the measured and simulated input and output matching: $|S_{11}|$ is below −10 dB for the whole −3 dB frequency band, while $|S_{22}|$ is below −10 dB up to 155 GHz, and it reaches −5 dB at 200 GHz.

Table 4.4 presents an overview of the state of the art for this class of circuits. The demonstrated design shows the highest frequency of operation, as well as the widest bandwidth of amplification. In fact, for BiCMOS processes [172, 173], the state of the art is improved by a factor of 10 from 20 GHz to 200 GHz for the highest operation frequency, defined as the frequency where the divider gain crosses 0 dB. Extending the comparison to other technologies, the highest frequency of operation reported is 40 GHz [174], which this work improves by a factor 5.

4.3 Antenna Design Requirements

In addition to the aforementioned broadband traveling-wave amplifiers, there is the necessity for broadband antenna designs. In this section, based on a short comparison between integrated and in-package antennas, several antenna design constraints due to semiconductor technology are presented. Moreover, several integrated antenna designs, both linear polarized as well as dual-polarized are introduced. The antenna designs presented in this section have been developed at the chair for RF and photonics engineering at the Technische Universität Dresden. As stated before, first, a short comparison of systems-on-chip (SoC) and systems-in-package (SiP) is drawn, with an emphasis on the requirements for the corresponding antenna design. Consequently, the semiconductor technology and here especially the back-end of line (BEOL) which contains the metal layers necessary for the antenna design is briefly introduced. Furthermore, the corresponding antenna design constraints due to the limitations imposed by the manufacturer are described.

4.3.1 Systems-on-Chip and Systems-in-Package

Combining antenna and integrated circuit can be performed in two different ways, basically. First, both parts can be manufactured in different processes and consequently, they need to be connected by e.g. wire-bonds or flip-chip. This is the so-called system-in-package (SiP) approach. One of its biggest advantages is that for each component the most suitable process can be selected [179]. In terms of of the antenna to be developed that results in choosing a

material with a low $\tan\delta$ in order to reduce the occurring losses. Moreover, in a lot of cases a low relative permittivity ϵ_r, e.g. in the range of three, is selected to enhance the radiation towards air and not into the substrate. This is different for the so-called system-on-chip approach (SoC). Integrating the circuit component as well as the antenna on the same chip and therefore into the same process results in disadvantages for the antenna design regarding the material characteristics and the process stack of the semiconductor process selected [179]. For standard silicon based processes, a substrate showing a high relative permittivity of approximately twelve as well as high losses needs to be taken into account for the antenna design. However, in contrast to the SiP approach, a fully integrated system does not need any connections such as wire-bonds and therefore less connection parasitics occur. Moreover, there will not be a $50\,\Omega$ boundary between antenna and circuit any longer if an antenna-amplifier co-design is performed [179]. Therefore, all antenna designs shown later on, are based on the SoC approach and, hence, a silicon substrate and the corresponding design constraints have to be taken into account for the antenna design.

4.3.2 Semiconductor Technology

The semiconductor technology used for the antenna designs is basically defined by the requirements of the amplifier design with respect to the required transit frequency and maximum oscillation frequency. Dealing with high-frequency designs in the area of 200 GHz, one suitable semiconductor process is the silicon-germanium based BiCMOS SG13 process of IHP [180]. This process offers a high transit frequency and maximum oscillation frequency of 300 GHz and 500 GHz, respectively, which enables a wideband system design in the frequency range addressed. A schematic diagram of the back-end of line of this process is given in Fig. 4.19. Seven metal layers, five thin ones (M1 ... M5) with a height around 0.45 µm and two thick ones, TopMetal2 (TM2) with a height of 3 µm and TopMetal1 (TM1) with 2 µm, result in an overall height of the BEOL of approximately 15 µm. Therefore, the height of the BEOL is only $1/100$ of the free space wavelength at 200 GHz. The BEOL is placed above the silicon substrate with a relative permittivity ϵ_r of 11.9 and a conductivity of $2\,\mathrm{S\,m^{-1}}$ [181]. An available height of the silicon substrate is 300 µm; however, several other heights can be selected. Depending on the actual height of the silicon

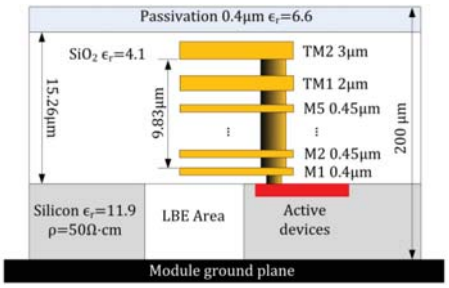


Figure 4.19
Back-end of line of the IHP SG13 process. From [181]. ©2014 IEEE

substrate and the placement of a reflector beneath the substrate, the substrate influences the antenna performance to a high extent, which will be discussed in more detail in the next section together with the design constraints defined by the thin BEOL.

4.3.3 Technology Constraints

Due to the thin BEOL, only planar antenna designs can be realized in standard technology without requiring any post-processing steps. Therefore, designs like horn antennas cannot be fabricated in such a standard technology. However, placing lenses beneath the silicon substrate can be an option in order to increase the available antenna gain. The placement of such lenses can be critical as well as the interface between silicon substrate and lens. Therefore, in the following, only planar antenna designs without the necessity for post-processing steps are discussed. Nevertheless, in order to increase the gain, a reflector is placed underneath the silicon substrate, which can decrease the achievable bandwidth of the overall system, as the placement of the reflector is frequency dependent. In general, the overall structure consisting of a region with a material of high relative permittivity, a reflector below and air above resembles a dielectric slab waveguide and therefore, in principal, substrate modes can propagate. The cut-off frequencies for these modes can be calculated as shown in [182]. It has to be stated, that the cut-off frequency of the TM_0 mode is 0 GHz (including a reflector) and therefore part of the radiated power is trapped in the substrate mode and partially radiated towards the edges of the silicon substrate. Moreover, the high relative permittivity of the silicon substrate of approximately 11.9 results in a preference of radiation towards the back of the substrate rather than towards air. Furthermore, due to the low conductivity, ohmic losses occur in the silicon substrate. Nevertheless, the antenna designs presented in this section later on show a moderate realized gain together with a high impedance bandwidth. Most semiconductor processes define metal density requirements. This implies that a minimum metal density as well as a maximum metal density need to be achieved on all metal layers. This results in the necessity of fill structures especially on the layers, that are only used for feeding and routing. However, the existence of such fill structures changes the effective material properties of the entire BEOL and therefore the antenna characteristics as well. In order to realize complex antenna designs, the layout needs to be rastered in a way that only 0°, 45° as well as 90° are allowed for the technology to be used.

4.4 Integrated Antenna Designs

In order to achieve high bandwidth values, several antenna design approaches have been studied. First, frequency-independent antennas have been investigated as they promise very high bandwidths. Second, using several small antennas for adjacent frequency ranges taking into account the total active reflection coefficient have been studied. Third, the use of localized-backside etching (LBE) as well as post-processing steps by using laser-beam etching have been examined. And fourth, dual-polarized antennas have been studied. In the following sections, exemplary antenna designs for broadband antennas based on the frequency-independent design approach as well as dual-polarized antenna designs will be presented.

4.4.1 Linear Polarized Antennas

Two linear polarized integrated antenna designs showing high bandwidth values are presented. First, a log-spiral antenna and, second, a stacked Vivaldi-shaped open-slot antenna. All simulations shown in the following are performed with Ansys HFSS.

4.4.1.1 Log-Spiral Antenna

The log-spiral antenna is based on the frequency-independent antenna concept. An antenna which can be described only by angles is defined as frequency-independent antenna [183]. In principal, an antenna design needs to be infinite in size in order to be truly frequency-independent. In reality, this is not the case and therefore the frequency range to be achieved will be reduced. The lower frequency limit is mainly defined by the overall size of the antennas, whereas the upper frequency limit is given by the size of the feeding gap. However, despite these limitations, in general, frequency-independent antennas with a bandwidth of 40:1 [183] can be designed. Fig. 4.20(a) shows a chip photograph of the fabricated log-spiral antenna [184]. More details about the log-spiral antenna presented in this section can be found in [184].

In order to contact the antenna for characterization purposes with standard microwave probes, a ground-signal-ground (GSG) pad structure is necessary. Therefore, a coplanar-waveguide to microstrip transition is included in the design. The microstrip line is used for feeding the antenna and is implemented on the lower metal layers Metal 5 (ground) and Metal 2 (signal). This configuration with the ground of the microstrip placed between the antenna and the signal line has been chosen in order to reduce the distortion of the antenna pattern due to the feeding line. As stated before, on all metal layers, fill structures have been placed as shown on the first metal layer in Fig. 4.20(a). Moreover, in order to comply with the design rules defined by the foundry, small slots are placed on the spiral. These slots do not deteriorate the perfor-

mance of the antenna. In order to define the bandwidth of the antenna, not only the impedance bandwidth is taken into account, but the radiation characteristics as well. Therefore, the bandwidth is defined as the frequency range, where S_{11} stays below $-10\,\mathrm{dB}$ and the realized gain is above $0\,\mathrm{dBi}$. This definition holds true for all the antenna designs presented in this section. First, a comparison of the measured and simulated impedance matching is shown in Fig. 4.20(b). A relative bandwidth of 36 % was measured, that is a bandwidth of 66 GHz at a center frequency of 183 GHz. There are slight differences between the measured and simulated values, which occur most probably due to differences of the real material values with the ones given by the foundry. In order to investigate such differences, a material characterization measurement platform is built at the chair for RF and photonics engineering. This platform is based on transmission line measurements and a consequent de-embedding in order to achieve the actual values of the material. As stated before, the second important parameter in order to define the overall bandwidth of the antenna is the realized gain. Simulations have shown, that the realized gain exceeds 0 dBi for the frequency range from 152 GHz to 220 GHz with a maximum value of 7.5 dBi at 220 GHz. Small dips occur at 164 GHz and 204 GHz [184]. Consequently, the antenna bandwidth can be given as 66 GHz and 36 %, respectively. A second antenna design promising similar bandwidth values is an open-slot antenna.

4.4.1.2 Stacked Vivaldi-Shaped Open-Slot Antenna

By using a stacked Vivaldi-shaped open-slot antenna, an increased radiation towards air shall be obtained in contrast to a one-element Vivaldi-shaped open-slot antenna. In this case, the stacked Vivaldi-shaped open-slot antenna consists of two Vivaldi-shaped elements which differ only in the length. This antenna has been presented in [185]. The length of the upper antenna element is reduced in order to increase the gain. All other geometric parameters (width, opening rate) stay the same. The upper antenna element is placed on TopMetal 2 while the lower one is placed on Metal 5. TopMetal 1 is used for the feeding line. Both antenna elements are fed by the same stripline, which is terminated by a stub. In order to ensure proper characterization, a stripline to coplanar-waveguide transition is included in the design as illustrated in Fig. 4.21(a), which shows the fabricated two times stacked Vivaldi-shaped open-slot antenna.

As for the log-spiral antenna, fill elements have been placed on all metal layers in order to comply with the metal density requirements of the selected manufacturing process. The silicon substrate has a height of 300 µm and a reflector is placed below in order to focus the radiation towards air. For the simulations, a reflector size of 1 mm × 1 mm has been chosen. In order to evaluate the impact of fill structures on the antenna performance, the S_{11} has been simulated for both cases, one including metal fill in the topmost three metal layers and one without any fill structures. Including metal fill on all

layers would increase the memory consumption and simulation time to a high extent. In Fig. 4.21(b) the simulation results for both cases in the frequency range from 160 GHz to 210 GHz are compared. It can be seen that, for this design, the fill structures do not influence the return loss to a high extent. In comparison to the simulation without fill, the presence of fill reduces the relative impedance bandwidth only slightly from 24.8 % to 23.2 %. Most probably this is caused by a changed value for the effective relative permittivity of the material as a result of including metal cells. Besides the return loss of the antenna, the radiation characteristics are of importance in order to evaluate the overall performance of the antenna design. The realized gain stays above 0 dBi for the frequency range from 165 GHz to 190 GHz. For frequencies above 190 GHz the realized gain drops below 0 dBi. According to the bandwidth definition determined in the previous section, the overall antenna bandwidth is 23 GHz, with the lower boundary at 167 GHz defined by the S_{11} and the upper boundary at 190 GHz defined by the realized gain. The radiation pattern in the x-z-plane as well as the y-z-plane for several frequencies is shown in Fig. 4.22.

Besides the maximum realized gain value, the half-power beamwidth (HPBW) is used to describe the radiation characteristics of the antenna design. A realized gain of 1.2 dBi, as well as a HPBW of 75° (x-z-plane) and 61° (y-z-plane) is achieved at 180 GHz. In order to further increase the antenna bandwidth, a modified design has been investigated including a third antenna element (see [186]). For this design, a usable bandwidth of approximately 45 % is achieved with the lower boundary at 155 GHz and the upper boundary at 244 GHz. Furthermore, a maximum realized gain of 3 dBi has been attained.

4.4.2 Dual-Polarized Antennas

Other possible antenna designs to achieve high available bandwidths in contrast to the aforementioned designs are dual-polarized antennas. In principal, by using both polarizations independently of each other, the overall usable system bandwidth can be increased. In the following, two antenna designs are presented: First, a crossed Vivaldi-shaped open-slot antenna and, second, a combined slot and fractal bowtie antenna.

4.4.2.1 Crossed Vivaldi-Shaped Open-Slot Antenna

The crossed Vivaldi-shaped open-slot antenna is based on the presented Vivaldi-shaped open-slot antenna in the previous section. However, for this dual-polarized design, only one antenna layer is used. The fabricated antenna has a size of 1.36 mm × 1.36 mm and is shown in Fig. 4.23(a) [187]. This design has been published in [187].

The antenna is comprised of two crossed slots and each one is fed by a microstrip line terminated by a stub. Since each slot is fed separately at its center position, the crossing of both slots needs to be performed out-of-center in order

to be able to wire the feeding lines to each element without the requirement of an additional crossing. In close proximity to each of the slots' ends, metal lines with a length of 300 µm have been added which act as directors and increase the gain towards air [188]. For contacting each port of the antenna, a microstrip to coplanar-waveguide transition is included in the design. The silicon substrate has a height of 300 µm and a reflector is placed below in order to enhance the gain towards air. In order to evaluate the impedance bandwidth of this antenna, a comparison of the simulated and measured S_{11} is shown in Fig. 4.23(b). The measured bandwidth is more than 40 % and the shapes of the measured and simulated S_{11} agree well. For the second port, the results are very similar. Deviations between measurement and simulation results are most probably due to slightly different material properties of the fabricated chip in comparison with the values given in the design kit. Moreover, for the simulated frequency range from 140 GHz to 210 GHz, the coupling stays below −13 dB [187]. Besides the return loss of each port and the coupling between each of the two ports, the radiation characteristics are investigated. For the simulation of these characteristics an infinite ground plane was taken into account and therefore, only radiation in the upper hemisphere can be noticed. Moreover, to achieve co-polarization and cross-polarization values, one port is activated and the other one is terminated. Therefore, it can be shown that each slot radiates a linear polarized field. In Fig. 4.24, the radiation characteristics of the dual-polarized crossed Vivaldi-shaped antenna are shown. Both radiation patterns are not identical due to the asymmetric configuration. However, a maximum realized gain of 5 dBi is achieved for both configurations as well as a HPBW of 45° for each co-polarization. The co-polarization to cross-polarization ratio is better than 15 dB if port 1 is active, and it is better than 25 dB if port 2 is active. Therefore, it can be seen that both polarization components corresponding to one port can be used independently of each other and, consequently, the overall system bandwidth can be increased to a high extent.

4.4.2.2 Combined Slot Fractal Bowtie Antenna

Another design to achieve higher usable bandwidths is a combination of a slot and a fractal bowtie antenna as shown in Fig. 4.25(a) [189]. A more detailed investigation of this antenna design can be found in [189]. Two slot bowtie elements are added symmetrically to a fractal bowtie design in order to achieve a symmetric radiation pattern. Therefore, three feeding ports, two for the slot bowtie elements and one for the fractal element, exist. Both slot feeding ports are connected to the same pad structure for probing with one microwave probe. Feeding the slot bowtie elements results in an orthogonal electric field in contrast to the electric field by feeding the fractal bowtie element. This is due to the fact that electric and magnetic fields are exchanged for a slot bowtie and its complementary bowtie, respectively. However, by adding slot feeding ports to the fractal bowtie design, the surface current density can be

influenced. In order to evaluate this effect, the surface current densities with and without added slot elements have been compared and it was found that the surface current density changes only to a low extent (see [189]). The same holds true for the influence of the feeding lines for the slot ports. They are not placed directly below the fractal bowtie but in a short distance to it and, therefore, the influence on the surface current density of the antenna can be decreased [189]. All feeding lines are microstrip lines and to ensure probing, microstrip to coplanar waveguide transitions are implemented to connect the ports to the GSG pads. The silicon substrate has a height of 300 µm and, in order to increase the gain, a reflector is placed underneath the substrate. The overall size of the fabricated antenna is 1.5 mm × 1 mm.

In order to evaluate the performance of the antenna, both, the impedance bandwidth as well as the radiation characteristics need to be investigated. The impedance bandwidth of both antenna elements is defined by S_{11} lower than −10 dB and therefore, the S_{11} of both elements is shown in Fig. 4.25(b). Simulations and measurements agree well; the existing deviations are mainly based on differences between the actual material parameters and the ones given in the design kit and the surrounding of the seal ring, which is defined by the foundry. The measurements have shown impedance bandwidths of more than 40 GHz. Similarly to the crossed Vivaldi-shaped open-slot antenna, in order to evaluate the co-polarization to cross-polarization ratios, the radiation patterns are shown for the activated slot bowtie port and the terminated fractal bowtie port and vice versa. Both cases are shown in Fig. 4.26. Since, in the simulations, there is an infinite reflector placed underneath the substrate, radiation occurs only in the upper hemisphere. If the fractal bowtie port is activated, a difference between co-polarization and cross-polarization of about 25 dB can be seen and if the slot bowtie port is activated, the difference is about 20 dB. Therefore, for both cases, one field component is dominating and, consequently, both field components can be used separately from each other; the overall available bandwidth can be increased in comparison with a single fractal bowtie antenna design.

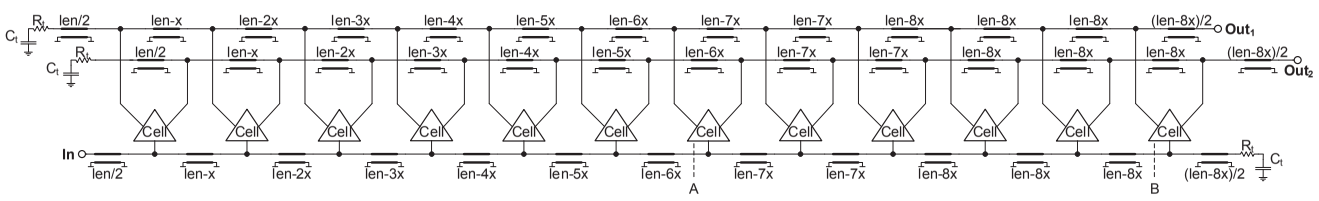


Figure 4.16
Circuit schematic of the developed traveling-wave divider: 12 gain cells are embedded in a tapered architecture. From [167]

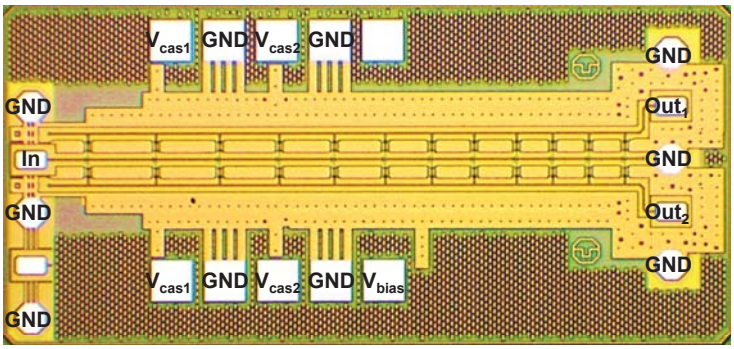


Figure 4.17
Micro-photograph of the fabricated TWD: the dimensions of the chip are 0.6 mm×1.3 mm, while the chip area is 0.8 mm^2. From [167] © 2018 IEEE

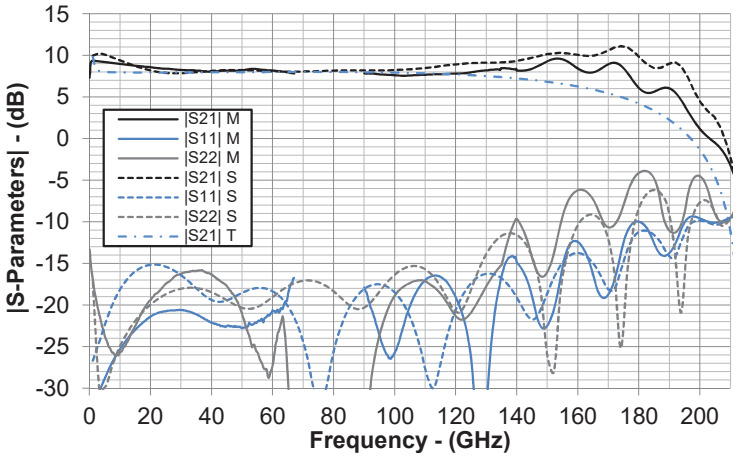
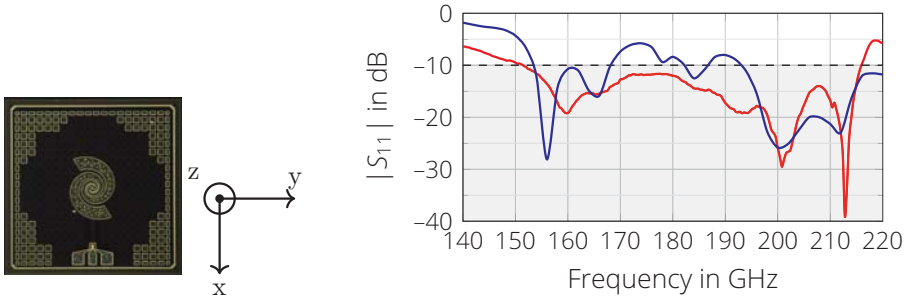


Figure 4.18
Measured (M) and simulated (S) and calculated (T) S-Parameter of the TWD in Fig. 4.17 . From [167] © 2018 IEEE

Table 4.4
State of the art of distributed power dividers. From [167] © 2018 IEEE

Ref.	[175]	[176]	[177]	[178]	[173]	[172]	[174]	This work
Gain>0 dB‡ (GHz)	1-10.6	1-20	2-18	0-20	2-30	2-30	0-40	0.1-200
3-dB BW (GHz)	8	18	16	10	20	21.5	25	180
Supply (V)	1.8	5	NA	2.5	2.5	NA	3	3
P_{DC}(mW)	20.5	NA	NA	160	100	66	NA	300
Gain (dB)	9.5	10	4	5	9.6	11	6	10
Gain Stages	2	5	2	2	2	1	5	12
o1dBCp (dBm)	7.5@5GHz	n.a.	4@6GHz	0@15GHz	2@10GHz	-5.4@12GHz -8.9@22GHz	5@40GHz	10@30GHz 5.6@140GHz
O-iso* (dB)	n.a.	n.an	n.a.	30@10GHz	22@2GHz	25@20GHz	30	35
OI-iso (dB)**	n.a.	60@10GHz	40@12GHz	n.a.	30@2GHz 35@25GHz	n.a	n.a.	30@60GHz 25@170GHz
Δtp/BW (ps/GHz)	n.a.	n.a.	n.a.	100/25	20/25	16/18	n.a	26/180
ΔGain† (dB)	n.a.	n.a.	n.a.	1@18GHz	0.8@15GHz	0.2@15GHz	2@40GHz	0.35@55GHz
ΔPhase† (○)	10/10	n.a.	n.a.	1@18GHz	3.5@15GHz	1.6@15GHz	14@40GHz	5@55GHz
Technology	130 nm CMOS	150 nm GaAs	200 nm GaAs	180 nm CMOS	130 nm SiGe	130 nm SiGe	90 nm CMOS	130 nm SiGe

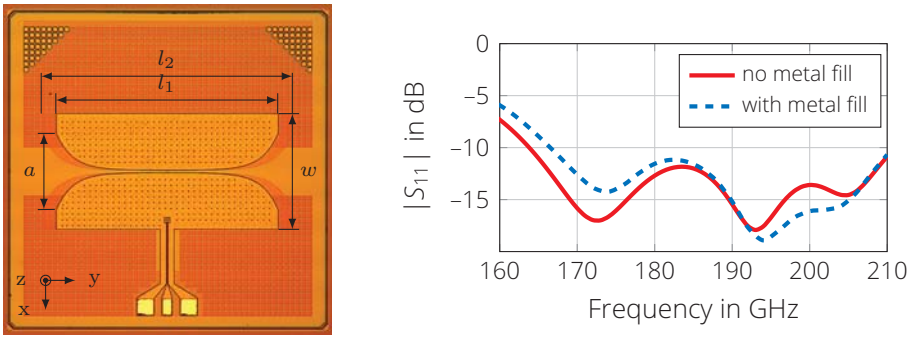
‡: Frequency region where the divider provides gain, *: Output isolation, **: Output to input isolation, †: Unbalance between the path responses.



(a) Chip photograph of fabricated log-spiral antenna.

(b) Comparison of simulated and measured S_{11} of log-spiral antenna. — Simulation, — Measurement

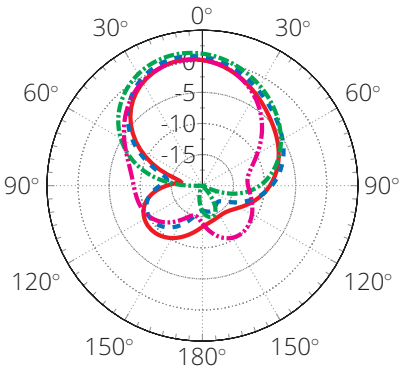
Figure 4.20
Integrated log-spiral antenna. From [184]. ©2018 IEEE



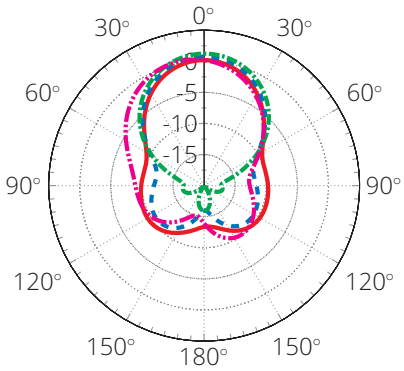
(a) Chip photograph of fabricated stacked Vivaldi-shaped open-slot antenna.

(b) Comparison of simulated and measured S_{11} of two times stacked Vivaldi-shaped open-slot antenna.

Figure 4.21
Integrated stacked Vivaldi-shaped open-slot antenna. From [185]. ©2015 IEEE

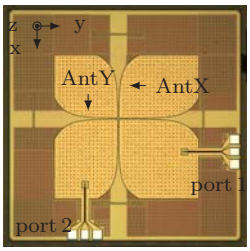


(a) Simulated realized gain in dBi of two times stacked Vivaldi-shaped open-slot antenna in x-z-plane.

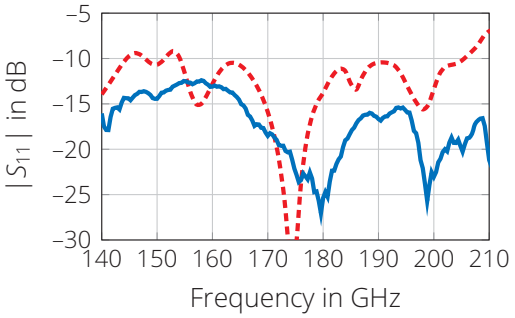


(b) Simulated realized gain in dBi of two times stacked Vivaldi-shaped open-slot antenna in y-z-plane.

Figure 4.22
Radiation characteristics of the integrated Vivaldi-shaped open-slot antenna. From [185]. ©2015 IEEE
— 165 GHz, - - 170 GHz, -·- 180 GHz and -··- 190 GHz.

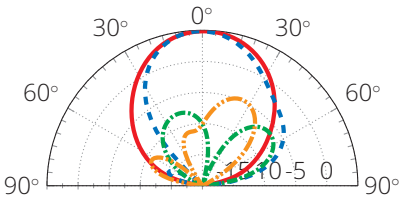


(a) Chip photograph of fabricated dual-polarized crossed Vivaldi-shaped open-slot antenna.

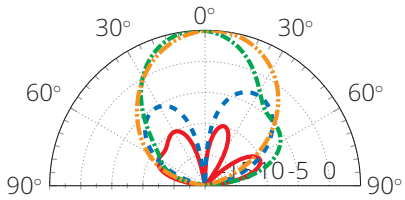


(b) Comparison of simulated and measured S_{11} for one activated port. - - Simulation, — Measurement

Figure 4.23
Integrated dual-polarized crossed Vivaldi-shaped open-slot antenna. From [187]. ©2017 IEEE

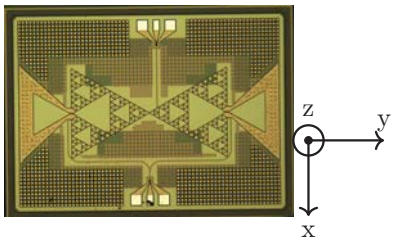


(a) Simulated realized gain in dBi at 180 GHz, port 1 with AntY excited.

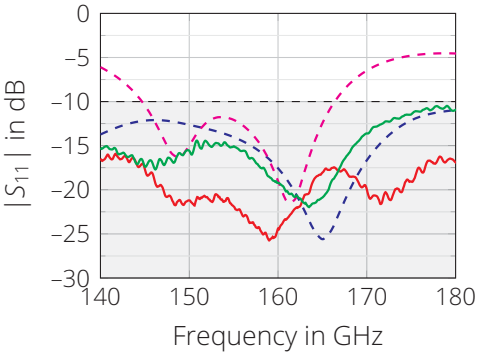


(b) Simulated realized gain in dBi at 180 GHz, port 2 with AntX excited.

Figure 4.24
Radiation characteristics of the integrated crossed Vivaldi-shaped open-slot antenna. From [187]. ©2017 IEEE
Realized gain, x-component: $\varphi = 0°$, $\varphi = 90°$,
Realized gain, y-component: $\varphi = 0°$, $\varphi = 90°$.

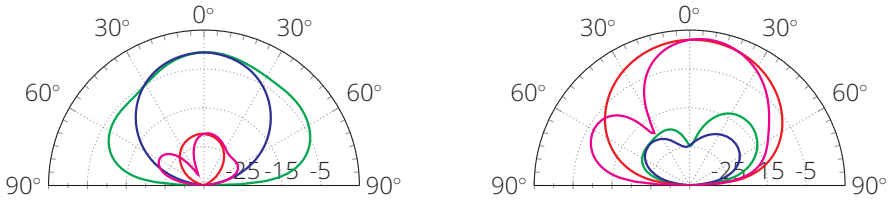


(a) Chip photograph of fabricated dual-polarized combined slot and fractal bowtie antenna.



(b) Comparison of the simulated and measured S_{11} of the dual-polarized combined fractal and slot bowtie antenna.
Simulation Fractal Bowtie Port,
Simulation Slot Bowtie Port,
Measurement Slot Bowtie Port,
Measurement Fractal Bowtie Port.

Figure 4.25
Integrated dual-polarized combined slot and fractal bowtie antenna. From [189]. ©2018 IEEE



(a) Simulated realized gain in dBi of the dual-polarized antenna at 160 GHz for the activated slot bowtie port.

(b) Simulated realized gain in dBi of the dual-polarized antenna at 160 GHz for the activated fractal bowtie port.

Figure 4.26
Radiation characteristics of the integrated dual-polarized combined slot and fractal bowtie antenna. From [189]. ©2018 IEEE
Realized gain, x-component: — $\varphi = 0°$, — $\varphi = 90°$,
Realized gain, y-component: — $\varphi = 0°$, — $\varphi = 90°$.
The cuts are named according to the coordinate system defined in Fig. 4.25(a).