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SPARS — Simultaneous Phase and Amplitude Regenerative Sampling

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2.1 Introduction

Future communication systems will still face a strongly increasing demand for higher data rates, especially regarding mobile devices. Since channel bandwidth is a limited resource, high mm-wave frequencies above 100 GHz are more and more considered especially for ultra-high speed communication links. Possible applications include short-range cable replacement, pass-by downloads and uploads of large amounts of data within seconds. Consequently, cost and energy efficient implementation techniques are a crucial prerequisite for the successful realization of such systems. Upscaling conventional system architectures like the homodyne transceiver towards higher frequencies and larger bandwidth [49], however, comes with notable performance issues due to technological limitations of the available seminconductor processes [50]. Operation above 100 GHz usually means approaching the transition frequency of the underlying seminconductor process, which leads to lower signal power gain per amplifier stage. In order to achieve sufficient total gain for low noise and power amplifiers, amplifier chains consisting of multiple stages are required [51], which leads to substantially larger chip area usage [52], power consumption and noise figure. To overcome this issue, we propose to reconsider fundamental system architecture design decisions. This especially applies to the super-regenerative amplifier as a traditional approach for efficient amplification [53], which has been proven to be scalable towards very high bandwidth and data rate in this project.

The core idea is based on efficient signal regeneration with positive feed-

back. If a single-stage amplifier output is coupled back to its input with more than unity gain, an oscillation emerges from noise. In case of an input signal injected into the feedback loop, e.g., a sinusoidal waveform with a phase and amplitude state which represents the information of a single communication symbol, the oscillation will start with its phasor. Thus, turning the oscillation process quickly on and off allows regenerating a modulated signal as a sequence of pulses with vastly increased power level. Such super-regenerative oscillators were traditionally narrow-band and low frequency, but have gained interest in the last years with the demonstration of faster modulation (11 Mbit/s at 2.4 GHz, [54]), broadband and short-pulse operation (1 ns at 7 GHz, [55]) as well as mm-wave implementation for imaging and radar systems [56, 57, 58].

2.2 System Concept and Demonstrator

In this project, a disruptive, novel system architecture concept has been established to enable efficient mm-wave ultra-high speed communication with substantially lower chip area and power requirements as well as with competitive noise performance and sensitivity even close to the technological limits of a seminconductor technology.

2.2.1 SPARS Concept

The investigated concept is based on regenerative sampling, which means sampling the amplitude and phase information carried by each symbol of a communication signal. This process is carried out by a (super-regenerative) oscillator (SRO) that is turned on and off for each symbol. During oscillation startup, the generated signal emerges from a weak input signal instead of noise and thus preserves the modulation state. At its output, a sequence of pulses with regenerated modulation state but potentially different frequency can be observed with a magnitude significantly larger (20-60 dB) than at its input while only requring a single stage amplifier at the oscillator core. This process is therefore entitled “Simultaneous Phase and Amplitude Regenerative Sampling” and can be employed for efficient amplification as a LNA, PA and driver amplifier replacement in communication systems.

Figure 2.1 shows the proposed system achitecture that targets exploiting this principle’s benefits. It employs an SRO as power amplifier in the transmitter to relax the power level requirements for the modulation and reference signal generation process. Since high gain can be expected, the local oscillator could be derived from a high-order harmonic of the baseband symbol clock and modulated with simple passive radio frequency digital-to-analog converter (RFDAC) cells. On the receiver side, the SRO replaces the low noise amplifier with the special ability to perform gain control over a large dynamic range by

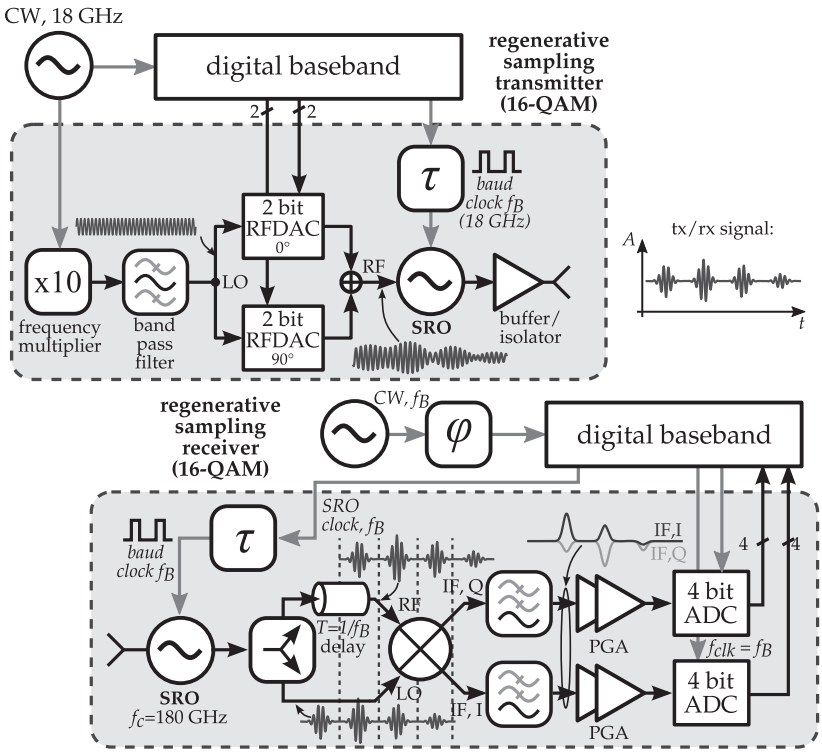

Figure 2.1
SPARS concept for a 100 Gbit/s transceiver with regenerativer sampling and a carrier frequency of 180 GHz. From [59] © 2015 IEEE

tuning the oscillator's duty cycle. Thus, a precisely defined amplitude corridor can be guaranteed at its output, which allows for efficient self-mixing based homodyne downconversion. Hence, the received communication signal is split into two paths and mixed with itself where one path is delayed by the symbol period. This effectively results in differential mixing between each symbol and the previous one. Self-mixing is known from ultra-wideband systems [60], but requires sophisticated gain control to avoid an increased dynamic range at the output due to squaring the signal, which is inherently guaranteed in this architecture. The combination of SRO and self-mixing is especially attractive for mm-wave systems since delay lines are small at high data rates and no PLL-based high output power synthesizer is required for phase-sensitive demodulation. Thus, system size and power consumption are significantly decreased with this approach.

At baseband, synchronous sampling ADCs acquire inphase and quadrature phase signal for one symbol per conversion. This requires some effort for synchronizing the receiver to the transmitters data clock, but synchronisation is required anyway for the SRO sampling process and synchronous operation saves at lot of signal processing in the digital domain. Since the energy per bit budget for approaching 100 Gbit/s is severly limited, this consideration is an important factor towards an efficient implementation of such a system.

2.2.2 Theory and System Analysis

In order to quantify the prospects of the proposed architecture, a theoretic and simulative analysis especially of the high pulse rate operation of a superregenerative oscillator (SRO) has been performed.

State of the art SROs typically operate notably below 1 GHz pulse repetition rate (e.g., 111 MHz at 2.4 GHz [54]) although short pulse generation is already established (e.g., 1 ns at 7 GHz [61]). Implementations in the mm-wave frequency range mostly target imaging applications and are thus low-rate (e.g., [56] at 144 GHz or [57] at 96 GHz). For high data-rate communication systems in the mm-wave domain, short pulses and high pulse repetition rates much beyond the state of the art are required. The maximum achievable data rate strongly depends on the quality factor Q_0 of the oscillator's resonator and the quenching waveform [62, 63]. Both parameters also influcence the input bandwidth and thus selectivity and noise figure. In order to estimate the achievable performance, a simulative analysis based on a parallel resonator with modulated negative resistance (RC-lowpass characteristic with time constant $\tau_0 = 1/f_{osc}$) has been performed for a fixed regenerative gain of 25 dB to determine the minimum time delay between two pulses, which are free of intermodulation. Its results are shown in Figure 2.2.

High symbol rates between 2 and 8 % of the oscillation frequency can be considered realistic for low Q_0 oscillators even with a low single-stage gain of less than 6 dB (see left plot in Figure 2.2), which corresponds to an amplifier

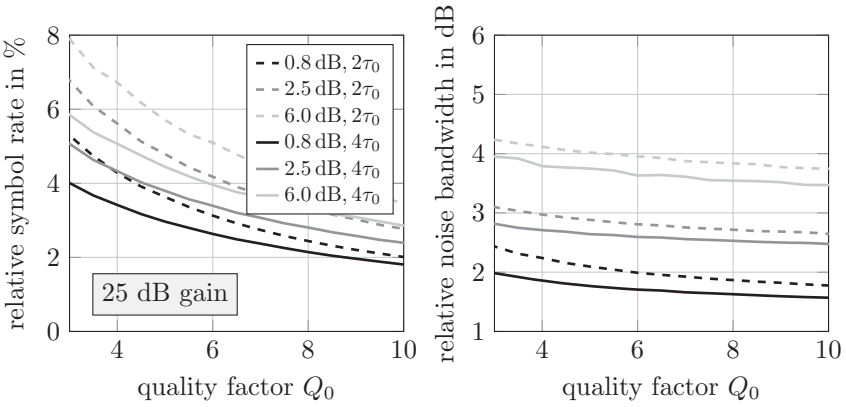

Figure 2.2
Achievable symbol rate in dependence of quality factor, RC constant and open loop gain. [64]

chain with more than four stages. At a center frequency of 180 GHz and 16-QAM modulation, this range already equals approximately 30-60 Gbit/s.

Regarding the achievable sensitivity, input/noise bandwidth and noise figure need to be analyzed. Since the SRO samples its input signal, the signal-to-noise ratio (SNR) is established and finally determined at this stage. Therefore, the SRO bandwidth has been calculated for high symbol rates and represented as the ratio between bandwidth and maximum achievable symbol rate for different quality factors, gain settings and modulation shapes (see right plot in Figure 2.2). The resulting figure "relative noise bandwidth in dB" can be considered the noise excess of the super-regenerative stage compared to an ideal homodyne receiver, e.g., with sinc-shaped symbol envelopes and optimal rectangular filter, which has a bandwidth equalling the symbol rate. Considering the simulation results, a noise excess between approximately 2 and 3 dB can be expected. This originates from the need for oscillation rise and decay during each symbol period, which demands for a higher bandwidth compared to non-pulsed systems. However, this disadvantage is compensated by a notably better noise figure compared to architectures based on amplifier chains. In amplifier chains with low gain per stage, the total noise figure quickly rises with typical degradations in the order of 2-3 dB compared to the single stage [65, 66]. On the contrary, the SRO is based on a feedback based amplification process, where the input signal is permanently present and adds power to the feedback loop for each oscillation cycle whereas the amplifier chain only has an input signal at the first stage. If we assume a noise power source at the amplifier's input, the ratio between signal and noise input power is always constant for the SRO compared to the amplifier chain where only noise is added after the first stage [67, 64]. Thus, the SRO's noise figure

equals the noise figure of a single stage amplifier. Overall, the SRO's noise figure advantage compensated the bandwidth disadvantage and thus results in a sensitivity performance comparable to classic system architectures, but with notably less complexity, chip area usage and power consumption.

From a system architecture point of view, the SPARS concept allows using an oscillator's positive feedback for amplification both in the transmitter and the receiver, which are unstabilized and thus oscillate at their natural frequency with low input power levels, only the oscillation's phase is recovered from the input. Since one of the approach's major benefits is the possibility to build phase sensitive transceivers without the need for mm-wave PLLs, the lack of frequency stability in the SROs has been investigated based on a theoretical analysis. Starting from a transmit signal

$$s(t) = \mathrm{Re}\left\{ \exp(j\omega_{Tr}t) \cdot \sum_n B[n] \cdot \mathrm{rect}(t - nT) \right\} \tag{2.1}$$

with complex data sequence $B[n]$, symbol duration T and transmit carrier frequency ω_{Tr}, the baseband signal sampled at the receiver after passing the system according to Figure 2.1 is according to [64]:

$$r(t) = \tfrac{1}{2} B[n] \cdot B^*[n-1] \cdot \left|H(\omega_{Tr}, T_d)\right|^2 \cdot \left|H(\omega_T, T_d)\right|^2 \cdot e^{j(\omega_{Tr}T + \omega_T \Delta T)}, \tag{2.2}$$

with time-variant SRO frequency response $H(\omega, t)$, transmitter SRO frequency ω_T, SRO pulse duration T_d and the deviation between transmitter and receiver sampling rate ΔT. Consequently, the only significant influence of the transmitter SRO is a phase offset, which depends on a mismatch between Tx and Rx symbol rate (like also present in conventional systems), whereas the receiver's SRO frequency disappears after self-mixing. If Tx and Rx have sufficient sampling clock synchronization, which is required anyway for synchronous SRO sampling at the pulse maxima, the error is low and only a constant phase offset remains, which depends on the (stabilized) transmitter reference. Hence, the use of unstabilized oscillators for regeneration does not result in significant disadvantages regarding carrier stability.

2.2.3 Homodyne System Demonstrator

In order to demonstrate the feasibility of the proposed novel architecture, its first demonstrator implementation has been performed at a low carrier frequency of 5.5 GHz, where comprehensive experimental characterizations of all system components are feasible compared to mm-wave systems that require higher integration levels.

Figure 2.3 shows the block diagram (top), the transmitter setup with passive modulator (center left), the self-mixing receiver setup (center right) as well as the transmission experiment setup (bottom). The system is based on an electrically small SRO assembled from lumped components, which achieves a pulse rate of 150 MHz with a 5.5 GHz oscillator core. Since this experiment was

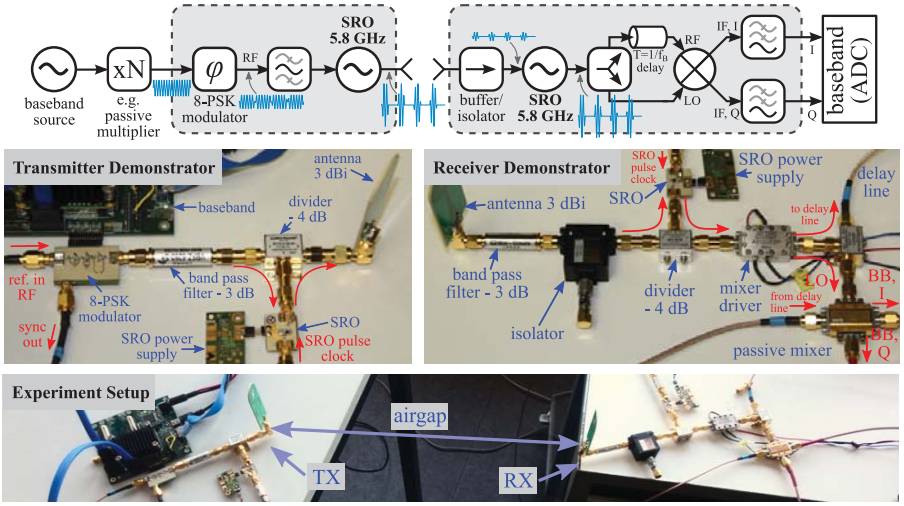

Figure 2.3
5.5 GHz implementation of an 8-PSK regenerative transmitter and receiver based on the SPARS concept to demonstrate over-the-air transmission with double regeneration (Tx PA-SRO and Rx LNA-SRO). From [67] © 2017 IEEE

focused on the most critical aspect of phase coherence and phase sensitivity, only PSK modulation has been implemented using a passive delay-switched 3-bit phase modulator, which delivers a data rate of 450 Mbit/s.

The transceiver performance (Figure 2.4) shows an overall EVM of -24 dB for a minimum required EVM of -18 dB for 8-PSK with a BER below 10^{-3}. The receiver is limited by its sensitivity of -75 dBm, which almost approaches the theoretic prediction of 77 dBm based on the properties of the given SRO implementation [67, 64].

In order to explore the possibility of 16-QAM modulation, a 21 GHz SRO demonstrator has been evaluated with 343 MHz symbol rate (1.37 Gbit/s) and 20 dB regenerative gain out of a 5 dB gain single-stage amplifier [59, 68]. Due to its microstrip implementation with four wavelengths in the feedbackup loop, the theoretical symbol rate for its Q_0 of 3 is 2.3% of the oscillation frequency, which has been approached closely with 1.63% despite the limitations of PCB-based technology.

In summary, the system concept has been successfully verified to enable very high data rates in relation to the carrier frequency with notably less complexity while retaining the sensitivity performance of classic system architectures.

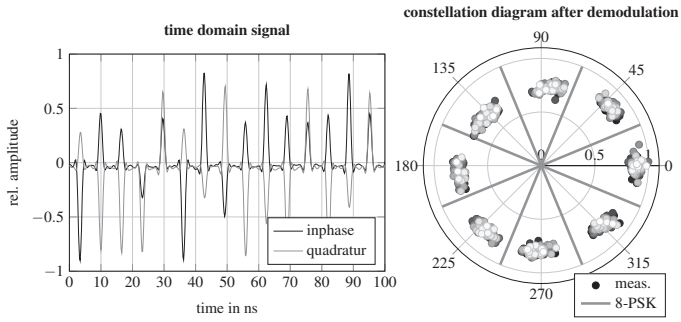

Figure 2.4
Transmission experiment results at 150 Mbaud and 8-PSK modulation (450 Mbit/s). From [67] © 2017 IEEE

2.2.4 Heterodyne System

High mm-wave frequency transmissions in the order of 180 GHz come with high geometric path loss and thus require either require highly directive antennas or short distances compared to lower frequency systems with the same transmit power. Therefore, efficient multi-channel/MIMO architectures are an attractive option to enable both multi-user capability as well as high directivity without the limitations of beamsteering. However, high power consumption and implementation size is even more critical for these systems since several transceivers must be integrated into a single system. Consequently, a modification of the aforementioned super-regenerative homodyne concept has been investigated, which is shown in Figure 2.5.

On the transmitter side, it is based on notably smaller units, each consisting of a simple BPSK modulator and an SRO as power amplifier. Two of these paths with 90° phase shift enable, e.g., QPSK modulation through signal combination over-the-air, which allows to abandon more complex modulator structures as well as lossy combining networks.

On the receiver side, two SROs are mixed in a dual sideband mixer with one SRO running at a frequency lower than the transmitted carrier signal and the other SRO running at a higher frequency. If they sample subsequent pulses and the delay is appropriately configured, an intermediate frequency (IF) signal is produced at the mixer's output, which is afterwards band pass filtered, amplified and converted to the digital domain using a very fast converter. With an IF of excactly one fourth of the ADC clock, signal processing for downconversion to complex baseband can be minimized (multiplexing and alternating sign inversion). This configuration saves large area I/Q-mixer structures required for the additional phase shift and signal distribution network.

The experimental verification of this concept is currently being carried out

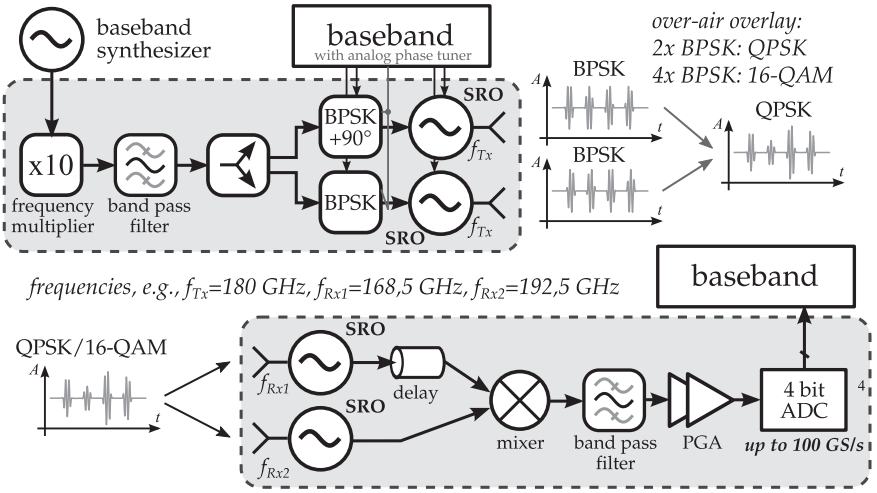

Figure 2.5
M-SPARS concept for an efficient multi-channel transceiver based on a heterodyne mixing approach. [64]

at a center frequency of 180 GHz in cooperation with TU Dresden. Since the second project phase is still ongoing, results are expected to be published in 2020 / 2021.

2.3 Transmitter Components

Fig. 2.1 shows the transmitter concept of the simultaneous phase and amplitude regenerative sampling system. An external signal source is used to generate the carrier signal. This has a frequency ten times lower than the desired frequency. The multiplication by ten of the signal is performed on-chip. The subsequent RF-DAC converts the digital baseband signal into an analog signal and simultaneously modulates the carrier with it. At the output of the transmitter a SRO is replacing a conventional power amplifier. When switched on, the SRO picks up the input signal at its current phase and repeatedly amplifises the signal through positive feedback with around 20 to 40 dB. Typical injection powers of SROs can be extremly low, which eases the design of the RF-AC in regard of output power. Before the phase gets out of sync or the amplitude reaches its compression level, the SRO has to be switched off.

2.3.1 Generation of the Carrier Frequency

The SPARS concept allows an energy-saving topology, because it does not require power-consuming PLL-based Synthesizers, as conventional systems does. For this approach, the required carrier signal can be derived from a VCO with a fundamental frequency, which is the sub-harmonic of the carrier signal. For this purpose, a frequency ten times lower than required is chosen. In this case (18 GHz). The reasons are that this frequency can be generated with lower power requirements and the phase noise is much lower in this frequency range for modern HBT transistors. Additionally, the phase noise can further decreased due the frequency multiplication, with the frequency multiplication factor N, by

$$\Delta_{PN} = 20 \cdot \log_{10}(\mathrm{N}) \tag{2.3}$$

For the realization of the SPARS demonstrator with 180 GHz carrier frequency, a multiplier with factor ten was chosen. It consists of two stages. The first stage is a frequency quintupler, which converts the input signal of 18 GHz to an output signal of 90 GHz. In a second step, the 90 GHz signal is doubled to the required 180 GHz by an frequency doubler.

2.3.1.1 Quintupler Stage

To realize a frequency quintupler, cascode differential amplifiers are used [69], which are loaded by narrow band transmission line filters. The schematic is depicted in Fig. 2.6. The resonance frequency of the filter is tuned to 90 GHz (five times the input frequency). The first stage represents the main quintupler with the narrow band transmission line filter consisting of TL1 - TL3.

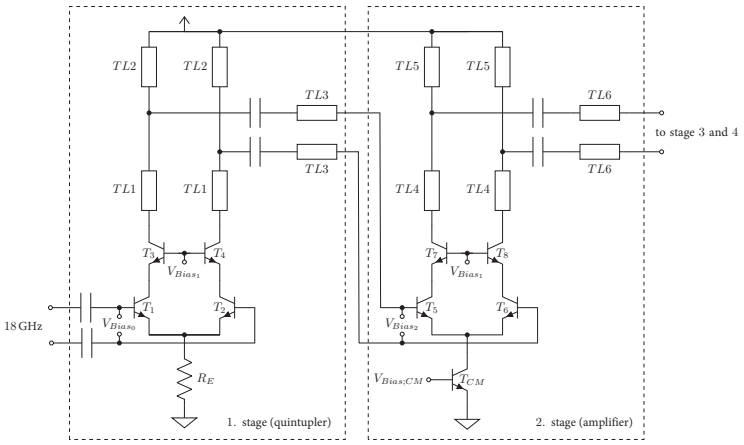

Figure 2.6
Four stage quintupler (stages 3 and 4 not shown).

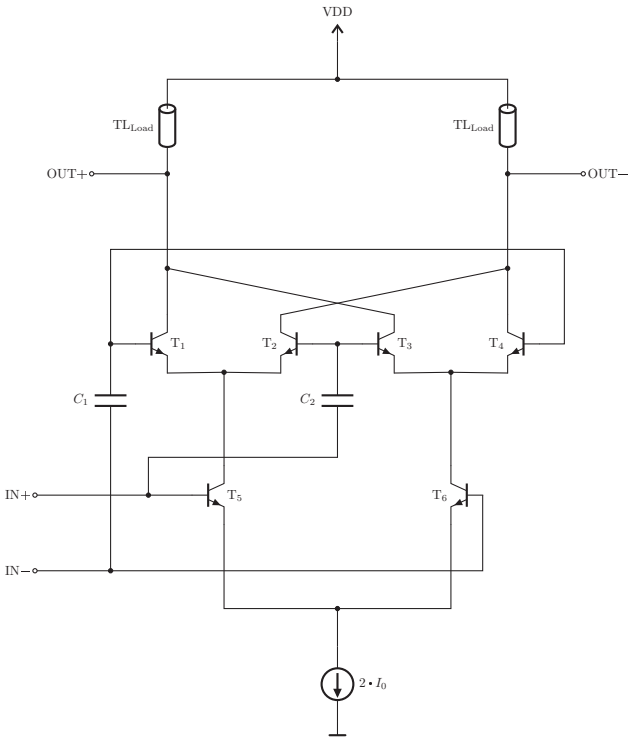

Figure 2.7
A conventional Gilbert-Cell doubler

Simulations show that the convertion loss at the fith harmonic is around -25 dB. To achieve optimum conversion efficiency of the Gilbert-Cell doubler, a power of 0 dBm at 90 GHz is required. Therefore three further amplifier stages (stage 2 - stage 4) are necessary. These amplifiers also have a cascode architecture. Since frequency multiplication inevitably results in additional harmonics in the spectrum, a narrowband load is used for the amplifier, which acts as a filter. The transmission lines TL4 - TL6 are used for this purpose.

2.3.1.2 Gilbert-Cell Multiplier

To double the 90 GHz signal to 180 GHz, a Gilbert-Cell doubler is used. The advantage of the Gilbert-Cell doubler compared to a push-push doubler is its differential output [70]. The Gilbert-Cell doubler is derived from a Gilbert-Cell by connecting the LO port of the switching quad transistors (T1 - T4) to the RF port of the transconductance stage (T5, T6) and feeding the same input signal. The schematic of a conventional Gilbert-Cell doubler is shown in Fig. 2.7. The drawback of this topology is that although a quadrature signal is applied to the LO and RF ports, no truly balanced output signal is generated.

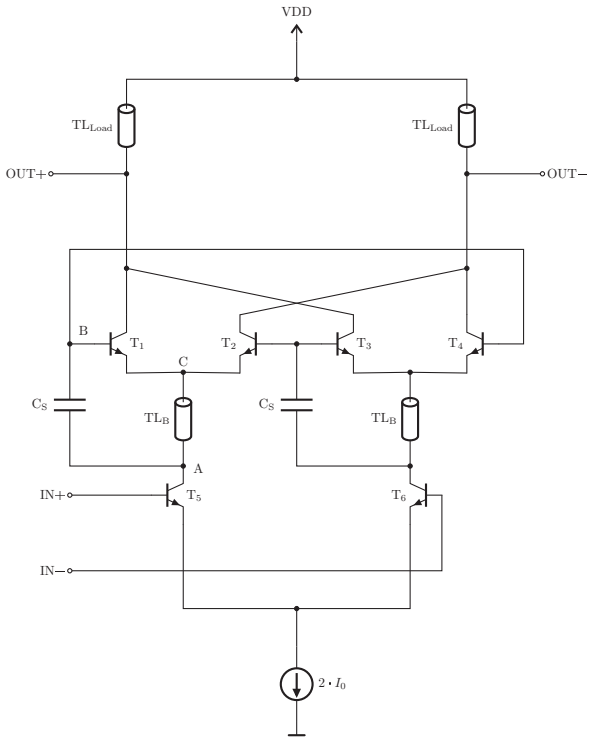

Figure 2.8
A Gilbert-Cell doubler with bootstrapping

Reasons for this are mainly a common mode LO feedtrough, which generates an unbalanced second harmonic output [71]. For the interested reader the derivation by Yuan et al. [71] is recommended.
To overcome this behavior, a modified so-called "bootstrapped" Gilbert-Cell doubler introduced by Yuan et al. [72] is used. The schematic of this modified Gilbert-Cell doubler is shown in Fig. 2.8. "Bootstrapping" is achieved by adding the capacitors C_S and the transmission lines TL_B compared to conventional Gilbert-Cell doublers. Now the switching transistors (T1 - T4) are driven by the differential pair (T5 and T6). Therefore a lower input power is required compared to conventional Gilbert-Cell doublers. A closer look at the schematic in Fig. 2.8 shows that the capacitors C_S act both as a DC blocker respectively as an RF short. The transmission lines TL_B are used as delay lines to create a phase difference between node A and C. So the potential V_C at node C can be written as the potential V_A at node A plus a phase shift θ:

$$V_C = \hat{V} \cdot \sin(\omega t + \theta) \tag{2.4}$$

$\hat{V}$ represents the amplitude of the potential at node A.
Assuming that the capacitors C_S represent an ideal RF short, the base-emitter voltage of the switching quad transistors can be described as follows:

$$V_{be} = V_B - V_C = V_A - V_C = \underbrace{2 \cdot \hat{V} \sin(-\frac{\theta}{2})}_{const.} \cdot \cos(\omega t + \frac{\theta}{2}). \tag{2.5}$$

Using equation 2.5, it will be seen that the amplitude of the base-emitter signal varies with the factor $2 \cdot \sin(-(\theta/2))$ depending on θ. This shows that by varying the length of the transmission line a phase difference of 90 ° is achievable, resulting in a better balanced output amplitude [72].
Figure 2.9 shows the measured output spectrum for different input frequencies of the Gilbert cell doubler used in this work. It can be seen that the output power of the doubler varies only about 6 dB over a bandwidth of 30 GHz.

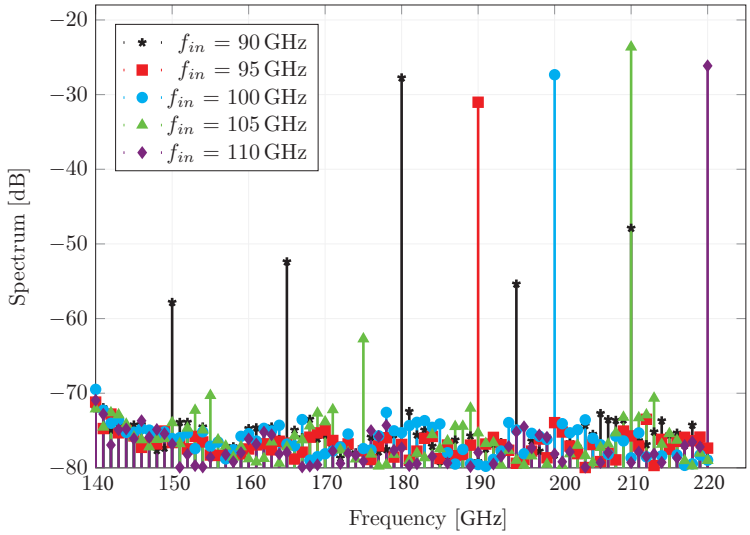

Figure 2.9
Output spectrum of the Gilbert-Cell doubler at different input signal frequencies (@ $P_{in} = -10$ dBm)

2.3.2 BPSK Modulators and RF-DACs

Communication systems are based on information transfer between transmitter and receiver. In digital communication systems, basically binary symbols have to be transferred into an analog domain, which can be send over the desired channel. In case of the described system, a Radio Frequency Digital-to-Analog-Converter (RF-DAC), based on Binary-Phase-Shift-Keying (BPSK)

modulators, is the key component for this task. An ideal BPSK signal, as depict in Fig. 2.10, consists of two symbols, realized by a phase shift of 180° of the carrier signal.

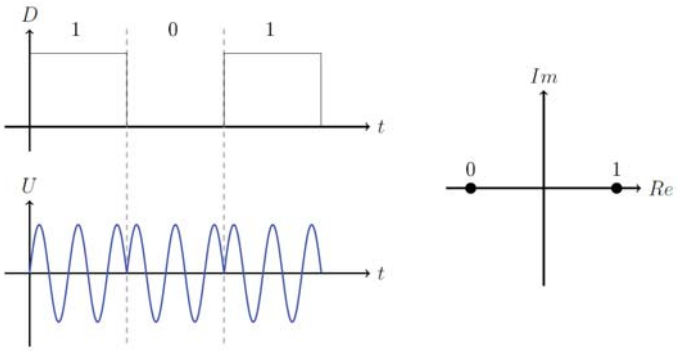

Figure 2.10
Idealized BPSK signal in time domain (left) and the corresponding constellation diagram (right).

The concept of radio-frequency DACs has been first proposed by [73] and has been implemented in various transmitter architectures since (see [74], [75]). A commonly used basis of RF-DACs are double-balanced Gilbert Cells. Here, the RF input is fed into the differential input pair and modulates the current source, while the digital data is fed to the switching squad. As shown in Fig. 2.11, the switching quad (2) steers the differential current flow thru the load (3).

Thus a binary phase shifted output signal is generated. Using more then one Gilbert cell with a differently (i.e. binary) weighted current in parallel, the resulting output signal consists of two amplitudes and two phases and thus creating a 2-bit cell. Putting several of those 2-bit cells in parallel and weighting the currents of each BPSK modulator accordingly, higher modulation rates are possible. In order to generate quadrature signals (for e.g. 16 QAM), two n-ary modulators with 90° phase shift have to be combined.

Fig. 2.12 shows the block diagram of the designed BPSK-Modulator. The RF input is converted to a differential signal first via a passive transmission line based $\lambda/4$ - $3\lambda/4$ - Balun (see [76]), before being fed into the BPSK modulator. The modulator (see fig. 2.13) is based on the classic double-balanced Gilbert Cell, which offers the best trade-off between conversion gain and switching speed.

The external data input is given into the LO-buffer, that is based on the Cherry Hooper amplifier [77] and serves several purposes. On the one hand it rectifies the sinusoidal data input and ensures a high and constant output swing regardless of the input power, so that the switching quad is driven optimally. On the other hand the amplifier has a pseudo-differential input at

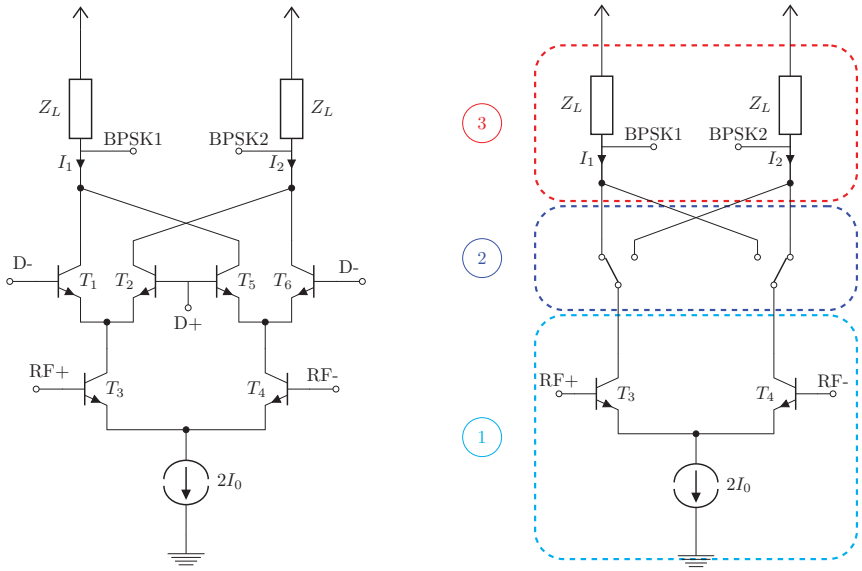

Figure 2.11
Idealized standard Gilbert cell (left) and its BPSK concept diagram (right)

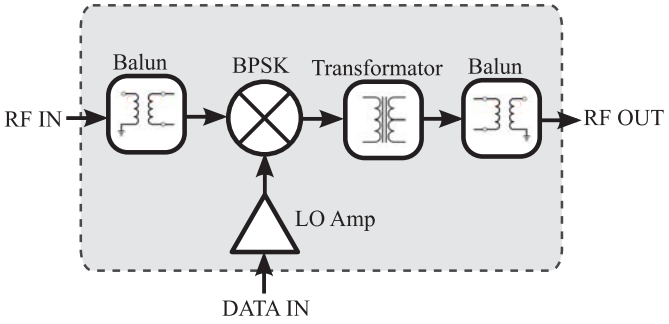

Figure 2.12
Block diagramm of the circuit

transistors T5 and T6. This has been implemented to circumvent the need of on chip balun and to fullfill measurement setup restictions.

The load of the modulator is realized by a 1:2 transformator, which decouples the BPSK modulator from the output pads, while also serving as supply voltage feed. Other advantages of a transformator load are increased linearity, common-mode isolation and filtering [75]. At the end, the signal is converted back to single-ended via a balun again.

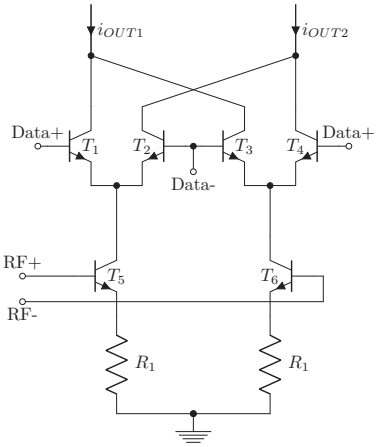

Figure 2.13
BPSK modulator as double-balanced Gilbert cell (biasing not shown)

Fig. 2.14 shows the resulting spectrum of modulation rates of 1 GHz and 6 GHz with a 180 GHz carrier frequency. The corresponding transient signal of the 6 GHz modulation is plotted in Fig. 2.16. The plots show a clean spectrum for both modulation frequencies as well as a clean phase shift. The output power averages a maximum of -35 dBm at a RF input power of approximately -17 dBm. Accounted for, are the conversion losses of the harmonic mixer in the test setup, but additional losses because of two waveguide bends, two probes and cables have not been included. Thus the expected output power of the chip has to be considered at around -20 dBm.

Fig. 2.15 shows a micrograph of the die, which was fabricated in IHPs 130nm BiCMOS technology.

2.3.3 Summary

For the SPARS concept, the transmitter with its key building blocks were shown, which were developed and designed to prove the SPARS concept at a carrier frequency of 180 GHz. An exception is the SRO. A tenfold multiplier was shown as first part of the carrier frequency generation for the SPARS transmitter. It consists of a quintupler stage followed by a doubler stage. Both together act as a frequency multiplier with factor ten. The input signal for the tenfold multiplier was generated with a external source, which contributes a 18 GHz driver signal. This concept is well suited for SPARS transmitters, because just a carrier frequency with less power is necessary for the SRO at the output of the transmitter. Furthermore, the weak carry signal relaxes also the requirements on the RFDACs in the transmitter chain. The RFDACs were also shown as a second key component of the SPARS concept.

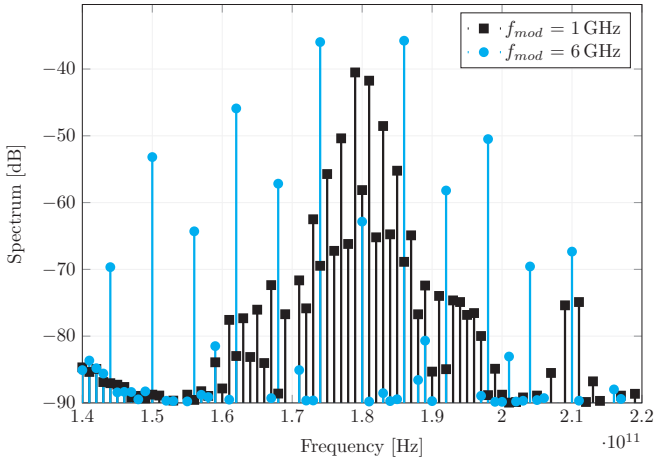

Figure 2.14
Spectrum of modulation rates of 1 GHz and 6 GHz with an RF input of 180 GHz

2.4 mm-Wave Frontend Components

2.4.1 180-GHz Super-Regenerative Oscillator with 58 dB Regenerative Gain

2.4.1.1 SRO Principles

The super-regenerative oscillator (SRO) circuit concept is presented in Figure 2.17. It is an oscillator circuit with an input port that is connected to the receive antenna, and employs a gain element with positive feedback. The signal is fed to the oscillator core and the phase and amplitude information is sampled at the turn-on instant, when the oscillator is most sensitive. The oscillation then grows exponentially to its steady-state level with the phase information preserved. To receive the following symbols, the oscillator has to be periodically quenched, thus each oscillation pulse represents one symbol. Depending on the quenching time T_{on}, the SRO circuit can have one of two modes of operation: linear mode or logarithmic mode, which are shown in Figure 2.18. If the oscillator is quenched before a steady-state is reached, there is a linear dependence between the input and output amplitudes [78], and the oscillator is said to be in linear mode. This is suitable for applications in which amplitude modulation is used. In case the oscillator amplitude is allowed to saturate, the amplitude information is lost, and the oscillator is in logarithmic mode. This mode is beneficial for phase modulation applications, as it leads to the highest regenerative gain. The possibility of simultaneous

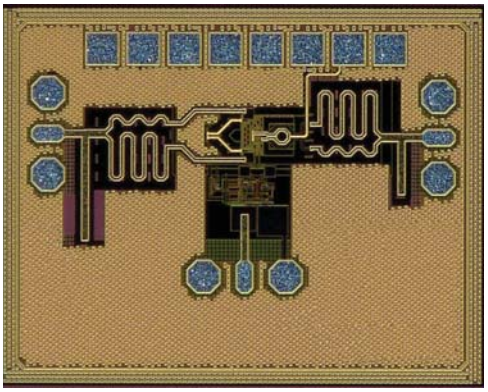

Figure 2.15
Chip foto of the fabricated BPSK modulator

phase and amplitude modulation in linear-mode SROs allows for their use with more complex modulation schemes, such as quadrature amplitude modulation (QAM), which leads to better spectral efficiency. [79, 80]

The advantages of this super-regenerative approach include low complexity, as well as high power and area efficiency, since one block can replace multiple gain stages in the receiver. Through pulsed operation by repeated quenching, the power consumption is further reduced. On the other hand, the high sensitivity of the super-regenerative circuit leads to susceptibility to interferers in adjacent channels. This limitation is, however, relieved by the large channel bandwidth in mm-wave bands, as well as the high propagation loss, which allows for frequency reuse after a short distance. Thus, typical use scenarios could include battery-powered point-to-point communication applications, in which very high energy efficiency is required.

2.4.1.2 Circuit Design

Figure 2.19 shows a schematic diagram of a proposed SRO circuit, which was found to be most suited for realization at 180 GHz. The oscillator core is realized with the transistors T_{1-4}, with the diode-connected transistor pair $T_{5,6}$ used as varactors for oscillation frequency tuning through the tuning voltage V_{tune}.

The core is based on the differential common-collector Colpitts topology, which has demonstrated superior performance at mm-wave frequencies [81]. A differential common-base output buffer consisting of transistors $T_{3,4}$ boosts

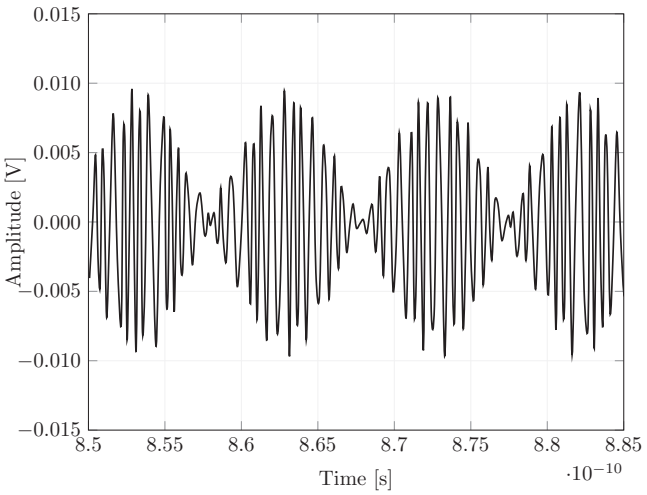

Figure 2.16
Measured transient signal of a 6 GHz BPSK modulated signal on a 180 GHz carrier

the output power delivered to the load, and ensures sufficient reverse isolation to prevent the locking of the oscillator to reflected pulses, in case of output impedance mismatch. The input transconductance stage consisting of transistors T_{7-10} acts as an active balun, injecting differential input currents into the oscillator. Additionally, it helps to provide a broadband match due to the small real part of the input impedance, which is transformed to 50 Ω by the short transmission line segment TL_{in} as well as the pad capacitance. A small inductor L_1 adjusts the phase balance between the two balun branches.

The diode-connected transistors $T_{11,12}$ form a current mirror with $T_{7,9,10}$, which allows the current biasing of the oscillator through I_{ref}. T_8 maintains the voltage common-mode balance between the two differential branches. By

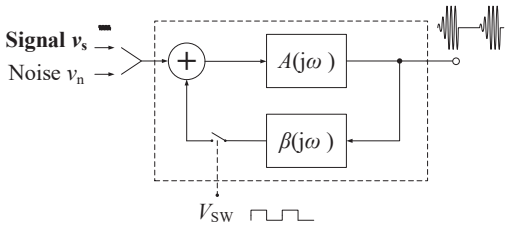

Figure 2.17
SRO operation principle based on positive feedback. From [80] © 2020 IEEE

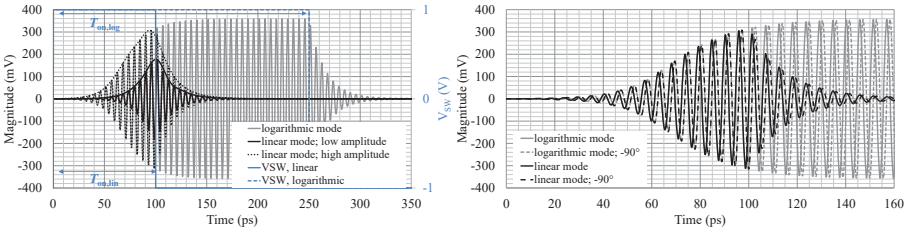

Figure 2.18
Numerical simulations for a 180-GHz SRO output with (a) amplitude modulation, and (b) phase modulation in linear and logarithmic modes. From [80] © 2020 IEEE

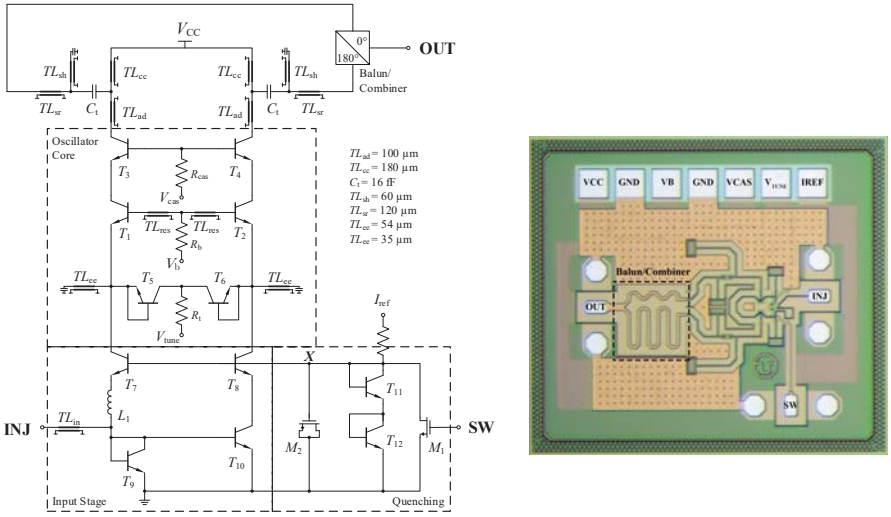

Figure 2.19
Schematic and micrograph of the 180-GHz SRO chip (area = 900 × 800 μm^2) From [79] © 2019 IEEE

adding the NMOS transistor M_1, a signal SW can be applied to periodically quench the oscillator as required, by sinking I_{ref} and pulling down the bias voltage node X. By adding capacitance to that node, the quenching slope of the oscillator at the turn-on instant can be slowed. This has been found to improve the SRO sensitivity in terms of the minimum input power required for low-BER phase recovery $P_{inj,min}$ [82, 83]. However, a large capacitance would limit the quench rate, thus reducing the achievable symbol rate. Therefore, an optimum value for the capacitance has been investigated and implemented with the NMOS capacitor M_2.

The supply voltage V_{CC} is provided through the feed lines TL_{cc}. The transmission lines TL_{ad}, TL_{sh} and TL_{sr}, as well as the capacitors C_t form an impedance transformation network at the output. The optimum load impedance was investigated by load-pull simulations, which used fast start-up rather than the highest output power as the optimization goal. From oscillator theory, the maximum amplitude is dependent on the real part of the tank admittance R_P. On the other hand, R_P also increases the RC time constant of the load, leading to a slower start-up. The reactive inductive part, therefore, has to be tuned to resonate with the capacitive part, leading to a fast start-up. Thus, a large R_P is required for a large swing, and a moderate inductance value L_P is required for a fast start-up.

All transmission lines were implemented as grounded coplanar waveguides (GCPW), and all bipolar transistors were sized at the emitter area $A_E = 2 \times 0.9 \times 0.07$ mm^2. The differential outputs are combined in a passive microstrip balun, which consists of one $\lambda/4$ and one $3\lambda/4$ transmission line segments, both with a characteristic impedance of 71 Ω. The balun also performs the function of impedance transformation of single-ended 50 Ω to differential 100 Ω [84].

2.4.1.3 Experimental Results

Figure 2.20 shows the measured oscillation frequency f_{osc} and the output power P_{out} as functions of V_{tune}, with both INJ and SW inputs terminated to 50 Ω. The frequency tuning range extends between 175.9–187.7 GHz, which amounts to 6.5%, or almost 12 GHz. The output power at 180 GHz is -2 dBm, whereas the maximum output power is 0.5 dBm.

With the capabilities of modern laboratory instrumentation at the time of writing, the time-domain characterization of SROs operating above 100 GHz was not possible. Thus, a common approach from previous work, which used a CW input signal of a known frequency f_{inj} and examined the spectrum was followed [58]. In case of phase coherence, the output spectrum is given by

$$V_{out}(f) = A_{out} D_{sw} \left| \mathrm{sinc}(\pi T_{on}(f - f_{osc})) \right| \sum_{n=-\infty}^{\infty} \delta\left((f - f_{inj}) - n f_{sw}\right) \quad (2.6)$$

where A_{out} is the output amplitude, D_{sw} is the duty cycle of the quench signal, and $T_{on} = D_{sw}/f_{sw}$ is the ON-state time before quenching. The spectrum

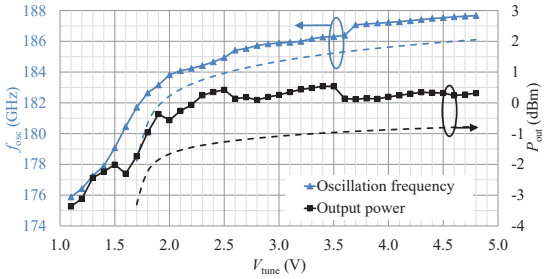

Figure 2.20
f_{osc} and P_{out} as functions of V_{tune} from measurements (solid) and simulations (dashed). From [79] © 2019 IEEE

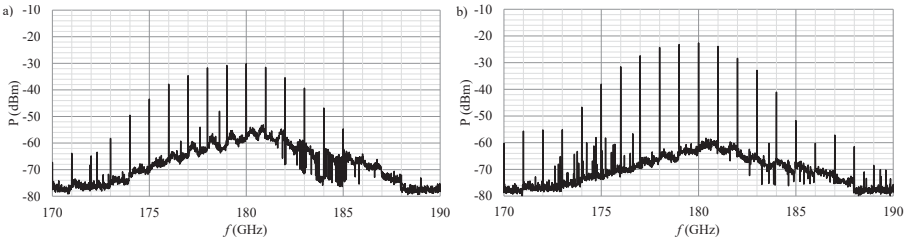

Figure 2.21
Measured SRO spectrum for f_{inj} = 180 GHz, f_{sw} = 1 GHz, and (a) P_{inj} = -58 dBm, (b) P_{inj} = -48 dBm. From [79] © 2019 IEEE

consists of a sequence of Dirac delta spectral peaks at $f_{inj} - nf_{sw}$, where n is an integer, superimposed by a sinc-shaped envelope centered around f_{osc}.

Figure 2.21 shows the SRO spectrum for an input CW signal at 180 GHz and a quench rate of 1 GHz. The duty cycle is set to approximately 30%, with a dc power consumption of 8.8 mW. In Figure 2.21 (a), phase coherence is observed for P_{inj} = -58 dBm with clear spectral lines. In Figure 2.21 (b), P_{inj} is increased by 10 dB, which leads to less sampling errors and improved phase coherence, which is observed as a slight reduction of the noise floor level. The amplitude also rises due to faster SRO start-up. In Figure 2.22, quench rates of (a) 5 GHz and (b) 10 GHz are shown, with input power P_{inj} = -26 dBm.

In order to demonstrate SRO regeneration of a modulated signal with high data rate (>1 Gbit/s), the setup depicted in Figure 2.23 has been employed. An n-PSK modulated signal is generated in complex baseband using a digital to analog converter and applied to a 15 GHz CW carrier using a quadrature mixer. Subsequently, the constant envelope signal is up-converted to 180 GHz with a network analyzer converter, which contains a frequency multiplier of factor 12. Thus, the baseband signal (blue) needed to be compressed in phase

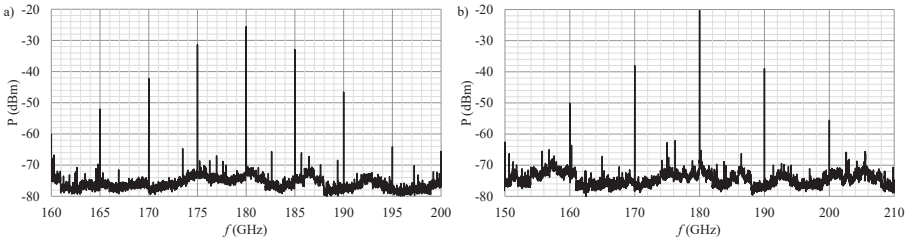

Figure 2.22
Measured SRO spectrum for f_{inj} = 180 GHz, P_{inj} = -26 dBm, and (a) f_{sw} = 5 GHz, (b) f_{sw} = 10 GHz. From [79] © 2019 IEEE

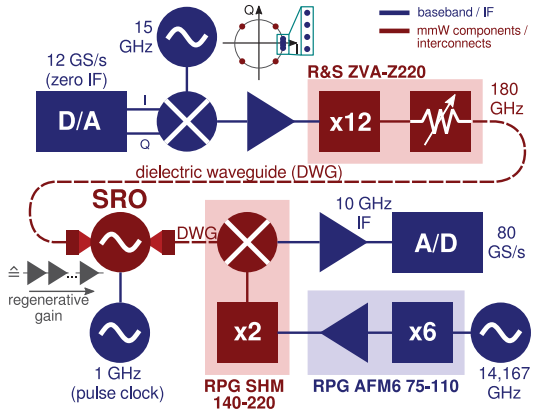

Figure 2.23
Measurement setup for demonstrating SRO-based regeneration of n-PSK modulated signals. From [79] © 2019 IEEE

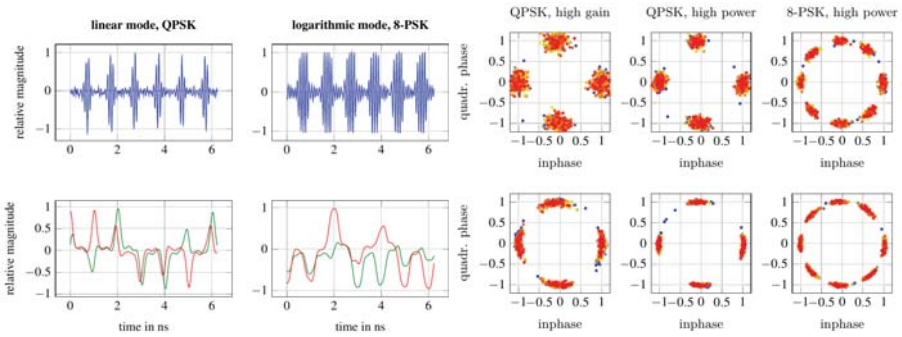

Figure 2.24
Measured IF and complex baseband signals in linear and logarithmic mode, and constellation diagram from measurements without SRO (top) and with SRO (bottom), for (A) QPSK with high gain (20 dB), (B) QPSK with medium gain (15 dB) and moderate compression, (C) 8-PSK with medium gain (15 dB). The color map indicates the order of reception. From [79] © 2019 IEEE

to be correctly mapped after multiplication (red; see top I/Q diagram in Figure 2.23 for an example with QPSK).

A subsequent attenuator is used to configure different input magnitudes for the SRO. The SRO itself is contacted with wafer probes and connected to the setup by dielectric waveguide cables (1 m, insertion loss ∼10 dB each). It samples the input communication signal at the center of each symbol and amplifies it repetitively through positive feedback until the desired gain has been reached and the oscillation is turned off. The SRO output signal with one pulse per symbol is down-converted to an intermediate frequency (IF) of 10 GHz.

For further processing, the intermediate frequency signal is amplified and digitized. Afterwards, a numerical computation software is used to remove the IF by mixing to complex baseband. Filtering is done by complex conjugate convolution with a pulse shaping filter, in addition to the detection of sampling position and phase offset through correlation with a 1k symbol preamble. Subsequently, 10k symbols are sampled and analyzed for BER and EVM. Communication signals with 180 GHz center frequency and 1 GBaud pulse rate, and modulations of QPSK (2 Gbit/s) and 8-PSK (3 Gbit/s) have been regenerated with a regenerative gain of up to ∼20 dB. This corresponds to a highly efficient 2.9 pJ/bit for 8-PSK.

Figure 2.24 shows the measured IF signal of the SRO output before and after down-conversion to complex baseband. Both linear amplification as well as high output power with compression can be achieved. Figure 2.24 also depicts the constellation diagrams before and after sampling the symbols with the SRO. They show very good phase linearity, even for high-order phase modulation. The dynamic range is sufficient for up to 20 dB gain with an EVM

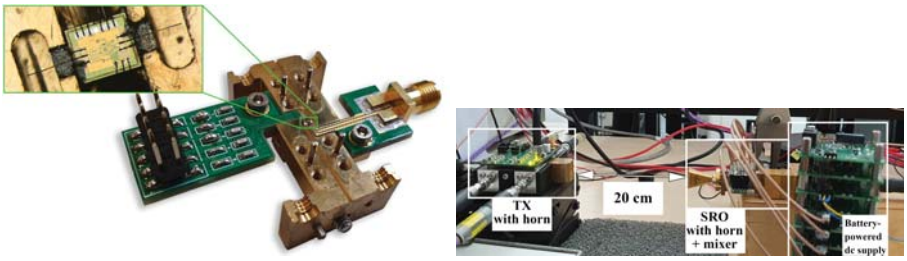

Figure 2.25
SRO waveguide module (lower part) with magnified chip transitions, and wireless link setup photo with labeled blocks. From [80] © 2020 IEEE

that is better than 16 dB. Since the gain can be easily controlled through pulse width over a wide range, gain can be traded off for EVM. This constitutes a notable advantage regarding complexity, system size and power consumption, especially at very high frequencies with very wideband signals since they can act as mm-wave variable gain amplifiers.

2.4.1.4 Waveguide Module and Wireless Data Transmission

To realize the regenerative gain capabilities of the SRO in practical use scenarios, it was beneficial to package the circuit into a standalone waveguide module, which achieves portability and flexibility of use. For this purpose, a mechanical construction that incorporates WR-5 waveguides for input and output was designed, and a brass prototype was manufactured. This bare module is shown as a split block in Figure 2.25 (only the lower half is shown). To couple the 180 GHz signals into and out of the chip, bondwires were used as E-field probes at the RF signal pads, as an alternative to expensive and impractical substrate probes [85]. The loss due to the waveguide packaging was found to be approximately 3 dB at 180 GHz.

A wireless link measurement was thus set up with waveguide horn antennas. A 180-GHz transmitter module with IQ inputs and an integrated antenna was used to mix up generated 16QAM symbols and transmit them over the air. On the receiver side, the SRO module was used to recover the symbols, followed by a subharmonic mixer to mix down the pulses. The data was then digitized and processed similarly to section 2.4.1.3. A photo of the setup is shown in Figure 2.25 for a link range of 20 cm. A custom-design battery-powered dc supply module was used in order to stabilize the SRO center frequency and eliminate the low-frequency supply noise that could degrade the SNR.

Figure 2.26 shows the measured QAM-modulated IF pulses and the result of their down-conversion to complex-baseband. The constellation diagram is also presented, and shows successful recovery of 16QAM data at 4 GBaud,

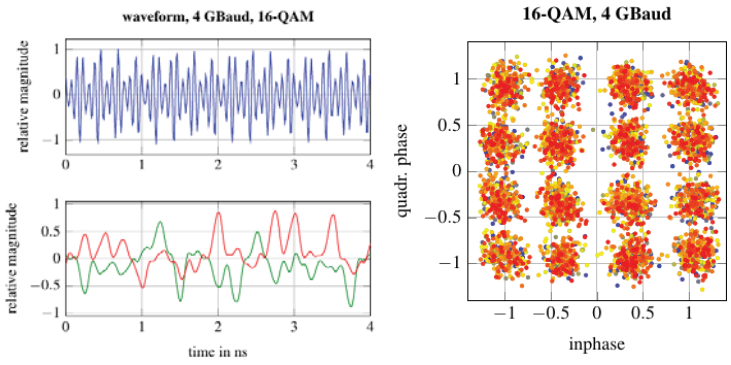

Figure 2.26
IF and complex baseband waveforms (left) and constellation diagram (right) for received 16QAM modulated pulses at 4 GBaud. The color map indicates the order of reception. EVM = -15.7 dB, BER = 8.5×10^{-3}. From [80] © 2020 IEEE

which corresponds to data transmission at 16 Gbit/s. This is the first demonstration of such high data-rate for a super-regenerative circuit.

2.4.2 180-GHz Down-Conversion Mixer with Broadband Rat-Race Coupler

2.4.2.1 Passive Mixer

With the goal of maximizing the efficiency of the receiver frontend, a passive mixer was preferred for frequency down-conversion, which would have close to zero dc power consumption. The conversion loss of the mixer could be tolerated due to the preceding high-gain SRO stage. The high linearity of passive architectures would also boost the dynamic range of the receiver. The design and layout of a passive integrated 180-GHz mixer in a 130nm SiGe BiCMOS technology, including a broadband rat-race coupler, is presented in the next section. . From [86] © 2019 IEEE

2.4.2.2 Circuit Design

Diode-connected heterojunction bipolar transistors (HBT) are very well suited for realizing passive mixers for high-frequency applications, thanks to their fast switching properties [87]. A single-balanced diode mixer consists of two diodes that are connected, with opposite orientations, to two mutually isolated ports of a 4-port hybrid. Their IF outputs are connected in parallel. The RF and LO signals are injected at the other two ports of the hybrid, which are also mutually isolated. Thus, such mixers typically have good LO-to-RF port isolation [88].

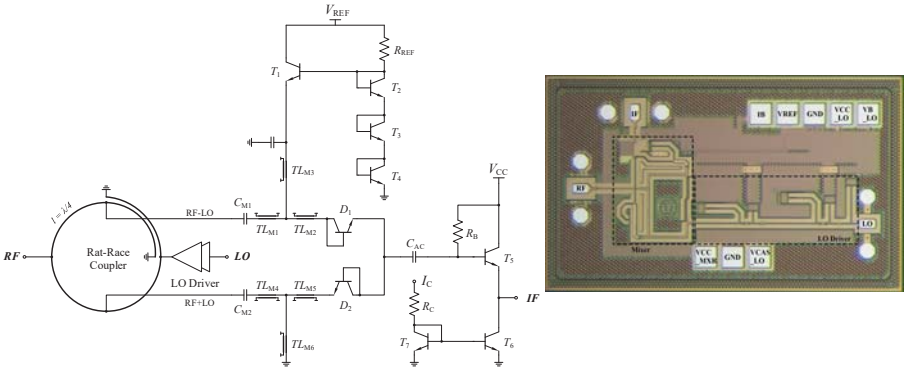

Figure 2.27
Schematic and micrograph of the 180-GHz mixer (area = 1240 × 710 μm^2). From [86] © 2019 IEEE

A schematic of the mixer is shown in Figure 2.27, which shows the hybrid implemented as an integrated rat-race coupler. The rat-race splits the RF signal with equal phases, and generates a differential LO signal between its mixer ports. The transmission lines TL_{M1-6} form the mixer matching network.

The IF currents due to the RF signal add at the diodes output, whereas LO noise currents are out of phase and cancel out. The IF port is single-ended, which is advantageous as it eliminates the need for bulky transformers at IF. A small dc bias current of 25 μA is provided by the network consisting of transistors T_{2-4} and is mirrored through the emitter-follower T_1 to the mixing diodes $D_{1,2}$. This dc current conditions the diodes in forward bias, thus reducing the LO power needed to drive the mixer. The mixer diodes are sized at the smallest emitter area of 0.9 × 0.07 μm^2 in order to reduce their junction capacitances, which in turn also reduces the conversion loss.

A common-collector buffer is designed at the IF port, which presents the mixer IF output with a high-impedance load. This allows trading off IF bandwidth for lower conversion loss, and helps achieve a broadband IF port match to 50 Ω. The buffer transistors are also sized at the smallest size to reduce their dc power consumption. Additionally, the buffer output impedance is thus close to 50 Ω, which facilitates the matching.

The LO signal power that can be generated in the lab is in the range of -20 dBm at the chip pads in the desired frequency range. Therefore, an LO driver [89] has been integrated to allow proper characterization of the mixer. This is, however, not desired in the receiver, as it would saturate the mixer and lead to the loss of SRO amplitude information. Thus, its power and area do not add to those of the receiver frontend.

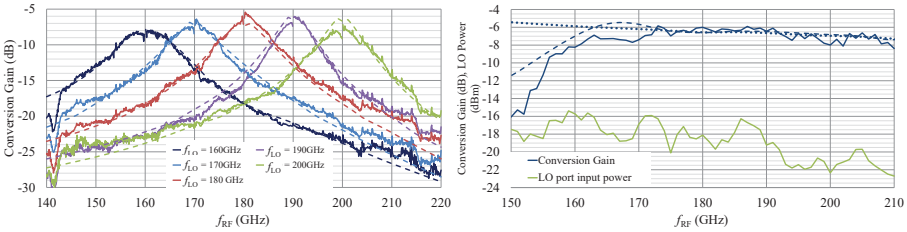

Figure 2.28
Measured (solid) and simulated (dashed) conversion gain against f_{RF} for multiple fixed f_{LO} (left), and for a fixed f_{IF} of 1 GHz (right), along with the the LO input power for the measurement. Simulation of the mixer conversion gain without LO driver is shown as a dotted line. From [86] © 2019 IEEE

2.4.2.3 Experimental Results

Figure 2.28 shows the measured and simulated down-conversion gain vs RF input frequency f_{RF}. The measurement is performed in 100 MHz steps for several constant LO frequencies f_{LO}. A minimum conversion loss of 6–8 dB is achieved over a wide frequency range between 160–200 GHz. It is worth noting that the frequency response towards lower frequency is masked by the LO driver bandwidth, which falls off below 170 GHz. The conversion gain is shown as a function of f_{RF} in 1 GHz steps for a fixed f_{IF} of 1 GHz. The measurement shows that the mixer exhibits a very large bandwidth of 50 GHz at the RF and LO ports. This is mainly due to the broadband rat-race design. Furthermore, it is also shown through simulation that the mixer, as a standalone module without LO driver, exhibits higher bandwidth exceeding 80 GHz.

The dependence of conversion gain on LO input power P_{LO} is shown in Figure 2.29 for an LO frequency f_{LO} of 180 GHz and f_{IF} of 5 GHz. The results for lower-side-band (LSB) and upper-side-band (USB) signals were observed to be almost identical. The conversion gain of the mixer is almost constant above -30 dBm, and does not fall at higher levels as simulated due to the saturation of the LO driver output, which is not considered in simulation. The LO input power at the chip pads is also shown for each measurement and shows a weak dependence of the conversion gain to the variations of LO power due to the incorporated LO amplifier. The linearity of the mixer as a function of RF input power P_{RF} is also presented in Figure 2.29 for f_{LO} = 180 GHz and $f_{IF} = 5$ GHz. The mixer shows high linearity, with an input-referred 1-dB compression point of -7 dBm.

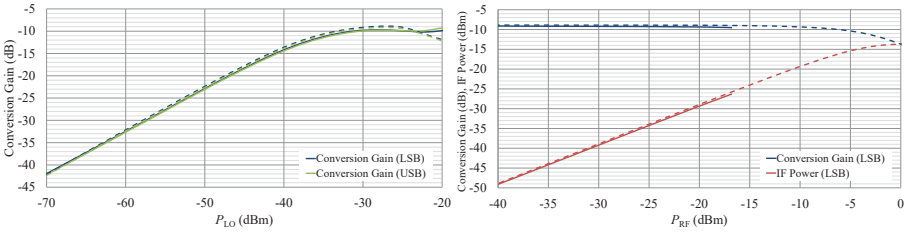

Figure 2.29
Measured (solid) and simulated (dashed) conversion gain against P_{LO} (left), and against P_{RF} (right), for $f_{LO} = 180$ GHz and $f_{IF} = 5$ GHz. . From [86] © 2019 IEEE

2.5 Analog Baseband Receiver Components

2.5.1 Indroduction

Classical homodyne I/Q receivers exploit quadrature mixers for the demodulation of the incoming radio frequency (RF) signal. These receivers require highly matched I/Q branches and exact quadrature phase shifts at all frequencies to prevent performance degradations by DC offsets, gain and quadrature-phase imbalances and carrier leakage.
In order to address these issues, the SPARS baseband receiver implements a direct I/Q sampling approach [90]. By employing an oversampling analog-to-digital converter (ADC), the I/Q components are extracted digitally from the converter data stream. The working principle of this demodulator is based on the incoming SRO RF output signal being mixed to an intermediate frequency (IF), band-pass filtered and subsequently sampled by 4 times the IF to extract the I/Q components in alternate 90° cycles from the ADC output data stream. As the digital I/Q demodulator only consists of one branch instead of two, it exhibits perfect gain, phase shift and offset matching between its I/Q components by design.
The implementation of the proposed homodyne receiver architecture in Fig. 2.1 necessitates a three-digit gigasample rate ADC with Nyquist performance. The design of such a fast converter presents a serious design challenge, as the speed performance of state-of-the-art mm-wave data converters has seemed to settle in recent years. The sampling rates of CMOS ADCs, for instance, have gone up to 90 GS/s [91]. Their bandwidths, however, have remained around 20 GHz since 2010 [91, 92, 93, 94] even though the used CMOS nodes in these ADC designs have improved from 40 nm to 14 nm since then. Just recently a 56 GS/s 8 bit time-interleaved successive approximation register (SAR) ADC in 28 nm CMOS [95] with 31,5 GHz bandwidth has been reported. The bandwidth enhancement has been realized by incorporation of advanced peaking

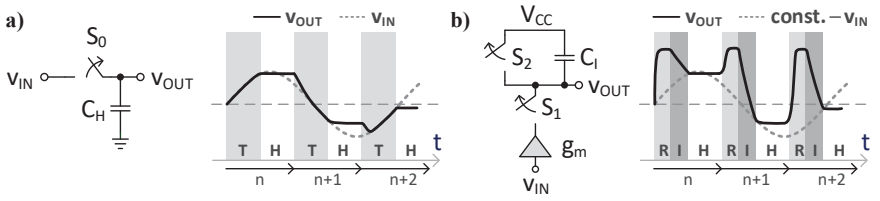

Figure 2.30
a) Voltage-mode sampler with Track (T) and Hold (H) phases. b) Charge sampler with Reset (R), Integration (I) and Hold (H) phases. From [96] © 2019 IEEE

techniques. Nevertheless, these recent advancements are still not sufficient to fulfill the speed requirements of this (and future) application(s). Thus, the development of new circuit concepts is inevitable.
An attractive solution to enhance the sample rate and the bandwidth of current state-of-the-art CMOS ADCs is the use of ultra-broadband analog demultiplexers. These circuits deinterleave the input signal to m branches. Subsequent data conversion of each branch signal then can be performed at 1/m lower sampling rate and 1/m lower bandwidth.
In this chapter the circuit idea, the implementation and the characterization of a proposed 112 GS/s charge-sampling ADC frontend in IHP 130 nm SiGe BiCMOS with 1-to-4 analog demultiplexing functionality [96] is presented. The circuit is demonstrated in real transmission experiments with 100 GBaud four-level pulse-amplitude-modulated (PAM4) test data [97]. The ASIC can be combined with commercial available mm-wave CMOS ADCs as a hybrid solution; alternatively it can be fully integrated with moderate or low resolution ADCs in the same technology. For later option, we present the design of a traveling-wave 40 GS/s 4 bit SiGe BiCMOS flash ADC based on a single-core architecture without track-and-hold circuit [98, 99]. Up to today, this ADC exhibits the highest reported sample rate for application-oriented single-core ADC designs.

2.5.2 A 112 GS/s 1-to-4 ADC frontend

2.5.2.1 Voltage versus charge sampling

Emerging Rx sampling circuits with three-digit gigasample rates exploit voltage-mode sampling architectures [100, 101, 102]. The sampling of the input signal in these architectures is realized by a hold capacitor and a switch that is instantenously triggered by either the rising or falling clock edge (see Fig. 2.30 a)). If the switch is closed, the circuit is transparent and the output tracks the input signal. During this phase, the hold capacitor is charged to the input voltage. If the next clock transition occurs, the switch is opened and

the output voltage ideally equals the voltage that is stored on the capacitor. For low-frequency input signals, this sampling technique exhibits excellent robustness against clock jitter. For high-frequency input signals, however, this sampling architecture can cause strong SNR degradations, as small time deviations in the clock transition can already result in large sampling errors. As shown in literature, e.g. [103], the SNR decreases linearly inversed with the input frequency f and the root-mean-squared clock jitter t_j:

$$SNR_{\mathrm{VS}} = \left(\frac{1}{2\pi f t_j}\right)^2. \tag{2.7}$$

To mitigate this dependency, a charge sampling architecture is used. By acquiring the output samples through current integration over a fixed time interval T_I, the SNR can be improved by up to 3 dB for the same rms clock jitter, if the input frequency exceeds $f \geqslant (4T_I)^{-1}$ [96]:

$$SNR_{\mathrm{CS}} = \left(\frac{1-\cos(2\pi f T_I)}{2\pi f t_j}\right)^2. \tag{2.8}$$

A simplified schematic of a single-core charge sampler together with its fundamental operation principle is depicted in Fig. 2.30 b). A linear transconductance amplifier converts the input voltage first into an equivalent input current. The input current charges the integration capacitor C_I and then the stored charge information is sampled. The acquisition of a sample is thereby achieved in three consecutive phases:
1. Reset (R): At the beginning of the sampling phase a discharge of the integration capacitor C_I is performed by closing S2. The discharge removes the charge information of the previous sample and sets the initial condition for the following integration. The capacitor voltage decreases and as a result the output voltage increases towards the positive power supply VCC.
2. Integration (I): After the output voltage has sufficiently settled, S2 is opened and at the same time S1 is closed. The input current charges C_I and the capacitor voltage increases.
3. Hold (H): The hold sample value is obtained by decoupling the integration capacitor. By opening S1 and S2 no discharging currents can flow and the output voltage is held constant.
The reset (R) and integration (I) phase acquire a quarter of the overall sampling period each while the remaining time is used for the hold phase (H). The acquisition of the next sample is performed in the same way: C_I is first reset, then integrated and finally isolated to obtain the hold sample value.

2.5.2.2 Circuit design

By combining four of these charge samplers with an analog current demultiplexer (see Fig. 2.31), a time-interleaved configuration can be realized. The analog demultiplexer is implemented as a two-stage hierarchical switch tree

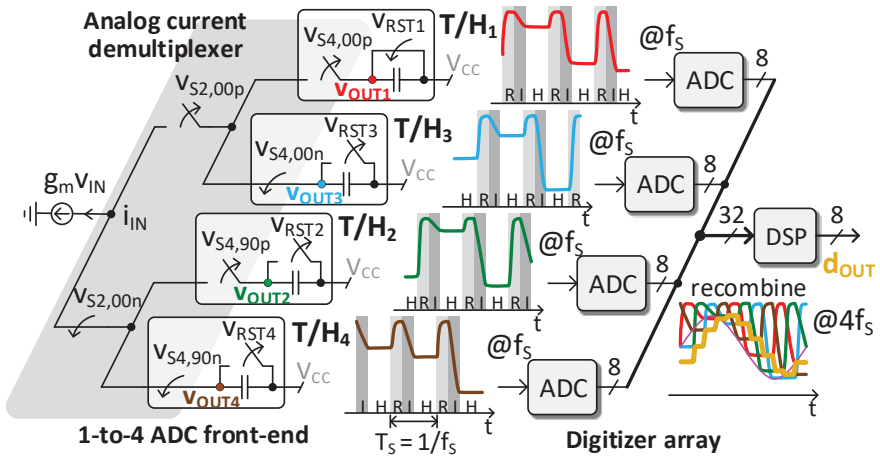

Figure 2.31
Time-interleaved 1-to-4 ADC frontend with illustrated output waveforms for a sinusoidal input signal. From [96] © 2019 IEEE

that is controlled by a differential half data rate clock ($v_{S2,00}$) and two differential quadrature quarter data rate clocks ($v_{S4,00}, v_{S4,90}$). The first switching level of the demultiplexer controls the steering of the input current to either the uneven (v_{OUT1}, v_{OUT3}) or even-numbered outputs (v_{OUT2}, v_{OUT4}). The second switching level then further refines the steering of the input signal to a single output (e.g. v_{OUT1}). Subsequent reset (R), integration (I) and hold (H) operations at each output then effectively provide samples at fourth times the channel sample rate (i.e. 4 x 28 GS/s). If all four ADC frontend output signals are digitized by following sub-ADCs, a complete reconstructed version of the input signal can be obtained by data interleaving (see orange waveform in 2.31 for a sinusoidal input signal).
The schematic core implementation of the 1-to-4 ADC frontend is shown in Fig. 2.32. The linear transconductance stage is realized by an emitter-degenerated differential pair (I). A hierarchical two-level current mode logic tree is used to implement the analog current demultiplexer (II). The first stage of the current demultiplexer is controlled by a half data rate clock ($v_{S2,00}$) and the second stage by two quadrature quarter data rate clocks ($v_{S4,00}$ and $v_{S4,90}$) that are derived by on-chip frequency divide-by-2 operations of the regenerated input clock. To improve the settling of the reset phase, the DC operation point of the demultiplexer's input current is reduced by two matched PMOS current sources (III). As less DC current is integrated on the integration capacitors, lesser charges have to be reset by the four switched emitter follower switches (IV). The control of these switches is achieved by four quadrature reset signals ($v_{RST1}, v_{RST2}, v_{RST3}$ and v_{RST4}) with 25% duty cycles each. On-

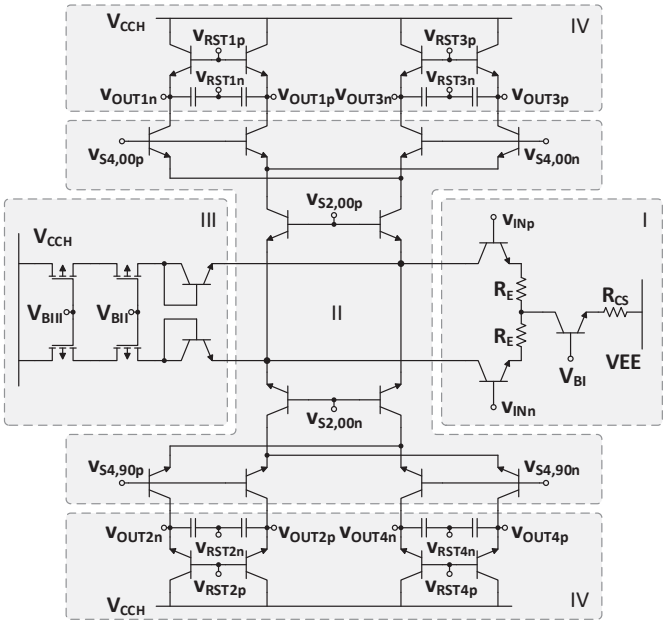

Figure 2.32
Schematic of the 1-to-4 ADC frontend core circuit. From [96] © 2019 IEEE

chip logic operations of the two divide-by-2 clocks ($v_{\mathrm{S},00}$ and $v_{\mathrm{S4},90}$) are used to generate these control signals.

2.5.2.3 Experimental results

The ADC front-end is implemented in IHP 130 nm SiGe BiCMOS and consumes a die area of 1.5 mm x 1 mm (see Fig. 2.33 a)). The technology (SG13G2) supports 300 GHz f_T and 450 GHz $f_{\max}$ for its HBTs and seven metal layers for routing. The chip is wire-bonded on a Rogers 3006 RF printed circuit. Fig. 2.33 b) depicts the dynamic range performance of the chip module at an effective sampling rate of 112 GS/s. Up to input frequencies of 43 GHz (frequency limit of used sine wave generator), a spurious-free dynamic range (SFDR) of more than 35-dBc and a signal-to-noise-and-distortion ratio (SNDR) of more than 28-dB are achieved for each channel [96].

2.5.3 A 40 GS/s 4 bit Flash ADC

2.5.3.1 "Traveling-wave" architecture

To enable the data digitization of the analog ADC frontend outputs, a mm-wave flash ADC with four bit nominal resolution is designed. The proposed ADC architecture is introduced in [98, 99] and is shown in Fig. 2.34 a). The

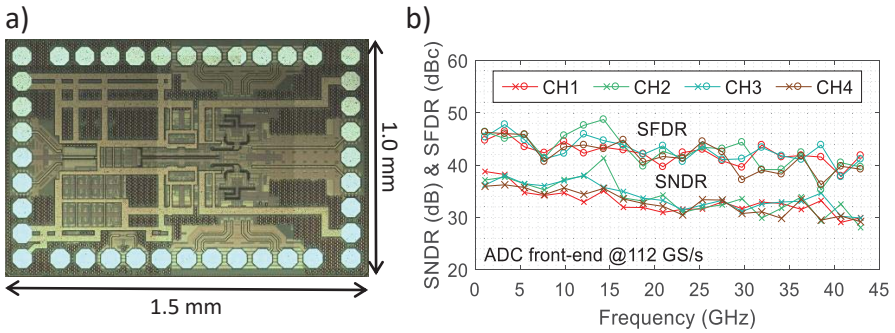

Figure 2.33
a) ADC front-end die photograph and b) measured SFDR and SNDR. From [96] © 2019 IEEE

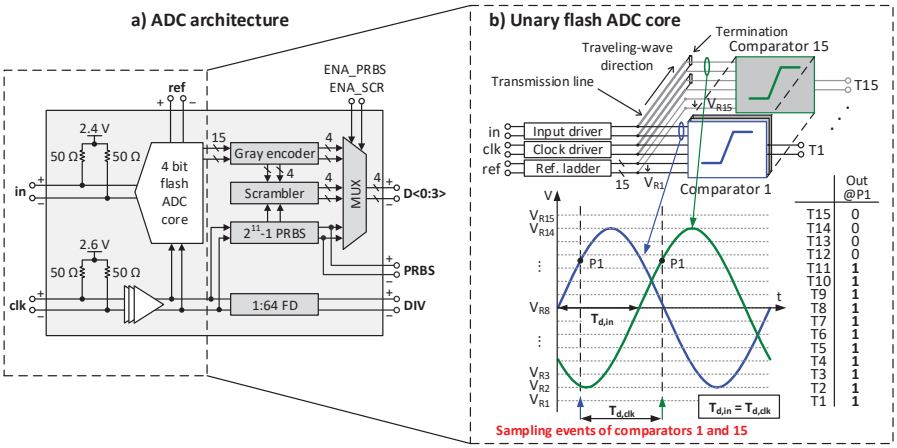

Figure 2.34
a) Flash ADC block diagram and b) signal distribution concept. From [99] © 2017 IEEE

main building blocks are a unary flash ADC core and a bubble-error suppressing gray encoder. To reduce the chip area, the power and especially the circuit complexity, no front-end track-and-hold amplifier (THA) is used. The increased data-to-clock skew requirement is addressed by exploiting a traveling-wave topology [104, 105, 99], where analog input and clock signal travel synchronously from comparator to comparator.
Fig. 2.34 b) exemplarily illustrates the signal distribution concept. A linear input driver feeds the analog input signal with help of a transmission line (TL) to a bank of parallel comparators. A high-gain clock driver equivalently does this for the clock signal. Due to the spatial location of the comparators the input and the clock signal do not arrive instantaneously at the same time at all comparators, but rather successively with small time delays. The idea exploited in traveling-wave ADCs is to keep the delays of the input and the clock signal equal between adjacent comparators. This ensures that every comparator quantizes the same input signal value at each sampling event, as illustrated in Fig. 2.34 b). Even though the comparators operate asynchronously due to the clock delays, the same results can be obtained as with flash signal distribution approaches, where input and clock signals arrive instantaneously at all comparators (e.g., with active input and clock distribution trees [106, 107]). However, since only two transmission lines are required - one for the input and one for the clock - the traveling-wave concept significantly consumes less area and has lower circuit complexity. The flash core performs a quantization of the analog input signal and delivers 15 unary coded digital output signals. For reduction of these signals, Gray encoding is performed. To enable the digital signal processing of the ADC data on an external field programmable gate array (FPGA), the ADC integrates a special designed multi-gigabit communication interface consisting of of a scrambler, a $2^{11} - 1$ pseudo random bit sequence (PRBS) generator, a 1:64 frequency divider (FD) and multiplexer (MUX). The operation modes of the integrated digital communication interface are explained in [108] are omitted in this section.

2.5.3.2 Circuit design

The flash ADC core is implemented fully-differentially in current-mode logic. For optimum circuit area utilization and to decrease the distance that the input and the clock signal have to travel along the transmission lines, the comparators are positioned in a U shape. Fig. 2.35 a) depicts the block diagram of the proposed traveling-wave flash ADC. The transmission lines are realized by microstrip transmission lines with 70Ω characteristic impedances each. The termination of the transmission lines is achieved by the load resistors of the differential input stages that are also used for I/U conversion of the input currents.
For the design of the comparators a Cherry-Hooper preamplifier with a cascaded master-slave Flip-Flop (MS-FF) is implemented. The schematic of the comparator preamplifiers is depicted in Fig. 2.35 b). By using negative feed-

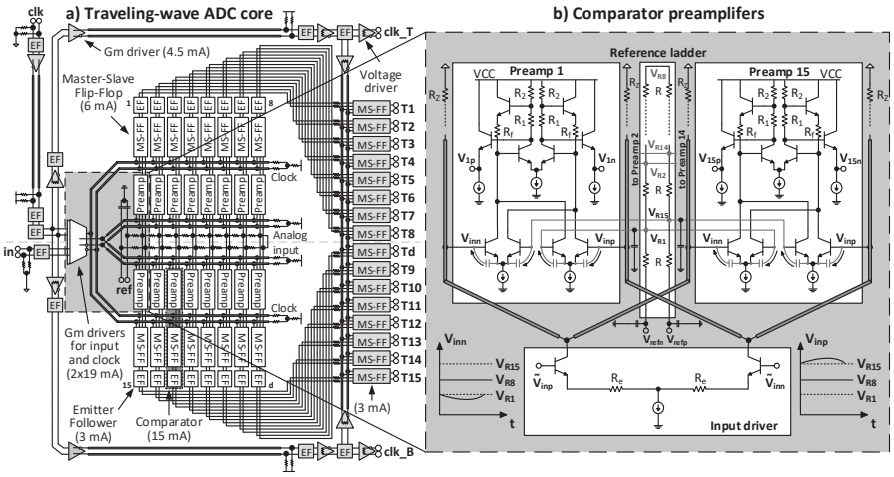

Figure 2.35
a) Traveling-wave flash architecture and b) schematic of comparator preamplifiers with integrated signal feedthrough compensation. From [99] © 2017 IEEE

back, a simulated gain of about 14 dB and a small-signal 3-dB bandwidth of about 63 GHz is achieved. The preamplifiers integrate a built-in signal feed-through compensation to stabilize the reference voltages of the resistor ladder. For high-input frequencies, the base-emitter capacitances of the differential input pairs form low-impedance paths from the input driver to the resistor ladder taps. As each reference voltage is compared against the negative and the positive input voltage, their signal feedthrough is compensated by first order.

2.5.3.3 Experimental results

The ADC RF board, die photograph, and measured effective number of bits (ENOB) are shown in Fig. 2.36 a), b) and c), respectively. The ADC dissipates 3.5 W while operating from a 3.5 V and 3 V power supply. The unary ADC core consumes 1.4 W and the encoder with the FPGA interface 2.1 W. Up to 39.04 GS/s the ADC provides an ENOB of more than 3 bits over the complete frequency band from DC to 20 GHz. The frequency band for an effective resolution better than 3 bits is 12 GHz at 40.32 GS/s and about 5.3 GHz at 42.24 GS/s.

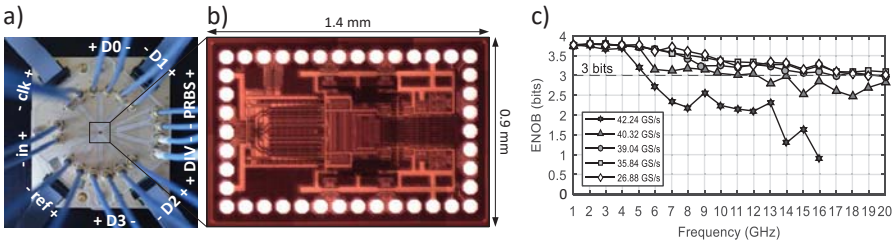

Figure 2.36
a) ADC on RF PCB, b) die photograph and c) measured ENOB. From [99]