

# Investigation of PSSS technologies to achieve 100 Gbps and beyond

Von der Fakultät 1 -MINT - Mathematik, Informatik, Physik,  
Elektro- und Informationstechnik

der Brandenburgischen Technischen Universität Cottbus-Senftenberg

genehmigte Dissertation

zur Erlangung des akademischen Grades eines

„Doktor der Ingenieurwissenschaften“

(Dr. -Ing.)

vorgelegt von

M.Sc.

Karthik Krishnegowda

geboren am 14. Januar 1988 in Bangalore, Indien

Vorsitzender: Prof. Dr.-Ing. Peter Langendörfer

Gutachter : Prof. Dr.-Ing. Rolf Kraemer

Gutachter : Prof. Dr.-Ing. Christoph Scheytt

Gutachter : Prof. Dr.-Ing. habil. Michael Hübner

Tag der mündlichen Prüfung: 11.06.2020



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# Abstract

The requirement for wireless communication with a speed beyond 100 Gbps is growing. There are mainly two possible approaches to achieve 100 Gbps system. One approach is to target lower transmission bandwidth and very high spectral efficiency. This method requires advanced digital signal processing operations, which are power-hungry. Another possible path is to go for a high-transmission bandwidth and a moderate spectral efficiency. We decided for this direction to implement a 100 Gbps system. We have chosen parallel sequence spread spectrum (PSSS) as an analog-friendly mixed-signal modulation where most of the baseband processing is in the analog domain, and only a small part is in the digital domain. For the channel equalization, we consider an “effective channel” that takes into account the wireless channel and the effects of the transmitter and receiver hardware impairments. The influence of the nonlinear channel response was analyzed for a PSSS modulated signal by employing the RAPP model for the power amplifier.

For the first time, we performed a Hardware-In-The-loop experiment using PSSS modulation in the terahertz band. A PSSS modulated signal at a chip rate of 20 Gcps with spectral efficiency of 4 bit/s/Hz is transmitted using a 230 GHz RF-frontend operating in the linear range to achieve a data rate of 80 Gbps. One more important property is that the channel estimation and equalization are performed in the analog domain. A high-speed channel equalization algorithm was developed and implemented on FPGA/ASIC, which operates at  $(\frac{1}{10})^{th}$  of PSSS symbol rate. A parallel PSSS encoder transmitter architecture was designed to work at a high chip rate, and it was implemented on FPGA/ASIC and had an energy efficiency of 0.21 pJ bit<sup>-1</sup> on 28 nm ASIC.

In this Thesis, we put forward a case for the analog-friendly modulation scheme called PSSS. This scheme does not only modulates the signal but rather builds up an eco-system (such as channel estimation, equalization, and synchronization), which is responsible for the baseband operation.

# Zusammenfassung

Der Bedarf an drahtlosen Kommunikationssystemen mit einer Übertragungsgeschwindigkeit von 100 Gbps und mehr wächst stetig an. Es gibt zwei mögliche Ansätze, um ein 100-Gbit/s-System zu erreichen. Ein Ansatz besteht darin, eine geringere Übertragungsbandbreite und eine sehr hohe spektrale Effizienz anzustreben. Dieses Verfahren erfordert fortschrittliche digitale Signalverarbeitungsvorgänge, die energieintensiv sind. Ein weiterer möglicher Weg ist die Wahl einer hohen Übertragungsbandbreite und einer moderaten spektralen Effizienz. Wir haben uns für diese Richtung entschieden, um ein 100 Gbps-System zu implementieren. Wir haben Parallel Sequence Spread Spectrum (PSSS) als analog-freundliche Mixed-Signal-Modulation gewählt, bei der sich der Großteil der Basisbandverarbeitung im analogen Bereich und nur ein kleiner Teil im digitalen Bereich befindet. Für die Kanalverzerrung betrachten wir einen "effektiven Kanal", der den drahtlosen Kanal und die Auswirkungen der Hardwarebeeinträchtigungen von Sender und Empfänger berücksichtigt. Der Einfluss der nichtlinearen Kanalantwort wurde für ein PSSS-moduliertes Signal analysiert, indem das RAPP-Modell verwendet wurde, das den Leistungsverstärker modelliert.

Zum ersten Mal haben wir ein Hardware-In-The-Loop-Experiment mit PSSS-Modulation im Terahertz-Bereich durchgeführt. Ein PSSS-moduliertes Signal mit einer Chiprate von 20 Gcps und einer spektralen Effizienz von 4 bit/s/Hz wird mit einem 230 GHz RF-Frontend übertragen, das im linearen Bereich arbeitet, um eine Datenrate von 80 Gbps zu erreichen. Eine weitere wichtige Eigenschaft ist, dass die Kanalschätzung und -entzerrung im analogen Bereich durchgeführt wird. Ein besonders schneller Algorithmus zur Kanalentsprechung, der mit  $(\frac{1}{10})^{th}$  der PSSS-Symbolrate arbeitet, wurde entwickelt und auf FPGA/ASIC implementiert. Eine parallele PSSS-Encoder-Senderarchitektur wurde entwickelt, um mit hoher Chiprate zu arbeiten, und sie wurde auf FPGA /ASIC implementiert und hatte eine Energieeffizienz von  $0.21 \text{ pJ bit}^{-1}$  auf 28 nm ASIC.

In dieser Arbeit stellen wir ein Modulationsschema namens PSSS als Beispiel für analog-freundliche Signalverarbeitung vor. Dieses Schema moduliert nicht nur das Signal, sondern ist umgeben von einem Ökosystem (z.B. Kanalschätzung, Entzerrung und Synchronisation), das für den Basisbandbetrieb verantwortlich ist.

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# Acronyms

**ACO-OFDM** Asymmetrically- Clipped Optical Orthogonal Frequency Division Modulation.

**ADC** Analog-to-Digital Converter.

**AGC** Automatic gain control.

**ASP** Analog Signal Processing.

**AWG** Arbitrary Waveform Generator.

**AWGN** additive white Gaussian noise.

**BCI** Wireless Brain-Computer Interactions.

**BER** Bit Error Rate.

**CAP** carrierless amplitude phase.

**CCW** counterclockwise rotation.

**CDC** Channel Deconvolution.

**CDMA** Code Division Multiple Access.

**CFO** Carrier Frequency Offset.

**CMOS** Complementary Metal-Oxide-Semiconductor.

**CO** Central Office.

**CRT** Chinese Remainder Theorem.

**CSK** Color Shift Keying.

**CTLE** continuous-time linear equalizers.

**DA** Data-aided.

**DAC** Digital-to-Analog Converter.

**DCMA** Dispersion Code Multiple Access.

**DCO-OFDM** DC-biased Optical Orthogonal Frequency Division Modulation.

**DD** Decision-directed.

**DDS** Direct Digital Synthesis.

**DFE** Decision Feedback Equalizer.

**DFG** Deutsche Forschungsgemeinschaft.

**DFT** Discrete Fourier Transform.

**DLL** Data Link Layer.

**DSA** Dynamic Signal Analyzer.

**DSB-SC** double side-band suppressed carrier.

**DSP** Digital Signal Processing.

**DSSS** Direct Sequence Spread Spectrum.

**EB** exabytes.

$E_b/N_0$  energy per bit to noise power spectral density ratio.

**EHF** Extremely High Frequency.

**EM** electromagnetic.

**E-O** Electro-Optical.

**ETSI** European Telecommunication Standards Institute.

**expt. 1** Experiment 1.

**expt. 2** Experiment 2.

**FA** Front Access.

**FDE** Frequency-domain equalization.

**FEC** forward error correction.

**FF** Flip Flops.

**FFT** Fast Fourier Transform.

**FIR** Finite impulse response.

**FPGA** Field Programmable Gate Array.

**FSO** Free-space optical communication.

**GaN** gallium-nitride.

**GEO** Geostationary Earth Orbit.

**HAP** high altitude platforms.

**HG** Hermite–Gaussian.

**HIL** Hardware-in-the-Loop.

**IDC** Integrate and Dump Correlator.

**IDFT** Inverse Discrete Fourier Transform.

**IF** intermediate frequency.

**IIR** Infinite Impulse Response.

**InP** indium-phosphide.

**ISI** Inter-Symbol Interference.

**ITRS** International Technology Roadmap for Semiconductors.

**ITU** International Telecommunication Union.

**KPI** Key-Performance-Indicator.

**LED** Light-Emitting Diode.

**LEF** Library Exchange Format.

**LEO** Low-Earth Orbit.

**LFSR** linear-feedback shift register.

**LG** Laguerre–Gaussian.

**Li-Fi** Light Fidelity.

**LNA** Low Noise Amplifier.

**LO** local Oscillator.

**LOS** line-of-sight.

**LPF** Low Pass Filter.

**LS** Least-Squares.

**LUT** Look-Up-Tables.

**MAC** medium access.

**MDM** Mode-division-multiplexing.

**MDMA** Mode Division Multiple Access.

**MFFT** Singleton's mixed-radix algorithm.

**MIMO** Multiple Input Multiple Output.

**MLS** Maximum Length Sequence.

**MMIC** Monolithic Microwave Integrated Circuit.

**MSP** Mixed Signal Processing.

**NCO** Numerically Controlled Oscillator.

**NDA** Non-data-aided.

**NIC** Network Interface Card.

**NRZ** Non Return to Zero.

**OAM** orbital angular momentum.

**OCC** Optical Camera Communication.

**O-E** Electro-Optical.

**OFDM** Orthogonal Frequency Division Modulation.

**OLT** optical line terminal.

**OOK** On-off keying.

**PA** power amplifier.

**PAM** Pulse-amplitude modulation.

**PAPR** Peak-to-Average Power Ratio.

**PDM** polarization-division-multiplexing.

**PE** plane-electromagnetic.

**PFA** Prime Factor Algorithm.

**PI** proportional-plus-integrator.

**PLE** Physical layout estimation.

**PLL** Phase locked loop.

**PPM** Pulse Position Modulation.

**PPS** Protocol Processing Stages.

**PRN** pseudorandom noise.

**PSSS** Parallel Sequence Spread Spectrum.

**PWM** Pulse Width Modulation.

**QPSK** Quadrature phase-shift keying.

**RF** Radio Frequency.

**RoF** Radio over fiber.

**RR-ASP** Radio Real-time Analog Signal Processing.

**RRH** Remote Radio Head.

**RTO** Real-Time Oscilloscope.

**SAM** spin angular momentum.

**SC** Single-carrier.

**SDC** Synopsys Design Constraints.

**SDM** Space-division-multiplexing.

**SFD** start frame delimiter.

**SiGe** silicon-germanium.

**SNDR** signal-to-noise-and-distortion ratios.

**SNR** Signal-to-Noise Ratio.

**SOC** System-on-a-Chip.

**SPP** Surface Plasmon Polariton.

**SPP** Special Priority Programmes.

**SSMF** Standard Single-Mode Fiber.

**TDE** Time-domain equalization.

**TDM** Time Division Multiplexing.

**TED** Timing Error Detector.

**UAV** unmanned aerial vehicles.

**UWB** ultra-wide bandwidth.

**VCO** voltage-controlled oscillator.

**VLC** Visible Light Communication.

**VLD** Violet Laser Diode.

**WDM** wavelength division multiplexing.

**WFTA** Winograd Fourier transform algorithm.

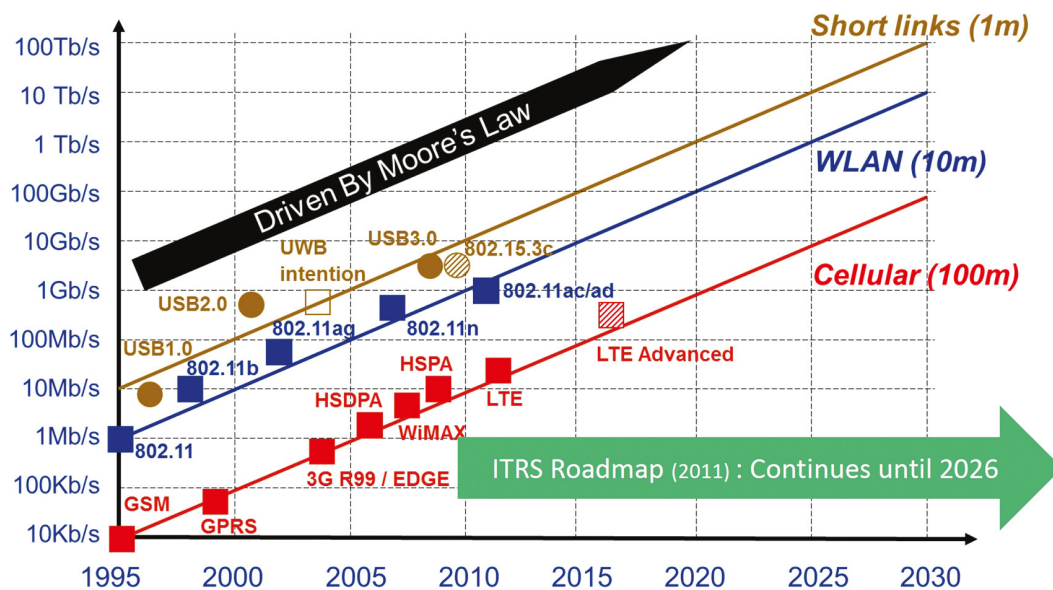
**XR** eXtended reality.

# Chapter 1

## Introduction and Motivation

Wireless communication technology is one of the fastest-growing sectors. This development is primarily driven by a continual need for higher data rates. Figure 1.1 shows the predicted data-rate based on the International Technology Roadmap for Semiconductors (ITRS), first published by Fettweis in 2007 [1]. The graph shows three main trends of modern communication technologies, which are, (i) cellular, (ii) WLAN, (iii) and short-range communication. The increase of the data transmission speed stays constant over time for all three technologies. According to this graph and based on the prediction by Yoakum [2], WLANs will operate at 10 Tbps in 2030.

The main reason for the increased number of networks is the growing data traffic for applications like video streaming, web browsing, social networking, and audio sharing. The Ericsson report [3] from 2019 gives an overview of the current data traffic, e.g., the



**Figure 1.1:** Wireless communication traffic growth prediction and is based on Moore's law. The Figure is taken from Ref. [1].



total number of mobile subscriptions around the world in March 2019 is 7.9 billion, and the number of LTE subscriptions is 3.7 billion. For 2024, there are 8.7 billion mobile broadband subscriptions predicted, and there will be 1.8 billion new 5G subscriptions. However, the number of fixed broadband connections is expected to decrease by around 3%, whereas the number of PCs, tablets, and routers shows a moderate growth up to 330 million in 2024.

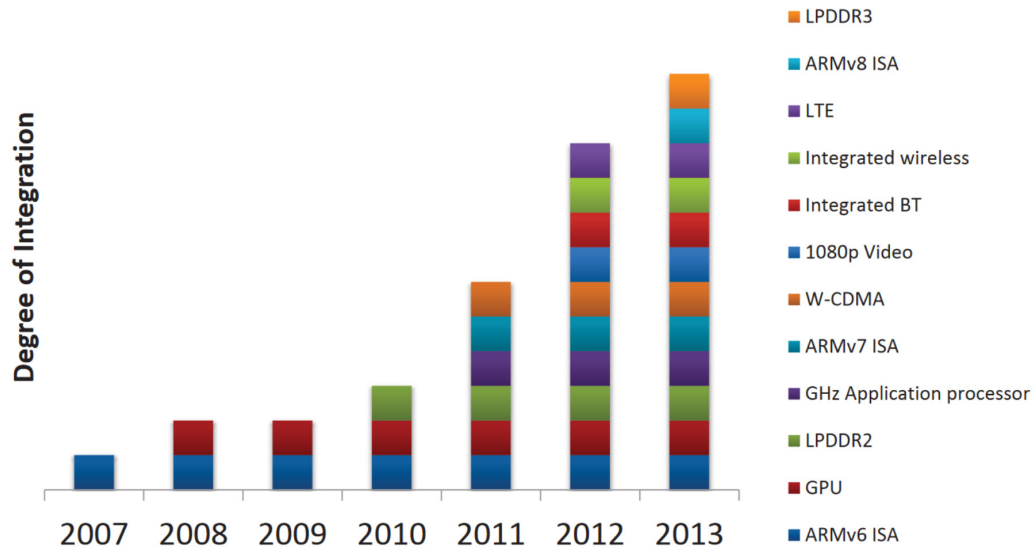
The Ericsson's report [3] also predicts a global mobile data traffic growth per month of 131 exabytes (EB) in 2024. It is estimated that the main part of the data traffic in 2024 will be due to video streaming, which will comprise 74% of the total traffic (which is 96 EB per month).

These above numbers give us the magnitude of the huge number of devices to be connected in within less than a decade. One has to think of how to serve them and their hunger for higher data rates. This is our motivation and challenge to develop a system being capable of handling 100 Gbps and beyond. We are investigating a complete system satisfying at least the following criteria: high data rate, low energy consumption and not to mention the portability of the final prototype to be embedded in mobile devices. There are many applications envisioned which require high data rates [4–8] such as

- eXtended reality (XR),
- Wireless Brain-Computer Interactions (BCI),
- Intra-Device Communication,
- Mobile fronthaul using 300-GHz link,
- ultra-fast wireless local-area-networks,
- intra-chip connectivity,
- kiosk downloads,
- and server farm connectivity,
- Wireless Backhaul, and
- Data Center.

It is a huge effort, to fulfill the demands of these new applications with existing technologies. These new applications do not only require high data rates but also a high reliability and low latencies. There are two ways to achieve high data rates. The first one is to chose a low bandwidth and a high spectral efficiency. The second choice is to move towards a higher bandwidth and a lower spectral efficiency.

The first two applications will reach their data rates by using high spectral efficiencies and low bandwidth available in the 60 GHz frequency range. Another possibility to achieve high data rates is to increase the bandwidth at extremely high frequencies, e.g., in the THz frequency range. In the THz domain, there exists an enormous amount of



**Figure 1.2:** Degree of integration of many functionality ICs in mobile application processors. The figure is taken from Ref. [9], and it reflects the Qualcomm Snapdragon family.

bandwidth available for the data transmission. This was the way to go, suggested in the IEEE working standard [6, 7] for the lower five applications, where only short range transmission is required.

Considering for example the development of Integrated circuits (ICs) in mobile devices, the number of integrated functions which they can perform has increased several fold in the last two decades. In the year 2000, it would require 2-5 min to load a webpage and now it happens within a fraction of seconds. In those times, we could not share photos and videos from our mobile phones. Now, we can stream our favorite series in HD video quality. All of this is the result of complicated IC design that encompasses many features such as WiFi, a GPU unit, a GPS chip, integrated HD video quality, a GHz application processor and many more.

Figure 1.2 shows the integration of a System-on-a-Chip (SOC) of the Qualcomm Snapdragon TM family [9, 10], and the growth of features in current application processors. As mentioned in the ITRS 2.0 report [9, 11], each new technology requires less power. From the year 2007 to 2013, the number of integrated application processes in the Snapdragon family was increased 11 times. The above phenomena lead to a decrease in the number of ICs in smartphones [9] by a factor of 20, while catering more demands of the user. These demands are (i) more computation performance, (ii) higher-speed wireless connection, (iii) and the ability to download higher-quality multi-media content. These interactions require a seamless working of analog and digital circuits. The conventional boundary between analog and digital signal processing is fading out due to the high degree of integration of many processing units on a single ICs (s. Fig. 1.2). Moreover, mixed-signal processing architectures are able to cater many different applications and simultaneously achieve higher data rates. This gives us a hint that we have to explore the possible mixed-signal processing based approaches to achieve 100 Gbps and beyond.

## 1.1 Frequency & Bandwidth choice for 100 Gbps

To enable the integration of “THz” ICs into smart devices for future, their power consumption has to be limited. To realize a data rate of 100 Gbps, there is a need to develop an RF-fronted, a baseband signal processing unit, and the processing of data-link layer protocols with a limitation of power by less than 1 W. However, the RF frontend system alone, as described in Ref. [12], consumes a power of more than 100 W to achieve 100 Gbps. Thus, we have to investigate possible architectures in the areas of:

- Antenna design concepts,
- RF-frontends,
- Signal processing,
- Protocol processing, e.g., MAC layer design.

The Special Priority Programmes (SPP)-1655 was initiated by Deutsche Forschungsgemeinschaft (DFG) [13] to develop solutions for next-generation 100 Gbps wireless communication systems. Within the framework of this call, 11 coordinated projects were granted for six years all over Germany, and each project is focused on dedicated issues ranging from the antennas to RF-frontends, baseband processing, and data-link layer designs. These programs were initiated in order to develop solutions that will reach the aforementioned requirements. Thus, coordinated research activities have been set-up to investigate these challenges and to aim for potential solutions and practical realizations in these research projects.

There are two possible strategies to implement 100 Gbps systems:

- Target for higher bandwidths with moderate spectral efficiencies.
- Target for higher spectral efficiencies with lower bandwidths.

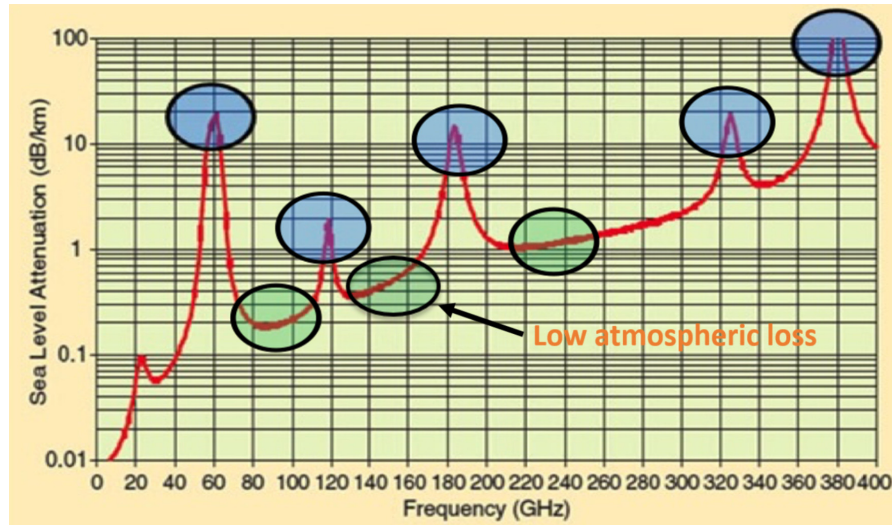
At low RF carrier frequencies (e.g., from 6 GHz to 60 GHz), less bandwidth is available. If, for example, the 60 GHz carrier frequency band<sup>1</sup> is used, a spectral efficiency of 50 bit/s/Hz is needed to achieve the desired 100 Gbps data rate. To arrive at these high spectral efficiencies, we need extremely high-performance baseband processing units. This requires a huge amount of digital signal processing and a high energy consumption.

We have more bandwidth available in a higher frequency spectrum (e.g., from 30 GHz to 3 THz). Thus, a system with RF-carrier frequency above 250 GHz will have bandwidth about 30 GHz is available. With a reduced spectral efficiency of 4 bit/sec/Hz, we will be able to realize 100 Gbps.

There is a trade-off between bandwidth and spectral efficiency. If we consider a 30 GHz baseband bandwidth at an RF-frequency of 60 GHz, this results in a relative bandwidth of 50%. Today we cannot build antennas that can work at this wide relative

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<sup>1</sup>At this frequency band, the available baseband bandwidth is 2 GHz.



**Figure 1.3:** Atmospheric absorption of electromagnetic waves at sea level versus frequency, including the free space path loss. The figure is taken from Ref. [17].

bandwidth. Whereas 30 GHz baseband bandwidth at a 240 GHz RF-frequency will have relative bandwidth around 10%. Thus, we decided for the latter option to implement a 100 Gbps system.

In order to do so, we have to move towards the Extremely High Frequency (EHF) band (from 30 GHz to 300 GHz) or the “Terahertz band” (from 300 GHz to 3 THz) where we have large bandwidth, which is not yet allocated by the European Union. The “Terahertz band” is also part of the EHF band. The EHF band is mainly used for point-to-point short-range communication. One of the drawbacks of the terahertz frequency range is the reduction of antenna aperture. As a result, we can perform data transfer in the THz frequency range only for short-distance communication links. The advantage of this frequency range is that it allows for a miniaturization of the antenna footprint area and opens up an opportunity to develop antenna arrays as fully silicon integrated solutions. In 2015, the European Telecommunication Standards Institute (ETSI) proposed a “Millimeter Wave Transmission document” to study the use cases for mm-Wave spectrum in a range from 50 GHz to 300 GHz [14]. In 2019, the International Telecommunication Union (ITU) allocates the frequency range from 275 GHz to 450 GHz for mm-Wave and THz wireless communication systems [15, 16].

Different frequency bands suffer from different atmospheric absorptions such as oxygen and water molecule absorption, and in addition to it, there is free space propagation loss. Figure 1.3 shows the atmospheric loss for frequencies up-to 400 GHz [18]. It can be observed that there are specific frequency ranges with low atmospheric loss; these frequencies should be used in the design of wireless communication systems. The area marked by blue circles in Fig. 1.3 is suitable for short-range application at 60 GHz, 120 GHz, 183 GHz, 325 GHz, and 380 GHz, and it will attenuate rapidly after a few meters. The area marked by green circles, like 77 GHz, 140 GHz, and 240 GHz suffer from losses less than 1 dB per km, and it is suitable for longer-range broadband communication [17, 19].

An atmospheric window marked around 240 GHz frequency band suffer fewer losses from atmospheric attenuation. This frequency range was used to build RF-frontends built. In our project, we have used RF-frontend operating at these frequencies.

## 1.2 General challenges of 100 Gbps systems

The main goal of SPP-1655 is to find a good trade-off between energy consumption and spectral efficiency to achieve data rates above 100 Gbps. In order to achieve such high transmission rates in wireless systems, new paradigms of system architectures, new algorithmic and technological methods, and possibly new semiconductor components must be developed. The greatest challenge here is the energy efficiency of wireless transmission. The challenge is to find a spectral area where we can achieve 100 Gbps. The bandwidth of the different spectral areas determines the necessary spectral efficiency. The spectral efficiency determines the signal processing effort and thus the energy consumption.

Moreover, if we shift into higher RF frequency bands, we have to deal with free space propagation losses. Thus, for the energy consumption, the trade-off is between relatively lower power consumption at lower spectral efficiency (high RF-frequency and high free space path loss) as opposed to higher power consumption due to the signal processing at higher spectral efficiency (low RF-frequency and low free space path loss)

To achieve these goals, highly integrated semiconductor components and integration concepts are required. New concepts for the distribution of signal processing tasks between analog and digital processing units need to be implemented to reduce energy consumption. This requires numerous synergies in the areas of baseband system architecture, electronic circuit technology, packaging and interconnection technology, and protocol design.

One of the crucial metrics of wireless communication systems is energy efficiency, which is critical for battery-driven devices such as mobile phones, tablets, and many other smart devices. The goal of SPP-1655 is to develop a system for mobile use with a maximal power consumption of 1 W. At a data rate of 100 Gbps, the energy efficiency of  $10 \text{ pJ bit}^{-1}$  can be achieved. A complete communication system consists of three major units, namely, the RF-frontend, the baseband, and a protocol processing unit. Thus, each unit has an energy budget of  $3 \text{ pJ bit}^{-1}$  to achieve 100 Gbps of data rate.

### 1.2.1 Digital design methodology

To reach the target data rate of 100 Gbps, we are going to use a high baseband bandwidth of 30 GHz bandwidth and a moderate spectral efficiency of 4 bit/sec/Hz. A very high-speed Analog-to-Digital Converter (ADC) is required to perform baseband signal processing in the digital domain. According to Nyquist, the sampling rate of the ADCs must be at least twice the transmitted bandwidth (60 GS/s). However, if we consider a practical system consisting of pulse shaping filters, we need at least an oversampling factor between 3 to 5. Thus, opting for a more pessimistic scenario leads to the choice of an oversampling factor for the ADCs of at least three times more than

the available bandwidth. So, the ADC sampling rate should be at least three times as large as the Nyquist frequency in real systems. With a baseband bandwidth of 30 GHz, we require at least ADCs that have a sampling rate of 90 GS/s.

The Murmann report [20] shows a figure of merit of ADCs over the period 1997-2018. The majority of research focuses on the ADCs with  $> 60$  dB signal-to-noise-and-distortion ratios (SNDR) from a single sample. The fastest wide-band ADC reported until now was implemented in 2018 by Kull *et al.* [21], it consumes 199 mW at 32 GS/s using 14 nm FinFET CMOS technology. Extrapolating these values, and assuming we need a minimum sampling rate of 90 GS/s, the *ADC alone* has an energy efficiency of  $5.97 \text{ pJ bit}^{-1}$  to achieve 100 Gbps.

The high-speed Digital-to-Analog Converters (DACs) reported in the last three years are able to achieve data-rates above 100 Gbps [22–27], and mainly the DAC reported in 2016 [22] has a high power dissipation of 15 W. An ultra-high-speed 2-bit DAC with a sample rate of 128 GS/s and a power dissipation of 2 W using  $0.25 \mu\text{m}$  InP DHBT technology was reported by Nagatani *et al.*, 2018 [23]. Following the same argument as before, to achieve 100 Gbps we need at least a DAC sampling rate of 90 GS/s. We arrive at an energy efficiency of  $5.5 \text{ pJ bit}^{-1}$  for the DAC reported by Nagatani.

Let us calculate the amount of power dissipation required if we were to implement a complete radio system *digitally* to achieve 100 Gbps. Consider an example of an IEEE 802.11ax standard for WLANs [28], and the maximum achievable throughput is 9.6 Gbps. The 7 nm ARM-based chip processor released in 2019 by TSMC [29] has four Arm Cortex-A72 processors operating at 4 GHz and has an energy efficiency of  $0.56 \text{ pJ bit}^{-1}$ . If this processor is used to perform only Digital Signal Processing (DSP) operations for baseband processing, we require 56 mW. Note that we have not taken into account the power consumption of many parameters like (i) inter-connects, (ii) DAC/ADC data converters, (iii) and the power required to reach higher spectral efficiency. Thus, there is a strong need for new algorithmic approaches to design the whole communication architecture.

### 1.2.2 Analog design methodology

Now let us consider the analog solution to implement 100 Gbps systems. In 2007, Mörz implemented an analog Viterbi decoder to perform forward error correction (FEC) at 800 Mbps consuming 120 mW in SiGe technology [30]. The required energy efficiency is  $160 \text{ pJ bit}^{-1}$  on  $0.25 \mu\text{m}$  SiGe technology. By extrapolating the results of Mörz to achieve 100 Gbps, we need a power of 6 W. Another example of analog-based Multiple Input Multiple Output (MIMO) processing was published by Soler, 2019 [31]. It reports the lower consumption of power and complexity compared to a digital solution.

Radio Real-time Analog Signal Processing (RR-ASP) is a recent promising technology for wireless communication [32–34]. The work-horse behind RR-ASP is the “phaser.” A phaser is a frequency-dependent delay line that outputs a specific group delay versus frequency response. It transforms an ultra-wide bandwidth (UWB) pulse into time-spread

version spectral components. An efficient technique for processing purely analog and real-time multiple access schemes is called Dispersion Code Multiple Access (DCMA) [35]. Zou *et al.*, 2018, [36] demonstrated a  $2 \times 2$  DCMA system in X-band frequency with a data rate of 500 Mbps, and they were limited by the measurement devices. The authors claim that the same technique can be extended to higher RF frequency in the THz region to achieve a higher data rate and also by using high-end measurement equipment. As DCMA is a real-time analog signal processing technology, it has several advantages over DSP-based technologies like the very low latency, lower complexity, lower cost, and power consumption and their scalability features in an mm-Wave/THz frequency range.

Complementary Metal-Oxide-Semiconductor (CMOS) scaling goes down to 5 nm and 3 nm. For the past six decades, “Boolean logic” has been the key enabling technology for DSP computation work. The “Boolean bottleneck” occurs when we perform a large number of power-intensive operations such as multiplication, division, and addition. These operations are required to implement baseband algorithms for 100 Gbps systems. Thus, solving the above computational problem leads to the development of “Non-Boolean” methods utilizing coupled oscillator systems [37–39], which is a type of analog signal processing technique. Shukla *et al.*, 2014, [40] demonstrated that pairwise coupled hybrid vanadium dioxide-MOSFET oscillators, which were used to perform image recognition, have  $\sim 20$  times lower power consumption compared with 11 nm CMOS design. Thus, we have to adopt analog signal processing techniques to perform complex baseband operations with low energy consumption.

### 1.2.3 Design challenges

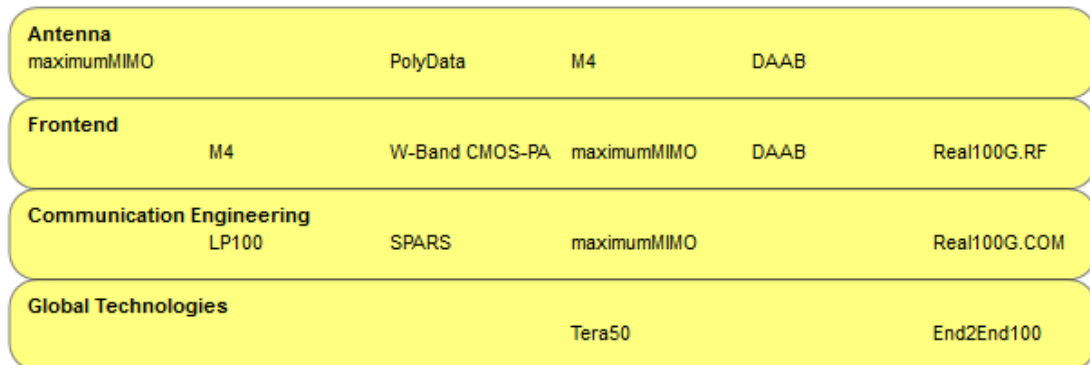
The SPP-1655 program targets future solutions for the implementation of 100 Gbps wireless communication systems. The main challenges arising are summarized below,

- Investigation of the new prototypes for reduced energy and complexity catering to ultra-high-speed wireless communication systems.
- Investigation of new baseband PHY algorithms considering the trade-off between spectral efficiency and energy efficiency.
- Investigation of signal boundary separation between analog and digital signal processing.
- Investigation of medium access (MAC) protocols for error correction and low energy.
- Investigation of non-Boolean computing architecture.
- Investigation of new transistors architectures with cut-off frequencies  $> 1$  THz.
- Investigation of end-to-end system architectures, including antenna design, RF-front-ends, baseband, and MAC layer protocols to achieve 100 Gbps.

### Vertical Cluster



### Horizontal Cluster



**Figure 1.4:** Cluster of projects in the program SPP-1655 [13] which are grouped according to a different theme.

## 1.3 Introduction to SPP-1655 projects

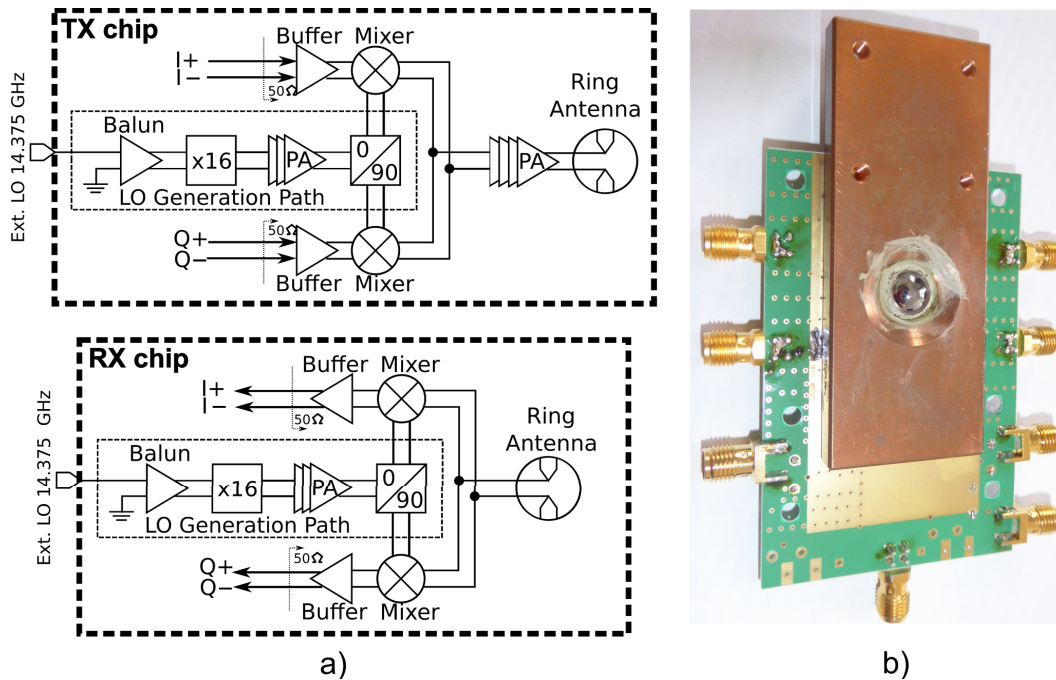
The SPP-1655 project is divided into two broad clusters, reflecting the interconnection of the project in the vertical cluster and the interdependency of the used scientific disciplines in the horizontal cluster, as shown in Fig. 1.4. Further down, the horizontal cluster is again sub-divided into four themes focusing on different areas of communications systems. The vertical cluster consists of projects which need to have a synergy to provide a complete wireless communication system that includes RF-frontends, PHY layer, and MAC layer. They are grouped according to different architectures of the systems. For a detailed description of all projects, see Ref. [13, 41].

The research subjects of this thesis are part of the project “Real100G.COM”. This project belongs to a vertical cluster “Real100G” which is marked in green, as in Fig. 1.4. The projects belonging to the green cluster are discussed briefly in the next section.

### 1.4 Real100G.RF

The objective of the Real100G.RF project is to leverage silicon-based economies-of-scale for a technology breakthrough in wireless communication above 200 GHz based on silicon circuits. This will be achieved with a completely new cross-cutting methodology for silicon-Monolithic Microwave Integrated Circuit (MMIC) design using SiGe, e.g., the development of wideband receiver and transmitter arrays, including on-chip antenna arrays. The Real100G.RF project will enable a real breakthrough in the functionality



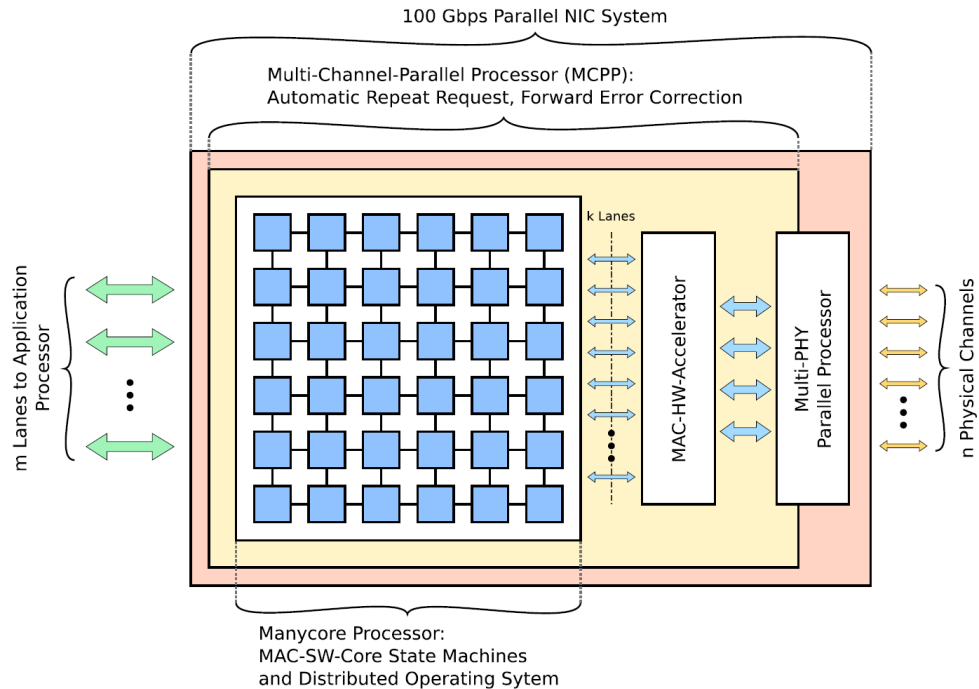


**Figure 1.5:** a) Transmitter and Receiver architecture b) photo of one of the RF modules. The Figure is taken from Ref. [42].

(number of RF elements), performance (data rate), component size (fully-integrated high-density arrays with integrated antennas), and power. The significant challenges of such a system are,

- Developing a low-cost, silicon-based, surface-mount RF front-end modules enabling 100 Gbps short-range wireless communication.
- Wideband millimeter-wave circuit architectures in silicon process technologies for above 200 GHz.
- A compact surface-mount radio module approach with package integrated antenna arrays.
- Silicon-based multi-antenna front-end concepts for 100 Gbps transmission.

At mm-Wave/THz frequencies (230 GHz), a complete RF-frontend chain was realized in a single silicon chip and integrated with a lens antenna array into a single package. A system-in-package consists of the input signal (the baseband I/Q signals), the control signals, DC signals, and the RF output signal as shown in Fig. 1.5. In this project, an ultra-compact radio with an RF-bandwidth of 26 GHz was developed. An entirely packaged 230 GHz RF-frontend with power combining antenna was designed using 0.13  $\mu\text{m}$  SiGe technology. The results of this project are presented in Ref. [43].



**Figure 1.6:** Processing Architecture of the 100 Gbps NIC.

## 1.5 End2End100

The task of the Data Link Layer (DLL) layer is to receive the raw data stream and forward it to the application processors. One more additional responsibility of the DLL is the flow control management. Büchner *et al.*, [44] evaluated that there are 120 ns available for the DLL to perform all the Protocol Processing Stages (PPS) to achieve a data-rate of 100 Gbps. In this short period, the DLL has to handle the following processes:

- checking the data for errors,
- determine the type of errors,
- performing retransmission of packets if necessary,
- also, finally, restoring the transmitted packet.

The main idea of the “End2End100” project is to investigate a new concept for the Network Interface Card (NIC) that handles the task of DLL. As shown in Fig. 1.6, the task is split into two notable areas [45], (i) Parallel protocol processing, (ii) and a Manycore processor. When transmitting user data, the MAC state machine running on the many-core architecture delivers data in parallel over  $k$  lanes to the next processing stage, i.e., to hardware accelerators. This data is processed in hardware accelerators and multiplexed to  $n$  physical channels.

100 Gbps wireless networks also put tremendous stress on the NICs themselves. Multiple channels need to be logically bonded to achieve the desired data rate. Thus, protocol

processing has to care about multiple channels in parallel. This scheme is in principle a stream processing scenario, where a single high-speed memory stream is broken up into several lower-speed streams that in turn are transmitted over separate wireless channels.

Care has to be taken of the dependencies within communication protocols, which impact parallelization. The above challenges were solved with a soft real-time stream processing, and it was presented in Ref. [44, 46]. Recently Lopacinski *et al.* published articles [47, 48] about achieving a 120 Gbps FEC for wireless 100 Gbps communication on a 40 nm CMOS technology using a silicon area of 1 mm<sup>2</sup> only, with an energy efficiency of 3 pJ bit<sup>-1</sup>.

There is a need for intelligent error correction schemes and flow control schemes for an ultra-high-speed requirement. The Protocol Processing Stages (PPS) and the flow control should be offloaded from the central client processor to the NIC, so that host-processor (s. Fig. 1.6) resources are free for other tasks from the higher layers of protocol processing. The results of this project are presented in Ref. [45].

## 1.6 Real100G.COM

The research conducted in this Thesis is part of the “Real100G.COM” project. We have focused on developing a PHY layer modulation scheme for the extremely high transmission speed of 100 Gbps. One possible approach to use an ultra-high RF bandwidth with moderate spectral efficiency and carrier frequencies in the THz region. In this project, we focus on system design, baseband signal processing, and synchronization in RF-domain. In our approach, the use of high RF bandwidth results in extreme bandwidth requirements for the baseband processor. Additionally, the ADCs/DACs for data rates at these speeds are extremely power-hungry and challenging to realize.

As outlined earlier, analog signal processing has the advantage to be both more energy-efficient, and it requires fewer transistors than CMOS digital implementations and is, therefore, less complex. We assumed an intelligent mixture of analog and digital signal processing has a great potential to outperform purely digital processing for power dissipation, hardware complexity, and cost. We chose Parallel Sequence Spread Spectrum (PSSS)<sup>2</sup> as an analog-friendly modulation and coding scheme that facilitates an efficient mixed-signal implementation of an 100 Gbps wireless baseband processor.

With respect to the trade-off between bandwidth and spectral-efficiency, we decided for the RF bandwidth to be in the range from 30 GHz to 50 GHz, and the spectral efficiency of 2-4 bit/sec/Hz. Such a bandwidth is only available at very high carrier frequencies > 200 GHz. The research of the Real100G.COM project is divided between three working groups, and this work is part of the prof. Kraemer’s group. The research challenges of this project are

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<sup>2</sup>PSSS is basically an orthogonalization method in the code domain. Coding, consequently, means mapping of bit values onto specific codes to enable concurrent transmission.

- Analog-/Mixed-Signal PSSS transceiver baseband for 100 Gbps system (prof. Kraemer and prof. Scheytt).
- Adaptive equalization of ultra-high bandwidth channels (prof. Kraemer and prof. Scheytt).
- Synchronous detection of wireless ultra-broadband signals (prof. Kallfass).

Prof. Kallfass's group studied feasibility, and experimentally evaluated the performance of synchronous reception methods at RF carriers approaching sub-millimeter-wave frequencies, namely wideband Costas loops and RF carrier recovery. Direct digital demodulation by Costas loops will provide a synchronous detector for PSSS-modulated signals. They designed and implemented a BPSK Costas loop operating directly at an RF  $> 200$  GHz. Moreover, to accommodate the I-Q transmission, a QPSK Costas loop on SiGe HBT MMIC technology had been realized.

Prof. Scheytt's group developed a mixed-signal PSSS receiver architecture. The received PSSS signal is decoded using parallel Integrate and Dump Correlators (IDCs). Critical circuit blocks of the mixed-signal 100 Gbps PSSS receiver architecture were designed and simulated on transistor-level. The results of this project are published in Ref. [49].

## 1.7 Motivation

Wireless ultra-high-speed communication systems at a speed of 100 Gbps or more are beyond today's state of the art. To implement a terahertz communication system at 200 GHz electronically, one can choose between various technologies like indium-phosphide (InP), gallium-nitride (GaN) or silicon-germanium (SiGe). The RF-frontends modules implemented using SiGe have low cost and easy integration into modern digital electronics. There are many 100 Gbps systems demonstrated in the literature [50–52] using known modulation schemes like QAM or QPSK with RF-frontends implemented using electronic technology (operating above  $> 200$  GHz). All of the above systems have one common feature that they use either an Arbitrary Waveform Generator (AWG) for the baseband signal generation at the transmitter or a Dynamic Signal Analyzer (DSA)/Real-Time Oscilloscope (RTO) at the receiver for off-line evaluation of the recorded data. None of the above-described approaches addresses the complete wireless system which encompasses tasks like synchronization, real-time demodulation of the received data, channel equalization, and the generation of the baseband signal for the transmitter to achieve 100 Gbps.

We have a very high baseband bandwidth of 30 GHz in the THz frequency band. In traditional transceiver systems, we need data converters (ADCs/DACs) with extremely high bandwidth and sampling rates. Also, the output from the data converters needs to be further down processed in the baseband operations (such as synchronization, channel equalization, and data demodulation) at a very high clock frequency. Even-though we target for low spectral efficiency (2 to 4 bit/sec/Hz), the amount of signal processing to

achieve the data rate of 100 Gbps is enormous.

Moreover, there is one more challenge to overcome in the design of equalization for such high bandwidth systems. We have to choose analog equalizers as they support very high data rates. Balachandran *et al.*, 2018, [53] implemented an analog continuous-time linear equalizers (CTLE) to achieve 32 Gbps using 65 nm CMOS with an energy efficiency of  $0.54 \text{ pJ bit}^{-1}$ . Mattia *et al.*, 2017, [54] realized an analog 5-tap Decision Feedback Equalizer (DFE) on a 28 nm CMOS. They have demonstrated data rates up to 36 Gbps with an energy efficiency of  $3.8 \text{ pJ bit}^{-1}$ . An adaptive digital equalizer was reported by Hsiao *et al.*, 2017, [55], which can achieve a data rate of 10 Gbps using 40 nm CMOS, and has an energy efficiency of  $1 \text{ pJ bit}^{-1}$ . All the above-mentioned equalizers do not operate at 100 Gbps, although analog equalizers can operate up to 36 Gbps. However, analog equalizers are not as adaptive as digital equalizers. The drawback of digital equalizers is that they can operate up to 10 Gbps. As previously stated, the baseband processor has a maximum energy budget of  $3 \text{ pJ bit}^{-1}$  to achieve 100 Gbps. The best analog equalizers from Balachandran *et al.*, 2018, [53] consume 17% of the total allocated energy budget for baseband processing. Thus, there is a need for equalizers which can achieve high data rates at low power consumption.

Therefore, there is a strong need to develop mixed-signal baseband algorithms that can perform real-time signal processing operations such as modulation, demodulation, and equalization. This is the point where Parallel Sequence Spread Spectrum (PSSS) as an analog friendly modulation system, plays an important role. The basic notion of the mixed-signal processing is the partitioning of signal processing tasks into a slower digital clock domain and a faster analog part, e.g., by exploiting the two natural clock domains available in the spread-spectrum communication systems, i.e., the lower symbol clock and the higher chip clock. As the PSSS modulation technique is also a form of spread spectrum communication, it inherently supports these two clock domains.

We employ a resource-efficient mixed-mode baseband processing based on PSSS modulation in (mostly) analog domain. Thereby, we avoid high-speed data converters<sup>3</sup>. Thus, the PSSS modulation has the following advantages,

- The PSSS transmitter development is simple as it consists of multipliers and adders. The whole transmitter design can be split up in two parts: One section is running digitally with the low PSSS symbol clock frequency, and a serializer unit is running at the chip clock frequency.
- The PSSS receiver can be realized with a parallel IDC operating at the chip rate to demodulate the received signal.

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<sup>3</sup>The factor at which we can have the PSSS symbol clock reduced depends on the choice of the m-sequence length. In our project, we have chosen m-sequences of the length of 15. Thus, a PSSS symbol clock operates 15 times slower than the chip clock.

- The PSSS modulation facilitates a hardware architecture wherein transmitted data can be demodulated, and at the same channel, equalization can be performed. The channel equalization scheme is implemented by code weighting.
- The ADCs/DACs need to be operated at the low PSSS symbol clock. The required bit resolution of these converters has to be equal to the target spectral efficiency.

To increase the efficiency of the spectral use, different advanced modulation techniques like orthogonal PAM-16 ( $2 \times 4$  bit/sec/Hz<sup>4</sup>) or higher level QAM techniques were investigated. The use of QAM has the advantage of increasing the Signal-to-Noise Ratio (SNR), but it requires a more complex Costas loop for synchronization when operating with a large analog baseband bandwidth.

## 1.8 Structure of the thesis

The structure of the Thesis is as follows:

- Overview of current and future 100 Gbps technologies (Chap. 2).
- Theoretical introduction and the PSSS system analysis (Chap. 3).
- PSSS transceiver system architecture (Chap. 4).
- Channel equalization implementation and PSSS transmitter implementation (Chap. 5).
- Results of the measurement experiments (Chap. 6).

## 1.9 List of Publications

### Contributions

Prof. Kraemer's group was responsible for designing the architecture of baseband systems and our contributions are,

- PSSS system model simulation for various spectral efficiencies.
- Analysis of the clipping effect on PSSS modulated signal by using the RAPP model.
- For the first time, we have performed Hardware-in-the-Loop (HIL) experiments on RF-frontends with a carrier frequency between 230 GHz to 280 GHz using PSSS modulation.
- With the use of Kasami codes, we utilize both I/Q channels of transmitter and receiver to increase the spectral efficiency further. We have performed initial HIL experiments to prove that I-Q transmission is successful with Kasami codes.

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<sup>4</sup>This modulation uses only constellation points on the I- and Q-Axis forming two independent orthogonal channels.

- We have developed and implemented a high-speed channel equalization algorithm.
- We have developed a parallel PSSS encoder transmitter architecture to operate at the chip clock rate.

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3. KrishneGowda, Karthik; Wolf, Andreas C.; Kraemer, Rolf; Messinger, Tobias; Kallfass, Ingmar, “Simulation of 100 Gbps using Parallel Sequence Spread Spectrum modulation (PSSS) with 240 GHz radio,” in Radio Science Conference (URSI AT-RASC), 2015 1st URSI Atlantic , vol., no., pp.1-1, 16-24 May 2015.
4. Krishnegowda, Karthik for a “PHY Layer Design for THz Communication” invited talk at the EMN Meeting on Terahertz 2016” which is held in San Sebastian, Spain from May 14-18 2016.
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8. K. Krishnegowda, P. Rodriguez-Vazquez, A. C. Wolf, J. Grzyb, U. R. Pfeiffer, and R. Kraemer, “100 Gbps and beyond: Hardware in the Loop experiments with PSSS modulation using 230 GHz RF frontend,” 2018 15th Workshop on Positioning, Navigation and Communications (WPNC), Bremen, 2018, pp. 1-5.
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Frequency Band,” 2018 26th Telecommunications Forum (TELFOR), Belgrade, 2018, pp. 1-5.

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1. A. R. Javed, J. C. Scheytt, K. Krishnegowda, and R. Kraemer, “System design considerations for a PSSS transceiver for 100Gbps wireless communication with emphasis on mixed signal implementation,” in 2015 IEEE 16th Annual Wireless and Microwave Technology Conference (WAMICON), 2015.
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3. A. R. Javed, J. C. Scheytt, K. Krishnegowda, and R. Kraemer, “System design of a mixed signal PSSS transceiver using a linear ultra-broadband analog correlator for the receiver baseband designed in 130 nm SiGe BiCMOS technology,” in 17th IEEE International Conference on Smart Technologies, EUROCON 2017 - Conference Proceedings, July 2017.
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5. E. R. Bammidi, A.R.Javed, K. Krishnegowda, and Kallfass, I, “A Differential Traveling Wave Active Power Divider in 130 nm SiGe: BiCMOS Technology for Application in Receiver Synchronization”, The 22nd European Microwave Week 2019, p. 5–8. October 2019. **(Accepted)**
6. J. C. Scheytt, A. R. Javed, E. R. Bammidi, K. Krishnegowda, I. Kallfass, and R. Kraemer, “100 Gbps Wireless System and Circuit Design Using Parallel Spread-Spectrum Sequencing,” *Frequenz*, vol. 71, no. 9–10, August 2017. **(Journal)**
7. L. Lopacinski and M. Marinkovic and G. Panic and M. H. Eissa and A. Hasani and K. Krishnegowda and R. Kraemer, “Data Link Layer Processor for 100 Gbps Terahertz Wireless Communications in 28 nm CMOS Technology,” in *IEEE Access*, vol. 7, pp. 44489-44502, 2019. **(Journal)**

### Patents

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2. Wimmer, Lara, and Methfessel, Michael and Kraemer, Rolf and Krishnegowda, Karthik.  
“Synchronization in a PSSS radio communication technology for high data rates.”  
European Patent Office, AZ: EP 19 167 902.6, filed April 08, 2019.

## Chapter 2

# Current and future 100 Gbps technologies

Wireless communication systems with data rates of 100 Gbps and beyond are required to handle the increasing data traffic predicted for future. Up to now, there exist no practical, usable End-2-End systems according to specifications for current mobile communication clients such as  $< 1$  W End-2-End power dissipation, and high integration into standard ICs.

The major IEEE groups created working on next-generation wireless communication systems are:

- **IEEE P802.11ax (Wi-Fi 6):** The standard is designed to operate in ISM bands between 1 GHz and 6 GHz. The Wi-Fi 6 have demonstrated a data rate of 10 Gbps. The key capabilities defined in the standard are Multi-user multiple input, multiple output (multi-user MIMO) , Orthogonal frequency division multiple access (OFDMA), Target wake time (TWT) and 1024-QAM [56, 57].
- **IEEE P802.11ay:** The standard defines new PHY and MAC specifications that enable 100 Gbps wireless communication at 60 GHz. It includes sophisticated baseband techniques like MIMO, channel bonding, improved channel access, and enhanced beam-forming [58].
- **IEEE P802.15.7m:** Short-Range Optical Wireless Communication including Optical Camera Communication (OCC) and LED-ID. OCC uses external modules of a camera such as flash, display and image sensors as a transceiver for positioning/localization and message broadcasting [59].
- **IEEE 802.15.13:** The IEEE 802.15.13 Multi-Gigabit/s Optical Wireless Communication Task Group specifies a Physical (PHY) and Media Access Control (MAC) layer for the light wavelengths from to 190 nm-10  $\mu$ m. The standard defines a data-rate up-to 10 Gbps at distances up-to 200m in a line-of-sight scenario [60].

- **IEEE802.15 IGthz:** This task group focuses on THz communication and applications in the frequency range of 275 GHz to 3 THz. THz wireless communication would offer very high data rates from 100 Gbps up-to 1 Tbps [61].

The IEEE P802.11ax and IEEE P802.11ay standards operate at ISM/mm-Wave band, and use baseband technologies (such as OFDMA, MU-MIMO, beam-forming) to achieve a data rate of 100 Gbps. The standards IEEE 802.15.13 and IEEE P802.15.7m do not explicitly aim as high as 100 Gbps but they employ technologies that can possibly be used for such high data rates as discussed in this Chapter. The last group listed targets the benchmark of 100 Gbps at THz frequency band.

The important Key-Performance-Indicators (KPIs) taken into account in 100 Gbps technologies are bandwidth, data rate, wireless distance covered, energy efficiency, and spectral efficiency. This Chapter provides an overview of currently existing 100 Gbps technologies and potential near-future technologies currently under development. These technologies are listed below:

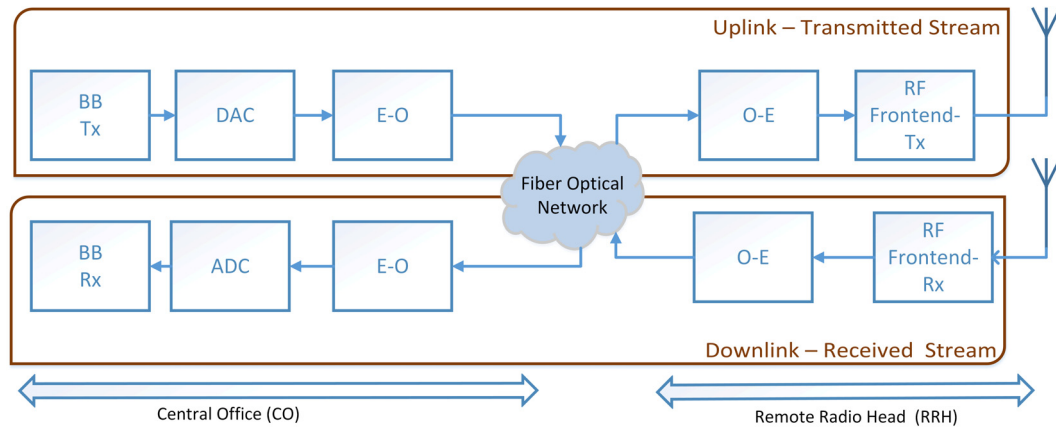
- **Direct modulation for THz communication** The baseband signals are directly mapped onto terahertz frequencies.
- **RoF:** In Radio over fiber (RoF) systems, a Remote Radio Head (RRH) is interfaced with a Central Office (CO) using Electro-Optical (E-O)/Electro-Optical (O-E) converters. These converters are based on optical modulators using either photonics or plasmonic technology. The last connecting part of the RRH is a THz RF-frontend.
- **OAM-MIMO:** A multiplexing of different, linearly independent orbital angular momentum (OAM) modes combined with the advanced DSP of MIMO systems facilitates data rates even above 100 Gbps [62].
- **FSO:** Free-space optical communication (FSO) systems use a laser to provide a directed beam in free space air for data transmission.
- **VLC:** In a Visible Light Communication (VLC) system, a LED is used for the data transmission. The receiver could be a mobile phone camera or a photo-detector.

In the following Sections, these technologies are described in more detail and discussed in comparison to the technologies applied within this Thesis.

## 2.1 Direct modulation for THz communication

In direct modulation THz communication systems, a baseband signal with a high analog bandwidth is directly modulated onto a carrier signal in the terahertz frequency range. This band offers large bandwidths facilitating high data rates with use of moderate spectral efficiency. Here, we focus on electronic systems without optical elements.

For a G-band transmission at 240 GHz, a QPSK modulated waveform was transmitted over a distance of 850 m to achieve 64 Gbps by Kallfass *et al.* [63]. The system reported



**Figure 2.1:** A generic block diagram of RoF systems.

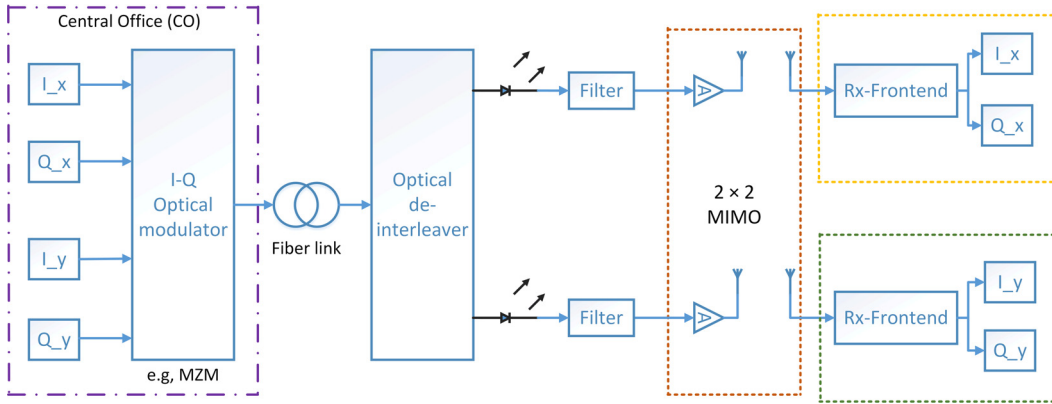
in Ref. [64] reached 96 Gbps with 8-PSK modulation with a 240 GHz electronic receiver and a fully electronic transmitter MMIC.

As discussed in the first Chapter, we decided for a direct modulation THz system to reach 100 Gbps. In our HIL experiments, we use two RF-frontends (SiGe and InP technology [65, 66]), employing a direct up-conversion of the baseband signal on to the THz frequency band. A generic block diagram of those systems is detailed in Chap. 4. Our measurement experiments using these two frontends are explained in Chap. 6. For the 230 GHz RF-frontend based on silicon-germanium technology [65] and a 1-m wireless link using PSSS modulation, we measure a data rate of 80 Gbps as described in our article [42]. Rodriguez-Vazquez *et al.*, 2019 [51], use the same above-frontend, and they achieve a data rate of 100 Gbps for 16-QAM modulation with a wireless distance of 1-m.

## 2.2 Radio over fiber systems

In radio over fiber systems, the RF signal is sent as an optical signal over a fiber. This procedure has the advantage that the signal can be transmitted over long distances without interferences and very low losses. Only at the end terminal, the message is sent as a wireless signal in air. The conversion from an optical to a radio signal can be implemented very efficiently, e.g., using photonics converters [67, 68].

RoF is currently considered to be a promising solution for mobile front-/backhaul and wireless distribution networks. Figure 2.1 shows a generic scheme of a radio over fiber system, consisting of a remote radio head connected to a central office. The communication element between the RRH and a CO is realized with a fiber-optic link. The baseband signal is converted to an electrical signal and then modulated onto an optical carrier via an E-O conversion process. In downlink direction, the modulated optical signal is photo-detected (O-E conversion) at the remote antenna base-station and is fed to the RF-frontend transmitter for the transmission. A similar process takes place for the downlink stream of the wireless network with fiber optic links transporting the radio signals from the RRH to the CO.



**Figure 2.2:** A generic block diagram of a MIMO-RoF system.

Many RoF systems described in the recent literature [69–72] either make use of photonic or plasmonic technology to design E-O/O-E converters. The accuracy of the high speed optical to electrical conversion makes radio over fiber systems particularly suitable for high data rates. Recently, data rates up to 400 Gbps have been demonstrated [73]. In the above-experiment they show integration of two optical wireless systems. The first system delivers a  $2 \times 112$  Gbps polarization-division-multiplexing (PDM) 16-QAM signal at an RF frequency of 37.5 GHz, and with a wireless distance of 1.5 m. A second system has a data rate of 108 Gbps employing PDM-QPSK modulation at RF frequency of 100 GHz, and with a wireless distance of 0.7 m.

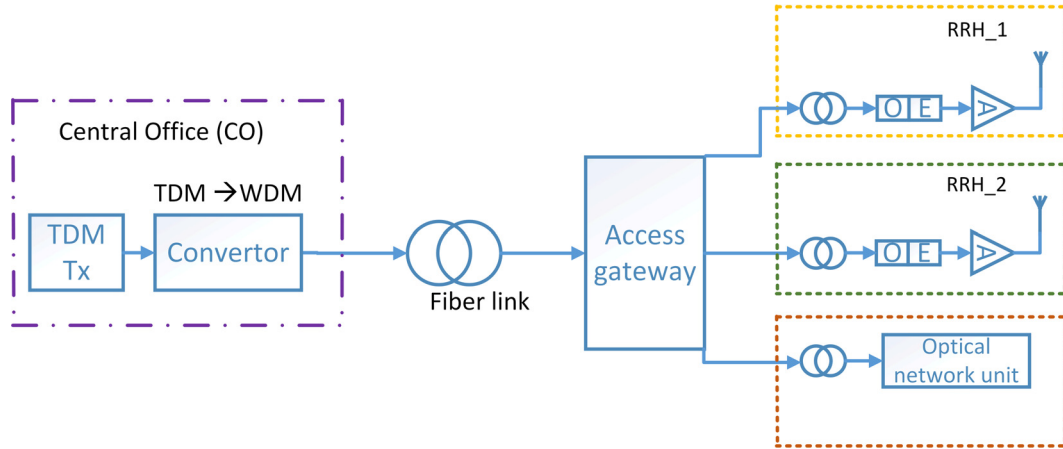
Radio over fiber systems are applicable for long haul data transmission, where the signal is only a wireless signal in the “last mile”. This requires the preparation of an extensive fiber infrastructure beforehand.

### 2.2.1 Photonic Technology

This Section provides an overview of the most recent works using photonic technology in combination with a mm-Wave/THz wave radio frontend to achieve 100 Gbps data rate and above. Photonic technologies offer various options to increase the data rate, e.g., combining photonics with MIMO or wavelength division multiplexing (WDM). A MIMO technique can be used at the RRH along with RoF systems employing photonic modulators for an increased transmission rate. Another method to enhance the data throughput is WDM. In a WDM scheme, several optical carrier signals are multiplexed onto a single optical fiber. The use of WDM-RoF facilitates the de-multiplexing of the optical signal at the remote receiver units into many RRHs. The above approach promotes the use of many RRHs, thereby increasing the data rate.

In a point-to-point communication scenario, Liu *et al.*, 2018, [69] demonstrated THz photonic wireless transmission of a 16-QAM modulated signal in the 350 GHz mm-Wave band. A data rate of 100 Gbps was shown over a 350 GHz wireless link at a distance of 2 m.

In Fig. 2.2, a generic MIMO-RoF system is shown. At the CO, an I-Q optical modulator



**Figure 2.3:** A block diagram of a WDM-RoF system operating with mm-Wave transmitters.

receives a baseband signal ( $I_x$ ,  $Q_x$ ,  $I_y$  and  $Q_y$ ) individually on x and y polarization and converts it into an optical signal to be transmitted along the optical fiber cable. At the optical receiver, an optical de-interleaver [74] separates the odd and even channel signals which are operated at C- or L-band wavelengths.

The x-polarized part of the signal is converted into an electrical signal by a photodiode and fed into the RF-frontend operating at sub-millimeter frequencies. The same operation is performed onto the y-polarized data. Thus, above configuration forms a  $2 \times 2$  MIMO system. Finally, the corresponding baseband data string on each channel is reproduced by the respective RRHs.

A  $2 \times 2$  MIMO system operating at D-band (carrier frequency 141 GHz) was shown to achieve a data rate of 352 Gbps using photonic technologies [70]. In this study, authors employ carrierless amplitude phase (CAP) modulation (i.e, 16-CAP at 22 Gbaud per side-band in each polarization). The mm-wave signal coming from photo detectors to the  $2 \times 2$  MIMO transmitter is amplified to 15 dB by electrical amplifiers (operating at D-band), and then transmitted wirelessly by horn antennas (with gain of 25 dBi). At the MIMO receiver, the signals were down-converted to an intermediate frequency (IF) of 29 GHz with use of 112 GHz local oscillators. The down-converted signals were stored in the RTO with a sampling rate of 160 GS/s, and the data analysis was performed offline. The transmitted wireless distance was 0.6 m and at this range, the Bit Error Rate (BER) was below the 20% FEC threshold.

Recently Kim *et al.* 2019 [75] demonstrated an over-the-air based  $4 \times 4$  MIMO distributed antenna system (DAS) with a single RoF link. The RF transmission was at a mm-wave frequency of 27.5 ~ 28.3 GHz catering to 5G mobile networking. To increase the optical transmission capacity, Kim *et al.* employ frequency/wavelength multiplexing so that RoF links transfer  $4 \times 8$  FAs (4-antennas, 8-Front Access (FA) per each antenna) 5G signals concurrently which is corresponding to  $\approx 147.4$  Gbps data rate.

The NG-PON2 standard [76] had opted for WDM as the essential enabler for future mobile fronthaul networks, and also for wireless distribution networks. The fundamental operation of a photonic-millimeter-wave transmitter is shown in Fig. 2.3. The “TDM Tx”

performs a multiplexing operation, wherein the data originating from several low-rate streams is converted into a single high-rate bit-stream (not shown in Fig. 2.3). The aforementioned high-speed signal is fed into a TDM-WDM converter. The converter module performs a mapping from the Time Division Multiplexing (TDM) channels onto WDM channels (i.e, M:1 mapping<sup>1</sup>), wherein each of the WDM channels has a different wavelength. Finally, the optical signal is sent along with the optical fiber link. At the receiver, an arrayed waveguide grating [77] is used as “Access Gateway” (s. Fig. 2.3) to extract the WDM data channel (i.e, 1:M mapping). The data is further transmitted to the RRHs or the optical network unit. At the RRH, a photodiode converts the optical signal into an RF electrical signal, which is fed to an antenna for wireless transmission. For the first time, Guan *et al.*, 2019, [78] proposed a highly flexible transmitter structure for an optical line terminal (OLT) for a WDM-PON system. The above-mentioned transmitter structure is capable of perfectly generating any combination of WDM-RoF channels and regular optical WDM channels. The WDM-ROF data channel needs a separate optical wave for hetrodyne up-conversion, and also a precise wavelength stabilization to maintain a stable wireless carrier frequency. Guan *et al.* have demonstrated  $12 \times 2.5$  Gbps with On-off keying (OOK) modulation and  $10 \times 4$  Gbps QPSK hybrid transmission over a 100 km Standard Single-Mode Fiber (SSMF) cable with a wireless distance of 0.5 m.

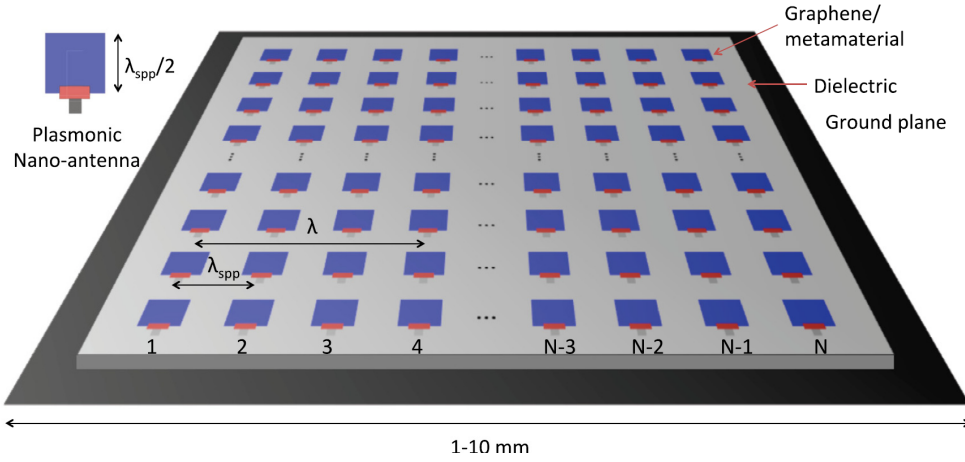
Analog RoF systems facilitate low complexity RRHs for wireless networks. Van Gasse *et al.*, 2018 [79] outline the core-components, i.e., E-O/O-E convertors implemented on single integrated photonic IC chips based on III–V silicon photonics technology. Van Gasse *et al.* demonstrated 120 Mbps data rate over 5 km of a SSMF cable with a 64-QAM OFDM signal at a carrier frequency of 5 GHz.

Most systems mentioned in this section apply standard modulation schemes, and the measurement experiments use an Arbitrary Waveform Generator (AWG) and an RTO for recording the waveform and analysis is performed offline by using Matlab. There is a long way to go from the works discussed above to a practical useable system including baseband processing etc. for the wireless part of the system such as channel equalization, synchronization, real-time signal generation at the transmitter, and demodulation at the receiver.

### 2.2.2 Plasmonic Technology

Figure 2.4 shows the conceptual idea of a plasmonic nano-antenna array. Plasmonic materials consist of metals which aid the propagation of Surface Plasmon Polariton (SPP) waves. It is proven that the mutual coupling between the plasmonic nano-antennas reduces significantly when the gap between two nano-antenna element approaches the SPP wavelength. The concept of Ultra-Massive MIMO communication with plasmonic

<sup>1</sup>M is the number of channels from which the source data originates. The data is generated from several low-rate streams.



**Figure 2.4:** A plasmonic nano-antenna array. The Figure is taken from Ref. [80] with permission to re-publish.

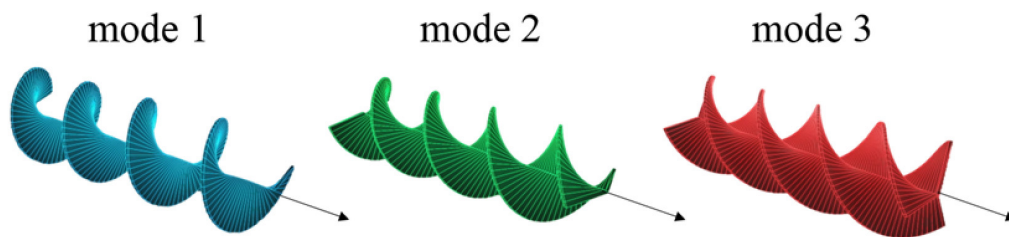
nano-antennas was suggested by Akyildiz, 2016 [80] and Nie *et al.*, 2019 [81]. For Ultra-Massive-MIMO systems, Akyildiz, 2016 [80] compute that they can embed  $1024 \times 1024$  nano-antenna array elements at 1 THz (in simulation) and the antenna arrays occupy just  $1 \text{ mm}^2$ . In a frequency band of  $1 \sim 10 \text{ THz}$ , several thousands of graphene-based plasmonic nano-antennas can be embedded in a few square millimeter areas.

All the demonstrator experiments discussed in the previous sub-section are using plasmonic technology and thus, depend on the high-speed electronics. Typically, the signal processing chain is as follows: an antenna receives the RF signal, the signal is amplified and converted to a baseband frequency with an electronic mixer. The electric signal is then converted to an optical signal by E-O modulators [82]. This is, where plasmonics can come into play. Plasmons are waves on metal surfaces. A charge carrier density wave directly below the metal surface creates an electrical field above the surface. The combination of the charge carrier wave and the electrical field wave is called surface plasmon polariton. On nanometric structures, surface plasmons radiate electromagnetic waves into air. Thus, plasmons enable a direct conversion from optical to electrical signal (i.e, baseband signal) and vice versa.

Salamin *et al.*, 2018 [71], developed a plasmonic mixer that directly maps the wireless information onto the optical signal (without RF-frontend). They demonstrated a direct wireless-to-optical receiver in a transparent optical link. A data rate of 20 Gbps was successfully transmitted across 1 m distance at an RF frequency of 60 GHz.

A demonstration of 36 Gbps data rate was performed by Ummethala *et al.* [83] at a 290 GHz with a wireless transmission distance of 16 m. Ummethala *et al.* performed an optical-wireless-optical link with purely optoelectronic frequency conversion at the THz transmitter and the THz receiver. A direct terahertz-to-optical conversion was utilized. The conversion was performed by an ultra-broadband silicon-plasmonic modulator having 3 dB bandwidth at 360 GHz. The conversion relies on photon-mixing in an uni-traveling carrier photodiode. Thus, plasmonic modulators are a powerful enablers for THz frontends [72, 84], as they do not require the up-down conversion performed by





**Figure 2.5:** An illustration of beams carrying different OAM modes. The Figure is taken from [62] with permission to re-publish.

RF-frontend circuits.

Electromagnetic phased arrays have been used in many applications like communication, radar, and astronomy at radio frequencies. The main issue of employing phased arrays at higher radio frequencies is deployment and scaling. However, a shorter optical wavelength is best suited for large-scale integration [85]. An optical antenna is a device for efficiently converting free optically propagating radiation to localized energy, and vice versa [86]. Sun *et al.*, 2013 [87], demonstrated a massive two-dimensional nano-phonic phased array (NPA) with  $64 \times 64$  (4096) optical nanoantennas that are densely integrated on a silicon chip with an area of  $576 \mu\text{m} \times 576 \mu\text{m}$ . Sun *et al.* show active phase tunability realized in the NPA by demonstrating dynamic steering with an  $8 \times 8$  array. Recently Calo *et al.*, 2018 [88], reported about an array of *plasmonic* Vivaldi antennas as a critical enabling component for on-chip optical wireless communication technology. The antennas have an in-plane maximum gain of 14.70 dB for an array with five antennas for on-chip point-to-point communication on an area of compact size of  $3.5 \mu\text{m} \times 8.7 \mu\text{m}$ .

The advantage of using plasmonic modulators for E-O/O-E conversion is that they avoid a complex RF-frontend chain. However, there is still a need to perform baseband processing of the signals coming to and from these E-O/O-E converters. Note that the optical signals which are down-converted to electrical signals have large bandwidth<sup>2</sup>. The baseband signal processing of the above down-converted signal purely by DSP requires high-speed data converters. Again, at this point, one needs a solution to perform signal processing operations, and mixed-signal processing techniques play a critically important role here.

## 2.3 OAM-MIMO

Current wireless communication is based on plane-electromagnetic (PE) waves. The momentum of an electromagnetic (EM) wave contains two parts, namely, spin angular momentum (SAM) and orbital angular momentum (OAM). SAM is associated with the polarization state of light. OAM describes the momentum of a helical wavefront by integer numbers. A flat wavefront has no OAM. If the wavefront is delayed by  $2\pi$  in

<sup>2</sup>A 290 GHz wireless THz frontend by Ummethala *et al.* [83] has a baseband bandwidth of 30 GHz.

$360^\circ$ , the OAM mode is 1, for  $2 \cdot 2\pi$  it is 2 and so on, as depicted in Fig. 2.5. The OAM has many different modes which are orthogonal (linearly independent) to each other and thus, can potentially be used as independent channels.

The potential applications of OAM have been in the focus of the wireless communication community for the past decade [89]. The orthogonality properties of OAM allow for an easy multiplexing/de-multiplexing of many modes resulting in a higher spectral efficiency. OAM opens up a novel multiple access method termed as Mode Division Multiple Access (MDMA), wherein users can employ different OAM-modes to transmit the data orthogonally. A detailed review of OAM for wireless communication was published by Cheng *et al.*, 2019 [90].

In hybrid systems combining spatial multiplexing and OAM multiplexing, Ren *et al.*, 2014 [91], achieved 16 Gbps (1-Gbaud symbol rate and 16-QAM was used) on a 28 GHz RF-carrier frequency. Yan *et al.*, 2016 [92] demonstrated a data-rate of 32 Gbps with 2-OAM modes on 60 GHz RF-carrier with a 16-QAM (2-Gbaud QAM symbol rate) data modulation. For point-to-point communication, Sasaki *et al.*, 2018 [62] demonstrated a data-rate of 120 Gbps. Here, they used an OAM-MIMO multiplexing system, with 5-OAM modes and 2-Gbaud symbol rate with a 256-QAM for the data modulation. The carrier frequency is the range of 27.5 – 29.5 GHz.

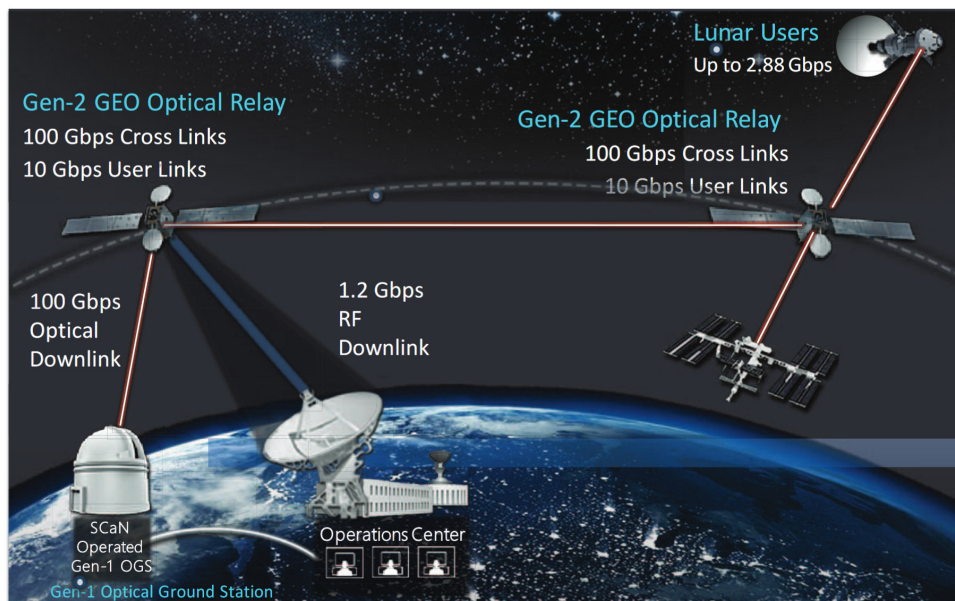
A combination of OAM-MIMO enables data rates above 100 Gbps. The use of MDMA along with the classical modulation schemes (QAM, QPSK) can already achieve very high data rates at 60 GHz RF frequency. Note that the symbol rate used is in the order of a few gigahertz. However, if we adapt the same techniques to the terahertz band, where large bandwidths are available, we could reach a data rate up to several hundred Gbps. This means, our baseband design techniques could be also applied in the case of OAM-MIMO transmission.

## 2.4 Free-space optical communication

Free space optical communication is a line-of-sight technology utilizing a laser to provide a directed beam in free space air, outer space, or vacuum to achieve wireless data transmission [94]. The operational wavelength for FSO communication is typically between 780 – 1600 nm, making use of E-O/O-E converters. The practical communication links involving FSO are deep-space probes, unmanned aerial vehicles (UAV), and high altitude platforms (HAP) as indicated in Ref. [95].

NASA's vision for *Next Generation Relay Constellation* in Geostationary Earth Orbit (GEO) is shown in Fig. 2.6. The system consists of two spacecrafts with 10 Gbps user service links, 100 Gbps optical downlink to the earth station and 100 Gbps cross-links between GEO satellites [93]. The 100 Gbps links between the GEO satellites will eliminate the need for ground stations, and all the traffic will be backhauled to an optical 100 Gbps link to the earth station.

A point-to-point FSO system was demonstrated by Wang *et al.*, 2018 [96] using a Violet



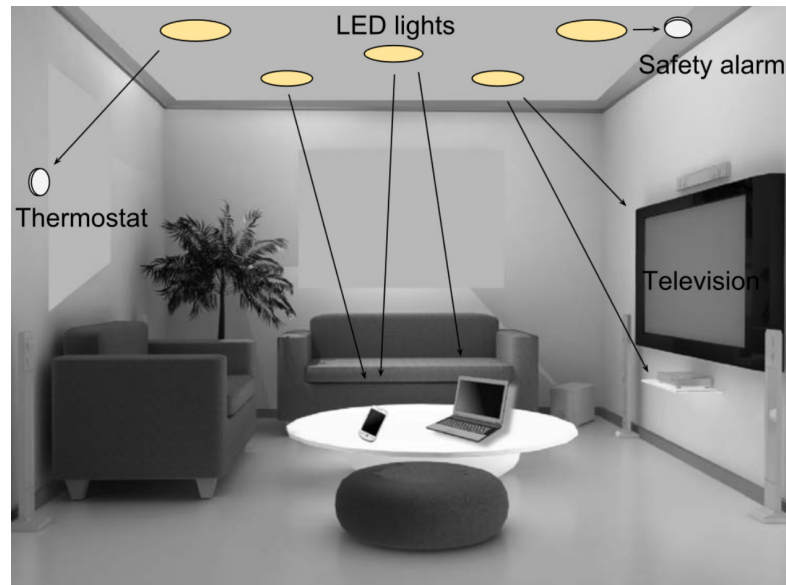
**Figure 2.6:** NASA's vision for free-space optical communication in GEO. The Figure is taken from Ref. [93].

Laser Diode (VLD). In this demonstrator system, direct encoding of a VLD signal is performed with a 64-QAM data stream for optical wireless communication with a distance of 10 m to reach a data-rate of 24 Gbps.

Space-division-multiplexing (SDM) is a suitable candidate to increase the spectral efficiency for free space optical communication systems as data-carrying beams can be transmitted at the same time in the medium [97]. Mode-division-multiplexing (MDM) is a sub-division of SDM in which data-carrying beams occupy different modes from many orthogonal modal basis sets [98]. Two orthogonal indices can describe the beam features. The beams originating from these orthogonal indices are named as Hermite–Gaussian (HG) beams and Laguerre–Gaussian (LG) beams. An HG beam can be characterized by planar  $(x, y)$  coordinates. An LG beam can be described by an azimuthal and radial directions [99]. Pang *et al.*, 2018 [100], demonstrated a 400 Gbps FSO link using QPSK modulation for both modal indices in HG/LG and with a free-space propagation distance of 1 m.

Robinson *et al.*, 2018 [101], plans to develop a direct optical link from Low-Earth Orbit (LEO) to ground station (with a distance range of 160 km to 1000 km) with data-rates up to 200 Gbps. The primary component of the whole architecture is a 100 Gbps fiber-coupled transceiver developed using *photonics technologies* that performs E-O/O-E conversion. The transmitted optical power was  $\approx 1$  W, transmitter lens diameter aperture was  $\approx 1$  cm, and receiver lens diameter aperture of a few 10's of centimeters.

FSO is particularly promising technique because it can achieve data rates greater than 100 Gbps, and more importantly, used for long distances (in the range of several hundred kilometers). A general factor to observe in the FSO method is that it fails to deliver a concrete solution for baseband processing operations. Again, here our mixed-signal



**Figure 2.7:** An example of a communication system setup using VLC. LEDs can communicate with various devices, including mobile phones and smart TV. The Figure is taken from Ref. [102].

processing approach to design baseband can be utilized.

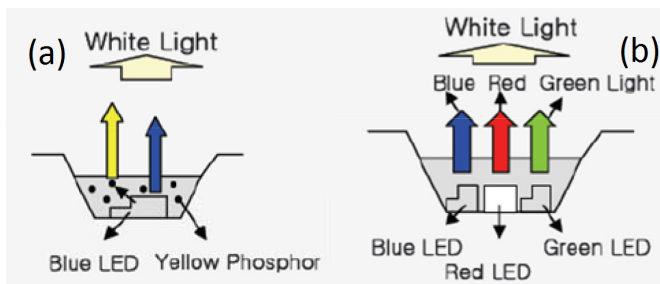
## 2.5 Visible Light Communication

The first concept of the VLC system was patented by Kamiya in 2002 [103]. In his work, he put forward the idea of using energy-efficient white Light-Emitting Diodes (LEDs) to transmit data. A research group from the Japanese Keio University [104–106] did an early investigation of VLC systems. They proposed the idea of using LEDs to build a home access network. Eventually, the Light Fidelity (Li-Fi) term was coined up, which is a VLC system capable of transmitting data at high speed in the visible light frequency range of 430 THz to 790 THz. The IEEE 802.15.7 standard [107] was created in 2011, which addresses the design specifications of the physical layer and the data-link layer for Li-Fi systems.

An indoor wireless unidirectional point-to-point communication scenario is illustrated in Fig. 2.7. The LEDs can be used to transmit data to various devices inside the room. The system can even coordinate itself to reduce the interference, enabling multi-point transmission to many smart devices.

A VLC transmitter consists of an LED luminaire. A LED luminaire consists of an LED light, ballast, housing, and a driver circuit. During the data transmission, the driver circuit controls the current flow through the LED to modulate the intensity of light emission. There are two types of VLC transmitter available to generate white light,

- **Blue LED + Phosphor:** The white light is generated with a blue LED having a yellow phosphor coating, as shown in Fig. 2.8(a).



**Figure 2.8:** Different types of LEDs used for data transmission: (a) shows the generation of white light by using blue LED and (b) shows the generation white light using three LEDs. The Figure is taken from Ref.[108].

- **RGB Sequence:** In this method, three LEDs, namely red, green, and blue, are used together to generate white light, as shown in Fig. 2.8(b).

In a VLC transmitter, the data cannot be encoded in phase and amplitude [109] like in a classical modulation system. Instead, the information has to be encoded in the varying intensity of the emitted white light wave. The data modulation scheme opted for VLC should satisfy the following two requirements: 1) It should not cause visible dimming [110] and 2) it should be able to mitigate the flickering effect [111]. The different modulation schemes used in VLC systems are as follows [107]:

- **OOK:** The data bits are transmitted by turning the LED to ON or OFF states.
- **Pulse Position Modulation (PPM):** In this scheme, the symbol duration is divided into  $t$  slots of equal length and position of the transmitted symbol.
- **Pulse Width Modulation (PWM):** In this method, the width of the pulses is adapted for the desired level of dimming while the pulses themselves carry the modulated signal in the form of a square wave.
- **Asymmetrically- Clipped Optical Orthogonal Frequency Division Modulation (ACO-OFDM):** In the above method, only odd sub-carriers are modulated, leading to asymmetric time-domain signal [112].
- **DC-biased Optical Orthogonal Frequency Division Modulation (DCO-OFDM):** In the above method, all the sub-carriers are modulated, and an additional positive direct current is added to make the signal unipolar [104, 113].
- **Color Shift Keying (CSK):** The white light is generated using three separate LEDs, namely, Red, Green, and Blue. A CSK method modulates the signal using the intensity of these three colors to transmit the information [107, 114].
- **CAP:** In this method, the QAM signal is generated by combining two PAM signals passing through a filter and thus resulting in Hilbert pair [115].

There are two types of VLC receivers used to decode the transmitted signal:

- **Photodetector:** A semiconductor device that converts the received light into a current. The data rates could be in the range of tens of gigahertz.
- **Camera sensor:** Camera sensors are available in most of the mobile phones. Using camera sensors as a receiver has the potential to convert every portable device to a VLC receiver. The data rate is low as it is limited by the number of frames per second (fps) captured by a mobile camera (usually less than 40 fps).

A hybrid FSO/VLC system with a 10-CAP modulation was demonstrated by Pesek *et al.*, 2019 [116]. Their system achieved a data-rate of 12.6 Mbps in a 3 m link. Quintana *et al.* [117] realized an ultra-wide coverage of a VLC system using mechanical beam steering at the transmitter terminal with a fluorescent optical concentrate at the receiver. The transmitter and the receiver had a full field view of 100° and 120°, respectively. The system performed at a data-rate of 300 Mbps with OOK modulation. Yeh *et al.*, 2019 [118], demonstrated for the first time a data rate of 1.25 Gbps with OOK modulation in free-space transmission over 150 cm. A white-light-phosphor laser diode at 460 nm was used at the transmitter and an optical filter at the receiver.

Tsonev *et al.*, 2014 [119], demonstrated 3 Gbps data-rate using a 50  $\mu\text{m}$  single gallium nitride LED with Orthogonal Frequency Division Modulation (OFDM) modulation at a distance of 5 cm. Using four LEDs sources (green, blue, yellow, and red), Wang *et al.*, 2015 [120], achieved 8 Gbps data-rate over a 1 m wireless channel with 16-CAP modulation. Ferreira *et al.*, 2016 [121], applied an array of micro-LEDs along with DCO-OFDM (using 512 sub-carriers) modulation to achieve 5.37 Gbps data rate over a 0.75 m wireless channel.

A spatial multiplexing concept was applied by Mesleh *et al.* [122] to perform MIMO-VLCs, and it relies only on spatial domain symbols. Rajbhandari *et al.*, 2017 [123], demonstrated a  $2 \times 2$  MIMO link with 50 cm free space showing a data rate of 6.95 Gbps with Pulse-amplitude modulation (PAM)-8 modulation.

As discussed in this Section, VLC is a promising technology to achieve 100 Gbps as its transceiver components are readily available. Here, the PSSS modulation can be applied for example in the context of “CSK” modulation, which can be mapped over the range of RGB colors.

The main disadvantage all VLC systems is that the back-channel has to be separately designed. The additional challenges of VLC systems are atmospheric absorption, beam dispersion, interference from the background light sources, requires “line of sight” channel, aperture of the receiver [124].

## 2.6 Comparison of technologies

We compare the different technologies in the Tab. 2.1, and observe which of those Key-Performance-Indicators (KPIs) like bandwidth, data rate, wireless distance covered, energy efficiency, and spectral efficiency are met. In Tab. 2.1, we notice two clear ways

**Table 2.1:** KPIs comparison.

	<b>Direct THz modulation</b> [51]	Photonics [73]	Plasmonics [83]	OAM-MIMO [62]	FSO [100]	VLC [120]
Data rate (Gbps)	100	224	36	120	400	8
Wireless distance (m)	1	1.5	16	10	1	1
Energy efficiency (pJ bit <sup>-1</sup> )	14	-	-	-	-	-
Spectral efficiency (bit/s/Hz)	4	16	2	60	8	25
Bandwidth (GHz)	26	14	18	2	50	0.32

to achieve a data rate above 100 Gbps: either you choose a high spectral efficiency which is associated with a lower bandwidth or the other way around. E.g., in “OAM-MIMO”, a bandwidth of 2 GHz with a spectral efficiency of 60 bit/sec/Hz leads to a data rate of 120 Gbps. And in “Direct THz modulation” (RF-frontend used in our Real100G.COM project), we have huge bandwidth of 26 GHz and with a moderate spectral efficiency of 4 bit/sec/Hz that results in 100 Gbps. Another important point to note is that most of the systems mentioned do not give any data about energy efficiency except the RF-frontend transceiver modules used in “Direct THz modulation”<sup>3</sup> [51].

## 2.7 Summary

Most of the above described demonstration systems use AWG for the signal generation at the transmitter and DSA for recording the signal at the receiver. None of the above-mentioned approaches addresses the complete wireless system which includes baseband processing operations like synchronization, real-time demodulation of the received data, channel equalization, and the generation of a baseband signal for the transmitter to achieve 100 Gbps.

We aim for a complete system that is capable of realizing 100 Gbps. We need a system that includes all necessary baseband processing features like modulation/de-modulation, synchronization, channel equalization, automatic gain control, and so on. Here, PSSS modulation is one of the possible solutions within the complete design space.

<sup>3</sup>LO circuitry is not considered. Also, the baseband circuit. The above value is only for transmitter and receiver frontend modules.

## Chapter 3

# Towards PSSS technology

In this Chapter, we give a brief introduction to the core components involved in building a complete PSSS system. The basics of spread spectrum techniques and spreading codes are introduced. A mathematical analysis of PSSS encoding and decoding is performed. Then, we introduce a “PSSS system model”, where the PSSS transceiver components are described. Finally, we discuss the synchronization, the channel estimation, and the channel equalization methods employed in PSSS systems.

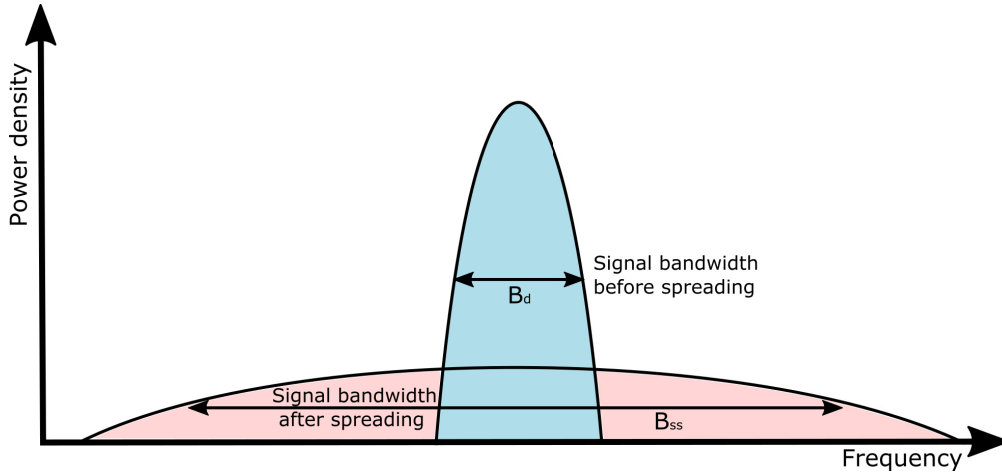
### 3.1 Spread Spectrum techniques

Spread spectrum techniques were developed already in the 1950s by both the U.S. and the U.S.S.R. military for communications and guidance systems, among others. The main advantages of spread spectrum techniques are the strong anti-jamming and anti-interference capacities [125]. Spread spectrum techniques are defined as follows by Ref. [126]:

“Spread spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum necessary to send the information; the band spread is accomplished by means of a code which is independent of the data, and a synchronized reception with the code at the receiver is used for despreading and subsequent data recovery.”

The signal is typically spread by a noise-like sequence. This makes the signal detection and interception very difficult without knowing the spreading code sequence. This offers an additional layer of privacy. In a spread spectrum system [127], the transmitted signal is spread over a large frequency band, which is much wider than the minimum bandwidth required to transmit the information (s. Fig. 3.1). The amount of performance improvement gained by spreading the signal is defined by a processing gain (PG). The PG of a spread spectrum is the ratio of the spreading bandwidth  $B_{ss}$  to the required





**Figure 3.1:** Power spectral density after direct sequence spreading.

signal bandwidth  $B_d$  [128],

$$PG \cong \frac{B_{ss}}{B_d}. \quad (3.1)$$

As illustrated in Fig. 3.1, the spreading technique requires a transmission bandwidth much greater than the signal bandwidth. We observe that the amplitude of the signal after spreading is smaller compared to the original signal. The spreading is performed such that the total transmitted energy remains the same, i.e., the integral over the original signal and the spreaded signal is identical. In UWB technologies (e.g., IEEE 802.15.4a Standard [129]), the spectral-power after spreading is limited to 40 dBm/MHz.

### 3.1.1 DSSS

PG is can also be expressed by the ratio of the height of the autocorrelation peak to the maximum side-lobe. Let us denote this ratio as  $A$ , then the processing gain (PG) in dB is,

$$PG = 10 \cdot \log_{10}(A). \quad (3.2)$$

As Barker codes possess an especially high “autocorrelation” property, the maximal achievable autocorrelation factor  $A$  is the same as the spreading code sequence length  $N$ . The processing gain depends on the kind of code, e.g., Gold codes, m-sequences, etc. For all other codes, except Barker codes, the  $A < N$ . This is the reason that Barker codes have been introduced for IEEE 802.11b because the processing gain is  $PG = 10 \cdot \log_{10}(11) = 10.4$  dB for a Barker code of length 11.

Figure 3.2 shows the modulation and demodulation of a standard Direct Sequence Spread Spectrum (DSSS) system. At the transmitter, the input data bits are first modulated by a standard scheme (e.g., PAM, QAM). After-wards, each of the symbols is multiplied by a spreading code, which is typically a pseudo-noise sequence. Normally, this pseudo-noise sequence is a Barker code of length 5, 7, 11, or 13. In a different application, if more processing gain is required, m-sequences or Gold codes are used, because Barker codes exist up to only a length of 13. If we use m-sequences or Gold

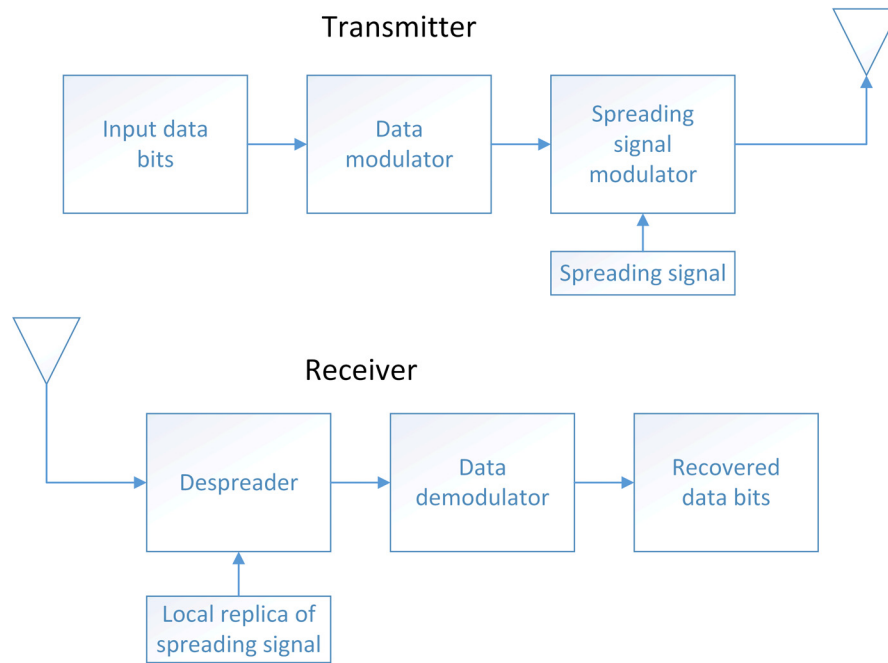


Figure 3.2: DSSS: modulation and demodulation.

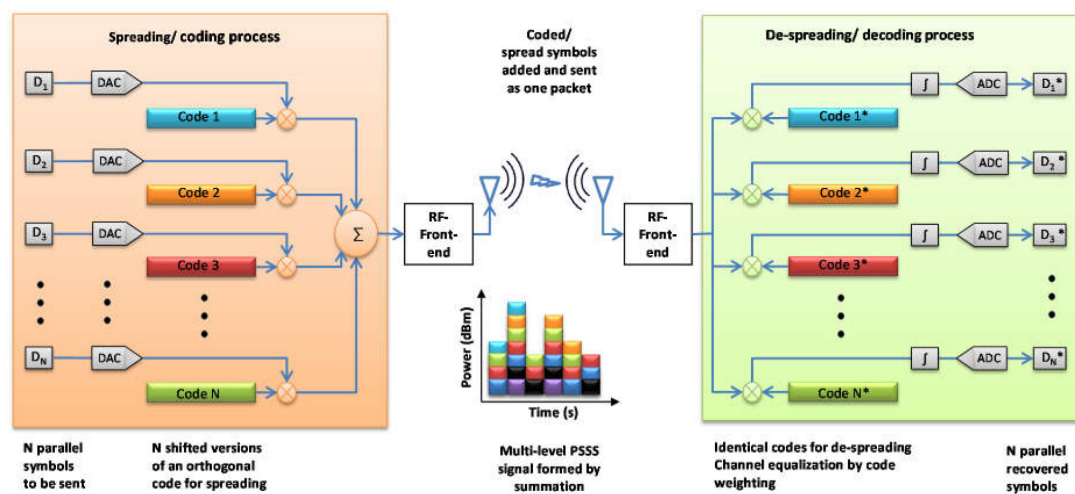


Figure 3.3: PSSS encoding and decoding. This Figure is taken from our article [49].

codes of a length  $> 100$ , it leads to a processing gain above  $> 30$  dB.

At the receiver, the incoming signal is demodulated by multiplication with a local replica of the spreading signal. This output signal is fed to a threshold detector to recover the original bits. In this way, the original narrow-band message signal is recovered.

### 3.1.2 PSSS

This Thesis focuses on “Parallel Sequence Spread Spectrum (PSSS)”, which uses  $m$ -sequences to perform encoding and decoding. PSSS is one of the PHY layer schemes for the IEEE 802.15.4 WPAN standard [130, 131].

In a PSSS transmitter,  $N$  parallel symbols  $D_1$  to  $D_N$  are encoded with  $N$  orthogonal

codes<sup>1</sup> and summed up to form a multi-level signal at the output of the PSSS encoder as depicted in Fig. 3.3. These signals are up-converted to Radio Frequency (RF), transmitted over the radio channel, and down-converted back to baseband at the receiver. The receiver cross-correlates the PSSS baseband signal with  $N$  known orthogonal PSSS codes and recovers the transmitted data symbols  $D_1$  to  $D_N$ . The IDC is used to perform the cross-correlation operations. Let us go through the reconstruction of the  $D_1$  symbol at the receiver: The received PSSS signal is multiplied with the known code sequence “Code 1”, and this result is passed to the “integrator”. The integration is performed over one PSSS symbol period. The output of the integrator is fed to the ADC. Then, the ADC recovers the  $D_1^*$  symbol as in Fig. 3.3.

In a time-span of one PSSS symbol, the above-described operation is performed in parallel to recover the data symbols  $D_1$  to  $D_N$ . Now, we notice that the ADCs boundary<sup>2</sup> is shifted from the RF-frontend to the point after the cross-correlation operations (performed by IDC). It is also clear that to recover the data symbols  $D_1$  to  $D_N$ , we require  $N$  ADCs operating at the PSSS symbol rate. Let us take an example system. To achieve a data rate of 100 Gbps, we need a signal bandwidth of 25 GHz and a bit spectral efficiency of 4 bit/s/Hz. If we use standard modulation schemes (for e.g., QAM-16), then ADC should at least have a sampling rate of 50 GS/s (according to Nyquist) and a resolution of 4 bits. But if we use PSSS encoding with PAM-16 ( $N = 15$ ), the ADCs needs to operate at a sampling rate of 1.67 GS/s<sup>3</sup> and a resolution of 4 bits. Another factor contributing to the low ADC sampling rate is the “coherence time”. We assume that the coherence time of the transmission channel is very long compared to the symbol duration. Thus, we can realize a part of signal processing operations required for channel equalization in the digital domain.

The complete spreading-/coding process in the transmitter and the despreading-/decoding process in the receiver can be implemented very efficiently in the analog domain using dynamic analog circuitry, such as analog multipliers, adders, and integrators. Important advantages of mixed-signal implementation are the reduced speed requirements for the data converters, the high-speed, and a short transistor count [132]. In a mixed-signal PSSS baseband system as depicted in Fig. 3.3,  $N$  parallel DACs and ADCs are utilized to operate at a sampling frequency equal to the symbol rate.

The complete digital implementation of a PSSS system requires a high DAC and ADC bit resolution to process the encoded PSSS signal. The data converters have to operate with a sampling frequency of at least the Nyquist rate, i.e.,  $2\times$  the PSSS signal bandwidth. In contrast to a digital implementation of PSSS systems, which requires a fully digital PSSS transceiver, we assume that a mixed-signal implementation requires less hardware and is more energy-efficient.

A further advantage of a mixed-signal PSSS transceiver is that an adaptive equalization

<sup>1</sup>Two codes are defined to be orthogonal if the cross-correlation property is 0 i.e. if the scalar product of the code-vectors is 0.

<sup>2</sup>Normally in communication systems, the ADCs are located right after RF-frontend.

<sup>3</sup>Assuming we have chip rate of 25 Gcps and m-sequence of length 15,  $\frac{\text{chip-rate}}{m\text{-seq}} = \frac{25 \times 10^9}{15} = 1.67 \text{ GS/s}$ .

of the received signal can be implemented in the despreading/decoding process [133] as a cross-correlation-based equalization. Decoding the received signal with a replica of a distorted PSSS code, we obtain a perfect correlation result, effectively compensating for the non-ideal channel impulse response. A similar equalizer was proposed for a DSSS system (i.e., Code Division Multiple Access (CDMA) downlink) where it was shown that it outperforms the Rake receiver [134]. The cross-correlation based equalization from Ref. [133] is very attractive since it can be implemented as a mixed-signal equalizer that performs spread-spectrum decoding and equalization in a single step.

## 3.2 Spreading Codes

An essential component of any spread spectrum system is the pseudo-random spreading code. “Ideal spreading codes” for data transmission have a delta function as an autocorrelation and zeroes as a cross-correlation. The ideal spreading code would be an infinite sequence of likely random binary digits. The implementation of such a spreading code would require unlimited memory at both the transmitter and receiver side, which is not a practical option. Thus, we use sub-optimal pseudorandom noise (PRN) codes that look like random noise and satisfy the standard test for statistical randomness. There exist many practical ways to evaluate the randomness test for a code sequence. These tests are either based on statistical tests, transforms, or complexity tests [135]. A few examples of statistical-based tests are the Wald–Wolfowitz test [136], and the Diehard tests [137].

For data transmission, we are looking for sequences that have good auto-correlation properties (a clear peak without side-lobes, s. Fig. 3.5) and low cross-correlation properties (i.e., orthogonality of different sequences). In the following section, we describe the generation and the correlation properties of Maximum Length Sequences (MLSs) and Kasami sequences since they were used in our experimental work (s. Chap. 6).

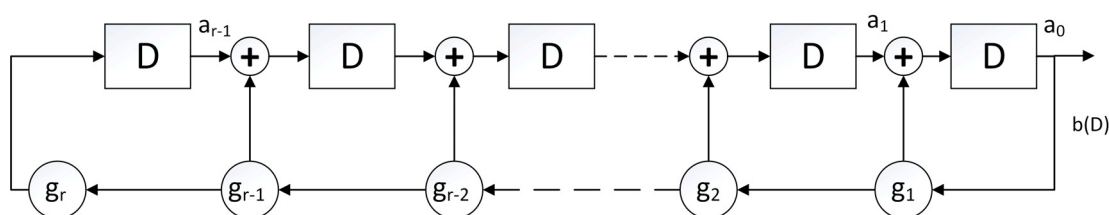
### 3.2.1 Pseudorandom sequences

PRN sequences have the following properties [126],

1. *Easy to generate:* Here, we mean that the chosen code must be easy to generate in the hardware.
2. *Satisfy randomness properties:* It should satisfy one of the pseudo-randomness tests mentioned in previous section.
3. *Posses longer periods:* This means that the chosen PRN sequence will be able to generate a longer spreading codes. For example, Barker codes are restricted up to code sequence length of 13, but an m-sequence can have longer sequence length. A longer sequence length leads to more processing gain.

**Table 3.1:** Code comparison.

Different codes	Property 1	Property 2	Property 3	Property 4	Property 5
m-sequences	Yes	Yes	Yes	Yes	No
Kasami codes	Moderate complexity	Yes	Yes	Acceptable	Yes
Gold codes	Moderate complexity	Yes	Yes	Yes	No
Walsh Hadamard codes	Moderate complexity	Yes	Yes	No	Yes

**Figure 3.4:** Configuration of a LFSR for the generation of  $m$ -sequences.

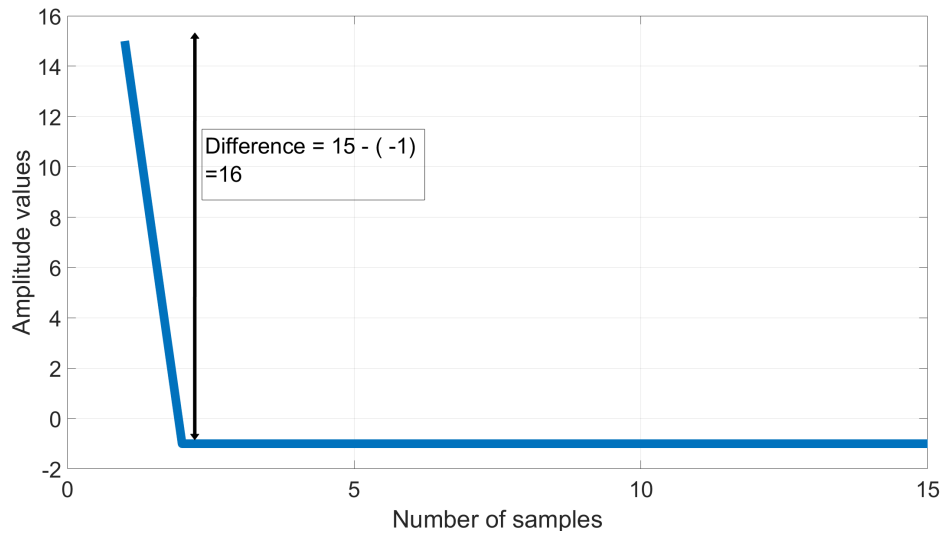
4. *Autocorrelation properties:* The chosen code should have a good autocorrelation function, i.e., the codes should have a delta function as their autocorrelation function.
5. *Cross-correlation properties:* The chosen code should have a good cross-correlation function, i.e., the codes should have 0 as their cross-correlation function.

The Tab. 3.1 compares the above-described properties for different codes. In Tab. 3.1, by “Moderate complexity”, we refer to the hardware complexity of the chosen code in comparison to the hardware effort required to generate m-sequence. We know for a fact that m-sequences are easy to construct using linear-feedback shift register (LFSR). The other term is “Acceptable” means that the correlation properties of the chosen code in comparison to the “ideal spreading codes”.

As we can see in Tab. 3.1, m-sequences satisfy most of the properties mentioned above except for cross-correlation. Kasami codes fulfill both acceptable autocorrelation and cross-correlation properties, which is an important basis for the data transmission using I/Q channel. Thus, we have selected m-sequences and Kasami codes.

### 3.2.2 m-Sequences

The length of a m-sequence ( $N$ ) depends on the coefficient values (or feedback taps)  $g_r$  as depicted in Fig. 3.4. The MLS, or  $m$ -sequences, are simple to generate with a LFSR as shown in Fig. 3.4. Each square box represents a 1-bit memory for a binary digit, and the symbol  $D$  stands for the delay of the chip time  $T_c$ , and the summing circles stand



**Figure 3.5:** Cyclic autocorrelation of an  $m$ -sequence of length 15.

for the binary modulo-2 sum. The connection circles with a label  $g_i$  are either closed or open depending on the generator polynomial  $g_r g_{r-1} \dots g_1$ . 1 implies that the connection is closed, and 0 that the connection is open. Here,  $b(D)$  indicates the output values, and  $a_{r-1}$  is the one clock cycle delayed version of  $g_r$ .

The generator polynomial is typically a primitive polynomial, which belongs to a group of prime polynomials. A detailed mathematical description of primitive polynomials is given in Ref. [138]. Every LFSR with a primitive polynomial can be used to generate a  $m$ -sequence. For a given primitive polynomial degree  $r$ , the number of primitive polynomials  $N_p$  [138, p. 117] is given by:

$$N_P = \frac{2^r - 1}{r} \prod_{i=1}^J \frac{p_i - 1}{p_i}, \quad (3.3)$$

where  $p_i$  is the prime factor of  $2^r - 1$ . E.g., to generate a  $m$ -sequence of length 15, we have  $r = 4$ . The prime factors of  $2^4 - 1$  are 3 and 5. Thus, the number of primitive polynomials is

$$N_P = \frac{2^4 - 1}{4} \left( \frac{5 - 1}{5} \right) \left( \frac{3 - 1}{3} \right) = 2. \quad (3.4)$$

For a primitive polynomial of degree  $r$ , the length  $N$  of the  $m$ -sequence is  $2^r - 1$ . For a MLS-15, those primitive polynomials are  $D^4 + D^1 + 1$  and  $D^4 + D^3 + 1$  ([138, p. 121]).

### Properties of $m$ -sequences

A maximum length sequence of degree  $r$  has a cyclic period of  $2^r - 1$ . If we have a  $m$ -sequence length of period 15 ( $2^4 - 1$ ), the sequence output will have the following values consisting of 1's and 0's: 1 0 0 0 1 1 1 1 0 1 0 1 1 0 0 provided the initial content of 4-shift registers (s. Fig. 3.4) is 1 0 0 0. An important property of MLS sequences is that they have good auto-correlation properties. Fig. 3.5 shows the cyclic auto-correlation of

an MLS-15, which is also described in Eqn.(3.5). The difference between the maximum peak and the lowest peak is 12.05 dB (from Eqn. (3.2)).

The properties of *m-sequences* are listed in the following:

1. An MLS contains one more 1 than 0. The number of ones in the sequence is  $\frac{1}{2}(N + 1)$ , where  $N$  is the length of the m-sequence.
2. The modulo-2 sum of an m-sequence and any phase shift of the same m-sequence is another phase of the same m-sequence (shift-and-add property).
3. If a window of width  $r$  is slid along an m-sequence for  $L$  shifts, each  $r$ -tuple except the all-zeros  $r$ -tuple will appear exactly once.
4. The periodic autocorrelation function  $\theta_b(k)$  is two-valued and described by:

$$\theta_b(k) = \begin{cases} 1.0, & \forall k = lN \\ -\frac{1}{N}, & \forall k \neq lN \end{cases} \quad (3.5)$$

where  $n$  is an integer and  $N$  is the sequence period or the length of the MLS. This property is used for the data transmission by using all the shifted version of m-sequences.

The autocorrelation function of a *m-sequence* almost resembles the delta function (s. Fig. 3.5), which makes it robust against a time offset. This property is utilized in PSSS modulation. M-sequences are the base codes for PSSS modulation. E.g., if we take a m-sequence of length 15 ( $N = 15$ ), we have 15 different cyclically shifted codes available. If we perform the autocorrelation between any two cyclically shifted codes, the result is a single peak (according to Eqn. (3.5)). Nevertheless, the cross-correlation of two *m-sequences* tends to be substantial, which is not an optimal property for the data transmission on I/Q channels of the transmitter. So we propose to use Kasami codes for data transmission on I/Q channels.

### 3.2.3 Kasami codes

Kasami codes have acceptable autocorrelation properties and good cross-correlation properties when compared to *m-sequences*. Thus, they have correlation functions close to “ideal codes”. Kasami code families are constructed from MLSs. Kasami sequence sets are one of the most often used types of binary sequence sets because of their low cross-correlation [139–141].

The cross-correlation is a measure for the similarity between two sequences as a function of the displacement of one sequence relative to the other. Low cross-correlation values imply that two sequences are not similar to each other. Thus, the above property is useful to separate the data sent on the I/Q channels of the transmitter. The cross-correlation

function of any two sequences  $x$  and  $y$  of length  $L$  is given by

$$R_c(n) = \sum_{k=0}^{N-1} x(k) \times y(n-k). \quad (3.6)$$

Ideally, we want to have a cross-correlation value of 0. This cannot be achieved in reality. *Welch's lower bound* sets a mathematical lower limit to the cross-correlation value of the chosen sequences. There are two sets of Kasami sequences: the small set and the large set. The small set of sequences is optimal in a sense that it has the lowest cross-correlation matching to Welch's lower bound [142]. Welch's bound is a lower bound on the total inner product of any set of sequences with an identical energy. A more detailed mathematical analysis is given in Ref. [143]. For a  $m$ -sequence with a period of  $N = 2^r - 1$ , where  $r$  is non-negative even integer, let  $u$  be a binary sequence of length  $N$ , and the sequence  $w$  is obtained by decimating  $u$  by  $2^{r/2} + 1$ . The small set Kasami sequences is described by [139],

$$K_s(u, n, m) = \begin{cases} u & m = -1 \\ u \oplus T^m w & m = 0, \dots, 2^{r/2} - 2 \end{cases} \quad (3.7)$$

Wherein  $T$  is the left shift operator,  $m$  is the shift parameter for  $w$ ,  $\oplus$  is an addition under modulo-2 and  $K_s$  is a small set Kasami sequence. The small set of Kasami sequences contains  $2^{r/2}$  sequences.

The small set of Kasami codes takes the cross-correlation values of  $-1, R_c, (R_c - 2)$  and  $R_c$  is taken from Ref. [139],

$$R_c = 1 + 2^{r/2}. \quad (3.8)$$

Let us consider an example for  $r = 4$ . Then we have a Kasami sequence of length  $N = 15$ . The small set of Kasami codes contains  $2^{4/2}$  unique different sequences which are periodic over a length of 15. These sequence are shown in Eqn. (3.9),

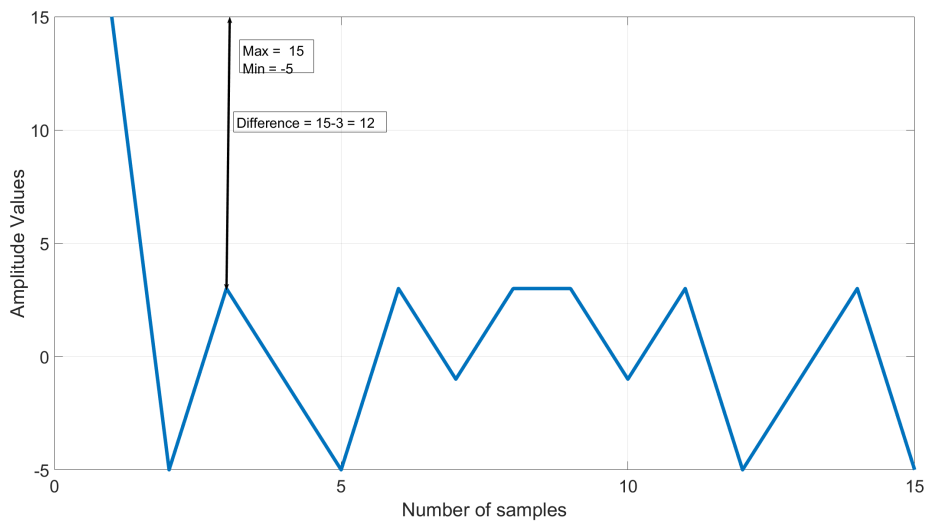
$$\begin{aligned} \text{Seq 1} &= [0\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 1\ 0\ 1\ 1\ 1\ 1]; \\ \text{Seq 2} &= [1\ 1\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1]; \\ \text{Seq 3} &= [0\ 1\ 1\ 1\ 1\ 1\ 1\ 0\ 1\ 1\ 1\ 0\ 1\ 0\ 0]; \\ \text{Seq 4} &= [1\ 0\ 1\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 0\ 0\ 1\ 0]. \end{aligned} \quad (3.9)$$

Since Kasami sequences are constructed by decimating  $m$ -sequences, Seq. 1 in Eqn. (3.9) is a  $m$ -sequence of length 15. To implement I-Q encoding, Seq. 1 is used to encode the I-Channel and Seq. 2 is used to encode the Q-Channel (s. Eqn. (3.9)).

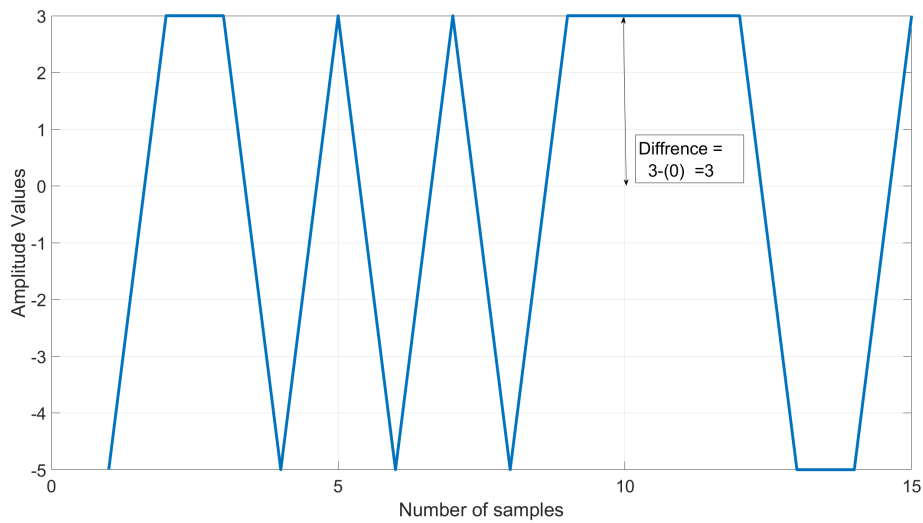
Figure 3.6 shows the cyclic auto-correlation of Seq. 2 as described in Eqn. (3.9). The difference between the maximum peak and the lowest value is 10.8 dB (from Eqn. (3.2)). The figures 3.5 and 3.6 show a reduced performance in the auto-correlation of 1.25 dB (12.05 – 10.8) for Kasami codes compared to  $m$ -sequences.

For the implementation of an I-Q system with a spreading code, it is desirable to have a very low cross-correlation between the codes used for the different channels to prevent





**Figure 3.6:** Cyclic autocorrelation of a Kasami sequence.



**Figure 3.7:** Cyclic cross-correlation of a Kasami sequence.

interference between both channels. Figure 3.7 shows the cross-correlation between Seq. 1 and Seq. 2, and takes the values as described in Eqn. (3.8). In Fig. 3.7, the maximum amplitude is 3 which is 4.8 dB (from Eqn. (3.2)).

To summarize, the advantages of using Kasami codes are:

- The cross-correlation property helps in the implementation of an I–Q transmission system.
- The “Acceptable” autocorrelation properties are employed for data transmission. E.g., Seq. 1 can be used to code the I-channel and Seq. 2 for the coding of the Q-channel. Moreover, the side-lobes that occur due to the non-ideal autocorrelation properties (as seen in Fig. 3.6) can be compensated using channel equalization.

- The I–Q cross-leakage that occurs at the receiver during down-conversion can be minimized since the I–Q channels are separated in the code domain.

### 3.3 PSSS Analysis

In this Section, we present an analytical analysis of the PSSS modulation scheme. We address the following topics:

- A mathematical model of PSSS including a PSSS-specific channel deconvolution method.
- The probability distribution of the discrete multi-levels of the PSSS-encoded signal.
- The effect of clipping the highest and the lowest values of the PSSS multilevel distribution.

The PSSS modulation is performed by a multiplication of the encoding matrix with the PAM modulated data string. The encoding matrix consists of cyclically shifted *m-sequences*. The introduction to *m-sequences* was given in the previous section Sec. 3.2.1. The PSSS modulation procedure is described in Sec. 3.1.2.

#### 3.3.1 Mathematical introduction of PSSS

PSSS uses orthogonal *m-sequences* in parallel. Equation (3.10) describes the base *m-sequence* denoted as  $ms_1$ ,

$$ms_1 = (C_1, C_2, C_3, \dots, C_N), \text{ with } C_i \in [-1, 1]. \quad (3.10)$$

The value  $N$  in Eqn. (3.10) is the length of the *m-sequence*. The sequence  $ms_1$  is the base *m-sequence*. The data input is described by a vector  $\vec{D}$  of length  $N$ :

$$\vec{D} = \begin{bmatrix} d_1 \\ d_2 \\ \cdot \\ \cdot \\ d_N \end{bmatrix}. \quad (3.11)$$

where  $d_i \in [-1, 1]$  for a bit loading of 1 bit,  $d_i \in [-3, -1, 1, 3]$  for a bit loading of 2 bits and  $d_i \in [-15, -13, -11, \dots, 15]$  for a bit loading of 4 bits. For a bit loading of 1-bit, the total number of possible data symbols ( $L$ ) is 2; a bit loading of 2-bits results in a total number of possible data symbols ( $L$ ) of 4; for bit loading of 4-bits we have a total number of possible data symbols ( $L$ ) of 16. This can be logically associated with PAM, e.g., in a PAM-16 modulation, one data symbol represents 4 bits. We transform the raw binary data bits to PAM symbols, and then we use those PAM symbols to achieve a spreading by the PSSS encoding.

Each element in one PSSS symbol  $\vec{S}$  contains information about all encoded bits of the data vector  $\vec{D}$ . The effect is that the information of the data values  $d_i$  is distributed along the one complete PSSS symbol vector  $\vec{S}$ . This is the effect of parallel spreading, e.g., one PSSS symbol of an m-sequence length  $N$  with a bit loading of 1 bit contains  $(N \times 1)$  bits, and one PSSS symbol of an m-sequence length  $N$  with a bit loading of 4 bits contains  $(N \times 4)$  bits.

The PSSS symbol  $\vec{S}$  is given by the input data encoded via matrix multiplication by the encoding matrix:

$$\vec{S} = C \times \vec{D}. \quad (3.12)$$

Equation (3.13) shows the PSSS encoding matrix. The rows in the encoding matrix  $C$  contain cyclic permutations of the base *m-sequence*  $ms_1$  (s. Eqn. (3.10)) of length  $N$  which forms the encoding matrix.

$$C = \begin{pmatrix} C_1 & \dots & C_N \\ \vdots & \ddots & \vdots \\ C_2 & \dots & C_1 \end{pmatrix}, \text{ with } C_i \in [-1, 1]. \quad (3.13)$$

The PSSS symbols of the vector  $\vec{S}$  are transmitted sequentially in air. The decoding of the PSSS symbols can be done by a cyclic correlation of the PSSS symbol vector  $\vec{S}$  with the base *m-sequence*  $ms_1$ . This operation is similar to a multiplication by the decoding matrix  $DE$  (as in Eqn. (3.14)) with the PSSS symbol vector  $\vec{S}$  resulting in Eqn. (3.15):

$$DE = C^T, \quad (3.14)$$

$$C\vec{C}F = DE \cdot \vec{S}. \quad (3.15)$$

The entries  $d'_n(ccf_n)$  in vector  $C\vec{C}F$  are the reconstructed PAM symbols.

### Channel Deconvolution

We define an “effective channel” that includes the impairments caused by the physical channel and the RF-frontend electronics. Channel deconvolution is a process where channel impairments occurring due to multipath propagation and RF-impairments are compensated.  $\vec{H}$  represents the channel response in time domain. The PSSS symbol  $\vec{S}$  convolved by the channel response  $\vec{H}$  results in  $\vec{G}'$ , which is the received PSSS symbol and  $\otimes$  represents a cyclic convolution in the time domain:

$$\vec{G}' = \vec{S} \otimes \vec{H}. \quad (3.16)$$

$ms_1^{-1}$  is the time-inverted sequence of (3.10) and is used as an initial correlation reference.  $C\vec{C}F'$  is the cyclic convolution of  $\vec{G}'$  with  $ms_1^{-1}$ .  $C\vec{C}F'$  as evaluated in Eqn. (3.17) does

not compensate for multipath effects and RF-impairment losses:

$$CCF' = \vec{G}' \circledast ms_1^{-1}. \quad (3.17)$$

$H^{-1}$  is the inverse channel response in time domain and by convolving it with  $ms_1^{-1}$  we obtain  $ms_{1\_new}^{-1}$  as new correlation reference as shown in (3.18),

$$ms_{1\_new}^{-1} = H^{-1} \circledast ms_1^{-1}. \quad (3.18)$$

$CCF'_{new}$  is the cyclic convolution of  $G'$  with  $ms_{1\_new}^{-1}$  as described in Eqn. (3.19).  $CCF'_{new}$  compensates for multipath effects and RF-impairment losses.

$$CCF'_{new} = \vec{G}' \circledast ms_{1\_new}^{-1}. \quad (3.19)$$

Thus,  $CCF'_{new}$  is used for the reconstruction of data bits. A new decoding reference  $ms_{1\_new}^{-1}$  is computed only, when the channel changes.

### 3.3.2 BER curves with PSSS

There are four options for choosing a PSSS encoding and decoding matrix. The first option is a bipolar encoding matrix used at the transmitter, wherein the entries of the coding matrix (as in Eqn. (3.13)) are  $-1$  and  $+1$  and a unipolar decoding matrix is used at the receiver, wherein the listings of the decoding matrix are  $1$  and  $0$ . In this case, the decoding matrix is the inverse of the encoding matrix. This results in an ideal autocorrelation function as described in the Sec. 3.2.1 and in Fig. 3.5.

The second option is to use a bipolar encoding matrix and a bipolar decoding matrix. This combination leads to an increase of the autocorrelation peak height and thus to a BER close to the BPSK error rate. This is a 3 dB gain compared to the combination bipolar-unipolar. Since the decoding matrix is not the inverse of the encoding matrix, the autocorrelation is not ideal. For short m-sequences, this leads to an increased BER compared to the ideal BPSK error rate. Hence, this option is not preferred.

The third option is to use a unipolar encoding matrix and a unipolar decoding matrix. This mixture results in a loss of the 3 dB gain while decoding at the receiver<sup>4</sup>, and also the decoding matrix is not the inverse of the encoding matrix. Thus, this option is not preferred.

The last option is to use a unipolar encoding matrix and a bipolar decoding matrix. This combination leads to an increase in the dynamic range of integrators. An IDC is used to realize the correlation operation. Besides, we need to shift the mean value (DC offset) of the decoding matrix to retrieve the transmitted data. Thus, this option is also not preferred.

As depicted in Fig. 3.8, the data bits are modulated with  $M^{\text{th}}$  order PAM followed by

<sup>4</sup>The autocorrelation peak height reduces by 3 dB. In Fig. 3.5, we have used a bipolar encoding matrix and unipolar decoding matrix, and this results in an autocorrelation value of 12.05 dB. If we use unipolar encoding matrix and a unipolar decoding matrix, then autocorrelation value would be 9.05 dB.

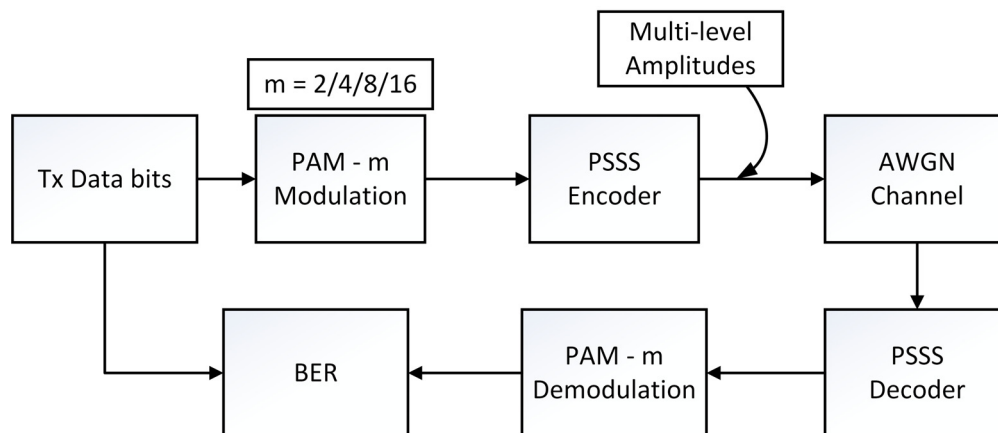


Figure 3.8: PSSS System model for BER evaluation.

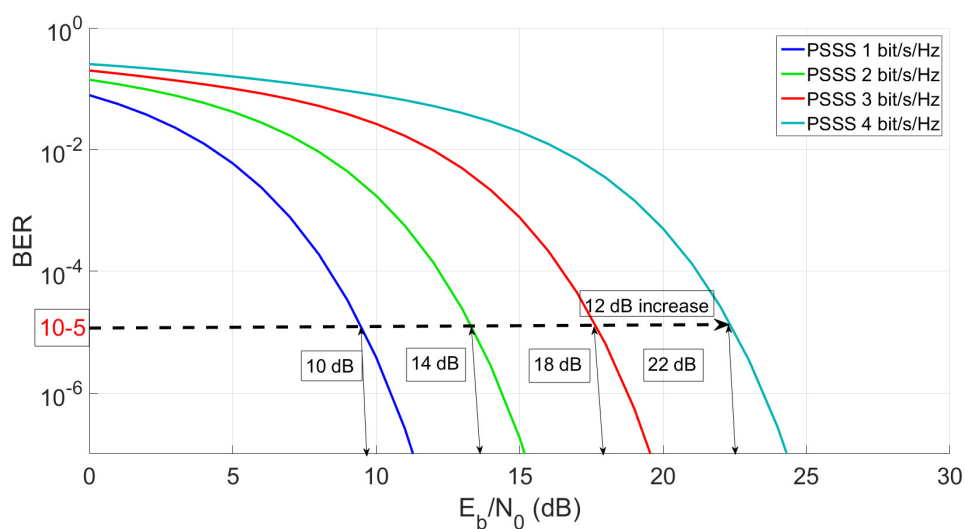
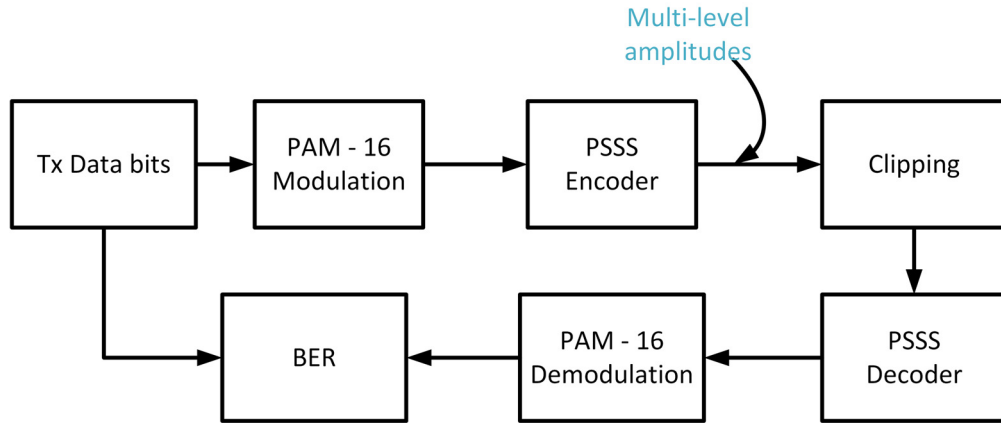


Figure 3.9: BER curves for PSSS modulation with different spectral efficiency.

a PSSS encoder. Here, we have chosen bipolar  $m$ -sequences for encoding and unipolar  $m$ -sequences for decoding (first option). The output of the encoder are discrete multi-level amplitudes, and the signal is passed through an additive white Gaussian noise (AWGN) channel. At the receiver, the noisy signal from the AWGN channel is fed into the “PSSS decoder” in which the signal is correlated with a known  $m$ -sequences pattern. This results in the recovery of the  $M^{\text{th}}$  order PAM signal. The output of the “PAM-M demodulation” blocks leads to the recovery of the transmitted data bits. Finally, the BER is computed from the recovered data bits and the transmitted data bits.

Figure 3.9 shows the BER vs.  $E_b/N_0$  for the AWGN channel. We can observe that to achieve BER of  $10^{-5}$ , we need an  $E_b/N_0$  of 10 dB for BPSK, whereas for PAM-16, the required  $E_b/N_0$  is 22 dB.



**Figure 3.10:** System model for evaluating the performance of PSSS modulation with clipping.

### 3.3.3 Probability distribution analysis

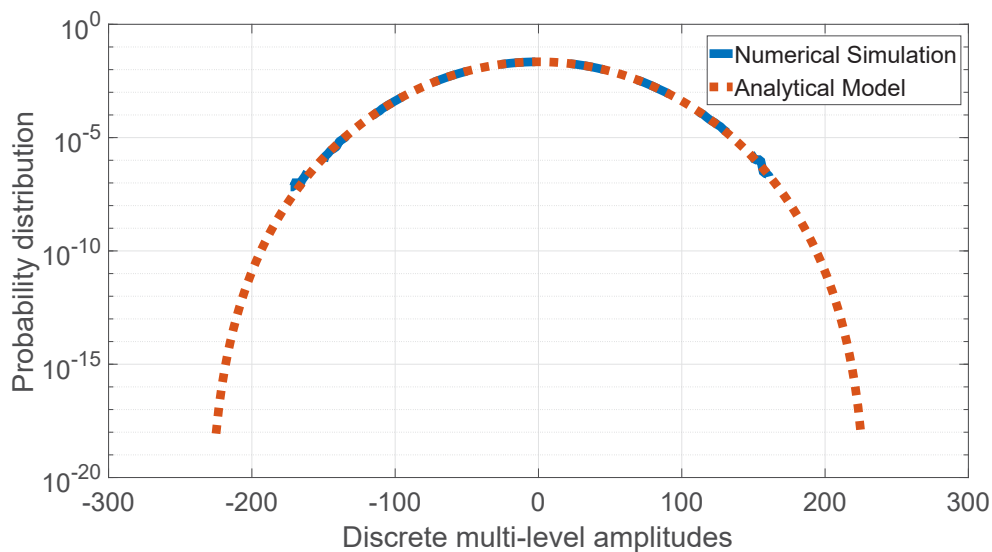
In this Section, we present an analysis of the probability distribution of multi-level PSSS chip values at the encoder. A comprehensive analytical description of the probability distribution of the number of discrete levels appearing at the output of the PSSS encoder is investigated in our work published in Ref. [144], and the mathematical analysis is described in Appendix A.

Fig. 3.10 indicates the structure of the scheme used for assessing the likelihood of the multi-level amplitudes at the PSSS encoder output. The output of the PSSS encoder (titled as “Multi-level amplitudes”) is tapped and utilized for the histogram. 60 million data bits have been used to compute the probability distribution. The transmitted information bits are modulated by a “PAM-16” modulation as in Fig. 3.10. The “PAM-16” output goes through a PSSS encoder (as in Eqn. (3.12)) to produce the multi-level signal. Eventually, the complete probability distribution of discrete amplitudes is evaluated from the output of the PSSS encoder by plotting a histogram.

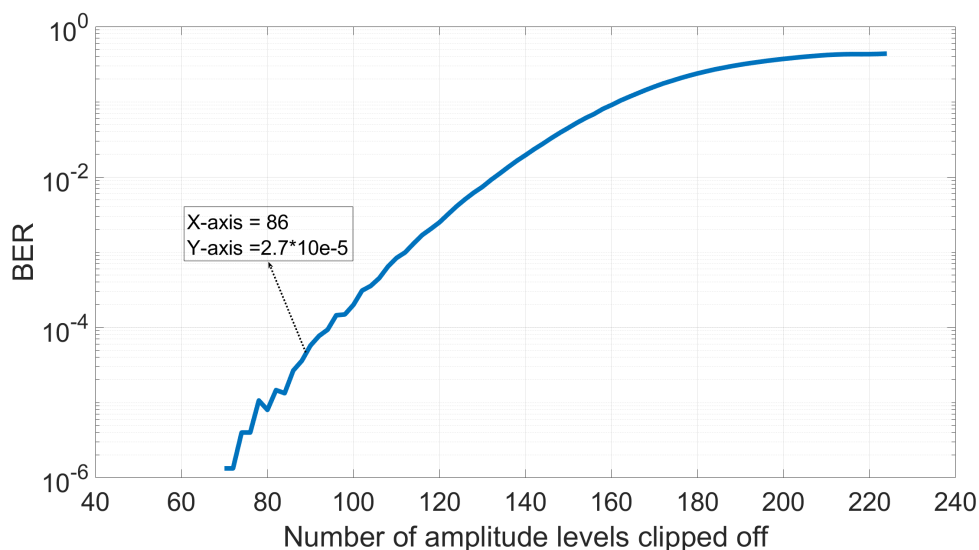
The final probability distribution of discrete PSSS chip-values at the output of the encoder is obtained analytically. This is described in the Appendix A. The analytical distribution, and the probability distribution obtained by numerical simulation is presented in *log scale* in Fig. 3.11. This is more useful for the representation of the low values of the probability distribution. Compared to the analytical probability distribution, the numerically computed values are in the highest agreement at high probabilities as shown in Fig. 3.11. Due to the huge amount of all input data combinations (which is  $16^{15}$ ) it is therefore not feasible to perform numerical simulations at lower probabilities.

### 3.3.4 PSSS transmitter clipping model

In Fig. 3.11, we can observe that there are many discrete multi-level amplitudes with very low probabilities. As we can observe in Fig. 3.11, the multi-level amplitudes outside the range from  $-130$  to  $130$  have a very low probability of less than  $1 \times 10^{-8}$ . We would like to investigate what is the effect on BER if we clip those multi-level amplitudes occurring



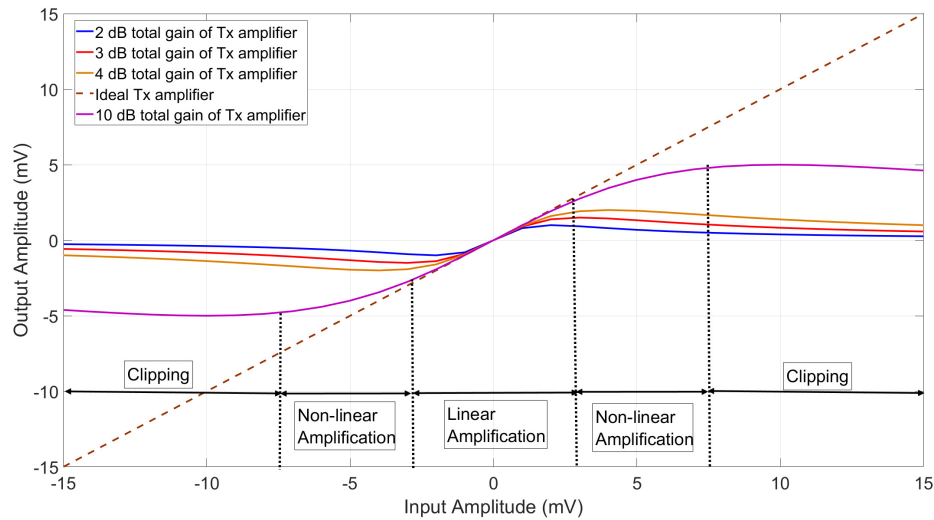
**Figure 3.11:** Different multilevel values of  $S$  are represented on the x-axis, and the y-axis is the probability distribution of these multilevel values using a logarithmic scale.



**Figure 3.12:** BER of the system model as shown in Fig. 3.10. The x-axis represents the number of amplitudes level clipped off, and the y-axis in log scale represents the BER.

with very low probabilities.

Figure 3.10 shows the setup to measure the BER for a PSSS system using PAM-16 and a  $m$ -sequence of length 15. Data bits with PAM-16 are modulated with a PSSS encoder, which results in multi-level amplitudes as depicted in Fig. 3.10. As illustrated in Fig. 3.11, the probability distribution of the 225 different amplitude levels indicates an immensely small likelihood for the maximum and minimum values. The multi-level amplitudes outside the range from  $-130$  to  $130$  (s. Fig. 3.11) are clipped off. These values are cut and assigned to the largest or smallest retained value to minimize the bit distortion emerging from the clipping. The output of the clipped distribution is fed



**Figure 3.13:** AM/AM response of a power amplifier.

through the “PSSS decoding” and followed up with “PAM demodulation” to recover the transmitted signal.

The BER as a function of the number of clipped amplitudes is shown in Fig. 3.12. For example, a clipping of 86 amplitudes, i.e., the 43 highest and lowest multi-level amplitudes, respectively, results in the total BER of  $2.7 \times 10^{-5}$ . Figure 3.12 indicates that a comparatively large amount of low probability amplitude levels cut leads only to a relatively small rise in the BER. Consequently, the analytical model enables to calculate the number of discrete amplitudes that occur at the PSSS encoder output, which in turn helps to calculate the amount of DAC quantization values that the PSSS transmitter requires.

To summarize, the advantages of clipping multi-level PSSS chip-values with lower probability of occurrence are (i) the Peak-to-Average Power Ratio (PAPR) reduction which leads to lowers the linearity requirements of the power amplifier (PA), and (ii) we can determine the optimal DAC resolution.

### 3.3.5 RAPP-Model for PSSS transceiver

Power amplifiers are used to increase the power of modulated waves to a rate that is sufficiently high to reach the required transmission range. Non-linear effects arise in communication systems in the form of harmonic distortion, gain compression, inter-modulation distortion by mixers, phase distortion, etc. [145]. In a PSSS modulated system, the transmitted signal is susceptible to the high PAPR, i.e., many discrete multi-level amplitudes values that occur at the output of PSSS encoder. Non-linear behavior of the power amplifiers results in clipping of those high levels of amplitude values (s. Fig. 3.11).

Figure 3.13 shows the behavioral response of the amplitude distortion of the power amplifier. A PA has three major working regions. In the first region named



“Linear Amplification”, the PA has linear gain characteristics wherein the input signal is amplified to the corresponding output signal. In the second region named as “Non-linear Amplification”, the characteristic gain transition occurs from linear region to saturation region. Finally, in the last region named “Clipping”, the gain values saturate, and a further increase in the input amplitude does not affect the output amplitudes. The distortion is caused by the non-linear amplification and clipping effects of the PA. The total gain represents the amplification due to the linear region and non-linear region (as shown in Fig. 3.13). It is clear from the graph that an increase in the total gain of the transmit amplifier will lead to a reduction in the clipping of the input signal. This means, a 10 dB total gain Tx amplifier does not clip off the input amplitudes between -5 dBm and +5 dBm, and it clips off of any inputs amplitude which does not fall in this ranges. In conjunction with the clipping of the PSSS amplitudes by the PA, we have to note that a clipping of higher and lower amplitudes (s. Sec. 3.3.4) leads to a lower input signal of the amplifier and thereby reduces the requirements for the total amplification.

A widely accepted solid-state “behavioral amplifier model” encompassing the amplitude clipping (i.e., AM-AM distortion) is the Rapp Model [146]. It is designed according to Eqn. (3.20) and produces a smooth transition for the envelope characteristic of the output signal as the input amplitude approaches saturation. The amplitude distortion (AM/AM) conversion is given by [147]

$$A_{out} = \frac{A_{in}}{\left[1 + \left[\frac{|A_{in}|}{A_{sat}}\right]^{2p}\right]^{1/2p}} \quad (3.20)$$

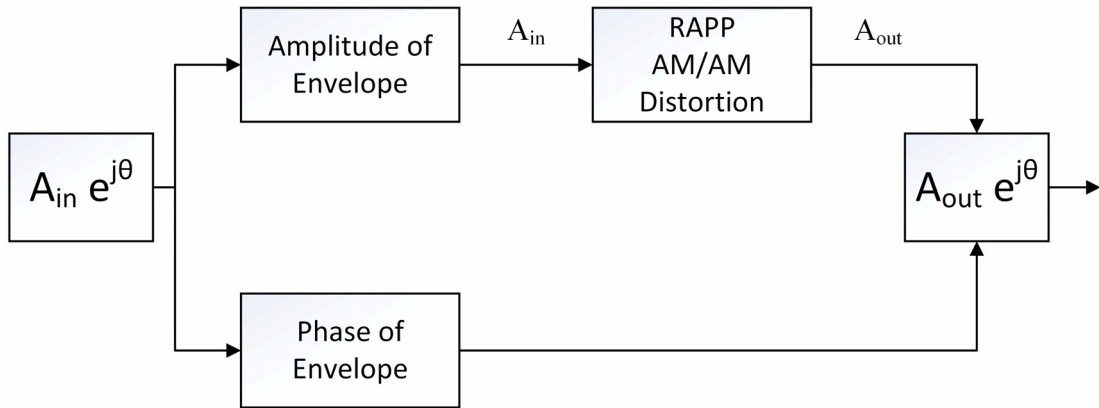
wherein  $A_{sat}$  is the saturation output amplitude,  $A_{in}$  is the input amplitude,  $A_{out}$  is the output amplitude, and  $p$  controls the smoothness of the transition from a linear region to a saturation region.

Figure 3.13 shows a PA curve of a “10 dB total gain of Tx amplifier”, which amplifies input voltages from -3 dBm to +3 dBm linearly, i.e.,  $A_{out}$  follows the  $A_{in}$ . The non-linear amplification<sup>5</sup> occurs in two regions: from -5 dBm to -3 dBm, and from +3 dBm to +5 dBm. The clipping starts if the signal level is above +5 dBm or signal level is below -5 dBm.

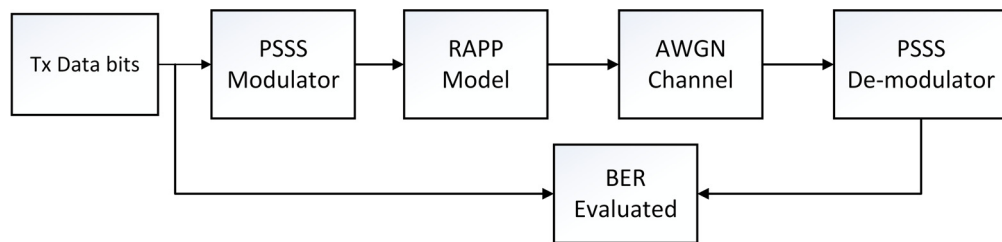
Here, the factor  $p$  plays an important role. In Fig. 3.13, the factor  $p$  was set to 2, so we have a smoother transition. But if we increase the factor  $p$  to 10, then transition to the saturation output amplitude  $A_{sat}$  will be sharper.

Figure 3.14 shows the RAPP-Model of the PA used in the IEEE 802.11 [147] standard. The RAPP-Model was used to describe the behavior of the PA for WLAN systems. The input signal envelope is measured using the “Amplitude of Envelope”, and the output of this block is further passed on to “RAPP AM/AM Distortion” block to simulate the clipping of the input amplitude (as described in Eqn. (3.20)). The phase of the input signal is unchanged.

<sup>5</sup>The transition from linear to saturation region.



**Figure 3.14:** Block diagram of the RAPP model. The amplitude of the input signal is varied, but the phase is kept constant.

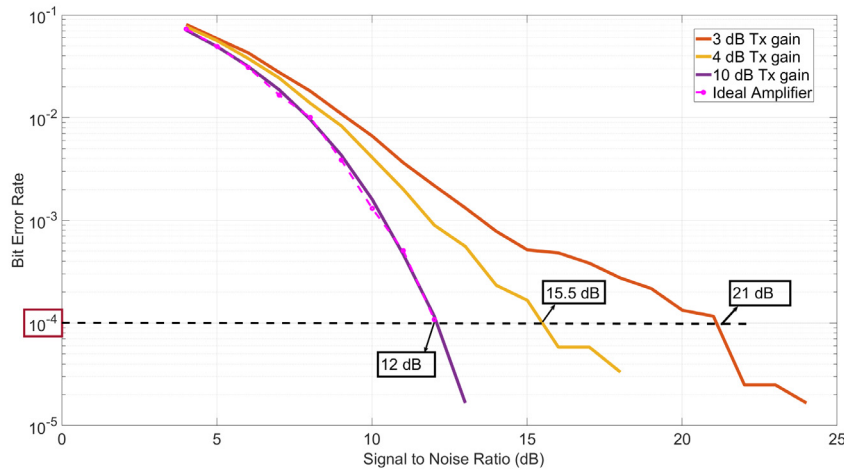


**Figure 3.15:** PSSS system simulation with the RAPP-Model to examine non-linear distortions induced by the PA.

Figure 3.15 shows the simulation model to investigate the behavior of the PSSS system in the presence of non-linear distortions caused by the PA. As shown in Fig. 3.15, the data bits are encoded using bipolar  $m$ -sequences by the “PSSS Modulator” block. The output of the PSSS modulator is fed into the RAPP-Model, which performs clipping and non-linear distortion, as described in Eqn. (3.20). The output signal coming from the RAPP model is fed to the “AWGN Channel” block to add white noise. At the receiver, the signal is decoded using an unipolar  $m$ -sequence. Moreover, the receiver also performs channel deconvolution. Thus, we can analyze the effect of the channel deconvolution on the “effective channel” rather than the AWGN channel only. The performance is measured by evaluating the BER. We examined how the PSSS receiver can tolerate the total distortion (i.e., non-linearity and clipping).

A PSSS encoded BPSK-signal is used for the following investigations. As shown in Fig. 3.16, we need an SNR of 21 dB with PA having a total gain of 3 dB to achieve BER of  $10^{-4}$ . However, the required SNR drops to 15.5 dB with the PA having a total gain of 4 dB. One more important point is that even if we have a very poor PA with a linear gain of 3 dB (PA characteristics as in Fig. 3.13), the PSSS demodulator is still able to recover the signal at the cost of an increased SNR. Thus, PSSS modulation/demodulation can tolerate the non-linear amplification and clipping caused by the PA.

Finally, the RAPP-Model facilitates to study the clipping of larger amplitudes and non-linear distortion in the transmission chain. We can optimize the amplifier chain of



**Figure 3.16:** BER vs. SNR for a PSSS modulated signal and different total gains of the transmit power amplifier.

the complete transmission system, i.e., the PA at the transmitter, the AWGN channel, and the Low Noise Amplifier (LNA) at the receiver.

### 3.4 PSSS system model

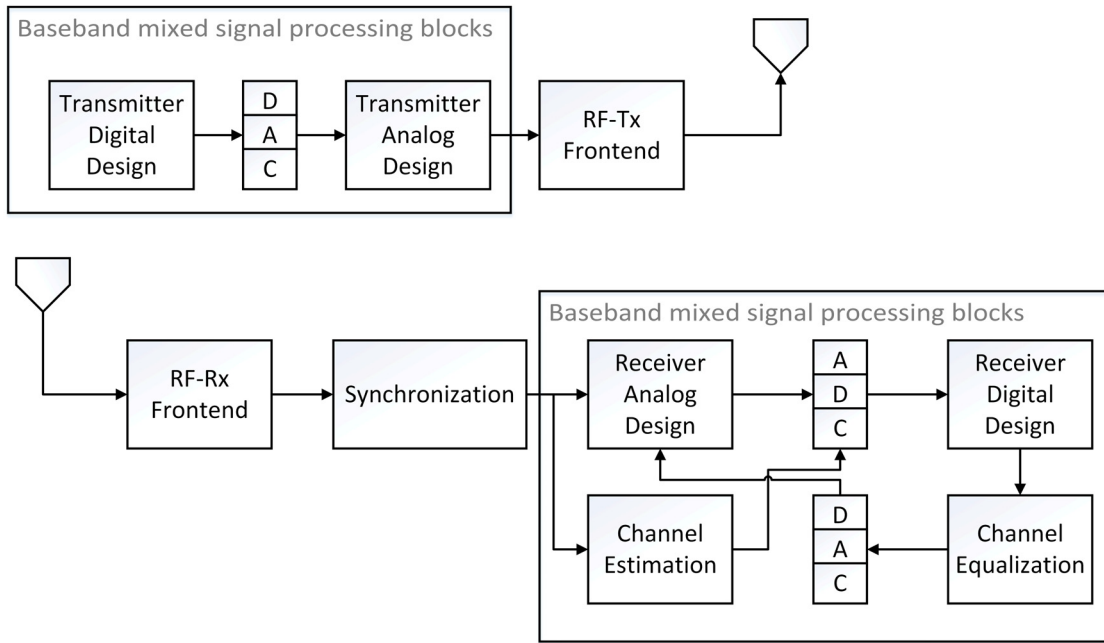
There are three types of signal processing techniques:

- Digital Signal Processing (DSP) / digital domain,
- Analog Signal Processing (ASP) / analog domain,
- Mixed Signal Processing (MSP) / mixed-signal domain.

Mixed-signal processing means that both analog and digital signal processing is performed as part of the system. Most of the electronic systems today are mixed-signal systems, i.e., they consist of analog and digital signal processing units connected by DACs and ADCs. In a general baseband system, some signal processing operations are performed in the analog domain, some in the digital domain, and the data converters are in between. The trend is to move the data converters close to a physical interface (right after RF-fronted) [148, 149].

However, moving the data converters close to RF-frontends puts huge efforts on realizing these improved converters in terms of dynamic range, bandwidth, and sampling rate. As outlined in the first chapter (s. Sec. 1.2.1), if we implement a 100 Gbps PSSS transceiver system in the digital domain, the data converters need to be operated at a sampling rate of 150 GS/s. With the usage of the MSP, we can move data converters close to the Data Link Layer (DLL) thereby relaxing the requirements on DACs/ADCs. We need a modulation scheme that inherently supports the mixed-signal processing operations.

PSSS modulation eases the implementation of synchronization, de-correlation, and the channel equalization operation as most of these operations can be performed by



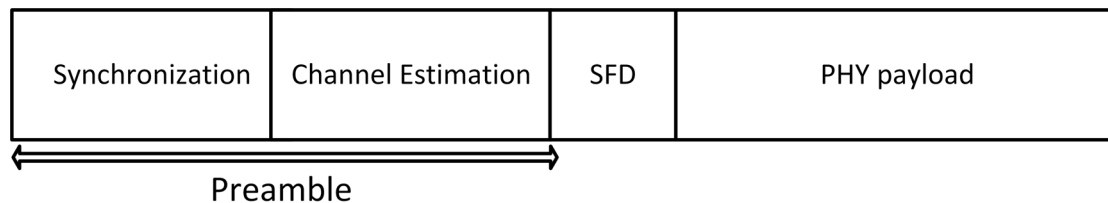
**Figure 3.17:** PSSS system model with transceiver components of a baseband system. The DACs and ADCs operate at the low PSSS symbol rate.

analog signal processing without the need for high-speed data converters and partly in the digital domain (i.e., using MSP technique). The PSSS modulation is quite attractive for ultra-broadband mixed-mode transmitter/receiver implementations and allows using low-speed data convertors [133, 150].

The mixed-signal baseband processing system of transmitter and receiver is as shown in Fig. 3.17. Targeting for higher data rates, we adopt a novel mixed-mode design where the baseband signal processing can be done mostly in the analog domain and partly in the digital domain. At the transmitter, the digital design part consists of conducting the PSSS encoding at the PSSS symbol rate. The DACs are also operating at the low PSSS symbol rate. These DACs are used to interface the PSSS encoders with a high-speed analog Mux running at the high chip-rate.

At the receiver, the received RF-signal is down-converted into baseband by the “RF-RX frontend” block. Then, the signal is passed to the “synchronization” block, where the synchronization is performed by the ASP technique. Then, the signal is fed in parallel to the “Receiver analog design” block and the “Channel Estimation” block. In the “Channel Estimation” block, a series of parallel IDCs calculates the channel impulse response using training symbols (i.e., m-sequences), and then low-speed ADCs convert them into a digital signal. This channel estimate is used by the “Channel equalization” to equalize the “effective channel”. The “Receiver analog design” block performs PSSS demodulation by using the same series of a parallel IDCs, which are operating at the chip rate<sup>6</sup>. Finally, the low-speed ADCs running at the PSSS symbol rate are used for

<sup>6</sup>The N-parallel IDCs performs both channel estimation and PSSS data demodulation. N is the length of the m-sequence. Here, “Channel Estimation” block and “Receiver Analog Design” block is shown as two separate blocks to ensure the proper understanding.



**Figure 3.18:** PHY packet structure.

digitizing the received analog signal. As we can observe, the DACs/ADCs are “moved” closer to the DLL layer<sup>7</sup>. This reduces the sampling rate of ADCs<sup>8</sup> to a low-PSSS symbol rate.

The data stream is modulated as PAM-16 before encoding the stream with orthogonal codes. To achieve the target data rate of 100 Gbps using PSSS with a MLS-15 coding matrix, a higher digital modulation complexity is required. The 50 GHz, double sideband RF bandwidth at 240 GHz translates to a 25 GHz baseband bandwidth, which limits the maximum chip rate to roughly 25 – 30 Gcps. With a chip rate of 30 Gcps, PSSS encoding requires a bit loading of at least 4 bits to achieve the target data rate of 100 Gbps.

### 3.4.1 PHY packet structure and System parameters

The physical channel packets are built by amending a coded preamble for the channel estimation, and the synchronization at the receiver. The preamble consists of a repeated number of *m-sequences*. Since we do not use I-Q channels at the transmitter, we are not using I-Q modulation schemes like QPSK or QAM. Also, the timing synchronization can be easily performed since we have a much higher correlation peak with the use of *m-sequences*.

Figure 3.18 shows the PHY packet structure. It consists of the preamble, a start frame delimiter (SFD), and the PHY payload. The preamble consists of symbols for the synchronization and channel estimation. The SFD is the value marking the end of the preamble and the start of the PHY payload. The SFD consists of an inverted *m-sequences*. The usage of the inverted *m-sequences* results in a negative auto-correlation peak after the correlation at the receiver. The PHY payload consists of PSSS modulated symbols. Normally, we use the preamble also for the Automatic gain control (AGC). AGC is necessary for a dynamic system where the received signal strength is not known in advance. We consider point-to-point systems wherein the AGC is not necessary, but it will be configured once manually. Thus, we do not need extra symbols in the preamble for the AGC.

**Table 3.2:** System Parameters

Parameters	Expected Values
Data rate (Gbps)	100 <sup>a</sup>
m-sequence length (N)	15
Bit-loading (bits)	4 <sup>b</sup>
Chip rate (Gcps)	30
Cyclic prefix (chips)	3 <sup>c</sup>
PSSS symbol rate (GHz)	1.67 <sup>d</sup>
Baseband Bandwidth (GHz)	25
RF-Bandwidth (GHz)	50
Target carrier frequency (GHz)	230 ~ 240

<sup>a</sup> With a bit loading of 4 bits and baseband bandwidth of 25 GHz, we have a data rate of  $25 \times 4 = 100$  Gbps. <sup>b</sup> This is the mapping from data bits to data symbols. In other words, we are using PAM-16 modulation on the raw data bits. <sup>c</sup> This comes from the expected delay spread of the channel at 250 GHz and the use of directed antennas. <sup>d</sup> One PSSS symbol consists of N chips and cyclic prefix. So, one PSSS symbol has 18 chips (15 + 3). We have a chip rate of 30 Gcps. It leads to symbol rate of  $\frac{30}{(15+3)} = 1.67$  GHz.

Tab. 3.2 shows an overview of the selected system parameters. We selected an m-sequence length of 15 because we wanted to limit the complexity and power consumption in the realization. We would not be able to realize IDC in ECL circuits if we opt for higher length m-sequences. Prof. Scheytt's group [132] set these design parameters. We assume a baseband bandwidth of 25 GHz. Thus, we require an RF-bandwidth of 50 GHz, and this huge bandwidth is available in the THz frequency range.

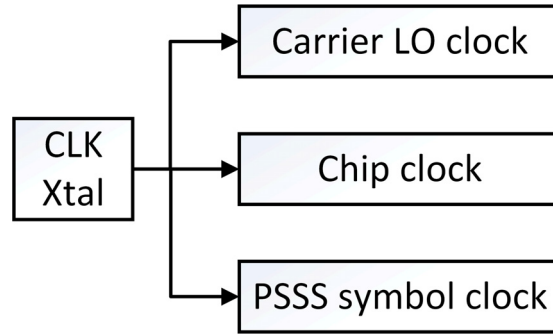
### 3.5 PSSS system synchronization

A synchronization procedure involves the recovery of the carrier frequency, the carrier phase, and the symbol timing from the received signal. Normally, carrier frequency and carrier phase recovery is the part of the RF-frontend to synchronize the receiver oscillator to the transmitter oscillator. The usage of a preamble achieves the symbol timing synchronization (s. Fig. 3.18).

The oscillators do not generate precisely the frequency as specified in the manufacturer's datasheet. This causes a frequency mismatch between the transmitter and receiver oscillators. There will always be some Carrier Frequency Offset (CFO). Besides, this offset is partly due to aging factors and depends on temperature and pressure. A "carrier frequency/phase synchronization" is a procedure through which the detector adapts the frequency and phase of its local oscillator to those of the received signal. A circuit that performs this operation is called "carrier synchronizer". The above-circuit can be implemented in the analog domain or digital domain [151–153].

<sup>7</sup>After the "Receiver digital design" block comes the Data Link Layer. This is not shown in the figure.

<sup>8</sup>We need slower DACs/ADCs operating at the PSSS symbol rate because there N-parallel IDCs are demodulating the data at the same time. We need "N" number of data converter connected parallelly to these IDC and effectively reducing the sampling rate of data convertors by a factor N.



**Figure 3.19:** Coherent receiver system.

The difference between actual and current sampling times is defined as “timing offset”. “Symbol timing synchronization” is a method where the receiver decides the right measurement instants of the recorded signal. After the down-conversion of the received signal to the baseband, we have to find the sampling times of the received waveform, and they are located approximately at the “peaks” of signal pulses [151]. Indeed, the locations of these optimum sampling points have to be accurately determined to perform reliable data demodulation. A circuit that performs this operation is called “timing synchronizer”. A timing synchronizer can be implemented in the digital domain or the analog domain [152, 153].

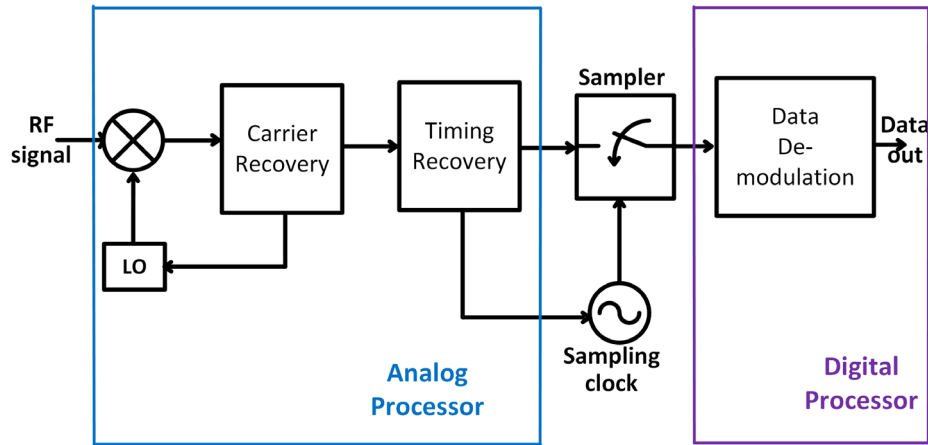
In this section, we introduce synchronization methods applied in our “PSSS system Model”, and types of architectures for carrier frequency/phase and timing recovery algorithms.

### 3.5.1 Coherent Synchronization in PSSS system

We have considered a coherent transmission system as indicated in Fig. 3.19 for our “PSSS system model”. In a coherent system, a single clock source (i.e., from a block named “CLK xtal”) from quartz drives the carrier LO clock, a chip clock, and a PSSS symbol clock. A fundamental requirement in coherent transmission systems is the recovery of the carrier frequency/phase synchronization. The PSSS chip and symbol timing were established by using a preamble (s. Sec. 3.4.1). Generally, the receiver does not possess prior knowledge about the physical channel associated with the transmitted signal. The ultimate task of the coherent receiver is to “extract” the synchronization information from the received signal.

We have used the following two models for achieving synchronization in this work:

1. **PSSS system Model:** The “Synchronization” block shown in Fig. 3.17 was implemented by using a Costas Loop. The Costas Loop helps to achieve carrier the frequency/phase synchronization.
2. **HIL experiments:** The synchronization algorithms were developed in the digital domain and were realized offline using Matlab.



**Figure 3.20:** Analog carrier/timing recovery.

Figure 3.17 shows a brief skeleton sketch of the “PSSS system model”. The PSSS receiver system shown in Fig. 3.17 is a fully coherent design. Further implementation details of the above “PSSS system model” are described in detail in Chap. 4 (specifically in Sec. 4.3). The carrier frequency/phase and timing synchronization was implemented in the analog domain for a baseband bandwidth of 25 GHz.

Hardware-in-the-Loop (HIL) is a technique where baseband algorithms can be tested in software (e.g., by using Matlab/Simulink) with the usage of RF-frontends. In our HIL experiments, the synchronization algorithms were developed in the digital domain using Matlab. This was possible because of the high-end measurement devices used in the experiments. The synchronization algorithms used for the HIL experiments are explained in Chap. 6.

### 3.5.2 Different concepts of synchronization

The carrier and timing recovery can be performed in analog domain or digital domain or both. Here, we refer to both carrier phase and carrier frequency recovery. In a broad sense, there are three concepts to perform synchronization [154],

- Analog carrier/timing recovery.
- Hybrid carrier/timing recovery.
- Digital carrier/timing recovery.

Figure 3.20 depicts an exemplary concept of an “Analog carrier/timing recovery” module. In this example, carrier/timing recovery is achieved by using Phase locked loops (PLLs). The above operation is performed in the analog domain directly on the down-converted baseband signal before it is digitized. As indicated in Fig. 3.20, the rest of the signal processing operation to demodulate the data is performed in the digital domain after the “sampler”. The sampler derives its clock from the “Analog processors”. As discussed in Sec. 3.3, we have a baseband bandwidth of 25 GHz. This means that the carrier and



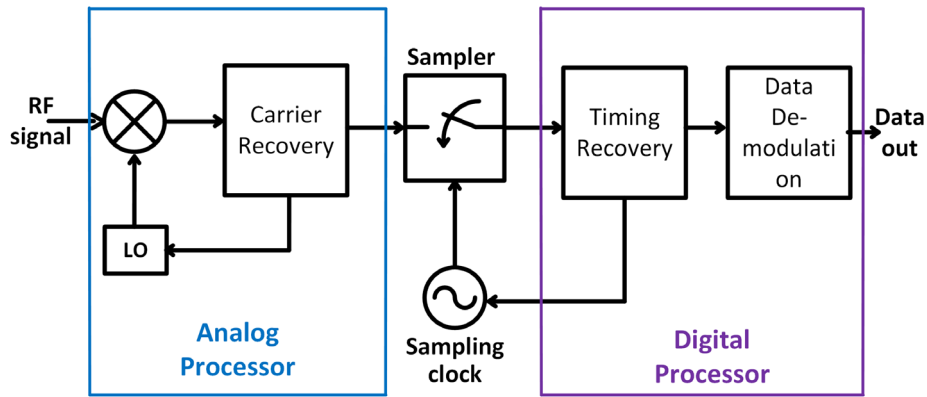


Figure 3.21: Hybrid carrier/timing recovery.

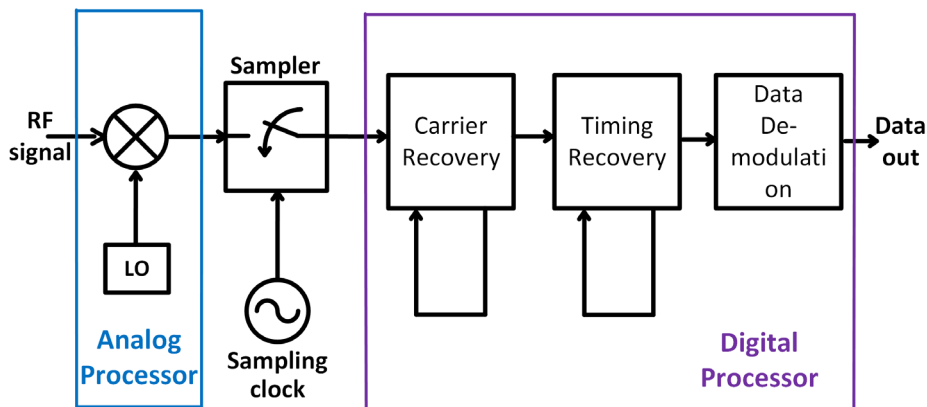


Figure 3.22: Digital carrier/timing recovery. An independent clock reference drives the LO and an independent sampling clock is used.

timing recovery has to be performed at high-speed. In our “PSSS system model”, the carrier frequency and phase recovery are performed in the analog domain by the use of a *Costas loop*. At such a high-bandwidth, a digital implementation is not possible.

Figure 3.21 depicts the idea of a “Hybrid carrier/timing recovery”. In this method, carrier recovery is performed in the analog domain, and the timing recovery is achieved in the digital domain. The “Digital processor” block provides a timing control signal to the sampling clock to achieve timing synchronization [154].

Figure 3.22 depicts the concept of a “Digital carrier/timing recovery”. In this method, a free-running oscillator is used for a frequency down-conversion and an independent sampling clock. The timing offset, the carrier phase error, and the CFO are compensated in the digital part. One crucial factor of implementing the above-algorithms is that we have to digitize the baseband signal at least with an oversampling factor of 2 [152, 155, 156]. In our HIL experiments with PSSS modulation, the timing recovery, and the carrier frequency/phase recovery are performed in the digital domain by post-processing in Matlab/Simulink. These methods are explained in Chap. 6.

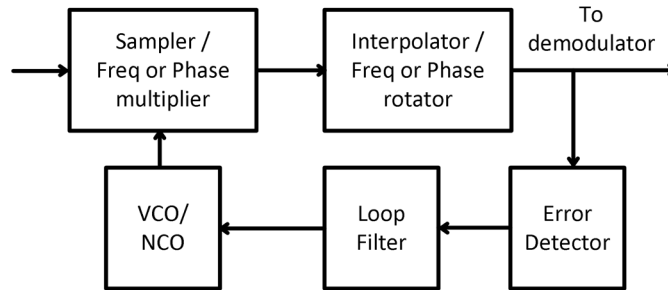


Figure 3.23: Feedback configuration for the carrier/timing recovery.

### 3.5.3 Architecture of synchronizers

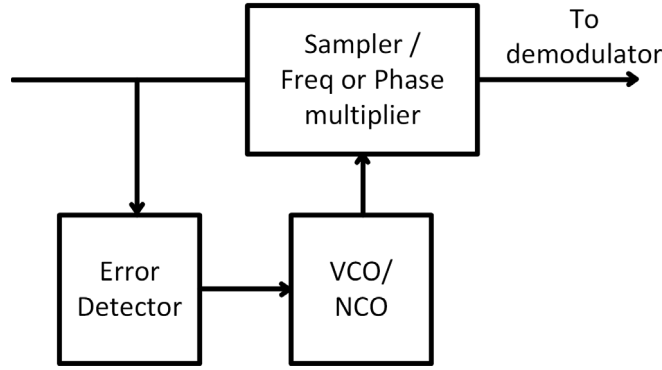
There are three types of synchronization principles [151, 152, 157, 158] and they are,

- **Data-aided (DA):** In the DA method, known reference symbol sequences are sent, which are known to the receiver, e.g., training symbols or preambles.
- **Decision-directed (DD):** In this method, detected symbol values are used as a reference.
- **Non-data-aided (NDA):** This method does not depend on known preamble symbols or detected symbol values. It is a form of blind synchronization method.

Carrier frequency/phase and timing recovery algorithms can be realized either in a feedback configuration or in a feed-forward configuration. Figure 3.23 shows a feedback configuration to implement synchronization algorithms. In the feedback setup, algorithms are usually based on a stochastic approximation approach. The “Error Detector” block in Fig. 3.23 estimates the timing error or the carrier frequency/phase error. This signal is routed to the “Loop filter” block, which drives a voltage-controlled oscillator (VCO) (analog domain) or a Numerically Controlled Oscillator (NCO) (digital domain). Finally, a VCO/NCO adjusts the sampling time, the frequency or the phase (of *Sampler* or *Frequency/phase multiplier* block) to compensate for the carrier phase, the carrier frequency or the timing error.

In Fig. 3.23, the *interpolator* block represents the feedback loop which is used for timing recovery, or it symbolizes the *frequency/phase rotator* when the loop is used for carrier frequency/phase recovery [151]. The “Costas Loop” [159] was implemented in the PSSS system model for carrier frequency/phase recovery. The “Costas Loop” is an example of a *feedback configuration*. Examples for a timing recovery algorithms in the feedback configurations are Gardner [157], Mueller & Mueller [160], etc.

Figure 3.24 shows a feed-forward configuration to implement carrier/timing recovery algorithms. Feed-forward structures are typically used in frame-based systems, i.e., the estimates are computed for fixed-length block samples. As shown in Fig. 3.24, the received signal is fed to the “Error Detector”, which calculates the error signal. The evaluated error signal is fed to the “VCO/NCO” block, which produces the corresponding “correction signal”. This signal is fed to the *Sampler* or *Frequency/phase multiplier*



**Figure 3.24:** Feed-forward configuration for the carrier/timing recovery.

block to compensate for the timing error or carrier frequency/phase error. Examples for carrier frequency/phase estimation algorithms that use feed-forward structures are Luise-Reggiannini, Mengali-Morelli, Rife-Boorstyn, etc [151, 159]. These algorithms are based either on Discrete Fourier Transform (DFT) or on autocorrelation. Designs for timing recovery algorithms in the feed-forward configurations are Oder & Meyr [155], Gardner, and others [151, 152, 159].

### 3.5.4 Synchronization in PSSS system model

The receiver synchronization unit should be capable of handling 100 Gbps in a variety of modulation schemes, including PSSS, but also PAM and QAM. We target a minimum spectral efficiency of 4 bit/s/Hz, resulting in 25 GHz bandwidth for double-sideband PSSS modulation using I-Q channels. The most bandwidth-efficient, frequency-scalable, and flexible receiver architecture would provide synchronous detection directly at the RF carrier frequency, i.e., in our case at  $> 200$  GHz. The conventional approach of super-heterodyne reception, with a synchronization at intermediate frequency (IF), results in a higher receiver complexity and extremely tough filtering requirements.

We employ an “Analog carrier/timing recovery” synchronization architecture as depicted in Fig. 3.20. In a PSSS system model (s. Sec. 4.3), the carrier recovery is implemented in the analog domain by employing a Costas loop.

In a coherent detection system, the carrier information is required at the receiver end, and it should be frequency/phase coherent with the transmitted carrier. This can be achieved by transmitting a carrier component with the modulated signal. But in our experiments, we are utilizing RF-frontends operating in the THz frequency range wherein it is difficult to transmit a carrier signal, as it increases the transmit power. Besides we have transmitted a double side-band suppressed carrier (DSB-SC) signal which does not have a carrier component. A Costas loop can generate a coherent carrier at the receiver and is therefore used for the modulation of DSB-SC modulated signals.

Figure 3.25 shows the Costas loop receiver block diagram. The Costas loop block diagram functioning can be logically divided into three parts, I-channel (one marked by purple color), Q-channel (enclosed by red color), and the middle section is the error signal

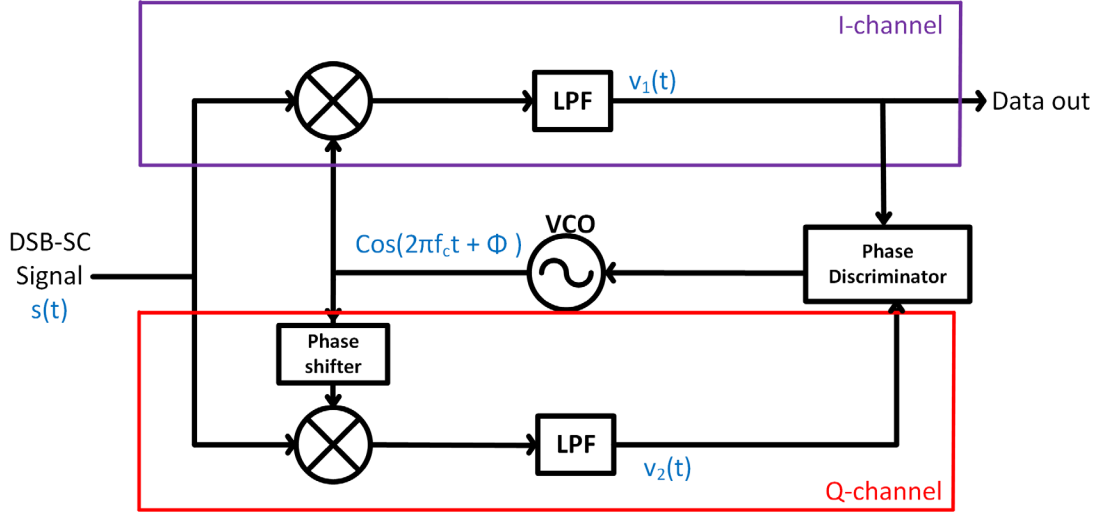


Figure 3.25: Costas Loop block diagram.

generation along with VCO. As we can observe in Fig. 3.25, the received DSB-SC signal  $s(t)$  is simultaneously fed to the I-channel and the Q-channel. When we consider the upper branch of block diagram (i.e., I-channel), the received signal  $s(t)$  is multiplied with a product modulator (represented by  $\otimes$  in Fig. 3.25) and the other input is taken from the VCO. The output of this above-product modulator is passed onto a Low Pass Filter (LPF) to remove the carrier signal. A similar operation is mirrored for the Q-channel with one exception that the input to product modulator is taken from VCO with a phase shift of  $-90^\circ$ .

The received DSB-SC signal is,

$$s(t) = A_c \cos(2\pi f_c t) * m(t). \quad (3.21)$$

wherein  $A_c$  is the received signal amplitude,  $f_c$  is the carrier frequency, and  $m(t)$  is the transmitted message signal. Let  $c_1$  be the output of the VCO and  $\phi$  be the phase of the VCO signal,

$$c_1(t) = \cos(2\pi f_c t + \phi). \quad (3.22)$$

The output of the LPF at the upper arm (I-channel) is given by Ref. [159, p. 312]

$$v_1(t) = \frac{A_c}{2} \cos(\phi) * m(t). \quad (3.23)$$

The output of the LPF at the lower arm (Q-channel) is

$$v_2(t) = \frac{A_c}{2} \sin(\phi) * m(t). \quad (3.24)$$

Now, these two outputs coming from the low pass filters, namely  $v_1(t)$  and  $v_2(t)$ , are fed to the “Phase Discriminator” block. Depending on the phase/frequency difference between these two signals, the phase discriminator outputs a DC control signal. This

signal is applied to the VCO input to the correct phase/frequency at the output of the VCO. Finally, the DC control signal has a zero value when the carrier signal (used in DSB-SC modulation) and the locally generated signal (VCO output) are in match with phase/frequency. The Costas loop hardware implementation details in the “PSSS system model” are explained in Chapter 4, specifically, in Sec. 4.3.

Timing recovery was performed in the analog domain. We make use of the Data-aided (DA) method wherein repeated *m-sequences* are transmitted as a preamble. An analog IDC (s. Chapter. 4 and Sec. 4.2.2) was used to detect the peaks and the symbol timing was established.

## 3.6 Channel estimation and equalization

The evaluation of channel estimates plays a critical role in wireless communication systems. A serial signal stream is transmitted to a receiver via our “effective channel”<sup>9</sup>. At the receiver, the transmitted signal gets distorted by the “effective channel”. Channel estimation can be achieved in several ways: (i) using a parametric model or without it, (ii) adopting wireless channel frequency or time correlation characteristics, (iii) blind techniques, (iv) using training symbols, (v) or adaptive or non-adaptive processes [161].

We perform “training based channel estimation” by using *m-sequences*. It is presumed that the channels remain constant during the duration of the packet, i.e., the time taken for the transmission of a packet is less than the channel coherence time.

Equalizers are designed to counteract both channel, noise, and other RF-impairments. An equalizer can be designed directly with the signal received, or the channel pulse response can be first estimated and an equalizer can be then designed according to the estimated channel. The article by Tugnait [162] provides a comprehensive survey done over two decades of research in the area of channel equalization. It covers a broad spectrum of channel equalization techniques like linear equalization, Kalman detector, decision feedback equalization, Maximum Likelihood Sequence Detector, Turbo equalization, etc. Some of the above-techniques are implemented either in time-domain or in frequency-domain.

We focus here on the frequency domain channel equalization, where we apply a DFT. The DFT calculation involves the evaluation of twiddle factors which requires more hardware resources. We give a brief introduction on how to perform a fast DFT for non-power of two frequency bins where there is no need to evaluate the twiddle factors. This helps in reducing the complexity, and also increases the speed of the computation.

### 3.6.1 Channel estimation

The training based channel estimation (i.e., with training sequences) is most suited for practical systems since it can be easily realized in hardware [163]. The Least-Squares

<sup>9</sup>An “effective channel” includes the transmitter RF-frontend, over the air transmission, and the receiver RF-frontend

(LS) channel estimation algorithm using periodic sequences has been investigated in Ref. [164]. It uses MLS or *m-sequences*. Furthermore, *m-sequences* have a Dirac-delta like auto-correlation function. This property is utilized for channel estimation [165].

In general, the channel estimation parameters are complex values. A PSSS modulated system uses only I-channel at the transmitter to transmit the data. At the receiver, the data is received on both I & Q channels. We perform synchronization by using a Costas-Loop. It uses the information in the Q-channel to de-rotate the I-Q coordinate system such that we receive data only in I-channel. Thus, we have shown channel estimation operation using real values as shown in Fig. 3.26.

Figure 3.26 depicts the operation of the channel estimation using *m-sequences*. Sub-figure (a) shows the transmitted *m-sequence* and Fig. 3.26(b) shows the received *m-sequence* with channel effects caused by impairments. After performing a correlation of the received signal with a known *m-sequence* at the receiver, we obtain the estimated channel coefficients as described in Fig. 3.26(c). By subsequently performing a channel equalization, we obtain a new reference pattern for the correlation at the receiver as in Fig. 3.26(e). If this new reference pattern is correlated with the received signal (as in Fig. 3.26(b)), we obtain a single peak, as shown in Fig. 3.26(e). As we observe in Fig. 3.26(e), the compensated channel after performing channel deconvolution resembles the Dirac-delta function.

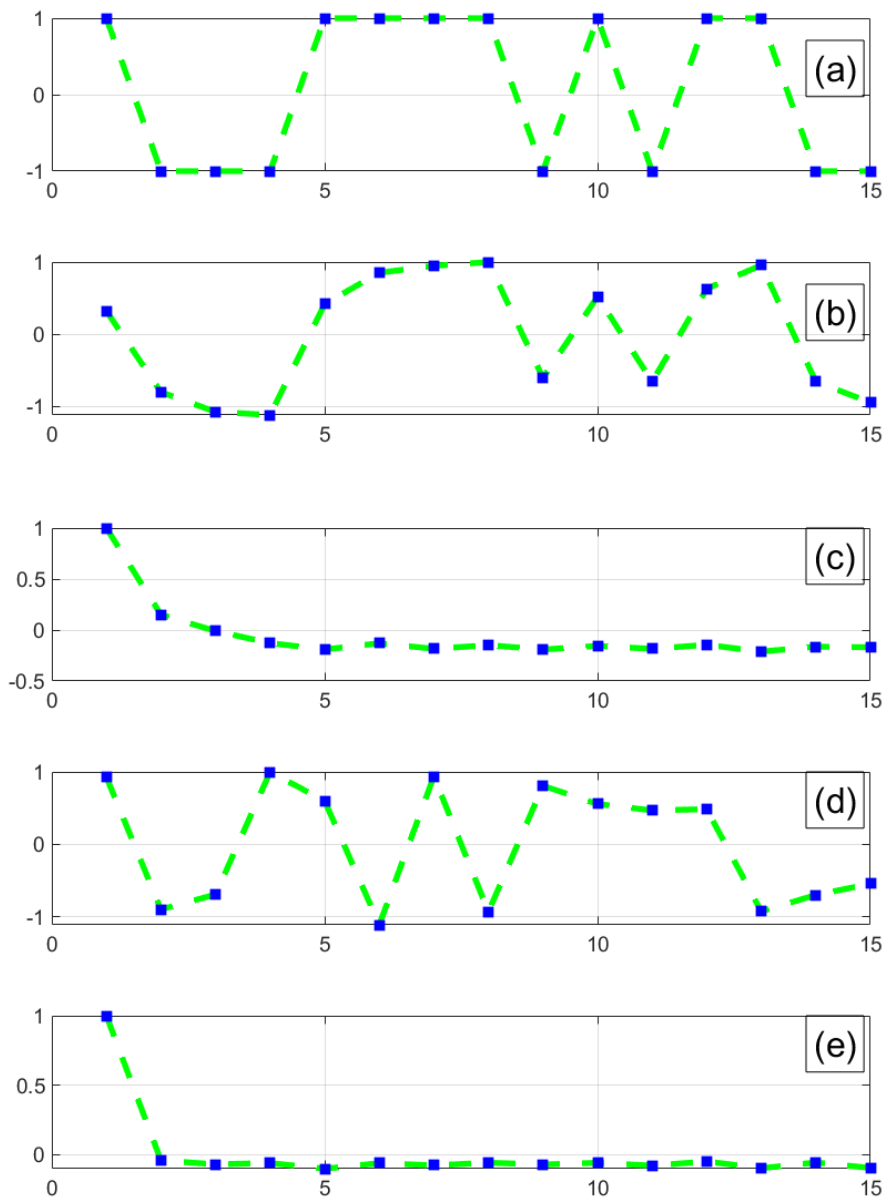
### 3.6.2 Channel equalization

The traditional approach in Single-carrier (SC) systems is the usage of Time-domain equalization (TDE) [166]. The Inter-Symbol Interference (ISI) in the data symbols is caused by the dispersion in the channel and also RF-frontend components. Let us assume that we require  $P$  symbols to combat the dispersion. The value of  $P$  increases linearly with the chip rate. Consider a PSSS system with a data rate of 100 Gbps, which requires a chip rate of 30 Gcps with a bit-loading of 4 bits. A chip rate of 30 Gcps translates to a chip period of 34 ps. We assume that in a THz line-of-sight (LOS) channel the RMS delay spread is 102 ps<sup>10</sup>. This corresponds to  $P \approx \frac{102ps}{34ps} = 3$  symbols of dispersion (or a cyclic prefix of 3 chips). A typical equalizer design complexity<sup>11</sup> would increase by 36 times ( $\propto P^2$ ) [167]. Thus, TDE is not suitable for high-speed transmission with the effective channel delay spread extending over many symbols.

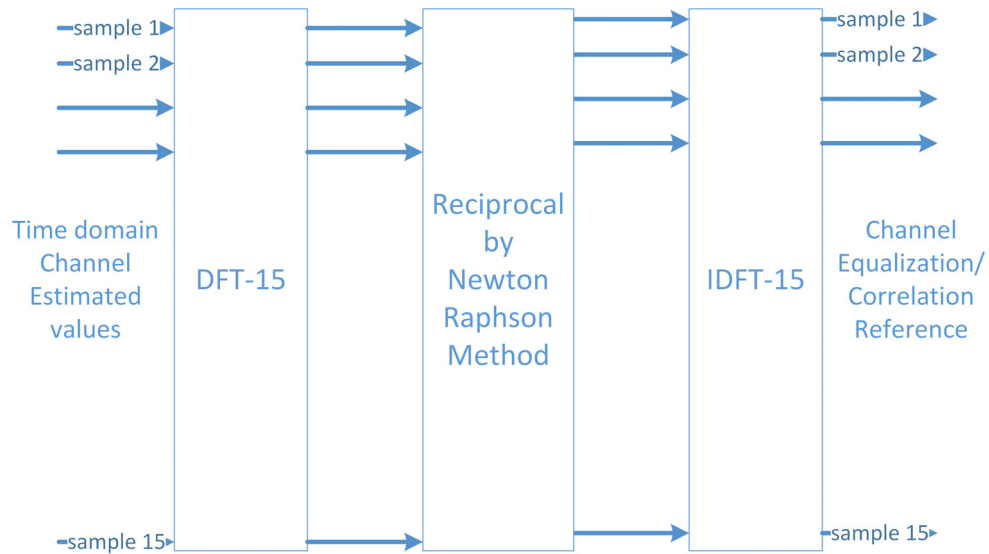
A promising alternative to TDE is Frequency-domain equalization (FDE) [167–170]. The use of FDE for a SC linear modulation was first examined by Schwartz *et al.*, 1973 [171], who showed that the algorithm converges faster than comparable time-domain equalizers. FDE technique [172–175] had been proved to possess a low complexity growth with

<sup>10</sup>We are using a THz channel operating at 230 GHz and directed antennas. At this high-carrier frequency, the channel will cause pulse stretching. And we assume this to be 3 chips long. At a chip rate of 30 Gcps, this corresponds to an RMS delay spread of  $34 \times 3 = 102$  ps

<sup>11</sup>In an FPGA implementation, the complexity of the equalizer decides the maximum achievable clock frequency, BRAM, and DSP slices consumed. For an ASIC implementation, the complexity is a function of the silicon area, the size of the chip, and the power consumption. The complexity calculation was evaluated from [167].



**Figure 3.26:** Illustration of the channel estimation and equalization. (a) transmitted  $m$ -sequence, (b) received  $m$ -sequence with channel effects, (c) estimated channel coefficients, (d) new reference pattern for the IDCs, and (e) equalized signal.



**Figure 3.27:** Algorithm for channel equalization in the frequency domain.

increasing  $P$ .

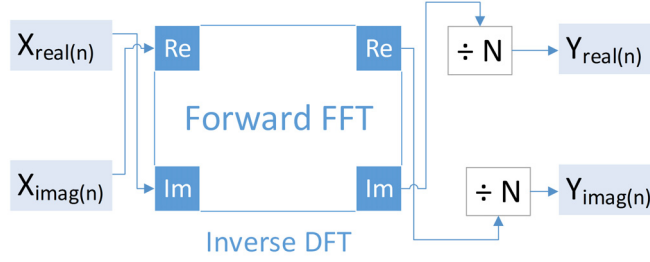
As discussed in the previous section (s. Sec. 3.3.5), we have non-linear distortion and clipping induced by the PA. And, we have to perform carrier frequency synchronization at the receiver to compensate for the CFO. Furthermore, SC–FDE scheme has a low sensitivity to both carrier frequency uncertainties, and nonlinear distortions caused by PA [175, 176].

The channel equalization/channel deconvolution method used in this work consists of performing a DFT on the estimated channel values, calculating the reciprocal of each DFT sample, and finally performing an Inverse Discrete Fourier Transform (IDFT) to obtain the channel equalization values (s. Fig. 3.27). Since we have chosen an  $m$ -sequence length of 15 as a system design parameter [132, 177], we perform a DFT of 15 points. The time-domain channel estimates evaluated from the training sequences ( $m$ -sequences) are fed into the “DFT-15” block as shown in Fig. 3.27. The Newton Raphson Method [178] is a technique for solving equations numerically. An important application of this technique is the “Newton–Raphson division” method [179, 180]. It is a method to find the reciprocal of a number by utilizing only multiplication and subtraction operations. Each of these DFT samples is inverted by using the Newton Raphson division and finally followed up by the IDFT-15 transformations to get back the corrected correlation references in the time domain. These are then used by the Integrate and Dump Correlator (IDC) during the demodulation of the data, which is in detail explained in the Sec. 4.2.2.

### 3.6.3 Mathematical algorithm for DFT using PFA

The DFT is the primary transform used for numerical computations in digital signal processing. It is used for spectral analysis, fast convolution, frequency domain channel equalization, and many other applications. The DFT transforms  $N$  discrete-time samples





**Figure 3.28:** Inverse IDFT using Forward DFT engine.

$(x_n)$  to the same number of discrete frequency samples  $(X_k)$  [181]:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \quad n = 0, 1, 2, \dots, N-1. \quad (3.25)$$

As shown in Fig. 3.28, we use a forward Fast Fourier Transform (FFT) (i.e., “DFT-15”) engine to evaluate the IDFT. Here, we swap the real and imaginary parts of the sequences of the complex data to obtain the IDFT [182]. The IDFT transforms discrete-frequency samples to the same number of discrete-time samples. The IDFT has a form very similar to the DFT

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) e^{i \frac{2\pi nk}{N}}. \quad (3.26)$$

The computation of the direct DFT involves complex multiplication/addition, and the FFT can be only applied if the number of points to be calculated is a power of 2. A multidimensional DFT decomposition theory was developed by Good [183] to evaluate the DFT for non-power 2 points and eliminates the calculation of twiddle factors. The algorithms developed are radix-2 FFT, radix-4 FFT, Prime Factor Algorithm (PFA), Winograd Fourier transform algorithm (WFTA), and Singleton’s mixed-radix algorithm (MFFT). The usage of those algorithms requires considerably less calculations compared to a direct DFT computation.

In the above technique, a large one-dimensional DFT is decomposed into a number of small point DFT transforms. The multidimensional decompositions are only applicable to DFTs of length  $N$ , where  $N$  is factorable into integer values (i.e.,  $N = N_1 * N_2$ ). The PFA can be applied only if  $N_1$  and  $N_2$  are relatively prime (greatest common divisor is 1), i.e.,  $\gcd(N_1, N_2) = 1$ .

$$n = (K_1 n_1 + K_2 n_2) \bmod N \quad (3.27a)$$

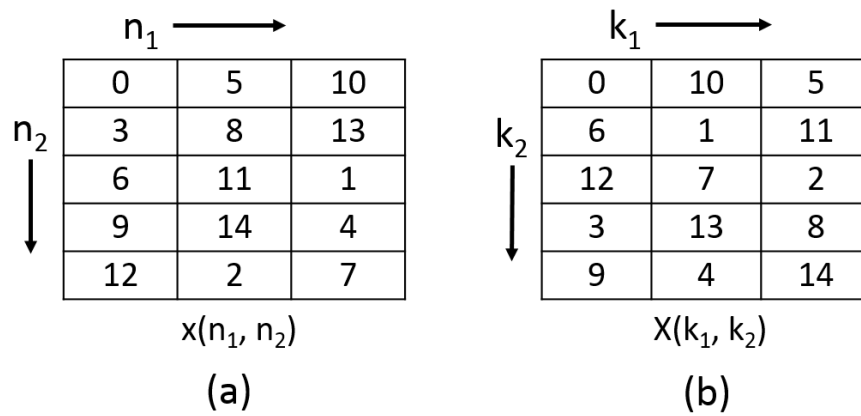
$$k = (K_3 k_1 + K_4 k_2) \bmod N \quad (3.27b)$$

$$n_1 = [0, 1, \dots, N_1 - 1] \quad (3.27c)$$

$$k_1 = [0, 1, \dots, N_1 - 1] \quad (3.27d)$$

$$n_2 = [0, 1, \dots, N_2 - 1] \quad (3.27e)$$

$$k_2 = [0, 1, \dots, N_2 - 1] \quad (3.27f)$$



**Figure 3.29:** The mapping of indices using Good's algorithm and Chinese remainder theorem.

where  $K_1 = aN_2$ ,  $K_2 = bN_1$ ,  $\gcd(K_1, N_1) = 1$  and  $\gcd(K_2, N_2) = 1$ . The 2D DFT is given as

$$X(k_1, k_2) = \sum_{n_1=0}^{N_1-1} \sum_{n_2=0}^{N_2-1} x(n_1, n_2) W_N^{K_1 K_3 n_1 k_1} W_N^{K_1 K_4 n_1 k_2} W_N^{K_2 K_3 n_2 k_1} W_N^{K_2 K_4 n_2 k_2}. \quad (3.28)$$

where  $K_1, K_2, K_3, K_4, N_1, N_2, a, b$  are integers.

The required conditions for a reduction of the DFT calculations and segmentation of a large DFT into small DFTs in the PFA algorithm are

- the required conditions for arithmetic savings, which do not involve the calculation of twiddle factors are  $K_1 K_4 \bmod N = 0$  and  $K_2 K_3 \bmod N = 0$ .
- the conditions to be changed into short-length transforms are  $K_1 K_3 \bmod N = N_2$  and  $K_2 K_4 \bmod N = N_1$ .

The re-arranging of indices in the time domain and the frequency domain can be done using the Chinese Remainder Theorem (CRT) [184, 185] and the Good's algorithm [183] respectively. The Prime factor 2D mapping of the indices is as shown in Fig. 3.29. Figure 3.29(a) depicts the time domain indices, and the values  $n_1/n_2$  are as in Eqn. (3.27c)/(3.27e) respectively. Fig. 3.29(b) depicts the frequency domain indices, and the values  $k_1/k_2$  are as in Eqn. (3.27d)/(3.27f) respectively.

We are evaluating DFT-15 for the channel deconvolution algorithm. Thus, the DFT of 15 points is split into 3-Point DFT and 5-point DFT. For example, the evaluation of

DFT of  $N = 15$  can be decomposed into two smaller DFTs of  $N_1 = 3$  and  $N_2 = 3$ .

$$\begin{aligned}
 n &= (5n_1 + 3n_2) \bmod 15 \\
 k &= (10k_1 + 6k_2) \bmod 15 \\
 5 &= K_1 = aN_2 = 5a \\
 3 &= K_2 = bN_1 = 3b \\
 \gcd(5, 3) &= 1 \\
 \gcd(3, 5) &= 1 \\
 10 &= K_3 = aN_2 = 5a \\
 6 &= K_4 = bN_1 = 3b \\
 \gcd(10, 3) &= 1 \\
 \gcd(6, 5) &= 1
 \end{aligned}$$

### 3.7 Summary

We have given an overview of spread spectrum systems, mainly DSSS and PSSS. A mathematical description of *m-sequences* and Kasami sequence was given, and also their correlation properties were discussed. An essential workhorse of the PSSS modulation are *m-sequences*. The orthogonality features of *m-sequences* are employed for a parallel transmission of the data in PSSS modulation. We have discussed comprehensively the functioning of PSSS modulation and the technique to perform channel equalization.

We have described the mathematical operations of PSSS encoding and decoding, along with a channel deconvolution operation. At the transmitter, PSSS encoding results are many discrete multi-level amplitudes. The occurrence probability of higher valued amplitudes is very low. The clipping of these amplitudes does not result in a significant loss of BER.

We have shown that the PSSS encoded signal can tolerate non-linear impairments caused by the PA and be still able to recover the transmitted signal by the usage of the RAPP-Model. The above analysis shows the high robustness of the PSSS modulation and its inherent ability to correct errors induced by non-linear effects by performing adaptive channel equalization at the receiver.

We have briefly introduced the concepts of carrier phase/frequency synchronization that can be designed in the digital-domain. And also we briefly introduced the analog-domain synchronization methodology adopted in the ‘‘PSSS system model’’ by using a Costas Loop.

The channel estimation method using *m-sequences* is described. We have used the FDE technique to compensate for the ‘‘effective channel’’ effects, including imperfections introduced by the RF-frontend electronics. The channel deconvolution can compensate for the nonlinear distortion and also clipping caused by the PA. The prime factor algorithm is used to evaluate DFTs for non-power of 2 points. This method can be implemented

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in Field Programmable Gate Array (FPGA) with a minimum number of resources as discussed in Sec. [5.1](#).

## Chapter 4

# PSSS transmitter and receiver architecture

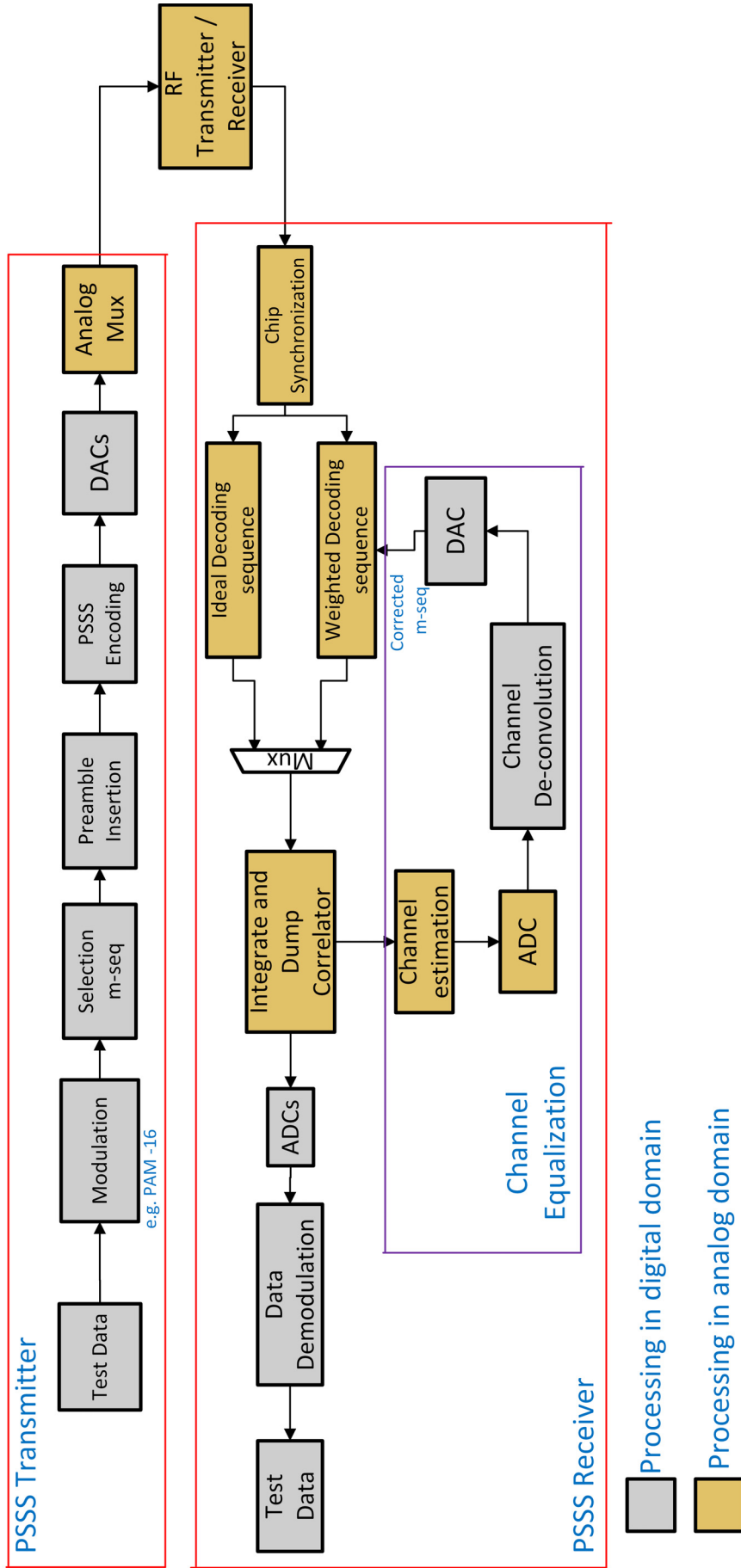
In this Chapter, we will discuss the complete architecture of the mixed-signal PSSS transceiver design, the synchronization using a Costas Loop, and the RF-frontends. Here, we also discuss the particulars of different components involved in the PSSS transceiver system.

We have to mention that the complete PSSS system transceiver architecture is the outcome of the three working groups in the Real100G.COM project. The PSSS baseband design was shared between Prof. Scheytt's group and Prof. Kraemer's group. The both groups were responsible for providing the 100 Gbps system parameters (s. Sec. 3.4.1). Prof. Kraemer's group was responsible for designing the digital part of the PSSS transmitter and also developing the channel equalization algorithm.

Prof. Scheytt's group was responsible for the PSSS baseband receiver implementation. The Costas loop synchronization was performed at baseband bandwidth by Prof. Kallfass group. We have used RF-frontends of 230 GHz/240 GHz from Prof. Pfeiffer and Prof. Kallfass groups, respectively.

### 4.1 PSSS transmission system

We have discussed the theory of different components involved in the PSSS transceiver system in Sec. 3.4. The PHY packet structure and the system parameters are given in Chap. 4. Figure 4.1 shows the individual working blocks of the PSSS transceiver system. On the transmit side, the bit-stream is parallelized and encoded with orthogonal codes. A MLS with length 15 is used as the orthogonal base code for the mixed-signal baseband implementation. A  $15 \times 15$  coding matrix is obtained by circularly shifting the base *m-sequence*. The length of the sequence and the number of bits encoded with a single code sequence (bit-loading) is determined according to the intended bit-rate, the available bandwidth and the required robustness of the system.



**Figure 4.1:** Block diagram of the PHY layer using PSSS modulation. The parts enclosed in the red box represent analog/mixed-signal processing components. The violet box shows the channel estimation.

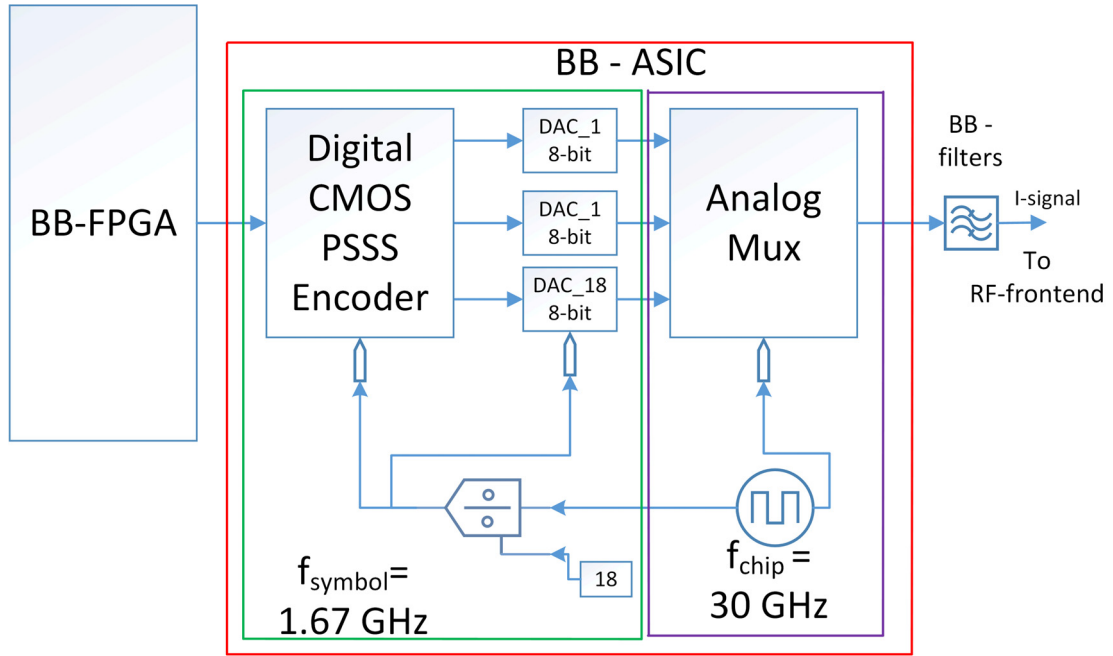
Now, the ‘‘PSSS Encoding’’ block adds up all chip values of all selected codes resulting in a discrete multivalued signal forming one PSSS symbol. One PSSS symbol consists of 15 chips and 3 chips of the cyclic extension (s. Tab. 3.2). A cyclic extension is required to reduce the ISI effects between adjacent PSSS symbols. This resulting multivalued signal is interfaced to an analog Mux by DACs operating at the PSSS symbol rate. Finally, the analog signal is up-converted to the carrier frequency and transmitted as shown in Fig. 4.1.

The PSSS system requires a coherent receiver that delivers a synchronous PSSS baseband signal (s. Sec. 3.5.1). The analog baseband signal needs to be phase-synchronized by using a set of preamble symbols. The use of a local Oscillator (LO) for the carrier recovery, as known from analog transmission systems, offers the advantage of independence from the modulation format. The local Oscillator (LO) signal of the receiving mixer is synchronized with that of the transmitting mixer by a phase-locked loop (PLL). The RF-frontends are used from the MILLILINK project [64] and the Real100G.RF project [186].

At the receiver, we use 15 parallel IDCs which perform both channel equalization and PSSS demodulation. The coefficients for the channel deconvolution are calculated in the digital domain. Since we assume that the channel coherence time is much longer than the symbol duration, we can use a low rate of DAC for the adaption of the deconvolution coefficients. Thus, in a mixed-mode analog/digital design, the receiver has a simplified design, in which the channel estimation and equalization is a classic analog cross-correlation as described in Ref. [133].

During the preamble transmission, the ideal decoding sequences (i.e. *m-sequence* known to transmitter and receiver) are used by a bank of parallel IDCs (see Fig. 4.1) to obtain the channel estimates. Here, the ideal decoding sequence means the unipolar decoding *m-sequence*, which is prior known to the receiver. Those estimates from the IDCs are converted into the digital domain by the ADC, and fed into the Channel Deconvolution (CDC) block. The CDC block calculates the corrected correlation references. This means that the CDC block evaluates new weights between 0 and 1, which are used by IDCs for correlation. The weights are calculated such that they reflect the inverse of the ‘‘effective channel’’ (for mathematical description s. Sec. 3.3.1). Thus, the ‘‘corrected m-sequence’’ shown in Fig. 4.1 reflects the new correlation sequence with a corrected weights. The ‘‘effective channel’’ consists of not only the channel impairments but also further impairments caused by the RF-frontend electronics.

After the down-conversion of the received signal to the baseband, the estimated channel coefficients do contain not only the linear distortion caused by the transmission channel but also the distortion of the RF-electronics (which is often non-linear). The deconvolution operation will not only correct the linear channel impairments but also (at least parts) of the non-linear dirty RF parts. For the correlation during the data transmission, the IDCs will use these corrected references to get the decoded data bits free from the channel impairments. Thus, CDC operation corrects all impairments of the



**Figure 4.2:** Baseband architecture of the transmitter. The blocks enclosed in the green box operate at a symbol rate of 1.67 GHz and the blocks in the violet box run at a chip rate of 30 Gcps.

“effective channel”.

## 4.2 Mixed-signal transceiver design

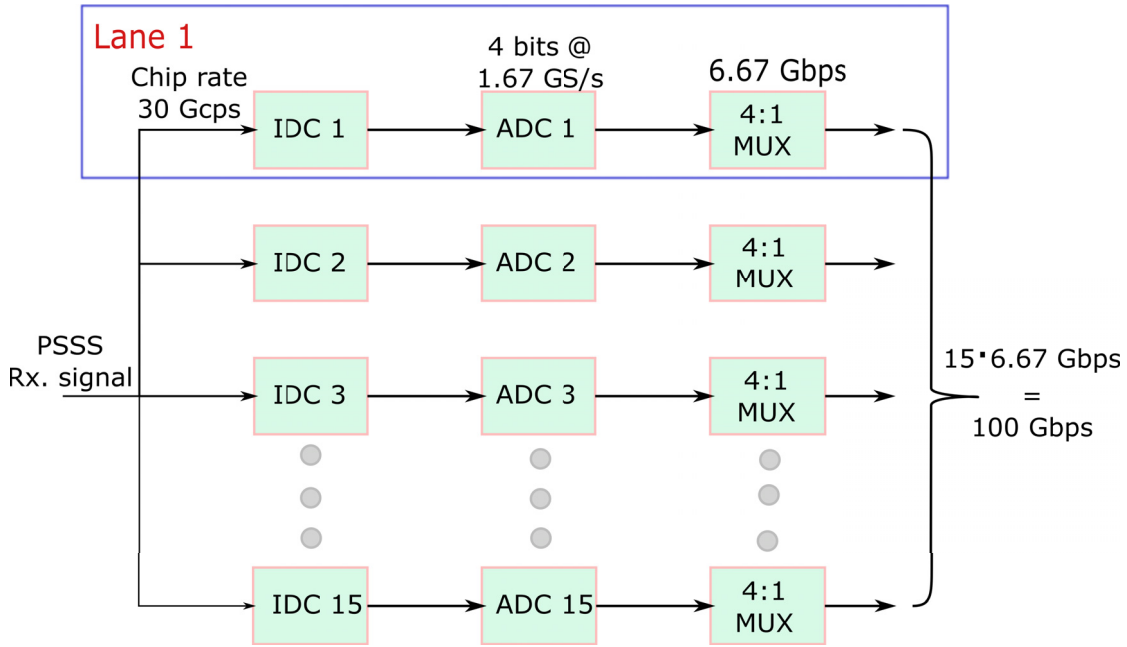
An analog-mixed signal baseband implementation for high data rate wireless communication offers several advantages, as discussed in Refs. [187, 188]. We have decided for PSSS as a baseband modulation scheme because the correlation and deconvolution operations can easily be realized in the analog domain. In contrast to a digital baseband implementation, we hypothesize that the mixed-signal design benefits from a decrease in the chip area and the power consumption. The PSSS modulation is well suitable for mixed-signal applications like the encoding of parallel data symbols and their combination into a multivalued PSSS stream in the transmitter, and the decoding of the received data using parallel IDCs. The channel equalization can be implemented using analog/mixed-signal circuitry, and the FDE is carried out in the digital domain.

### 4.2.1 Transmitter mixed-signal baseband processing

The basic concept of our mixed-signal baseband transmitter is shown in Fig. 4.2, and our work is published in Ref. [150]. The block diagram of the BB-ASIC to transmit data with PSSS modulation is shown in Fig. 4.2 (red color box). Since all transmission is performed in the real-domain, the I-signal is generated in the form of a differential signal with a chip-rate of 30 GHz and send to the RF-Frontend.

The block named “Digital CMOS PSSS encoder” performs most of the digital baseband





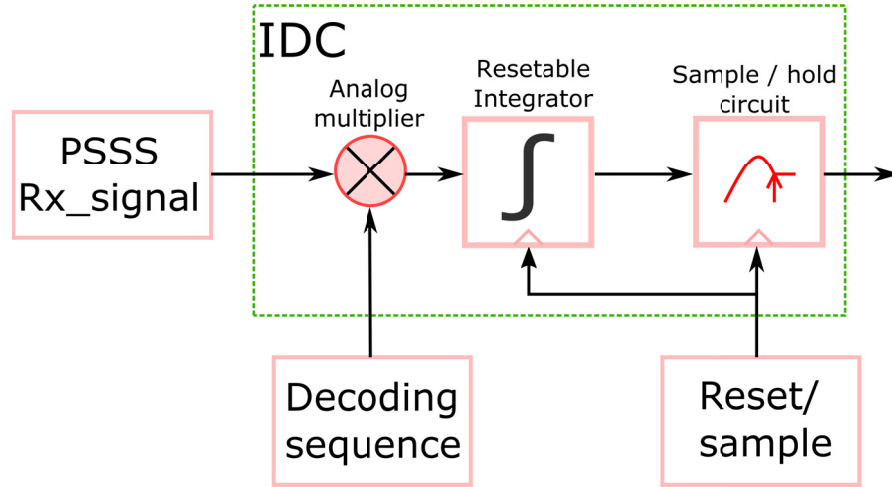
**Figure 4.3:** Baseband architecture of the receiver. The IDC uses the known MLS-15.

processing, including the spreading. Subsequently, the concurrent DACs are used to generate a current signal as an input to the broadband high-speed analog multiplier. These blocks operate at the PSSS symbol rate of 1.67 GHz.

The critical design parameter is the linearity and the bandwidth of the analog multiplexer, as it is operating at a chip rate of 30 GHz. The output of the multiplexer is connected to BB-filters that are used for spectrum shaping<sup>1</sup>. The implementation of the PSSS transmitter in FPGA and in ASIC is explained in detail in Sec. 5.2.

#### 4.2.2 Receiver baseband architecture

A mixed-signal PSSS receiver architecture is described in [49, 132]. This work was done by Prof. Scheytt's group. The received PSSS signal is decoded using 15 identical IDCs (IDC 1 to IDC 15) whereby each IDC consists of a programmable decoding sequence generator, an analog 15:1 MUX, an analog multiplier, a reset-table integrator, and a 4-bit ADC. As highlighted in Fig. 4.3, a single lane consists of an IDC module, an ADC operating at the PSSS symbol rate, and a 4:1 MUX to serialize the data. The collective data rate of all 15-IDCs results in a data rate of  $15 \times 6.67 = 100$  Gbps. The analog output of the IDC is fed to an ADC. The ADC has a sampling rate of 1.67 GHz and a bit resolution of 4 bits. Then 4:1 digital MUX is used to create a single stream of the digital data stream at 6.67 Gbps, and it can be interfaced with high-speed transceivers on FPGA.



**Figure 4.4:** Architecture of the analog integrate and dump the correlator circuit.

### Single IDC module

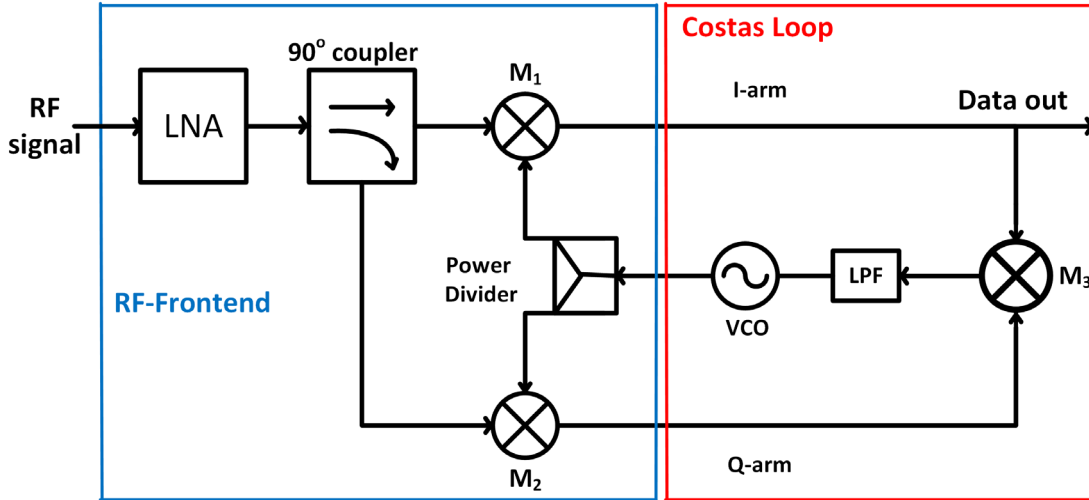
The crucial component in the PSSS receiver is the IDC module consisting of a broadband multiplier and a resettable integrator, as depicted in Fig. 4.4. The target parameters for the correlator are 30 GHz of bandwidth, sufficient linearity for the multi-level PSSS signal, a very high slew rate, and a short reset time (100 ps). One of the inputs to the analog multiplexer is a DC current signal [132], which are generated by the known decoding sequence, and the other is the incoming PSSS stream at 30 Gcps. The resettable integrator circuit integrates the output of the multiplier, and at the end of the integration time (which is  $N \times T_{chip} = 15 \times \frac{1}{30 \times 10^9 \text{Hz}} = 500 \text{ ps}$ ) it generates a cross-correlation result. A sample and hold circuit is placed before the ADC, as depicted in Fig. 4.4. The linear operating range of the sample/hold circuit should be corresponding to the final integrator output and should exhibit a low decay period. The ADC is operated at the PSSS symbol rate, and with a bit resolution same as the the targeted spectral efficiency (i.e., a bit resolution of 4 bits).

## 4.3 Synchronization in PSSS system

A fully coherent receiver architecture is utilized in the “PSSS system model”, as explained in Sec. 3.5.1. The basic operation of “Synchronisation” block in Fig. 4.1 is to retrieve the clock signal. This clock signal is used to drive the oscillator that performs I-Q down-conversion and also for the analog baseband processing unit.

The theory of Costas Loop was discussed in Sec. 3.5.4. Direct digital demodulation by Costas loops will provide a synchronous detector for PSSS-modulated signals. The use of a LO carrier recovery, as it is known from analog transmission systems [189], offers the advantage of independence from the modulation format. The local oscillator signal of the receiving mixer is synchronized with that of the transmitting mixer by a PLL.

<sup>1</sup>BB-filters are required to pre-distort the PSSS baseband signal to compensate for potential bandwidth limitation in the signal chain.



**Figure 4.5:** Costas loop synchronization for a spectral efficiency of 1 bit/sec/Hz or BPSK. A red box encloses the Costas loop, and the signal feeding from the RF-frontend is enclosed in a blue box. The multipliers  $M_1$  are  $M_2$  are sub-harmonics broadband mixers.

The core modules of a Costas loop are the following: A PLL, broadband mixers with up to 25 GHz bandwidth, a loop filter, a VCO, and a decision circuit that is implemented in the form of MMICs based on IHP ultra-fast SiGe BiCMOS technology [190]. In the following section, we will briefly describe the operation of a BPSK and a QPSK Costas loop. With a BPSK Costas loop, we can achieve a spectral efficiency of 1 bit/sec/Hz. Similarly, a QPSK Costas loop helps to achieve a spectral efficiency of 2 bit/sec/Hz. This work was done by Prof. Kallfass's group.

### 4.3.1 BPSK Costas loop

A direct down-conversion receiver is used to utilize the full RF bandwidth [186, 191], as the target carrier frequency is 240 GHz, and the chip rate is 30 Gcps. The carrier frequency and phase recovery are performed directly on the converted baseband signal. Hence, the Costas loop operates directly on the RF signal.

Figure 4.5 shows the block diagram of a BPSK Costas Loop along with a generic RF-frontend. The down-converted signal from the RF-frontend block (marked by blue color in Fig. 4.5) is fed into the Costas loop for synchronization (marked by red color in Fig. 4.5). It can be seen as a double-sided PLL, with an additional multiplier or so-called error detector ( $M_3$ ), which generates the error signal [192, 193]. The down-converting I-mixer ( $M_1$ ) and the Q-mixer ( $M_2$ ) act as phase detectors where the outputs are baseband signals whose amplitudes vary to the phase difference between the LO of the transmitter and the receiver [49]. The  $M_1$  and  $M_2$  mixers execute a non-linear frequency mixing, and  $M_3$  multiplies the amplitudes of the two input signals linearly. The signals over the I/Q – arms show the recovery of data along the I – arm as the Costas Loop reaches the locking state, and the data along the Q – arm goes to zero. A detailed explanation is given by our project partners (Prof. Kallfass's group) in Ref. [194].

### 4.3.2 PSSS receiver architecture with QPSK Costas loop

A Costas loop can also be modified to operate for a PSSS modulated signal with 2 bit/sec/Hz or for Quadrature phase-shift keying (QPSK) modulated signals. Since we send a repeated *m-sequence* as a preamble on I/Q channel, the receiver Costas loop gets locked during the preamble phase.

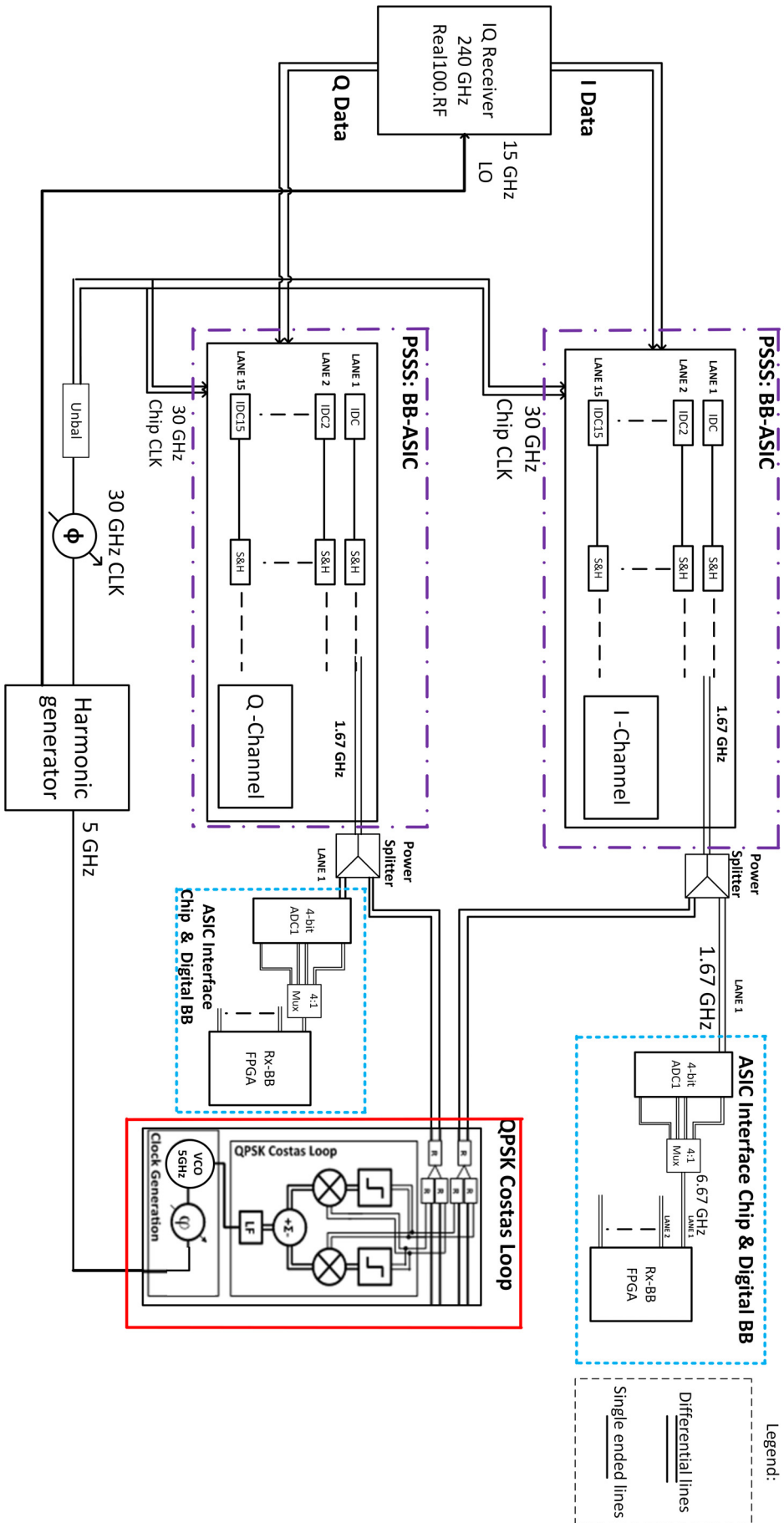
At the transmitter, the preamble consists of bipolar *m-sequences* on both I–Q channels. We have to note that bipolar *m-sequences* resemble a Non Return to Zero (NRZ) signal. The analog baseband QPSK Costas loop takes these bipolar signals as the input on I–Q channel and generates the required carrier frequency at its output during the preamble transmission phase.

The PSSS receiver architecture with a QPSK Costas loop setup is shown in Fig. 4.6. It consists of the following three main sub-blocks:

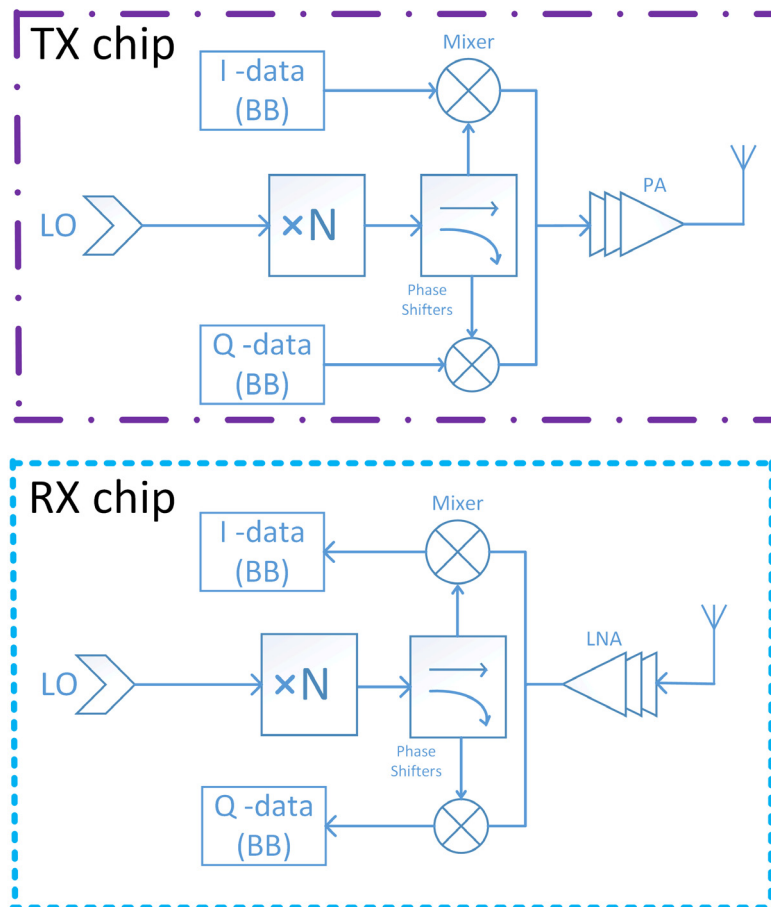
- **PSSS: BB-ASIC:** This unit performs an analog correlation on I/Q signals by using the a bank of IDCs. It is enclosed by violet color.
- **ASIC Interface Chip & Digital BB:** This block is responsible for the inter-connection of the analog baseband to the digital baseband. It is enclosed by blue color.
- **QPSK Costas Loop:** This block implement QPSK Costas loop synchronization. It is enclosed by red color.

The down converted signal from the I/Q receiver is routed to the “PSSS: BB-ASIC” blocks wherein the parallel IDCs perform an analog correlation with a known *m-sequence* pattern at a chip rate of 30 Gcps. The output from the lane 1 “PSSS: BB-ASIC” block from I-Channel (s. Fig. 4.6) is fed into the “Power Splitter”. The “Power Splitter” divides the signal into two parts: (i) part of the signal is fed into the “ASIC Interface Chip” followed by the “Digital BB” block (marked by blue color), (ii) and another part goes into the “QPSK Costas loop” (marked by red color). The above-operation is mirrored for the Q-channel.

A QPSK Costas loop consists of an error detector, a limiter, and an active power splitter. Their operations are detailed in our project partners (Prof. Kallfass’s group) article in Ref. [195]. The error detector is required to acquire the control signal for the VCO. A 5 GHz VCO is used as an input to the “Harmonic generator” block, as shown in Fig. 4.6. The “Harmonic generator” generates two clock frequencies, one for the LO (15 GHz) and another one for the chip-clock (30 GHz) for the analog “PSSS: BB-ASIC” block. Finally, the “ASIC Interface Chip and Digital BB” is responsible for the interface between the analog PSSS baseband and the digital baseband. The “4-bit ADC1” residing inside the logical block “ASIC Interface Chip and Digital BB” outputs 4-bits at a PSSS symbol rate of 1.67 GHz, and a “4:1 Mux” serializes the output from the ADC to a single stream of 6.67 Gbps. This high speed of 6.67 Gbps digital data stream is interfaced with a FPGA using high-speed GTH transceivers [196].



**Figure 4.6:** Costas loop synchronization for a spectral efficiency of 2 bit/sec/Hz or QPSK. It consists of an RF-frontend, a PSSS correlator, and a digital baseband.



**Figure 4.7:** Generic RF frontend circuit approach for the transmitter, and receiver based on frequency up-scaling methods.

## 4.4 RF-frontends

A high carrier frequency above 200 GHz can be employed to achieve an ultra-compact radio module with high data rates using an RF-bandwidth of 25 GHz to 40 GHz. At millimeter waves (mm-wave) frequencies, a complete RF-frontend is designed on a single chip and integrated into a single chip-package together with an antenna array [197, 198].

A generic block diagram of the I/Q direct down-conversion system is illustrated in Fig. 4.7. It comprises a frequency multiplier by  $N$ , direct up-/down conversion mixers,  $90^\circ$  phase shifters, PA and LNA. At the transmitter chip, a LO signal is brought up to the terahertz carrier frequency by a frequency multiplier  $N$ , and the sub-harmonic mixer modulates the incoming baseband data. Finally, the up-converted baseband signal is transmitted using the PA based on a wideband 4-way power combiner architecture [199]. At the receiver chip, almost the same structure as in the transmitter is repeated, except for the LNA.

We have used two RF-frontend systems in our HIL demonstration setup. The first RF-frontend system as described in [64, 66] has a LO signal of 20 GHz and  $12\times$  frequency multipliers (i.e.,  $N = 12$  in Fig. 4.7) enable an RF-frequency of 240 GHz. This was developed by Prof. Kallfass's group.

The second RF-frontend system is reported in Refs. [65, 186] and, has a LO signal of 14.375 GHz and  $16\times$  frequency multipliers (i.e.,  $N = 16$  in Fig. 4.7) enable to reach an RF-frequency of 230 GHz. This was developed by Prof. Pfeiffer's group.

## 4.5 Summary

In this Chapter, the architecture of the PSSS system was discussed in detail. It is composed of mainly three core components, a PSSS mixed-signal transmitter, a PSSS mixed-signal receiver, and a Costas loop for synchronization. At the baseband transmitter, the encoder performs most of the digital processing at the PSSS symbol rate of 1.67 GHz. At the baseband receiver, we perform channel deconvolution to evaluate the new correlation reference. These references are used by 15 parallel IDCs to perform channel equalization. The novel idea here is that we can use data converters (DACs/ADCs) at a relatively low symbol rate (1.67 GHz), which is facilitated by the PSSS modulation and achieve a data rate of 100 Gbps.

## Chapter 5

# Channel Deconvolution & PSSS transmitter: Implementation

In this Chapter, we will discuss the implementation aspects of the channel deconvolution, i.e., the evaluation of new correlation reference values for the IDCs and the hardware resources required to perform those operations. Firstly, we realize the algorithm on the FPGA and verify it using a “FPGA-in-the-loop” simulation. Finally, we synthesize the design on GlobalFoundries 28 nm ASIC technology. We published our work on the implementation of channel deconvolution in the digital domain in Ref. [200].

We describe a novel mixed-mode architecture where the transmitter baseband processing can be performed in both analog and digital domain. We published an article in Ref. [150] about how to design and implement a PSSS transmitter architecture to reach 100 Gbps.

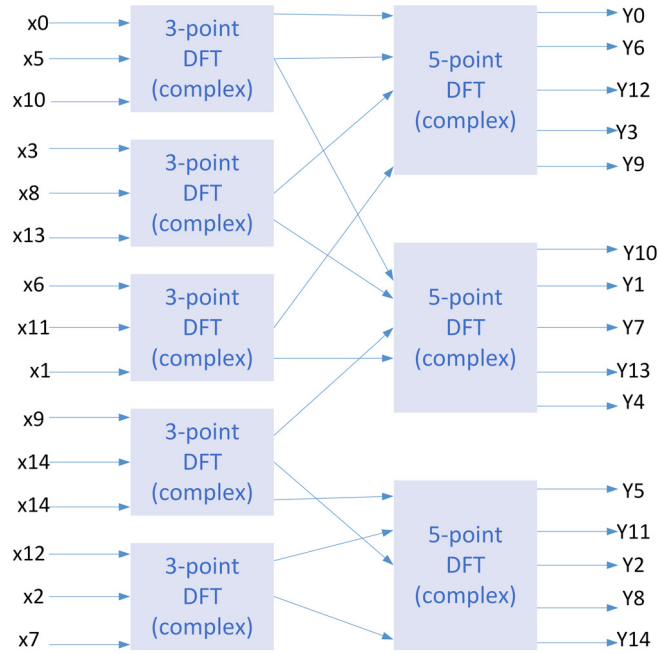
### 5.1 Implementation of channel deconvolution

In Chap. 4, we discussed the overall PSSS transmission system (s. Fig. 4.1). The channel estimates are obtained in the analog domain, and those estimates are fed through the ADC running at the PSSS symbol rate of 1.67 GHz to the “Channel deconvolution” block. The “Channel deconvolution” block evaluates the new correlation reference values in the digital domain. These new correlation reference values are converted to analog values by a DAC operating at the PSSS symbol rate of 1.67 GHz. The evaluated values are then stored in the parallel IDCs (s. Sec. 4.2.2 and Fig. 4.3).

#### 5.1.1 DFT-15: Realization

The theory of channel deconvolution is discussed in Sec. 3.6. An overview of the channel equalization procedure is described in the Sec. 3.6.1, and specifically illustrated in Fig. 3.27. As clarified in Sec. 3.6, a DFT of 15 points can be divided into small DFTs of 3 and 5 points according to the Prime Factor Algorithm (PFA) algorithm, which is

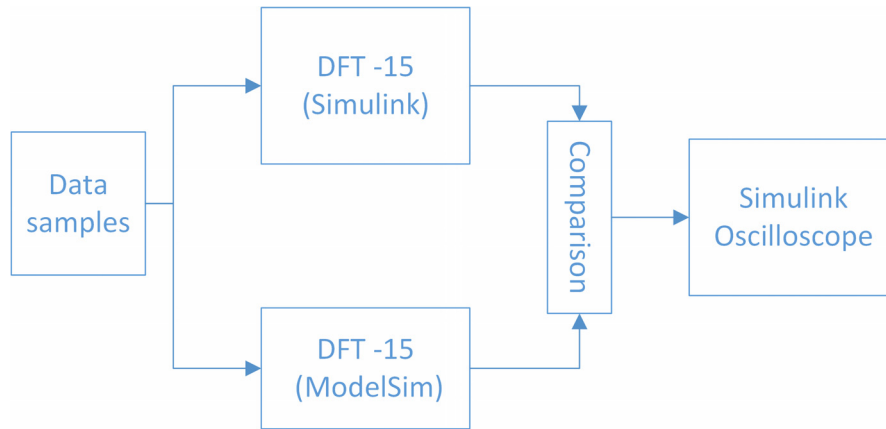




**Figure 5.1:** A graph illustrating a 15-point complex DFT using the PFA algorithm.

depicted in Fig. 5.1. The central notion for computing a short length DFTs is to scale down the issue from evaluating the twiddle factor into a calculation of cyclic convolutions. There are many efficient algorithms that exist for performing circular convolutions, and they can be all employed to evaluate a DFT [184]. It was shown by Rader [201] that if  $N$  is prime, the  $N$ -point DFT can be evaluated by performing  $(N - 1)$  point circular convolutions. The problem of evaluating the circular convolution of two sequences can be viewed as a polynomial multiplication problem [202]. For the evaluation of the short length DFTs, the algorithms have been derived and are explained in Ref. [185] and [203]. For a short length DFT of  $N$ -points (if  $N$  is prime), an efficient algorithm called Prime Factor Algorithm (PFA) was introduced by Burrus [204, 205], which requires fewer arithmetic operations (i.e., combined additions and multiplications).

According to Ref. [205], a 3-point complex DFT requires a 4 real multiplications and 12 real additions. A 5-point complex DFT requires 10 real multiplications and 34 real additions. The PFA algorithm was modified during this work to perform a *complex DFT of 15-points*. A complex DFT of 15 points requires five 3-Point complex DFT blocks and three 5-point complex DFT blocks, as shown in Fig. 5.1. The indices sorting at the input of DFT-3 blocks is based on the Good's algorithm [183] as illustrated in Fig. 5.1. At the output, the transformed values read out from DFT-5 blocks are indexed using the Chinese remainder theorem [206]. To evaluate a complex DFT-15 requires 50 real multiplications  $((4 \times 3) + (10 \times 3))$  and 162 real additions  $((12 \times 5) + (34 \times 3))$ .



**Figure 5.2:** DFT-15 Co-simulation model with Simulink and Modelsim.

**Table 5.1:** Logic utilization of DFT-15.

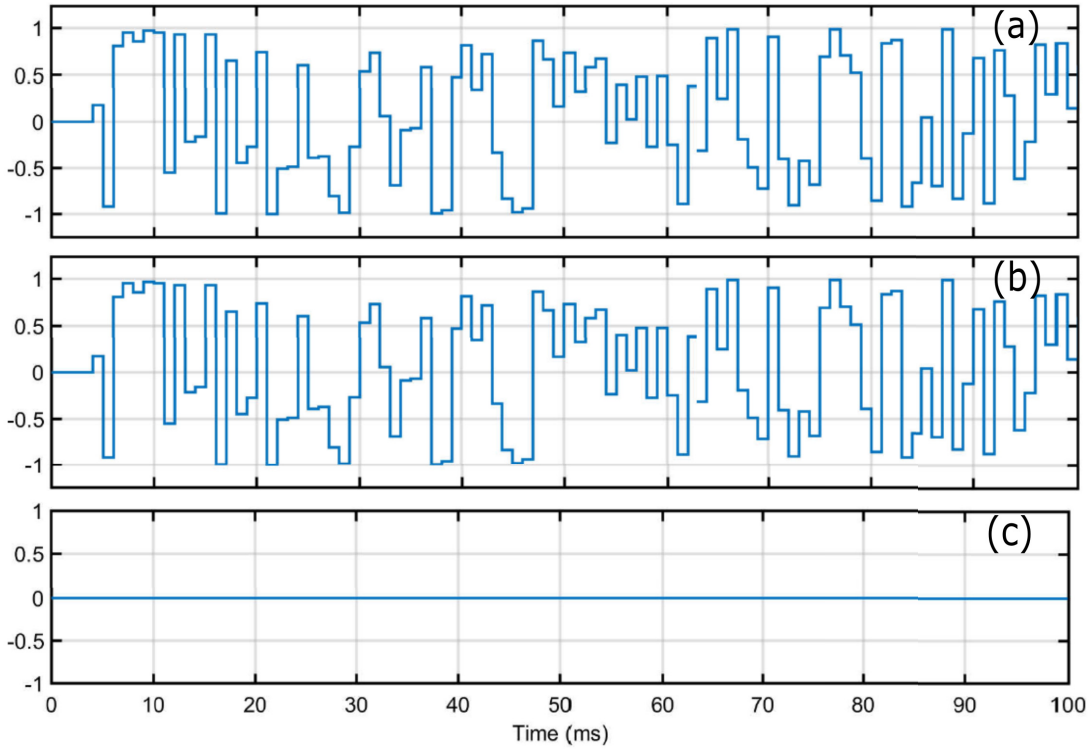
	Utilized	Available	Utilization percentage %
LUT	2146	537600	0.4
FF	1059	1075200	0.1
DSP	50	768	6.51

### DFT-15: FPGA Implementation

The DFT is the vital core module that needs to be optimized for implementation in order to achieve high-speed channel equalization. Figure 5.2 shows the co-simulation of the DFT-15 model developed in Simulink with the VHDL code of DFT-15 simulated on ModelSim, i.e., the two simulations are performed concurrently and the results are compared. We developed a 64-bit model (double data type) of the DFT-15 model in Simulink. A 16-bit fixed-point representation was selected to represent the complex DFT-15 input/output signals. Both implementation use the same model as shown in Fig. 5.1. Only the value representation is different. This is of course important for the comparison of the results.

Using the HDL-Coder [207], the simulink code was translated to RTL code. The generated 16-bit resolution RTL code of DFT-15 was executed on ModelSim and compared with the Simulink model by a co-simulation engine. Fig. 5.3 illustrates the comparison result for one of the 15 transformed outputs, namely  $Y_9$  (s. Fig. 5.1). Figure 5.3(a) shows the output from the Modelsim model, using the 16-bit fixed-point representation, Fig. 5.3(b) depicts the output from the Simulink model, using the higher resolution floating point representation, and Fig. 5.3(c) shows the error signal. Although the error signal in Fig. 5.3(c) is displayed as zero, it is in the order  $10^{-10}$  and it cannot be seen in the Fig. 5.3(c) due to the scaling of the y-axis. From Fig. 5.3(c), we can conclude that the generated VHDL code has sufficient bit-resolution to reproduce the results from the floating point model.

From the generated RTL code, we synthesized and implemented the DFT-15 model on a Xilinx VCU108 FPGA board [196]. The design runs at 200 MHz clock frequency.



**Figure 5.3:** A Co-simulation result between the DFT-15 ideal Simulink model and the VHDL design simulated on ModelSim. The clock frequency is 200 MHz, and the y-axis shows the unit-less magnitude of evaluated DFT values.

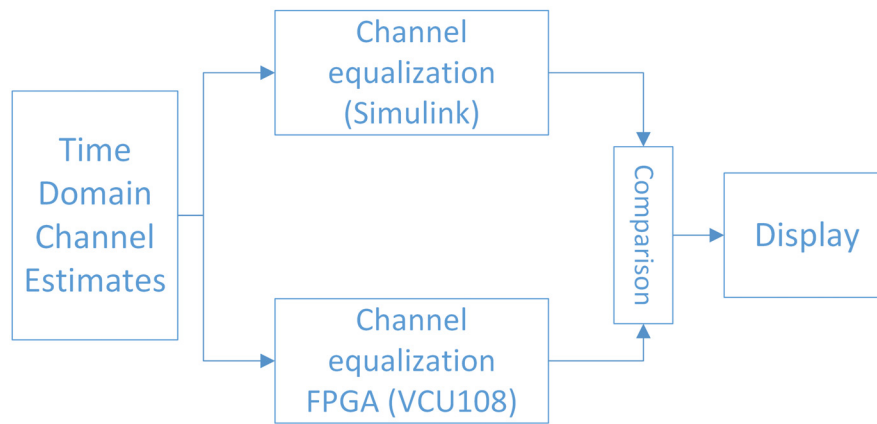
Tab. 5.1 shows the hardware utilization of the complex DFT-15 design on the VCU108 board. The model is extremely parallelized. Each DFT-3/DFT-5 modules in Fig. 5.1 is implemented using basic multiplication and an addition blocks. In total, there are 8 parallel DFT blocks operating at the same time to reduce the latency. As a result of the extreme parallelization, we notice a moderate usage of DSP cores (6.5%), whereas Look-Up-Tables (LUT) and Flip Flops (FF) occupy less than 1% of the design area. Even though, the DSP cores usage of 6.5 % appears to be a low number, we have to note that the VCU108 FPGA board (high-end board from Xilinx) has 768 DSP cores when compared with the Artix-7 board (entry board from Xilinx) [208] which has 90 DSP cores.

A hardware comparison with different FPGA implementations of a DFT-15 is shown in Tab. 5.2. In the above Tab. 5.2, R.A denotes real adders, R.M denotes real multipliers, and BRAM is the Block RAM. We want to compare the amount of logic cells with the achieved latency. As we can see in Tab. 5.2, we use a moderate amount of logic cells, on the other hand, we achieve very low latency of 1 clock cycle. A low latency and high-speed design is the core requirement for 100 Gbps system.

As shown in Tab. 5.2, our DFT-15 implementation requires more R.A/R.M compared to any other implementation, but it has a very low latency of only *one clock cycle*. Since no external memories are used in the design, it contains only pure logic like VHDL statements/branches. The low-latency enables the DFT-15 core to operate at a high

**Table 5.2:** Performance comparison.

	R.M	R.A	Latency (in clock cycle)	Memory (BRAM)	LUT	Clock Fre- quency (MHz)
This work	50	162	<b>1</b>	–	20346	<b>200</b>
Xilinx IP Core [209]	16	79	62	7	11570	122.8
GMR [210]	26	82	13	5	23807	122.8
Chen [211]	44	108	11	7	16151	122.8

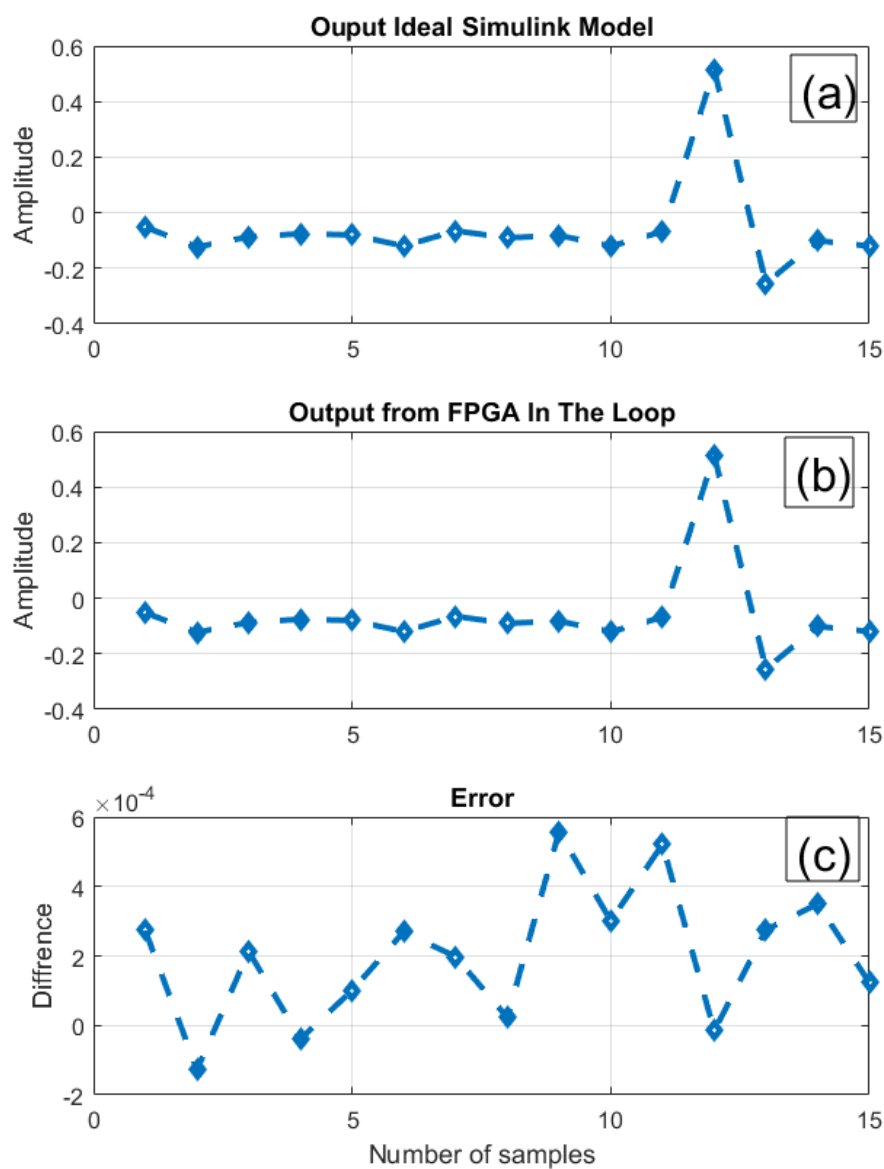
**Figure 5.4:** FPGA-In-The-Loop Simulation Model.

clock frequency of 200 MHz because there is no memory read/write access operation.

### 5.1.2 Channel equalization: Implementation

The channel equalization method was described in Sec. 3.6.1 (s. Fig. 3.27). It consists of a DFT-15 module, a reciprocal unit which is implemented using the Newton-Raphson approximation algorithm [178], and finally an IDFT-15 module which gets back the samples in time-domain. The VHDL code for the complete channel equalization generated using the Matlab HDL coder is described and compared with a floating point channel equalization model in Simulink.

The time-domain channel estimates are obtained from the measurement experiments with the 240 GHz RF-frontend module from TU Stuttgart (s. Sec. 6.3.2 and Fig. 6.5). As shown in Fig. 5.4, the measured channel estimates are fed into both Simulink and FPGA models. We choose a 16-bit fixed point representation for the input/output signals as well as for the block named “Channel Equalization FPGA (VCU108)” in Fig. 5.4. It operates at a clock rate of 166.67 MHz on the VCU108 board. The output from “Channel Equalization FPGA” / “Channel Equalization (Simulink)” block gives the new correlation reference values to be used by the IDCs (s. Fig. 4.3). These two results, the “data from



**Figure 5.5:** Channel equalization verification on a VCU108 board and comparison of the data from the ideal Simulink model to the data recorded from the FPGA.

Simulink models” and the “data from the FPGA” are compared using the tool Simulink scope.

A comparison between the correlation reference results obtained by the Simulink model and the results from the FPGA is shown in Fig. 5.5. The output from the reference model (Simulink model) with 64-bit floating point representation is depicted in Fig. 5.5(a), and Fig. 5.5(b) demonstrates the output captured from the FPGA by an “FPGA-In-The-Loop” simulation using the “Data Capture” module from the HDL Coder/HDL Verifier [207]. Finally, Fig. 5.5(c) depicts the error between these measurements in the order of  $10^{-4}$ .

Table. 5.3 shows the hardware utilization of the complete channel equalization module

**Table 5.3:** Logic utilization of the channel equalization module.

	Utilized	Available	Utilization percentage %
LUT	14656	537600	2.73
FF	33364	1075200	3.1
DSP	247	768	32.16
LUTRAM	223	76800	0.29

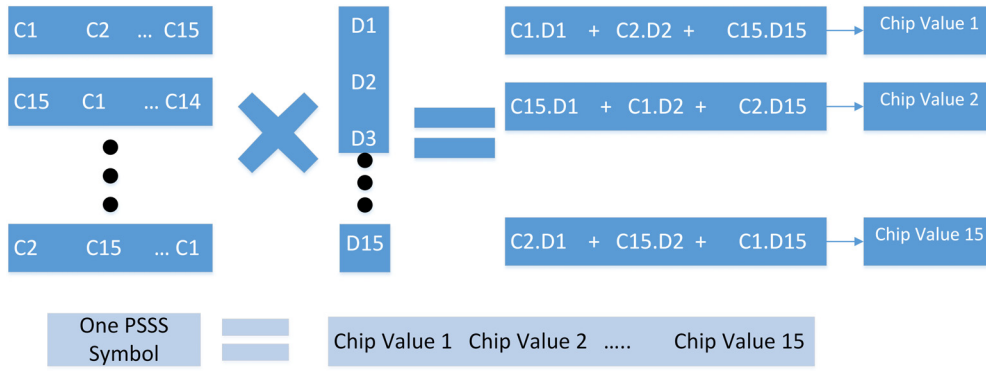
**Table 5.4:** Digital ASIC synthesis.

	IHP 250 nm [212]	IHP 130 nm [190]	Nangate 40 nm [213]
Clock Period (ns)	15	11.3	6.3
Frequency (MHz)	66.67	85	158
Area ( $\mu m^2$ )	9504354	2988756	278630
Power (mW)	415	63	20.8

(s. Fig. 6.5) on a VCU108 board. The main target of the design is a very low latency and a high clock frequency. To accomplish these design criteria, we highly parallelized the channel equalization module. The higher parallelization leads to the usage of more hardware blocks. The DSP utilization is 32%, the usage of LUT is 2.7%, and the usage of 1-bit registered FFs is 3%. However, the amount of generated blocks is still moderate and can be accepted. The reason for a moderate utilization of the DSP resources is that we implement a fixed point integer divider using Newton Raphson method to evaluate the reciprocal of each DFT sample. It is essential to ensure the high numerical integrity of the operation as it decreases the error threshold minimum as shown in Fig. 5.5(c). We also achieve a very low latency of *one clock cycle* and a clock frequency of 166.67 MHz.

The primary motivation of synthesizing the “Channel equalization” design in digital ASIC technology was to validate how close we can come to the target PSSS symbol frequency of 1.67 GHz [132]. We have discussed the PHY packet structure in Sec. 3.4.1. We have used 50 PSSS symbols in the preamble for channel estimation and equalization. Ideally, if we operate the channel equalization in ASIC at the PSSS symbol rate, it results in a reduction of the preamble length. An increased speed of the channel equalization design for 100 Gbps system results in a smaller number of preamble symbols to be transmitted. This, in turn, reduces the transmission overhead and thus effectively increases the transmitted data rate.

We used the generated VHDL code from the HDL Coder for the channel equalization block and synthesized it using a Synopsis DC ultra-compiler [214] on different ASIC technologies. The results of the compiler are linked with libraries from different technologies to estimate the area, speed, and power dissipation as shown in Tab. 5.4. The PSSS receiver chip (s. Sec. 4.2.2: Fig. 4.3) is designed in IHP 130 nm technology with a symbol rate of 1.67 GHz. If we compare with IHP 130 nm technology, the synthesized code runs at  $\frac{1}{20^{th}}$  (s. Tab. 5.4: clock frequency 85 MHz) of the PSSS symbol rate. As we can see in the Tab. 5.4, the best results are achieved using the open source cell library Nangate 40 nm



**Figure 5.6:** An illustration of a PSSS-15 modulation with a circular coding matrix formed by MLS-15.

technology. This code runs at 158 MHz.

We can improve the channel equalization speed by using GlobalFoundries 28 nm FDSOI technology. Utilizing this technology, we might operate the channel equalization module close to the PSSS symbol rate (1.67 GHz). Although this is not required because there is no need to estimate the channel in every PSSS symbol. Since we assume the channel is static over a one PHY packet, i.e., packet transmit time is shorter than the channel coherence time.

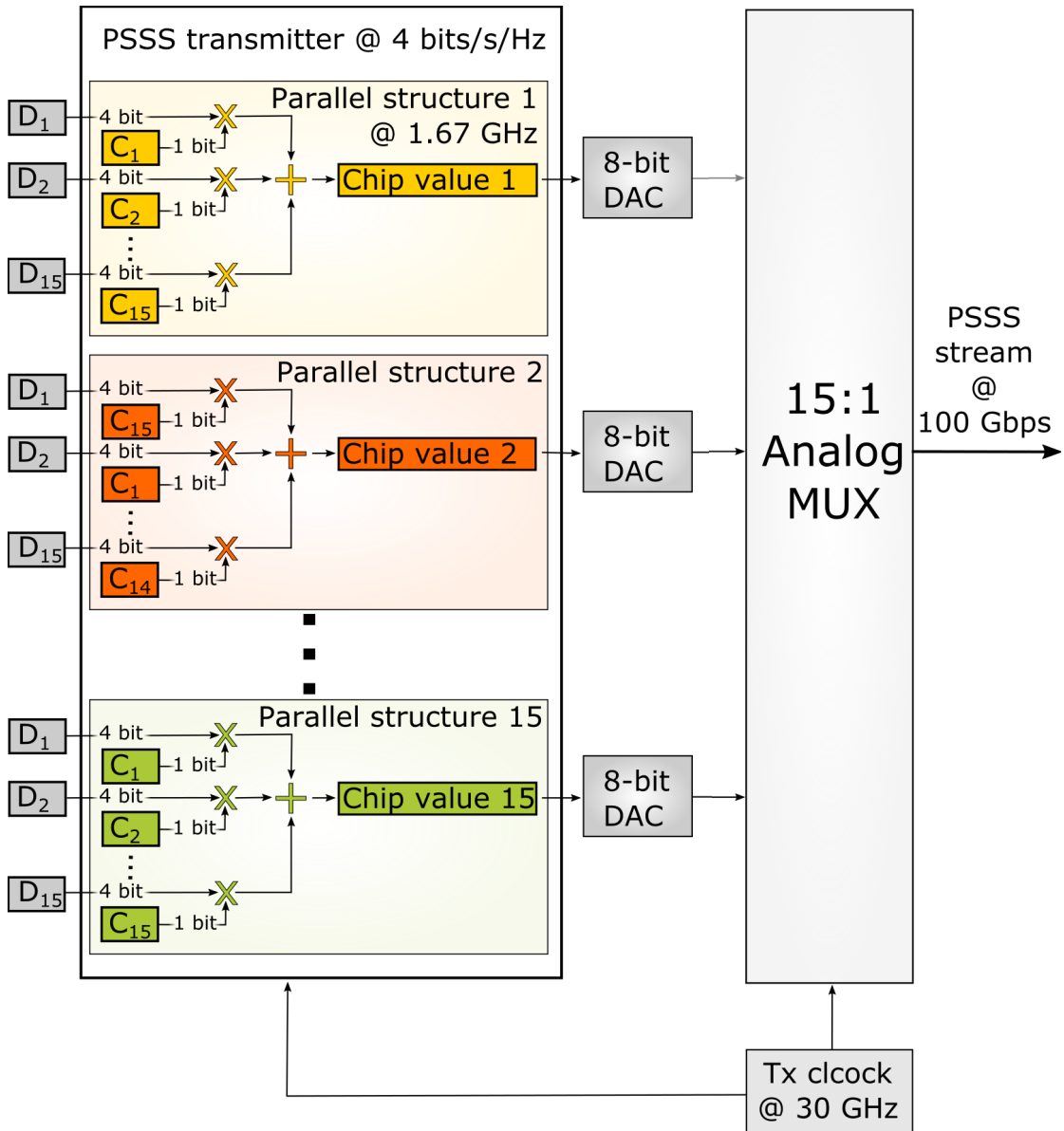
## 5.2 PSSS transmitter implementation

To the best of our knowledge, a PSSS transceiver IC implementation exists only for the IEEE 802.15.4-2006 standard [130] which operates in the 868 MHz band and achieves 250 kb/s [131]. In Sec. 4.2.1, we give an overview of the PSSS transmitter mixed-signal baseband processing. The PSSS modulated output signal with PAM-16 at a chip rate of 30 Gcps results in a 100 Gbps data rate. In this section, the PSSS transmitter module is verified on FPGA and synthesized on ASIC.

### 5.2.1 PSSS transmitter architecture

Before jumping into the details of the PSSS transmitter architecture, we would like to introduce the mathematical concepts which help to implement the parallel transmitter design in hardware. As explained in Sec. 3.3, the input data symbols are divided into segments  $D$  of length  $N$  where  $N$  is equal to the length of the  $m$ -sequence (which is 15). The input data symbols are modulated with PAM-16.

Figure 5.6 shows the formation of a PSSS symbol from the cyclic matrix and the input data vector. We notice that one PSSS symbol consists of 15 chip values. Each chip value is generated by different shift combination of  $m$ -sequences. An essential point to observe is that the data symbols stay constant for the complete PSSS symbol. To illustrate this point, a chip-value 1 is generated by an  $m$ -sequence with the following pattern ( $C_1 C_2 C_3 \dots C_{15}$ ) and a chip-value 2 is generated by the  $m$ -sequence with the resulting



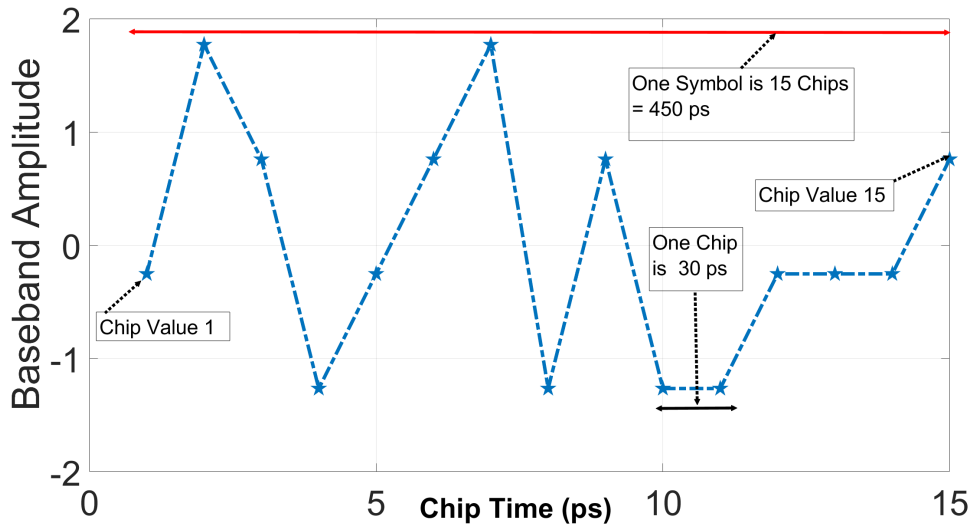
**Figure 5.7:** PSSS transmitter architecture with a chip-rate of 30 Gcps and a PSSS symbol rate of 1.67 GHz.

design shifted by one value ( $C_{15} C_1 C_2 \dots C_{14}$ ), and so on. Thus, the above-procedure facilitates a parallel structure implementation of the PSSS modulator in hardware.

A data symbol is fed to 15 parallel structures each consisting of a multiplier and a subsequent adder as depicted in Fig. 5.7. The input data vectors are multiplied with corresponding shifts of the *m*-sequence in each parallel structure. Each chip-value is generated by an adder in each parallel structure that computes the sum over the vector<sup>1</sup>. For example, the “Parallel structure 1” block, which is marked in the yellow color in Fig. 5.7 generates chip value 1 and the “Parallel structure 15” block, which is marked in

<sup>1</sup>This vector is the product of the data vector and the corresponding shifted *m*-sequence pattern, e.g., in a sub-block named “Parallel Structure 1”, a dot product of ( $C_1 C_2 C_3 \dots C_{15}$ ) and ( $D_1 D_2 D_3 \dots D_{15}$ ) leads to the above-vector.





**Figure 5.8:** Output of the PSSS transmitter observed at the output of an Analog Multiplexer.

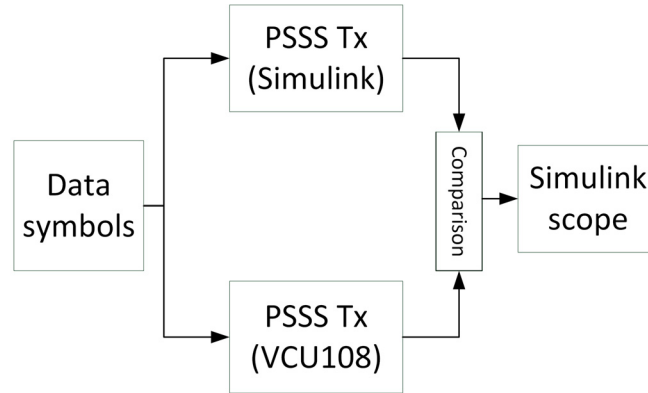
green color in Fig. 5.7 produces chip value 15.

The complete PSSS transmitter is split into two parts, one titled “PSSS transmitter @ 4 bit/s/Hz” is designed in the digital domain and the other is a “15:1 Analog Mux” which is developed in the analog domain. All blocks in the “PSSS transmitter @ 4 bit/s/Hz” operate at the PSSS symbol rate of 1.67 GHz (s. Tab. 3.2) and the output of these blocks are 15 chip values forming one PSSS symbol. These chip-values are fed into an “Analog MUX” via 8-bit DACs running at 1.67 GHz. The analog MUX is clocked with 30 GHz and the block named “PSSS transmitter @ 4 bit/s/Hz” obtains an 1.67 GHz clock signal from the same oscillator driving the analog MUX (30 GHz), as depicted in Fig. 5.7. The analog MUX serializes the output signal of the DACs at a chip rate of 30 Gcps. Thus, with a chip-rate of 30 Gcps and spectral efficiency of 4 bit/s/Hz, we can achieve 100 Gbps data-rate.

An example output of the PSSS modulated signal is illustrated in Fig. 5.8. It shows a PSSS symbol having 15 different chip-values, and the duration between each pair of chip-values is 30 ps. Thus, one PSSS symbol consists of 15 chip-values, and it lasts for 450 ps. In Fig. 5.7, each parallel structure holds its corresponding chip-value for 450 ps, while the high-speed analog MUX reads those values in 30 ps intervals.

### 5.2.2 PSSS transmitter architecture: FPGA verification

We verified the entire PSSS transmitter structure, as described in Fig. 5.7 including DACs and analog MUX on Xilinx VCU108 FPGA board [196]. Figure 5.9 shows the approach used to verify the PSSS transmitter design by comparing the output results of the data captured on the FPGA board to the data generated by the Simulink model. The Matlab HDL coder automatically generates VHDL code from the PSSS transmitter module. The output of each “Parallel Structures” block (in Fig. 5.7) is connected to the “15:1 Analog Mux” by 8-bit DACs. This is the reason to select an 8-bit fixed point representation for



**Figure 5.9:** FPGA-In-The-Loop data-capture using the Xilinx VCU108 FPGA board Model.

**Table 5.5:** Logic utilization of PSSS transmitter module.

	Utilized	Available	Utilization percentage %
LUT	1893	537600	0.35
FF	1275	1075200	0.12

the input/output signals for the “PSSS Tx (VCU108)” block in Fig. 5.9. The “PSSS Tx” runs at a chip rate of 454 MHz. The PSSS symbol clock frequency is 25.23 MHz  $(15 + 3)/454$ , since we have selected 3 chips for the cyclic prefix. The design has a latency of 15 chip-clock cycles,

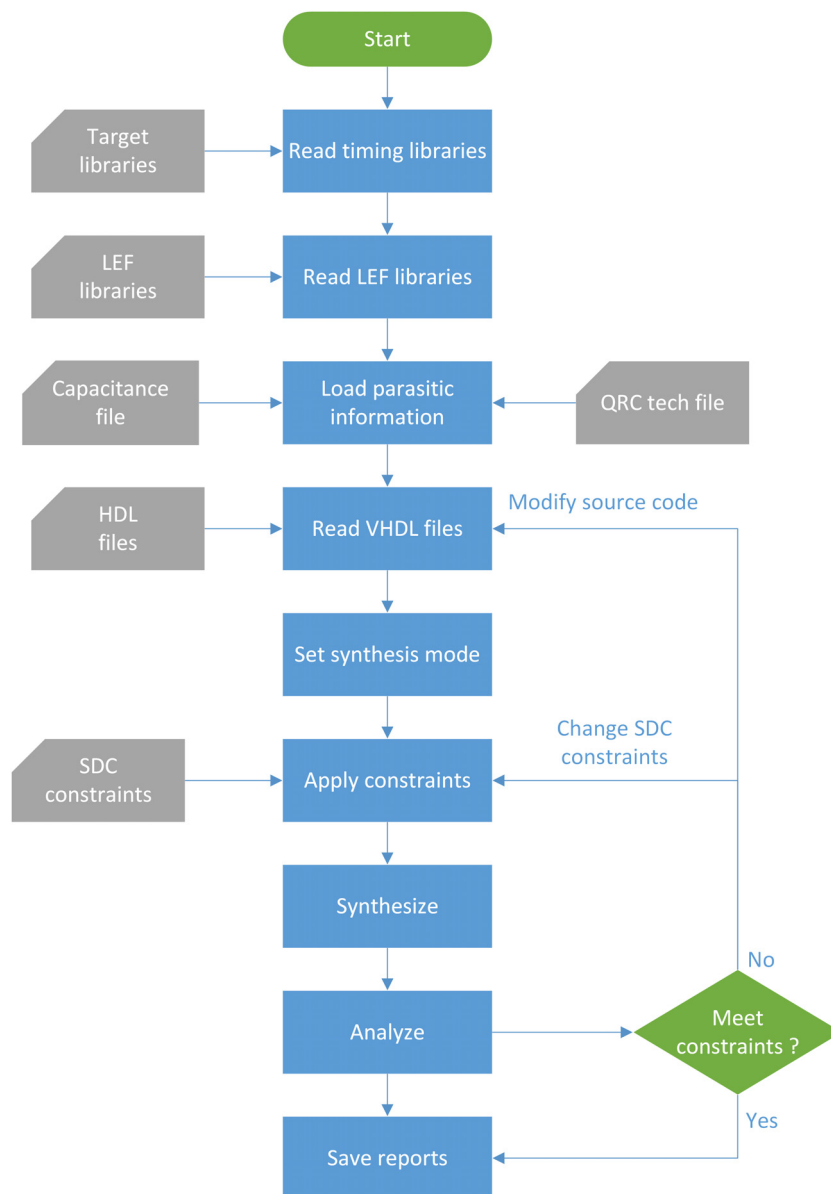
$$(15) \times \left( \frac{1}{454\text{MHz}} \right) = 0.034\mu\text{s}.$$

In Fig. 5.9, the block named “PSSS Tx (VCU108)” employs an 8-bit fixed-point data type. The “PSSS Tx (Simulink)” is based on a 64-bit floating point data type. We have compared the PSSS modulated signal emerging from those two blocks above, showing a perfect agreement.

Tab. 5.5 displays the logic area utilization of the PSSS transmitter architecture on the VCU108 board. Since we have employed a parallel architecture for the PSSS transmitter, we achieved a low latency of 15 clock cycles. The designed area occupied on the VCU108 board is very small i.e., only 0.35% of LUT is used and the FFs occupy 0.12% of the total available area on the FPGA. We also notice that the design does not require any DSP slices or memory units (like Block RAM). Thus, the PSSS transmitter architecture is simple, and is easily portable onto ASIC technology to realize the target PSSS symbol rate of 1.67 GHz.

### 5.2.3 PSSS transmitter architecture: ASIC implementation

The ASIC synthesis flow was performed using the Cadence Genus tool on Global-Foundaries 28 nm FDSOI technology. Figure 5.10 shows the flow chart for synthesizing VHDL/RTL design files (obtained by Matlab HDL coder) to Physical layout estimation



**Figure 5.10:** ASIC Synthesis flow with Cadence Genus tool for physical layout estimation.

(PLE). Commonly, in the case of most synthesis tools, there is no 1:1 matching for the estimation of parameters (like area, power, timing) between the wire-load models and the physical information of the model. PLE uses physical information to represent the effects of placement depending on the current VHDL design file. Embedding physical layout design into the synthesis will help to further reduce the cyclic repetition between the frontend and the backend ASIC design process. The PLE, which we perform, uses the physical information to model the effects of parasitics (resistance, capacitance).

The timing libraries and Library Exchange Format (LEF) libraries are obtained from the GlobalFoundries 28 nm process, as shown in Fig. 5.10. The QRC technology file and the capacitance table contain the parasitic information of the GlobalFoundries 28 nm FDSOI technology. The RTL files are automatically generated by the HDL coder from the Simulink model. We have three synthesis modes available in the Cadence Genus tool,

**Table 5.6:** Results for various synthesis mode.

	<b>syn_generic</b>	<b>syn_map</b>	<b>syn_opt</b>
Critical path slack ( <i>ps</i> )	245	41	18
Total area ( $\mu\text{m}^2$ )	11379	6041	5949

- Syn\_generic: The design is mapped using generic gates.
- Syn\_map: Maps the design to the cells onto the GlobalFoundries 28 nm technology library based on the LEF library and also performs a logic optimization.
- Syn\_opt: This option executes the gate level optimization resulting in a reduction of the timing on critical paths and a recovery area on non-critical paths.

The constraints are specified in the Synopsys Design Constraints (SDC) file, and they are imported into the Cadence Genus tool. Then we perform the synthesis of the “PSSS transmitter” module and verify if the design constraint is met. If the timing constraints are not matched, either we have to change the source code in Simulink or to change the synthesis option in the Cadence tool until we reach the target PSSS symbol frequency of 1.67 GHz.

In Fig. 5.7, we have implemented a block named “PSSS transmitter @ 4 bit/s/Hz” which consists of 15 parallel PSSS encoders. We have not designed the *parallel DACs* and the *15:1 analog MUX*. The results of the PSSS transmitter design on GlobalFoundries 28 nm are:

- The total area occupied is 0.0073 mm<sup>2</sup>.
- Power: 20.867 mW + 0.015 mW (leakage power) = 20.882 mW.
- The maximum clock frequency achieved is 1.785 GHz or clock period is 560 ps.

Tab. 5.6 summarizes the main results (like critical path and total area) for different synthesis modes, and the operating PSSS symbol clock frequency is 1.785 GHz. As we can observe from the Tab. 5.6, the best results are obtained by selecting the *syn\_opt* mode, where both area and critical path are optimized. Thus, the digital unit of the PSSS transmitter (s. Fig. 5.7) has an energy efficiency of 0.21 pJ bit<sup>-1</sup> to achieve 100 Gbps data rate.

### 5.3 Summary

We designed and implemented a high-speed channel equalization algorithm wherein we evaluate new correlation reference values for the IDCs. The time-domain channel estimates were obtained by the measurement experiment with a 240 GHz RF system. These channel estimates were used to validate the channel equalization algorithms both on FPGA and on ASIC. The primary workhorse in achieving the high-speed channel equalization scheme is the optimized DFT algorithm. The DFT-15 was performed using

DFT-5 and DFT-3 by using the Prime Factor Algorithm (PFA). The channel equalization model was implemented on a Virtex Ultrascale FPGA, and it is running at a clock frequency of 166.67 MHz. Furthermore, the with 40 nm NanGate ASIC technology, the channel equalization module runs at 158 MHz, which is  $\frac{1}{10^{th}}$  of the PSSS symbol rate (1.67 GHz).

A technique for the high-speed transmission of a PSSS modulated signal was developed. The core idea for driving the operation of the PSSS transmitter to achieve 100 Gbps is that we operate the parallel PSSS encoders at lower symbol rate. And we need only a serializing unit, namely an Analog MUX, which clocks at the chip rate. In our above-experiments, the concept was proven on FPGA with a lower PSSS symbol clock of 25 MHz, and using 28 nm ASIC technology we could achieve PSSS symbol clock rate of 1.785 GHz. Fundamentally, the proposed parallel transmitter architecture can be also applied to different encoding schemes, and is also not only limited to wireless communication.

## Chapter 6

# Hardware-in-the-Loop experiments

Until now, there were no previous experiments involving the transmission of a PSSS modulated waveform in the THz frequency range. In this Chapter, we discuss the results of our Hardware-in-the-Loop (HIL) experiments performed by employing THz radios with a PSSS transceiver system.

In our HIL experiments, a PSSS modulated signal is transmitted using an RF-frontend operating at sub-millimeter-wave frequencies of 240 GHz/230 GHz. The PSSS transceiver operations are pre/post-processed offline in MATLAB/Simulink. In the pre-processing part, the PSSS modulated symbols/waveforms are generated and loaded onto an AWG and then transmitted using the 240 GHz wireless frontend. A Dynamic Signal Analyzer (DSA) or a Real-Time Oscilloscope (RTO) samples and stores the received signal. In the post-processing steps, the PSSS receiver performs synchronization, channel estimation, and demodulation.

We performed two HIL experiments using PSSS transmission systems with two different RF frontends. For the first time, we demonstrated a PSSS encoding/decoding scheme transmitting wireless data up-to 80 Gbps [42] on air with a distance of 1 m using a 240 GHz RF-frontend developed by the University of Wuppertal [65, 186]<sup>1</sup>.

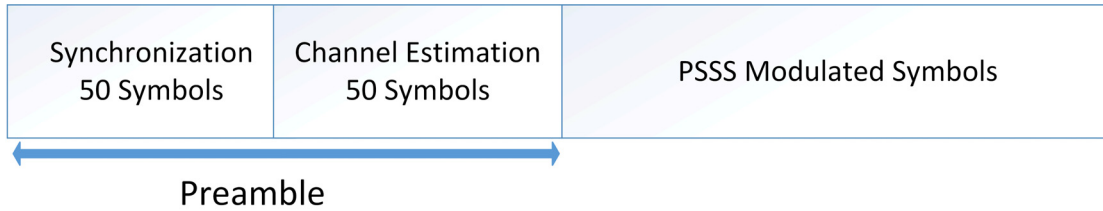
We performed the following HIL experiments:

- Experiment 1 (expt. 1): We achieved 80 Gbps by using the RF-frontend of the TU Wuppertal [65], and particulars are presented in Ref. [42].
- Experiment 2 (expt. 2): We achieved 20 Gbps by using the RF-frontend of the TU Stuttgart [66], and specifics are published in Ref. [215].

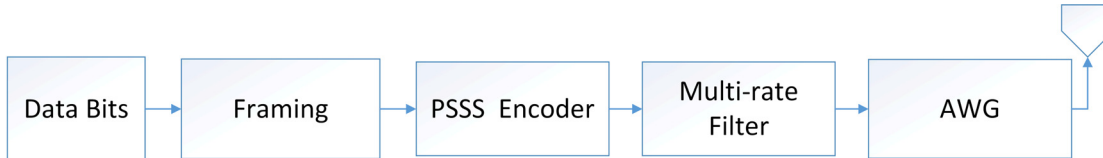
In the following section, we discuss the generic model of the PSSS transmitter/receiver developed in Matlab/Simulink, brief details of the two RF-frontends, methods of synchronization, HIL measurement setup and finally, we explain the results.

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<sup>1</sup>This was part of the Real100G.RF project.



**Figure 6.1:** Frame structure used for the HIL experiments for the measurements of expt. 1 and expt. 2.



**Figure 6.2:** PSSS transmitter. Post-processing performed in Matlab/Simulink.

## 6.1 HIL model for a PSSS-15 Transmitter

Our mixed-signal PSSS system is explained in Chap. 4. All the individual blocks in the box “PSSS transmitter” in Fig. 4.1 are designed in Matlab/Simulink. A general PHY packet structure is given in Sec. 3.4.1. Figure 6.1 shows the frame structure used in the HIL experiments. We take 100 symbols for synchronization and channel estimation. By averaging channel estimates over 50 symbols, the noise is reduced. The preamble consists of a repeated pattern of “m-sequences”. In Experiment 1, 3000 PSSS symbols are modulated with PAM-16 carrying 180 000 bits ( $3000 \cdot 15 \cdot 4$ ). Experiment 2 employs 4920 PSSS symbols modulated with BPSK which carry 73 800 bits ( $4920 \cdot 15 \cdot 1$ ).

The generation of PSSS symbols to be transmitted by the RF-frontend is shown in Fig. 6.2. The data bits are converted to the targeted spectral efficiency by bit-loading and then passed on to the PSSS encoder (Sec. 3.1.2 and Sec. 3.3.1). The output of the encoder is routed through the “Multi-Rate Filter”, which adjusts the chip-rate to an appropriate sampling rate of the AWG. In expt. 1, the PSSS signal is up-sampled by a factor of two using a multi-rate filter to match the AWG sampling rate of 40 GS/s. In expt. 2, a PSSS encoded signal was up-sampled by a factor of three using a multi-rate filter to match the AWG sampling rate of 60 GS/s.

We used two different measurement instruments in the HIL setup. For expt. 1, we used an AWG from Tektronix. For expt. 2, we used an AWG from Keysight. The AWG module from these two devices has different values for the storage of the sampling points and the sampling rates on which they can be set. Hence, the two measurement experiments have different payloads and sampling rates.

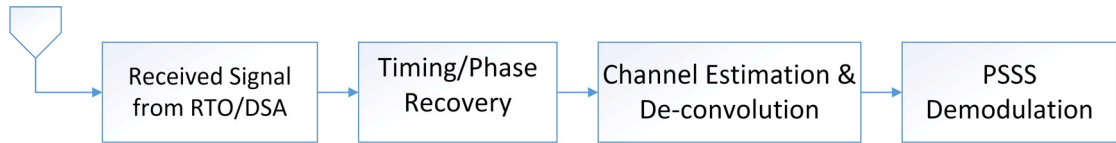


Figure 6.3: PSSS receiver post-processing performed in Matlab/Simulink.

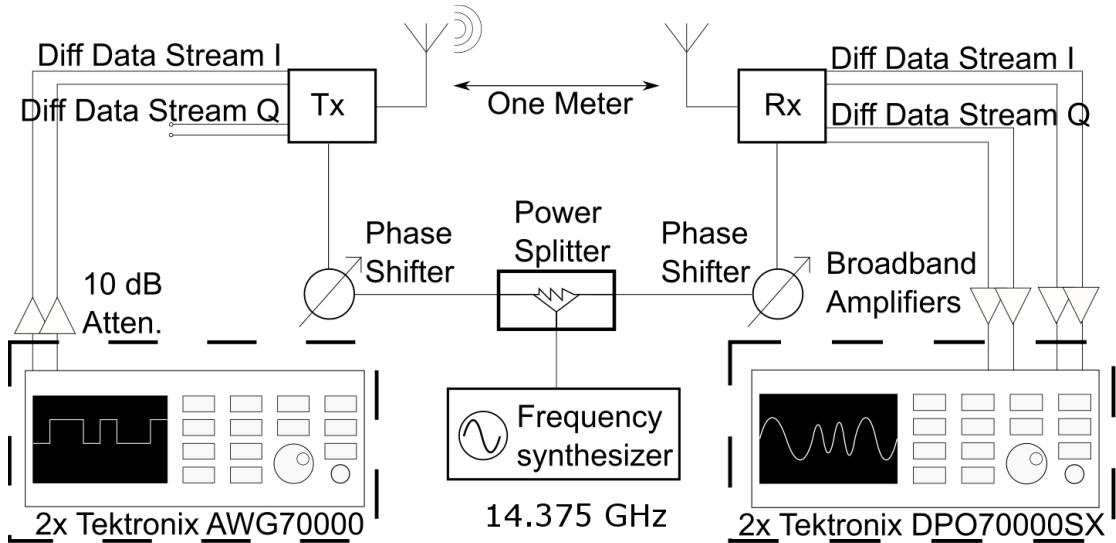


Figure 6.4: Measurement setup of the 230 GHz communication link.

## 6.2 HIL model for a PSSS-15 Receiver

As shown in Fig. 6.3, the received down-converted signal from the RF-frontend is digitally sampled by a Dynamic Signal Analyzer (DSA). Then the PSSS symbol timing and the carrier phase/frequency are recovered by post-processing of the samples in Matlab/Simulink, using the algorithms explained in Sec. 6.4.1. After the synchronization, the baseband processing chain is followed up by channel estimation and channel deconvolution. Finally, the transmitted bits are recovered, and the BER is evaluated. In expt. 1, the RTO operates at a sampling rate of 100 GS/s and in the expt. 2, the DSA runs at 80 GS/s. For expt. 1, we used an RTO from Tektronix. For expt. 2, we used a DSA from Keysight. This leads to various sampling rates of oscilloscopes for the expt. 1/expt. 2.

## 6.3 Demonstrator Setup

In this Section, we briefly describe the demonstrator setup and the RF-frontend used in expt. 1 and expt. 2.

### 6.3.1 Measurement setup for Experiment 1

The transceiver RF-frontend modules are described in Ref. [65]. A 1-meter link at 230 GHz was set up using an RF frontend module, which consists of a transmitter (Tx) and a receiver (Rx) [65, 186] as depicted in Fig. 6.4. These modules are based on a



chip-set produced in a SiGe 0.13  $\mu\text{m}$  HBT technology [216]. The LO of 14.375 GHz is used as illustrated in Fig. 6.4. Both modules are provided with a 230 GHz carrier signal generated by a  $16\times$  multiplier chain, i.e,  $16 \times 14.375 = 230$  GHz.

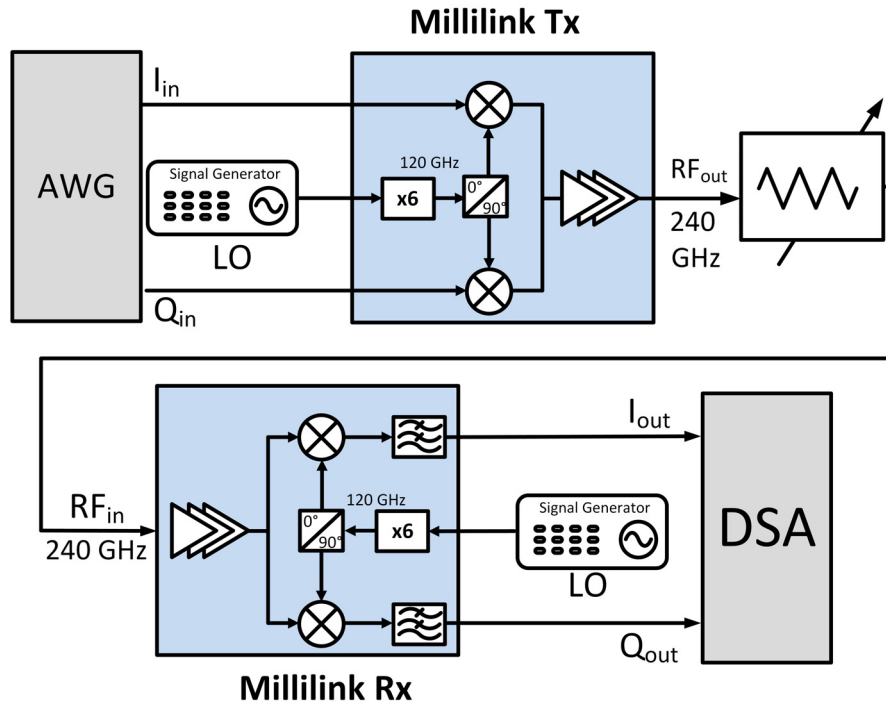
The frequency synthesizer is capable of generating signals up to 20 GHz. The up-/down conversion mixers at the Tx/Rx are controlled by the output signal of the multiplier chain. Both mixers are assembled with baseband buffers to provide a  $50\ \Omega$  connection to interface the high-speed baseband signals (I/Q signals as in Fig. 6.4). Each of the modules is mounted with on-chip linearly polarized ring antennas that radiate through the silicon substrate into a 9 mm silicon lens (s. Fig. 1.5). The modules achieve a directivity of 25.5 dBi at 230 GHz with the help of a focusing lens. In this experiment, the RF-frontend has a high transmit linearity and helps to achieve higher spectral efficiency.

The experimental system, as depicted in Fig. 6.4, was employed to achieve high-speed communication with PSSS modulation. At the transmitter, a differentially operated Tektronix AWG70000s (40 GS/s sampling rate each) generates the baseband signal that goes into the I-channel of the transmitter, and the Q-channel of the transmitter is grounded. To ensure the operation of the transmitter in a linear region, 10 dB attenuators are placed at the output of AWGs. The received signal from the RF-frontend receiver chip-set is digitized by two differentially driven Tektronix DPO70000SX RTO. A set of broadband amplifiers are used to boost the received signal before it is fed to the RTO. This ensures that the received signal is above the noise floor of the scope. A single frequency synthesizer tuned at 14.375 GHz is used to generate the LO signal. The power splitters and the phase shifters are there to ensure a maximum frequency alignment. The real-time Tektronix oscilloscope is running at a maximum sampling rate of 100 GS/s and acquires the received baseband signal.

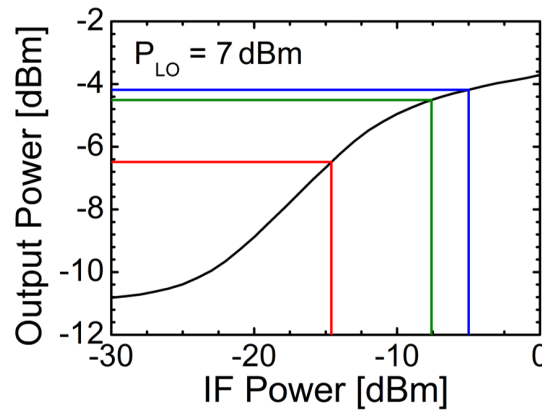
### 6.3.2 Measurement setup for Experiment 2

The transmitter and receiver modules used in the experiment are described in Refs. [64, 66]. The receiver chip-set has a subharmonic I/Q mixer with an RF bandwidth of 40 GHz. The modules can receive an RF signal between 200 GHz to 280 GHz. The LO signal required is 120 GHz. It was generated by using a chain of frequency ( $\times 6$ ) multipliers, as illustrated in Fig. 6.5. The frequency multipliers receive an input signal at 20 GHz generated by a signal generator. The 3 dB RF bandwidth is about 20 GHz, and the I/Q amplitude imbalance is about 1.9 dB. The LNA consists of a three-stage cascade amplifier in both transmitter and receiver. The receiver chips saturate at nearly -30 dBm. A variable WR-3 waveguide attenuator (s. Fig. 6.5, 220 GHz to 325 GHz) was used to ensure power levels below -35 dBm for a proper functioning of the receiver chipset.

The LO leakage leads to many problems when it comes to coherent transmission with an exact LO used at the transmitter/receiver, e.g., a severe LO leakage may lead to a saturation of the transmitter/receiver amplifiers, and it will also cause a DC offset at the receiver. Thus, one needs to have excellent LO-to-RF isolation, achieved by using balanced mixers at transmitter/receiver MMIC [66].



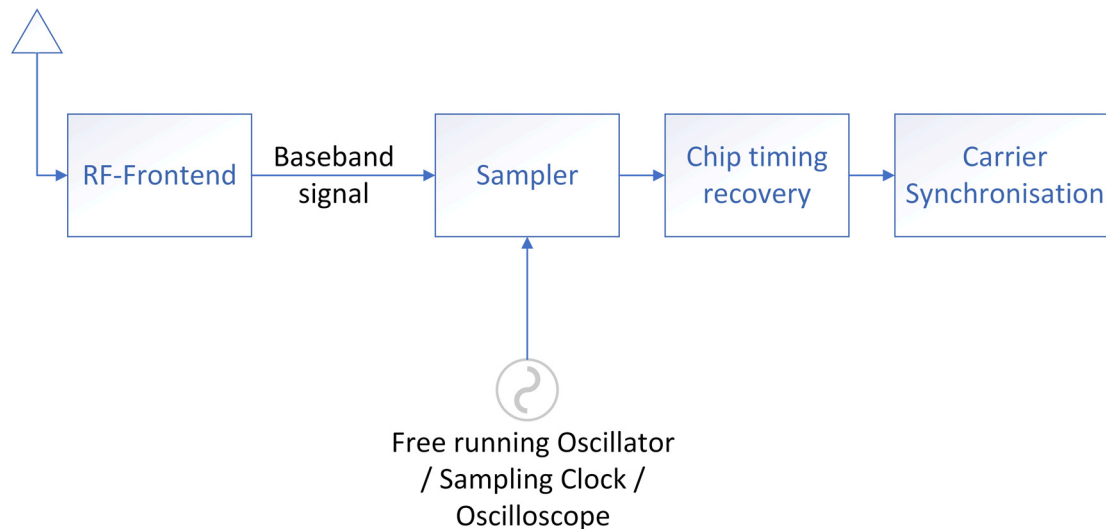
**Figure 6.5:** Measurement setup of the 240 GHz communication link.



**Figure 6.6:** Experimentally measured RF output power versus IF input power of the transmitter module operating at 240 GHz. The figure is taken from Ref. [217].

At the transmitter, the amplifier saturates at a maximal output power of -3.6 dBm. The noise floor is around -11 dBm at a LO input power of 7 dBm, and the low-level noise floor is achieved by having the best LO-to-RF isolation [217]. The measured transmitter linearity is shown in Fig. 6.6. We can observe that the usable linear range of the transmit power amplifier is about 7 dB. The PSSS modulation is robust against amplitude clipping, as described in Sec. 3.3.5. With such a low linear gain, we are able to transmit PSSS with BPSK modulation. But the linear gain is not sufficient to transmit PSSS with PAM-16 modulation.

The HIL experiments are performed in a back-to-back setup, as shown in Fig. 6.4. The baseband signal to the RF-transmitter module is generated using a Keysight M8195A



**Figure 6.7:** Synchronization in the digital domain.

AWG operating at 60 GS/s. After I-Q down-conversion, the I/Q signal from the receiver chip-set is digitized and stored by a Keysight DSO-X 93204A oscilloscope operating at a sampling rate of 80 GS/s.

## 6.4 Synchronization in HIL experiments

As discussed in the Sec. 3.5, we have two models for synchronization. The one for the “PSSS system Model” utilized in the PSSS transceiver system (s. Chap. 4) and another model for the HIL experiments. In this section, we describe the synchronization models used in HIL experiments.

We have performed a carrier frequency/phase and a chip timing recovery in our HIL experiments offline by using MATLAB/Simulink. The overall synchronization architecture resembles the “Digital carrier/timing recovery” (s. Fig. 3.22). Figure 6.7 shows the main functional blocks required to achieve synchronization. The received signal is down-converted to a baseband signal by an RF-frontend. The baseband signal is sampled with an oscilloscope at an extremely high sampling rate, as shown in Fig. 6.7. This above over-sampled signal is fed to a “Chip timing recovery” block to recover the chip timing, and a “Carrier synchronization” block to recover the carrier frequency/phase. After these steps, the transmitted data is recovered by demodulation at the receiver.

In our HIL measurement experiment, we have used a chip-rate of 20 Gcps, and we sample this signal with an oscilloscope at a sampling rate of 80 GS/s or 100 GS/s. So, this leads to an over-sampling factor ( $R$ ) of 4 to 5. The synchronization algorithms developed in Matlab use the-above over-sampling factor to recover the carrier frequency, the carrier timing or the chip timing.

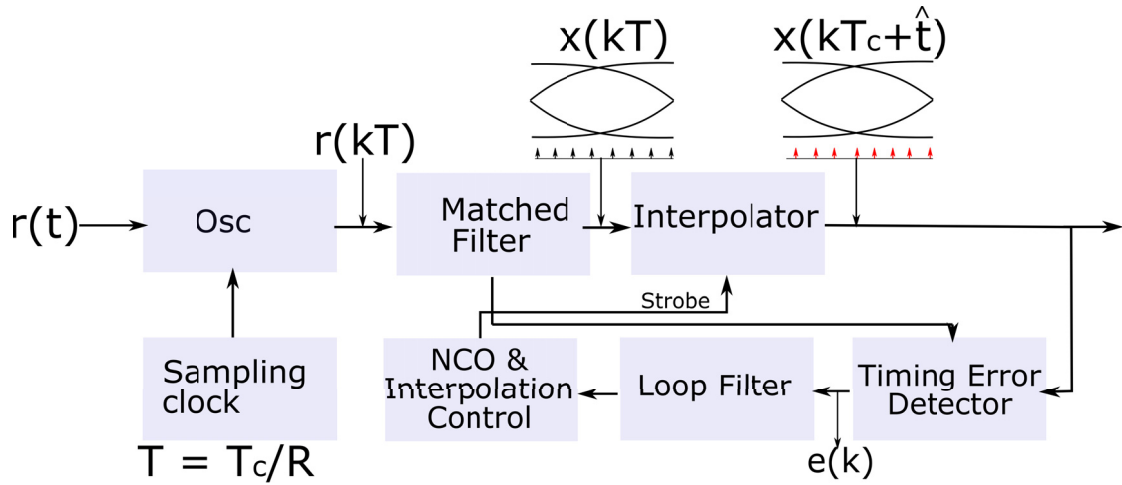


Figure 6.8: Timing synchronization.

### 6.4.1 Chip timing synchronization

The architecture of the all-digital timing retrieval procedure is shown in Fig. 6.8. Digital timing recovery algorithms are defined in Refs. [155, 157, 218]. In essence, the operation of the above-algorithm includes generating a timing error signal for the receiver. This error signal is then typically used to regulate a NCO that produces the sampling strobes. The acquired signal is generally over-sampled by an oscilloscope in real-time, as shown in Fig. 6.8. The oscilloscope sampling rate is  $1/T$  with an oversampling factor  $R$ , which is asynchronous to the chip rate of  $1/T_c$ . The time delay  $\tau$  is predicted from the  $x(kT)$  signal at the output of the matched filter. The output at the matched filter generates samples that are not aligned with the chip timing limits, as shown in Fig. 6.8. The function of the symbol timing synchronization is to “shift” the samples to the required time instants. This process is called interpolation. Since the timing synchronizer has to adapt to the unknown time delay, the interpolator must be adjustable. If the timing delay is correctly estimated, the interpolation produces output samples aligned with the symbol boundaries as illustrated in the eye-diagram at the output of the “interpolator” block in Fig. 6.8.

The timing synchronization is performed using a time-discrete PLL composed of three basic units: (i) a Timing Error Detector (TED), (ii) a loop filter, (iii) an interpolator, (iv) an interpolation control and an NCO as shown in Fig. 6.8.

The TED generates an error signal  $e(k)$  for each chip based on recent timing estimates  $x(kT_c + \hat{\tau})$  provided by the interpolator, and is using a matched filter input  $x(kT)$  as depicted in Fig. 6.8. For each chip time, the time discrete error signal is revised. An ideal interpolation calculates the correcting timing instants  $x(kT_c + \hat{\tau})$  using an instantaneously measured value  $\hat{\tau}$ .

### Gardner Timing error detector

The “Timing Error Detector” block in Fig. 6.8 employs the Gardner algorithm to determine the sampling instants at the receiver. The main concept of the Gardner algorithm is to compute the zero-crossings at the output of the interpolating filter (s. Fig. 6.8). The crucial point of the Gardner TED is that it does not require additional information except the prevailing samples to recover the timing information, i.e., it is a non-data-aided TED method. The algorithm proposed by Gardner uses 2 samples per chip, and one of the samples is used for chip time detection [157]. The error signal produced by the Gardner  $e(k)$  TED is given by Ref. [151, p. 393]:

$$e(k) = x((k - 1/2)T_c + \hat{\tau})[x(k - 1)T_c + \hat{\tau} - (kT_c + \hat{\tau})]. \quad (6.1)$$

### Interpolator

In an asynchronous sampling, the sampling clock at the receiver is independent of the data clock used by the transmitter. As a result, the sample rate and the chip rate are incommensurate and the sample times never coincide exactly with the desired interpolant time. If the PLL is in a locked state, then the interpolants sampling instant is the same as the chip time  $T \sim T_c$ .

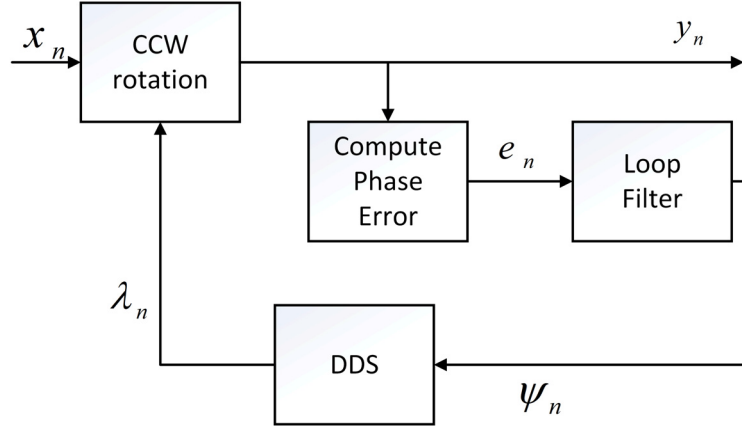
The ideal interpolation filter is the Infinite Impulse Response (IIR). Since the implementation of an IIR is difficult, the interpolator is realized by Finite impulse response (FIR) filters. FIR interpolating filters are a class of piecewise polynomial filters. A piecewise parabolic interpolator with a Farrow structure and a coefficient  $\alpha$  set to 1/2 as described in Refs. [151, 153] is applied to “move” the samples as shown in Fig. 6.8.

### Interpolation control and NCO

The role of the “Interpolation control and NCO” block depicted in Fig. 6.8 is to provide an interpolator with a base-point index and a fractional interval for each desired interpolant. The base-point index is usually not computed explicitly but rather identified by a signal called “strobe”. The NCO produces a “strobe” signal which is fed into the “Interpolator” block. The “Modulo-1 counter interpolation Control” method is used, and it is described in detail in Ref. [153, p. 475].

### Loop Filter

The loop filter is very important to the operation of the whole PLL. It removes unwanted components of the phase detection frequencies and acts as a low-pass filter. Its objective is to force the VCO to replicate and track the frequency and phase at the input when it is in lock [219]. The loop filter must have a nonzero DC gain to drive the steady-state phase error to zero in the presence of a phase offset and a large DC gain to drive the steady-state phase error to zero in the presence of frequency offset. A loop filter which satisfies the above criteria is called a proportional-plus-integrator (PI) loop filter. All



**Figure 6.9:** Carrier phase synchronization.

PLLs use a PI filter. The VCO is characterized by a single pole element in the Laplace domain. A loop filter with one pole leads to a second-order feedback control system in the form as described in Ref. [153, p. 724]. The PI filter function  $F$  is a second-order PLL:

$$F(s) = K_1 + \frac{K_2}{s}, \quad (6.2)$$

wherein  $K_1$ ,  $K_2$  are loop filter gain, and  $\theta$  is an interim term as defined in Eqn. (6.3)

$$K_1 = \frac{-4\zeta\theta}{(1+2\zeta\theta+\theta^2)K_p},$$

$$K_2 = \frac{-4\theta^2}{(1+2\zeta\theta+\theta^2)K_p}, \quad (6.3)$$

$$\theta = \frac{B_n T_c}{\zeta + \frac{1}{4\zeta}}.$$

The terms  $N$ ,  $\zeta$ ,  $B_n T_c$  and  $K_p$  represent the oversampling factor, the damping factor, the normalized loop bandwidth, and the detector-gain respectively.

### 6.4.2 Carrier frequency/phase synchronization

The digital carrier frequency/phase synchronization method is illustrated in Fig. 6.9. After the down-conversion of the received signal from RF to baseband, a phase compensation is realized by the “counterclockwise rotation (CCW) rotation” block. This block uses the correction  $\lambda_n$  provided by Direct Digital Synthesis (DDS) to compensate for the phase/frequency error. The carrier phase PLL is formed by a closed loop created by a phase error detector, a loop filter, and a DDS. The error signal generated by the “Compute Phase Error” block uses the de-rotated signal space projections and the data symbol estimates. The loop is locked when  $e_n = 0$ . Since the carrier phase is recovered completely in a digital domain, the PLL loop operates at 1 chip/sample. The PLL used is called a decision-directed loop [220]. The “carrier phase synchronization” block in Fig. 6.7 is running at the chip rate. The “carrier phase/frequency synchronization” is

performed after achieving the timing synchronization (i.e, chip-clock recovery). The all-digital timing synchronization method was discussed in the previous section.

The output of the carrier synchronization  $y_n$  is a frequency shifted version of the input signal  $x_n$  for the  $n^{th}$  sample:

$$y_n = x_n \cdot e^{i\lambda_n}. \quad (6.4)$$

To compensate for the frequency offset, we determine  $e_n$ , and from Ref. [153, p. 375] we get:

$$e_n = \text{sgn}(\text{Re}\{x_n\}) \times \text{Im}\{x_n\}. \quad (6.5)$$

The phase error passes through a biquadratic loop filter [221], which assures the system stability:

$$\psi_n = g_I e_n + \psi_{n-1}, \quad (6.6)$$

where  $\psi_n$  is the output of the loop filter at the sample  $n$  and  $g_I$  is the integrator gain defined as:

$$g_I = \frac{4(\theta^2/d)}{K_p K_0},$$

$$\theta = \frac{B_n}{\left(\zeta + \frac{1}{4\zeta}\right)}, \quad (6.7)$$

$$d = 1 + 2\zeta\theta + \theta^2.$$

Here  $B_n$  is the normalized loop bandwidth, and  $\zeta$  is the damping factor. The DDS gain  $K_0$  is equal to the number of samples per chip. The phase error detector gain  $K_p$  depends on the type of modulation. For the PAM-16 modulation,  $K_p$  is 2 [153, p. 738].

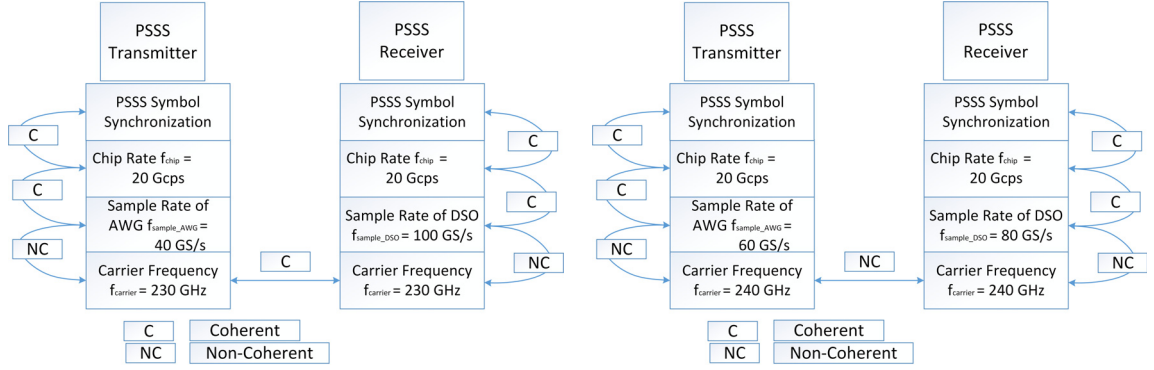
The output of the loop filter is then passed to the DDS. The DDS is another biquadratic loop filter. Its mathematical expression is based on the forward Euler integration rule as given in Eqn. (6.8), and  $g_P$  is the proportional gain:

$$\lambda_n = (g_P e_{n-1} + \psi_{n-1}) + \lambda_{n-1}, \quad (6.8)$$

$$g_P = \frac{4\zeta(\theta/d)}{K_p K_0}.$$

The normalized pull-in range  $(\Delta f)_{\text{pull-in}}$  is:

$$(\Delta f)_{\text{pull-in}} \approx \min\left(1.2\pi \times \sqrt{2} \times \zeta \times B_n\right). \quad (6.9)$$



(a) Limited coherent communication setup for expt. 1. (b) Non-coherent communication setup for expt. 2.

**Figure 6.10:** Synchronization setup for the HIL experiments for the expt. 1 and expt. 2.

The maximum frequency offset that can be compensated is  $1/T_{FL}$  and the phase lock delay  $T_{PL}$  as a functions of several samples, is given by

$$T_{FL} \approx 4 \times \frac{(\Delta f)_{pull-in}^2}{B_n^3}, \quad (6.10)$$

$$T_{PL} \approx \frac{1.3}{B_n}.$$

### 6.4.3 Synchronization layers of coherent/non-coherent systems

In the above previous two sub-sections, the theory of chip timing and chip frequency/phase recovery was outlined. We have implemented these algorithms in Matlab to perform synchronization in the HIL experiments.

In a fully coherent system, the clock signal used in the generation of the RF signal and the chip clock. The PSSS symbol clock has to be multiple factors of the same clock reference. The general synchronization levels which have to be achieved before PSSS modulated signal decoding can start are depicted in Fig. 6.10. We note that there are several synchronization levels, and they are carrier frequency synchronization, sampling frequency synchronization, and chip-rate recovery. Lastly, we perform the start of the PSSS symbol detection to identify the beginning of the payload data.

Figure 6.10a shows a limited coherent setup system, where the carrier frequency at 230 GHz required at both transmitter/receiver is generated by a single LO source at 14.375 GHz (s. Fig. 6.4). Figure 6.10b shows a non-coherent setup system, where the carrier frequency at 240 GHz required at both transmitter/receiver is generated by a two separate LOs at 20 GHz (s. Fig. 6.5).

For expt. 1, the synchronization relationship between the PSSS transmitter/receiver is depicted in Fig. 6.10a. There is a coherence relationship between the PSSS symbol synchronization, the chip rate (20 Gcps), and the sampling rate of the AWG (40 GS/s) at the transmitter. It should be noted that there exists a non-coherence relation between the AWG sampling rate (40 GS/s) and the carrier frequency at the transmit side. Since the same LO signal is fed to the transmit/received chip-set (s. Fig. 6.4), there is no



need to perform a carrier frequency recovery. At the PSSS receiver, there is a coherence relationship between the PSSS symbol synchronization, the chip rate (20 Gcps) and the sampling rate of the RTO (100 GS/s) but there is no coherence relationship between the RTO sampling rate (100 GS/s) and the carrier frequency (230 GHz). Since the transmitted PSSS modulated signal at 20 Gcps is sampled by a RTO at 100 GS/s, we have an oversampling ratio of 5 samples/chip.

The synchronization relationship between the PSSS transmitter/receiver for expt. 2 is illustrated in Fig. 6.10b. At the transmitter, we see the coherence connection between the PSSS symbol synchronization, the chip-rate (20 Gcps), and the sampling rate of AWG (60 GS/s). The non-coherence is due to the use of different references to generate the LO signals (s. Fig. 6.5). In addition, the baseband data generated at 60 GS/s uses an internal clock source of the Keysight AWG module. The clock for the RF-signal is generated using a different frequency synthesizer.

At the PSSS receiver (s. Fig. 6.10b), there is a coherence relationship between the PSSS symbol synchronization, the chip rate (20 Gcps) and the sampling rate of the DSA (80 GS/s). Nevertheless, we note that there is no coherence relationship between the DSA sampling rate (80 GS/s) and the carrier frequency (240 GHz). The sampling rate of the DSA is 80 GS/s. The PSSS modulated signal is transmitted with a Chip rate of 2 Gcps, resulting in an oversampling ratio of four samples/chip

We have an oversampling factor of 5 samples/chip for expt. 1 and 4 samples/chip for expt. 2. The above-described algorithms use this oversampling factor to recover the carrier frequency/phase and the chip timing by post-processing in Matlab/Simulink.

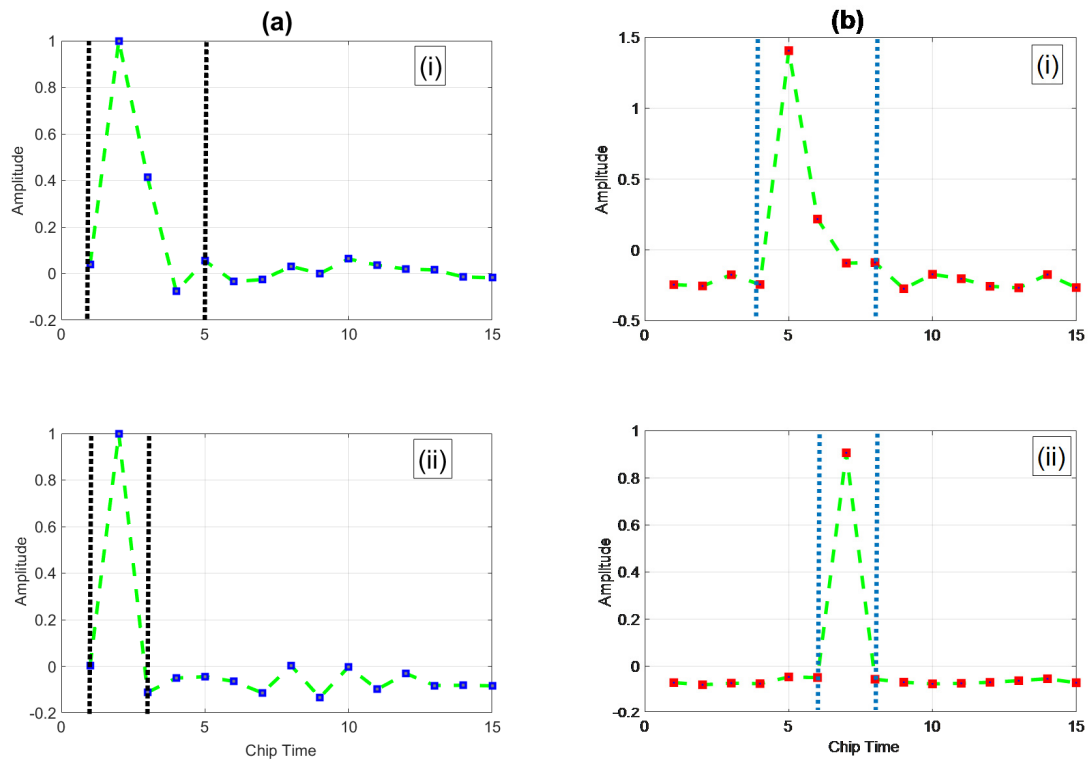
## 6.5 Performance results

In this Section, we discuss the measurement results of our HIL experiments. The essential results are the channel estimation/channel equalization. We compare the eye diagram in the cases of expt. 1/expt. 2 for a spectral efficiency 1 bit/sec/Hz at a chip-rate of 20 Gcps. The PSSS symbols are also reconstructed for 4 bit/s/Hz for expt. 1.

### 6.5.1 Channel estimation and equalization

The main theoretical concepts of channel estimation and channel equalization are introduced in Sec. 3.6.1. The core idea of the channel estimation method applied in our experiments is to use the Dirac-Delta like autocorrelation function of *m*-sequences (Sec. 3.2). This is utilized for channel estimation by sending repeated strings of *m*-sequences in the preamble.

Figure 6.11a shows the channel response evaluated using *m*-sequences before and after the channel deconvolution procedure for expt. 1 (s. Fig. 6.4). Figure 6.11a(i) shows the measured channel response in time-domain before deconvolution and Fig. 6.11a(ii) shows the channel response in time-domain after the deconvolution at 20 Gcps. In Fig. 6.11a(i), the channel response is spread over three chips, and we observe strong side lobes due to



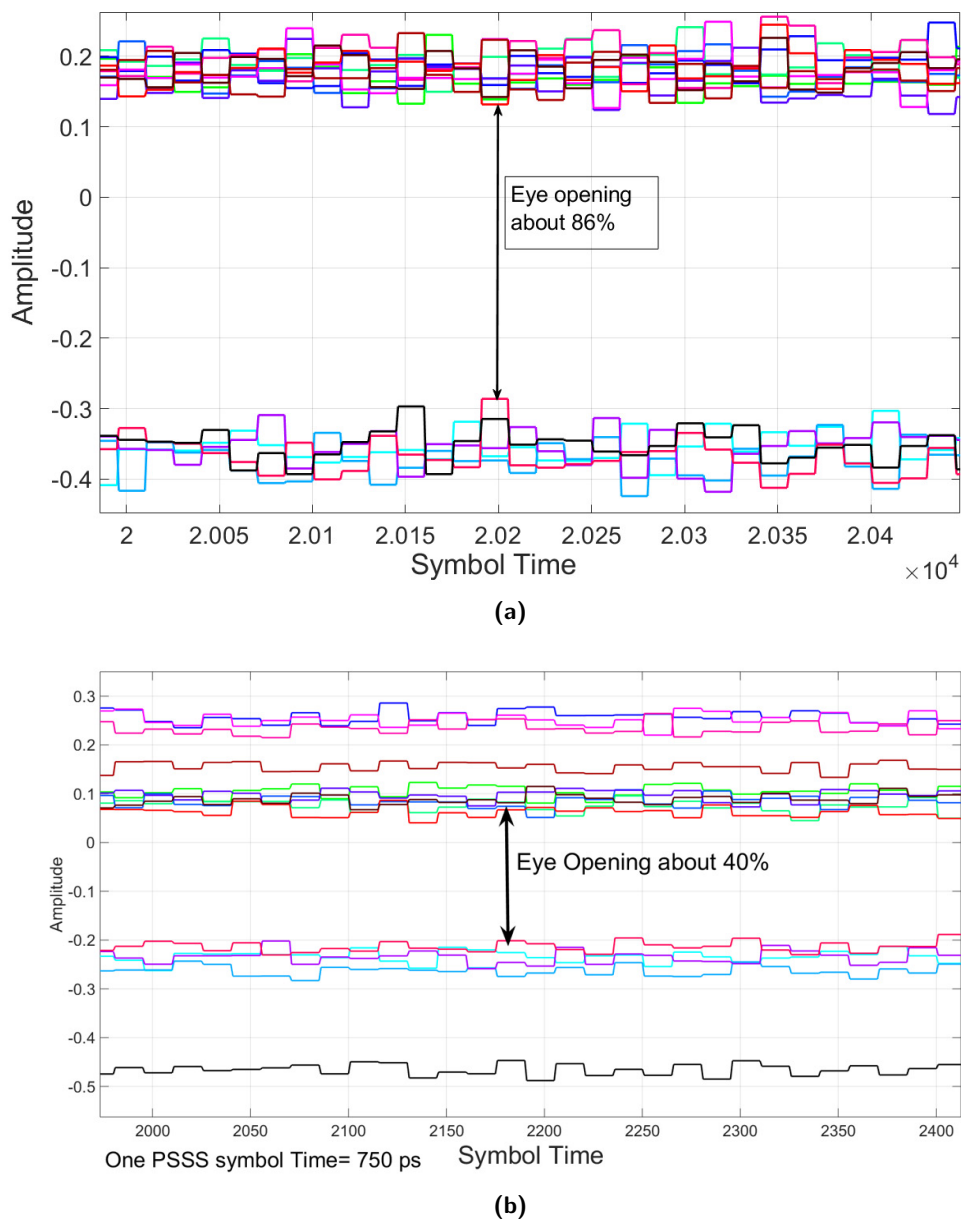
**(a)** Measured channel response before deconvolution for the 230 GHz transmission link as described in expt. 1. As indicated by the dotted black line window, the channel response is spread over three chips. (ii) shows the channel response after performing deconvolution. As indicated by the dotted black line window, the channel response is confined to one chip.

**(b)** Measured channel response before deconvolution for the 240 GHz transmission link as described in expt. 2. (i) as marked with the dotted blue line window, the channel response is spread over four chips. The channel response after performing deconvolution in (ii) is confined to one chip.

**Figure 6.11:** Measured channel response before and after deconvolution for the THz transmission link for the HIL experiments 1 and 2.

the impairments caused by the RF-frontends. For illustration, before the deconvolution (s. Fig. 6.11a(i)), the first side lobe at a chip time 3 has an amplitude of 0.4. After we perform channel deconvolution (s. Fig. 6.11a(ii)), the channel response is confined to one chip and has a Dirac-delta like auto-correlation function. As we can observe in Fig. 6.11a(ii), the side lobe amplitude at chip time 3 is less than zero. Consequently, all distortion caused by the “effective channel” could be compensated by deconvolution. Here, the “effective channel” consists of the transfer function of the RTO, the AWG, the signal transmitted over the air and the RF-frontend impairments of the Tx/Rx modules.

Figure 6.11b shows the channel response evaluated using *m-sequences* before and after the channel deconvolution procedure for expt. 2 (s. Fig. 6.5). Figure 6.11b(i) shows the measured channel response in time-domain before deconvolution and Fig. 6.11b(ii) illustrates the channel response in time-domain after deconvolution at 20 Gcps. As explained in the previous section, channel deconvolution corrects the impairments induced by the effective channel (s. Fig. 6.11b(ii)). We can conclude that channel deconvolution is the



**Figure 6.12:** Eye-diagram of a PSSS modulated signal measured using two RF-frontends. (a) Eye-diagram for a PSSS modulated signal transmitted at 20 Gcps with BPSK using a 230 GHz RF-frontend (expt. 1)[65, 186]. (b) Eye-diagram for a PSSS modulated signal transmitted at 20 Gcps with a BPSK using a 240 GHz RF-frontend (expt. 2)[64, 66].

critical technology to correct channel impairments very effectively. Thus, the channel equalization facilitates the use of higher spectral efficiencies.

### 6.5.2 PSSS modulated data with BPSK

Typically, for a spectral efficiency of 1 bit/s/Hz, we have only two levels in an eye diagram, but there are multi-levels as depicted in Fig. 6.12b. Each of the output levels in Fig. 6.12b is the result of fifteen parallel IDCs (s. Fig. 4.3 in the Chap. 4), and they stay constant over the symbol time of 750 ps.

Ideally, each output level representing the integration result of a single IDC<sup>2</sup> should be mapped onto +1 or -1 values, but this is not the case in Fig. 6.12b. The high non-linearity of the power amplifier (operating range  $\approx 7$  dB, Fig. 6.6) is the leading cause, which clips of the multi-level PSSS signal and results in an eye-opening of 40% (s. Fig. 6.12b). We cannot explain why one code (black-code in Fig. 6.12b) behaves differently from all the other codes. But in expt. 1 all codes behave as expected.

A high SNR can be achieved by driving the power amplifier close its saturation, but this causes a clipping of the PSSS modulated waveform, which in turn decreases the eye-opening. Thus, there is a trade-off between the transmit power amplifier drive and the percentage of the eye-opening. In case of the used RF-frontend in the expt. 2 [66], a further improvement of the parameters was not feasible due to the high non-linearity of the amplifier function. The results of expt. 2 are published in Ref. [215].

In case of expt. 1 (s. Fig. 6.4), the 3-dB RF bandwidth of the transmitter module is 26 GHz (230–250 GHz). At 230 GHz RF frequency, the measured linear gain of the transmitter module is 16 dB [65]. As we can observe in Fig. 6.12a, the eye-opening is 86% due to the high linear transmit gain of the power amplifier. Thus, we have an RF-frontend transmitter, which has a higher dynamic operating range to achieve a high energy per bit to noise power spectral density ratio ( $E_b/N_0$ ), which in turn allows us to reach the targeted 4 bit/s/Hz spectral efficiency. The results of expt. 1 are published in Ref. [42].

### 6.5.3 PSSS modulated data with PAM-16

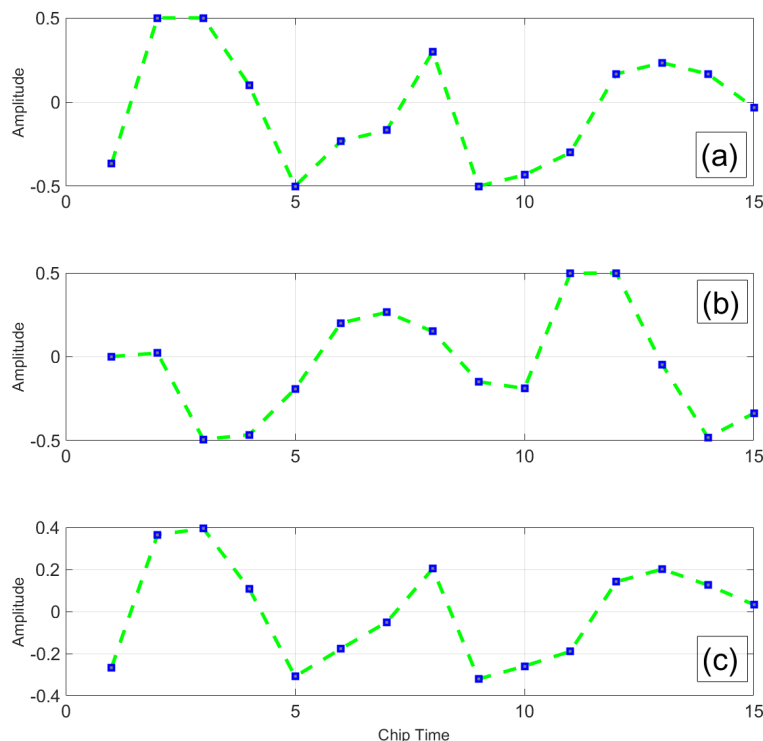
The number of discrete levels that have to be distinguished at the output of the parallel ADCs (Sec. 4.2: As in Fig. 4.3) increases with higher spectral efficiency. E.g., to achieve 1 bit/s/Hz, one needs to detect two levels, and it means that the ADC needs to have a bit resolution of 2 bits. The sampling rate of the ADC should be the same as the PSSS symbol rate of 1.67 GHz. Similarly, to realize 4 bit/s/Hz, the ADC should have a resolution of 4-bit<sup>3</sup> with a sampling rate of 1.67 GHz. For PSSS transmission at 20 Gcps with PAM-16, the recorded BER is  $2.072 \times 10^{-3}$  as described in Ref. [42].

As outlined in the Chap. 3 (particularly in Sec. 3.5.4), the PSSS modulation uses only the I-channel of the transmitter. This can also be observed in the experimental setups (s. Fig. 6.4 and Fig. 6.5). A higher order PAM-modulation can be combined with PSSS encoding to achieve higher spectral efficiency, e.g., PSSS with PAM-2 results in a bit loading of 2 bits and PSSS with PAM-16 leads to a bit loading of 4 bits [222, 223].

Figure 6.13 shows a PSSS modulated signal with a spectral efficiency of 4 bit/s/Hz (or with a PAM-16 overlay of data bits) at 20 Gcps to achieve 80 Gbps. Figure 6.13(a), depicts the transmitted PAM-16 symbols, Fig. 6.13(b) illustrates the received symbols before channel deconvolution at the receiver and Fig. 6.13(c) shows the received symbol after channel deconvolution. By comparing Fig. 6.13(a) and Fig. 6.13(c), it is evident that

<sup>2</sup>There are 15-parallel IDCs operating simultaneously as described in receiver baseband architecture. It is described in Sec. 4.2.2.

<sup>3</sup>The number of discrete levels that need to be detected is 16.



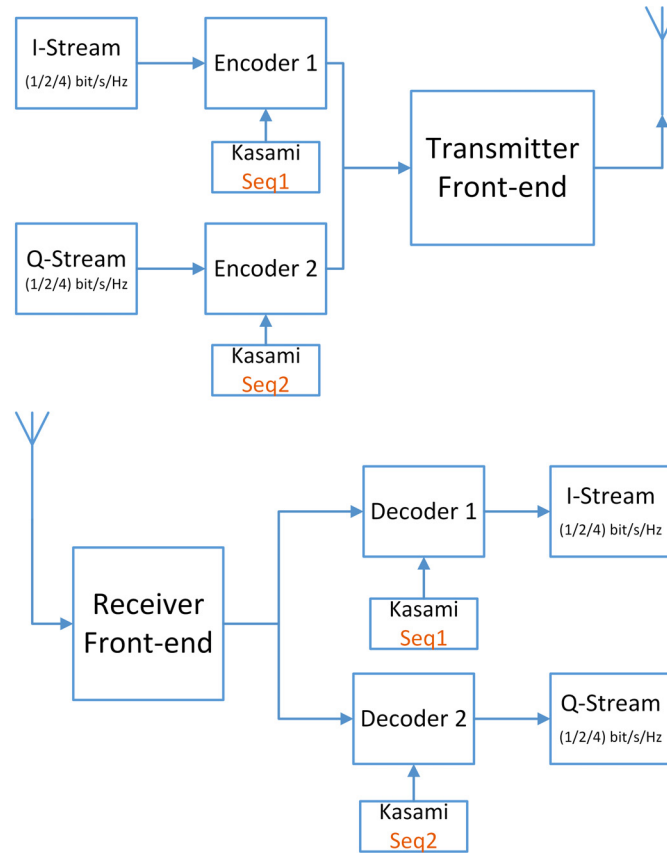
**Figure 6.13:** PSSS transmission at a chip-rate of 20 Gcps with PAM-16 to achieve 80 Gbps.

we can recover the transmitted PAM-16 symbols. This plot also indicates the significant impact of channel equalization performed by using deconvolution. The LO leakage at the receiver limits the IF bandwidth to 14.375 GHz. Thus, we were not able to target a higher chip rate above 20 Gcps.

As described in Ref. [51], the maximum data rate achieved is 100 Gbps using the same RF-frontend as in expt. 1 with 16-QAM modulation. It has to be noted that the article does not discuss other baseband operations like synchronization, channel estimation, and equalization. But in Ref. [51], both I/Q channels of the transmitter were used. With the usage of only the I-channel at the PSSS transmitter (s. Fig. 6.4), we have demonstrated 80 Gbps data rate. If we apply the concept of spreading on I/Q channels, we could be able to double the data rates. Thus, we have shown that the PSSS modulation technique is a worthy competing baseband technology to achieve 100 Gbps in the Terahertz band.

## 6.6 Kasami codes transmission on I/Q channels

In the past two measurement experiments (expt. 1 and expt. 2), the PSSS transmitter uses only the I-channel of the transmit RF-frontend to send the modulated data and the Q-channel is not used (s. Fig. 6.4 and Fig. 6.5). We have investigated the techniques to use the Q-channel of the transmit RF-frontend to double the data rate. For the first time,



**Figure 6.14:** Orthogonal PAM overlay modulation using a different set of Kasami base-codes on I and Q channel.

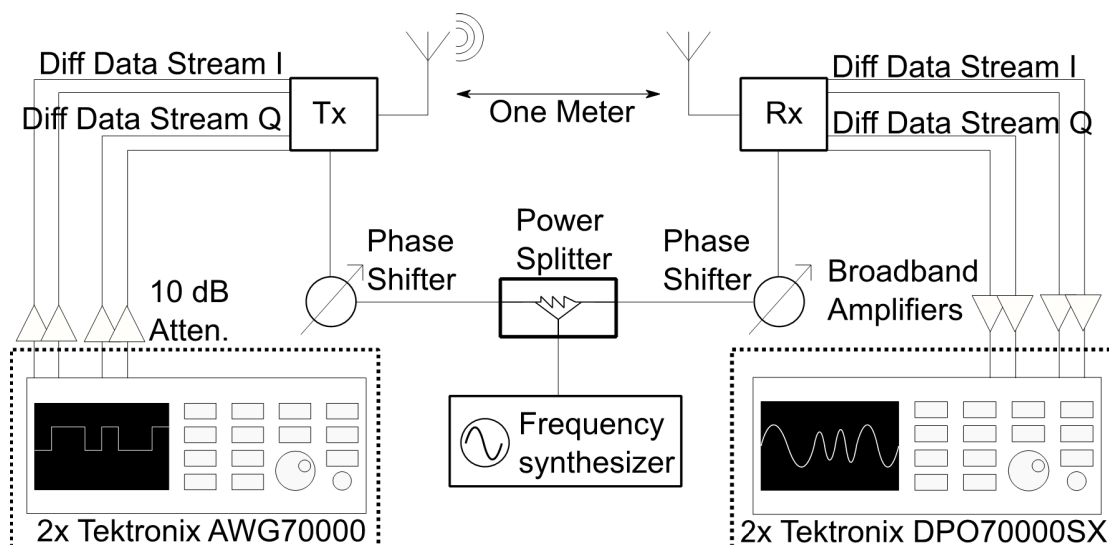
we have adopted the idea of parallel spread spectrum transmission to transmit data on both I/Q channels by performing encoding/decoding using Kasami codes. As explained in Sec. 3.2, for a Kasami code length of 15, there are 4 different unique sequences available, possessing acceptable auto-correlation and good cross-correlation properties (s. Fig. 3.6 and Fig. 3.7). One of the attractive features of Kasami codes is that out of these 4 sequences, one of them is the m-sequence. Thus, this m-sequence<sup>4</sup> is the only sequence in Kasami family that possesses good autocorrelation<sup>5</sup> and cross-correlation<sup>6</sup> property.

Figure 6.14 shows the general concept how to encode/and decode using Kasami codes. I and Q domains are used as two independent channels, wherein the I-channel operates with a cyclically shifted bi-polar encoding matrix generated by using “Seq 1” (s. Eqn. (3.9), *m-sequence* of length 15). The Q-channel operates with a cyclically shifted bipolar encoding matrix generated by using “Seq 2” (s. Eqn. (3.9)). Before performing the encoding, each channel can be overlaid with a PAM modulation of 1/2/3/4 bit/s/Hz spectral efficiency. At the receiver, a uni-polar decoding matrix is generated by using “Seq 1” for I-channel. For the Q-channel, the uni-polar decoding matrix is generated by

<sup>4</sup>One of the code belonging to Kasami family code sequences.

<sup>5</sup>M-sequence are known to possess good autocorrelation property.

<sup>6</sup>The codes belonging to Kasami family are known to possess good cross-correlation properties.



**Figure 6.15:** Transmission experiments with a 230 GHz link by using Kasami codes. The RF-frontend is described in Ref. [65, 186].

using “Seq 2”. From the above matrices, the two different independent transmitted data streams are reconstructed at the receiver.

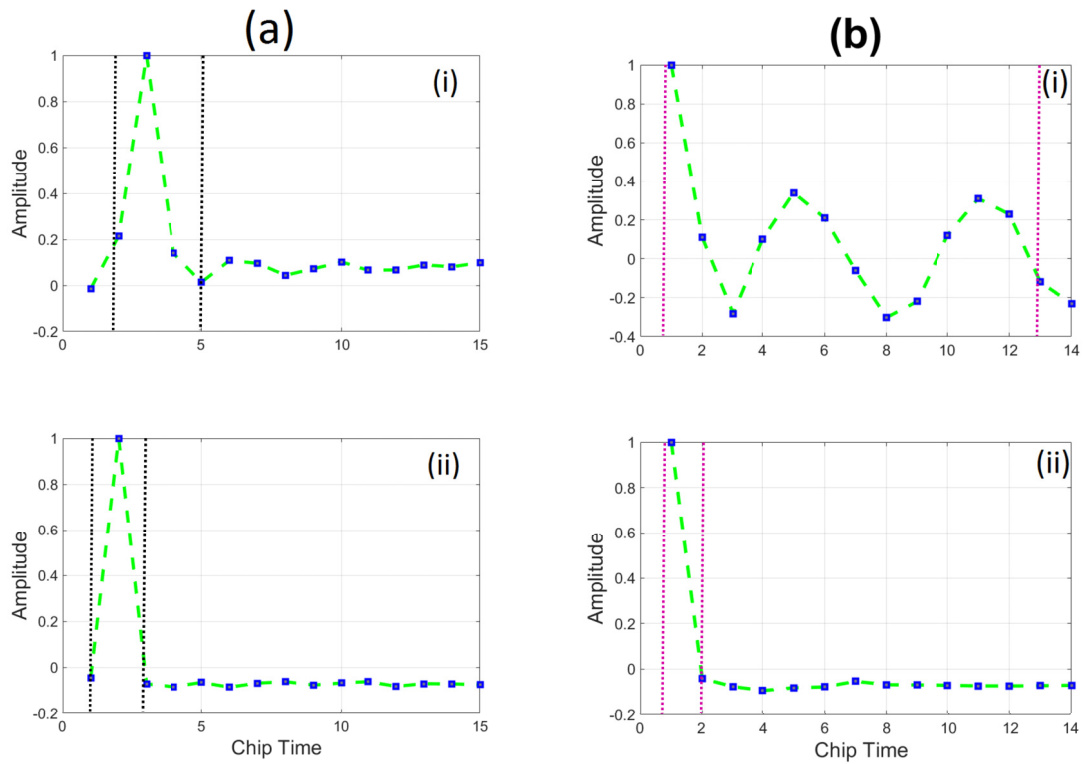
### 6.6.1 Measurement setup of the 230 GHz communication link with Kasami codes

The RF-frontend is described in the Sec. 6.3.1. The only difference in this setup is that the Q-channel at the transmit RF module is not grounded as in Fig. 6.15 when compared with Fig. 6.4, wherein the Q-channel is left unconnected. The AWG generates independent data streams on I/Q channels using “Seq 1”/“Seq 2” at a chip rate of 10 Gcps<sup>7</sup> with a spectral efficiency of 4 bit/s/Hz (i.e., PAM-16 overlay modulation), respectively. The sampling rate of the AWG is set to 40 GS/s. At the receiver, the RTO samples the incoming data from the receiver RF-frontend module at a rate of 100 GS/s, and it is stored in the memory. The synchronization, channel estimation, and recovery of the transmitted data symbols are performed by post-processing of the data in Matlab/Simulink. The synchronization is implemented similarly as described in Sec. 6.4.

### 6.6.2 Channel estimation with Kasami codes

In the transmitted frame of the I-channel, the preamble consists of a repeated vector of “Seq 1”, and the Q-channel preamble consists of a repeated vector of “Seq 2”. The primary purpose of using two different sequences on the I-Q channel is to avoid cross-channel leakage at the receiver after down-conversion, i.e., a part of the energy is leaked from I to Q and vice versa. This is the point where cross-correlation plays a vital role as Kasami codes have an almost ideal cross-correlation value of about 4.8 dB (Sec. 3.2 and in Fig. 3.7), compared to the absolute perfect cross-correlation value of 0 dB. This helps

<sup>7</sup>The limitation comes from the LO leakage and I-Q cross leakage at the receiver. More on this later.



(a) Measured channel response before deconvolution for the 230 GHz transmission link as described in the setup in Fig. 6.15 and the chip-rate is 10 Gcps. The I-channel uses “Seq 1” which has ideal auto-correlation properties. (i) as indicated by the dotted black line window, the channel response is spread over three chips. (ii) shows the channel response after performing channel deconvolution. As indicated by a dotted black line window, the channel response is confined to one chip.

(b) Measured channel response before deconvolution for the 230 GHz transmission link as described in the setup in Fig. 6.15 and the chip-rate is 10 Gcps. The Q-channel uses “Seq 2”. This sequence does not possess ideal autocorrelation properties like a *m*-sequence. (i) The dotted black line window indicates that the channel response is spread over 13 chips. (ii) shows the channel response after performing deconvolution. As indicated by the dotted pink line window, the channel response is confined to one chip.

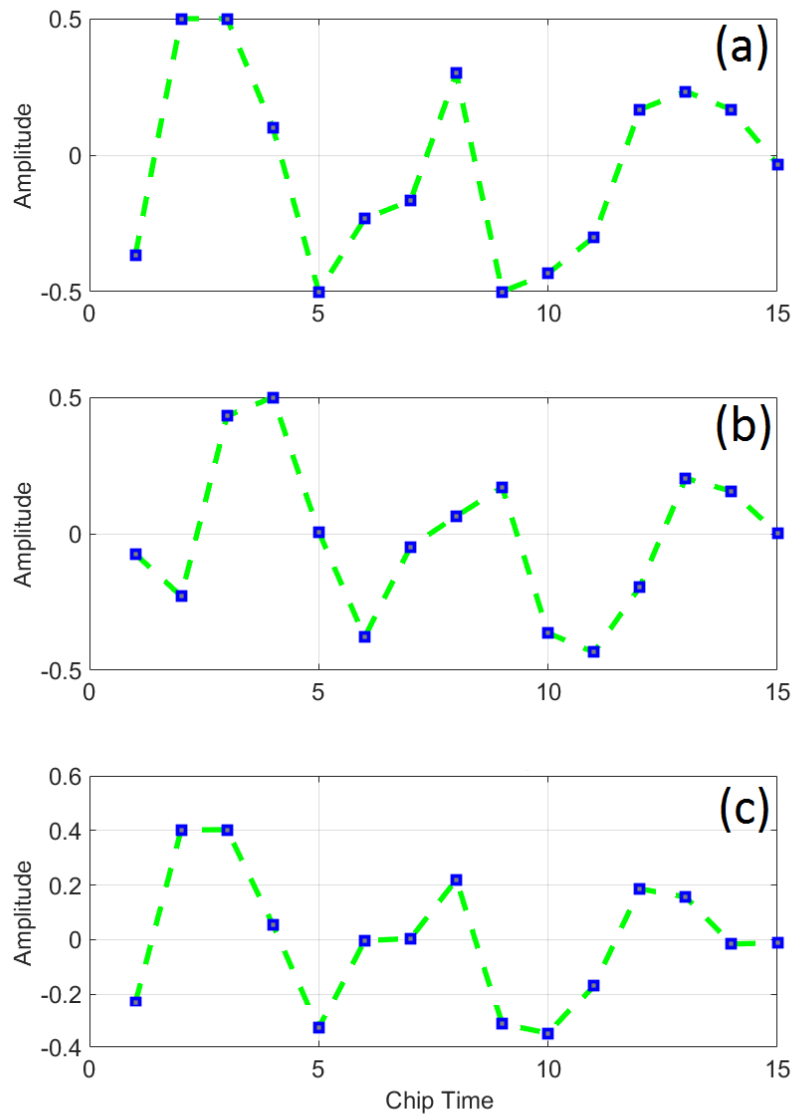
**Figure 6.16:** Measured channel response before and after deconvolution for the 230 GHz transmission link, setup as described in Fig. 6.15.

in the separation of I-Q channel as they are separated in the code-domain.

Since the I-channel uses a “*m*-sequence”, its channel response is spread only over 3 chips as in Fig. 6.16a(i), and this is also corrected by channel deconvolution as depicted in Fig. 6.16a(ii).

There is a trade-off between having excellent cross-correlation properties among the sequences “Seq 1”/“Seq 2” and having a non-ideal auto-correlation property of “Seq 2”. This can be observed in Fig. 6.16b (i), where the side-lobes of the channel estimation of Q-channel are spread over 13 chips. However, as it can be seen in Fig. 6.16b (ii), due to the channel deconvolution scheme, we observe no side lobes. The error caused by non-ideal autocorrelation is “deterministic” and thus can be corrected using deconvolution.



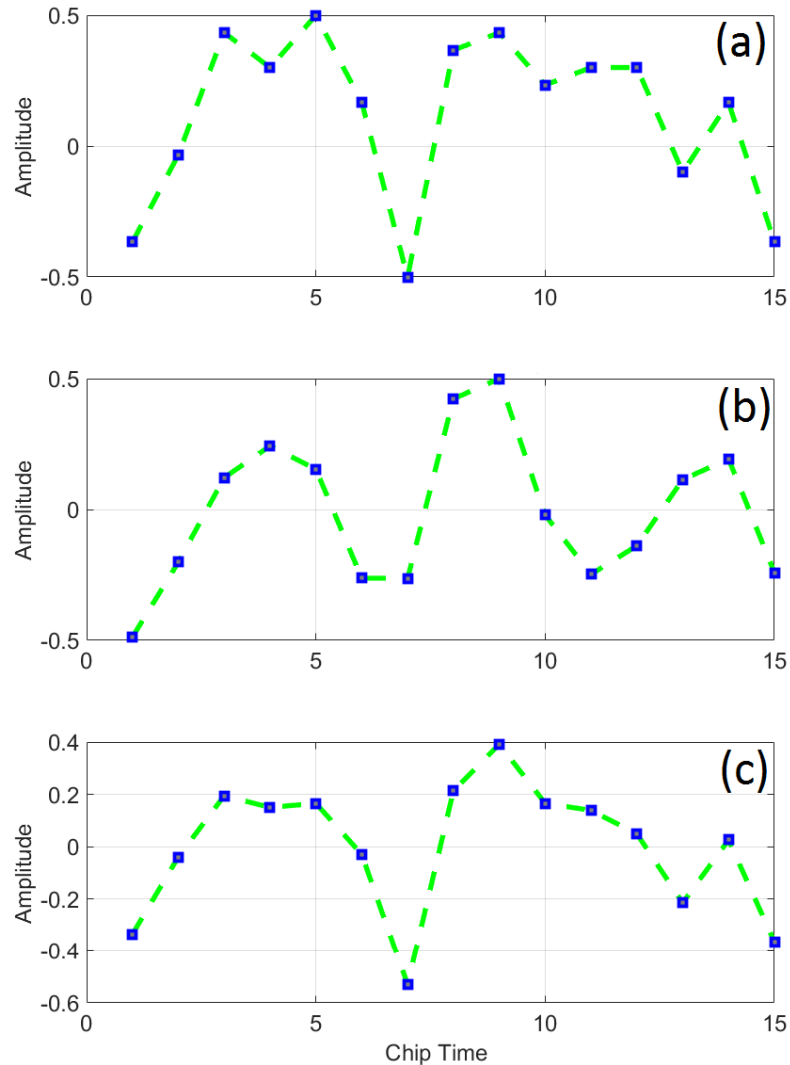


**Figure 6.17:** Independent I-channel of the PSSS transmission at a chip-rate of 10 Gcps with PAM-16 to achieve 40 Gbps.

### 6.6.3 Kasami codes with PAM-16

A PSSS modulated signal at 10 Gcps with PAM-16 was independently transmitted on the I-Q channel resulting in a cumulative data rate of 80 Gbps.

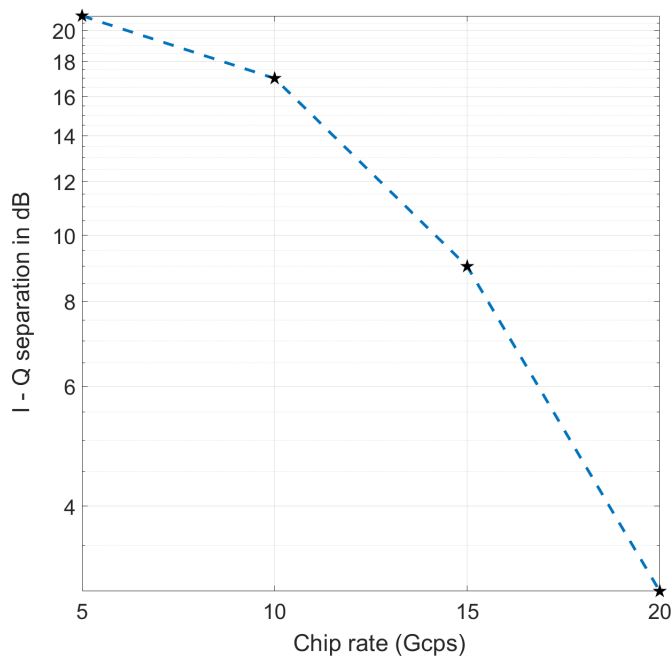
Figure 6.17(a), depicts the transmitted PAM-16 symbols on the I-channel of the transmitter at 10 Gcps, Fig. 6.17(b) shows the received symbols before channel deconvolution at the receiver and Fig. 6.17(c) shows the received symbol after channel deconvolution. By comparing Fig. 6.17(a) and Fig. 6.17(c), it is clear that we can recover the transmitted PAM-16 symbols. This plot also indicates the massive impact of channel equalization performed by using deconvolution.



**Figure 6.18:** Independent Q-channel - PSSS transmission at a chip-rate of 10 Gcps PAM-16 to achieve 40 Gbps.

Figure 6.18(a), depicts the transmitted PAM-16 symbols on the Q-channel of the transmitter at 10 Gcps, Fig. 6.18(b) depicts the received symbols before channel deconvolution at the receiver, and Fig. 6.18(c) shows the received symbol after channel deconvolution. By comparing Fig. 6.18(a) and Fig. 6.18(c), it is evident that we can recover the transmitted PAM-16 symbols. We can recognize the influence of the effective channel compensation carried out by the deconvolution procedure.

Here, we have to point out that we conducted I-Q transmission using repeated data symbols, and these symbols are reproduced as shown in Fig. 6.17 and Fig. 6.18. In principle, we have demonstrated that we can transmit two separate symbols independently on the I/Q channel. Therefore, a further extensive measurement campaign needs to be



**Figure 6.19:** I-Q channel separation measured at the receiver.

performed to evaluate the BER. We can conclude from the channel equalization plots performed on I and Q channel (s. Fig. 6.16a and Fig. 6.16b) that the deterministic error occurring on the Q-channel can be completely corrected.

The maximum possible chip-rate to be transmitted depends on the I-Q channel cross-leakage and the LO leakage of the 230 GHz receiver module [224]. The LO leakage sets a sharp usable IF bandwidth of 15 GHz. This is due to the feed-through of the LO signal back to the I-Q baseband down-converter circuits.

Figure 6.19 shows the I-Q channel separation at the receiver for different chip-rates for the RF-frontend used in expt. 1. We can conclude that more I-Q channel separation gain results in less I-Q cross leakage during the down-conversion at the receiver RF-frontend modules, e.g., in Fig. 6.19, for 5 Gcps we have an I-Q separation of 21 dB, and for 20 Gcps we have 3 dB. Thus, the above factor limits the chip-rate of 10 Gcps, wherein the I-Q separation is 17 dB.

## 6.7 Summary

The PSSS encoded waveform output is a discrete multi-level signal. A PSSS modulated signal always uses *m-sequences*, and it is fed only to the I-channel of the transmit RF-fronted module. We have discussed various HIL experiments setups, and they show that PSSS is a suitable modulation format candidate for THz frequency range transmission. A PSSS modulated waveform was transmitted using 230 GHz link to achieve a maximum data-rate of 80 Gbps.

For the first time, we have extended the concept of PSSS transmission on I-Q channels

by using Kasami codes. We have transmitted a Kasami coded signal with 10 Gcps with PAM-16 independently on the I and Q channels. This results in a cumulative data rate of 80 Gbps.

From our HIL experiments, we can conclude that the main limitations to higher chip-rates are the LO leakage, the available RF/IF bandwidth, and the I-Q cross leakage. The main limitation of targeting higher spectral efficiency is the linear gain of the transmit power amplifier in the THz radios.

## Chapter 7

# Conclusion

Innovative and efficient wireless technologies for a range of transmission links have to be developed to cater to the demands for higher data rates. In this thesis, we have argued a case for the PSSS modulation as one of the PHY layer technology with built-in support to mixed-signal processing. There is a strong requirement to develop new design concepts for antennas, RF- frontends, and baseband processing algorithms to cater for this high demand. The key performance indicators in the design of 100 Gbps systems are bandwidth, spectral efficiency, and energy efficiency. There are two possible ways to achieve 100 Gbps system. One way is to target lower transmission bandwidth and very high spectral efficiency. The above-method requires a lot of digital signal processing techniques that are power-hungry. Another direction is to opt for a high-transmission bandwidth and moderate spectral efficiency. We decided for this direction to implement the 100 Gbps system, where the major baseband processing is performed in the analog domain.

We chose the PSSS modulation since it facilitates signal processing operations like encoding, decoding, and channel estimation in the analog domain. Only channel equalization was performed in the digital domain. For the first time, we have shown a data rate of 80 Gbps using PSSS modulation with PAM-16 in our HIL measurement experiment by using the RF-frontends from TU Wuppertal [150].

PSSS was introduced as an IEEE standard in 2006 [223]. Since then, all the PSSS transmission experiments were done by utilizing only I-channel at the transmitter, and the Q-channel was unused. For the first time, we have demonstrated that Kasami codes can be used in both I/Q channels at the transmitter for data transmission to achieve 80 Gbps.

In the PSSS transmitter design, we implemented fifteen parallel PSSS encoders in 28 nm CMOS technology which operate at a clock rate of 1.785 GHz. The digital design segment of a PSSS transmitter has an energy efficiency of  $0.21 \text{ pJ bit}^{-1}$  [150]. Furthermore, the challenging task is to design an analog mux operating at a chip-rate of 30 GHz that has to be integrated with a group of parallel encoders via low-speed DACs operating

at a symbol rate of 1.67 GHz.

We target for a point-to-point communication scenario in the THz transmission range. We assume that the channel has a high coherence time. This allows for a sufficient time to estimate the channel and to perform the corrections. The channel equalization is as simple as replacing the correlator coefficient values evaluated from the “channel deconvolution” procedure. We have shown that the PSSS channel deconvolution procedure consumes a time about ten times more than the PSSS symbol time (1.67 GHz) with 40 nm NanGate ASIC technology.

In this dissertation, we have proved in principle that the PSSS modulation as an analog-friendly modulation scheme can be applied for systems operating in the THz frequency range. Thus, we have put forward a case for PSSS as a potential candidate for the baseband design in the THz frequency domain wherein massive bandwidth is available.

## Outlook

As we look into different potential 100 Gbps systems developed in electronics, photonics, or plasmonics (like OAM-MIMO, VLC, and so on) for THz frequency applications, one substantial thing stands out. It is that they all make use of either an AWG at the transmitter for a signal generation or a DSA at the receiver to analyze the recorded data. Thus, there is more than ever a need to focus our thinking on designing complete “End-2-End systems” consisting of the baseband, the MAC layer, and an RF-frontend. A further upcoming challenge in developing a complete “100 Gbps demonstrator” is the integration of the baseband developed in Real100G.COM, the MAC layer exhibited in End2End and the RF-frontends developed in the Real100G.RF.

Kasami codes do not have perfect autocorrelation properties, but they have good cross-correlation properties. This can be used for data transmission on I/Q channels. This opens up a whole new field of possibilities, e.g., we can transmit different spectral efficiencies separately on I/Q channels depending on the RF-frontend impairments, and perform a separate channel estimation for I/Q channels.

The complexity of the channel deconvolution depends on the length of the *m-sequence* in the PSSS system. The channel deconvolution procedure consumes more hardware resources and introduces latency (i.e., calculation of DFT and IDFT) for a more extended period length *m-sequences*, e.g., PSSS – 511 or PSSS – 1023. Thus, an approach to make channel deconvolution independent of the *m-sequence* length, and more hardware efficient is discussed in one of our patents [225].

The IEEE standardization activities extended to frequency bands up to 3 THz. As we move into the higher frequency bands, the available baseband bandwidth increases, and it can span over more than 100 GHz. Hence, we have addressed high-speed synchronization, which is independent of the data modulation scheme in our second patent [226] and it works in conjunction with PSSS modulation.

To this end, PSSS helps to build an ecosystem for high-speed PHY layer baseband designs comprising a channel equalization scheme, a synchronization scheme, and its inherent property to promote mixed-signal processing techniques addressing the THz frequency regime. With the emergence of THz communication systems, societies will experience unlimited wireless connectivity, virtual reality, and HD streaming are amongst many promising applications to be built in the THz frequency band.

## Appendix A

# Probability distribution: PSSS Encoder

In this Chapter, the probability distribution analysis of discrete amplitudes occurring at the output of the PSSS encoder is presented. Here, we consider the specific example of an  $m$ -sequence of length 15, which results in the PSSS encoding matrix of order  $15 \times 15$ . We used a PAM-16 symbol representation for the data symbols. The analysis was presented in our article Ref. [144].

### A.1 Probability distribution analysis

The probability distribution of multi-level amplitudes appearing at the output of the PSSS encoder  $\vec{S}$  (as in Eqn. (3.12)) is evaluated. Due to the cyclic permutations of the  $m$ -sequences in the coding matrix  $C$  (as in Eqn. (3.13)), the entries in the signal vector  $S$  in Eqn. (3.12) can be expressed as

$$\begin{aligned} S_1 &= \sum_{i=1}^N C_i d_i, \\ S_2 &= \sum_{i=1}^1 C_{i-1+N} d_i + \sum_{i=2}^N C_{i-1} d_i, \\ S_3 &= \sum_{i=1}^2 C_{i-2+N} d_i + \sum_{i=3}^N C_{i-2} d_i, \\ S_j &= \sum_{i=1}^{j-1} C_{i-(j-1)+N} d_i + \sum_{i=j}^N C_{i-(j-1)} d_i. \end{aligned} \tag{A.1}$$



The range of values for each entry  $S_j$  is:

$$\begin{aligned} \text{Minimum of } S &: -15 \cdot 15 = -225 \\ \text{Maximum of } S &: 15 \cdot 15 = 225 \end{aligned} \tag{A.2}$$

with a spacing of 2.

The noteworthy factor contributing to the probability distribution of  $S$  is the number of combinations of the data vector (as in Eqn.(3.11)), not the permutation. The computation of the multi-level amplitude probability distribution  $S$  is done in three steps:

1. Considering eight entries with value 1 in the  $m$ -sequence, we assess the probability distribution of  $S$ . To assess this probability distribution, we use combinatoric logic [227] and the Urn Model [228].
2. We measure the likelihood distribution of  $S$  considering seven entries with value -1 in the  $m$ -sequence.
3. These two partial distributions are combined to calculate the full likelihood distribution of the multi-level amplitudes in  $S$ .

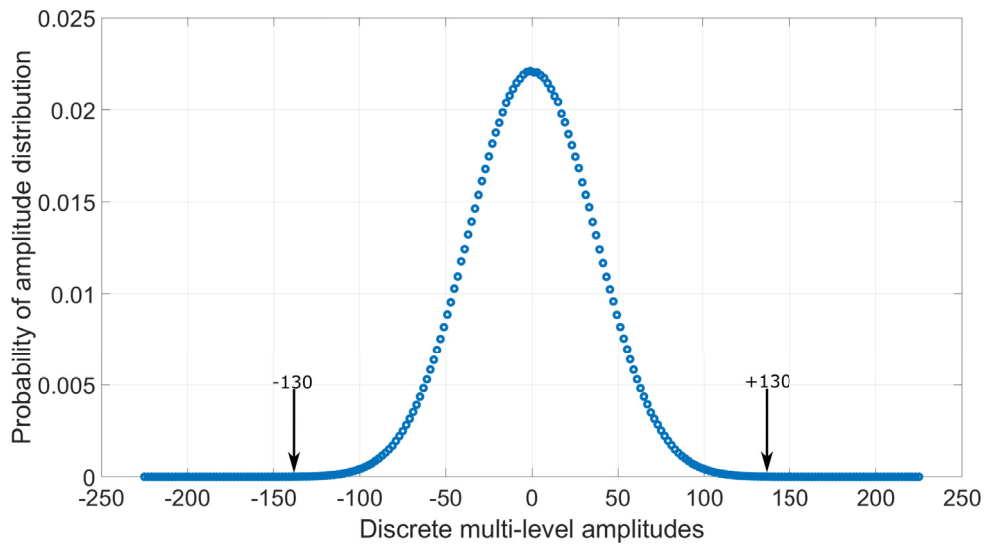
The range of values that the data vector  $\vec{D}$  can have is 16 (for a 4 bit/sec/Hz spectral efficiency). To get the probability distribution of  $S$  by simulation, we have to calculate the multi-level amplitudes of  $S$  (as in Eqn. (A.2)) for  $16^{15}$  (for an  $m$ -sequence of length 15, and for a spectral efficiency of 4 bit/sec/Hz) totally different entries of the data vector. Consequently, there would be a huge effort in simulating all attainable input data vectors combinations to realize the output results. As mentioned previously, we have to estimate the combinations of the data vector  $\vec{D}$  leading to the distinctive entries in  $S$ . From Refs. [227, 228], we will acquire the distinctive combinations of the data vector  $\vec{D}$  as in Eqn. (A.3)

$$\text{combinations of } D = \binom{L + N - 1}{N} = \binom{16 + 15 - 1}{15} = \binom{30}{15} \tag{A.3}$$

A multinomial distribution [227] encompasses a set of  $k$  potential results  $X_1, X_2, X_3, \dots, X_k$  with associated probabilities  $p_1, p_2, p_3, \dots, p_k$ , wherein  $\sum p_i = 1$ . Then for  $n$  perennial trials of the method, let  $x_i$  indicate the quantity of times that the result  $X_i$  happens, subject to the limitations that  $0 \leq x_i \leq n$  and  $\sum x_i = n$ . Then, the multinomial distribution is provided:

$$P(X_1 = x_1, X_2 = x_2, \dots, X_k = x_k) = \frac{n!}{x_1! \times x_2! \times \dots \times x_k!} \times (p_1^{x_1} \times p_2^{x_2} \times \dots \times p_k^{x_k}). \tag{A.4}$$

By applying the multinomial distribution, we assess the first portion of the probability distribution of  $S$  (as in step 1) with eight entries in the  $m$ -sequence with values 1, and with the premise that all data vectors  $D$  are distributed uniformly. Equation (A.5) shows



**Figure A.1:** Different multilevel values of  $S$  (output of PSSS Encoder) are represented on the x-axis and the y-axis is the complete probability distribution of these multilevel values using (A.5) and (A.6) by an analytical method.

the partial probability distribution with  $n$  equal to 8 in (A.4), also the probability of all the incoming data vectors ( $\vec{D}$ ) is  $1/L$ .

$$P(X_1 = x_1, X_2 = x_2, \dots, X_k = x_k) = \frac{8!}{x_1! \times x_2! \times \dots \times x_k!} \times \left(\frac{1}{L}\right)^8 \quad (\text{A.5})$$

Now we assess a partial probability distribution of  $S$  (as in step 2) considering seven entries with value -1 in the  $m$ -sequence. In replacing  $n$  equal to 7 in Eqn. (A.4), we have a second part of partial probability distribution, as shown in Eqn. (A.6), if the data vectors  $\vec{D}$  are uniformly distributed.

$$P(X_1 = x_1, X_2 = x_2, \dots, X_k = x_k) = \frac{7!}{x_1! \times x_2! \times \dots \times x_k!} \times \left(\frac{1}{L}\right)^7 \quad (\text{A.6})$$

Therefore, these two probability distributions must be combined in order to attain the final probability distribution of discrete amplitudes at the PSSS transmission output. The algorithm to assess the entire distribution of  $S$  probabilities is as follows:

- Utilize Eqn. (A.2) to obtain a histogram of possible  $S$  values.
- Use the  $\vec{D}$  vector (Eqn. (A.3)) of each possible data combination.
- Compute with Eqn. (A.5) and Eqn. (A.6) the probability of each data vector sequence  $\vec{D}$ .
- Utilize Eqn. (A.1) to analyze the partial probability distribution of  $S$  (as earlier outlined in step 1 and step 2) for the above data combination.

- The final probability distribution shown in Fig. A.1 is obtained from combining Eqn. (A.5) and Eqn. (A.6).

At the output of PSSS encoder, the occurrence of multi-level amplitudes is depicted in Fig. A.1. We can observe in Fig. A.1, the discrete levels below -130 have probability distribution of  $1 \times 10^{-9}$  and the discrete levels above 130 have a probability distribution of  $1 \times 10^{-9}$ . Thus, we say most transmitted information is confined in the range of multi-level amplitudes from -130 to 130.

## A.2 Summary

The probability distribution multi-level amplitudes (or different chip values) occurring at the output of PSSS encoder is mathematically derived. For an m-sequence of length 15 with a PAM-16 data symbols representation, we have in-total 255 chip values after the PSSS modulation.

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# Acknowledgement

Of course, this work has also not been done without support. At this point, I would like to thank everyone who helped me.

My first thanks go to my doctoral supervisor Rolf Kraemer, who made this work possible in the first place. I thank him for all the excellent advice, for his patience while correcting many of my texts, for his helpful feedback, and for the opportunity to participate in international conferences. He supported me in everything: to learn German language, to attend many FPGA/ASIC courses, and to purchase whatever tools I required to get the job done. In fact, he is a kind of facilitator who taught me that a lack of funding should never block us from achieving the scientific goals.

I would like to thank Andreas C. Wolf<sup>1</sup> for his technical advice during the course of my PhD study. He taught me so many technical and practical skills which were required for completion of my work.

Eswara<sup>2</sup> was a good friend and helped me a lot with technical discussions on synchronization topics. Pedro Rodriguez<sup>3</sup> supported me during our measurement campaign in Wuppertal.

Lukasz<sup>4</sup> assisted me in learning FPGA design. Goran, Frank and Dan<sup>5</sup> showed me how to perform synthesis and implementation using Cadence tools for ASIC development.

I would like to thank my parents Manjula and Krishnegowda for their loving support and backing during my entire studies, including my doctorate.

My girlfriend Lara Wimmer has supported me substantially before handing over this work. She moved to Frankfurt Oder, and importantly she cooked hot foods in the weekends. She carefully proof read my thesis many times and also corrected it. She gave an idea on the points where to improve my thesis. Danke dir!

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<sup>1</sup>From Dr. Wolf Wireless GmbH

<sup>2</sup>From prof. Kallfass's group

<sup>3</sup>From prof. Pfeiffer's group

<sup>4</sup>From IHP

<sup>5</sup>From IHP