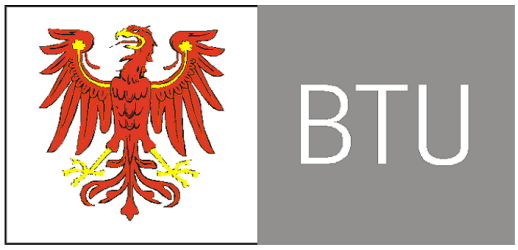

Millimeter-wave Integrated Circuits in SiGe:C Technology

A Dissertation approved by Faculty of Mathematics, Natural Science, and Computer Sciences

at Brandenburg Technical University Cottbus

in partial fulfillment of the requirement

for the award of academic Degree of Doctor of Engineering Science

(Dr. -Ing.)

by

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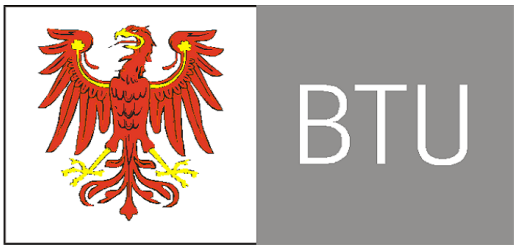

Integrierte Millimeterwellenschaltungen in SiGe:C Technologie

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Gutachter: Prof. Dr. -Ing. George Boeck

Gutachter: Prof. Dr. phil. Joe. McGeehan

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Dedicated to

My parents, my husband and my other family members
who always give me encouragement and support

and

All my colleagues and friends
who gave my great help during my study in Germany

Abstract

During the last decades the research and implementation of integrated circuits in W-band (frequencies from 75GHz to 111GHz) or frequencies beyond were mainly dominated by GaAs technologies due to their high-performance devices. However, the low-cost requirement of commercial consumer products limits the application of GaAs technologies. Recently, the advents of 200 GHz f_T SiGe:C technologies pave the way for realizing the millimeter-wave circuits with their lower cost and excellent performance. This work is focused on the design and implementation of circuits in IHP's low-cost SiGe:C technology at W-band and frequencies beyond.

Different types of high-speed frequency dividers as benchmarking circuits are designed and measured to show the speed and power performance of the SiGe technology in this work. Furthermore, this work includes the design and implementation of 77 GHz/79 GHz automotive radar front-end circuits. The results are compared with the state-of-the-art to demonstrate the performance of the circuit and technology. The aim is to show the design techniques and the possibility of adopting IHP's low-cost SiGe:C technology to realize high-performance circuits for high-speed applications such as future automotive radar system.

Declaration

The work in this thesis is based on research carried out at the IHP Microelectronics GmbH, Germany. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

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10 January, 2009

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Chapter 1

Introduction

During the past years, most of the reported millimeter-wave (mmW) circuits were realized by using GaAs technologies for their excellent device performance [1], [2], [3], and [4], etc. However, the high production cost, especially for mass production, limits their application in consumer products such as 77 GHz automotive radar and 60 GHz Wireless Local Area Network (WLAN).

Recently, silicon-based technologies have made significant progress. The use of single-poly silicon self-aligned transistor and the improvement in the doping profile strongly increase the speed of heterojunction bipolar transistor (HBT). Additionally, the possibility of being integrated with silicon complementary-metal-oxide-semiconductor (CMOS) allows digital and analog circuits on the same chip to realize the system-on-chip (SoC) or single transceiver solutions.

These advantages of the advanced silicon germanium (SiGe) BiCMOS technology motivate us to apply the SiGe BiCMOS technology as an alternative to III-V semiconductor for high-speed system applications. The major work in this thesis comprises: analysis of existing structures, proposal of an improved micromixer structure, design and implementation of high-speed circuits and

front-end circuits, focusing on automotive radar applications and using the low-cost SiGe:C BiCMOS technology of IHP Microelectronics GmbH.

1.1 Objective of the Work

The aim of this work is to present the high performance of integrated building blocks at microwave frequencies using the low-cost SiGe:C bipolar technology, including high-speed static and dynamic frequency dividers, low noise amplifiers (LNAs), down-conversion micromixer at 77 GHz/79 GHz frequency range and beyond.

First, the target and specification are well defined for each design based on IHP's technology. Second, the circuit topology and structure are analyzed during the design procedures. Not only the active transistors, but also passive elements such as resistors, capacitors, transmission lines and varactors are considered. Finally, each block is optimized to achieve the specification and a trade-off is always taken into account for conflicting circuit characteristics.

1.2 Thesis Organization

This thesis is organized as follows:

In Chapter 2, I firstly introduce the advanced IHP's SiGe:C technology based on. The process concept, basics of the fabrication process are described. The small and large signal models of the HBT transistors are also discussed.

Then I explain the necessity of automotive radar system for future car and analyze the system structures for automotive radar application in Chapter 3. A receiver structure consisting of an LNA and down-conversion mixer is adopted.

This single-ended LNA and down-conversion micromixer are realized for the first time at 77 GHz/79 GHz in SiGe technology.

Chapter 4 describes the design and realization of passive devices which will be used in the succeeding circuits. Simulation and measurement results of passive elements are shown.

In Chapter 5, the design and implementation of the high-speed frequency dividers are explained in detail. The measurement results and the comparisons to the state-of-the-art for each type of frequency dividers show the good performance of the circuit and technology.

Based on the structure analyzed in Chapter 3, Chapter 6 describes the design and implementation of the 77 GHz/79 GHz LNA. The measurement results and the comparison to the state-of-the-art are shown. Additionally, a 0.7 GHz - 1.4 GHz LNA for multiband application is designed and implemented.

In Chapter 6, the design and implementation of the 77 GHz/79 GHz down-conversion micromixer in proposed structure are explained in detail. The measurement results are compared with the state-of-the-art.

Finally in Chapter 8, I present the implementation and measurement performance of 79 GHz receiver system, then summarize the work and give an outlook for future designs at mmW frequency range.

1.3 Original Contributions

The following original contributions are made in this thesis:

- A new micromixer structure, which was first proposed by the author of this thesis in [5], is presented in Chapter 7. The analysis and simulation

results [5] prove that the proposed structure shows improved performance in terms of gain and noise figure. Using this new structure, I designed and implemented a down-conversion micromixer at 77 GHz/79 GHz, and successfully measured it. This micromixer circuit achieves the highest operating frequency in the reported micromixers in SiGe technology at the time of the publication [5]. The mixer shows 60% better linearity and consumes 41% less power compared with the common Gilbert mixer in measurement. The paper [5] was awarded as the Best Student Paper in IEEE MTT-S International Microwave Symposium (IMS) 2006.

- A 77 GHz/79 GHz cascode LNA in single-ended mode is reported by the author of this thesis in [6]. This is the first cascode LNA at 77 GHz/79 GHz in single-ended mode in SiGe technology at the time of the publication [6]. The design and implementation are elaborated in Chapter 6.

- The 79 GHz single-ended automotive radar receiver in SiGe technology is first reported by the author of this thesis in [7]. The receiver includes the aforementioned single-ended cascode LNA, down-conversion micromixer, and VCO.

- In Chapter 5, I present the design and implementation of a static frequency divider which shows the highest speed-to-power ratio among the state-of-the-art in similar high-speed SiGe technologies. This work is published by the author of this thesis in [8], which was awarded as the Best Student Paper in IEEE MTT-S Silicon Monolithic Integrated Circuits in RF Systems (SiRF) 2006.

- I present the design and implementation of a digital dynamic frequency divider in SiGe technology, which demonstrates the highest operating

frequency among digital dynamic frequency dividers in SiGe technology so far.

Chapter 2

Silicon Germanium Carbon BiCMOS Technology

The whole work is based on the SiGe:C BiMOS technology of IHP, the technology was updated during the Ph.D work. Therefore the chips were fabricated in the different stages of the technology. In this chapter, I describe the technology and the important issues which are considered during the design procedures.

Firsly, section 2.1 describes the SiGe:C BiCMOS technology and the process of this advanced technology. Then, the transistor models are introduced in section 2.1.1. Finally, section 2.2 introduces the passive devices provided by the SiGe:C BiCMOS technology.

2.1 Single-poly Silicon Self-aligned Transistor

SG25H1 is an improved version of SGC25C which is IHP's first BiCMOS process, and offers bipolar transistors with 180 GHz cut-off frequency [9]. The active devices of the two technologies are same, the only difference is the

added thick metal five in the new SG25H1 technology. The HBT has a single-poly silicon construction and an implanted extrinsic base layer (Fig. 2.1). This layer is formed on isolator regions during the non-selective epi-process applied to grow the intrinsic SiGe:C base layer and a Si cap. The implantation step for doping the extrinsic base layer is carried out self-aligned to the outer edge of the poly silicon emitter, but not self-aligned to the emitter window. The high f_T is primarily due to a novel collector design, which substantially reduces base-collector charging and transit time. The key new SGC25C device features are the formation of the whole HBT structure in one active area without shallow trench isolation (STI) stripe between emitter and collector contacts, the complete lateral enclosure of the highly doped collector wells in the STI sidewalls, and the self-alignment of the collector contact region to the base poly-silicon edge (Fig. 2.1). This achieves lower collector resistances than the emitter resistance.

In addition, the new design reduces device dimensions and parasitic capacitance. The reduced collector area results in a 50% reduction in the collector-substrate capacitance compared to the HBTs of the previous BiCMOS generation (SGC25B). Furthermore, since the collector well fabrication is imple-

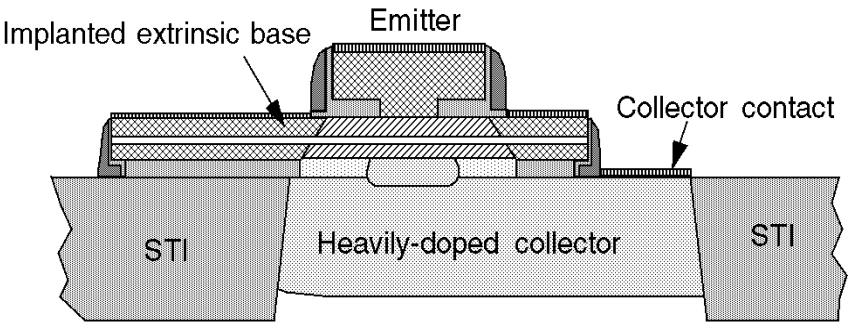

Figure 2.1: Cross section of SiGe:C HBT in SGC25C technology.

mented after the critical thermal treatments, this device design produces extremely steep collector doping profiles and achieves better control of the width of the base-collector space charge regions. Finally, the absence of deep trench isolation (DTI) improves the heat dissipation and reduces the thermal resistance. The base-collector as well as the emitter-base depletion widths are also optimized by adjusting the buffer and cap thicknesses of the epitaxial layer stack in order to maximize f_T. Fig. 2.2 compares the f_T vs. I_C curves of SGC25B and SGC25C HBTs.

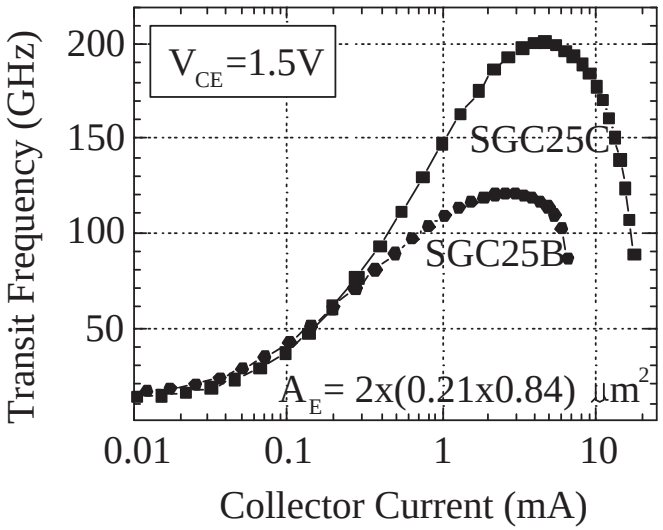

Figure 2.2: Transit frequency vs. collector current for SGC25C HBTs.

In the epitaxial grown base layer, the Germanium (Ge) content is linearly graded in the base up to a maximum value of 20% (Fig. 2.3). This enables band gap engineering and the fabrication of HBTs in silicon-based materials. Additionally, a boron (B in Fig. 2.3) peak is surrounded by carbon (C in Fig. 2.3) to suppress undesirable boron diffusion in the further steps of fabrication process. Table 2.1 summarizes the parameters of the bipolar transistor of SG25H1 technology. The bipolar devices with transit and maximum oscillation frequencies (f_T/f_{max}) up to 180/200 GHz enable high-speed application areas.

Because CMOS is not included in this work, so the description is omitted here.

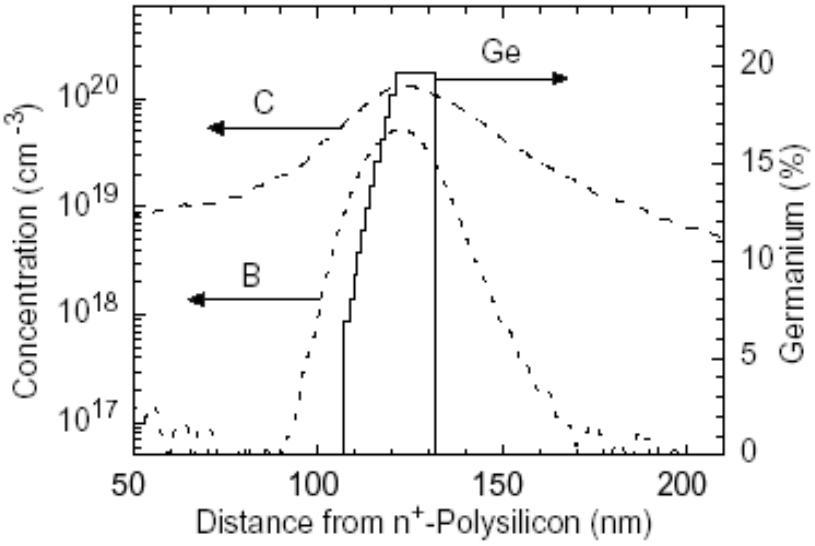

Figure 2.3: Doping profile.

Parameter	Value	Unit	Remark
Emitter area	0.21×0.84	μm^2	Drawn dimension
Current gain	300		$@V_{BE} = 0.7\,V$
Peak f_T	180	GHz	$@V_{CE} = 1.5\,V$
Peak f_{max}	200	GHz	$@V_{CE} = 1.5\,V$
BV_{CEO}	1.9	V	
BV_{CBO}	4.5	V	
Va	>40	V	

Table 2.1: SG25H1 transistor parameters

2.1.1 Vertical Bipolar Inter-Company (VBIC) Model

The design of radio-frequency integrated circuits requires accurate and compact models of the bipolar transistors. A large variety of bipolar transistor models have been developed so far. Starting from the original compact Ebers-Moll model which describes the fundamental DC behavior of the transistor using four parameters: the ideal forward and reverse common-base current gain

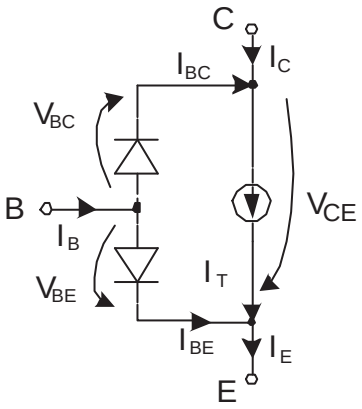

Figure 2.4: A simple equivalent circuit model for bipolar transistors.

(F and R) and the saturation current of the base-emitter and the base-collector diode ($IBES$ and $IBCS$). However many effects like the Early and Kirk effect as well as conductivity modulation are not covered. Another compact model that is more appropriate for the description of the bipolar transistor is the Gummel-Poon model [11]. This model is based on the integral charge control concept by introducing the normalized majority base charge q_b. So, many of the effects not contained in the basic Ebers-Moll model are incorporated in an integral, physical way. The Gummel-Poon model has been implemented in a slightly modified version into the circuit simulation tool SPICE [12], and this SPICE-Gummel-Poon (SGP) model has become a standard for modeling of bipolar transistors (Fig. 2.4). A comprehensive presentation of modeling high-frequency bipolar transistors can be found in [13]:

$$I_C = I_S(1 + \frac{V_{CE}}{V_{AF}}) \cdot exp(\frac{V_{BE}}{V_T}) \tag{2.1}$$

$$I_B = \frac{I_S}{\beta_F} \cdot exp(\frac{V_{BE}}{V_T}) \tag{2.2}$$

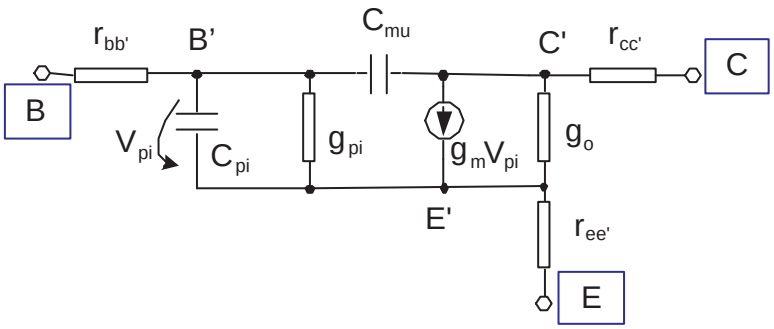

Figure 2.5: High frequency small-signal equivalent circuit model.

$$\alpha_F = \frac{\beta_F}{1+\beta_F}, \tag{2.3}$$

where I_S is the transfer saturation current, V_T denotes the thermal voltage, V_{AF} is the Early voltage, and β_F is the common-emitter forward current gain which relates to the already mentioned common-base forward current gain α_F via equation (2.3). The above equations characterize the large signal behavior of a bipolar transistor neglecting series resistance.

When the signal levels of the circuits are very small compared to the bias currents and voltages, then the small signal model (shown in Fig. 2.5) can be used to analyze the circuits. g_m, g_{pi}, and g_o are the input conductance, the transconductance, and the output conductance, respectively. They can be derived as the following:

$$g_m = (\frac{\partial I_C}{\partial V_{BE}})_{V_{CE}} = \frac{I_C}{V_T} \tag{2.4}$$

$$g_{pi} = (\frac{\partial I_B}{\partial V_{BE}})_{V_{CE}} = \frac{I_B}{V_T} \tag{2.5}$$

$$g_o = (\frac{\partial I_B}{\partial V_{CE}})_{V_{BE}} = \frac{I_C}{V_{CE} + V_{AF}} \tag{2.6}$$

The input resistance $r_{pi} = 1/g_{pi}$ and output resistance $r_o = 1/g_o$. The small signal current gain β_0 for short-circuit can be calculated as:

$$\beta_0 = (\frac{\partial I_C}{\partial I_B})_{V_{CE}} \tag{2.7}$$

The high-frequency behavior of the transistor can be modeled by two capacitors C_{pi} and C_{mu}. Each capacitance includes the diffusion and depletion parts. In forward operation ($V_{BC} < 0$, and $V_{BE} \gg V_T$), the diffusion charge of BC diode can be neglected, so:

$$C_{mu} = C_{jc}, \tag{2.8}$$

$$C_{pi} = C_{je} + \tau_F \cdot g_m, \tag{2.9}$$

where C_{je} and C_{jc} denote the depletion capacitance of BC and BE diodes, respectively. τ_F is the forward transit time, and $\tau_F g_m$ is the diffusion capacitance of the BE diode.

The frequency range of a transistor is usually defined by the frequency where the magnitude of current gain drops to unity

$$\beta(f) = \frac{\beta_0}{1 + jf/f_\beta} \rightarrow f_T \approx \beta_0 \cdot f_\beta, \tag{2.10}$$

where f_β denotes the 3 dB cutoff frequency of β, and f_T denotes the cutoff frequency of the transistor. f_T is related to the bias conditions, for a low collector current I_C, f_T can be calculated as [13]:

$$f_T \approx \frac{g_m}{2\pi \cdot (C_{je} + C_{jc})} \tag{2.11}$$

For a large I_C, f_T turns to be [13]:

$$f_T \approx \frac{g_m}{2\pi \cdot [\tau_F + (r_{ee'} + r_{cc'}) \cdot C_{jc}]} \tag{2.12}$$

At high collector currents, τ_F increases with I_C which results in a decrease of f_T . So there is an optimal collector current leading to a maximum cutoff frequency (Fig. 2.2).

Another important parameter of transistor is the maximum oscillation frequency f_{max}, which is defined as the frequency where the unilateral power gain of the transistor becomes unity [10]. It can be calculated as [13]:

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi \cdot (r_{bb'} + r_{ee'} + 1/g_m) \cdot C_{jc}}} \tag{2.13}$$

The SPICE-Gummel-Poon model also incorporates bias-dependent resistances for base and collector contact, an emitter resistance as well as diffusion and depletion capacitance. Further effects like carrier recombination in the space charge region and collector substrate coupling are considered, see [13].

The VBIC model developed recently is likely to replace the SGP model as the industry standard for SPICE circuit simulation of bipolar transistor-based integrated circuits. This model physically can be modeled as an npn and a pnp transistor connected between b, e, c, and substrate node, as shown in Fig. 2.6 (a). The model can also be electrically illustrated in Fig. 2.6 (b). The VBIC model is based on the SGP model, thus it can be degenerated into SGP model. Compared to SGP model, however, VBIC model includes more effects,

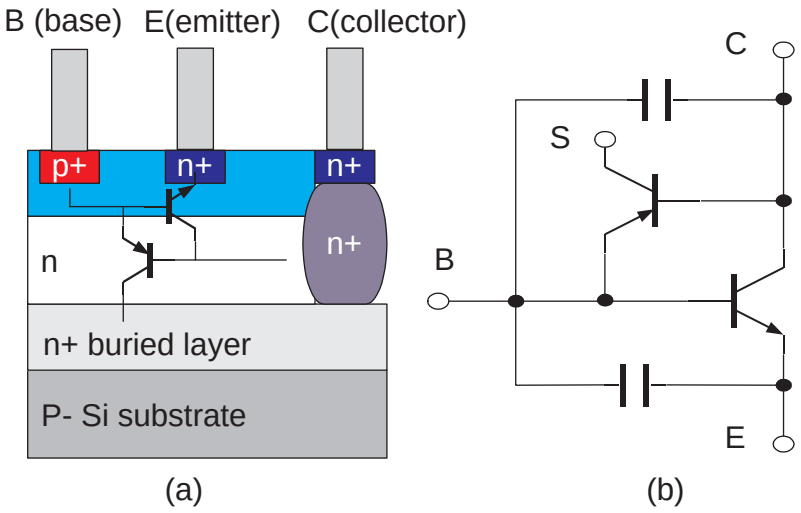

Figure 2.6: (a) Physical VBIC model, (b) Electrical VBIC model.

such as parasitic PNP, improved temperature modeling, and self-heating, etc. Therefore, it is an industry standard replacement for SGP model.

2.1.2 Comparison Between SGP Model and VBIC Model

The SGP model is a three-terminal model (i.e., emitter, base, and collector terminals) and consists of three current sources I_{cc}, I_{bc}, and I_{be}, two capacitance associated with the charges stored between base and collector terminals, and between base and emitter terminals, respectively, and four series resistances, two associated with the base region and the other each associated with the base and collector regions. The basic of all variants of the SGP model is the integral charge control model for the dc current passing through the emitter and collector terminals [11].

Fig. 2.7 shows the equivalent circuit of the new VBIC model. Unlike the conventional SGP model, which has three terminals, the VBIC model is a four-terminal model comprising the base, emitter, collector, and substrate denoted by the letters b, e, c, and s respectively. The other nodes in the VBIC are

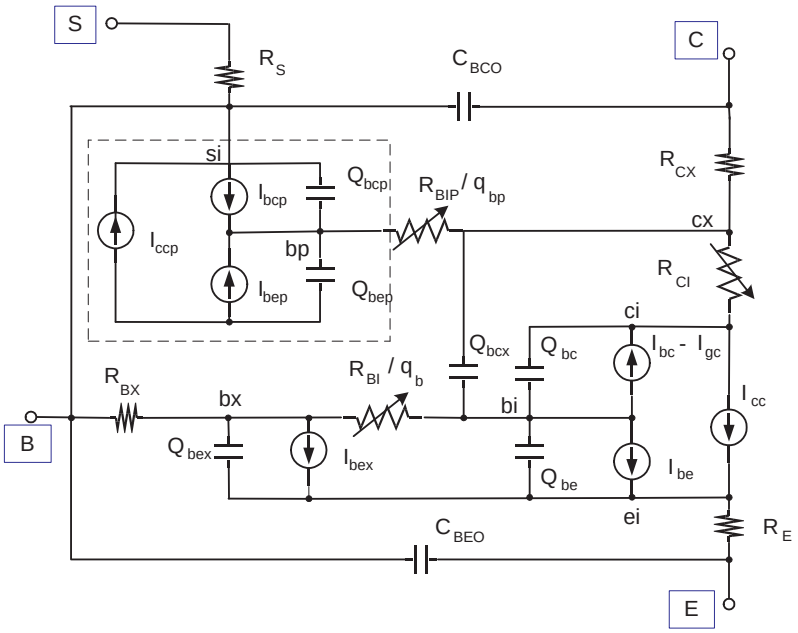

Figure 2.7: Equivalent circuit of VBIC model.

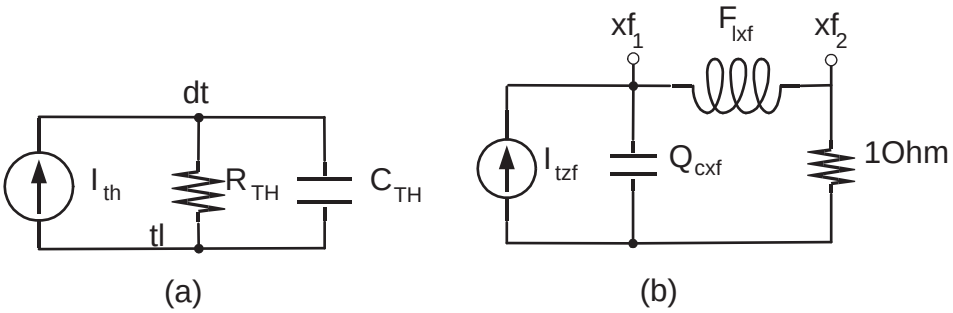

Figure 2.8: (a) Thermal network, (b) Excess phase network.

the extrinsic base *bx*, parasitic base *bp*, intrinsic base *bi*, intrinsic emitter *ei*, intrinsic collector *ci*, and extrinsic collector *cx*. Additionally, a thermal network and excess phase network are shown in Fig. 2.8 (a) and (b) respectively. The VBIC model includes several features that make it distinct from the SGP model. For example, the effect of parasitic substrate PNP transistor is included by a simplified SGP model (represented in Fig. 2.7 by the SGP equivalent circuit connected to the substrate terminal with components marked by a dashed block). Another feature included is that the quasi-saturation behavior

is modeled with the elements R_{CI}, Q_{bcx}, and a modified Q_{bc} [13]. Self-heating and excess-phase effects have also been accounted for in the VBIC model as separate options as shown in Fig. 2.8 (a) and (b) [14].

We can summarize the following major improvement of VBIC model over SGP model:

- Correct early effect model based on the junction charges without making simplification
- Modified Kull model for quasi-saturation valid into high-injection at the collector
- Parasitic substrate transistor
- Weak avalanche current is included for base-collector junction
- Self-heating model is defined as hooked in code by sub-circuit
- First-order model of distributed-base for AC and DC emitter crowding
- Improved single-piecewise junction capacitance model is added as option
- Improved complete static temperature mapping
- Inclusion of overlap capacitance
- Improved high-level diffusion capacitance modeling
- Second-order excess phase network consistent with AC→transient
- High-order continuity in equations

The incompatibilities exist between VBIC and SGP model: Early effect modeling and I_{RB} emitter crowding model. In sum, VBIC model is designed to be

similar to SGP model, but overcomes its major deficiencies. VBIC model is a public domain replacement for SGP model.

2.2 Passive Devices

IHP's SG25H1 technology provides five aluminum (Al) metal layers. The thickness of top metal five and metal four are 3 μm and 2 μm respectively. Between metal two and metal three, the metal-insulator-metal (MIM) capacitor is formed, the capacitance per unit area is 1 $fF/\mu m^2$. The maximum capacitance of a unit capacitor achievable on chip is 4.9 pF. The expected capacitance can be freely defined by changing the area of the two plates of the capacitor or connecting capacitors in parallel or in series.

There are four types of resistors available in the SG25H1 technology. Table 2.2 summarizes the characteristics of the resistors.

Components	Type	Sheet resistance ($\Omega/\square$)
R_{hbt} high ohmic	unsal. poly silicon	1.6K
R_{ppd} medium ohmic	unsal. p-doped poly silicon	210
R_{pnd} medium ohmic	unsal. n-doped poly silicon	280
R_{sil} low ohmic	sal. n-doped poly silicon	6.9

Table 2.2: Resistor types and values available in SG25H1 technology

Name	Value ($fF/\mu m^2$)	Quality factor	$V_{GateWell}$(V)
MCVAR_m25	2.7	132	-2.5
MCVAR_0	6.3	49	0
MCVAR_25	8.9	29	2.5

Table 2.3: Available MOS varactor models of the foundry library

The available nMOS varactor models are also shown in Table 2.3.

The passive devices such as transmission lines, inductors and transformers based on this metalization information aforementioned will be designed and discussed in Chapter 4 in detail.

Chapter 3

Structure of Automotive Radar Receiver

In this chapter, the necessity of the automotive radar system for future car is introduced, and the structures of receiver front-end are discussed. The advantages and disadvantages of several structures are analyzed by comparing the simulation results. Then the optimal structure is employed in this work. The design and implementation of the components corresponding to this structure will be elaborated from Chapter 5 to Chapter 8.

3.1 Introduction

To increase the safety of future car and avoid unnecessary collision such as tailgating caused by inattentiveness or unaided braking, the radar system is a very promising solution to improve the safety standard. Radar holds promise in a variety of automotive applications, from collision-warning systems, robotically controlled vehicles to speeding down a highway in convoys with the vehicles separated by inches. Although the latter application is at least a decade or

two away, radar is already used for adaptive-cruise control in luxury passenger vehicles, and prototypes are providing collision-avoidance assistance in heavy equipment.

The European Conference of Postal and Telecommunications Administrations (CEPT) represents 43 European regulators. CEPT, through European Radiocommunications Committee (ERC) Decision (92)02 [17], decided that the 77-81 GHz band should be designated to vehicular radar systems on a non-exclusive basis. Therefore it is desirable to offer every car in future to lower the number of accidents with lower cost.

Compared with the expensive GaAs technology, SiGe BiCMOS is a low-cost technology and allows fully integrated systems, making it perfectly suited for mass-market applications such as automotive radar systems. However, the capability of SiGe technology in the frequency range of 77 GHz to 81 GHz has so far not yet been established and is still in research. This work deals with the design of key blocks for automotive radar applications operating around 77 GHz/79 GHz in SiGe BiCMOS technology.

Fig. 3.1 shows the radar functions furnished to a car. The radar systems consist of two types: short range radar (SRR) and long range radar (LRR). The SRR detects 0.1 m to 20 m range. 24 GHz is the most used frequency but 77 GHz is also considered. The sensors could cover a lot of applications such as parking and back-up aid, but also "stop and go" function and side object detection, blind spot detection. The LRR detects the moving objects mainly in the range of 1 m to 200 m in front of the car, the speed is above 30 km/h and the angular coverage is around $+/-5^{\circ}$ respectively. Therefore it is also called Autonomous Cruise Control (ACC) radars. The frequency range is mainly from 77 GHz to 81 GHz.

During the last years, great progress has been demonstrated in GaAs technologies [1], [2], [3], [4], and [18], etc. However, due to their high cost, the mass market of commercial radar products is still pending. The major cost contributors are the RF-front-end, MMIC, antenna system, and chip-packaging. Since the cost of the first two contributors will be reduced by the production volume, and chip-packaging is dependent upon the system architecture. Therefore, the system structure plays an important role in reducing the cost. So the structure of 77 GHz/79 GHz SiGe ACC receiver system will be analyzed and discussed in this chapter.

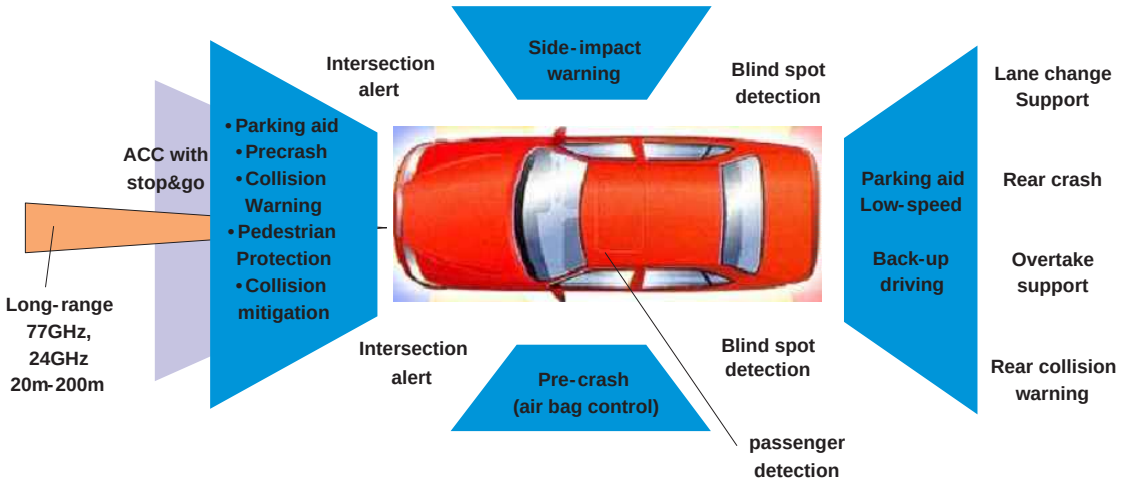

Figure 3.1: Radar system functions to improve safety of future car.

3.2 Structure Analysis

The three different receiver front-end structures of the radar system are depicted in Fig. 3.2. The LO signal and the received signal are in 77 GHz range, the modulated output intermediate frequency (IF) is between 50 MHz

and 1 GHz. These structures are based on the commercially available GaAs MMIC.

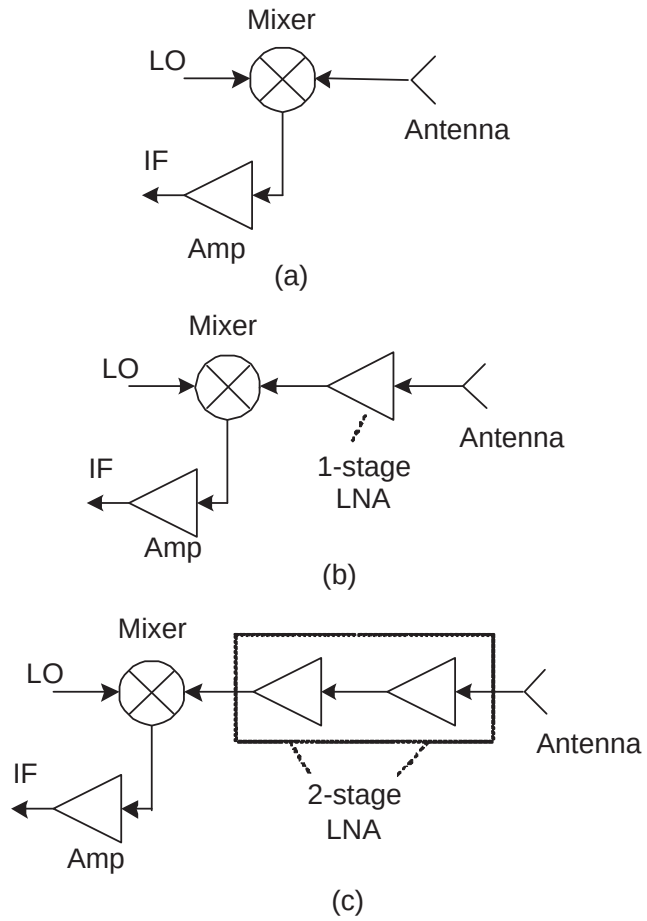

Figure 3.2: Three structures of the radar receiver front-end.

For structure (a), a balanced Schottky diode down-conversion mixer[1] is adopted. The achievable noise figure (NF) and conversion loss are around 18 dB and 8 dB respectively. This structure features low NF especially at very low IF frequencies, and is the simplest structure of the receiver unit. Thus the packaging is easier since only one bare mixer die is connected to the antenna, and the IF amplifier can be connected easily. While in structure (b) and (c), the one-stage and two-stage RF LNA are added for comparison. The RF LNA[2]

[1]UMS CHM2179
[2]UMS CHA 1077

shows 15 dB gain and 4.5 dB NF. Then by calculating the gain and NF of the whole receiver link using Friis' formula, we get a comparison listed in Table 3.1.

Structure	Gain (dB)	Noise Figure (dB)
(a)	-8	18
(b)	7	8.5
(c)	22	7

Table 3.1: Summary of system data from different front-end structures

From the analysis above, we could find that the additional LNA in structure (b), compared with structure (a), improves the NF due to the dominance of LNA's NF in the whole link. Furthermore, additional LNA in structure (c) compared with structure (b) decreases the NF and increases the gain further. Therefore, structure (c) consisting of an LNA and mixer is selected for the 77 GHz front-end in my work due to the advantages of low NF and high gain. In the following chapters, the design of passive devices, the key building blocks such as frequency dividers, LNA, and down-conversion mixer will be presented in IHP's SiGe:C BiCMOS technology.

Chapter 4

Design of Passive Devices

The passive devices play very critical roles in the analog and RF circuit design, and the discrepancies between circuit simulation and measurement are often caused by them due to their inaccurate modeling, especially in the mmW frequency range. Additionally, parasitic effects are also not negligible in the circuit design of mmW range. In this chapter, I will focus on the design of passive device design for mmW circuits.

Firstly I will present the study and optimization for important devices such as transmission lines, inductors, and transformers. By using electromagnetic (EM) simulation tool — ADS Momentum, I will show the comparison between the measured and simulated data. These devices will be applied in the design of frequency divider, LNA, and mixer.

4.1 Brief Overview of SG25 Series Technology

The SG25H1 technology is a high performance SiGe:C technology developed by IHP Microelectronics GmbH in Germany. Besides the ability of combining

the high performance HBT and CMOS devices into one technology, this technology provides two thick top metal (TM) layers, i.e. metal five and metal four. SG25C is SG25H1's previous version and provided one thick metal layer, i.e. metal four. The metalization stack of IHP's $0.25\,\mu m$ SG25H1 technology is shown in Fig. 4.1. There are totally five aluminum (Al) metal layers provided by this technology. The thickness of metal five layer and metal four layer is $3\,\mu m$ and $2\,\mu m$ respectively, while the other three thin metal layers have $0.73\,\mu m$ or $0.58\,\mu m$ thickness. The dielectric constant between the layers is 4.1. Between metal two and metal three, the MIM capacitor is formed, the capacitance per unit area is $1fF/\mu m^2$ and the maximum single capacitor achievable on chip is 4.9 pF. Any expected capacitance can be flexibly obtained by defining the capacitor area and connecting in series or in parallel.

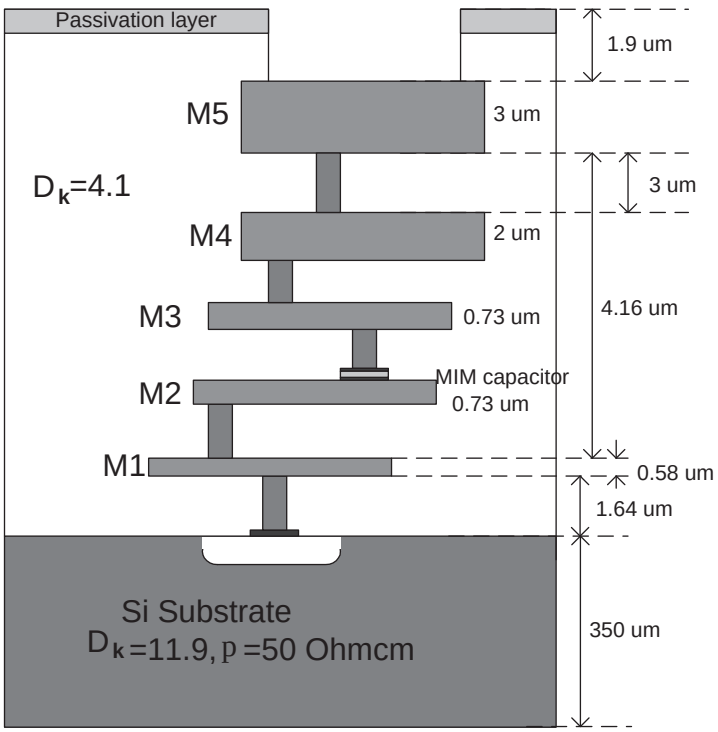

Figure 4.1: Cross-section of SG25H1 with thick metal five.

4.2 On-chip Transmission Line Design

When the operating frequency goes high up to tens of GHz, the length of the interconnection lines like the transmission line is comparable with the wavelength λ, the effects of transmission line become an essential part in the RF circuit design.

The basic intention of using transmission line is to transmit the signals between separate stages with impedance match or transformation. The transmission line should have characteristic impedance Z_0, acceptable loss A_0, and capacitance per unit length C_0. The characteristic impedance of a lossy transmission line can be expressed as:

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}}, \tag{4.1}$$

where R_0, L_0, and G_0 define the resistance, inductance, and conductance per unit length, respectively, so Z_0 is frequency dependent. If R_0 and G_0 are close to zero for ideally lossless conduction, or $R_0 \ll \omega L_0$ and $G_0 \ll \omega C_0$, or $R/L = G/C$, then we get an approximation of Z_0:

$$Z_0 \approx \sqrt{\frac{L_0}{C_0}} \tag{4.2}$$

The performance of signal transmitted on this transmission line can be expressed by the complex propagation constant:

$$\gamma = \sqrt{(R_0 + j\omega L_0) \cdot (G_0 + j\omega C_0)} = \alpha + j\beta, \tag{4.3}$$

where α is called the attenuation constant, and A_0 is is related to it by $A_0 = 20 \cdot log_{10}(e^{-\alpha})$, and β is the phase constant. Obviously, A_0 is a compositive

value related to the metal conductivity, dielectrics, and the Si substrate, thus the analysis is dependent on a full EM consideration in the design process.

Another parameter when we discuss the passive devices is the quality factor Q, which is defined as [19]:

$$Q = 2\pi \cdot \frac{E_{store}}{E_{diss}}, \tag{4.4}$$

where E_{store} and E_{diss} are the energy stored and energy dissipated per cycle, respectively. The higher the Q, the lower the loss dissipated by the device. Q is mostly related to the material properties of the technology, the semiconductor substrate and metal layers playing the most important roles in the performance.

4.2.1 Loss Mechanisms

The loss of the transmission line can be classified into DC/low-frequency and AC/high-frequency two types. The ohmic resistance of the metal line contributes loss for the whole frequency range. While at high frequencies, the time-varying EM field radiates to the materials surrounding it, this results in losses for ac signals. The energy can also be coupled to the conductive Si substrate as eddy current and displacement current. At increasingly higher frequencies, even without the substrate, the current distribution in the metal layers changes due to the eddy current in the metal, this is known as skin and proximity effects, and current crowding. Alternating currents take the path of smallest impedance and accumulate at the outer skin of the conductors because the magnetic fields penetrate the conductor and generate electric fields within the conductors. With the increasing frequencies, more energy is converted into heat due to the increased current density and decreased effective

cross section area. This skin effect is in proportion related to frequency by $\sqrt{f}$. The strength of the skin effect is displayed by skin depth δ in equation (4.5):

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}, \tag{4.5}$$

where ω is the angular frequency, μ represents the permeability and σ denotes the conductivity of the material. The skin depth in aluminum at 77 GHz is 0.33 μm.

The design of the passive device needs much effort to reduce the loss of the device and improve the Q value for expected inductance or capacitance. The composite effects can be analyzed in an advanced tool to provide accurate models for the high frequency integrated circuits. In the following sections, the most often used passive devices are analyzed and designed by using ADS 2.5-D EM simulator — Momentum, the simulation and measured results are compared. These are the preparation work for the integrated circuits in the succeeding chapters.

4.2.2 Microstrip Line and Metal Line Design

The Microstrip Line is constructed by the top metal layer (metal four of previous SGC25C and metal five of current SG25H1 technology) and bottom layer (metal one) as depicted in Fig. 4.2 (a). This minimizes the capacitance between metal layers compared with using metal two or other metal layers as the bottom layer as ground. Therefore it is possible to use wide metal trace as the conductor to minimize the ohmic loss for a targeted Z_0. The bottom metal layer as ground shields the electrical field from penetrating to the lossy substrate, therefore the loss of the transmission line consists of the conduc-

tor loss from the top metal and the eddy current resulted from the magnetic field coupling. While the structure of Metal Line is shown in Fig. 4.3 (a), the metal one shielding is omitted, therefore the electric-magnetic field penetrates further into the substrate and the additional dielectric loss in introduced.

4.2.2.1 Modeling

The lumped models of a Microstrip Line and Metal Line are shown in Fig. 4.2 (b) and Fig. 4.3 (b) respectively. The DC component R_s can be estimated by the sheet resistance of metal layer transmitting signal for low frequency operation. L_s represents the series inductance of the structure and can be calculated by using the formula from Greenhouse [20]. C_{ox} is the capacitance in the dielectric layer of SiO_2, C_{sub} and R_{sub} represent the capacitance and resistance into the substrate, respectively. C_{sub} and R_{sub} are also important parameters in achieving good agreement with the measured data at high frequencies. In the mean time, due to the nonuniform current flow resulted from skin effect and magnetic fields in the top metal layer at high frequencies, R_s is modeled as a frequency dependent parameter in equation (4.6) to improve the accuracy:

$$R_s = R_0 \cdot (1 + K_1 \cdot f^{K_2}), \tag{4.6}$$

where R_0 is the DC resistance, f is the operating frequency in GHz, K_1 and K_2 are constants [21].

4.2.2.2 Optimization and Experiments

The inductance and Q factor are analyzed for Microstrip Line and Metal Line in ADS simulation. One end of top metal line is connected to 50 Ω port, the other end is connected to ground in S-parameter simulation, since this is the

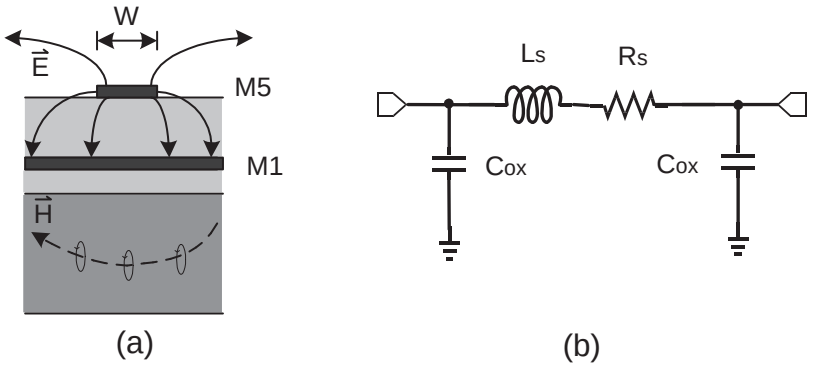

Figure 4.2: (a) Cross section of Microstrip Line. (b) Equivalent model of Microstrip Line.

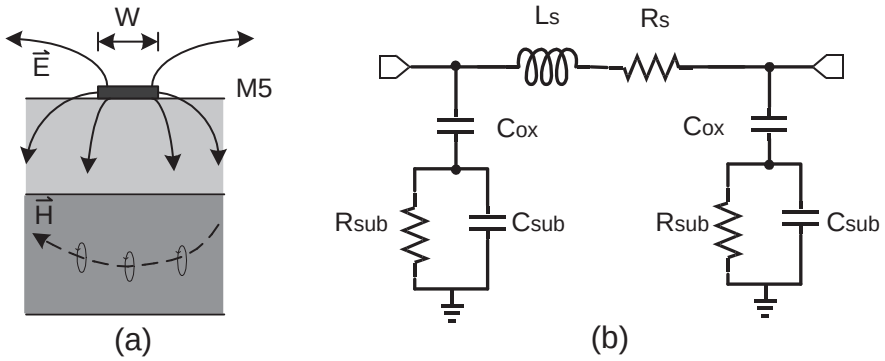

Figure 4.3: (a)Cross section of Metal Line. (b) Equivalent model of Metal Line.

common case applied in the amplifier circuits. The impedance of one port network is calculated by:

$$Z_{11} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}}, \tag{4.7}$$

and then the inductance is

$$L = \frac{Im(Z_{11})}{\omega}. \tag{4.8}$$

Q factor is calculated by

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})}. \tag{4.9}$$

Fig. 4.4 shows the EM simulation results of the Q factor and inductance for Microstrip Line and Metal Line [22]. We find that the inductance of Microstrip Line is relatively flat from 40 GHz to 80 GHz, and the values of Q factor between 60 GHz and 80 GHz for Metal Line and Microstrip Line are very close to each other.

In Fig. 4.5 and Fig. 4.6, the S-parameter simulation from 1 GHz to 110 GHz are illustrated for Microstrip Line and Metal Line in EM simulation and in lumped model simulation respectively [22]. From comparison we observe the expected relatively ideal reactive performance of Microstrip Line, and the obvious extra substrate loss suffered in Metal Line. Good agreements between EM simulation and lumped model simulation for Microstrip Line and Metal Line are achieved. In my circuit design at high frequencies, the Microstrip Line is preferred because of its reactive transformation and higher accuracy that are most expected.

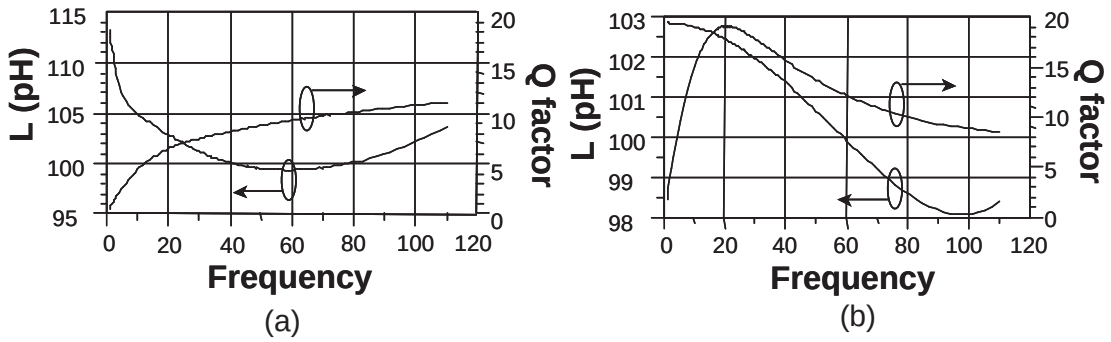

Figure 4.4: EM Simulation of inductance and Q factor for 0.1 nH at 70 GHz for: (a) Microstrip Line, (b) Metal Line.

The ADS EM simulation tool is adopted in the passive device simulation, modeling, and optimization. The structures in Fig. 4.7 are adopted to deembed the pad and interconnect parasitics. In the on-wafer S-parameter measurement, imperfections from the cables, probes, and connectors are negated by using

the standard Short-Open-load-Through (SOLT) calibration procedure. The measured and simulated S-parameter results for Microstrip Line are compared in Fig. 4.8 [23]. We find that the ADS 2.5-D EM simulation tool provides very good fit to the measured data from DC to 70 GHz, for the frequencies higher than 70 GHz, the discrepancy increases. To overcome the discrepancy between simulation and measurement, we should generate accurate models and minimize the parasitic effects in layout.

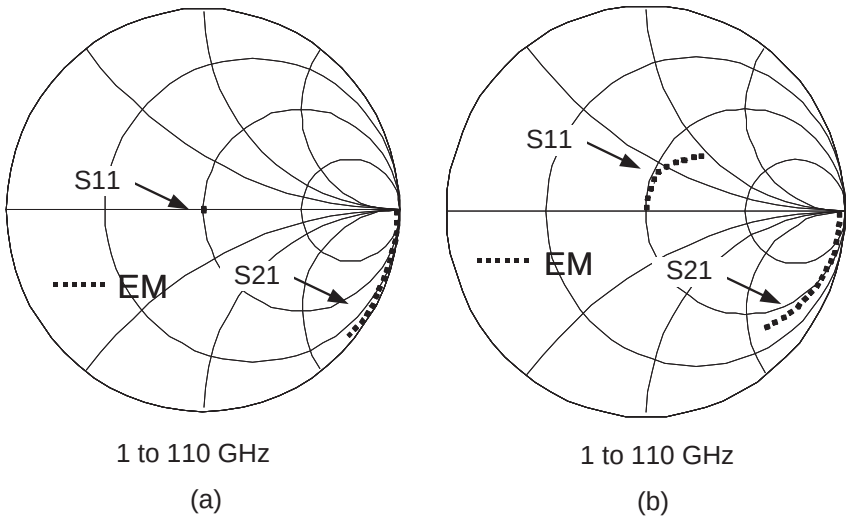

Figure 4.5: EM simulation for (a) Microstrip Line, (b) Metal Line.

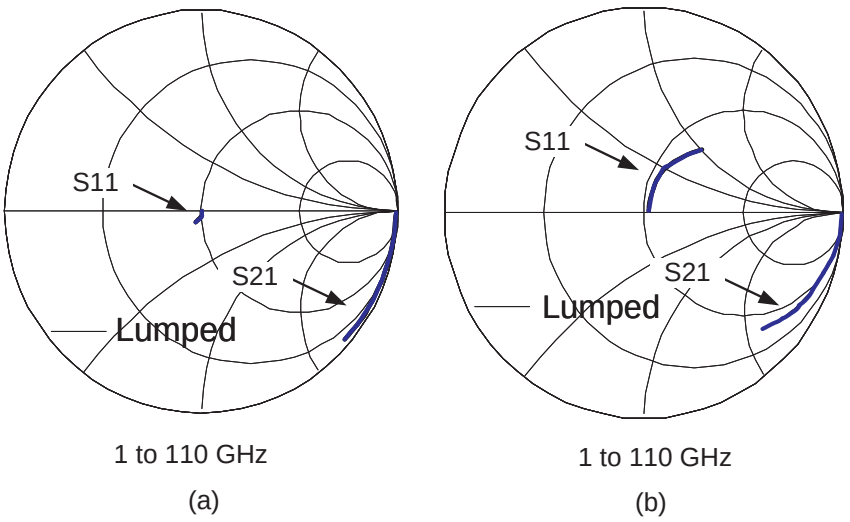

Figure 4.6: Lumped model simulation for (a) Microstrip Line, (b) Metal Line.

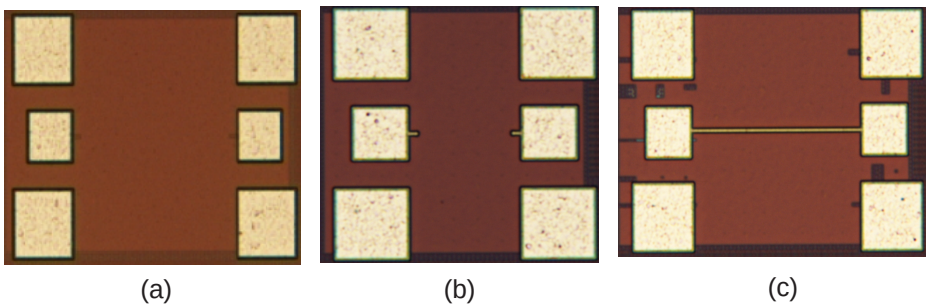

Figure 4.7: Die photos of: (a) Open test structure, (b) Short test structure, (c) Microstrip Line structure.

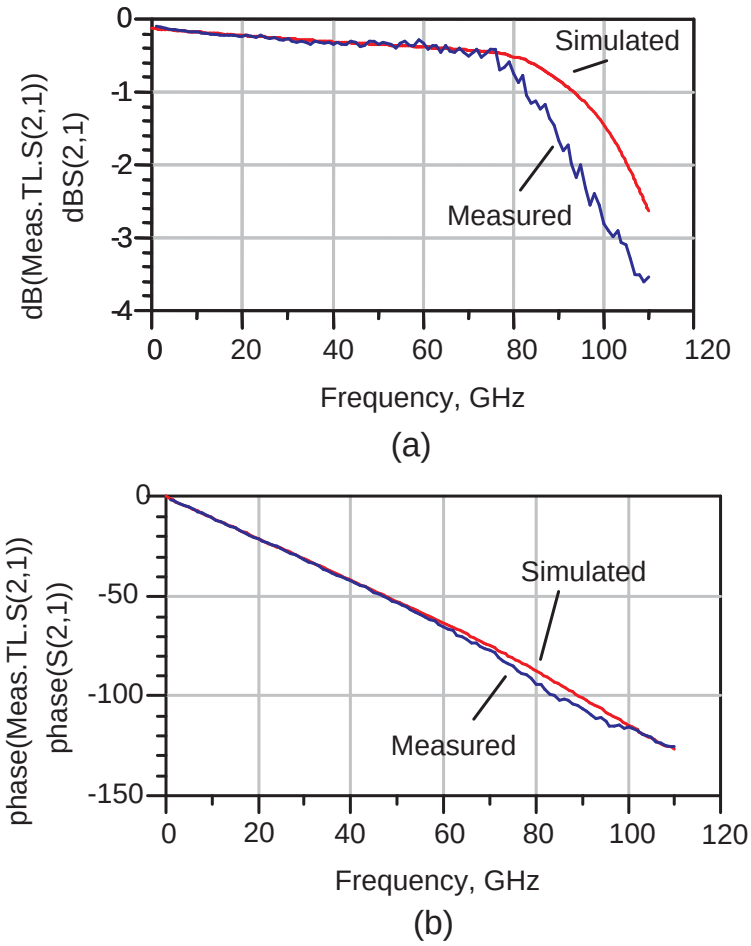

Figure 4.8: Simulation and measurement results of Microstrip Line (using metal four) 3 μm width and 200 μm length at DC-110 GHz: (a) dB(S_{21}), (b) Phase(S_{21}).

A Microstrip Line with 3 μm width 200 μm length is manufactured, which

uses metal four for signal transmission and metal one as the ground layer. The measurement results are shown in Fig. 4.9.

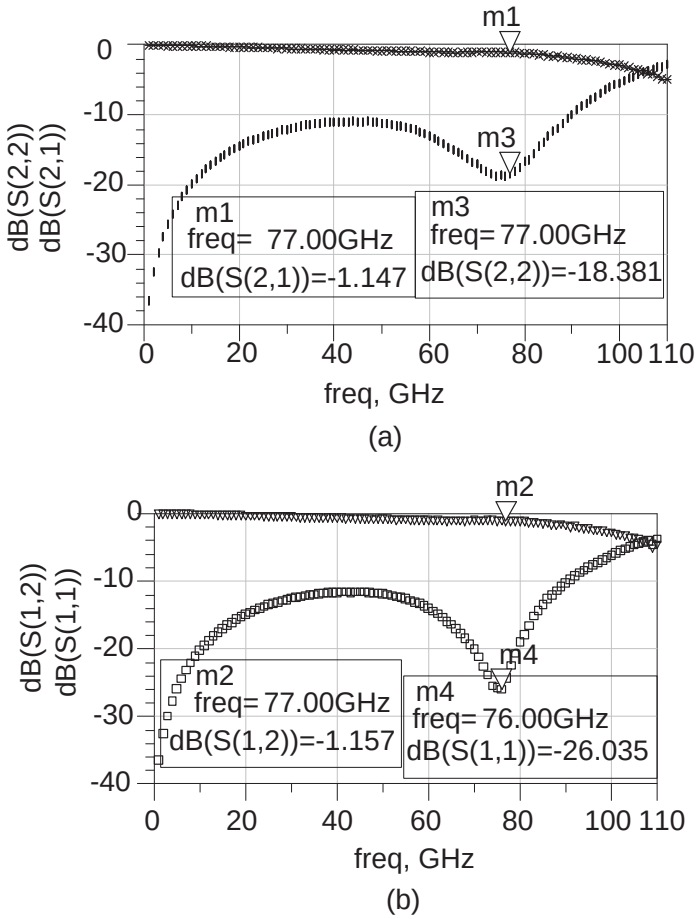

Figure 4.9: On-wafer S-parameter measurement of Microstrip Line (using metal four) with 3 μm width and 200 μm length.

Further, a comparison is made for Microstrip Line using metal five as the top metal for signal transmission, the on-wafer transmission coefficient S_{21} and its phase are shown in Fig. 4.10 (a) and (b) respectively.

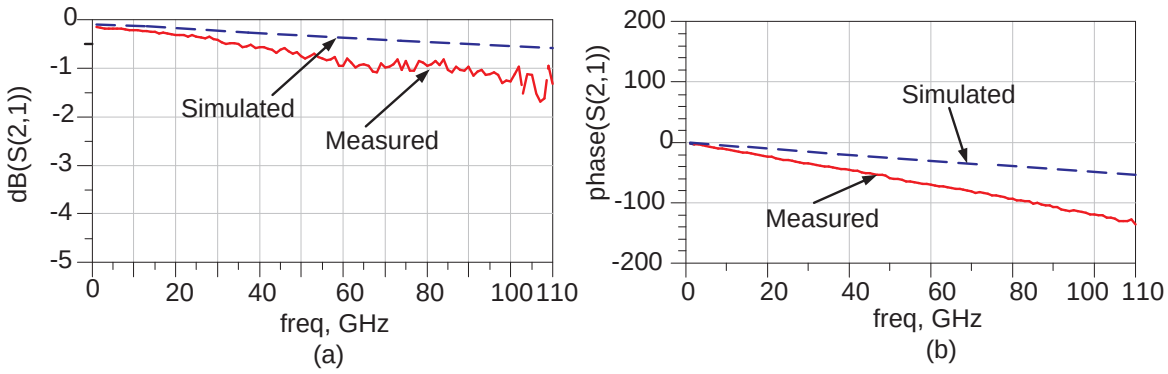

Figure 4.10: Simulation and measurement results comparison for Microstrip Line (using metal five): (a) dB(S_{21}), (b) phase(S_{21}).

4.2.3 Coplanar Wave Guide

Coplanar wave guide (CPW), which is different from Microstrip Line in configuration, employs the top metal both for signal and ground, the structure is shown in Fig. 4.11 (a). This structure confines the EM fields radiation to free space. Z_0 is dependent on the metal width W and space S between the signal line and ground. We know that L_0 decreases if the width W increases, and C_0 decreases if the space S increases.

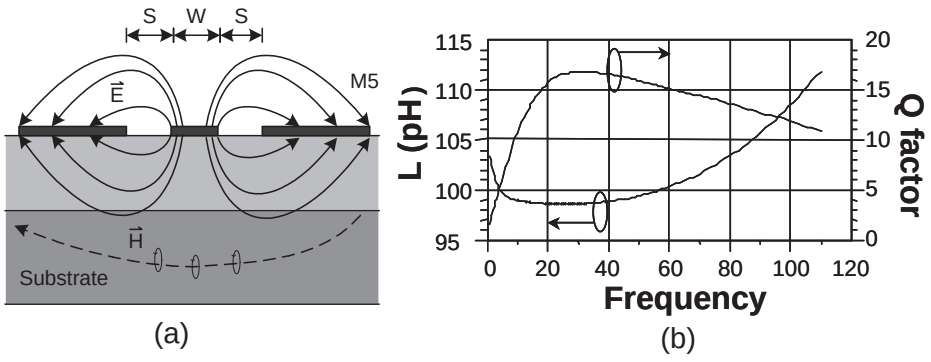

Figure 4.11: (a) Cross section of CPW, (b) EM Simulation of inductance and Q factor for around 0.1 nH at 70 GHz.

At higher frequencies, CPW structure with larger W and S induces more

substrate loss, which dominates the total loss at high frequencies.

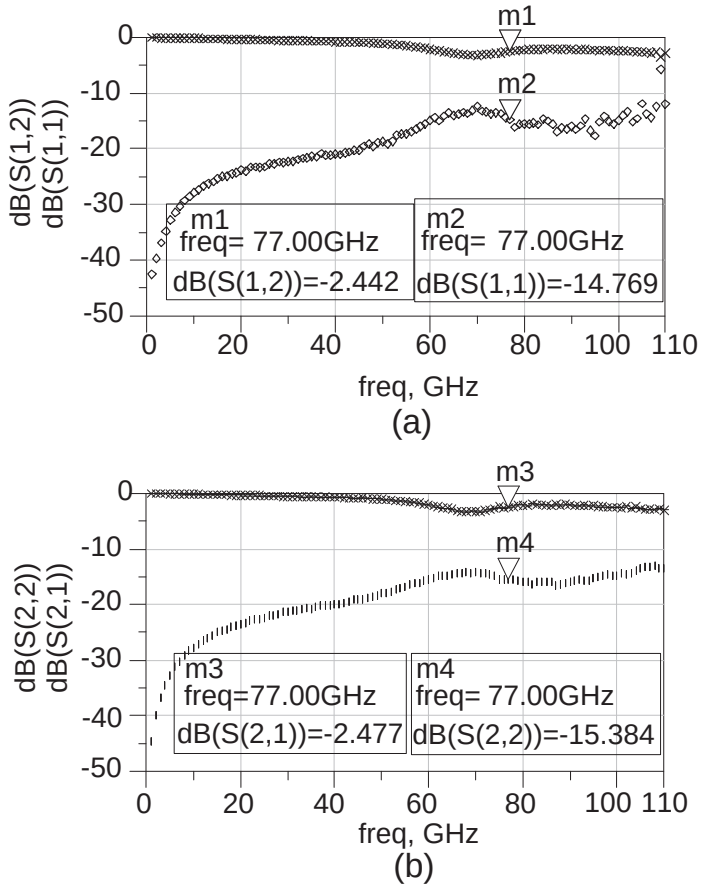

Figure 4.12: On-wafer S-parameter measurement of CPW line (using metal five) with 23 μm width and 54 μm gap, 202 μm length.

By analyzing the EM field of the CPW line, we know that CPW has stronger coupling effect to the lossy substrate especially at higher frequencies when the W or S is large, this results in significant losses. The EM simulation results are shown in Fig. 4.11 (b). Further, the CPW occupies much larger area than Microstrip Line because CPW needs large enough top metal as the ground layer.

An on-wafer measurement of CPW line at 77 GHz with 70.7 Ω characteristic impedance and 45° electrical length is shown in Fig. 4.12. Because CPW line suffers higher loss at high frequencies compared to Microstrip Line and Metal

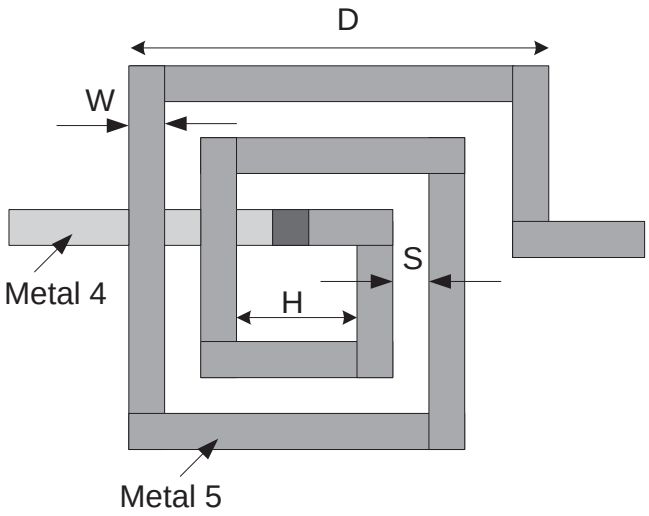

Figure 4.13: Plan view of a square inductor.

Line, and it occupies much larger area, so it is not adopted in my design.

4.3 On-chip Planar Inductor Design

On-chip inductor is another alternative passive component which provides larger inductance with compact area. However the on-chip inductor suffers from relatively low quality factor Q and limited maximum operating frequency. Further, the proximity effects of the nearby conductors enhance the magnetic field near a given conductor, the ac resistance will increase further. In my circuit design at W-band frequency range, this type of inductor is not adopted, but it is applied in an LNA design for variable band application around 1 GHz.

4.3.1 Design of Spiral Inductor

The most important parameters of the inductors like the trace width W, trace spacing S, outer diameter D, hollow sizes H and turn number N (shown in

Fig. 4.13) are analyzed in ADS Momentum in order to achieve the inductance with a high Q in the desired frequency range. The study on the above parameters with EM simulator is performed and we draw the following conclusions which are considered in the inductor design.:

- There is an optimal value W for maximum Q to achieve a targeted inductance. The larger the W, the larger the area covered by inductor surface, thus the larger the capacitance induced to the substrate. This results in the increase of loss to the substrate and decreases the self-resonance frequency. As W increases, maximum Q and the self-resonance frequency decrease, and the peak of the Q factor shifts to lower frequency.

- Additionally, there exists an optimal H/W value for maximum Q. Because, first, the inner turns of the inductor contribute less inductance due to smaller area, but they include larger series resistance due to strong center magnetic flux induced by eddy current at high frequencies. Therefore a hollow structure is beneficial. Second, the negative magnetic mutual coupling between opposite sides of the traces should be minimized by leaving an appropriate spacing.

- The trace distance spacing should be small to obtain tight magnetic coupling, and this also reduces the chip area. There is an optimal spacing to achieve maximum Q and self-resonance frequency.

4.3.2 Modeling

The cross section and equivalent circuit of a spiral inductor are shown in Fig. 4.14. C_p is the fringing capacitance between adjacent metal turns and

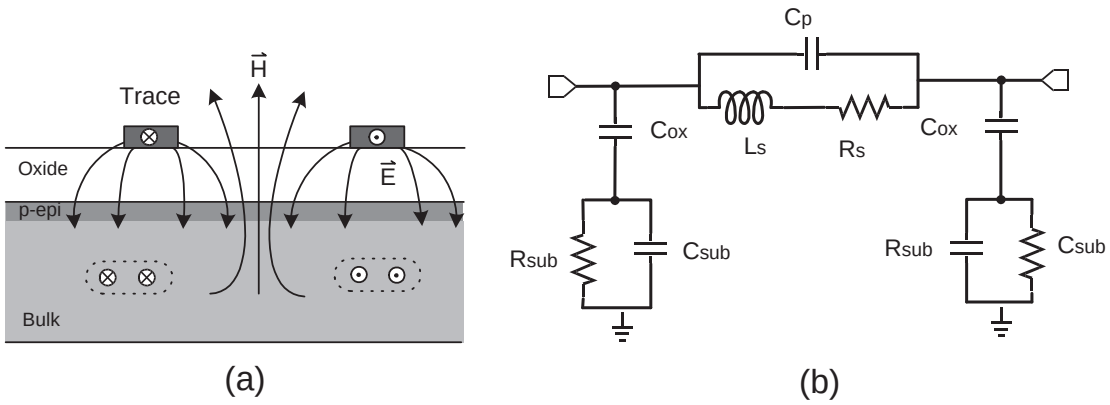

Figure 4.14: (a) Cross section of planar inductor. (b) Equivalent model of planar inductor.

the overlap capacitance associate with the underpass. This parameter is omitted for straight Microstrip Line and Metal Line models. The other parameters have the same definition as Metal Line.

The inductance and Q factor of the spiral inductor can be derived from the S-parameter:

$$L = \frac{Im(y_{21})}{2\pi f \cdot ((Im(y_{21})^2 + (Re(y_{21})^2))} \tag{4.10}$$

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{4.11}$$

4.3.3 Application

For W-band frequency circuits, the inductance needed in circuit is within 1 nH range in general, therefore it is enough to use microstrip line to realize the required small inductance. For a few GHz frequency range, the required inductance is about 5 nH and beyond, in this case, it is convenient to adopt the available on-chip inductor model with very high accuracy from foundry library.

4.4 On-chip Varactors

4.4.1 Principle

Variable capacitors (*varactors*) are semiconductor devices that are widely used in electronic circuits where a voltage controlled variable capacitance is required, such as voltage controlled oscillators, filters, and phase shifters, etc. The tunable network usually consists of varactors and inductors. The tuning range is related to the tuning ratio of C_{max}/C_{min} of the varactor and L_{max}/L_{min} of the inductor. Varactor is tuned by the control voltage and the inductance L can be either fixed or tuned by cutting the line with focused ion beam (FIB) technique [24]. FIB technology is a widely used tool for microelectronics. A FIB system using liquid metal ion sources is capable of forming very small probes with high current densities. The ions strike the specimen to remove materials through a physical sputtering process. A combination of a focused ion beam and a reactive gas also causes various physical effects on the specimen. Gas molecules above a specimen may be dissociated resulting in a local etching or deposition of the specimen. Based on these phenomena, the FIB system has been utilized in IC device modification, semiconductor process monitoring, failure analysis, micromachining, etc. Tuning varactor can be understood as a soft tuning while tuning inductor by using FIB can be understood as a hard tuning.

The quality factor of the varactor is relatively higher than that of on-chip inductor in optimum design, so on-chip inductor dominates the Q of the resonant circuit. The linearity of the tuning performance relies on the tunable capacitance versus control voltage.

In standard BiCMOS process, there are two kinds of devices that can be used

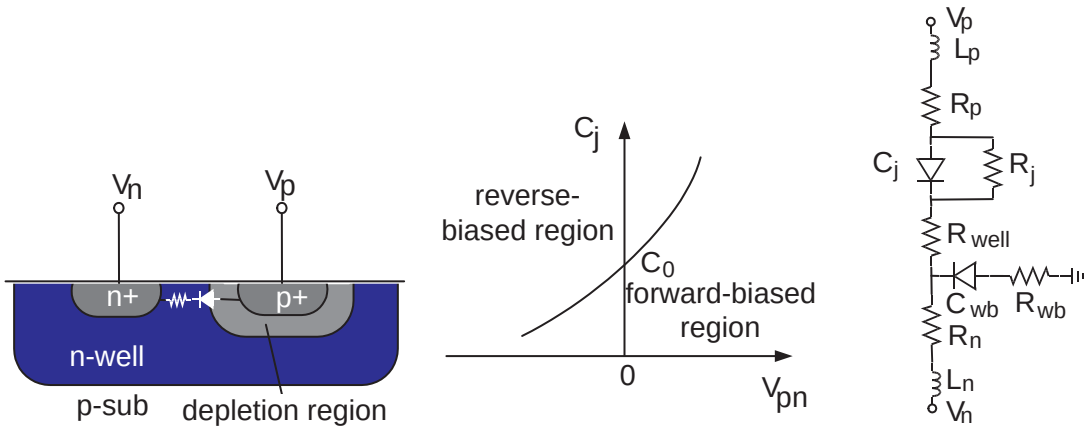

Figure 4.15: Junction varactor.

for varactors: junction varactors and MOS varactors.

- *Junction varactors*

The operation of this kind of varactor is based on the fact that a reverse biased PN junction acts as a variable capacitor and varying the junction voltage changes the capacitance. Although any ordinary diodes can be used this way, varactor diodes manufactured for this purpose can offer controlled and higher levels of capacitance variation. If a forward bias is across the diode, the depletion region decreases and the conduction takes place eventually. Therefore a reverse bias voltage is always placed across the varactor to prevent conduction. The cross section, $C_j(V) \sim V_{pn}$, and the equivalent model in reverse region are shown in Fig. 4.15.

When the voltage across the varactor diode V_{pn} changes, the width of the depletion layer varies. The larger the voltage, the wider the depletion layer, and the smaller the junction capacitance across the diode. This can be described as:

$$C_j(V) = \frac{C_0}{[1 - \frac{V}{\phi}]^\delta}, \tag{4.12}$$

where C_0 is the zero bias capacitance, ϕ is the built-in voltage which varies for different foundries, i.e, $0.7\,V$ for silicon PN junctions, and δ is a constant that is 0.5 for abrupt junction and 0.33 for a gradual junction.

- *MOS varactors*

By connecting the drain and source of a MOS transistor together, and the bulk to a fixed voltage, we can realize a MOS capacitor with capacitance controlled by the voltage V_{GS}. V_{th} is the threshold voltage of the transistor. In general application, V_S is used as the tuning terminal to avoid the parasitic capacitors on source/drain.

The cross section, capacitance tuning curve and equivalent model of an nMOS varactor are shown in Fig. 4.16. If $V_{GS} = 0$, the equivalent model consists of the oxide capacitor C_{ox}, $p^+ - implantation$ channel resistor and source/drain capacitors between gate and source/drain. If a small $V_{GS} < V_{th}$ is added to the terminals, the holes beneath the gate are pushed away from the surface and a depletion region between source and drain is created. The total C_{GS} is equal to C_{ox} and depletion capacitance C_{dep} in series connection. If we increase $V_{GS} > V_{th}$, then the mobile electrons build up the *inversion* channel. Under large V_{GS}, the conductive inversion layer with low resistance provides a maximum C_{GS}, i.e., equal to C_{ox}.

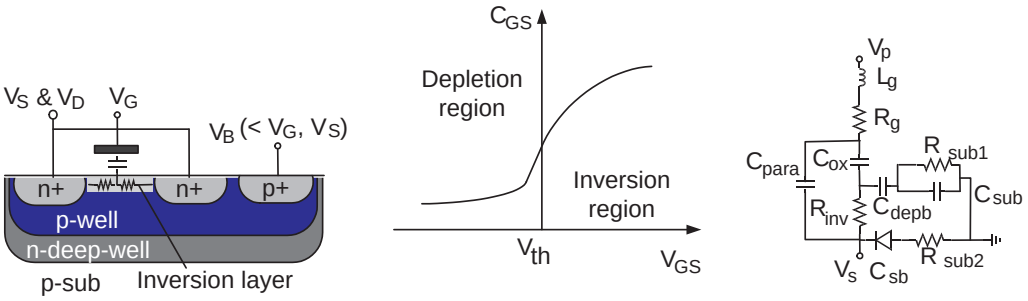

Figure 4.16: Inversion-mode MOS varactor.

To avoid the transistor entering the hole accumulation region, we can apply a lowest dc-voltage in the circuit (i.e., ground) to V_B, then the source/drain junction are always reverse biased and a monotonic tuning curve is achieved. The deep n-well in Fig. 4.16 provides good isolation to the substrate noise.

Another type of nMOS varactor is based on a different structure from the above type. The MOS transistor is placed in an n-well (Fig. 4.17), the terminal connections are same as the above mentioned.

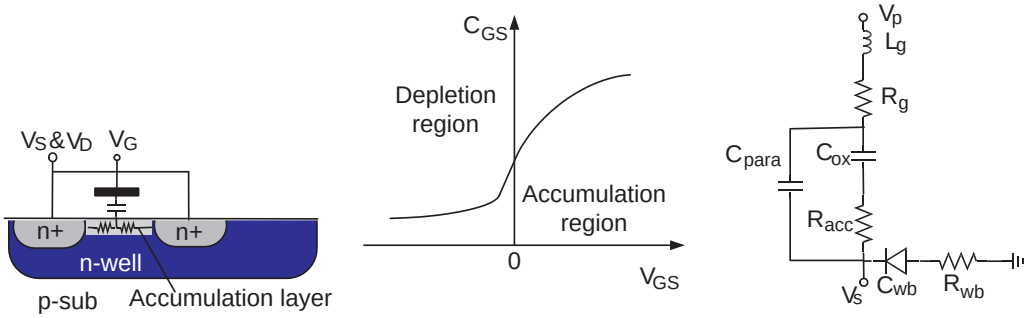

Figure 4.17: Accumulation-mode MOS varactor.

When we apply a negative voltage V_{GS} between gate and source/drain, the electrons beneath the gate are pushed away from the surface and a depletion region between source and drain is created. The total C_{GS} is equal to C_{ox} and depletion capacitance C_{dep} in series connection. The depletion region decreases if the V_{GS} increases. When we increase $V_{GS} > 0$, then with mobile

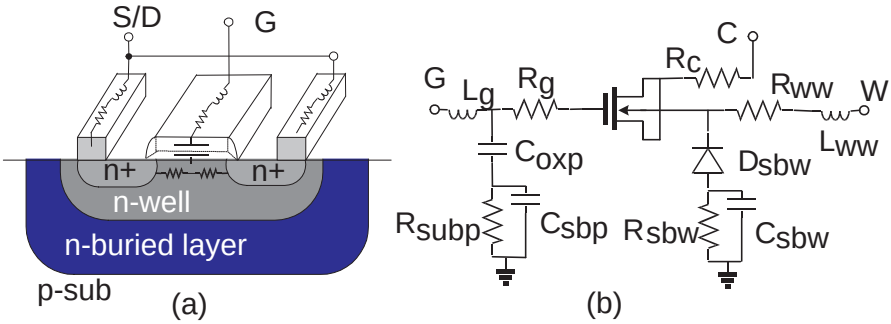

Figure 4.18: (a) Varactor cross section; (b) Schematic model of varactor.

electrons accumulate gradually at the n-well surface forming the conductive *accumulation* layer. Under large V_{GS}, the conductive accumulation layer with low resistance provides a maximum C_{GS}, i.e., equal to C_{ox}. Because there is no p-doping in this structure, the transistor will not operate in the hole inversion mode and a monotonic tuning curve is achieved.

For the two modes of nMOS varactors, the maximum capacitance is equal to $C_{ox} = \varepsilon_{ox}\omega\ell/t_{ox}$, where t_{ox} is the gate oxide thickness of the transistor.

The pMOS counterparts of the two modes of MOS varactors have the similar principle of operation with the only difference, that the holes compose the inversion layer in inversion mode and accumulation layer in accumulation mode.

4.4.2 Modeling

In the SG25H1 BiCMOS technology, nMOS varactor in accumulation mode is provided. The cross section and schematic model of the varactor are shown in Fig. 4.18 (a) and (b) respectively.

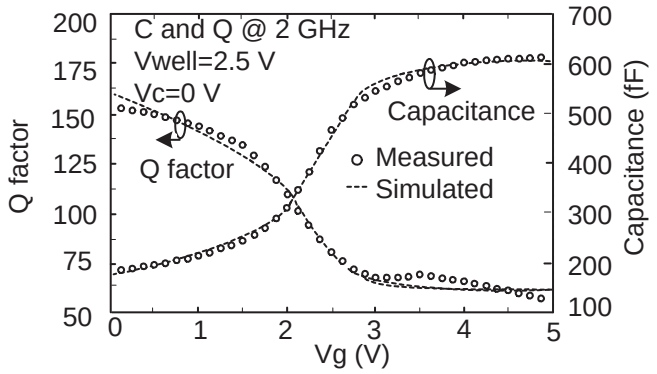

Figure 4.19: Q factor and capacitance versus tuning voltage.

The tuning ratio C_{max}/C_{min} of the varactor is around to 3 in IHP's foundry models. The measurement and simulation of varactor's capacitance and Q factor versus tuning voltage at 2 GHz are shown in Fig. 4.19.

4.5 Summary

This chapter presents the study and optimization of important on-chip microstrip lines, metal lines, CPW, inductors, and varactors, in 0.25μm SiGe BiSMOS technology, these passive devices are indispensable in the RF circuit design. The application of different devices is dependent upon the analysis and comparison of simulation results in ADS 2.5-D EM simulator — Momentum in different specific frequency bands. The optimization results are based on the given process conditions and restricted by them. In the circuit designs of the following chapters, on-chip microstrip lines, inductors, and varactors are widely used.

Chapter 5

High-speed Frequency Dividers

5.1 Introduction

Frequency divider is an important component widely used in the communication systems and measurement equipments. When sub-harmonic techniques are not used in a system, frequency dividers will deal with the highest frequency in the system. In this case, the transistors used by the frequency divider should be optimally biased to reach the full speed but with very high power consumption. While for dividers working at lower speed, the bias current can be greatly reduced. With the growing commercial demand for high data rate 60 GHz Wireless Local Area Network (WLAN) and automotive radar in mmW range, high-speed and low-power frequency dividers are very urgently needed. This is the major motivation of the work in this chapter.

In the following sections, I will report my design and implementation of three types of frequency dividers that are often used: static frequency divider, analog dynamic frequency divider and digital dynamic frequency divider. Firstly, the principle and structure of each type are analyzed. Then, the circuit design is

presented. Finally, the measurement results are compared with the state-of-the-art.

5.2 Static Frequency Divider

5.2.1 Principle

The basic cell of a static frequency divider is a D[1]-type flip-flop (FF). The D-type flip-flop itself is constructed by two D latches, one acting as a master and the other acting as a slave. With the inverted output $\overline{Q}$ connected back to input D, a T-type[2] FF (T-FF) is realized. Fig. 5.1 illustrates the configuration. The time domain transition diagram is shown in Fig. 5.2. The output of the T-FF toggles at the falling edge of the input clock signal, so the frequency of the output Q_s is half of the input frequency F_{in}, therefore we have realized a frequency divider with division ratio of 2. By simply cascading N stages of divide-by-2 circuits, we could realize a division ratio of 2^N (Fig. 5.3).

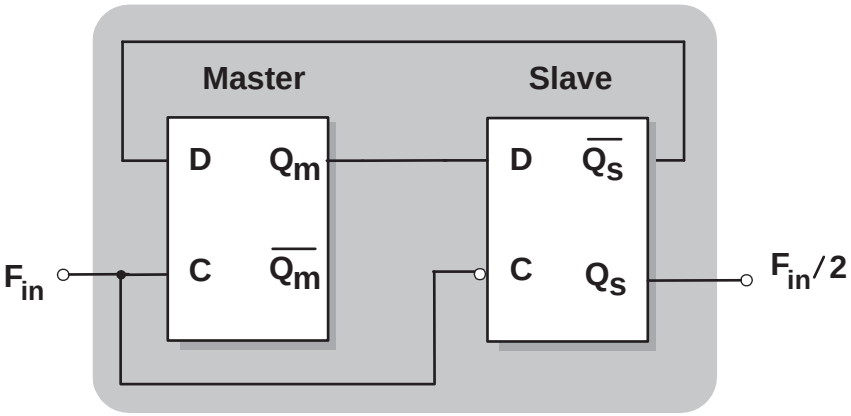

Figure 5.1: Block diagram of the T-type flip-flop.

[1] D stands for "Delay"
[2] T stands for "Toggle"

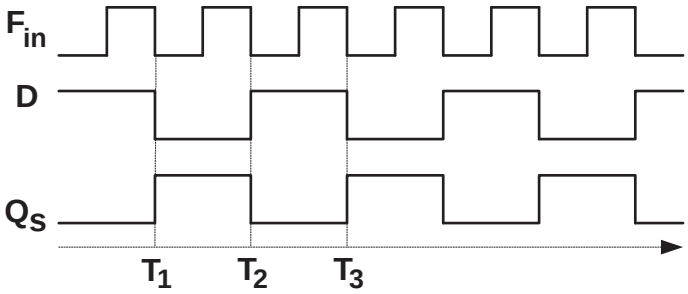

Figure 5.2: Transition diagram of the T-type flip-flop in time domain.

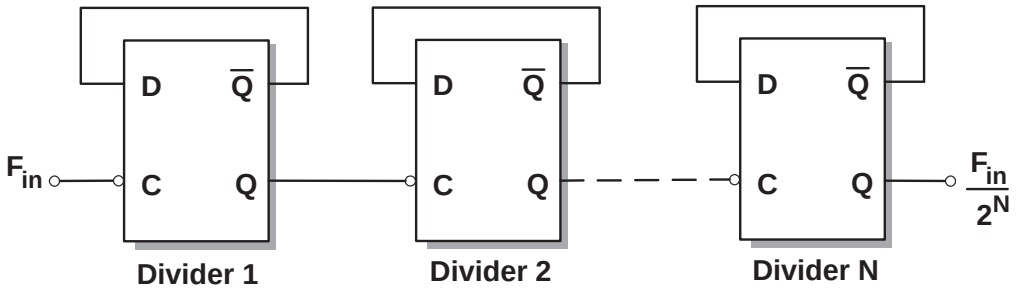

Figure 5.3: Frequency divide-by-2^N by series connection.

5.2.2 Circuit Design

5.2.2.1 Choice of Logic: Emitter Coupled Logic (ECL)

The most often used logic form is the differential current steering logic (CSL) family, such as source-coupled field-effect transistor logic ($SCFL$) for GaAs or CMOS, and emitter coupled logic (ECL) for bipolar transistor. If a logic form has several gates stacked above each other, then it is called E^2CL. The advantage of ECL is that no transistor is working in saturation region and the speed is high due to no injection of minorities into the collector. The structure is in differential mode and immune to common mode noise, thus the switching errors are reduced.

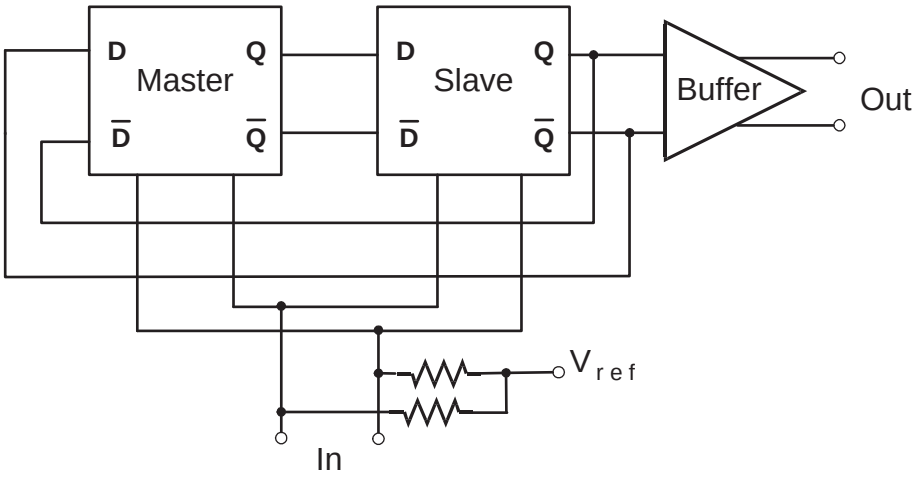

Figure 5.4: Block diagram of static frequency divide-by-2.

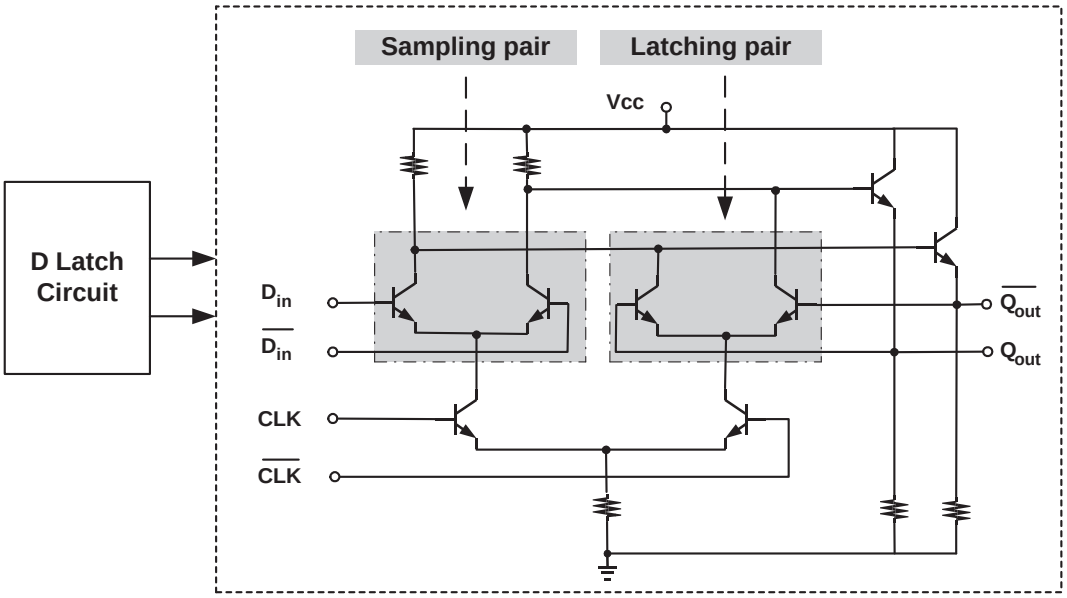

Figure 5.5: Schematic of ECL D-type latch.

5.2.2.2 Circuit of frequency divide-by-2

Fig. 5.4 depicts the block diagram of a static frequency divider, which consists of a clock input stage, a master-slave D-Flip-Flop (D-FF) with negative feedback, and an output buffer. The circuit of D-latch and the whole D-FF

are shown in Fig. 5.5 and Fig. 5.6 respectively. We choose one stage emitter follower (EF) between the D latch to speed up the transition of the switching pair and to provide the voltage level shifting. 50 Ω resistors are used to feed the DC bias for the sampling pair and to match the 50 Ω on-chip transmission line that connects to the probe at the input port. The FF employs a typical ECL which is biased near the optimal current for f_T by a current mirror. The output buffer consists of an EF pair and a differential amplifier with 50 Ω load matching to the output. The circuit is designed with a differential structure, but can also be measured and used in single-ended mode. Because there is a proportional relation between the power consumption and the circuit parameters [31]:

$$P \propto C \times V_{pp} \times V_s \times f, \tag{5.1}$$

where C is the total capacitance of the critical node, V_{pp} is the voltage swing, V_s is the power supply, and f is the operating frequency. Therefore, the power consumption at the designated frequency can be reduced by optimizing these parameters. Firstly, the sizes of the transistors in the critical path are optimized to reduce the load capacitance. Secondly, the voltage swing should be large enough to switch the transistors, and the voltage supply is reduced (in static frequency divider to be 3.5 V) to greatly reduce the total power consumption.

In Phase Locked Loop (PLL), a frequency divider is often followed by an edge triggered circuit such as Phase/Frequency Detector (PFD), which is a threshold sensitive circuit. The noise from the logic devices will be summed up in the overall edge jitter noise.

The signal from VCO feeding to the prescaler can be expressed as:

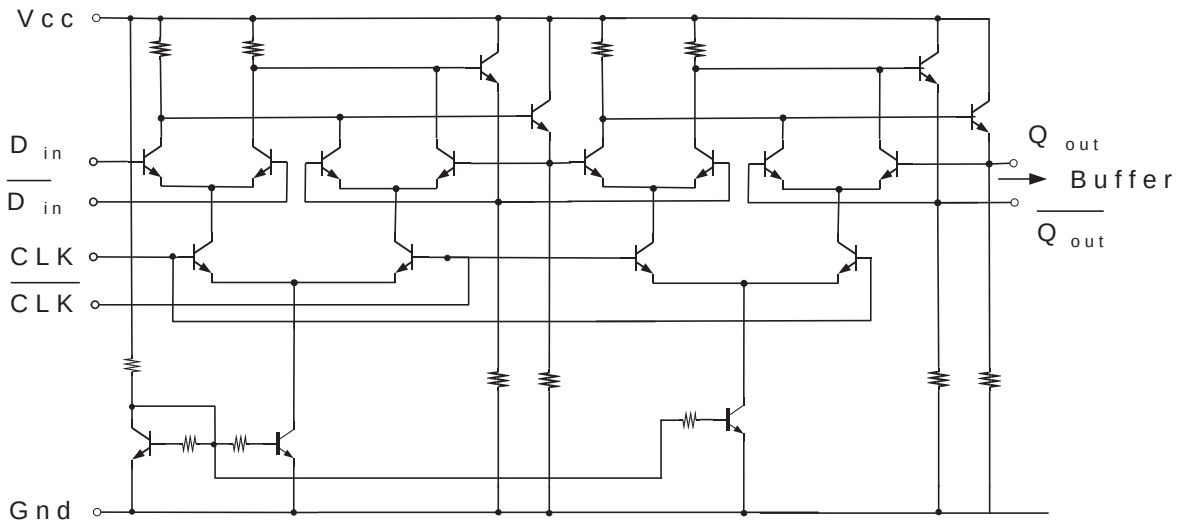

Figure 5.6: Schematic of the core of static frequency divide-by-2.

$$S(t) = V(t) \cdot cos\left[\omega_0 t + \theta(t)\right], \tag{5.2}$$

where $V(t)$ describes the amplitude variation as a function of time, $\theta(t)$ is the phase variation and referred to as phase noise. For a high-quality oscillator, the amplitude is very stable, and $V(t)$ can be considered constant. Then a carrier signal of amplitude V and frequency f_0, which is frequency modulated by a sine wave of frequency f_m, can be expressed by:

$$S(t) = V \cdot cos\left[\omega_0 t + \frac{\Delta f}{f_m} \cdot sin\left(\omega_m t\right)\right], \tag{5.3}$$

where Δf is the peak frequency deviation and $\theta_p = \omega_0 t + \frac{\Delta f}{f_m}$ is the peak phase deviation. From the equation (5.2) and (5.3), the instantaneous phase $\theta_i(t)$ of a carrier frequency modulated by a sine wave of frequency f_m is

$$\theta_i(t) = \omega_0 t + \frac{\Delta f}{f_m} \cdot sin\left(\omega_m t\right) \tag{5.4}$$

Instantaneous angular frequency is defined as the time derivative of the phase:

$$\omega = \frac{d\theta_i}{dt} = \omega_0 + \frac{\Delta f}{f_m} \cdot \omega_m \cdot cos\left(\omega_m t\right) \leqslant \omega_0 + \Delta\omega \tag{5.5}$$

If this signal is fed into the frequency divider with division ratio N, the output frequency ω_o is expressed as

$$\omega_o = \frac{\omega_0}{N} + \frac{\Delta\omega}{N} \cdot cos\left(\omega_0 t\right) \tag{5.6}$$

The output phase is:

$$\theta_o\left(t\right) = \frac{\omega_0 t}{N} + \frac{\Delta f}{N \cdot f_m} \cdot sin\left(\omega_m t\right) \tag{5.7}$$

The frequency divider reduces the frequency by N, the peak phase deviation is also reduced by N. The ratio of the noise power to carrier power is:

$$\frac{V_n^2}{V^2} = \frac{\theta_p^2}{4} \tag{5.8}$$

Based on these analysis, the influence on the phase noise of PLL is $20log\left(N\right) dBc/Hz$ from the frequency divider. Therefore when a divider is used as a component of PLL, we should also take the trade-off between noise influence and speed into consideration in the bias optimization of the circuit design. The difference between the optimal speed and optimal noise level varies between 10% and 20% in simulation [32].

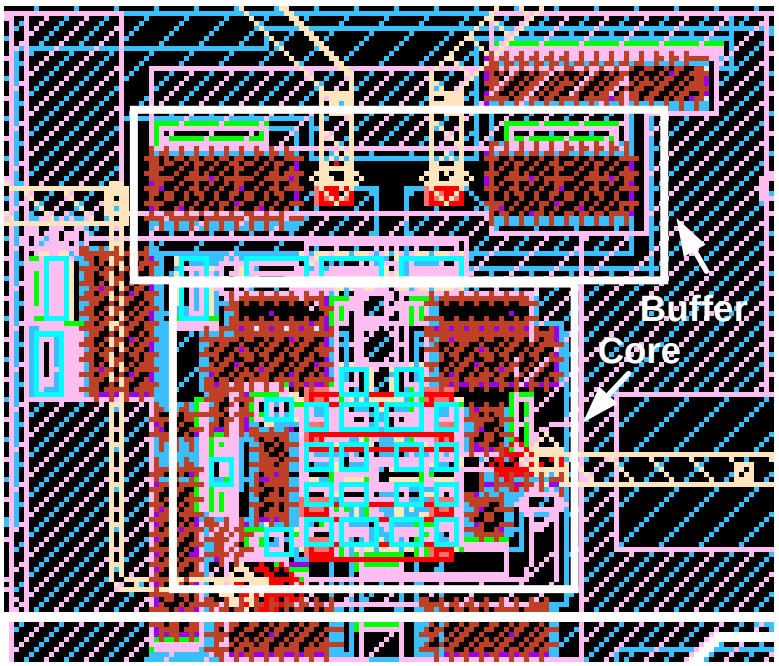

Figure 5.7: Enlarged layout of static frequency divide-by-2.

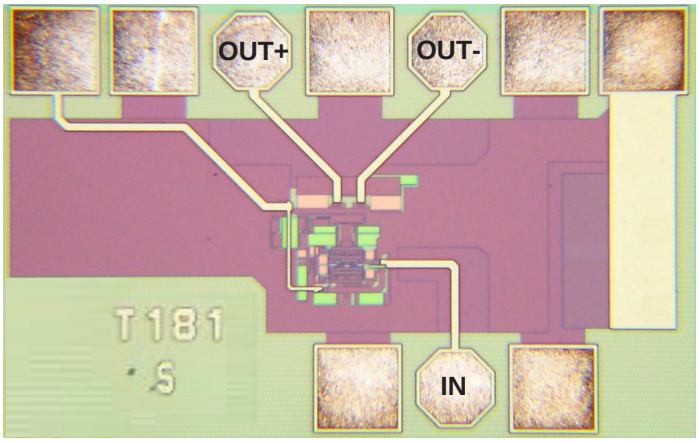

Figure 5.8: Chip photo of static frequency divide-by-2.

5.2.3 Layout

This static frequency divider is implemented in SGC25C technology and the layout (shown in Fig. 5.7) is arranged to be symmetric to ensure the same delay for the differential signals. Additionally, the lines that feed the signals

from the slave latch back to the master latch are kept as short as possible to reduce the propagation delay and guarantee the high speed. The whole layout is arranged as compact as possible. The core area is $0.2 \times 0.25\,mm^2$. Fig. 5.8 shows the chip photo. The chip area is $1 \times 1\,mm^2$ to meet the arrangement of the probe tip configuration.

5.2.4 Measurement Results and Comparison

For input frequencies lower than 60 GHz, the signal generator ROHDE&SCHWARZ SMR60 is used. For frequencies higher than 60 GHz, the signal generator SMR40 generating continuous-wave signal up to 40 GHz is connected to a multiplier by 4 which provides a single-ended high frequency sinusoidal input signal. The measurement is performed on wafer with Cascade GS-150 probe, the output can be drawn from one of differential output ports.

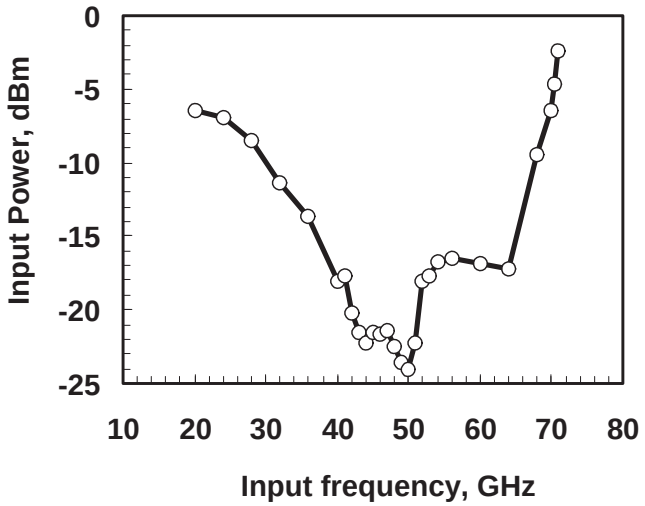

Figure 5.9: Measured input sensitivity characteristic of the static frequency divide-by-2.

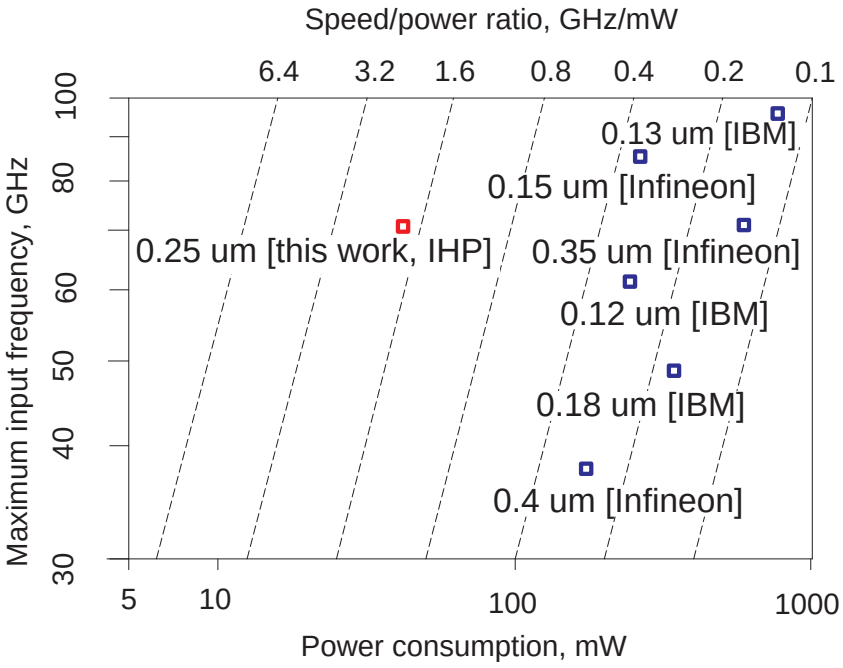

Figure 5.10: Performance comparison to the state-of-the-art of static frequency dividers with ratio 2 in SiGe technology.

With 3.5 V voltage supply, the divider core consumes 12 mA current and total current including the output buffer is 40 mA. The power of the single-ended output is -17 dBm@71.5 GHz, and -7.7 dBm@60 GHz including the loss of the cable and other connectors. Fig. 5.9 shows the minimum required power for the input frequency of the static frequency divider. A division function from 18 GHz to 71.5 GHz has been observed. The ostensible loss in sensitivity below 18 GHz is caused by the low slew rate of the input signal and will disappear for square pulses.

A 25 GHz self-oscillation at the output is observed. The maximum operating frequency is 74 GHz in the simulation, so there is a good agreement between the simulation and the measurement.

Compared with the so far reported SiGe static frequency dividers with ratio 2 in [25](Infineon), [26](IBM), [27](Infineon), [28](Infineon), and [29](IBM), with

similar technologies, the speed-to-power ratio of static frequency divider in this work [30] is much higher than the others, as shown in Fig. 5.10.

5.3 Dynamic Frequency Dividers — Analog Type and Digital Type

5.3.1 Analog Dynamic Frequency Divider — Regenerative

5.3.1.1 Principle

The principle of the regenerative dynamic frequency divider is illustrated in Fig. 5.11. It is based on a Gilbert cell mixer with a feed-back topology. By feeding the lower sideband output of an active double balanced mixer back to its input, a regenerative frequency divide-by-2 is realized.

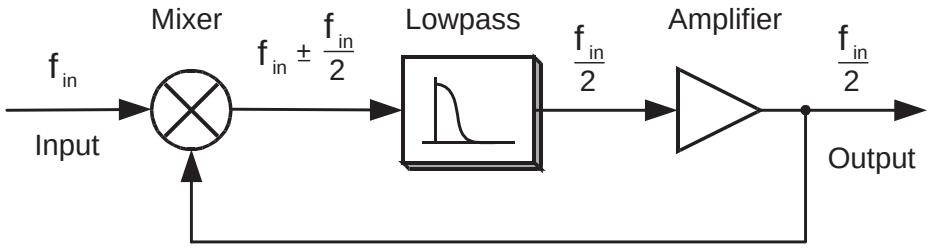

Figure 5.11: Block diagram of regenerative dynamic frequency divider.

5.3.1.2 Circuit Design

The schematic of the regenerative dynamic divider is shown in Fig. 5.12. Due to the low-pass characteristics inherent to the mixer, low-pass filter is not needed. Three stages of EFs' feed the signals into the mixer core and the

output buffer. The quad transistors of the mixer core are biased near the optimal current for f_T. The output buffer following the divider consists of an EF pair and a differential amplifier with 50 Ω load matching to the output. The circuit is designed in a differential structure, but it also can be measured and used in single-ended mode.

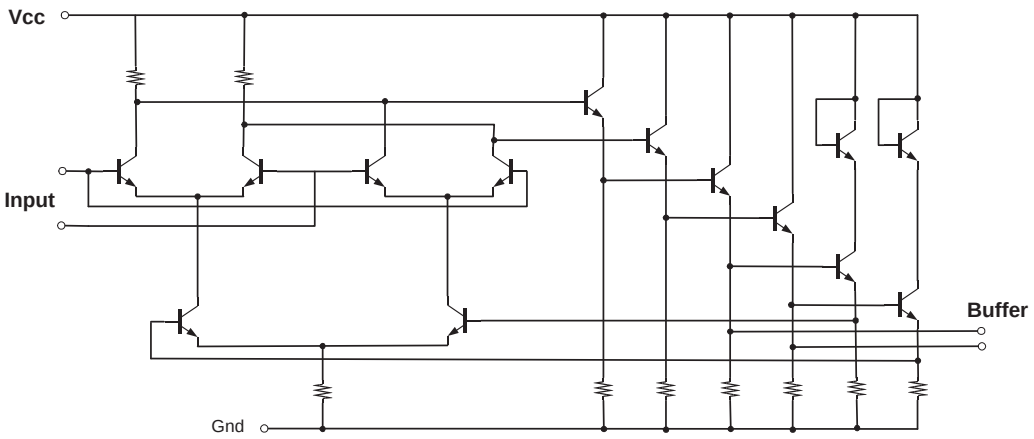

Figure 5.12: Schematic of regenerative dynamic frequency divider.

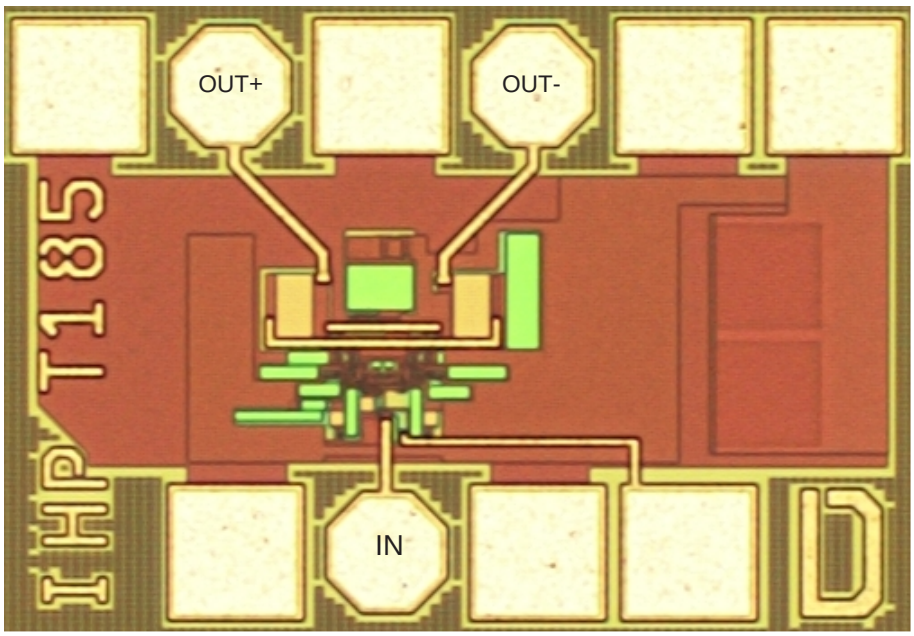

Figure 5.13: Chip photo of the regenerative dynamic frequency divider.

5.3.1.3 Layout

This regenerative dynamic frequency divider is realized in SGC25C technology and Fig. 5.13 shows the chip photo. The RF input signal is single-ended and fed to the lower side input port, and the differential outputs can be measured from the upper side output ports. The chip area is almost same as the static one, and the divider core occupies only $0.25 \times 0.2\,mm^2$. The differential transistors are arranged symmetrically, and the interconnection lines are made as short as possible to reduce the propagation delay.

5.3.1.4 Measurement Results and Comparison

The measurement is performed on wafer with Cascade GS-150 probe, the output can be drawn from one of differential output ports by simply connecting the other output port with DC blocker and 50 Ω load. For the input frequencies lower than 70 GHz, the measurement set-up is same as that for the static frequency divider. For the input frequencies higher than 70 GHz, a multiplier by 6 is connected to the SMR40 to provide the higher input frequencies. The power of the single-ended output is -2 dBm@60 GHz, and -7.3 dBm@84 GHz including the loss of the cable and other connectors. In simulation, the maximum operating frequency is up to 120 GHz. In the measurement, a 37 GHz self oscillation frequency is observed. The maximum operating frequency is measured up to 103.16 GHz as reported in [8], this value is higher than my previous report in [30] in same technology. The measurement of the speed higher than 100 GHz is mostly limited by the equipment. The measured input sensitivity curve is shown in Fig. 5.14. The output spectrum after division is shown in Fig. 5.15. This divider consumes 195 mW including the buffer with 41 mW for the divider core at 5.2 V supply voltage.

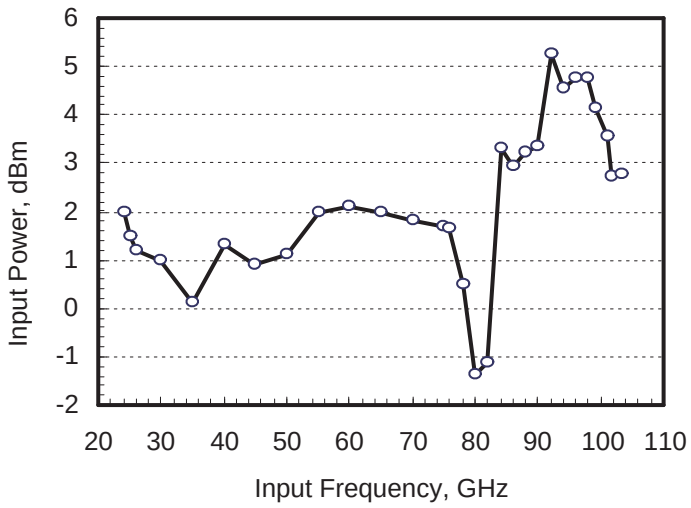

Figure 5.14: Measured input sensitivity characteristic of the regenerative dynamic frequency divider.

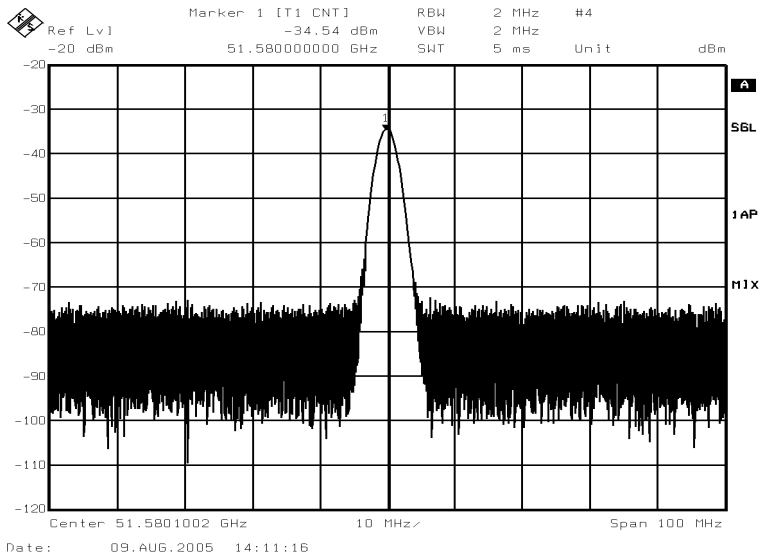

Figure 5.15: Measured output spectrum at 103.16 GHz input frequency of the regenerative dynamic frequency divider.

A summary of the latest reported analog dynamic frequency divider is listed in Table 5.2. The power consumption includes the buffer stage for all the dividers. We see that my divider in IHP's technology shows very fast speed in lower f_T than other SiGe technologies.

	[26]	[28]	This work [8]
Vcc (V)	-3.8	-4.5	3.5
Current (mA)	30	50	30
Max. Operating Freq. (GHz)	100	110	**103.16**
Technology	$0.12\,umSiGe$	$0.15\,umSiGe$	$0.25\,umSiGe$
f_T/f_{max}(GHz)	207/285	$200/n.a$	180/200
Chip Size(mm^2)	$n.a$	0.55×0.45	0.25×0.2

Table 5.2: Comparison to the state-of-the-art of SiGe regenerative dynamic frequency dividers.

5.3.2 Digital Dynamic Frequency Divider — Clocked-Inverter Feed-forward TFF

5.3.2.1 Principle

The digital dynamic frequency divider is in principle a clocked-inverter feed-forward Toggle-FF (CIFF-TFF) frequency divider, which removes the latching pairs of the Master latch and Slave latch of the static frequency divider, therefore the speed is much higher than that of Master-Slave FF [35]. The 150 GHz CIFF-TFF frequency divider in InP/InGaAs DHBT technology is reported [35] as the fastest digital dynamic frequency divider so far. I will present the result this type of frequency divider in IHP's SiGe technology.

5.3.2.2 Circuit Design

The schematic of the digital dynamic divider is shown in Fig. 5.16. Besides the removal of the latching pairs of Master and Slave latch, the collectors of emitter followers T_5 and T_6 (T_7 and T_8) are connected to the load resistors of transistor T_4 and T_3 (T_1 and T_2). Since the transient current of T_5 induces voltage drop at the collector of differential pair before T_4 turns on, thus T_4 switching is accelerated and the transition speed is increased. Therefore the total delay of the

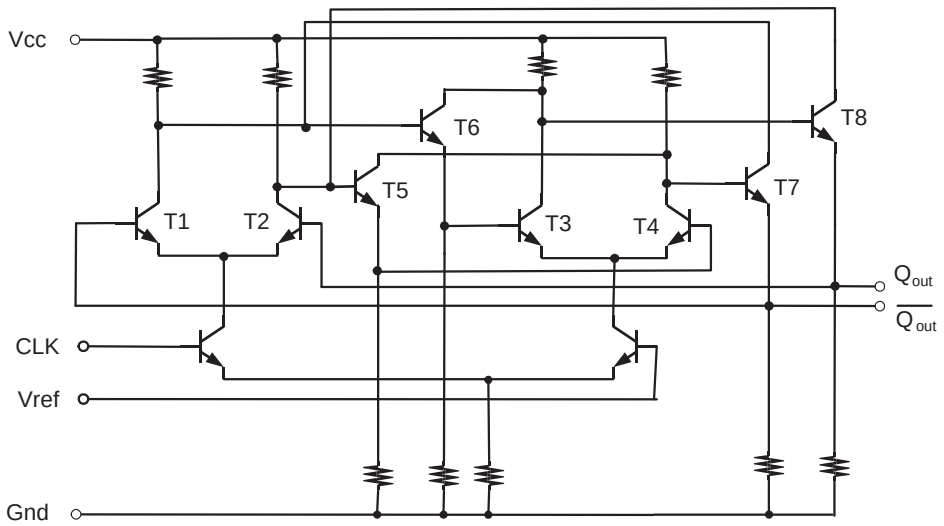

Figure 5.16: Schematic of digital dynamic frequency divider.

feedback loop is reduced and the maximum operating frequency is increased.

The output buffer design is same as that in the aforementioned divider design, which consists of an EF pair and a differential amplifier with 50 Ω load matching to the output. The circuit is designed in a differential structure, but it also can be measured and used in single-ended mode.

5.3.2.3 Layout

This digital dynamic frequency divider is implemented in SG25H1 technology and Fig. 5.17 shows the chip photo. The chip area including pads is almost same as the static one, and the divider core consumes only $0.25 \times 0.2\,mm^2$.

5.3.2.4 Measurement Results and Comparison

The measurement is performed on wafer with Cascade GS-100 probe, the output can be drawn from one of differential output ports by simply connecting the other output port with DC blocker and 50 Ω load. W-band source mod-

ule is connected to the W-band waveguide to provide the input signal to the divider input. The measured input sensitivity is shown in Fig. 5.18.

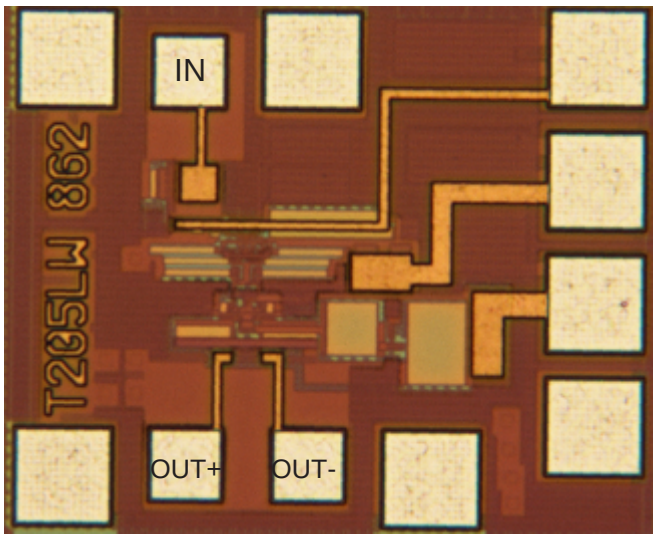

Figure 5.17: Chip photo of the digital dynamic frequency divider.

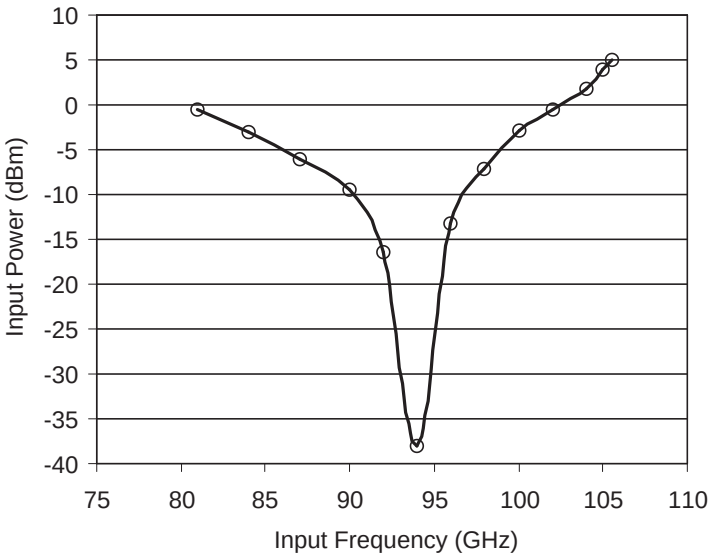

Figure 5.18: Measured input sensitivity characteristic of digital dynamic frequency divider.

In the measurement, a 47 GHz self oscillation frequency and a maximum operating frequency of 105.5 GHz are observed. In simulation, the maximum

operating frequency is about 120 GHz. The speed loss is due to the insufficient power of the source module. We see that the maximum speed is much higher than the maximum operating frequency of the static frequency divider in Fig. 5.9 and this agrees with the principle. The output spectrum after division is shown in Fig. 5.19. The divider core consumes 16.8 mA current and the whole circuit consumes 111.8 mW at 5 V supply voltage.

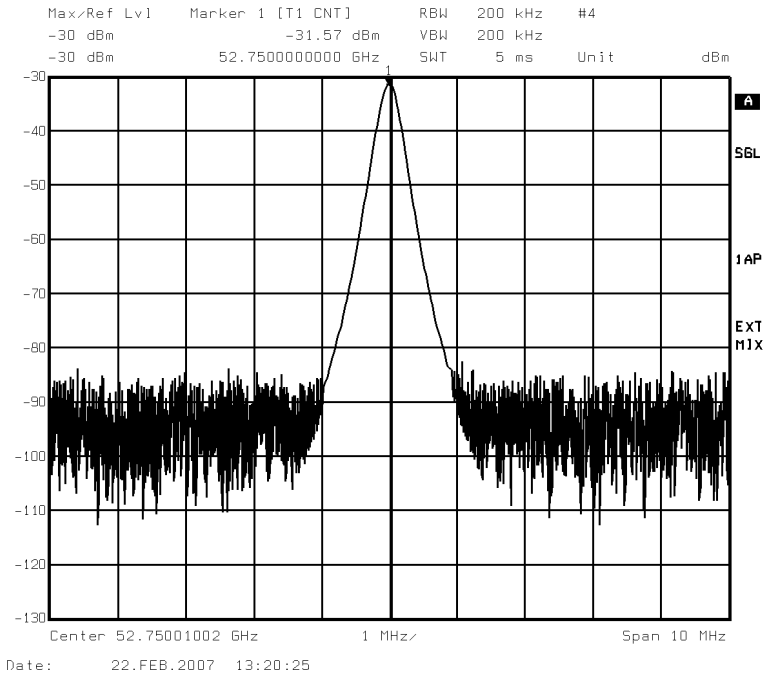

Figure 5.19: Measured output spectrum at 105.5 GHz input frequency of the digital dynamic frequency divider.

A comparison to the latest reported digital dynamic frequency dividers in GaAs technology is summarized in Table 5.4. The SiGe frequency divider in IHP's technology exhibits 100 GHz beyond maximum operating frequency compared with those in faster GaAs technologies.

	[33]	[34]	[35]	[This work]
Vcc (V)	-5.2	-5.5	5.5	5
Current (mA)	229	215	64.9	22.36
Max. f_{in} (GHz)	74	90	150	**105.5**
Technology	$0.1umGaAs$	$1umGaAs$	$0.8umGaAs$	$0.25umSiGe$
f_T/f_{max}(GHz)	$200/n.a$	150/200	245/370	180/200
Chip Size(mm^2)	2×2	0.4×2	1.5×1.5	0.25×0.2

Table 5.4: Comparison to the state-of-the-art of digital dynamic frequency dividers

5.4 Summary

In this chapter, I present the design, implementation, and successful measurement of one static and two dynamic frequency dividers. As the benchmarking circuits, the comparisons to the state-of-the-art demonstrate design techniques and the speed performance of IHP's SiGe HBT technology, which is very attractive in application of future high speed system such as 60 GHz WLAN, automotive radar system, and the optical communication systems.

The results of three types of frequency dividers realized in IHP's technology are summarized in Table 5.5. These frequency dividers demonstrate the high speed and low power consumption of the advanced SiGe:C technology and can be considered as benchmarks for the operation frequency of ultrahigh-speed IC's.

Type	Vcc	Current (mA)		Max. Speed
	(V)	divider core	total including buffer	(GHz)
Static MS-FF	3.5	12	40	71.5
Analog Dynamic	5.2	7.88	37.5	103.16
Digital Dynamic	5	16.8	22.36	105.5

Table 5.5: Summary of frequency dividers included in this work in IHP's SiGe technology

Chapter 6

Design and Implementation of Low Noise Amplifiers

In this chapter, I present the design and implementation of mmW low noise amplifiers (LNAs) in IHP's 0.25 um SiGe:C BiCMOS technology. Two LNAs are designed and measured: one for 77 GHz/79 GHz automotive radar application, the other for 1 GHz multi-band application. Firstly, the important parameters of LNA are discussed and the topologies are analyzed. Then, the circuit design is described in detail. Finally, the measurement results are compared with the state-of-the-art.

6.1 Fundamental Theory of LNA Design

6.1.1 System Requirements for LNAs

In the receiver link of most communication systems, LNA is connected to the antenna or a band selection filter after the antenna. The received signal has very low power and should be amplified by an LNA which should introduce

as little noise and distortion as possible. The following sections describe the essential parameters of LNA and how these parameters are calculated and optimized to meet the system requirements.

6.1.1.1 Sensitivity and Noise Figure

The minimum signal is determined by the sensitivity level, and should be detected with a sufficient signal quality. Typically, it is determined by the bit error rate (BER) or frame error rate (FER). This level is expressed as

$$S_{sensitivity} = -174\,dBm + 10 \cdot log(B) + \frac{S_{min}}{N_{min}} + NF, \tag{6.1}$$

where $-174\,dBm$ is the available noise power from the source at $290K$, *i.e.* kT, B is the channel bandwidth, S_{min}/N_{min} is the minimal signal-to-noise ratio required for acceptable BER, and NF is the noise figure of the receiver. Then we get the maximum allowable noise figure of the receiver from equation (6.1)

$$NF = S_{sensitivity} + 174\,dBm - 10 \cdot log(B) - \frac{S_{min}}{N_{min}}. \tag{6.2}$$

The NF of the receiver describes how much the receiver degrades the signal-to-noise ratio of the signal received. It is defined as

$$NF = 10 \cdot log\{\frac{S_{in}}{N_{in}} / \frac{S_{out}}{N_{out}}\}, \tag{6.3}$$

where S_{in}, S_{out}, N_{in}, and N_{out} are the signal and noise powers at the input and output of the receiver, respectively. The noise figure of cascaded blocks can be calculated by using different methods. Friis' formula is a traditional approach,

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \cdots \frac{F_n - 1}{G_1 \cdots G_{n-1}}, \tag{6.4}$$

$$NF_{tot} = 10 \cdot log(F_{tot}), \tag{6.5}$$

where F_n and G_n are the noise factor and available gain of the n_{th} block, respectively. Friis' formula shows that the noise contribution of each block after the first block is reduced if the gain of the preceding stage is increased. The most noise dominant block is the first of all blocks. LNA as the first stage of the receiver, the noise figure and gain are both so important that both should be designed to be optimal. The NF requirement for 77 GHz receiver is 16 dB [4]. In implementation of the LNA design, the design margin of at least 1 dB should be left.

6.1.1.2 Gain and Noise Matching

A two-port network shown in Fig. 6.1 is always adopted in analysis. The signal transmission is understood as voltage waves. The reflection coefficient is the ratio between the reflected voltage wave from a port and the incident voltage wave entering the port, and is defined by equation (6.6):

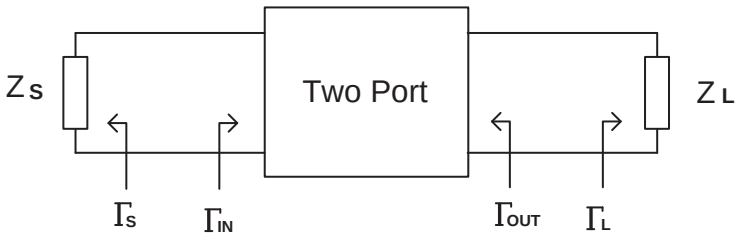

Figure 6.1: Two-port network reflection coefficients.

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \tag{6.6}$$

where Z_0 is a reference impedance, normally as 50 Ω. When the characteristic impedance at the interface of two ports are different, a reflection wave occurs.

Only when the port impedance Z is equal to Z_0, no reflection wave occurs at the port interface, the input power is fully transferred into the port.

When considering the gain of a two-port, we need to know the definitions for the power gains:

G_T is the transducer power gain, and is probably the most meaningful gain metric:

$$G_T = \frac{P_L}{P_{AVS}}, \tag{6.7}$$

where P_L and P_{AVS} are the power transferred to the load and power available from the source respectively.

G_P is the power gain, and refers to the power that is delivered to the load from the power input to the network:

$$G_P = \frac{P_L}{P_{IN}}. \tag{6.8}$$

G_A is the available power gain, and represents the power available from the network given the power available from the source:

$$G_A = \frac{P_{AVN}}{P_{AVS}}. \tag{6.9}$$

From these definitions, we could notice that the relation among them, i.e. $G_T \leq G_P$ and $G_T \leq G_A$. Only when the source and load are both conjugate matched to the input and output impedance of the two-port network, we get $G_T = G_P = G_A$. Therefore in the LNA design, the inter-stage matching for gain stage should be conjugate matched in order to achieve maximum power gain.

Besides the gain issue of LNA, noise figure of LNA is also very important be-

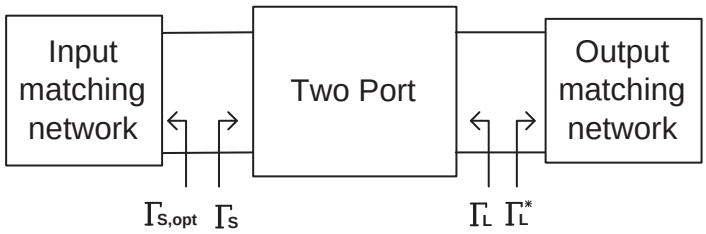

Figure 6.2: Noise matching and conjugate gain matching of a two-port network.

cause it contributes the most part of the noise figure of the total receiver in equation (6.4). Similarly, for multi-stage LNA, the first stage is the most important stage for both noise and gain optimization. A good matching for LNA means a minimum noise figure, maximum gain, and acceptable return loss. Conflicts are very often met for the same input matching network. Therefore, the input matching of the first stage should ideally achieve simultaneous gain and noise match by achieving $\Gamma_S = \Gamma_{S,opt}$ as depicted in Fig. 6.2, where Γ_S and $\Gamma_{S,opt}$ are the reflection coefficient for input port and reflection coefficient for optimum noise reflection, respectively. For the other stages, gain matching can be employed to achieve the maximum power transfer.

Equation (6.10) describes the noise figure of the two-port network by the related parameters. F_{min} is the minimum noise figure which can be achieved. Therefore it is easily seen that in order to achieve the minimal noise figure F, Γ_S should be optimized to be equal to $\Gamma_{S,opt}$, this is what we called noise matching.

$$F = F_{min} + \frac{4 \cdot R_n \cdot \mid \Gamma_S - \Gamma_{S,opt} \mid^2}{(1 - \mid \Gamma_S \mid^2) \cdot \mid 1 + \Gamma_{S,opt} \mid^2} \tag{6.10}$$

For HBT devices, the F_{min} can be expressed as equation (6.11) [36]. F_{min} is dependent on the technology parameters f_T, β, R_b, and the current related

parameters like β and I_c, while R_b is related to the transistor selection.

$$F_{min} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T} \cdot \sqrt{\frac{I_c}{2V_T} \cdot (R_E + R_b) \cdot (1 + \frac{f_T^2}{\beta f^2}) + \frac{f_T^2}{4\beta f^2}} \tag{6.11}$$

6.1.1.3 Stability Issue

Stability is a very important issue for amplifiers. To avoid oscillation, the stability should be guaranteed during the whole design process. A common definition for stability factor is *Rollet's stability condition* [37] expressed as

$$k = \frac{1 - \mid S_{11} \mid^2 - \mid S_{22} \mid^2 + \mid S_{11}S_{22} - S_{12}S_{21} \mid^2}{2 \mid S_{12}S_{21} \mid} > 1 \tag{6.12}$$

and

$$\mid \Delta \mid = \mid S_{11}S_{22} - S_{12}S_{21} \mid < 1 \tag{6.13}$$

To fulfill an unconditional stability, the necessary and sufficient conditions are the combination of equation (6.12) and either equation (6.13) or stability measure defined in [38] as:

$$b = 1 + \mid S_{11} \mid^2 - \mid S_{22} \mid^2 - \mid S_{11}S_{22} - S_{12}S_{21} \mid^2 > 0. \tag{6.14}$$

Another μ factor [39] is also very often used to check the stability of LNA. μ is defined as

$$\mu = \frac{1 - \mid S_{11} \mid^2}{\mid S_{22} - (S_{11}S_{22} - S_{12}S_{21})S_{11}^* \mid + \mid S_{12}S_{21} \mid} > 1. \tag{6.15}$$

The circuit is unconditional stable when $\mu > 1$. This measure is the distance of the Smith chart to the nearest stability circle, the larger the μ value, the more stable the circuit. The stability of the LNA circuit in this work is checked

from DC to 110 GHz in both simulation and measurement.

6.1.1.4 Linearity

The output power of an amplifier increases linearly with the input power in the case of small signal excitation, in this case, the amplifier can be treated as a linear circuit. While 1 dB gain compression point and $3^{rd} - order$ intercept point are commonly characterized as the limits of the linear operation region.

Due to the nonlinear behavior, harmonics and mixing products occur at the output of the device, a non-linear transfer function can be approximated as a Taylor series expansion:

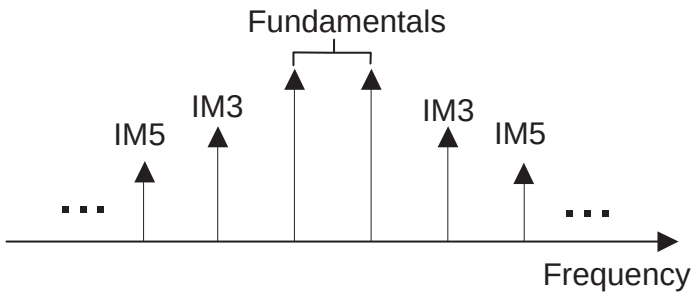

Figure 6.3: Output spectrum of a two-tone excitation for a non-linear amplifier.

$$V_{out}(x) = k_0 + k_1 \cdot V_{in}(x) + k_2 \cdot V_{in}^2(x) + k_3 \cdot V_{in}^3(x) + \cdots \tag{6.16}$$

We assume $V_{in}(t) = V \cdot [sin(\omega_1 t) + sin(\omega_2 t)]$, then the mixing products appear at the device output at signal frequencies of $2\omega_1$, $2\omega_2$, $3\omega_1$, $3\omega_2$, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, $\omega_1 \pm 2\omega_2$, $\cdots$ Harmonics and even-order mixing products are easily filtered out, so these will not cause problems. The most troublesome terms are the $3^{rd} - order$ inter-modulation at $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$ and the $5^{th} - order$ inter-modulation at $3\omega_1 - 2\omega_2$, $2\omega_2 - 3\omega_1$. The spectrum is shown in Fig. (6.3). The

graph in Fig. (6.4) shows the relation between the fundamental tone and the $3^{rd} - order$ tone, the curves go to saturation with larger input, therefore they don't intersect. However, the intersection point can be found if we extrapolate the linear part of the curves. This theoretical intersection point is called IP_3, the power corresponding to the input and output are defined as $3^{rd} - order$ input intercept point (IIP_3) and $3^{rd} - order$ output intercept point (OIP_3) respectively. The definition for $5^{th} - order$ is same as the above. If ω_1 is close to ω_2, then $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are very close to the signal frequencies and are troublesome.

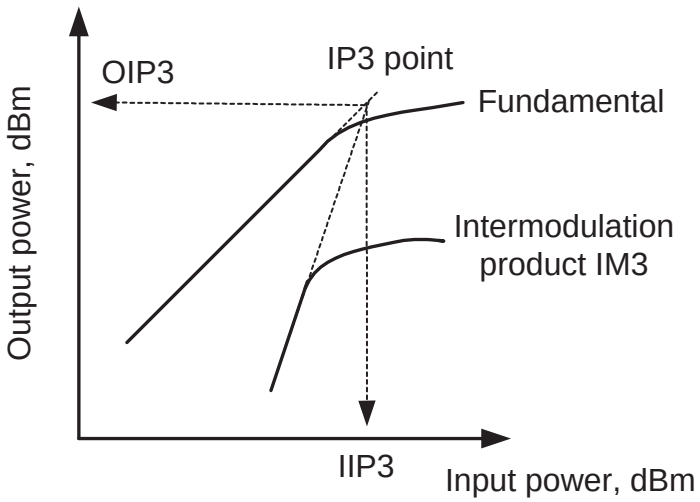

Figure 6.4: Definition of the third-order intercept point (IP3).

For small signals the fundamental tone increases linearly by 20 dB/decade, and the inter-modulation products of $3^{rd} - order$ increases as the cube of the input by 60 dB/decade. Therefore at the $3^{rd} - order$ intercept point, we have this relation:

$$\frac{k_1 \cdot V}{0.75 \cdot \mid k_3 \mid \cdot V^3} = 1 \tag{6.17}$$

where k_1 and k_3 are constants in equation (6.16).

When $V = V_{IP3}$, we get

$$V_{IP3} = 2 \cdot \sqrt{\frac{k_1}{3 \cdot \mid k_3 \mid}} \tag{6.18}$$

where V_{IP3} is the input voltage at the $3^{rd} - order$ intercept point.

6.1.1.5 Figure of Merit

The overall performance of an LNA can be judged by means of a figure-of-merit (FOM) which is defined as [40]:

$$FOM = \frac{G_{max} \cdot BW}{(NF_{avg} - 1) \cdot P_{diss}}, \tag{6.19}$$

where G_{max} and NF_{avg} are the maximum gain and average noise figure, and both are in absolute values and not in dB, BW is the covered 3 dB bandwidth, and P_{diss} is the dissipated DC power by LNA. Because this FOM takes into account the very important parameters such as gain, bandwidth, noise figure, and power consumption, so it is adopted in the comparison to the measurement results of state-of-the-art.

6.2 77 GHz/79 GHz LNA

6.2.1 Circuit Design

6.2.1.1 Topologies

There are basically three structures which can be adopted in LNA design: common emitter (CE), common base (CB), and cascode structure. The structures are shown in Fig. (6.5). Due to the small signal transmission mode in LNA, the small signal equivalent circuit is used to analyze the characteristics of

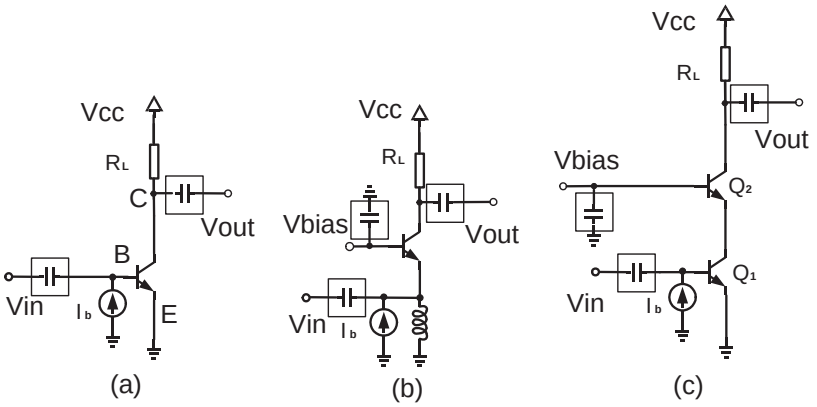

Figure 6.5: Topologies of LNA circuit: (a) Common emitter, (b) Common base, (c) Cascode structure.

these structures. The corresponding small signal equivalent circuits are shown in Fig. 6.6, Fig. 6.7, and Fig. 6.8 respectively.

In Fig. 6.6, the equivalent circuit of the CE transistor is marked in the dashed block. To analyze the gain performance of the CE transistor, we use Kirchhoff's law at the collector output node C, because r_{ce} is much larger than R_L, so r_{ce} is neglected in current analysis. We have:

$$(V_{out} - V_{be}) \cdot j\omega C_{bc} + g_m \cdot V_{be} + V_{out}/R_L = 0, \tag{6.20}$$

from which the voltage gain can be derived by:

$$G(j\omega) = \frac{V_{out}}{V_{be}} = -g_m R_L \cdot \frac{1 - j\omega(C_{bc}/g_m)}{1 + j\omega C_{bc} R_L}. \tag{6.21}$$

Then we know that for low frequencies the voltage gain is close to $G(\omega \to 0) = -g_m R_L$. Because

$$i_{bc} = (V_{be} - V_{out}) \cdot j\omega C_{bc}, \tag{6.22}$$

by putting equation (6.21) into equation (6.22), we have

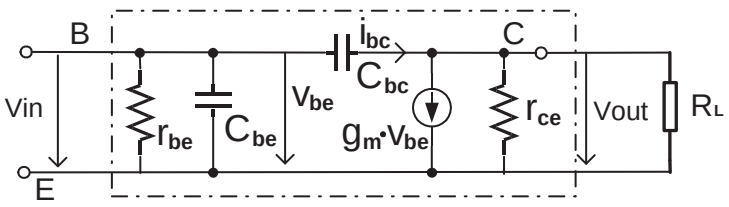

Figure 6.6: Small-signal equivalent circuit of CE structure.

$$i_{bc} = \underbrace{(1 - G(j\omega)) \cdot j\omega C_{bc}} \cdot V_{be}. \tag{6.23}$$

In equation (6.23), the part in bracket can be treated as a new capacitance C_M,

$$C_M = (1 - G(j\omega)) \cdot C_{bc} \tag{6.24}$$

At lower frequencies,

$$C_M \approx (1 + g_m R_L) \cdot C_{bc}. \tag{6.25}$$

This is the so-called Miller Capacitance, which has an amplification factor $(1 + g_m R_L)$ for C_{bc}. This means from node B looking into the circuit, the capacitance C_M is connected in parallel with C_{be} to ground, this capacitance decreases the gain at higher frequencies significantly.

The equivalent circuit of CB structure is shown in Fig. 6.7. Since $i_c \approx i_e$, for the case of same input and output impedance, this configuration provides almost no voltage gain. While it offers three advantages over CE structure: higher linearity, easier input matching due to the smaller input impedance, and larger reverse isolation due to quite large r_{ce} between the input port and the output port.

Cascode structure includes one CE and one CB transistor, the equivalent circuit is shown in Fig. 6.8. Because $g_{m2} \approx g_{m1}$, and input impedance of the CB

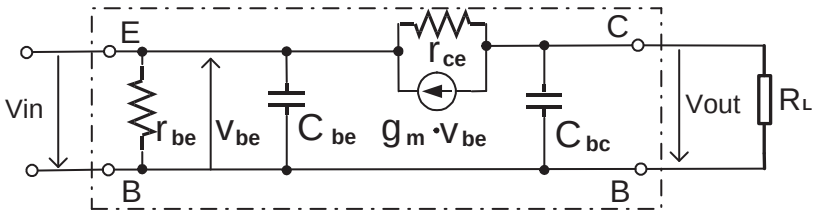

Figure 6.7: Small-signal equivalent circuit of CB structure.

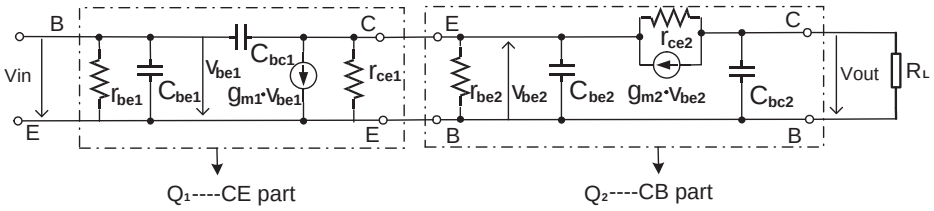

Figure 6.8: Small-signal equivalent circuit of cascode structure.

stage ($\approx \frac{1}{g_{m2}}$) which is usually smaller than the load impedance, is the load of the CE stage, therefore from equation (6.25), we get C_M for cascode structure:

$$C_M \approx 2 \cdot C_{bc1} \tag{6.26}$$

By comparing equation (6.25) and (6.26), we know that the cascode transistor reduces the Miller effect of the input CE transistor. Additionally, the cascode transistor increases the separation between the input and output ports of the cascode amplifier compared to a single CE amplifier. This cascode topology has significant improvement on the performance of the reverse isolation. The improved isolation decreases the LO leakage to the input port of LNA and is beneficial to the system.

For LNA design at mmW frequency range, it is very necessary to select a structure which is robust enough to meet the gain and matching requirements. Cascode structure shows better robustness, therefore it is selected in my design. Of course, since it includes more transistors than other structures, thus more noise contributors are included, so the drawback is the slightly increased noise

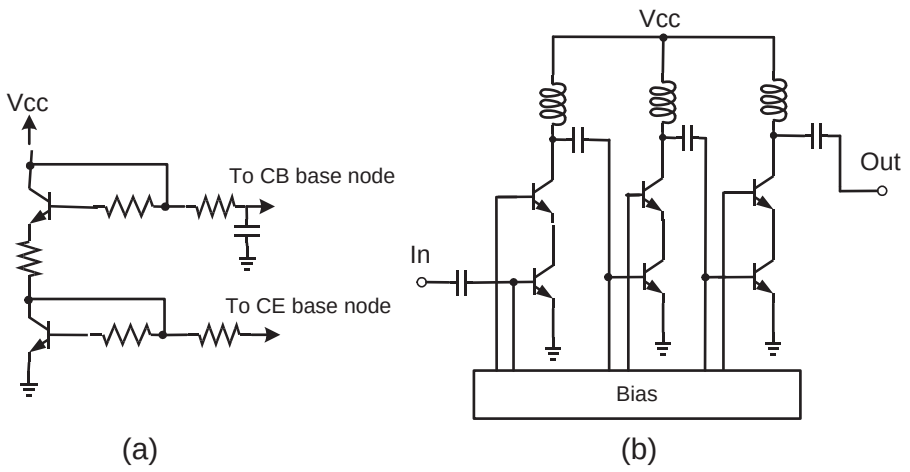

Figure 6.9: Schematic of: (a) Bias network for one-stage LNA, (b) single-ended three-stage cascode LNA.

figure.

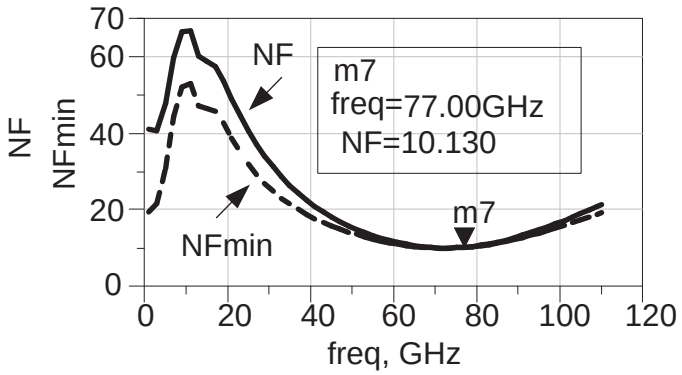

Figure 6.10: Noise figure optimization in frequency range from 77 GHz to 79 GHz .

6.2.1.2 Design and Optimization

Based on the advantages and disadvantages discussed in Section 6.2.1.1, I employ the cascode topology to realize an LNA in W-band at 77 GHz and 79 GHz. I adopt the single-ended structure and realize a single-ended receiver with lower power consumption and less chip area. The bias circuit shown in Fig. 6.9 (a) is the mirrored cascode current source, and Fig. 6.9 (b) shows

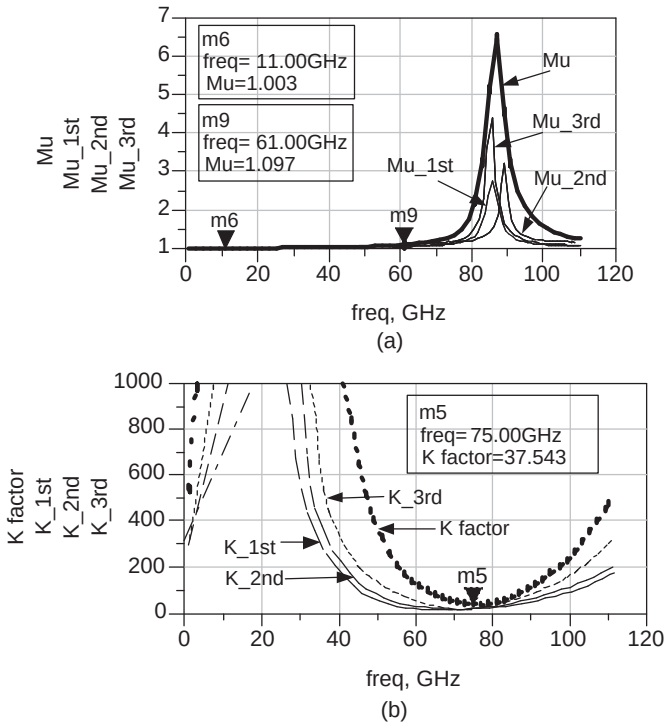

Figure 6.11: Stability analysis in simulation: (a) Mu factor, (b) K factor.

the single-ended three-stage cascode amplifier. MIM capacitors not only act as DC blockers at the input, output, and inter-stages, but also construct the matching network. Microstrip lines are used in the inductive load of each stage and the other matching networks. The probe pad is modeled as a capacitor in simulation with top metal and bottom metal as two plates.

For each individual stage of the LNA and the whole LNA circuit, the stability is checked and guaranteed by simulating the Mu factor and K factor. Mu factor is larger than 1 and K factor is larger than 0 for frequency ranging from 0.1 GHz to 110 GHz (Fig. 6.11). The stability factor is also guaranteed in simulation in temperature variation range from -40 degree to 125 degree in Fig. 6.12.

The optimization of the input port impedance for the first stage of LNA takes both the noise and power match into consideration, so that the minimum noise

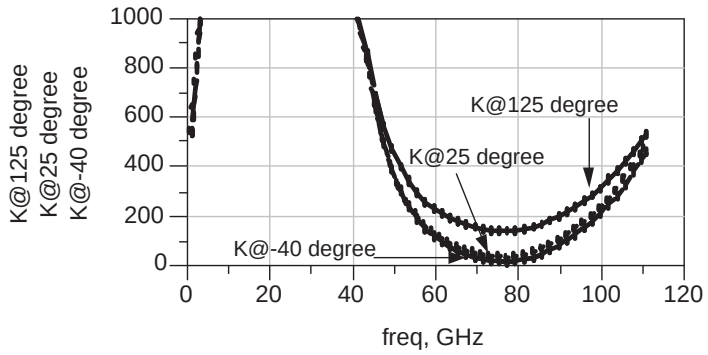

Figure 6.12: LNA's K factor versus temperature in simulation.

figure (Fig 6.10) and maximum power transfer can be achieved simultaneously. Fig. 6.13 shows that the input port impedance is matched to 50 Ω and the optimum noise source impedance is also very close to 50 Ω between 77 GHz and 79 GHz frequency range.

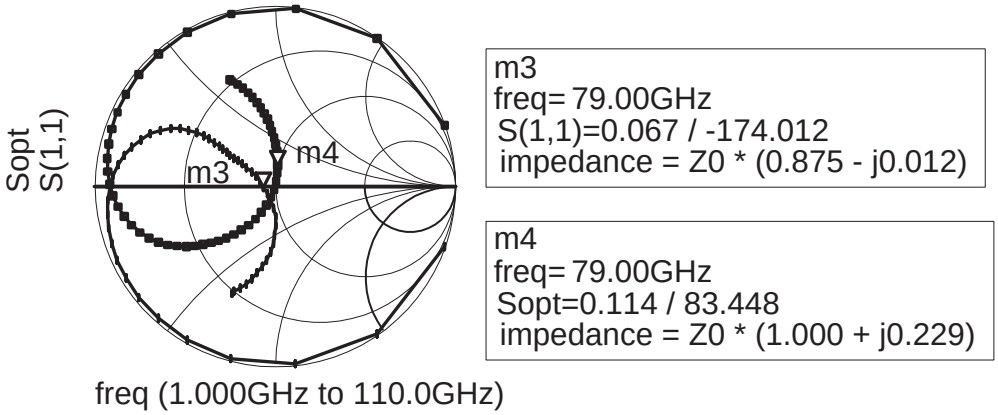

Figure 6.13: Optimization of input impedance for power and noise match.

Since this LNA is designed to operate at very high frequencies, so small parasitic effects introduced in the layout are also considered in the circuit optimization. Therefore we include the additional layout effects in simulation to compensate the unexpected difference between simulation and measurement. The simulation results of S-parameter are compared with the measurement results in Fig. 6.15

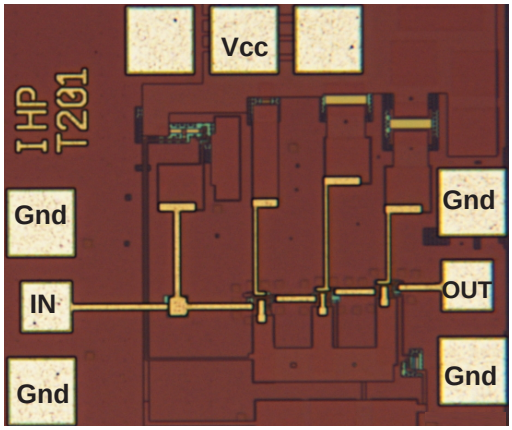

Figure 6.14: Chip photo of 77 GHz/79 GHz LNA.

6.2.2 Layout

The chip photo of 77 GHz/79 GHz LNA is shown in Fig. 6.14. It occupies $0.6 \times 0.5\,mm^2$ including pads, and $0.42 \times 0.42\,mm^2$ without pads. RF input signal is fed to the Ground-Signal-Ground (GSG) pad from left, the output signal is obtained from the GSG pad on the right, only one voltage supply is needed and fed from the top pad. All the probe pitch is 100 μm.

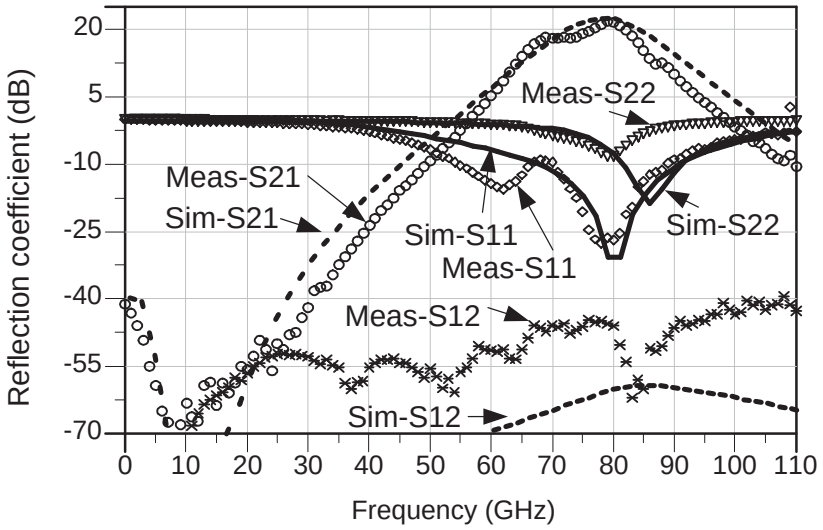

Figure 6.15: Measurement and simulation S-parameter results of 77 GHz/79 GHz LNA.

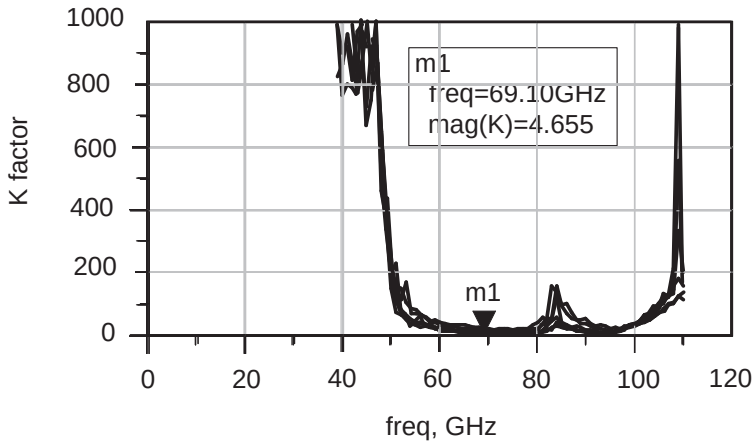

Figure 6.16: Measured K factor of 77-79 GHz LNA at 27, 50, 70, 85, 100, 125 degrees.

6.2.3 Measurement Results

6.2.3.1 S-parameter

The LNA is measured on wafer with DC-110 GHz S-parameter equipment, and is unconditionally stable in the whole frequency range. The LNA is designed to provide peak gain in the frequency range between 77 GHz and 79 GHz to meet the future automotive radar applications. The input matching and output matching of each stage are optimized to cover 77 GHz and 79 GHz. The on-wafer measured S-parameter results are compared with the simulation results in Fig. 6.15, this result [7] shows improvement of in-band gain over my previous work reported in [6], which showed 3 dB gain ripple between 77 GHz and 79 GHz. In this work, the measured peak gain S_{21} is 21.7 dB at 79 GHz and 20 dB at 77 GHz, 1 dB gain ripple is between 77 GHz and 81 GHz, and 3 dB bandwidth is from 74 GHz to 83 GHz. S_{11} and S_{22} measurement results show that good input and output port impedance match are achieved at 77 GHz and 79 GHz. Additionally, port isolation S_{12} is better than 45 dB in this range.

The LNA is also measured on wafer in available temperature variation range between 27 and 125 degree. The measured K factor extrapolated from the measured S parameter by 6.12 and 6.13 versus temperature (Fig. 6.16) shows the unconditional stability from DC to 110 GHz. The LNA's gain varies from 21.7 dB@27 degree to 11.3 dB@125 degree and works stably (Fig. 6.17).

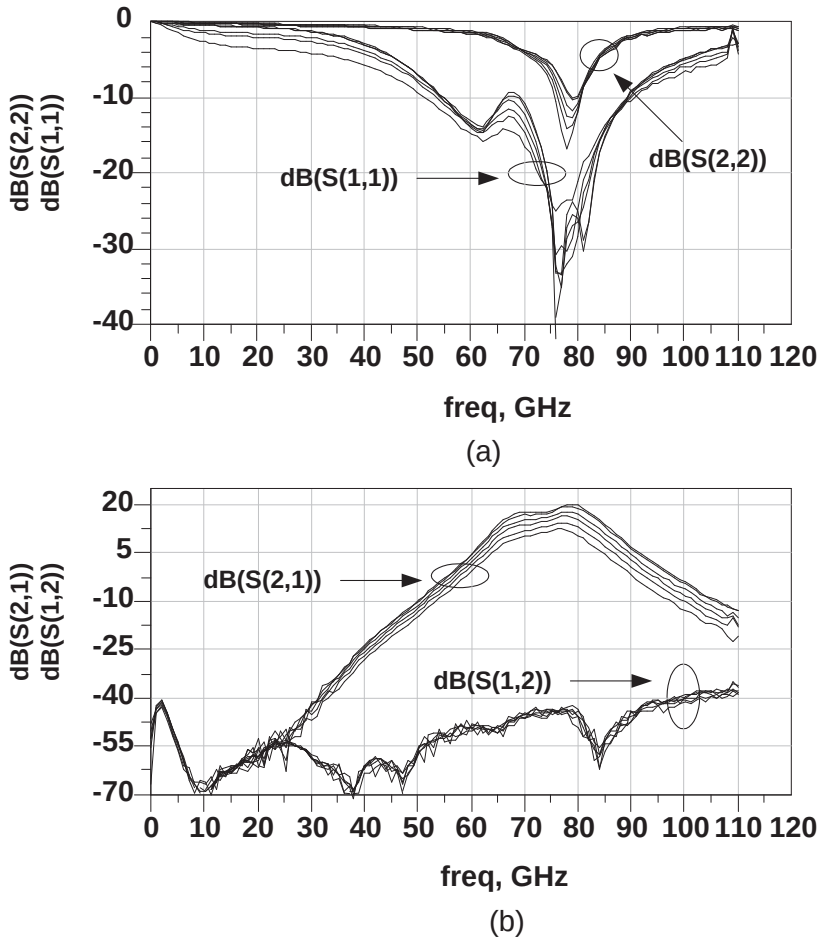

Figure 6.17: Measured S-parameter of 77-79 GHz LNA at 27, 50, 70, 85, 100, 125 degrees: (a) S_{11} and S_{22}, (b) S_{21} and S_{12}

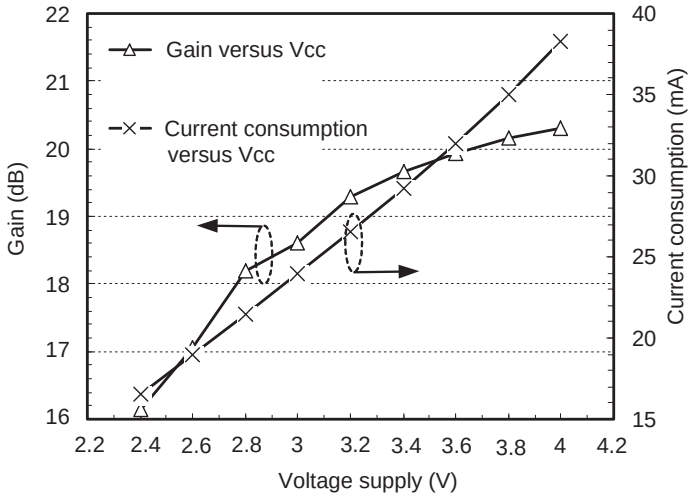

Figure 6.18: Measured Gain and current consumption versus voltage supply for 77 GHz/79 GHz LNA.

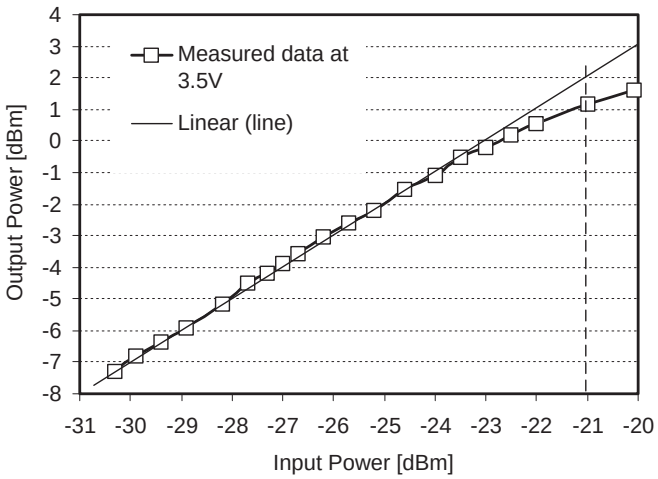

Figure 6.19: Measured linearity performance of 77 GHz/79 GHz LNA at 3.5 V voltage supply.

6.2.3.2 Linearity

Additionally, the measurements for gain and current consumption versus supply voltage are investigated and the results are shown in Fig. 6.18. The gain increases less when the supply voltage is larger than 3.5 V, therefore the whole measurement is done at 3.5 V. The current consumption is proportional to

the supply voltage. The linearity of the LNA is also measured by single-tone set-up. E-band source module and W-band power sensor are used. The linearity performance is illustrated in Fig. 6.19. The LNA works linearly when the input power is below -21 dBm, which is the 1 dB gain compression point of this LNA.

Due to the limitation of equipment, the measurement of the noise figure was not performed. Based on the comparison between S-parameter simulation and measurement results, we estimate that the noise figure of the LNA should be about 10.1 dB.

	[41]	[42]	[43]	This work [7]
Stage	3-stage	3-stage	2-stage	3-stage
Type of LNA	single-ended	single-ended	differential	single-ended
Vcc (V)	3	2	3.5	3.5
Current (mA)	30	19.2	25	30
Gain_max (dB)	10	15	23.8	21.7
NF (dB)	4	3.5	8	10.1
BW (GHz)	8	10	6	9
Isolation (dB)	-	-	-	-45
Technology	$0.15\,umGaAs$	$0.19\,umGaAs$	$0.12\,umSiGe$	$0.25\,umSiGe$
f_T/f_{max}(GHz)	$80/n.a$	$n.a/n.a$	207/285	180/200
Chip Size(mm^2)	1.34×1.0	1.88×1.20	0.86×0.36	0.42×0.42
FOM	0.58	6.65	2.21	1.38

Table 6.2: Comparison of FOM of 77 GHz/79 GHz LNAs.

6.2.4 Comparison to the State-of-the-art

The FOM in equation (6.19) [40] is used to compare this work with the other latest reported 77 GHz/79 GHz LNAs so far. In Table 6.2, the technical data is summarized for SiGe and GaAs LNAs and the FOMs are compared. This is the first reported single-ended cascode LNA in SiGe technology at 77 GHz/79 GHz at the time of publication of [6]. The LNA shows better FOM than some in

GaAs technology, and shows comparable FOM compared with other in more advanced SiGe technology. The performance of the LNA can still be improved with the progress of the more advanced technology of IHP. The measurement results and comparison show that our component is a promising alternative in the future SiGe radar products.

6.3 Tunable 0.7 GHz - 1.4 GHz LNA

6.3.1 Motivation — Multi-band Applications

With the remarkable growth of the wireless communications, personal communications systems, and WLANs' are realized with the monolithic integrated circuit in both licensed and unlicensed bands.

Due to the lack of universal standards for different signal transmission mode (analog or digital), users either need to switch among different bands (in multi-band cellular phones) or use multiple frequency modes (multi-band cellular phone with global position system and Blue-tooth interface). Therefore, it would be highly beneficial to provide a receiver which has variable or multiple frequency bands.

Although the reported micro electromechanical system (MEMS) technology is also compatible with integrated circuits (IC) process, it is expensive, and it requires large voltage supply, so it is more suitable for special applications like high-resolution imaging of human eye or other measurements.

Another proposed structure is a dual-band receiver. This structure adopts a dual-band antenna, dual-band filter, and dual-band LNA which are matched to the designated frequency bands. This concurrent multi-band receiver design

is very useful for supplying redundancy in mission critical data transmission application. For different bands, the receiver system needs to provide multi-band antennas, and multi-band filters simultaneously. Focusing on the multi-band LNA, multiple resonators for the targeted frequency bands are needed at the input and output. This requires multiple inductors on chip, thus larger chip area. Further, due to the simultaneous amplification of the received signals of different bands and the non-linearity of the transistor in the wide-band LNA, the non-linearity would put forward a high phase noise requirement for the voltage controlled oscillator (VCO), and the non-linearity after the mixer and introduces bottlenecks in system performance. Additionally, various techniques like using switched inductors [44] and switched capacitors [45]-[46] all require additional passive elements in the matching networks. This increases the chip area and cost. Thus, a variable single or multi-band functionality using small chip area and with good linearity performance is preferred.

This work [47] presents a variable single or multi-band amplifier architecture which can be applied in a certain frequency range with variable operating frequencies.

6.3.2 Circuit Design

The schematic shown in Fig. 6.20 adopts the cascode topology. The noise match, power match, and the stability issues are in principle same as those in Section 6.2.1. By comprising a varactor C_V in the network of the input, the output, or both in an LNA, the impedance is matched to the designated frequency band. In specific circuit design, it can be flexibly selected. In this circuit, the input match does not include the varactor and the circuit provides a wide band input impedance matching, while the output load provides a

variable band output impedance matching. The resonant gain can be adjusted to operate at the expected frequency band by tuning the control voltage V_{ctrl} after the chip fabrication. The bias circuit is similar as that used in Fig. 6.9. The four inductors are fully integrated on chip without using off-chip inductors or bond wires to reduce the chip size and increase the accuracy. By adjusting the capacitance of the varactor in the resonant load matching network, this method can be applied in variable band amplifier, in LNA or mixer for one single frequency band or multiple bands. In principle, compared with adopting the general wide-band LNA in multi-band applications, this band selective structure provides better non-linearity performance after the mixer, improves the dynamic range of the receiver, and relaxes the phase noise requirement for the VCO.

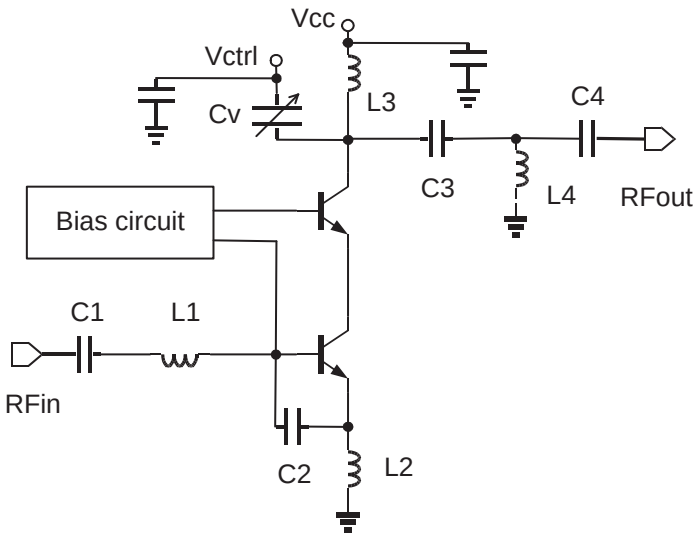

Figure 6.20: Schematic of single-ended one-stage variable band LNA in cascode structure.

6.3.3 Layout

This LNA is designed and implemented with the SG25H1 technology which provides five metal layers and same active devices as SGC25C technology. The chip photo of LNA is shown in Fig. 6.21. The chip occupies $1.3\times0.9\,mm^2$ area including pads.

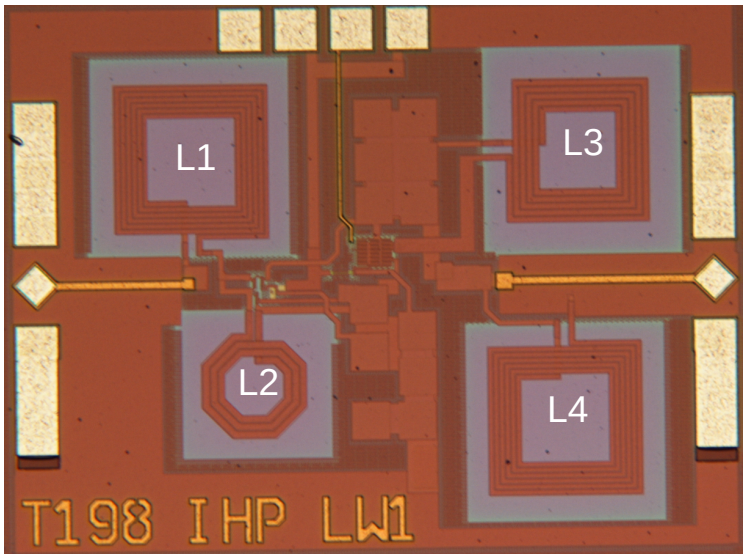

Figure 6.21: Chip photo of 0.7 GHz-1.4 GHz tunable LNA.

6.3.4 Measurement Results

6.3.4.1 S-parameter

All the measurements are performed on wafer using $100\,\mu m$ pitch probes. The LNA consumes 17.5 mW with 2.5 V DC supply voltage. By sweeping the control voltage V_{ctrl} from 0 V to 5 V, we observe the operation band of the LNA is changed from 1.4 GHz to 0.7 GHz (shown in Fig. 6.22).

The measured tuning range is shown in the gain curve S_{21} in Fig. 6.22 (a), S_{21}, S_{11}, and S_{22} in the S-parameter measurement agree with the results in simulation very well. The port isolation S_{12} between the input and output is

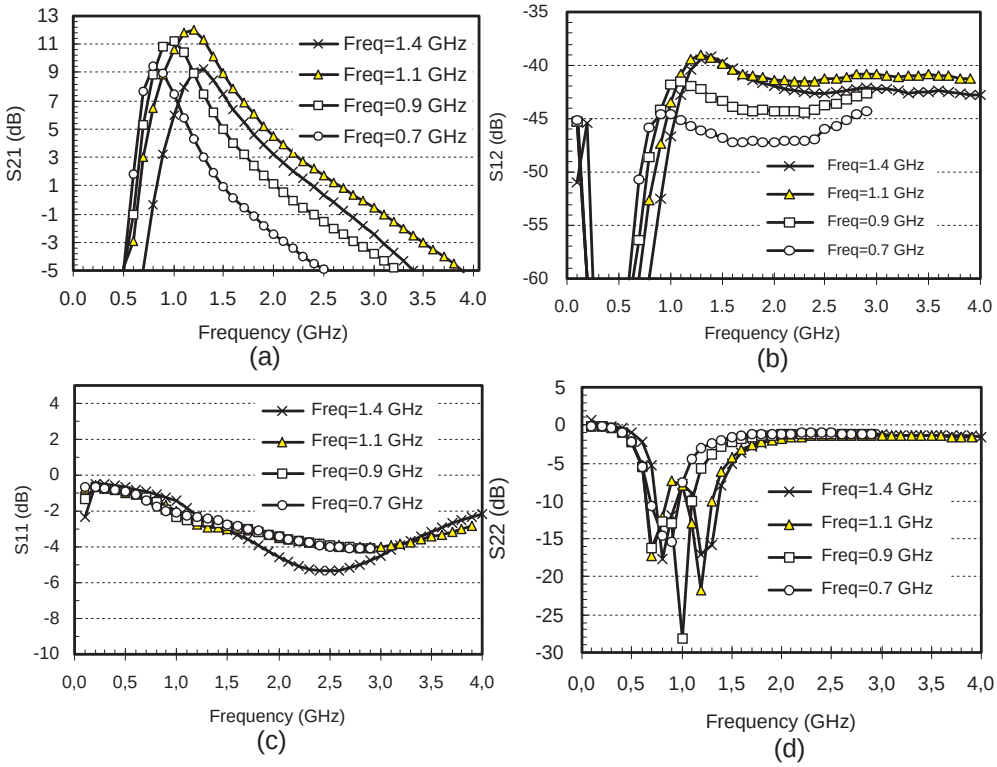

Figure 6.22: On-wafer measurement of S-parameter in dB: (a) S_{21}, (b) S_{12}, (c) S_{11}, (d) S_{22}.

higher than 40 dB due to the adoption of cascode topology. Its bandwidth covers the mobile and GPS frequency band. In system design, thess control voltages can be fed from the processor and memory which relates to the voltage controlled oscillator's frequency for multi-band system.

6.3.4.2 Noise Figure

The simulated and measured noise figures of the LNA are shown in Fig. 6.23. We observe that the measured noise figure is about 2 dB larger than the simulated result. The gain in S-parameter measurement is also about 2 dB larger than that in single-tone measurement. The reason is related to the path calibration of between the two different measurement set-up. The noise figure does not change with the control voltage during the measurement observation.

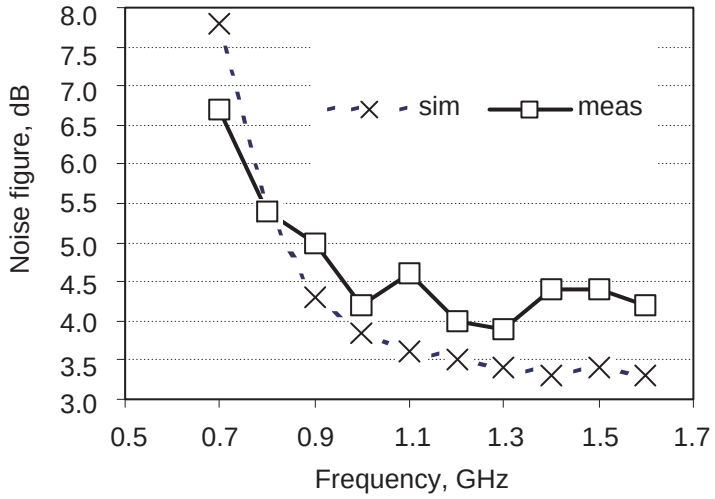

Figure 6.23: Simulation and measurement results of NF of 0.7 GHz-1.4 GHz tunable LNA.

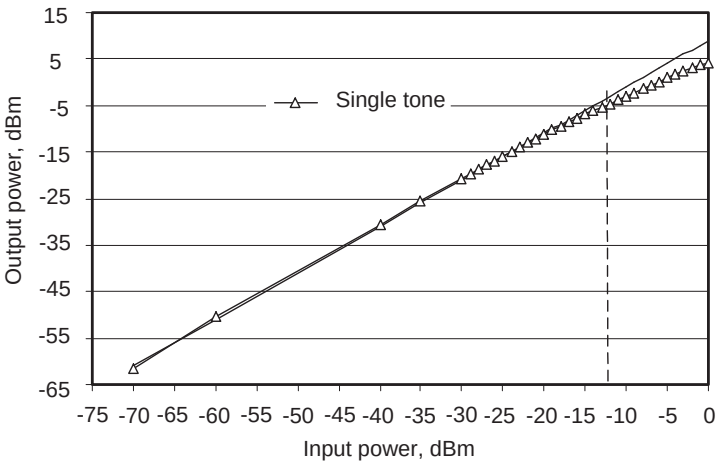

Figure 6.24: Measured linearity of LNA at 1.2 GHz with single-tone excitation.

6.3.4.3 P_{1dB} and IP_3

The linearity of the LNA is measured by the single-tone excitation, 1 dB compression point of the input power is about -12 dBm at 1.2 GHz (Fig. 6.24). The non-linearity performance of the LNA is measured by a two-tone set-up. The frequency offset of the two tones is 1 MHz. Fig. 6.25 shows that the extrapolated third-order intercept point is about -8 dBm for the input signal.

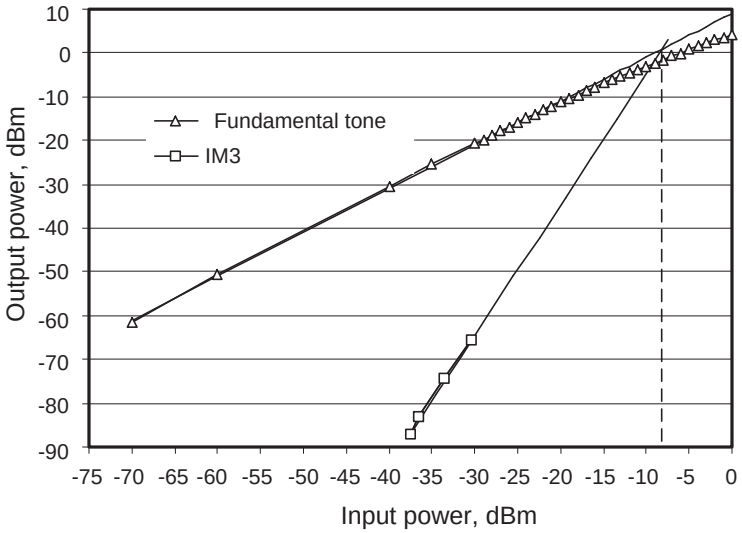

Figure 6.25: Measured IP3 of LNA at 1.2 GHz by a two-tone set-up.

6.4 Summary

This chapter reports the design and implementation of an LNA operating at 77 GHz and 79 GHz for automotive radar system covering the LRR and SRR simultaneously. The measurement shows that 21.7 dB peak gain occurs at 79 GHz and 20 dB gain occurs at 77 GHz. The 1 dB gain ripple bandwidth 4 GHz between 77 GHz and 81 GHz, and 3 dB gain bandwidth is 9 GHz in the range of 74 GHz to 83 GHz.

Another variable band LNA is also designed and measured for multi-band applications. This LNA presents a wide band input match to 50 Ω load, and employs a varactor in the output impedance matching network to ease the implementation of the variable band function. This LNA works between 0.7 GHz and 1.4 GHz by tuning the control voltage, and it can be applied in the multi-band systems to realize the tunable function without using bondwires and switches or tuning inductors.

Chapter 7

77 GHz/79 GHz Improved Down-conversion Mixer

In this chapter the design and implementation of a fully integrated active down-conversion mixer for automotive radar applications are presented. Firstly, the current existing mixer structures are analyzed. Secondly, a new micromixer structure, which was first published by the author of this thesis in [5], is proposed; theoretical analysis and circuit simulation show that both the gain and the noise figure of a micromixer with this structure are improved against the other existing micromixer structures at the time of publication of [5]. Thirdly, a 77 GHz/79 GHz down-conversion mixer with the proposed structure is designed and implemented; the measurement method is described in detail and the measurement results are shown. Finally, a comparison to the state-of-the-art microwave mixers shows that this micromixer achieves the highest figure-of-merit defined by [54]. This is the first micromixer implemented at 77 GHz/79 GHz in SiGe technology in the world.

7.1 Introduction

Performing the mixing function for signals in the transmission paths, mixer influences the system performance with its parameters such as linearity, noise figure, and gain, which relate with the structure and the technology adopted in the mixer design. Some millimeter-wave mixers in GaAs technology have been reported since decades ago [49], [50], etc. This chapter will demonstrate down-conversion mixer in SiGe technology for the automotive radar application in W-band. In this following sections, I will elaborate the mixer design, the new structure, implementation, and the measurement results in detail.

7.2 Fundamental Characteristics of Mixer

7.2.1 Mixer Topologies

Mixers can be classified into active and passive mixers. Passive mixers such as diode mixers and resistive mixers show conversion loss but with usually better noise figure and higher linearity. Active mixers usually provide gain which in turn reduce the noise contribution from the succeeding stages to the whole receiver. Due to the limitation of diode model in the available technology, I design an active mixer with gain and acceptable noise figure instead of a Schottky diode mixer with higher loss observed in simulation at 77 GHz band.

Mixer topology can be divided into unbalanced, single-ended RF single-balanced, differential RF double-balanced, and single-ended RF double-balanced. In the following, the structures of the active mixer topologies will be discussed.

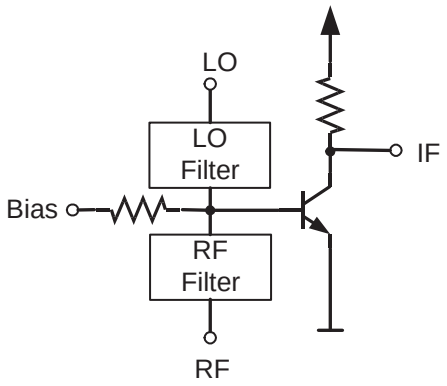

Figure 7.1: Unbalanced active mixer.

Unbalanced Structure The simple unbalanced mixer structure is shown in Fig. 7.1. The RF and LO signals are mixed at the base of the transistor after the respective filters. LO signal modulates the transistor with enough large amplitude, and the non-linearity of the transistor performs the mixing function.

The unbalanced mixer structure does not reject RF-IF, LO-IF, and LO-RF feed-through. The LO signal is injected into the RF port through the RF filter, the RF signal also enters the LO port through the LO filter. In the case of low IF, LO and RF frequencies are very close to each other. So high-order filters would be required to reject the LO-RF leakage.

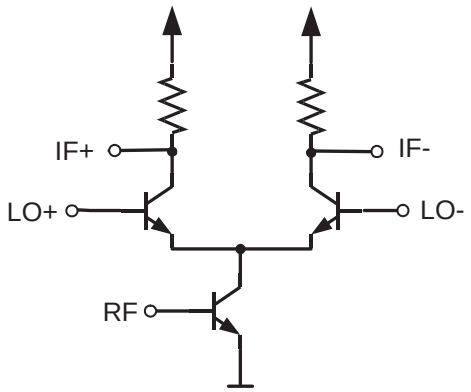

Figure 7.2: Single-Ended RF single-balanced active mixer.

Single-Ended RF Single-Balanced Structure Fig. 7.2 depicts the topology of a single-ended RF single-balanced mixer. The single-ended RF signal is fed to the lower CE transistor, while the differential LO signals are fed to the upper switching transistor pair. Multiplicative mixing is performed by the switching pair which should switch instantaneously from one transistor to the other. Therefore a high LO power level is required. A low LO power causes unsatisfying switching and thus degradation of the gain and noise figure. The single-balanced mixer structure rejects RF-IF and LO-RF feed-through, but does not reject LO-IF feed-through.

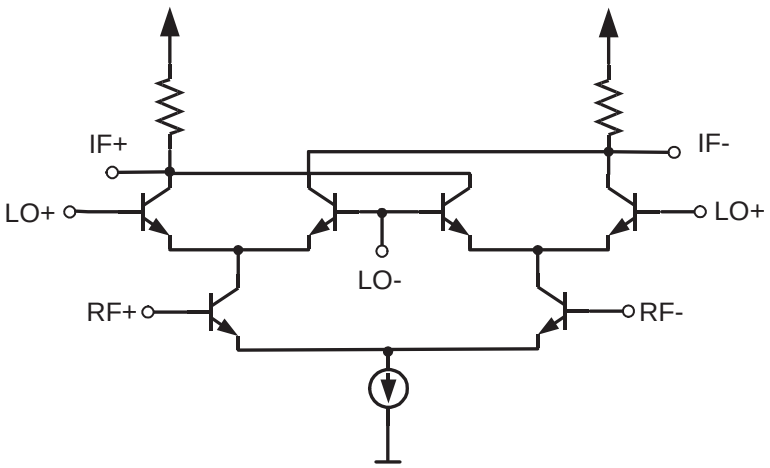

Figure 7.3: Differential RF double-balanced active mixer.

Differential RF Double-Balanced Structure Fig. 7.3 shows the well-known double-balanced Gilbert cell mixer. This mixer consists of a differential amplifier and a switching quad. The RF signals are amplified by the differential amplifier. The LO signals are fed to the switching quad. The linearity of the mixer is dominated by the differential amplifier. The mixing functionality is performed by the switching quad transistors. The balanced circuit structure suppresses the LO-IF and RF-IF feed-through. LO-RF feed-through is also

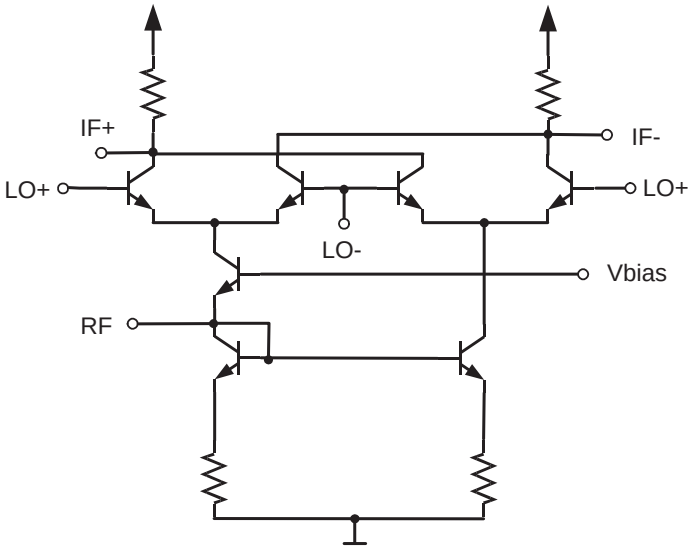

Figure 7.4: Single-ended RF double-balanced active micromixer.

rejected if the switching quad transistors are driven differentially.

Single-Ended RF Double-Balanced Structure As depicted in Fig. 7.4, this structure needs a single-ended RF input signal and does not need a single-to-differential converter or a differential LNA before the mixer. This structure provides differential RF signals to the LO quad transistors by the current mirror. Therefore, it is a double-balanced structure. The LO-IF feed-through is suppressed, and LO-RF and RF-IF feed-through are dependent upon the quality of the differential RF signals.

7.2.2 Mixer Parameters

Conversion Gain As a non-linear circuit, a mixer translates the frequency from an input RF to an output IF (for down-conversion mixer). The voltage gain is defined as the division ratio between the amplitudes of the output IF and the input RF, therefore the name of "conversion gain".

Noise Figure The noise figure (F) is defined as the division ratio between the signal-to-noise ratios (SNRs) at the output and the input. The noise figure of an amplifier is defined as how much noise is added by the amplifier, and can be expressed as:

$$F = \frac{SNRI_{IN}}{SNR_{OUT}} = \frac{kTBG + N_a}{kTBG} \tag{7.1}$$

where k is the Boltzmann constant and is equal to $1.38 \times 10^{-23} J/K$, T is the temperature in Kelvin, B is the measurement bandwidth, G is the gain of the amplifier, and N_a is the added noise from the amplifier.

The noise figure for mixer can be expressed as single-sideband (SSB) or double-sideband (DSB). SSB noise figure is defined when the expected signal is only in the upper or lower sideband, no image signal is included, but noise includes the contribution from the desired and the image frequency band and it is related to the hetero-dyne architecture. Then the definition of SSB noise figure is:

$$F_{SSB} = \frac{kTB_LG_L + kTB_UG_U + N_a}{kTB_UG_U}, \tag{7.2}$$

where B_L, G_L are the bandwidth and gain at the lower sideband, and B_U, G_U are the bandwidth and gain at the upper sideband respectively.

The DSB noise figure applies for the signal and noise which appear in both sidebands. We use the definition of DSB noise figure:

$$F_{DSB} = \frac{kTB_LG_L + kTB_UG_U + N_a}{kTB_LG_L + kTB_UG_U} \tag{7.3}$$

Therefore, $F_{SSB} = F_{DSB}(1+\frac{G_L}{G_U})$. For low IF and high LO frequencies, the gain at lower sideband is nearly equal to that at upper sideband, then $F_{SSB} = F_{DSB} + 3\,dB$.

1 dB Gain Compression Point 1 dB gain compression point is a measure of the linearity of the mixer. It occurs when the RF input power induces an output power which is 1 dB less than its linear magnitude. Above this level, the mixer does not work in a linear region and has not a linear increase in output power.

DC Offset DC offset is a measure of the unbalance of the mixer and is zero for an ideal mixer. DC offset defines the output voltage at IF port if only LO signal is applied and the RF port is terminated with 50 Ω load.

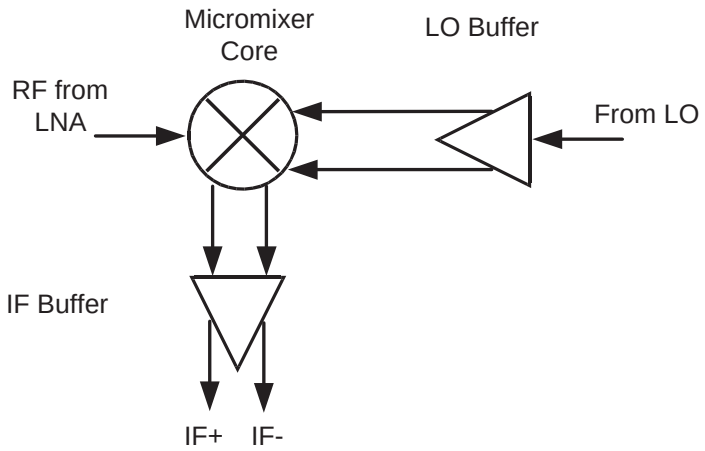

Figure 7.5: Block diagram of the mixer design in this work.

Isolation Isolation is a measure of the leakage between the mixer ports and denotes the balance within the mixer. A high isolation corresponds to a low leakage or feed-through. The LO-RF isolation is the amount of LO level attenuated when measured at the RF port, when the IF port is terminated with 50 Ω load. Since normally RF power is much smaller than LO power, so only LO isolation is specified, and RF isolation is not a problem. The requirement for the isolation levels are different for different systems in which the mixer is used. The LO-IF isolation and RF-IF isolation are critical because leakage

level may saturate the following stage.

7.3 Circuit Design of 77 GHz/79 GHz Down-Conversion Mixer

The mixer in this work includes a micromixer core with single-ended RF input, thus without the need of using an RF balun at the RF input. The block diagram of the whole mixer is illustrated in Fig. 7.5. This micromixer structure was first proposed by the author of this thesis in [5].

The LO buffer is added to provide large enough LO power to drive the mixer core with differential LO signals. The IF buffer is to provide a matching port to the impedance of the measurement equipment.

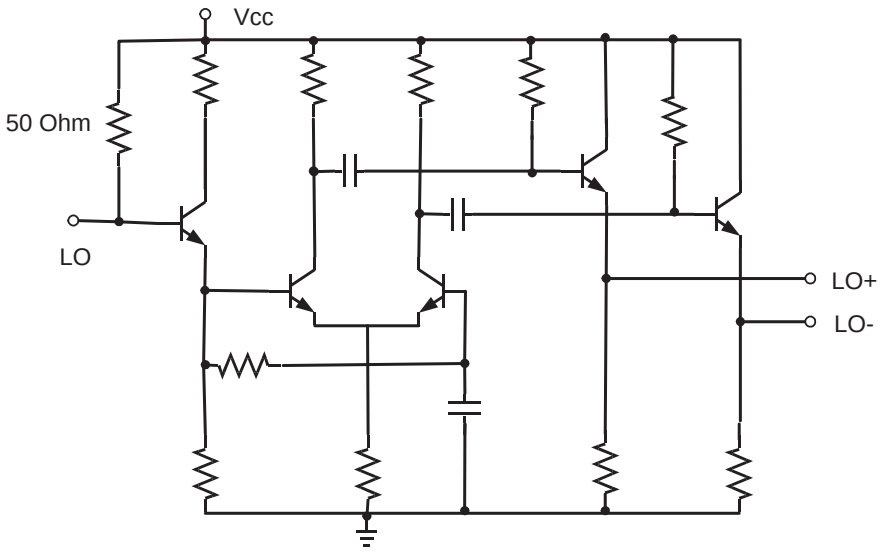

Figure 7.6: Schematic of LO buffer.

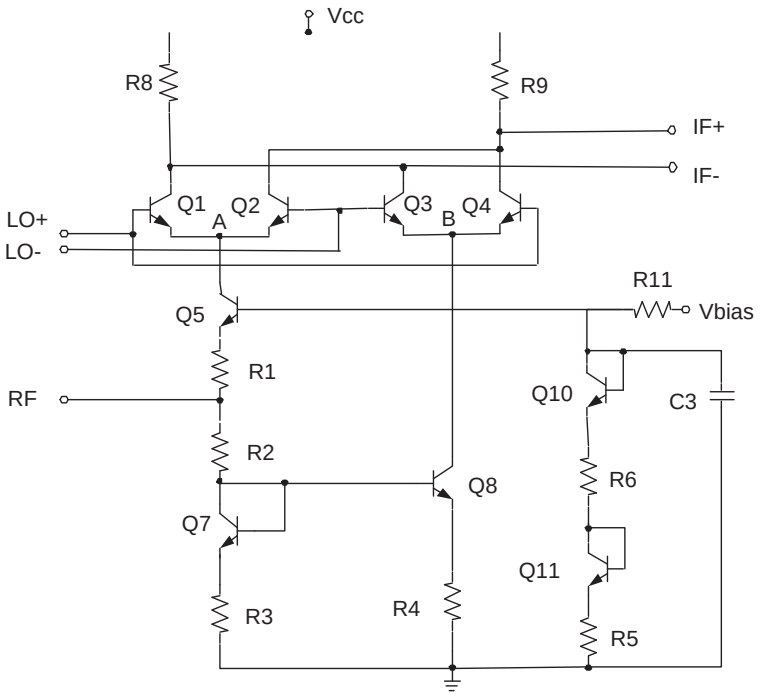

Figure 7.7: Gilbert micromixer core [58].

7.3.1 LO Buffer

The schematic of the LO buffer is shown in Fig. 7.6. It consists of a differential amplifier providing differential output signals to the following stages. A 50 Ω resistor and transmission line are used at the input to provide a good match to the 50 Ω LO input port. Additionally, the LO buffer provides constant gain for the LO differential signals and provides sufficient power to drive the mixer. AC coupling is used to remove the DC offset of the differential LO signals. Furthermore, emitter followers behave as low impedance interface to the mixer core.

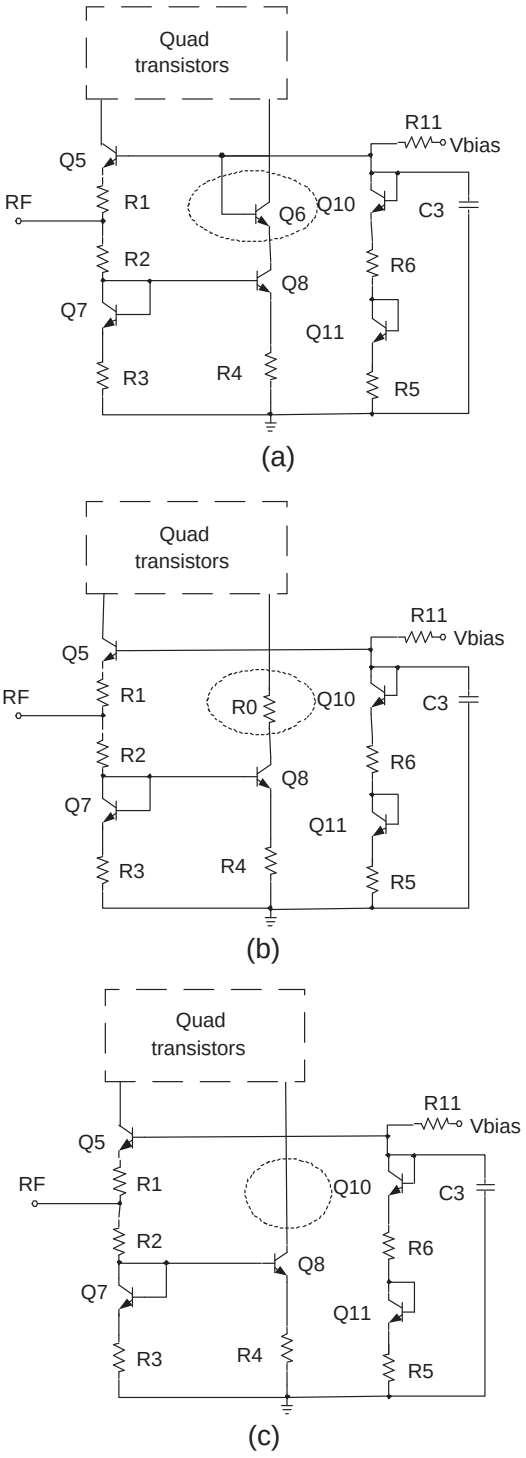

Figure 7.8: Current existing micromixer structures: (a) Structure in [58], (b) Structure in [60], (c) Structure in [61].

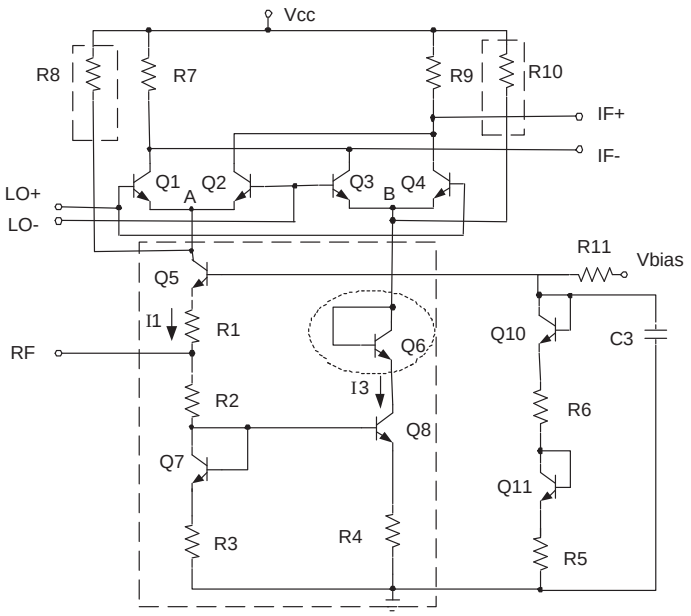

Figure 7.9: Schematic of proposed 77 GHz micromixer core with single-ended RF and differential LO and IF.

7.3.2 Improved Micromixer Core

The micromixer core I designed is based on the Gilbert micromixer cell [58], as shown in Fig. 7.7. The Gilbert micromixer has better linearity performance due to its common base RF input stage compared with the common Gilbert double-balanced mixer which feeds the RF signal to the common emitter RF input stage (Fig. 7.3). The so far reported micromixer structures are shown in Fig. 7.8, what differentiates my proposed structure from the existing structures is the mirrored RF branch which is marked in an ellipse. Q_6 is either not used or connected in different ways in the previous existing structures. We are concerned about the RF signals fed to the switch quad at node A and node B, because the left branches providing the RF signal are same for structures in Fig. 7.8, so we concentrate on the amplitude and phase comparisons for current in the right branch for the four structures.

In my proposed mixer structure, Q_6 is connected in a diode form as shown

in Fig. 7.9. The benefit of connecting Q_6 in this way is the better balancing of the amplitude and phase of the differential RF signals. This is realized by providing a more symmetric structure for RF signals at node A and B. Then this results in the cancellation of the non-linearity of I_1 and I_3 and improves the performance of the micromixer.

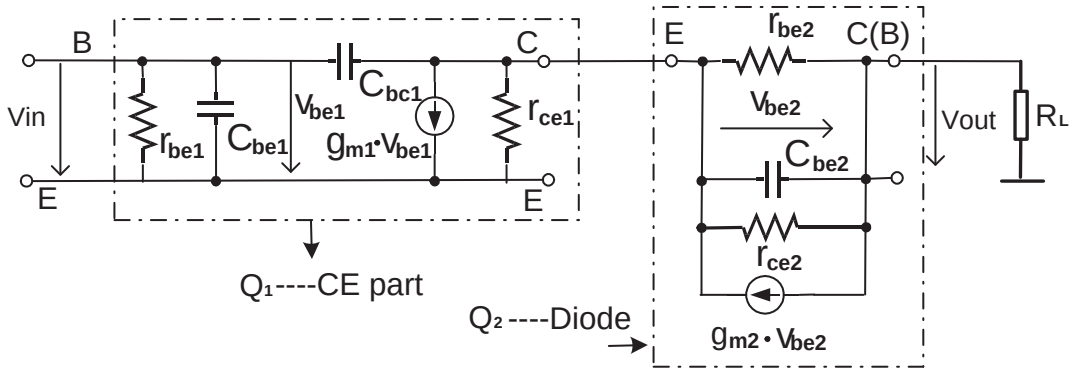

Figure 7.10: Equivalent circuit for right branch of (new) in 7.9: CE and diode in series.

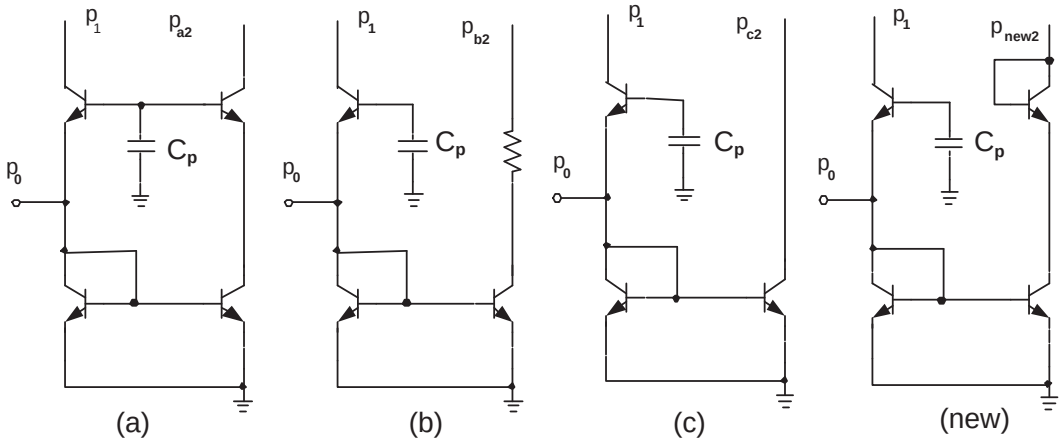

Figure 7.11: Phase definitions for each structure.

The equivalent circuits of the right branch of the structure (a) is in cascode topology, the equivalent circuit is shown in Fig. 6.8 in Chapter 6. Fig. 7.10

shows the right branch of the structure (new). We can neglect r_{ce} in current analysis becasue it is much larger than R_L .Connecting transistor Q_6 in diode form does not change the output impedance of the CE transistor in cascode topology too much, i.e, $\approx \frac{1}{g_{m2}}$. And $i_c \approx i_e$ for transistor Q_6, similarly in cascode topology, so the current magnitudes in the right branch for structure (a) and (new) have little difference. However the capacitor C_{bc2} between collector and grounded base included in Fig. 6.8 is shorted, and the capacitor C_{be2} is connected in series, so the equivalent capacitance between the base of CE and the collector of the diode is reduced by the C_{be2} in series in Fig. 7.10, this compensates the phase lag of V_{out} in Fig. 6.8 at high frequencies.

I construct the simulation in ADS to compare the phase and amplitude difference for four structures in Fig. 7.11. In three-port S-parameter simulation, port one is the RF input port with phase p_0, port two is defined for phase p_1 corresponding to node A, and port three is defined for phase p_{a2}, p_{b2}, p_{c2}, and p_{new2} corresponding to node B for the four structures. Voltage drop on R_0 in structure (b) is 0.7 V same as that for the diode. The four simulation results are compared in Table. 7.1. The proposed structure shows better phase balance than the other three types because of the compensation for phase shift of RF signal at right branch. While structure (c) has the best amplitude balance, this is because that in (c), the incidental inequality of VCE of Q_8 helps to recover some current gain in the mirror lost due to its finite ac beta. Since the structure depicted in Fig. 7.8 (c) uses no component in the mirrored RF branch, Q_8 suffers avalanche risk. This is particularly important for SiGe technologies which have low BV_{CEO}. Since BV_{CEO} is 1.9 V in f_T 180 GHz SiGe technology, V_{CE} of Q_8 is at the limit. Therefore structure (c) is not suitable for low BV_{CEO} technologies. In sum, the proposed structure improves the linearity of the two differential RF signals and thus increases the gain, reduces the

NF without increasing the complexity of the circuit and avoids the avalanche risk.

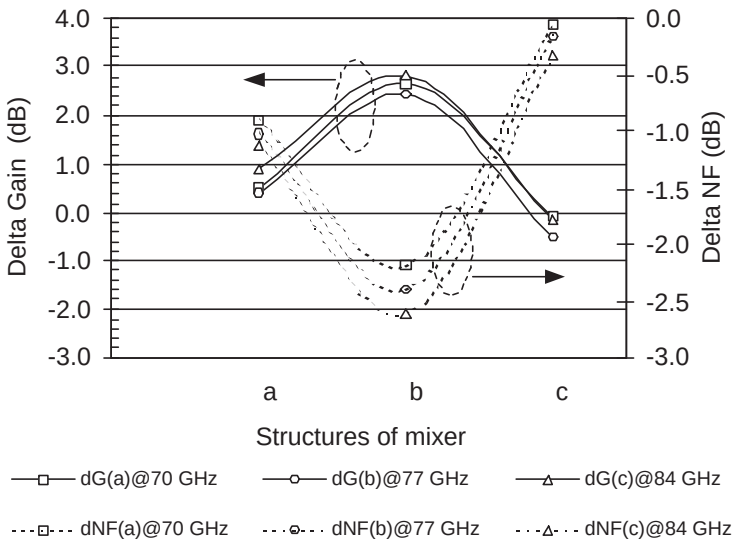

Figure 7.12: Gain and NF comparison between the proposed mixer structure and the existing structures at different frequency bands.

	Type (a)	Type (b)	Type (c)	Type (new)
$(\angle(S_{21})\text{-}\angle(S_{31}))^\circ$	-122.436	-106.163	-115.231	-146.606
$\lvert S_{21}\rvert\text{-}\lvert S_{31}\rvert$	0.232	0.35	0.210	0.225
S_{21}[dB]-S_{31}[dB]	5.623	11.381	4.025	5.443

Table 7.1: Phase and amplitude comparison in ADS S-parameter simulation.

To verify the improvement, three circuits are designed at 70 GHz, 77 GHz, and 84 GHz respectively. The gain and noise figure between the proposed mixer structure and the existing micromixers are compared in simulation and illustrated in Fig. 7.12. We define dG_x=G_new-G_x, dNF_x=NF_new-NF_x, where G_new (or NF_new) and G_x (or NF_x) are the gain (or NF) of the new structure and structure (x) in Fig. 7.8 respectively, x denotes a, b, and c. My proposed structure reduces the NF compared with other three structures and the reduction is more noticeable at higher frequencies. The reason is that the individual non-linearity of I_1 and I_3 are cancelled, thus

the noise interference part is removed. The improvement for the gain is also compared with structure (a) and (b) for the same reason. Compared with structure (c), the gain is reduced by 0.09 dB, 0.51 dB, and 0.15 dB at 70 GHz, 77 GHz, and 84 GHz respectively. These results agree with the above analysis.

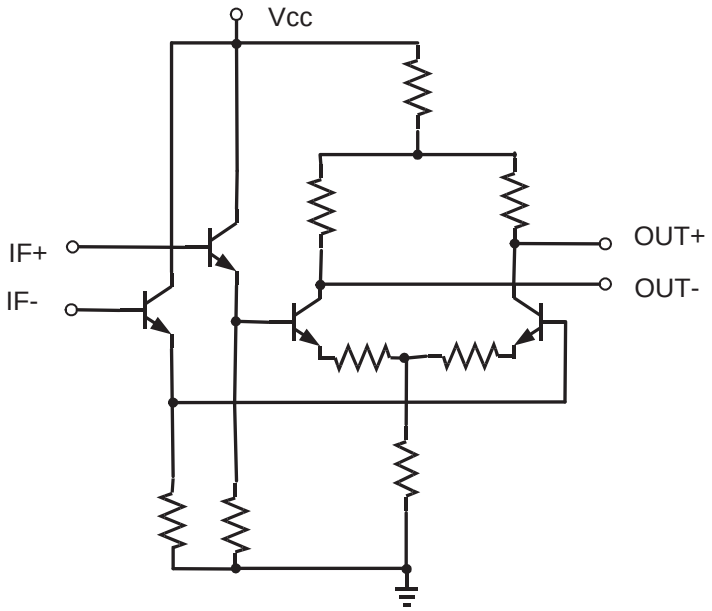

Figure 7.13: Schematic of IF buffer for measurement and output port matching.

The RF port matching can be further finely optimized by the control voltage V_{bias}. R_8 and R_{10} (Fig. 7.9) in the dashed block are used to inject current and increase the gain without increasing the tail current and power consumption [59].

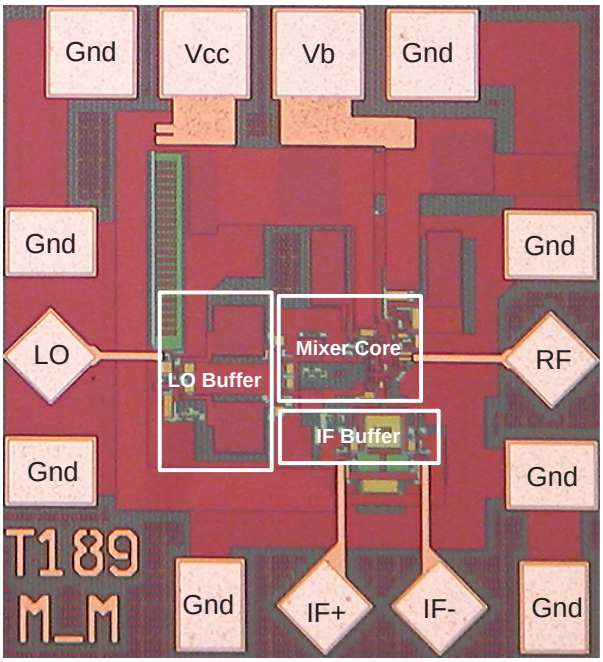

Figure 7.14: Chip photo of the 77 GHz/79 GHz down-conversion micromixer.

7.3.3 IF Buffer

The IF buffer is a differential amplifier to provide the IF signal to the 50 Ω measurement port. The circuit is shown in Fig. 7.13. To avoid the influence of IF buffer to the measurement of mixer, the gain of the IF buffer is designed to be only 1 dB in simulation. Therefore the gain and noise figure of mixer core are not influenced in measurement.

7.4 Layout

Fig. 7.14 shows the chip photo of the mixer die. The chip occupies $0.5 \times 0.55\,mm^2$ including pads, and $0.3 \times 0.2\,mm^2$ without pads. Input and output port matching are achieved by employing the transmission line and including the pad capacitance.

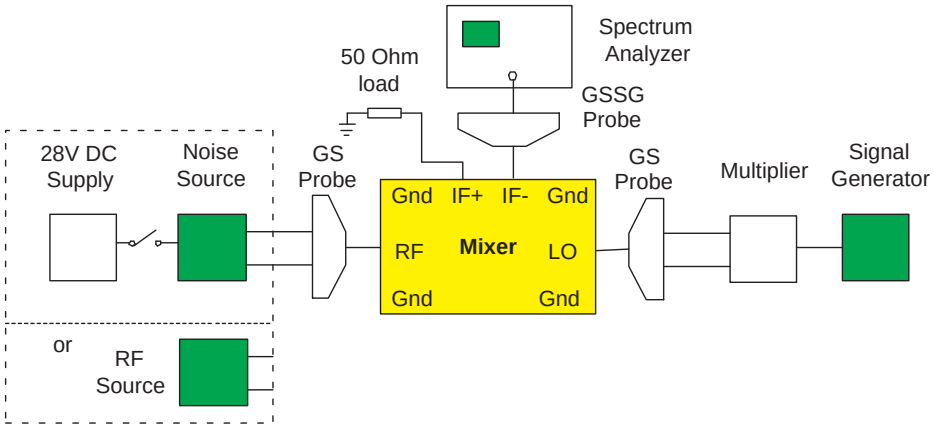

Figure 7.15: Block diagram of mixer measurement set-up for gain and noise figure.

7.5 Measurement Results

The measurements are performed on wafer with HP 83558A source module and multiplier for 75-110 GHz (W-band), Agilent W8486A W-band power sensor, HP E4419B power meter, W-band noise source, and Aeroflex PN9000 phase noise test system. GSG probe for W-band and GSSG probes for low frequency are used.

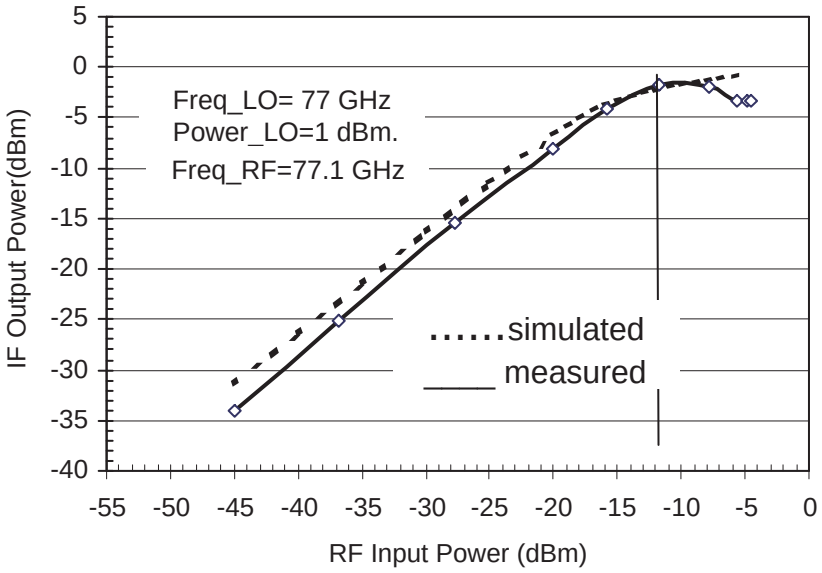

Figure 7.16: Measured conversion gain versus RF power.

7.5.1 Linearity, Gain, and Port Isolation

Fig. 7.15 is a block diagram of the setup for gain and NF measurement. The mixer consumes 176 mW totally with only 49.5 mW for the mixer core, operating at 4.5 V with total current consumption of 39 mA. With 2 dBm LO power, a maximum gain of 13.4 dB at 77 GHz is measured. Fig. 7.16 depicts the output power for an IF frequency of 100 MHz versus RF input power. The LO frequency and power is 77 GHz and 1 dBm respectively. The mixer shows a wide dynamic range with input 1 dB compression point of -12 dBm.

In Fig. 7.17, the simulated and measured conversion gain versus LO and RF frequency are shown for 100 MHz IF frequency and 1 dBm LO power. The measured conversion gain versus RF frequency is larger than 10 dB at center frequency of 77 GHz and 84 GHz and peaks also for LO frequency at 77 GHz. The gains at 77 GHz and 79 GHz are 13.4 dB and 7 dB respectively. The conversion gain versus LO power is also investigated, the simulated and measured

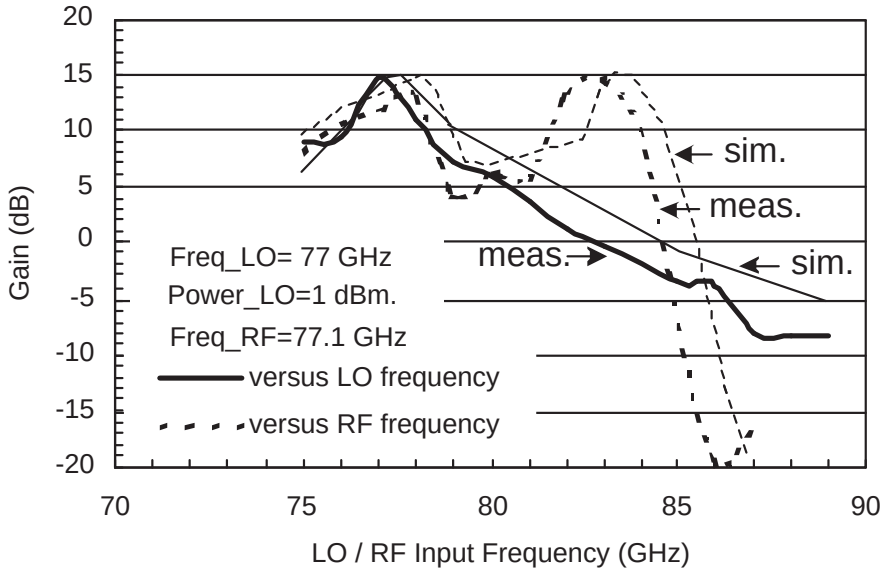

Figure 7.17: Conversion gain versus LO and RF input frequency.

curves are shown in Fig. 7.18. The gain varies linearly with the LO power up to 2 dBm, then the gain approaches saturation.

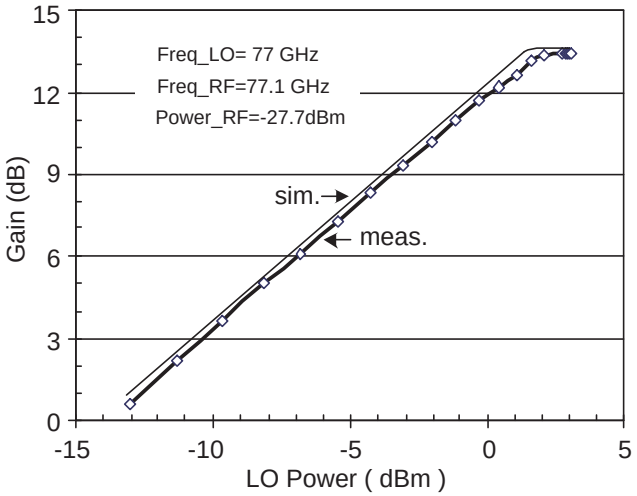

Figure 7.18: The measured conversion gain versus LO power.

Another important issue is the isolation between the ports of mixer, especially the LO port leakage to other ports. The measurement shows that the isolation is larger than 28 dB between LO port and IF port and larger than 34 dB between LO port and RF port (Fig. 7.19).

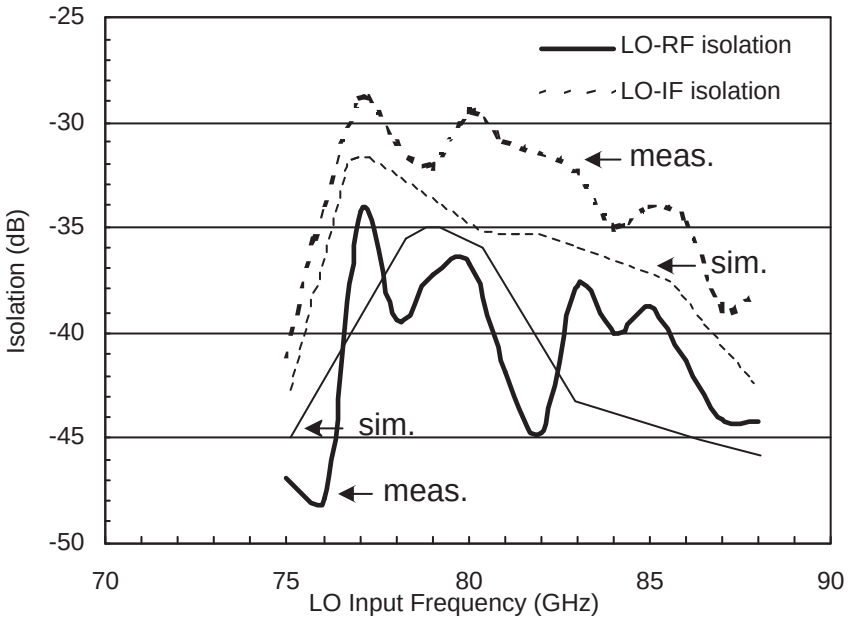

Figure 7.19: Measured port isolation of LO to RF, and LO to IF.

7.5.2 Noise Figure

Noise figure (or Noise factor) contains the important noise information of the noise performance of the RF system. The basic definition is:

$$NoiseFactor(F) = \frac{TotalOutputNoisePower}{OutputNoiseDueToInputSourceOnly}. \tag{7.4}$$

Measurement methods can vary for different systems. Some systems have high gain and low noise figure, some have low gain and high noise figure, and some have very high gain and wide range of noise figure. Measurement methods can be selected accordingly.

A straightforward way to measure the noise figure is by using the noise figure meter. One can measure the noise figure over a certain frequency range, and the analyzer can display the system gain and noise figure simultaneously. However, this method has also limitations. The analyzer has frequency limits, and if we

measure the high noise figures, e.g. when the noise figure exceeds 10 dB, the measurement can be not accurate.

Y factor method is also a popular way to measure the noise figure. Similarly as the noise figure meter as mentioned in the above method, an ENR (Excess Noise Ratio) source is needed. The ENR requires a high voltage DC supply, works over a wide band, and it has its own standard noise figure parameter at specified frequencies. By turning the noise source on and off (switch the DC voltage on and off), we can measure the difference of the output noise spectral density from the spectrum analyzer.

$$NoiseFigure(NF) = 10 \times \log_{10}(\frac{10^{(ENR/10)}}{10^{(Y/10)-1}}), \tag{7.5}$$

where ENR is the number listed on the table on ENR head, Y is the difference of the output noise spectral density for on and off states. The definition for ENR is: $ENR = \frac{T_H - 290}{290}$. T_H is a hot T when the noise source is on, and 290 K corresponds to a cold T.

Another convenient and more accurate method is called "Gain Method" which is also based on the definition mentioned earlier in equation (7.4). In equation (7.4), the "Noise" is due to two effects. The noise in the nominator is that the interference feeds into the RF systems in the form of signals that differ from the expected one. The other item in the denominator is due to the random fluctuation of carriers in the RF system (or DUT). The second effect is a Brown motion, the available noise power is:

$$P_{NA} = k \cdot T \cdot \triangle f, \tag{7.6}$$

where k is the Boltzmann's constant ($1.38 \times 10^{-23} Joules/\triangle K$), T is the

temperature in Kelvin, and $\triangle f$ is the noise bandwidth (Hz). At room temperature, T=290 K. The noise power density is -174 dBm/Hz. Then we have the equation of noise figure below:

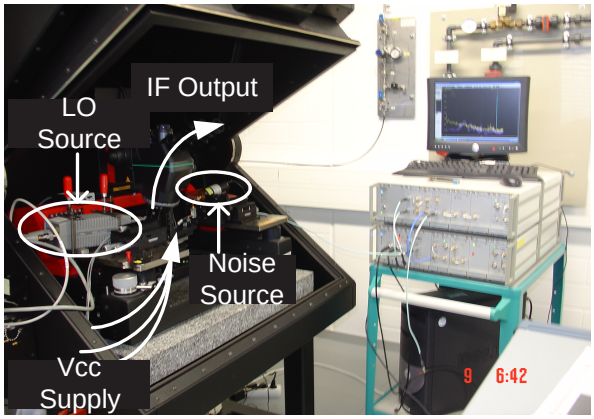

Figure 7.20: Mixer measurement set-up.

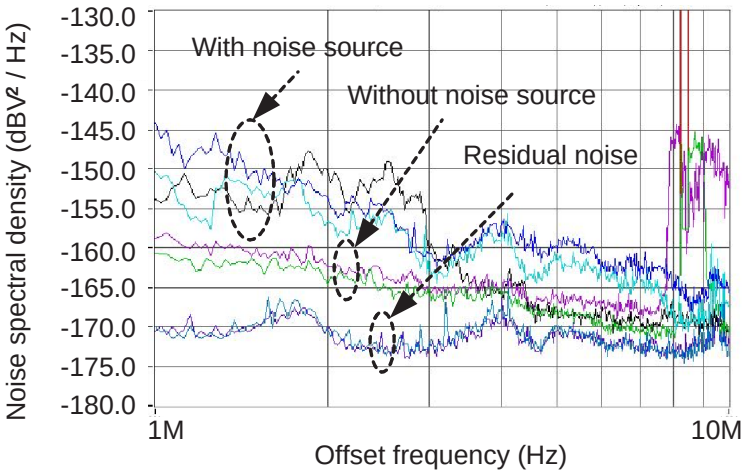

Figure 7.21: Measured noise spectral density at IF port.

$$NF = P_{NOUT} - (-174dBm/Hz + 20 \cdot \log_{10}(BW) + Gain), \tag{7.7}$$

where P_{NOUT} is the measured total noise output power, the noise power density is -174 dBm/Hz at room temperature 290° K, BW is the interested bandwidth,

Gain and NF are the gain and noise figure of the DUT respectively. All the units are in dB. To make the formula easier, we can directly measure the noise spectral density (dBm/Hz). Then the equation turns to be: $NF = P_{NOUTD} + 174\,dBm/Hz - Gain$. Based on the advantages and disadvantages of the three methods, I adopted the "Gain Method" in my mixer noise figure measurement. The noise spectral density is measured by Aeroflex PN9000 phase noise test system. The set up is shown in Fig. 7.20. The measured noise spectral density is recorded as shown in Fig. 7.21.

By measuring the noise spectral density of three cases, i.e. the residual noise, the noise with and without noise source shown in Fig. 7.21, the measured output noise power density of the mixer and the residual noise power density are $-160\,dBV^2/Hz$ and $-170\,dBV^2/Hz$, respectively. The data was obtained by repeating each step several times with the similar curves shown in Fig. 7.21. 18.4 dB noise figure was obtained by calculation.

7.5.3 Discussion

The third-order intercept point (IP_3) is also a very important parameter for mixer. However, we have not found reports about measured IP_3 results near 77 GHz range or beyond. The practical problems prohibit us from building a measurement set-up. The mechanical difficulties encountered during installing the required equipment and apparatus is the installing two 77 GHz RF sources, a W-band coupler, a W-band LO source module, and four probes. Another source (from Agilent) using tricky mixing algorithm to establish a two-tone signal works for low frequencies only. Since all the measured data, including 1 dB compression point, conversion gain, and port matching agree with the simulation data very well, we can approximately use the simulated $-2.5\,dBm$

IP_3 as a practical metric for the mixer. Furthermore, the rule of thumb states that the real IP_3 is around $10\,dB$ than P_{1dB}. That is, the real IP_3 can be estimated as $-12\,dBm + 10\,dBm = -2\,dBm$. This IP_3 also agrees well with the simulated IP_3 of -2.5 dBm with only $0.5\,dBm$ estimation error. Therefore we could estimate that IP_3 is about $-2.5\,dBm$.

7.6 Comparison to the State-of-the-art

To compare the performance of our mixer with the other state-of-the-art, I adopt the definition of FOM in [62]:

$$FOM_{MIX} = (CG - NF) + (MIX_{LIN} - NF) - MIX_{PWR} - MIX_{ISO}, \quad (7.8)$$

where CG is the conversion gain, and

$$MIX_{LIN} = 10Log(\frac{(IP_{1dB})_W \star (IIP_3 - 9.6)_W}{(IP_{1dB})_W + (IIP_3 - 9.6)_W}) \quad (7.9)$$

$$MIX_{PWR} = 10Log(\frac{P_{diss}}{1mW}) \quad (7.10)$$

$$MIX_{ISO} = ISO_{LO-RF} + ISO_{LO-IF} + ISO_{RF-IF} \quad (7.11)$$

$$ISO_{LO-RF} = 10Log(\frac{(LO_{PWR-RF})_W}{IP_{1dB} - 10)_W} + 1) \quad (7.12)$$

$$ISO_{LO-IF} = 10Log(\frac{(LO_{PWR-IF})_W}{IP_{1dB} - 10)_W} + 1) \tag{7.13}$$

$$ISO_{RF-IF} = 10Log(\frac{(LO_{PWR-IF})_W}{IP_{1dB} - 10)_W} + 1) \tag{7.14}$$

Since not all papers provide the isolation data, so MIX_{ISO} is omitted in FOM_{MIX}. Table 7.3 includes the technical data of 77 GHz mixers and illustrates a comparison to the state-of-the-art. Our mixer achieves the highest FOM_{MIX}, showing 60% better linearity with 41% less power consumption compared to the reported active SiGe mixer.

	[51]	[52]	[53]	This work [5]
Type of Mixer	Subharmonic	Subharmonic	Gilbert	Micromixer
Vcc (V)	5	n/a	-5	4.5
Current (mA)	4.4	n/a	60	39
Conversion Gain (dB)	0.7	-14∼-18	22	13.4
LO Power (dBm)	10	5	2	2
LO Frequency (GHz)	38	36	77	77
SSB Noise Figure(dB)	23(sim.)	n/a	14	18.4
P_{1dB}input/output (dBm)	-8/-7.3	0	-30/-4	-12/1.3
Isolation (dB)	>30(LO-RF)	40(LO-IF)	n/a	>34(LO-RF)
				>28(LO-IF)
Technology (SiGe)	$0.5\,um$	$0.15\,um$	$0.18\,um$	$0.25\,um$
$f_T(GHz)$	80	n/a	200	180
Chip Size(mm^2)	0.86×0.9	1.5×1.0	0.55×0.45	0.5×0.55
FOM	-99.72	n/a	-93.58	-89.07

Table 7.3: Comparison to latest reported 77 GHz integrated microwave mixers.

7.7 Summary

An improved micromixer structure is proposed in this work and the analysis and simulation show the improvement on noise figure and gain for mixers. A

fully integrated active down-conversion micromixer in this structure is designed and measured at 77 GHz/79 GHz. The mixer works from 74 GHz to 84 GHz and the gain is larger than 10 dB. A 12.6 dB gain at 77 GHz and a 18.4 dB noise figure are achieved with 1 dBm LO power. With 2 dBm LO power, the maximum available gains are 13.4 dB and 7 dB at 77 GHz and 79 GHz, respectively. In comparison to the state-of-the-art mixers, this reported mixer shows the highest figure-of-merit. Compared with the active mixer in SiGe technology, the linearity of this mixer is 60% better while consuming 41% less power. Additionally, there is no need of using an RF balun. The disadvantage of the proposed mixer is the slightly higher noise figure, but the whole noise contribution from the mixer to the receiver is smaller than 0.1 dB if the LNA reported in chapter 6 is added before the mixer. So this slightly higher noise figure plays negligible influence on the total noise figure of the receiver.

Chapter 8

Measurement of Radar Receiver

8.1 Measurement and Discussion

Using the circuits presented in the previous chapters as building blocks, I designed an automotive radar receiver including a 77 GHz/79 GHz single-ended LNA, a 77 GHz/79 GHz down-conversion micromixer, and a 79 GHz to 82 GHz differential VCO. The block diagram of the receiver is illustrated in Fig. 3.2 (c) in Chapter 3. The radar receiver chip is implemented in SG25H1 technology, and the chip photo is shown in Fig. 8.1. This receiver chip occupies $1.26\,mm^2$ with pads and $0.5\,mm^2$ without pads. The system measurement set-up is depicted in Fig. 8.2.

Each building circuit of the receiver is measured separately. The separate on-wafer measurement of LNA is shown in Fig. 6.15. In the measurement with 3.5 V supply voltage, the peak gain S_{21} is 21.7 dB at 79 GHz, the gain is 20 dB at 77 GHz; the 1 dB gain ripple is between 77 GHz and 81 GHz, and the 3 dB bandwidth is from 74 GHz to 83 GHz.

The mixer has 13.4 dB and 7 dB gain at 77 GHz and 79 GHz, respectively

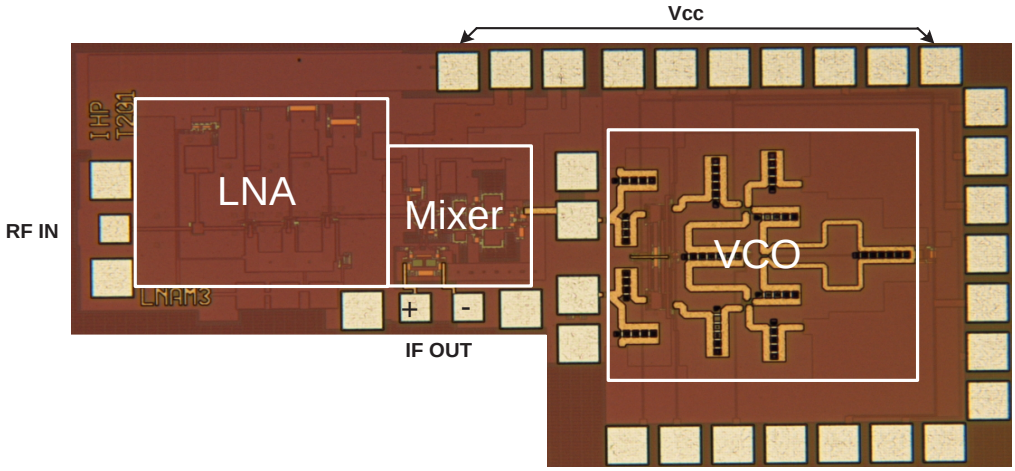

Figure 8.1: Die photo of the 79 GHz automotive radar receiver.

(Fig. 7.17). The input 1 dB compression point of the mixer is -12 dBm. The VCO frequency is also monitored and the measured oscillation frequency is between 79 GHz and 82 GHz as shown in Fig. 8.3.

The VCO's oscillation frequency can be shifted lower and trimmed to cover 77 GHz and 79 GHz simultaneously by cutting the lines using FIB technique[1]. The oscillation frequency is measured versus control voltage before and after cutting the lines (Fig. 8.3).

[1]The VCO block is from work done by Srdjan Glisic at IHP.

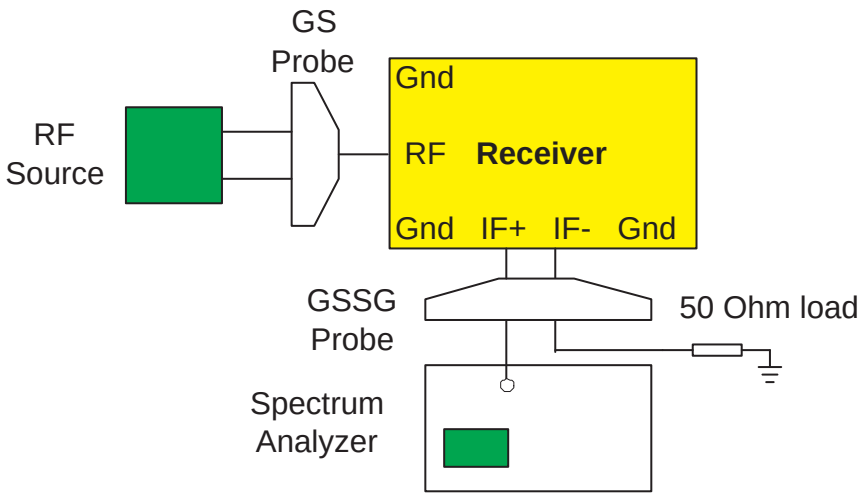

Figure 8.2: Block diagram of receiver measurement set-up for gain and linearity.

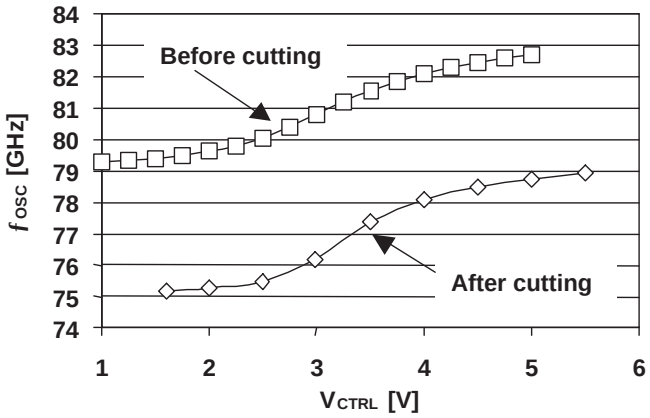

Figure 8.3: On-wafer measured VCO output oscillation frequency versus control voltage before/after cutting the lines.

The output power of VCO is also measured as shown in Fig. 8.4. The oscillation frequency versus temperature is observed in temperature range of -25 degree and 125 degree (Fig. 8.5). Additionally, the phase noise is measured and shown in Fig. 8.6, phase noise is -90 dBc@1 MHz offset.

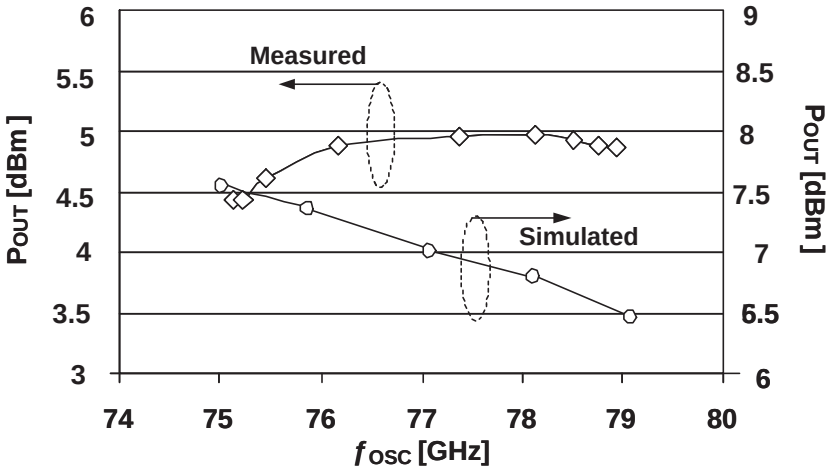

Figure 8.4: Measured and simulated VCO output power as function of oscillation frequency.

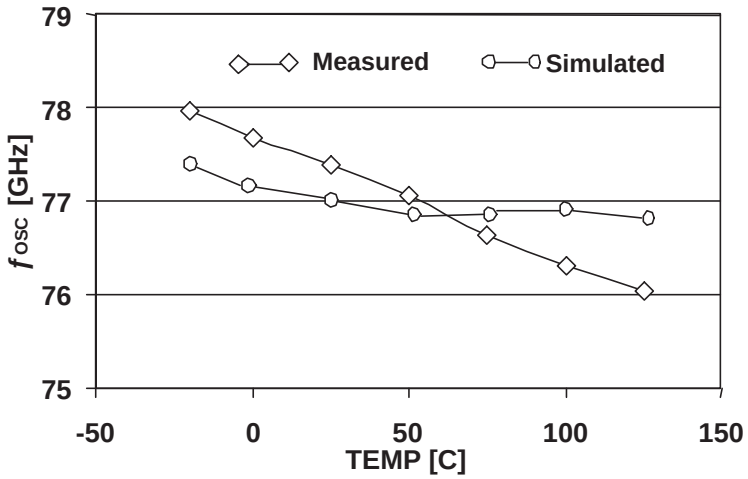

Figure 8.5: VCO oscillation frequency versus temperature.

This is the first reported single-ended 79 GHz radar receiver in SiGe technology in the time of the submission of [7] by the author of this thesis. In the receiver measurement set-up (Fig. 8.2), an RF signal is provided by E-band source module; one output port of the differential IF signal is connected to a 50 Ohm load, and the other output port of the differential IF signal is fed to the spectrum analyzer. The receiver is measured at 79 GHz, the output of IF spectrum is shown in Fig. 8.8. The simulated and measured gain and linearity

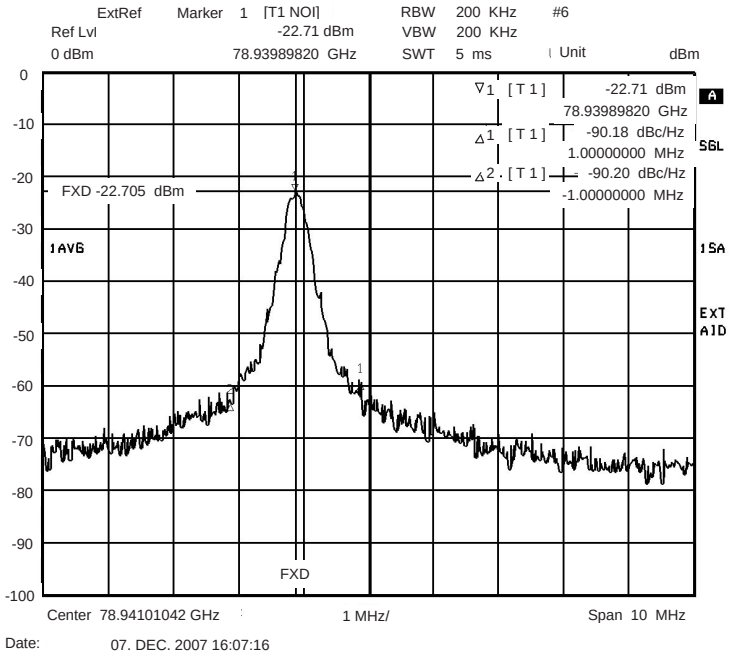

Figure 8.6: Measured VCO phase noise.

of the whole receiver are shown in Fig. 8.7.

The input 1 dB compression point of the whole receiver is about -35 dBm. The receiver shows 20-26 dB gain in the linear region, this is consistent with the calculation data from the LNA and mixer. Due to the equipment limitation in the receiver measurement, the NF was not measured. From the calculation from the measurement data of LNA and mixer, the NF is about 10.2 dB. Based on the good agreement of measurement and simulation of LNA and mixer, we estimate that the receiver's NF is about 10.2 dB which is less than the requirement [4].

8.2 Summary

The technical data of the receiver components is summarized in Table 8.1.

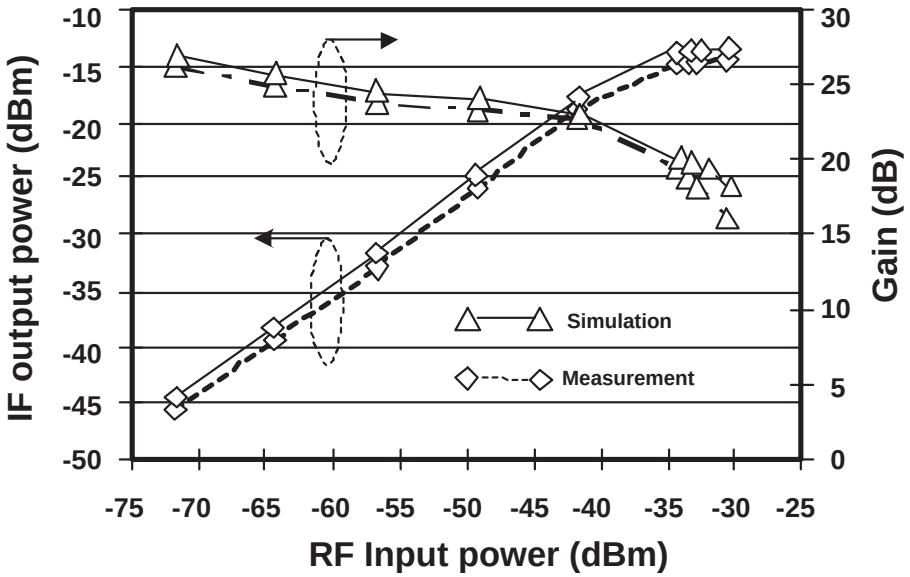

Figure 8.7: Simulation and on-wafer measurement results of linearity and gain of the whole receiver.

Further improvement of the circuit performance can be achieved by the redesign. The transmission lines of the VCO can be trimmed to cover the 77 GHz and 79 GHz simultaneously. The high speed low power frequency divider described in section 5.2 can be employed in VCO or PLL in future.

So far I have designed and implemented high-speed integrated circuits for 79 GHz receiver in IHP's SG25H1 technology. This is the so far first reported single-ended 79 GHz radar receiver [7] in SiGe technology. These results present the techniques of circuit design, and demonstrate the technology's good performance: small power consumption, less chip area, thus lower cost. This work shows that the SiGe technology is really one promising alternative to the expensive GaAs technology for applications such as automotive radar.

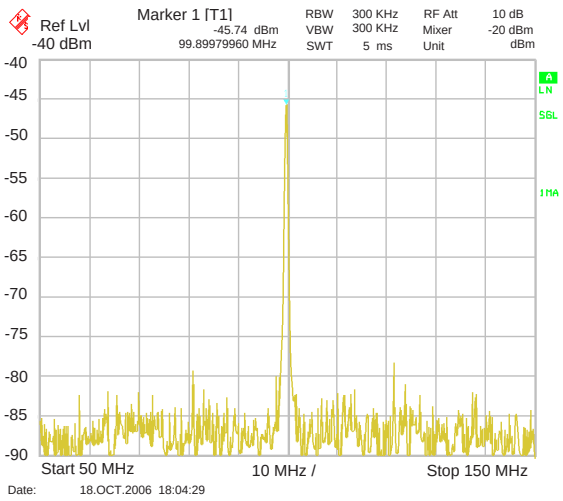

Figure 8.8: IF output spectrum of on-wafer measurement of the whole receiver.

	Vcc(V)	I(mA)	Power(mW)
LNA	3.5	30	105
Mixer core	5	10	50
Mixer with buffer	5	50	250
VCO core	5.5	20	110
VCO with buffer	5.5	69	380
Gain_LNA	21.7 dB@79 GHz, 20 dB@77 GHz		
Gain_Mixer	7 dB@79 GHz, 13.4 dB@77 GHz		
VCO frequency	79.1 GHz ~82.4 GHz		
Whole receiver gain	20~26 dB		
Input P_{1dB}	-35 dBm		
NF_{sim}	10.2 dB		

Table 8.1: Summary of the technical data of the 79 GHz receiver

Chapter 9

Conclusion and Outlook

With the growing demand to low-cost consumer products, the SiGe:C HBT technology becomes an alternative to the III-V technology due to its excellent device performance and lower cost. Based on IHP's SGC25C and SG25H1 technology, this thesis presents the work including high-speed frequency dividers, low noise amplifiers, and down-conversion micromixer for 77/79 GHz automotive radar receiver system and frequencies beyond.

After the introduction of the passive and active devices of the technology, I give a further analysis of passive devices, such as microstrip line, metal line, and coplanar line by simulation and measurement, and prepare for the circuit design at millimeter wave frequency range. The microstrip line is widely adopted in millimeter wave circuit design.

Three types of frequency dividers are designed, implemented, and measured in this work. The first type is a static frequency divider which employs the master-slave flip-flop. The circuit is biased at the optimal current density to achieve high speed. The layout is designed to be as compact as possible and the delay path is made as short as possible. The circuit was successfully mea-

sured, and the maximum operating frequency is 71.5 GHz at 3.5 V voltage supply. The whole circuit, including the output buffer, consumes 40 mA. The divider core consumes 12 mA current. Compared with the state-of-the-art, this divider shows much higher speed-to-power ratio than others in the similar SiGe technologies. Furthermore, I designed two types of dynamic frequency dividers - analog type and digital type. The regenerative dynamic frequency divider as the analog type employs a mixer core with output fed back to the mixer input to realize a divide-by-2 circuit. It is measured up to 103.16 GHz at 5.2 V supply voltage with 41 mW for the divider core and 195 mW for the whole circuit including the buffer. Another digital type dynamic frequency divider removes the latching pairs of the Master latch and Slave latch of the static frequency divider, therefore the maximum operating speed is improved and it is measured up to 105.5 GHz. This divider core and and the whole circuit consume 16.8 mA and 22.36 mA at 5 V supply voltage, respectively. The measurement of maximum operating frequency beyond 100 GHz is limited by the output power of measurement equipment. In summary, the static frequency divider shows wide bandwidth, and the dynamic frequency dividers are faster with limited bandwidth. For different applications, we can choose different types of dividers, and the trade-off in optimization should be taken into account.

I designed an LNA for the 77/79 GHz radar receiver system. Among the three often adopted structures: common base, common emitter, and cascode, the cascode structure has higher gain and isolation between input and output ports. Since a robust structure is beneficial to the millimeter wave frequency band, an LNA with cascode structure is selected and designed. The single-ended mode is used to reduce the power consumption and to half the chip area compared to the differential mode. The noise and power matching are

achieved simultaneously at the input port, while the other inter-stage matching and output matching are designed to obtain the maximum power transfer. The LNA was measured successfully on wafer in 110 GHz measurement set-up. It occupies $0.6 \times 0.5\,mm^2$ with pads, and $0.42 \times 0.42\,mm^2$ without pads. The measured peak gain S_{21} is 21.7 dB at 79 GHz, and the gain is 20 dB 77 GHz. 1 dB gain ripple is between 77 GHz and 81 GHz, and 3 dB bandwidth is from 74 GHz to 83 GHz. This LNA covers both 77 GHz and 79 GHz frequency band of automotive radar system. The linearity of the LNA is also measured by single-tone set-up. The LNA works linearly with the input power up to -21 dBm. A comparison to the reported 77 GHz LNAs demonstrates that this LNA has better FOM than other LNAs in GaAs technology and comparable FOM with LNAs' in more advanced SiGe technology.

In addition, I designed a tunable LNA covering 1 GHz frequency band. The LNA was measured on wafer consuming 17.5 mW with 2.5 V DC supply voltage. By adjusting the capacitance of the varactor in the resonant load of matching network, the center frequency can be tuned from 0.7 GHz to 1.4 GHz, the gain varies from 9 dB to 12 dB which agree with the simulation results. The measured noise figure is about 4.5 dB which is about 2 dB larger than the simulated value. 1 dB compression point of the input power is about $-12\,dBm$ at 1.2 GHz. This method can be applied in variable band amplifier, in LNA or mixer for one single frequency band or multiple bands.

A key circuit I designed and measured is a micromixer, which operates at 77 GHz and 79 GHz. I proposed an improved structure, which shows improved performance from simulation results compared with the existing structures. In on-wafer measurement, the mixer provides a maximum gain of 13.4 dB at 77 GHz with 2 dBm LO power at 4.5 V with total current consumption of 39 mA, and consumes 176 mW with 49.5 mW for the mixer core. The mixer

circuit shows a wide dynamic range with input 1 dB compression point of -12 dBm. With 1 dBm LO power, the measured conversion gains at 77 GHz and 79 GHz are 13.4 dB and 7 dB, respectively. The noise figure of the mixer is measured by using the gain method, 18.4 dB and 18.72 dB noise figure are obtained at 77 GHz and 79 GHz respectively.

Using the above components, I designed a receiver including an LNA, down-conversion mixer, and a VCO. The whole chip occupies $1.26\,mm^2$ including pads and $0.5\,mm^2$ without pads. Without trimming the transmission lines of the VCO, the VCO oscillates from 79-82 GHz, and the receiver was measured at 79 GHz with 100 MHz IF output. In future, the VCO can be trimmed to cover the 77 GHz and 79 GHz simultaneously, this will be the receiver which can work in both 77 GHz and 79 GHz for automotive radar system. This is the so far first reported single-ended 79 GHz radar receiver in SiGe technology.

In summary, this work presents the outstanding performance of building blocks in millimeter wave range and demonstrates the possibility to realize high-speed system using this SiGe technology. The low power consumption, small chip area, and thus lower cost are due to the advanced technology development, circuit design and optimization. The technology being further developed will push the frequency limit higher. Further research work include the whole transceiver and the packaging which very likely will adopt the flip-chip assembly technology.

Appendix A

Abbreviations

AC	alternating current
ACC	autonomous cruise control
Al	aluminum
B	boron
BER	bit error rate
BiCMOS	bipolar and complementary metal oxide semiconductor
BW	3-dB bandwidth
Cascode	cascaded anodes
C	carbon
CB	common base
CE	common emitter
CIFF	clocked-inverter feed-forward
CMOS	complementary metal oxide semiconductor
CPW	coplanar wave guide

CSL	current steering logic
DC	direct current
DTI	deep trench isolation
DSB	double-sideband
DUT	device under test
ECL	emitter coupled logic
EF	emitter follower
EM	electromagnetic
ENR	excess noise ratio
FER	frame error rate
FIB	focused ion beam
FF	flip-flop
FMCW	frequency modulated continuous wave
FOM	figure of merit
GaAs	gallium arsenide
GSG	ground-signal-ground
HBT	heterojunction bipolar transistor
IBES	saturation current of the base-emitter diode
IBCS	saturation current of the base-collector diode
IC	integrated circuit
IF	intermediate frequency

IHP	Institute of Innovations for High Performance Microelectronics
LAN	local area network
LNA	low noise amplifier
LPF	low-pass filter
LRR	long range radar
MAG	maximum available gain
MEMS	micro electromechanical system
MMIC	microwave monolithic integrated circuit
MMW	millimeter wave
MPW	multi-project wafer
NF	noise figure
PFD	phase / frequency detector
PLL	phase locked loop
RADAR	radio detection and ranging
RF	radio freuency
Rx	receive
SCFL	source-coupled field-effect transistor logic
SiGe:C	silicion germanium carbon
SGP	spice gummel-poon
SNR	signal to noise ratio
SoC	system-on-a-chip
SOLT	short-open-load-through

SRR	short range radar
SSB	single-sideband
STI	shallow trench isolation
TFF	Toggle-FF
Tx	transmit
TM	top metal
VBIC	vertical bipolar inter-company
VCO	voltage controlled oscillator
WLAN	wireless local area network

Appendix B

Symbols

α	attenuation coefficient
β	phase coefficient for lines; current gain for transistor current gain
bx	extrinsic base
bp	parasitic base
bi	intrinsic base
ei	intrinsic emitter
ci	intrinsic collector
cx	extrinsic collector
$\varepsilon_{r,eff}$	effective relative dielectric constant
ε_0	dielectric constant $(= 8.854 \cdot 10^{-12} F/m)$
ε	permitivity
$\gamma = \alpha + j\beta$	complex propagation coefficient
Γ	reflection coefficient
$\Gamma^\star$	complex conjugate reflection coefficient

Γ_S	reflection coefficient for input
$\Gamma_{S,opt}$	noise optimal source reflection coefficient
ρ	electrical resistivity
σ	electrical conductivity
b	stability measure
BV_{CBO}	base-collector breakdown voltage
BV_{CEO}	base-emitter breakdown voltage
c_0	speed of light ($= 3 \cdot 10^8 m/s$)
F	noise figure
f_{max}	maximum frequency of oscillation
F_{min}	minimum noise figure
f_t	transit frequency
G	gain
G_T	transducer power gain
G_P	power gain
G_A	available power gain
g_m	transconductance
I_C	collector current
λ	wavelength
A_0	loss
C_0	capacitance per unit length
R_0	resistance per unit length
L_0	inductance per unit length
G_0	conductance per unit length
Q	quality factor
E_{store}	energy stored per cycle

E_{diss}	energy dissipated per cycle
δ	skin depth
ω	angular frequency
μ	permeability of the material
σ	conductivity of the material
IIP_3	$3^{rd} - order$ input intercept point
OIP_3	$3^{rd} - order$ output intercept point
IP_3,IP_5	3^{rd},5^{th}-order intercept point
k	stability factor
P_{diss}	dissipated DC power
P_{1dB}	1 dB compression point
S_{11}	input reflection coefficient
S_{12}	reverse isolation coefficient
S_{21}	transmission coefficient
S_{22}	output reflection coefficient
SNR	signal to noise ratio
V_a	Early-voltage
V_T	thermal voltage
Z_0	characteristic impedance
Z	complex impedance
$Z^\star$	complex conjugate impedance

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