

# **GaN HEMT Modeling Including Trapping Effects Based on Chalmers Model and Pulsed S-Parameter Measurements**

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*To my mother, my father, my wife, and my baby princess*

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# Abstract

Although GaN HEMTs are regarded as one of the most promising RF power transistor technologies thanks to their high-voltage high-speed characteristics, they are still known to be prone to trapping effects, which hamper achievable output power and linearity. Hence, accurately and efficiently modeling the trapping effects is crucial in nonlinear large-signal modeling for GaN HEMTs.

This work proposes a trap model based on an industry standard large-signal model, named Chalmers model. Instead of a complex nonlinear trap description, only four constant parameters of the proposed trap model need to be determined to accurately describe the significant impacts of the trapping effects, e.g., drain-source current slump, typical kink observed in pulsed I/V characteristics, and degradation of the output power. Moreover, the extraction procedure of the trap model parameters is based on pulsed S-parameter measurements, which allow to freeze traps and isolate the trapping effects from self-heating. The model validity is tested through small- and large-signal model verification procedures. Particularly, it is shown that the use of this trap model enables a dramatical improvement of the large-signal simulation results.

AlGaIn/GaN HEMT, modeling, pulsed S-parameter measurements, trapping effects, drain-lag

# Zusammenfassung

Obwohl GaN HEMTs wegen ihrer hohen Durchbruchspannungen und ihrer hohen Driftsättigungsgeschwindigkeit als eine der vielversprechendsten HF-Leistungstransistortechnologien angesehen werden, ist bekannt, dass sie anfällig für Trappingeffekte sind. Diese verschlechtern die erzielbare Ausgangsleistung und die Linearität. Folglich ist die genaue und umfassende Modellierung dieser Trapping-Effekte entscheidend für ein gutes nichtlineares Großsignalmodell der GaN HEMTs.

In dieser Arbeit wird ein Trap-Modell vorgestellt, das auf dem Chalmers Modell beruht, einem allgemein in kommerzieller Entwurfssoftware verfügbaren Großsignalmodell für Transistoren. Anstelle einer komplizierten nichtlinearen Trap Modellierung müssen im von mir vorgeschlagenen Modell nur vier Parameter zur Beschreibung der wesentlichen Trap-Wirkungen bestimmt werden. Trap-Wirkungen sind hier Drain-Source-Strom-Abfall, Abknicken der gepulst gemessenen Ausgangskennlinie und Verschlechterung der Ausgangsleistung. Die Extraktion der Trap-Modell-Parameter stützt sich auf gepulst gemessene S-Parameter. Dadurch wird der Trap-Zustand bei der Messung eingefroren und Selbsterwärmung vermieden. Die Gültigkeit des Modells wird anhand von Klein- und Großsignalmessungen überprüft. Speziell wird hier gezeigt, dass durch die Verwendung meines Trap-Modells die Großsignal-Simulationsergebnisse deutlich verbessert werden.

AlGaN/GaN HEMT, Modellierung, gepulste S-Parameter Messungen, Trapping-Effekte, Drain-Lag

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# Chapter 1

## Introduction

Gallium Nitride high electron mobility transistors (HEMT) utilize high-density two-dimensional electron gas (2DEG) accumulated in the boundary layer between GaN and AlGa<sub>N</sub> through their piezoelectric effect and natural polarization effect [1]. This makes it possible to realize a high current density and a high saturation voltage as its main transistor characteristics. Combined with its other characteristics, such as high power, low noise, and a high breakdown voltage, those outstanding characteristics make it ideal for high-power, high-frequency, low noise applications [2–4], e.g., in high-power amplifiers and LNA [5–9]. Furthermore, GaN HEMT has also shown great potential in extreme operation environments, e.g., high/low temperature operation conditions, which actually have a strong impact on the electrical performance of devices [10, 11]. Hence, despite that the technology of GaN HEMT is not as well understood as the previously adopted devices, e.g., GaAs HEMT, the development of its commercial production never stopped.

However, this puts the circuit designers in a very awkward position: on one hand, they are attracted to the outstanding characteristics of GaN HEMTs, and many of them actually have already benefited from the use of GaN HEMTs in their designs. On the other hand, the demand for accurate GaN HEMT models is still pressing, as they are still not fast enough to be used in most circuit simulators.

During the past years, many large-signal models for GaN HEMTs in different types were developed to characterize their large-signal behavior [12–15]. However, high modeling accuracy can be considered to be quite close to be guaranteed in the academic world, but still far away from being accessible to circuit designers. This is mainly due to the anomalies of GaN HEMTs caused by dispersion effects [16–18],

which are still the key issues in the modeling community.

In the following, different types of large-signal models will be first discussed and compared. Next, the challenges of the GaN HEMT modeling will be presented in detail. Finally, a brief review of the whole work will be addressed.

## 1.1 Large-Signal Model Types

Large signal models normally fall into two main types:

### 1. Physical models

These models use the parameters based upon device properties, such as gate width, gate length, and thickness of layers, or upon physical data, such as carrier transport properties and the device geometry, in order to solve physics equations that describe the device characteristics, e.g., current, voltage, power, etc [19–23].

### 2. Empirical models

This type of model is entirely based upon curve fitting. This means the parameters of these models are normally determined by fitting the equations to the measured data through mathematical optimization.

Considering the shortcomings of traditional empirical model, such as non-physical nature and too many fitting parameters, which are often difficult to be understood and extracted, physical models show their advantages due to its inherent superiority such as explicit physical implication and unified expression to describe all the regions of device operation [24–27].

Compared with physical models, the empirical large-signal equivalent circuit model is simpler and easier to be implemented in commercial simulators and has been widely used in circuit design [28]. Basically, the nonlinear empirical models are generated with nonlinear functions that could account for the current flow (I/V functions) and the charge dynamic variation. They are also able to describe the device physical phenomena as long as the model parameters are linked to physical effects. However, the modeling accuracy strongly depends on the accuracy of the measurements, and the adequacy of the model formulation. Moreover, these models can also be constructed based upon a lookup table developed from the measured



data, and therefore are called “table-based models” [29–31]. Moreover, recently, a new type of empirical models has been presented, which utilizes artificial neural network, or AAN [32–35].

In this work, a well known empirical model, i.e., the Chalmers (Angelov) non-linear model [36], has been adopted, as it is one of the frequently used GaN HEMT models. Its parameter extraction techniques have been already researched and developed in the last years [37–39], e.g., its drain current model’s parameters can be directly extracted by simple inspection of the experimental DC I/V and  $g_m$  characteristics, in this way. the model can accurately predict not only  $I_{ds}$  but also its derivatives. However, for GaN HEMTs, the drain current model is more complex than that for Si or GaAs devices [36], since the model should also include the functions to account for the trapping effects that GaN HEMTs encounter under working conditions. The details will be addressed in next section.

## 1.2 GaN HEMT Modeling Challenges

As mentioned previously, GaN HEMT offer outstanding characteristics, that attracts more and more circuit designers. However, at the same time, its models suffer from the electrical anomalies of the GaN HEMT induced by the trapping effects. The trapping effects can normally be split into two groups: drain-lag effects are caused by the charge capture and emission processes of the donor traps in the buffer layers below the 2DEG and gate-lag effects are mainly due to the presence of negative charges trapped on the semiconductor surfaces of the epitaxial layers above the 2DEG [40]. Gate-lag effects in recent AlGaIn/GaN technology have been significantly reduced by passivation and field plate. For some devices, e.g., in our case, gate-lag effects are so weak, that it is almost impossible to distinguish between gate-lag effects and thermal effects even by means of pulsed measurements [41]. Hence, drain-lag effects remain the main trap phenomena. Since static DC I/V measurements without separating trapping effects can lead to inaccurate RF models [42],[43], it is important to include these effects in the transistor large-signal models to describe the transistor’s RF behavior accurately.

From a view of DC/pulsed I/V characteristic prediction, a drain-lag model worth its salt would have the following abilities: First, it should be able to describe the drain-source current slump, which is known as the knee-walkout [17]. Furthermore,

the typical kink observed in pulsed I/V curves should also be described, which is mainly due to the asymmetry in time constants associated with capture and release of charge traps [44].

On the other hand, it is reported that the transconductance dispersion is mainly related to gate-lag effects [45], while output conductance dispersion is mainly related to the drain-lag effects [46]. Hence, the drain-lag model is also supposed to be able to provide a correction term  $\Delta G_{ds}$  to account for the difference between the output conductance  $G_{ds}$  extracted from small-signal RF characteristics ( $G_{ds,RF}$ ) and that obtained from DC I/V characteristics ( $G_{ds,DC}$ ) [47]. The use of the drain-lag model without this correction term could result in a mismatch in predicting the real part of  $S_{22}$ , which is basically influenced by the output conductance  $G_{ds}$ .

In the last decade, a significant interest on modeling drain-lag effects can be observed within the microwave community. As a result, various trap models [47–52] have been published. However, until now, none of them was available in commercial EDA tools. There are two main reasons here: on the one hand, some models are of little use to describe some impacts of drain-lag effects, e.g., Jarndal et al. [47] proposed a drain-lag model which cannot account for the difference between emission and capture time constants. On the other hand, some drain-lag models are most accurate since they are able to fully predict the impact of trapping effects on nonlinear device performance. However, the parameters of these models have proven to be too complicated to be extracted, e.g., Jardel and Quéré et al. [44, 48] developed a drain-lag model (in this work it is called Quéré drain-lag model), but no publication so far exactly addresses the question how to describe the values of the trap-related parameter  $k$  employed in this drain-lag model, as it is only assumed to be a linear function of  $v_{gs}$  for reasons of simplicity in [44, 48].

In this work, first of all, a simple drain-lag model, named parameter-scaling drain-lag model [49], is proposed. This drain-lag model is able to predict device performance well for various trap states. It relies on scaling of model parameters with quiescent drain voltage which yields convenient parameter extraction. Another benefit of this model is that it reduces to the standard Chalmers model with optimized parameters for fixed drain bias. However, it is of little use in describing the typical kink around the quiescent drain voltage from pulsed I/V curves or predicting the RF output conductance under large-signal condition. Thus, the Quéré drain-lag model was integrated to overcome these drawbacks. This drain-lag model employs

a pseudo gate-source voltage at the input of the current source. The pseudo gate-source voltage is related to a fitting parameter  $k$ , which is linked to the amplitude of traps and is assumed to be a linear function of  $v_{gs}$ . However, it is shown that, instead of the complicated expression of parameter  $k$  as presented in Quéré drain-lag model, a constant value should yield the same modeling performance if combined with the parameter-scaling drain-lag model. This can significantly simplify the model parameters extraction process.

### 1.3 Outline of the Thesis

This thesis is structured as follows:

**Chapter 1** describes the objective of this thesis and the motivation behind performing this research. The state of art of the GaN HEMT trap models is briefly reviewed and the associated problems due to their inaccuracy and complexity are summarized.

In **Chapter 2**, at first, a brief overview of the structure and operation of Al-GaN/GaN HEMT is given in order to provide the physical background of the main behaviors to be modeled. Next, a detailed description of the proposed GaN HEMT modeling strategy is presented. Finally, the physical mechanisms of the trapping effects are introduced, and the advantages and drawbacks of the published trap models are clarified.

**Chapter 3** presents the principle and set up of the used multi-bias pulsed S-parameter measurements. Moreover, the main characteristics of pulsed measurements are discussed.

The GaN HEMT modeling relying on the pulsed S-parameter measurements is covered in **Chapter 4**. The impact of the use of the pulsed S-parameter measurements on the extraction of extrinsic parameters and intrinsic capacitances of small-signal model is presented in the first section of this chapter. The second part shows that better large-signal models can be extracted by using the multi-bias pulsed S-parameter measurements.

**Chapter 5** addresses a novel drain-lag model to account for trapping effects in the large-signal description of GaN HEMTs. The model formulations are presented and reasoned, and the methods to determine the model parameters are explained. However, significant discrepancies are observed when verifying the model with

pulsed S-parameters. The reason for this drawback is discussed in detail at the end of the chapter.

A solution to overcome this drawback is presented in **Chapter 6**. The modeling accuracy and the reliability of the extraction results are verified by comparison of small- and large-signal simulations with measurement data.

General conclusions and required improvements in future work are discussed in **Chapter 7**.

# Chapter 2

## GaN HEMT Modeling Strategy

The significant progress made on technology of GaN HEMTs for the last years makes them usable in many different areas where e.g., high power and high frequency are needed, and they seem to be able to replace several existing semiconductor technologies, e.g., GaAs, Si, and SiC devices, in these areas [53]. With this rapid development a need of accurate large-signal models for GaN HEMT is pressing, since these models are the key elements to simulate the circuits in commercial EDA tools.

In Section 1, the fundamentals of technology, structure, and basic operation of GaN HEMTs will be discussed in detail. This background information is very important for the accurate device modeling.

The proposed modeling strategy in this thesis can be split in two stages: small- and large- signal modeling. Section 2 introduces the extraction process of the small-signal equivalent circuit parameters, which has become well published for HEMTs or FETs in some references [54–56].

Section 3 will address the next issue after small-signal modeling: Large-signal modeling. The Chalmers (Angelov) model [36–39] was applied here, as it is a frequently used and well-known GaN HEMT model.

Section 4 discusses the state-of-the-art dispersive effect modeling strategy of GaN HEMTs. As mentioned in Chapter 1, dispersion effects, also known as memory effects, not only hamper the achievable output power and linearity of HEMTs, but also significantly influence the modeling accuracy. Therefore, much effort has been devoted to understand and model them.

## 2.1 AlGaN/GaN HEMT

GaN HEMTs have reached the commercialization phase and are already available from a number of companies, since these devices have shown several outstanding properties such as high power, low noise, high efficiency, etc. These properties enable to make the design of power amplifiers more efficient, compact, easier, and reliable.

In this section, a brief review of vital characteristics, e.g., structure and technology, and basic operation of GaN HEMTs is presented.

### 2.1.1 AlGaN/GaN HEMT Structure

A detailed description of the GaN HEMT processing technology is beyond the purpose of this thesis but a brief introduction of the GaN HEMT structure would be helpful in understanding the performance of GaN HEMTs.

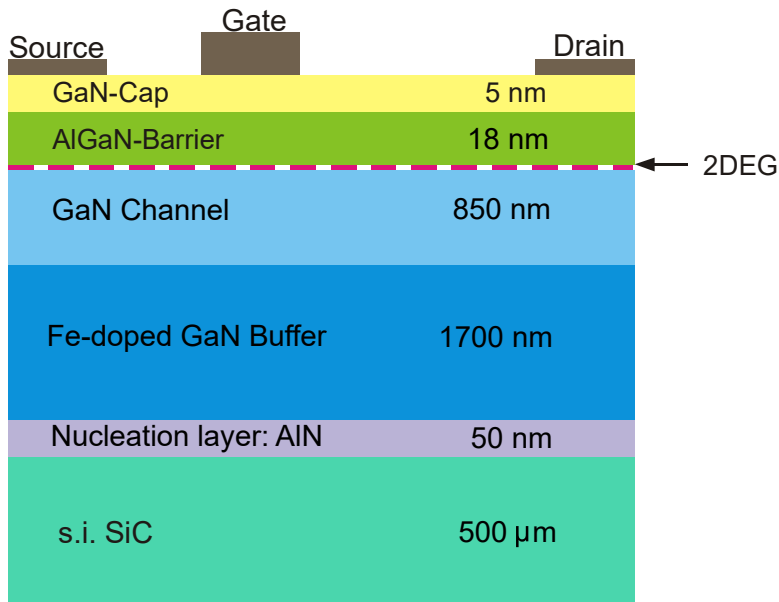


Figure 2.1: The structure of modeled AlGaN/GaN HEMT in this thesis.

The basic concept in a HEMT is the aligning of a wide and narrow bandgap semiconductor adjacent to each other to create a heterojunction. In AlGaN/GaN HEMTs, the carriers from a wide energy gap material (AlGaN) diffuse to the narrow bandgap material (GaN) where a dense two-dimensional electron gas (2DEG as shown in Fig. 2.1) is formed on the GaN side close to the boundary with the AlGaN

[57]. The high sheet charge density of the 2DEG in AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT combined with the high saturation velocity in the undoped Ga<sub>N</sub> is one of its peculiar useful properties for providing high current densities.

Fig. 2.1 shows the basic structure of modeled AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT in this thesis. As seen in this figure, SiC is used as substrate [58]. It is one of the best choices for high power applications due to its good thermal performance. In our case, the substrate provides an excellent thermal conductivity of 3.5 W/cm. Besides, sapphire ( $Al_2O_3$ ) or silicon (Si) are also an option for substrate. They are relatively inexpensive but have worse thermal conductivity.

The epitaxial growth of the transistor structure starts with the deposition of a 50 nm thick AlN nucleation layer upon the substrate to reduce the lattice mismatch when growing the Ga<sub>N</sub> layer on the SiC substrate [59]. A 1.7  $\mu$ m thick Fe-doped Ga<sub>N</sub> layer and a 850 nm undoped Ga<sub>N</sub> layer are then deposited to provide free charge carriers and to increase the electron mobility, respectively. These Ga<sub>N</sub> layers are followed by a 18 nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier layer. Finally, the whole structure is capped with a 5 nm thick Si-doped Ga<sub>N</sub> layer ( $2 \times 10^{18} \text{ cm}^{-3}$ ) to increase the effective Schottky barrier, which improves the breakdown characteristics and decreases the gate leakage [60].

To summarize, as shown in Fig. 2.1, the AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT structure used in this thesis consists of 50 nm AlN nucleation layer, 1.7  $\mu$ m Fe-doped Ga<sub>N</sub> buffer layer, 850 nm Ga<sub>N</sub> layer, 18 nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier layer, and 5 nm Ga<sub>N</sub> cap layer on a 500  $\mu$ m thick semi-insulating SiC substrate.

### 2.1.2 Basic AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT Operation

The structure of AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT takes the advantage of superior transport properties of electrons in a potential well of lightly doped semiconductor material. A simplified AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT structure is presented in Fig. 2.2.

As shown in this figure, a doped or undoped wide energy gap material (AlGa<sub>N</sub>) lies on the narrow bandgap material (Ga<sub>N</sub>). This results in a sharp dip in the conduction band edge at the AlGa<sub>N</sub>/Ga<sub>N</sub> interface as shown in the band diagram of the structure in Fig. 2.2(b). This leads to a high carrier concentration in a narrow region, called a quantum well, along the hetero interface. The distribution of electrons in the quantum well can be considered as two-dimensional instead of three-dimensional due to its very small thickness. Therefore, the charge density is termed the 2DEG

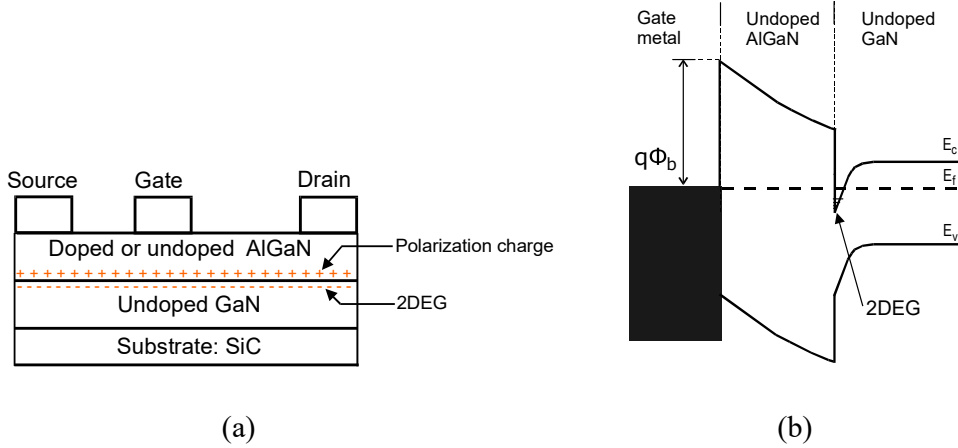


Figure 2.2: (a) basic configuration of AlGaIn/GaN HEMT, (b) band diagram [81].

and quantified in terms of sheet carrier density ( $n_s$ ).

What is to notice is that, unlike in AlGaAs/GaAs HEMT, a 2DEG is able to be formed at the AlGaIn/GaN interface even when the wide energy gap material (AlGaIn) is undoped. This is mainly due to the presence of a strong polarization field across the AlGaIn/GaN heterojunction. In this way, a 2DEG with the sheet carrier density up to  $10^{13} \text{ cm}^{-2}$  can be achieved without any doping [1]. As the surface states act as a source of electrons in 2DEG [61], the band diagram and the electron distribution of the AlGaIn/GaN heterostructure are changed by the built-in static electric field in the AlGaIn layer induced by spontaneous and piezoelectric polarization. Hence, a number of electrons transfer from the surface states to the AlGaIn/GaN interface, leading to a 2DEG with high density.

## 2.2 GaN HEMT Small-Signal Modeling

The first phase in the determination of a HEMT model is the extraction of the extrinsic and intrinsic parameters shown in Fig. 2.3, a standard small signal equivalent circuit for GaN HEMTs, which is inherited from models of GaAs FETs and can also represent the effects found in GaN devices. The linear model extraction is a critical step since this model will lay the initial foundation for the modeling accuracy of final nonlinear model. Direct extraction techniques for determining the small-signal equivalent circuit parameters from S-parameter data have become well known in recent years for FETs and HEMTs [54–56]. In this thesis, the extrinsic parameters will



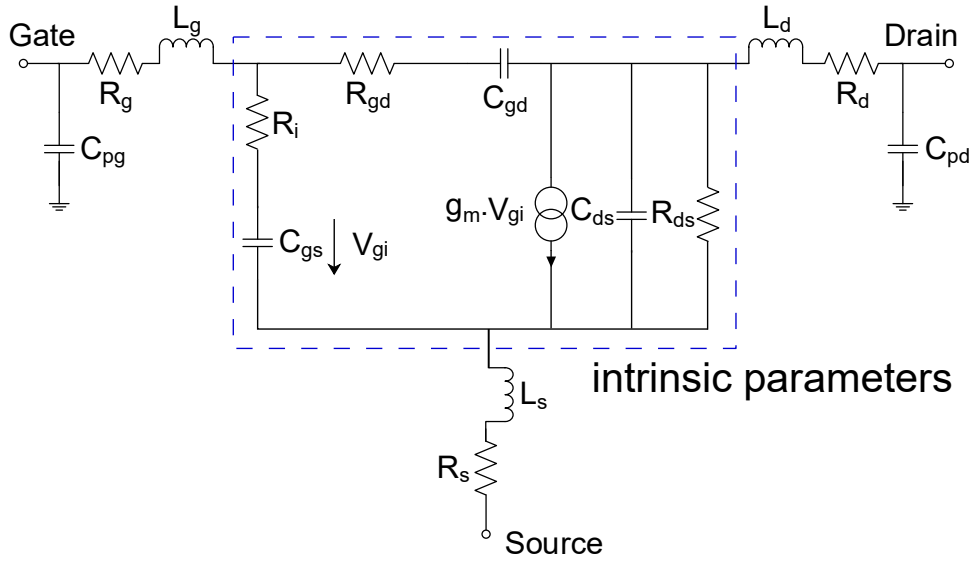


Figure 2.3: Small signal equivalent circuit for GaN HEMTs

be determined by using cold-FET S-parameter data [56]. The small-signal model is then completed with the calculation of its intrinsic parameters, using S-parameters measured at active bias points.

### 2.2.1 Extrinsic Parameter Extraction

The basic procedures for extrinsic parameters ( $R_g$ ,  $R_d$ ,  $R_s$ ,  $L_g$ ,  $L_d$ ,  $L_s$ ,  $C_{pg}$ ,  $C_{pd}$ ) extraction require zero drain voltage S-parameter measurements (cold FET condition) with the gate in forward conduction or with the channel pinched off. Under the cold FET condition, the voltage-controlled drain-source current can be neglected. Moreover, using the mentioned two gate bias conditions allows a further simplification of the equivalent circuit by excluding some elements, thereby reducing the number of unknowns.

The extrinsic parameter extraction can be split in two stages: Capacitance extraction on the one side and inductance and resistance extraction on the other side. All extraction results in the following sections are performed with a  $250 \mu\text{m}$  wide HEMT, manufactured in a  $0.25 \mu\text{m}$  GaN-on-SiC process at the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik.

#### A): Capacitances ( $C_{pg}$ , $C_{pd}$ ) extraction

Setting  $v_{ds}$  to zero and  $v_{gs}$  below pinch-off voltage simplifies the equivalent circuit

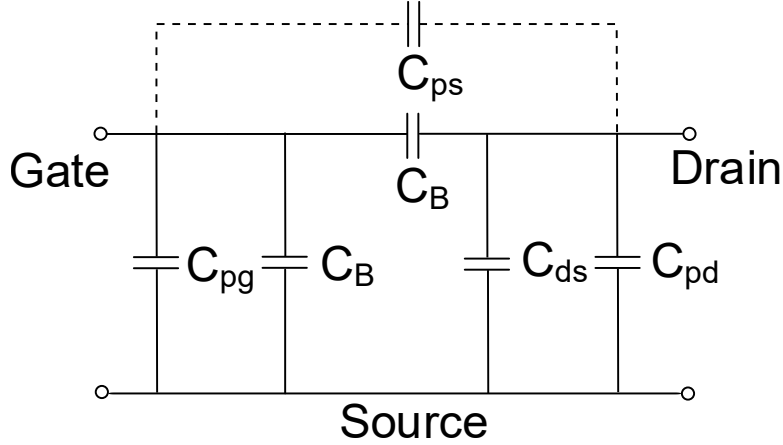


Figure 2.4: Simplified equivalent circuit for GaN HEMTs at  $v_{ds} = 0$  V,  $v_{gs} < V_{pinchoff}$

as illustrated in Fig. 2.4, since the internal transistor shows a very high impedance and can be described with capacitances only. Moreover, since  $v_{ds} = 0$  V, the field under the gate is symmetric. The simplified equivalent circuit now results in the following equation:

$$\begin{aligned}
 \text{Im}(Y_{11}) &= j\omega(C_{pg} + 2C_B + C_{ps}) \\
 \text{Im}(Y_{12}) = \text{Im}(Y_{21}) &= -j\omega(C_B + C_{ps}) \\
 \text{Im}(Y_{22}) &= j\omega(C_{pd} + C_{ds} + C_B + C_{ps})
 \end{aligned} \tag{2.1}$$

where  $C_B$  represents the fringing capacitance or depletion region under the gate extending into the channel,  $C_{ps}$  is the extrinsic feedback capacitance and can be neglected for considered FETs. It is evident, that  $C_{pg}$  can be then calculated from the slope of the  $\text{Im}(Y_{11} + 2Y_{12})$  versus  $\omega$  as:

$$C_{pg} = \frac{\text{Im}(Y_{11} + 2Y_{12})}{\omega} \tag{2.2}$$

In order to determine  $C_{pd}$ ,  $C_{ds}$  must be lumped in with  $C_{pd}$ . Hence, an additional condition (e.g., the ratio between  $C_{ds}$  and  $C_{pd}$ ) should be needed. In references [56] and [62] two different extraction algorithms are published and can be found in the following equations:

$$\text{Dambrine}[56] \quad C_{ds} = 0 \quad \Rightarrow \quad C_{pd} = \frac{\text{Im}(Y_{22} + 2Y_{12})}{\omega} \tag{2.3}$$

$$\text{Tayrani}[62] \quad C_{ds} = 4C_{pd} \quad \Rightarrow \quad C_{pd} = \frac{\text{Im}(Y_{22} + 2Y_{12})}{5\omega} \tag{2.4}$$

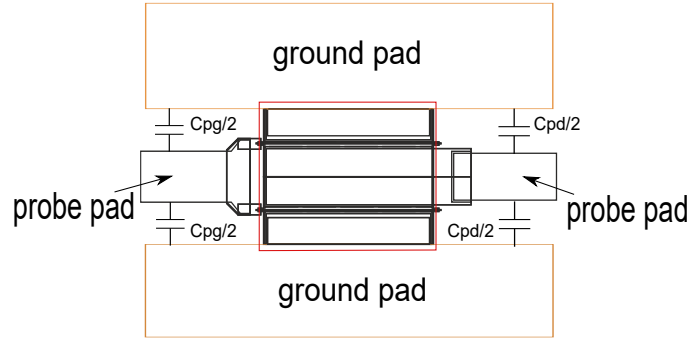


Figure 2.5: The layout of AlGaIn/GaN HEMT with 2 finger.

However, these extraction assumptions are not based on physical effects. What is to notice is that, the pad capacitances ( $C_{pg}$  and  $C_{pd}$ ) are established by the probe pad configuration. As shown in Fig. 2.5, the probe pads, which are connected with the gate and the drain, respectively, have almost the same length, width and distance to the ground pad. Therefore, this enables the usage of an approximation that might simplify the extraction effort [63]:

$$C_{pd} \approx C_{pg} \quad (2.5)$$

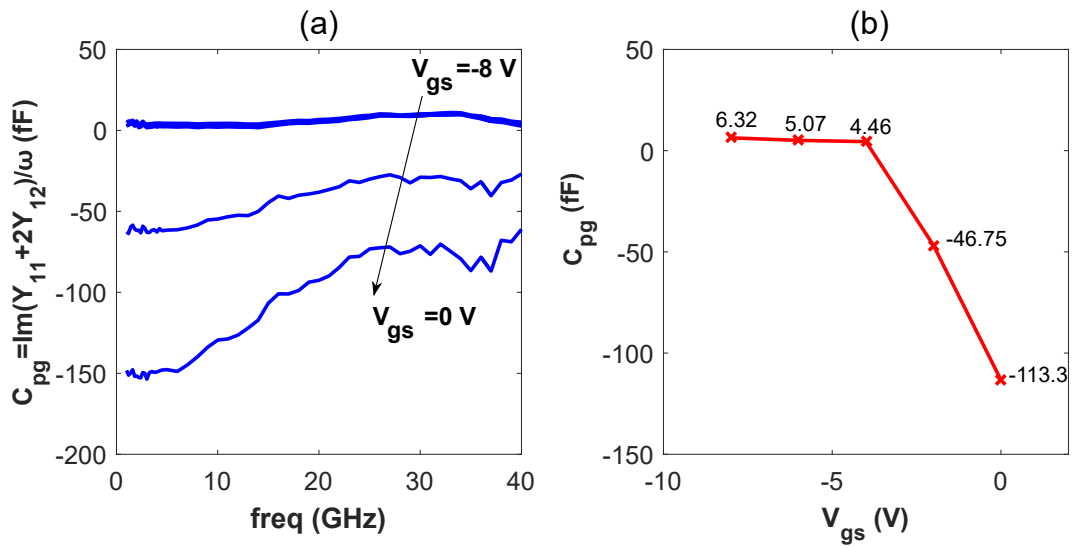


Figure 2.6: Extraction result of extrinsic capacitance  $C_{pg}$  for a 250  $\mu$ m GaN HEMT by using pinch-off S-parameters at different frequencies and different gate bias voltages.

Fig. 2.6 shows the  $C_{pg}$  extraction result for a 250  $\mu\text{m}$  GaN HEMT based on Equation (2.2) at different gate bias voltages for frequency from 400 MHz to 40 GHz. The result illustrates that a smooth and reliable extraction can be performed at the far pinch-off region.

### B): Inductances ( $L_g, L_d, L_s$ ) extraction

The cold FET S-parameters measured at  $v_{ds} = 0$  and  $v_{gs} > 0$  were used to determine the inductances ( $L_g, L_d, L_s$ ). In this condition the parallel capacitors  $C_{pg}$ ,  $C_{pd}$  and  $C_{ds}$  can be neglected, since the transistor is in a low-resistance state if the Schottky diode is conducting. Fig. 2.7 shows the simplified equivalent circuit [64], and the following equations can be concluded:

$$\begin{aligned} Z_{11} &= R_g + R_s + \frac{R_c}{2} + j\omega L_g + j\omega L_s + \frac{R_j}{1 + j\omega C_j R_j} \\ Z_{12} = Z_{21} &= R_s + \frac{R_c}{2} + j\omega L_s \\ Z_{22} &= R_c + R_d + R_s + j\omega L_s + j\omega L_d \end{aligned} \quad (2.6)$$

where  $R_c$  is the channel resistance,  $R_j$  and  $C_j$  represent the differential resistance and capacitance of the Schottky barrier, respectively. And now considering the gate

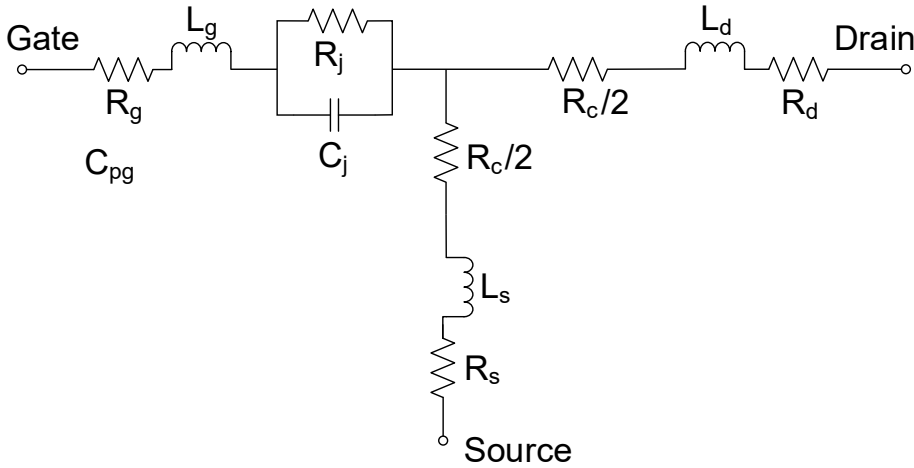


Figure 2.7: Simplified equivalent circuit for GaN HEMTs at  $v_{ds} = 0$  V,  $v_{gs} > 0$  V.

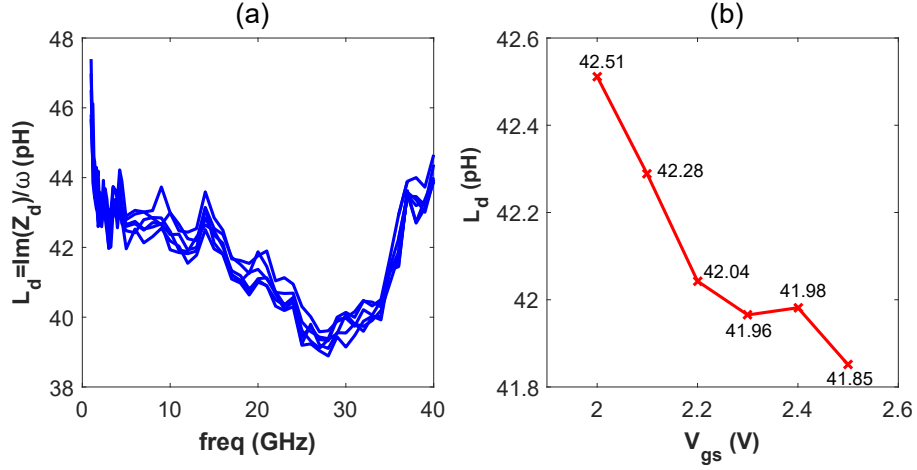


Figure 2.8: Extraction result of extrinsic inductance  $L_d$  for a 250  $\mu\text{m}$  GaN HEMT by using “cold” S-parameters under gate-forward condition.

$Z_g$ , source  $Z_s$ , and drain  $Z_d$  branch impedances, the following equations were used in the extraction of extrinsic inductances:

$$\begin{aligned} Z_g &= Z_{11} - Z_{12} = R_g + j\omega L_g + \frac{R_j}{1 + j\omega C_j R_j} \\ Z_s &= Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \\ Z_d &= Z_{22} - Z_{12} = R_d + \frac{R_c}{2} + j\omega L_d \end{aligned} \quad (2.7)$$

It is evident that the inductances except  $L_g$  can be obtained by using the imaginary part of the Z-matrix, which can be simply obtained by converting the S-matrix:

$$L_d = \frac{\text{Im}(Z_d)}{\omega} \quad (2.8)$$

$$L_s = \frac{\text{Im}(Z_s)}{\omega} \quad (2.9)$$

Fig. 2.8(a) presents the shape of  $\text{Im}(Z_d)$  versus  $\omega$  under gate-forward condition, namely the extraction results for  $L_d$ . Fig. 2.8(b) illustrates the estimated values of  $L_d$  at each gate voltage, and an almost constant value (around 42.2 pH) can be finally obtained.

For  $L_g$ , under the condition of low frequency and high gate forward bias the

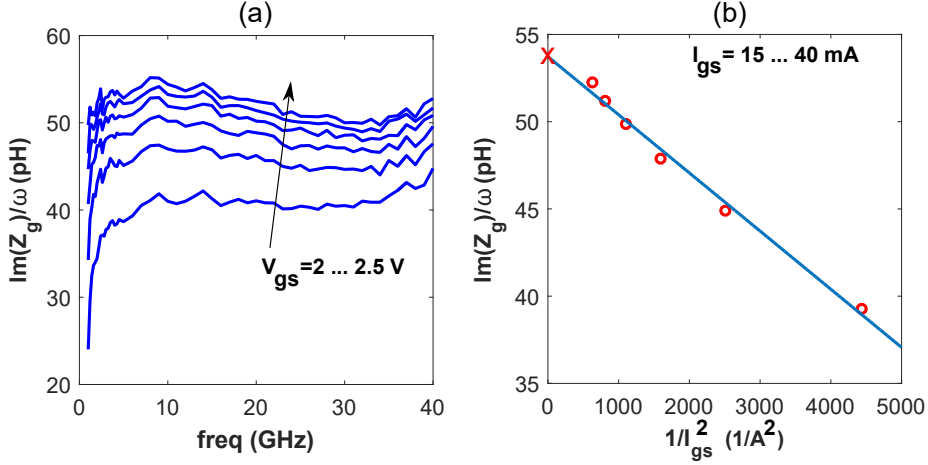


Figure 2.9: Extraction result of extrinsic inductance  $L_g$  for a 250  $\mu\text{m}$  GaN HEMT by using “cold” S-parameters under gate-forward condition.

following equations results:

$$(\omega R_j C_j)^2 \ll 1$$

$$R_j = \frac{R_{j0}}{I_{gs}}$$

And the imaginary part of  $Z_g$  can be now simplified as following:

$$\begin{aligned} \text{Im}(Z_g) &= \omega \left( L_g - \frac{C_j R_j^2}{1 + (\omega C_j R_j)^2} \right) \\ &\approx \omega (L_g - C_j R_j^2) \\ &\approx \omega \left( L_g - C_j \frac{R_{j0}^2}{I_{gs}^2} \right) \end{aligned} \quad (2.10)$$

Therefore,  $L_g$  can be identified with the plot of  $\text{Im}(Z_g)/\omega$  versus  $1/I_{gs}^2$ . Fig. 2.9 shows the  $L_g$  extraction results based on Equation (2.10). It is evident that the values of the imaginary part of  $Z_g/\omega$  shown in Fig. 2.9(a) in the frequency range from 5 GHz to 40 GHz are rather constant, and these values were next applied to approximate a straight line against  $1/I_{gs}^2$  as shown in Fig. 2.9(b). The intersection point with the y-axis provides the extracted value for  $L_g$ .

As shown in Fig. 2.5, the probe pads connected to the gate and drain have almost the same length. Hence, the contribution of probe pads to the extracted values of

gate and drain inductances ( $L_g$  and  $L_d$ ) is almost same. However, for 2 finger transistor, the probe pad is connected with 2 gate terminals at one side, and at another side the probe pad is connected with only one drain terminal. This makes  $L_g$  larger than  $L_d$ .

### C): Resistances ( $R_g, R_d, R_s$ ) extraction

The same bias conditions used in the inductance extraction were also adopted in the resistance extraction procedure. However, the chosen frequency should be low enough to overcome the capacitance of the Schottky diode, so that the influence of  $C_j$  can be neglected. Therefore, the real part of  $Z_g$  can be simply rewritten as following:

$$\begin{aligned} \text{Re}(Z_g) &= R_g + R_j \\ &\approx R_g + \frac{R_{j0}}{I_{gs}} \end{aligned} \quad (2.11)$$

This simplified equation illustrates that  $R_g$  can be determined from the plot of  $\text{Re}(Z_g)$  versus  $1/I_{gs}$ .

Fig. 2.10(a) illustrates the shape of real part of  $Z_g$  converted from a cold-FET S-parameter measurements at different gate conditions. The values in the frequency range from 1 GHz to 40 GHz were next supplied to approximate a straight line over

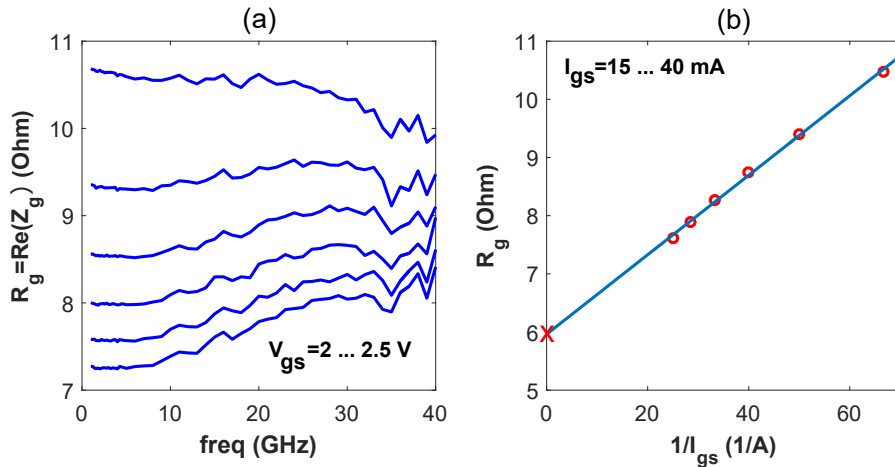


Figure 2.10: Extraction result of extrinsic resistance  $R_g$  for a 250  $\mu\text{m}$  GaN HEMT based on Equation (2.11).

$1/I_{gs}$  as shown in Fig. 2.10(b). The extracted value of  $R_g$  can then be noted from the y-intercept of this line.

The extraction of  $R_d$  and  $R_s$  can be more problematic due to the unknown resistance  $R_c$  in both  $Z_{12}$  and  $Z_{22}$ . In this thesis, to overcome the  $R_c$  problem we used the approximation published in reference [62] as following:

$$R_d = \text{Re}(Z_d) \quad (2.12)$$

$$R_s = \text{Re}(Z_s) \quad (2.13)$$

However, it has been found this approximation is accurate only for small devices when using TRL calibration [65].

## 2.2.2 Intrinsic Parameters Extraction

After extracting the extrinsic parameters, the bias dependent intrinsic parameters were determined based on the extracted extrinsic parameters and the multi-bias S-parameter measurement. The extracted extrinsic parameters were first used to de-embed the measured S-parameters to give “intrinsic S-parameters” at the intrinsic reference planes of the transistor. And the “intrinsic S-parameters” were next converted to Y-parameters, which were finally used to calculate the intrinsic parameters by using several expressions shown in the following.

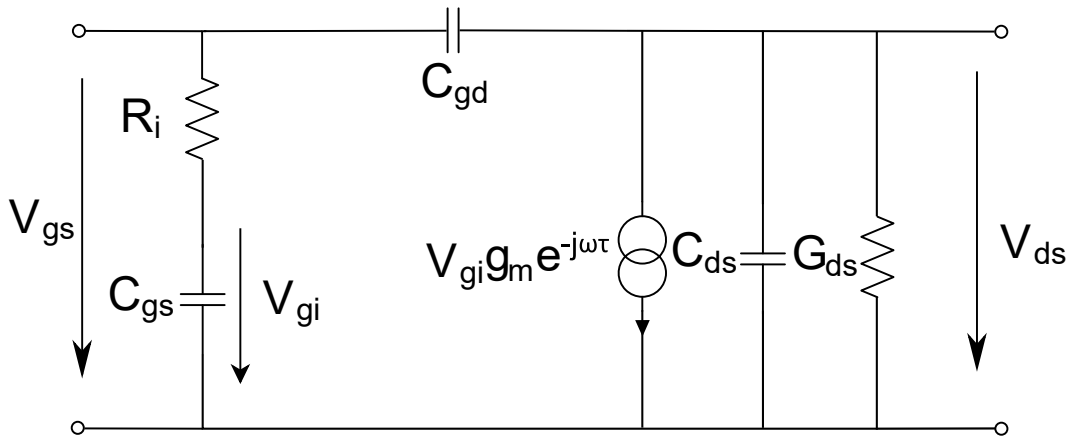


Figure 2.11: Simplified equivalent circuit for the intrinsic GaN HEMT in  $\Pi$ -topology.



Fig. 2.11 shows the equivalent circuit in  $\Pi$ -topology for the intrinsic HEMT, and this equivalent circuit can result in the following Y-parameters:

$$\begin{aligned}
 Y_{11} &= \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega \left( \frac{C_{gs}}{D} + C_{gd} \right) \\
 Y_{12} &= -j\omega C_{gd} \\
 Y_{21} &= \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \\
 Y_{22} &= \frac{1}{R_{ds}} + j\omega (C_{ds} + C_{gd}) \\
 D &= 1 + \omega^2 C_{gs}^2 R_i^2
 \end{aligned} \tag{2.14}$$

For low-noise devices,  $R_i$  and  $C_{gs}$  have small values at low frequencies, so that the approximation  $D = 1$  can be used in this Y-matrix [56]. Hence, the bias dependent values of the intrinsic elements ( $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $R_i$ ,  $G_{ds}$ ,  $g_m$ ,  $\tau$ ) can be simply calculated in selected frequency range using the following equations:

$$C_{gs} = \frac{Im(Y_{11} + Y_{12})}{\omega} \tag{2.15}$$

$$C_{gd} = \frac{Im(Y_{12})}{\omega} \tag{2.16}$$

$$C_{ds} = \frac{Im(Y_{22} + Y_{12})}{\omega} \tag{2.17}$$

$$R_i = \frac{1}{Re(Y_{11} + Y_{12})} \tag{2.18}$$

$$G_{ds} = Re(Y_{22}) \tag{2.19}$$

$$g_m = |(Y_{21} - Y_{12})(1 + j\omega R_i C_{gs})| \tag{2.20}$$

$$\tau = \frac{-\arg((Y_{21} - Y_{12})(1 + j\omega R_i C_{gs}))}{\omega} \tag{2.21}$$

Figs. 2.12 and 2.13 show the bias-dependency of the intrinsic parameters  $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $g_m$ ,  $G_{ds}$ , and  $\tau$  extracted by using multi-bias S-parameters within selected frequency ranges.

It has to be noted that the extracted values of intrinsic capacitances  $C_{gs}$ ,  $C_{gd}$ , and  $C_{ds}$  above  $v_{gs} = 0$  V will not be accounted for in the large-signal modeling, since the used large-signal model, namely the Chalmers model, can not take these values into account and the extracted values of intrinsic capacitances lack physical meaning to be used.

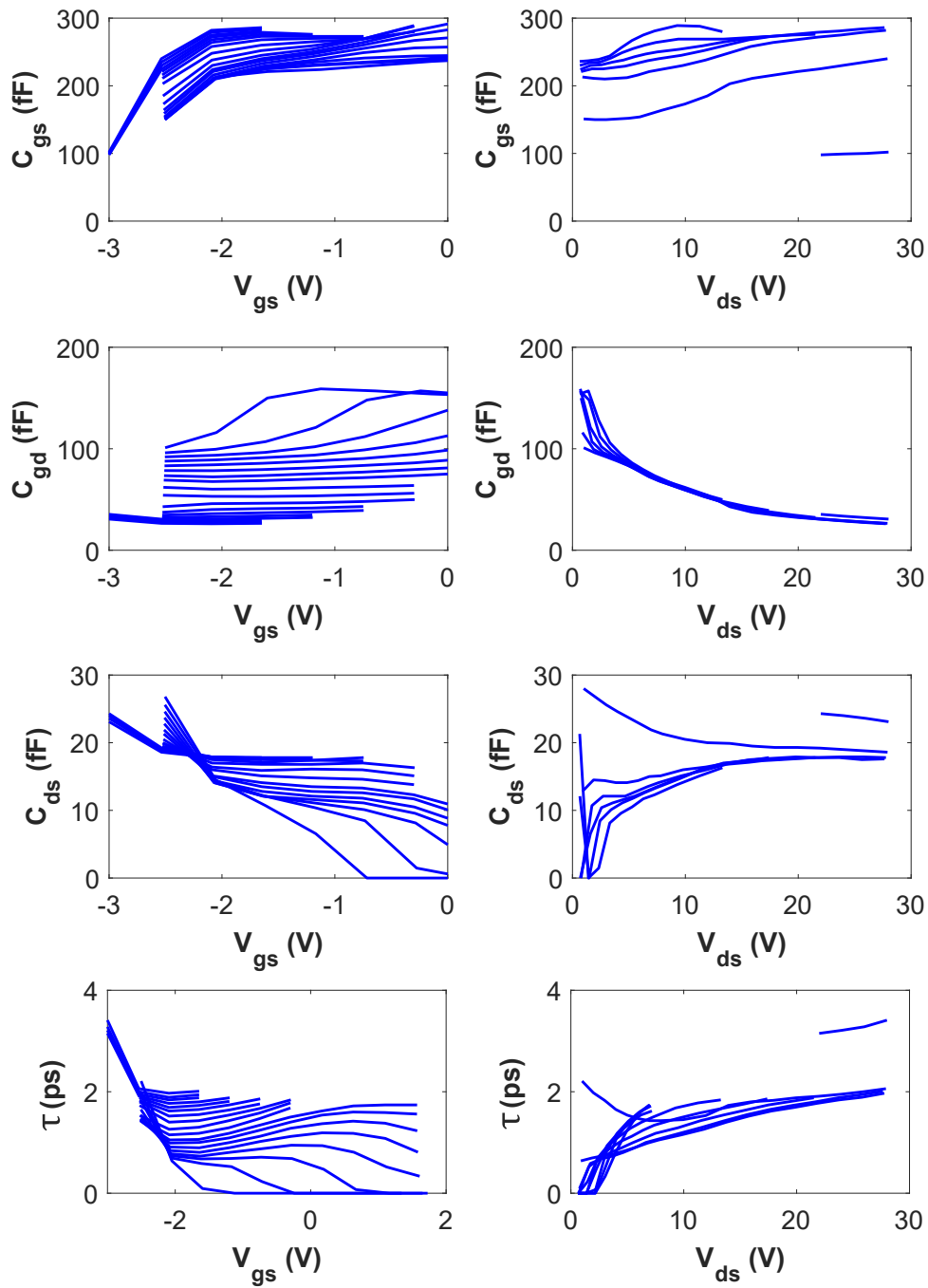


Figure 2.12: Extracted bias-dependency of intrinsic capacitances and  $\tau$  of the small-signal model for a 250  $\mu\text{m}$  GaN HEMT.

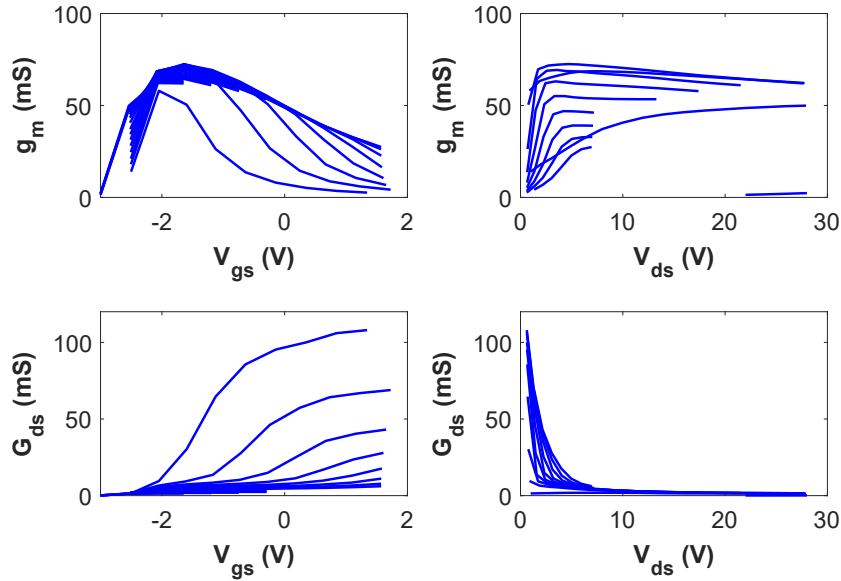


Figure 2.13: Extracted bias-dependency of intrinsic parameters  $g_m$ ,  $G_{ds}$  of the small-signal model for a  $250\ \mu\text{m}$  GaN HEMT.

## 2.3 GaN HEMT Large-Signal Modeling

For a GaN HEMT, its large-signal modeling can be split into several parts: the drain-source, gate-source, gate-drain current modeling, and nonlinear capacitances modeling. These parts can describe the main nonlinearities of the devices. However, the drain-source current represents the dominant and the most important nonlinearity, so its model is normally considered as the key issue in large-signal modeling procedure. Moreover, the drain-source current model also represents the DC and dynamic characteristics of the devices, which play a decisive role in predictions of small- and large-signal behavior of the devices.

When modeling the intrinsic currents and nonlinear capacitances, it should be noted that the extrinsic elements are already extracted as discussed in previous subsections. In this section, the proposed large-signal modeling procedure will be addressed. In this procedure, both the current ( $I(V,T)$ ) and nonlinear capacitance or charge ( $C(V,T)$  or  $Q(V,T)$ ) models were formulated with intrinsic voltages using the basic electrical equivalent circuit as shown in Fig. 2.14 and the parameters within these models were optimized by using the bias dependent small-signal model.

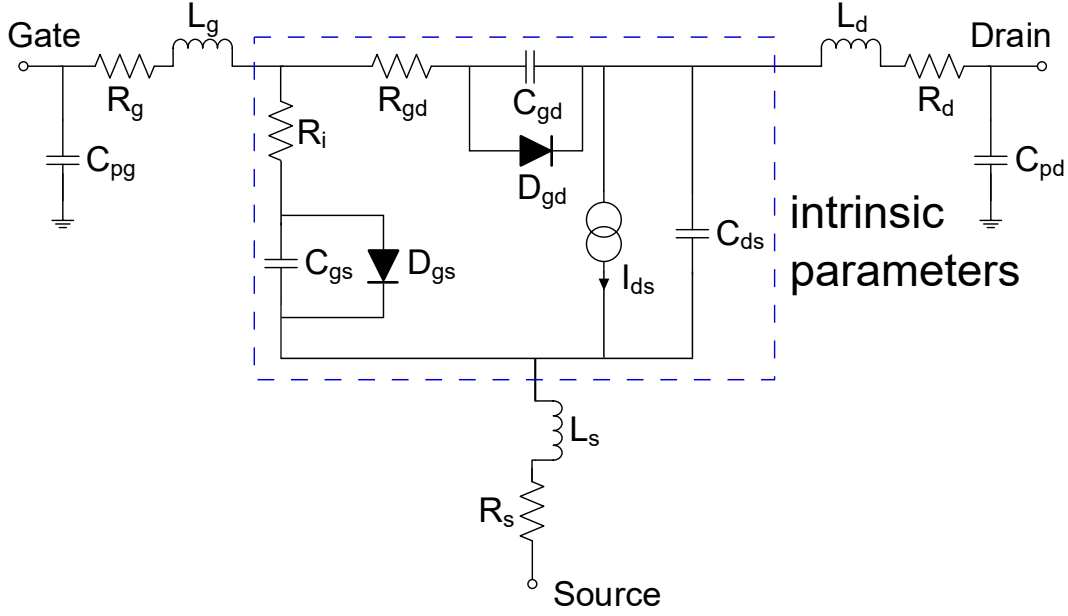


Figure 2.14: Basic equivalent circuit used in this thesis for large-signal model.

### 2.3.1 Nonlinear Circuit Modeling

The Chalmers model [36, 38] was applied in this thesis to model the intrinsic nonlinear current source of GaN HEMTs, as it is a frequently used and well-known GaN HEMT model. In this compact model the current sources are described by nonlinear functions of intrinsic voltages  $v_{ds}(t)$  and  $v_{gs}(t)$ . It has to be noted that the proposed large-signal model was empirical, which means that the model parameter extraction routine is always based on measurements. In this thesis, multi-bias S-parameter measurements were adopted to determine the model parameters and also to validate the extracted models.

#### A) Drain-source current model

The drain-source current function of the Chalmers model can be expressed as:

$$I_{ds}[V_{gs}, V_{ds}] = I_{pk0} \cdot (1 + \tanh(\psi)) \cdot \tanh(\alpha \cdot V_{ds}) \cdot (1 + \lambda \cdot V_{ds}) \quad (2.22)$$

where  $I_{pk0}$  is the drain current at maximum transconductance  $g_m$ ,  $\lambda$  is the channel length modulation parameter and  $\alpha$  is the saturation voltage parameter. The param-

eters  $\lambda$  and  $\alpha$  are also used in some other models, i.e. Statz [66] and Curtice [67] GaAs FET models.

In this formulation, it is evident that the gate voltage dependence is described by a hyperbolic tangent function, whose derivatives are normally available in commercial HB simulations. And the gate dependent parameter  $\psi$  is a polynomial function of  $v_{gs}$  expressed as:

$$\psi = P_{1m} \cdot (V_{gs} - V_{pkm}) + P_2 \cdot (V_{gs} - V_{pkm})^2 + P_3 \cdot (V_{gs} - V_{pkm})^3 \quad (2.23)$$

$$P_{1m} = P_1 \cdot (1 + B_1 / \cosh^2(B_2 \cdot V_{ds})) \quad (2.24)$$

$$V_{pkm} = V_{pks} - D_{vpks} + D_{vpks} \cdot \tanh(\alpha_s \cdot V_{ds}) \quad (2.25)$$

where  $V_{pks}$  is the gate voltage at which the maximum of transconductance  $g_m$  occurs,  $D_{vpks}$  is the difference of the gate voltage measured at the drain voltage in the saturated region and close to zero,  $P_1$ ,  $P_2$ , and  $P_3$  are fitting parameters, which contribute to the prediction of measured “bell-shaped”  $g_m$  structure,  $B_1$  and  $B_2$  are fitting parameters for  $P_1$ .

The parameter  $\alpha$  is also a bias dependent parameter and can be described as:

$$\alpha = \alpha_r + \alpha_s \cdot (1 + \tanh(\psi)) \quad (2.26)$$

where  $\alpha_r$  indicates the slope at low voltage and low current region,  $\alpha_s$  represents the slope at low voltage and high current region.

The detailed formulas for the differential information of  $i_{ds}$ , e.g.,  $g_m$  and  $G_{ds}$ , are summarized in Appendix A.

The drain-source current model parameter extraction routine is based on multi-bias S-parameter measurements, where the drain voltage is normally swept from 0V, and the gate voltage is swept from below pinch-off to a positive value, thereby completely covering the relevant part of output I/V and transfer characteristics field. The model can then be directly fitted against the currents measured along the S-parameter and  $g_m$  from the small-signal model determined from S-parameters with the least square algorithm in Scilab program [68]. The whole calculate and optimization procedures have been implemented in a Scilab toolbox.

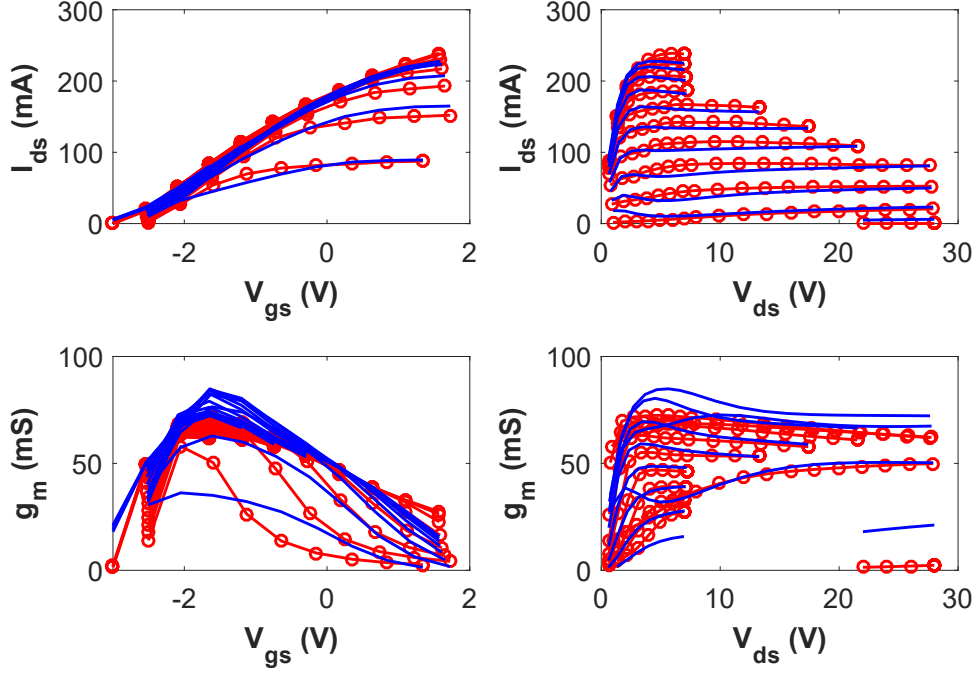


Figure 2.15: Measured (symbols) and modeled (lines)  $I_{ds}$  and  $g_m$  of the  $250 \mu\text{m}$  GaN HEMT, described by the Chalmers current model.

Fig. 2.15 shows large-signal model predictions of  $I_{ds}$  and  $g_m$  together with the DC and small-signal parameters against which the models were fitted. It is evident that a significant deviation can be observed between modeled and simulated transconductance  $g_m$  since the model cannot account for the difference between  $g_m$  determined from S-parameters and  $G_m$  being the derivative of the DC current  $dI_{ds}/dV_{gs}$ , and in case of GaN HEMTs, it cannot be generally assumed that  $g_m$  and  $G_m$  are identical or close to each other. However, a good agreement has been achieved for prediction of  $I_{ds}$  by using Chalmers model formulations.

## B) Gate-source and gate-drain current model

In the proposed large-signal model, the gate-source and gate-drain current sources were modeled by two diodes which connect gate with source and drain. The values of the diodes were extracted from simple forward biased measurements, and a modified Schottky diode formulation was employed to describe them as:

$$I_{gs} = I_j(e^{(P_g \tanh(2(V_{gs}-V_{jg})))} - e^{(P_g \tanh(-2V_{jg}))}) \quad (2.27)$$

$$I_{gd} = I_j(e^{(P_g \tanh(2(V_{gd}-V_{jg})))} - e^{(P_g \tanh(-2V_{jg}))}) \quad (2.28)$$

where  $I_j$  is the gate forward saturation current,  $P_g$  is a fitting parameter, which contributes to predict the slope of the curve ( $I_g/V_{gs}$ ),  $V_{jg}$  is the gate voltage at which the transistor is operated.

### 2.3.2 Large-signal Capacitances Modeling

After modeling the nonlinear current parameters, the large-signal capacitances are to be modeled by fitting the large-signal capacitances to the small-signal equivalent-circuit parameters.

For the Chalmers model, although its capacitance model and charge model have the same parameters, the capacitance model as opposite to the charge model was mostly used for convenience. However, it is known that the use of charge model as opposite to capacitance model enables a good convergence and ensures energy conservation [69, 70].

#### a. Capacitance model

In case of the capacitance model, the large-signal equivalent circuit has the same topology as the small-signal equivalent circuit in  $\Pi$ -configuration as illustrated in Fig. 2.16. For simplicity, the intrinsic resistances are not shown. It is evident that the large-signal capacitances and the small-signal capacitances can be related to each other as:

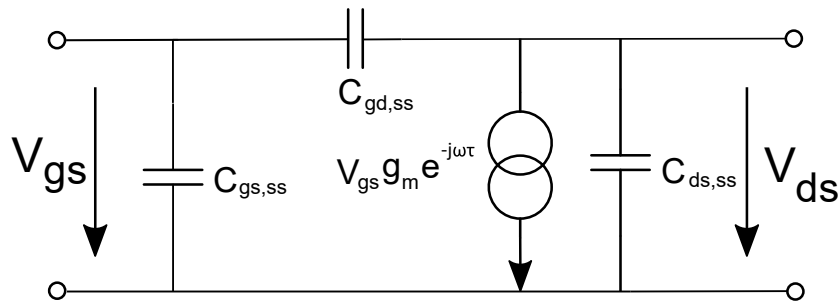


Figure 2.16: Intrinsic small-signal equivalent circuit in  $\Pi$ -configuration. For simplicity, the intrinsic resistances are not shown.

$$C_{gs,ss} = C_{gs,ls} \quad (2.29)$$

$$C_{gd,ss} = C_{gd,ls} \quad (2.30)$$

$$C_{ds,ss} = C_{ds,ls} \quad (2.31)$$

For GaN HEMTs, the gate-to-source and gate-to-drain capacitances  $C_{gs}$  and  $C_{gd}$  present a nonlinear dependence on both gate-source and drain-source voltages  $v_{gs}$  and  $v_{ds}$  as shown in following equations:

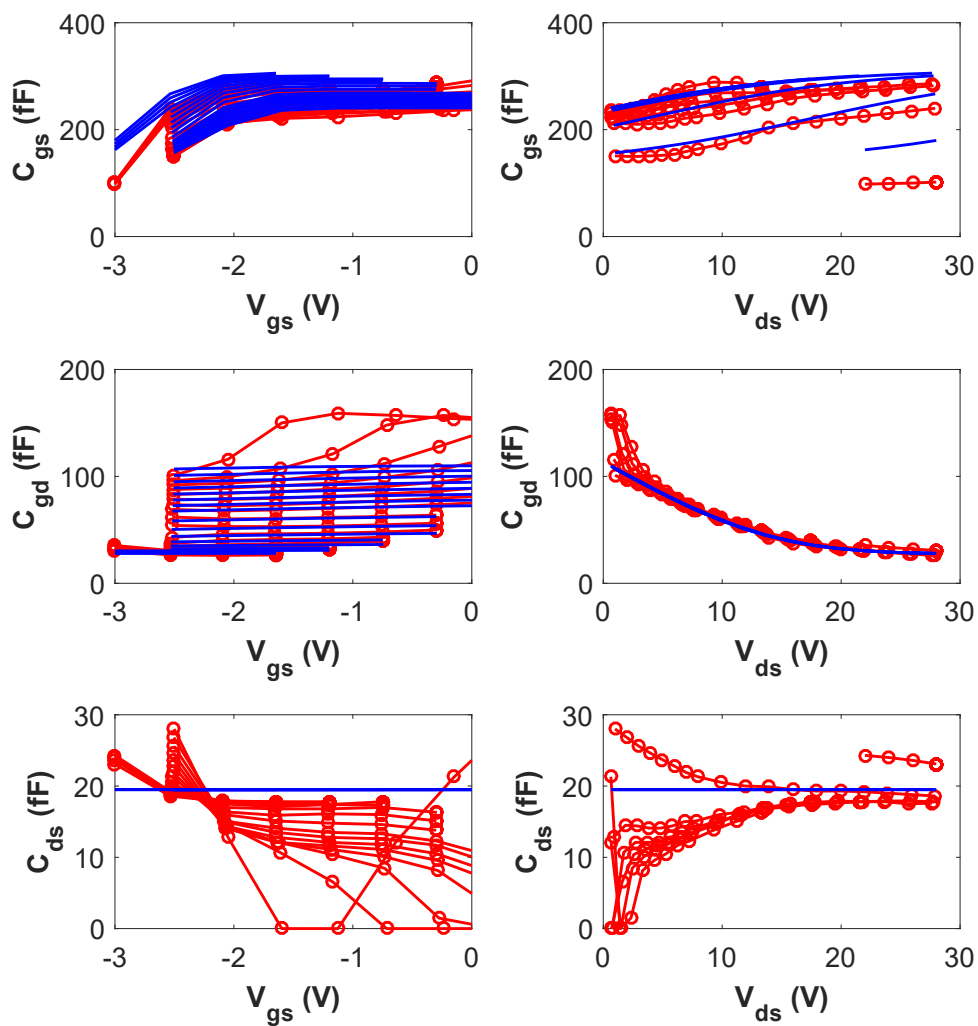


Figure 2.17: Modeled intrinsic capacitances against  $v_{gs}$  and  $v_{ds}$  extracted from multi-bias S-parameter measurements, small signal model (symbols) and large signal model (lines).



$$C_{gs} = C_{gs\pi} + C_{gs\rho} \times (1 + \tanh(\psi_1)) \times (1 + \tanh(\psi_2)) \quad (2.32)$$

$$C_{gd} = C_{gd\pi} + C_{gd\rho} \times ((1 - P_{111} + \tanh(\psi_3)) \times (1 + \tanh(\psi_4)) + 2 \times P_{111}) \quad (2.33)$$

$$\psi_1 = P_{10} + P_{11} \times V_{gs} + P_{111} \times V_{ds} \quad (2.34)$$

$$\psi_2 = P_{20} + P_{21} \times V_{ds} \quad (2.35)$$

$$\psi_3 = P_{30} - P_{31} \times V_{ds} \quad (2.36)$$

$$\psi_4 = P_{40} + P_{41} \times V_{gd} - P_{111} \times V_{ds} \quad (2.37)$$

where  $P_{10}$ ,  $P_{11}$ ,  $P_{20}$ ,  $P_{21}$ ,  $P_{30}$ ,  $P_{31}$ ,  $P_{40}$ ,  $P_{41}$ , and  $P_{111}$  are the main fitting parameters of the capacitances model. The drain-to-source capacitances  $C_{ds}$  is assumed to be constant. These parameters were determined by fitting the simulation curves to the small-signal equivalent-circuit parameters below  $v_{gs} = 0$  V. As shown in Fig. 2.17, the intrinsic capacitances can be well modeled by using the capacitance model.

## b. Charge model

As mentioned before, the use of a charge model is necessary in the large-signal modeling, not only realizing a good convergence in simulations but also ensuring energy conservation. However, one of the major problems during the extraction of the charge model parameters is the discrepancy that occurs when attempting to relate the large-signal model to the small-signal model using the same topology as shown in Fig. 2.16. This discrepancy is mainly due to the so-called transcapacitances, which are caused by the multiple voltage dependence of the charges in the large-signal model [70], e.g., for Chalmers GaN HEMT charge model:  $Q_{gs}$  and  $Q_{gd}$  are known to be functions of both gate and drain bias voltages.

First, considering the traditional intrinsic small-signal model in  $\Pi$ -configuration illustrated in Fig. 2.16, the resulting bias-dependent small-signal intrinsic Y-parameters are then given by:

$$Y_{int,ss} = \begin{Bmatrix} j\omega(C_{gs,ss} + C_{gd,ss}) & -j\omega C_{gd,ss} \\ g_{m,ss}(1 - j\omega\tau_{ss}) - j\omega C_{gd,ss} & j\omega(C_{ds,ss} + C_{gd,ss}) \end{Bmatrix}$$

with

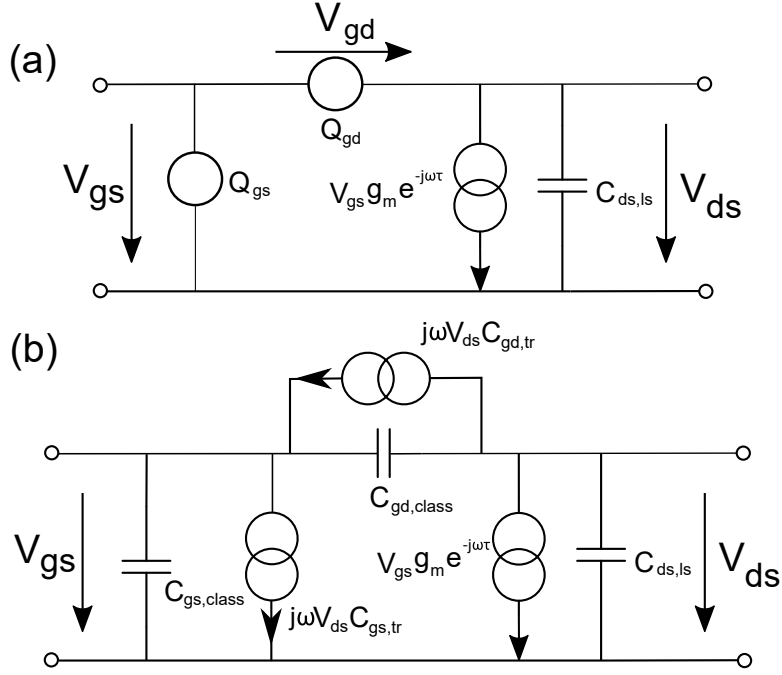


Figure 2.18: (a) Large-signal equivalent circuit of the intrinsic GaN HEMT. (b) Intrinsic large-signal model in the presence of transcapacitances  $C_{gs,tr}$  and  $C_{gd,tr}$  parallel to  $C_{gs,class}$  and  $C_{gd,class}$ .

$$e^{j\omega\tau} \approx 1 - j\omega\tau \quad (2.38)$$

The intrinsic capacitances found in (2.38) are extracted from multi-bias S-parameter measurements after deembedding the extrinsic elements extracted from cold-FET measurement.

Fig. 2.18(a) shows the intrinsic part of the large-signal equivalent circuit. It consists of the gate-source charge ( $Q_{gs}$ ), the gate-drain charge ( $Q_{gd}$ ), a current source and drain-source capacitance ( $C_{ds,ls}$ ). The functions of the charges  $Q_{gs}$  and  $Q_{gd}$  have been presented in [71] as:

$$Q_{gs} = C_{gs\pi} \cdot V_{gs} + \frac{C_{gs0}}{P_{11}} \cdot (1 - P_{111} + \tanh(P_{20} + P_{21} \cdot V_{ds})) \cdot (\phi_1 + \ln(\cosh(\phi_1)) - Q_{gs0}) + 2 \cdot C_{gs0} \cdot P_{111} \cdot V_{gs} \quad (2.39)$$

$$Q_{gd} = C_{gdpi} \cdot V_{gd} + \frac{C_{gd0}}{P_{41}} \cdot ((1 - P_{111} + \tanh(P_{30} - P_{31} \cdot V_{ds})) \quad (2.40)$$

$$\cdot (\phi_4 + \ln(\cosh(\phi_4)) - Q_{gd0}) + 2 \cdot C_{gd0} \cdot P_{111} \cdot V_{gd} \quad (2.41)$$

with

$$\phi_1 = P_{10} + P_{11} \cdot V_{gs} + P_{111} \cdot V_{ds} \quad (2.42)$$

$$\phi_4 = P_{40} + P_{41} \cdot V_{gd} - P_{111} \cdot V_{ds} \quad (2.43)$$

$$Q_{gs0} = P_{10} + P_{111} \cdot V_{ds} + \ln(\cosh(P_{10} + P_{111} \cdot V_{ds})) \quad (2.44)$$

$$Q_{gd0} = P_{40} - P_{111} \cdot V_{ds} + \ln(\cosh(P_{40} - P_{111} \cdot V_{ds})) \quad (2.45)$$

where  $C_{gs\pi}$ ,  $C_{gs0}$ ,  $C_{gd\pi}$ ,  $C_{gd0}$ ,  $P_{10}$ ,  $P_{11}$ ,  $P_{20}$ ,  $P_{21}$ ,  $P_{30}$ ,  $P_{31}$ ,  $P_{40}$ ,  $P_{41}$ , and  $P_{111}$  are all fitting parameters, which are also adopted in the Chalmers capacitance model.

It is evident that the charge  $Q_{gs}$  depends on two bias voltages  $V_{gs}$  and  $V_{ds}$ , while the charge  $Q_{gd}$  depends on  $V_{gd}$  and  $V_{ds}$ . Therefore, the classical capacitances and transcapacitances yield:

$$C_{gs,class} = \left. \frac{\partial Q_{gs}}{\partial V_{gs}} \right|_{V_{ds}=const} \quad C_{gd,class} = \left. \frac{\partial Q_{gd}}{\partial V_{gd}} \right|_{V_{ds}=const} \quad (2.46)$$

$$C_{gs,tr} = \left. \frac{\partial Q_{gs}}{\partial V_{ds}} \right|_{V_{gs}=const} \quad C_{gd,tr} = \left. \frac{\partial Q_{gd}}{\partial V_{ds}} \right|_{V_{gd}=const} \quad (2.47)$$

The detailed formulas for classical capacitances and the transcapacitances can be found in Appendix.

Now, it can be found that the resulting capacitances  $C_{gs,class}$  and  $C_{gd,class}$  of the charge model share the same functions with the Chalmers capacitance model for  $C_{gs}$  and  $C_{gd}$ . Fig. 2.18(b) illustrates the resulting topology. Here, the transcapacitances are understood as a remote-voltage dependent current source with  $j\omega$ . Now, the resulting intrinsic Y-parameters are given by:

$$Y_{int,ls} = \left\{ \begin{array}{cc} j\omega(C_{gs,class} + C_{gd,class}) & -j\omega(C_{gd,class} - C_{gd,tr}) + j\omega(C_{gs,tr}) \\ g_{m,ls}(1 - j\omega\tau_{ls}) - j\omega C_{gd,class} & j\omega(C_{gd,class} - C_{gd,tr}) + j\omega(C_{ds,ls}) \end{array} \right\} \quad (2.48)$$

It is obvious that the transcapacitances only impact on the modeling of  $Y_{12}$  and  $Y_{22}$ . Hence, it can be assumed that a good modeling performance of  $Y_{11}$  and  $Y_{21}$  can be expected when using the parameters determined for the capacitance model in the

charge model. In order to relate the small-signal and large-signal Y-parameters, the  $Y_{11}$  and  $Y_{21}$  of equation (2.48) should be rewritten in the following form:

$$\begin{aligned} Y_{11} &= j\omega C_{gs,class} + j\omega(C_{gd,class} - C_{gd,tr}) + j\omega(C_{gd,tr}) \\ Y_{21} &= g_{m,ls}(1 - j\omega\tau_{ls}) - j\omega(C_{gd,class} - C_{gd,tr}) - j\omega(C_{gd,tr}) \end{aligned} \quad (2.49)$$

Therefore, as long as we have a negligible  $C_{gs,tr}$  to  $Y_{12}$  and a negligible  $C_{gd,tr}$  to  $Y_{11}$  and  $Y_{21}$ , the small-signal and large-signal capacitances can be related to each other as:

$$C_{gs,ss} = C_{gs,class} = C_{gs,ls} \quad (2.50)$$

$$C_{gd,ss} = C_{gd,class} - C_{gd,tr} = C_{gd,ls} \quad (2.51)$$

$$C_{ds,ss} = C_{ds,ls} \quad (2.52)$$

These equations enable a numeric extraction of the parameters of the charge expressions  $Q_{gs}$  and  $Q_{gd}$  by fitting the proposed large-signal capacitances to the small-signal capacitances. Fig. 2.19 shows the comparison between the small-signal  $C_{gd}$  extracted from S-parameter measurements and S-parameter simulation

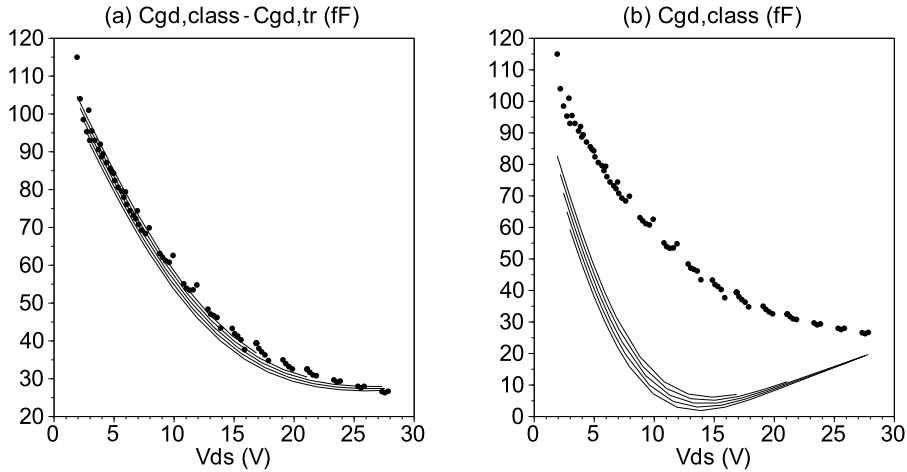


Figure 2.19: Small-signal intrinsic capacitance  $C_{gd}$  extracted from S-parameter measurements (dots) and S-parameter simulation (lines) based on the charge model with (a) and without (b) considering transcapacitance  $C_{gd,tr}$ .  $V_{gs} = -2.5$  V to  $-0.5$  V in 0.5 V steps.

using the extracted parameters for the charge model (a) and for the capacitance model (b). As seen in the figure, the intrinsic capacitances of the transistor can be modeled very well in application of the proposed procedure, which takes the transcapacitance effects into account. However, the extracted capacitance model without transcapacitance  $C_{gd,tr}$  dramatically underestimates the value of  $C_{gd}$ .

Figs. 2.20(a) presents the proportion of the extracted values of  $C_{gd,tr}$  to  $C_{gd,ss}$  against  $V_{ds}$ . As seen in this figure, the impact of  $C_{gd,tr}$  significantly increases with the increase of  $V_{ds}$ , and it is obviously not negligible. Fig 2.20(b) shows the proportions of the extracted values of  $C_{gs,tr}$  to  $C_{gd,ss}$ . It is obvious that  $C_{gs,tr}$  has almost no effect on the extraction of  $C_{gd}$  from  $Y_{12}$ , especially at high  $V_{ds}$  region.

As an other necessary condition for the application of the relationship between small-signal and large-signal capacitances as formulated in Equations (2.50),  $C_{gd,tr}$  should be negligible in  $Y_{11}$ . This condition is verified by Figs. 2.20(c), where  $C_{gd,tr}$  shows little importance to  $Y_{11}$ , for its share is always below 10% of  $(C_{gs,ss} + C_{gd,ss})$ . In the situation of  $Y_{21}$ , the importance of  $C_{gd,tr}$  increases to a certain extent, e.g., 20% at 28 V, which should be further optimized.

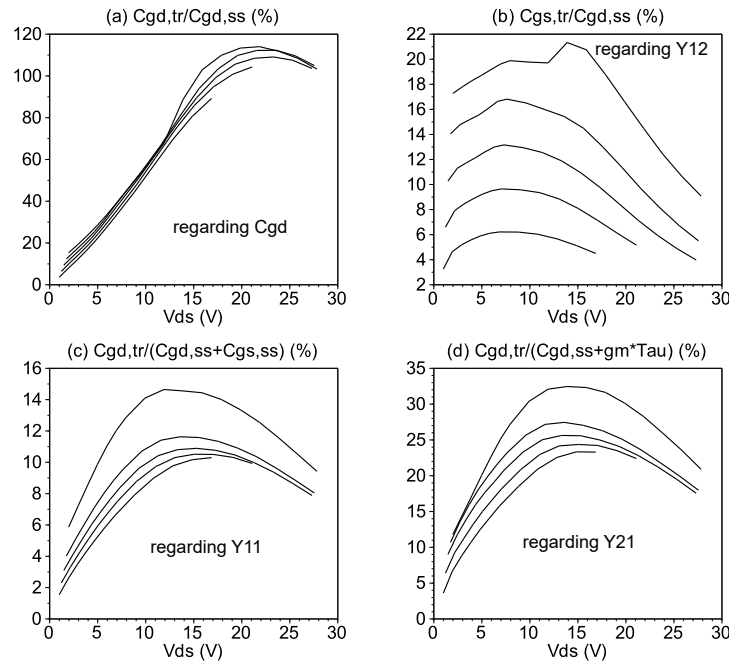


Figure 2.20: Proportions of (a)  $C_{gd,tr}$  to  $C_{gd,ss}$ ; (b)  $C_{gs,tr}$  to  $C_{gd,ss}$ ; (c)  $C_{gd,tr}$  to  $(C_{gs,ss} + C_{gd,ss})$ ; (d)  $C_{gd,tr}$  to  $(C_{gd,ss} + g_{m,ss} \cdot \tau_{ss})$ , against  $V_{ds}$ ,  $V_{gs}$  is from -2.5 V to -0.5 V in 0.5 V steps.

## 2.4 Trapping Effects in GaN HEMTs

It is well known that GaN HEMTs suffer from trapping effects, which hamper the achievable output power, output current, and linearity. However, unlike GaAs MES-FETs [72] the trapping effect phenomena observed in GaN HEMTs are very complex and not completely understood yet. The recent studies provide only qualitative and contradicting explanations of the trapping phenomena. This places the circuit designers in a very tough situation: on one hand, the trapping effects cannot be solved rapidly by the development of HEMT technology; on the other hand, until now, none of the trap models has been available in commercial tools. This is the basis to find an accurate and efficient way to characterize these trapping effects, which can be used by the circuit designers.

In this section, first the state of the physical explanation for trapping effects will be reviewed. Next, two published models, which can take the trapping effects into account, will be presented.

### 2.4.1 Physical Mechanisms of Trapping Effects

Understanding the origin of the traps in GaN-based transistors, their location, and the physical mechanisms involved in the trapping is important for the optimization of device performance. From an electrical point of view, the traps are known as energy levels located within the energy band gap of semiconductor materials. They cause many electrical anomalies, such as current collapse, the discrepancy between trans-conductance under static and dynamic conditions and frequency dispersion of the output conductance [40, 73]. GaN HEMTs usually exhibit short capture time constants, when the traps capture free charge carriers and long emission time constants, when the traps release free charge carriers [44]. These time constants induce a delayed response of the channel current to the fast changing electrical command signals (RF/Microwave). In recent years, the identification of traps in GaAs-based transistors have already been studied well [72]. However, in the case of GaN HEMTs, the identification of the traps has proven to be much more difficult due to the non-reproducibility of measurements and invalidity in some cases [74]. Many factors may explain these limitations:

- Fabrication: The unstable material qualities and growth processes.

- Electric field: The specific mechanisms, such as the Poole-Frenkel effects [75], can occur due to the very high values of electric field in wideband gap materials. In the presence of an electric field, the characteristics of the capture and emission process change.
- Defects and dislocation: GaN contains high densities of defects and dislocations formed during the growth due to the large difference in lattice constants and in thermal expansion coefficients of the substrate and the epi-layers [61].

As already mentioned, the traps are able to capture and release the free charge carriers. The important characteristics have been given in the Shockley-Read-Hall (SRH) statistics [76]. The occupation factor  $f_T$  of the traps, presented in Equation (2.53), is described by the balance of the capture and emission processes as:

$$\frac{df_T}{dt} = n \cdot C_n(1 - f_T) - E_n \cdot f_T \quad (2.53)$$

with

$$C_n = \sigma_n \cdot v_{thn} \quad (2.54)$$

where  $f_T$  is the electron occupancy ratio for deep traps,  $n$  is the electron concentration,  $\sigma_n$  is the electron capture cross-section, and  $v_{thn}$  is the electron thermal velocity. The term  $(n \cdot C_n)$  gives the capture rate, while the emission rate  $E_n$  is demonstrated by the Arrhenius law as:

$$E_n = \frac{1}{\tau_{emission}} = A \cdot T^2 \cdot e^{\frac{-E_A}{kT}} \quad (2.55)$$

where  $A$  is a constant,  $T$  is the temperature,  $k$  is the Boltzmann's constant,  $\tau_{emission}$  represents the charge emission time constant, and  $E_A$  is the activation energy.

In the simplest case, the activation corresponds to the position of the trap level with respect to the bottom of the conduction band for a donor-type trap (or with respect to the top of the valence band for an acceptor-type trap). It is evident that the capture rate is proportional to the electron concentration  $n$ , while the temperature together with the position of the trap level with respect to the bottom of the conduction band strongly influence the emission rate  $E_n$ . The emission and capture rates  $E_n$  and  $(n \cdot C_n)$  can be measured by monitoring the time evolution of the

drain current. However, from the Equations (2.54) and (2.55), it can be concluded that the emission time constants are several order magnitude longer than the capture time constants. This peculiar behavior is very important to understand the transistor electrical characteristics under RF drive, under transient conditions and also under steady state operation.

For GaN HEMTs, the traps can be separated into two types "Gate-Lag" and "Drain-Lag". They correspond to the delayed response of the drain current with respect to  $V_{gs}$  and  $V_{ds}$  control voltages, respectively. Consequently, in frequency domain, the impact of gate lag is noticeable on trans-conductance (the partial derivative of drain current with respect to gate potential), and the impact of drain lag on the output conductance ( the partial derivative of drain current with respect to drain potential).

### 2.4.2 Gate-Lag Effects

Gate-lag effects are mainly due to the presence of negative charges trapped at the semiconductor surface of the epitaxial layers above the 2DEG. In this region, the electric field is strongest, and the gate can provide free electrons to fill the surface states.

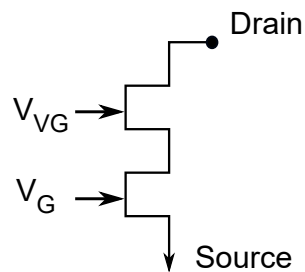


Figure 2.21: Equivalent circuit with two gates:  $V_G$  is the normal metal gate and  $V_{VG}$  is the virtual gate.

In GaN HEMTs, in order to take gate-lag effects into account, *Vetury et al.* [17] introduced the concept of "virtual gate", which is a pseudo gate mainly caused by the negative charges on the surface. Due to the resulting negative surface potential, the channel of electrons is depleted and the gate depletion region is extended. These surface states act as a second gate electrode. Fig. 2.21 shows the equivalent circuit with two gate potentials:  $V_G$  is at the normal metal gate and is controlled by the



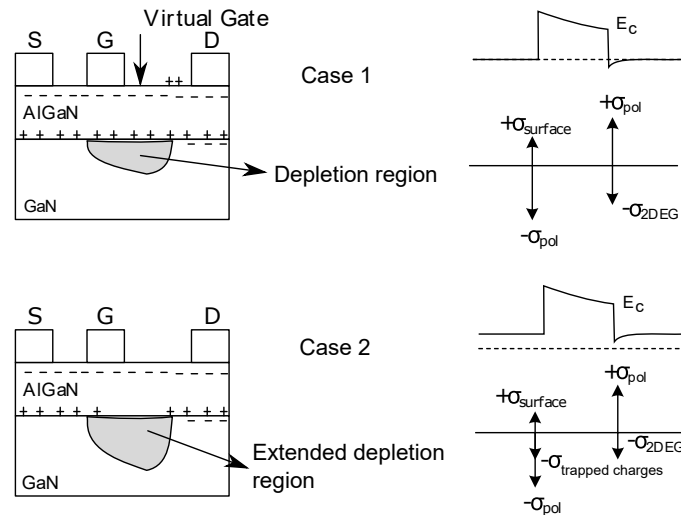


Figure 2.22: Equivalent circuit with two gates:  $V_G$  is the normal metal gate and  $V_{VG}$  is the virtual gate [17].

applied gate bias,  $V_{VG}$  is at the virtual gate and is controlled by the amount of the trapped charges. Fig. 2.22 shows the schematic illustration of this concept and explains, how the “virtual gate” acts as a second gate. In the first case, the surface donors are ionized, which leads to the additional electrons in the 2DEG, while in the second case, the partial occupation of these surface states with electrons results in a somewhat lower 2DEG concentration [74], compared to case 1.

Gate-lag effects are supposed to be observed using pulsed I/V characteristics.

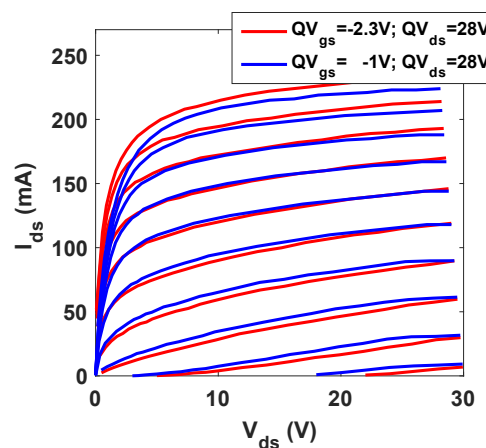


Figure 2.23: Pulsed I/V curves for different pulse quiescent gate voltages and same pulse quiescent drain voltage of a 250  $\mu\text{m}$  GaN HEMT (pulse length: 250 ns, dynamic  $v_{gs}$  from -3 V to 1.5 V).

However, due to the recent improvements in AlGaIn/GaN technology, Gate-lag effects have been significantly reduced by passivation and field plate, e.g., in our case, gate-lag effects are so weak, that it is almost impossible to distinguish between gate-lag effects and thermal effects even by means of pulsed measurements [49]. As shown in Fig. 2.23 for two pulsed I/V curves with different quiescent gate voltages, the deviations between these two  $i_{ds}$  curves of different dynamic  $v_{gs}$  for  $v_{gs} < 0$  V can be attributed to gate-lag effects. However, the reverse deviations observed for  $v_{gs} > 0$  V is mainly due to the thermal effects.

### 2.4.3 Drain-Lag Effects

In GaAs MESFETs, the output current determined by the effective channel thickness is normally modulated by the gate potential. However, due to the ionized traps in the substrate [77] or at the substrate-channel interface [78], it is also modulated by the extension of the depletion layer into the active region. The injection of free electrons is determined by the drain potential, and this mechanism is called “drain-lag effect” or also “self-backgating” (as the traps act like a pseudo backgate terminal [79]).

In GaN HEMTs, the phenomenon of drain-lag is very similar but the output current is now modulated by the density of free electrons in the channel. The presence of a 2D electron gas (2DEG) is to compensate the positive (polarization) charge  $\sigma^+$  at the AlGaIn/GaN interface [80]. However, if the ionized traps are located near to the AlGaIn/GaN interface, the resultant change is not zero and becomes negative, the equilibrium is kept by changing the 2DEG density ( $n_s$ ) as shown in the following equation:

$$\sigma_+ = q \cdot (n_s - Nd^+ + Na^-) \quad (2.56)$$

where  $Nd^+$  is the density of ionized donors,  $Na^-$  is the density of ionized acceptors, and  $q$  is the electron charge.

Fig. 2.24 explains how the traps impact the 2DEG density when a drain pulse is applied. Three different states can be observed in the conduction band diagrams under the gate: the initial state marked as case 1, after a positive drain pulse as case 2, back to the initial state as case 3. Here, it is assumed that the buffer already holds deep donors and acceptors with densities  $Na$  and  $Nd$  ( $Na < Nd$ ), respectively. To

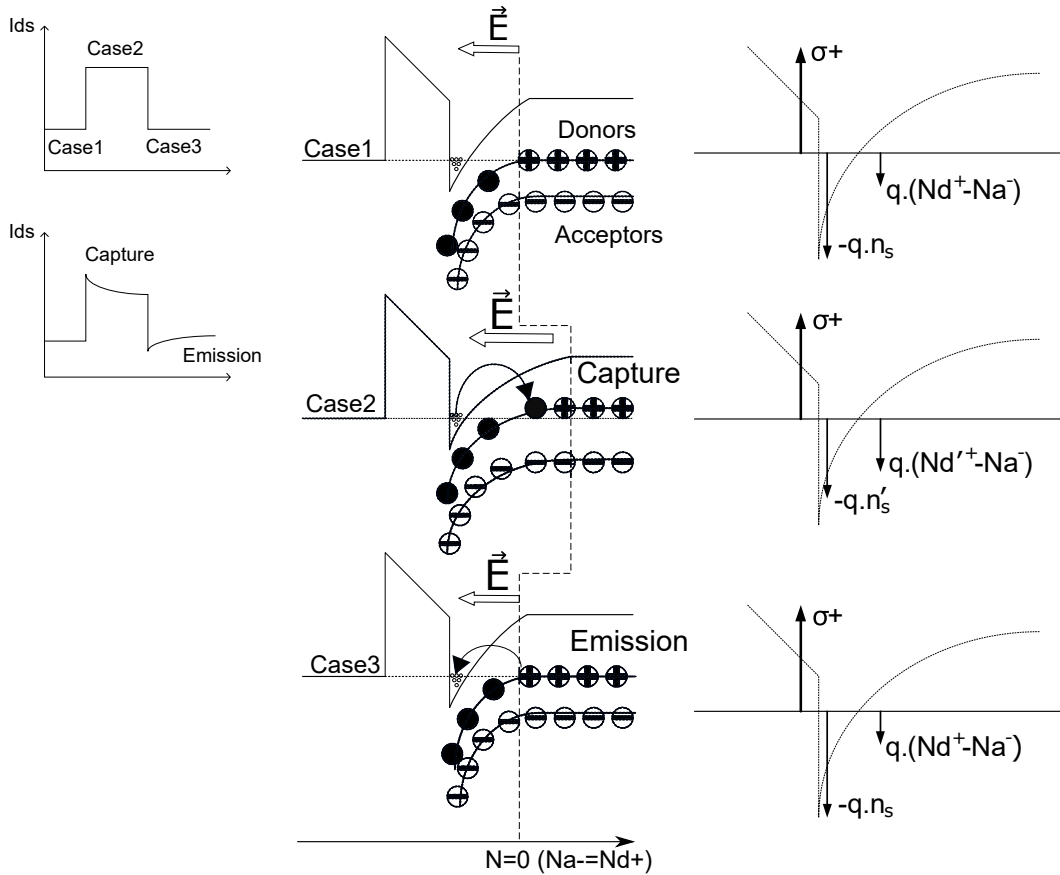


Figure 2.24: Description of trapping and detrapping process of traps located in the GaN buffer of HEMT technology ( $N_d > N_a$ ) [81].

maintain the equilibrium, the Fermi energy is clipped to donor energy level in the absence of electric field.

$$N_d^+ = N_a^- \quad \text{when } E=0 \quad (2.57)$$

On the other hand, when an electric field is applied as in case 1, the equilibrium is reached if:

$$n_s = (\sigma_+)/q + N_d^+ - N_a^- \quad (2.58)$$

When the drain voltage is pulsed up as shown in case 2, the induced vertical electric field causes the deep buffer scattering from the 2DEG channel, which can

be captured by the donor traps. Hence, the density of ionized donors is reduced to  $Nd'^+$  and becomes neutral. This modifies the charge equation as:

$$n'_s = (\sigma_+)/q + Nd'^+ - Na^- \quad (2.59)$$

When the drain voltage is pulsed back to the initial voltage as shown in case 3, the reverse situation would happen. The charge equation should come back to Equation (2.58). However, this process, namely the emission process, presents a much longer time constant than capture process. This asymmetry of the time constants of capture and emission processes is very critical not only in the modeling but also for understanding the pulsed I/V measurements.

Drain-lag effects can be observed using pulsed I/V characteristics, as shown in Fig. 2.25, at different quiescent drain voltages: when the dynamic  $v_{ds}$  is pulsed to a value below  $QV_{ds}$ , the emission process predominates for drain-lag-related traps and the drain-source currents are here dependent on different  $QV_{ds}$ . When the dynamic  $v_{ds}$  is pulsed to voltages above  $QV_{ds}$ , the capture process predominates and the drain-source currents now are dependent on dynamic voltage  $v_{ds}$ , so these two curves are very similar, as expected from physics.

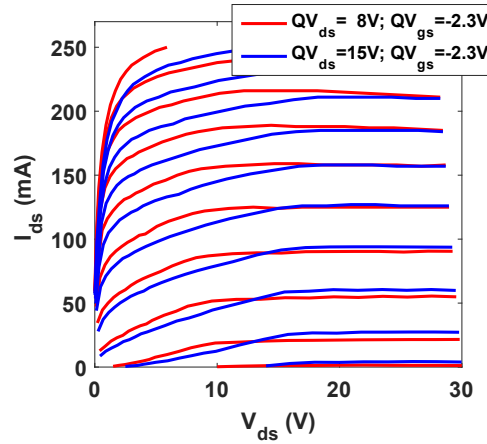


Figure 2.25: Pulsed I/V curves for different pulse quiescent drain voltages and same pulse quiescent gate voltage of a 250  $\mu\text{m}$  GaN HEMT (pulse length: 250 ns, dynamic  $v_{gs}$  from -3 V to 1.5 V).

## 2.4.4 Overview of the Published Models

For GaN HEMTs, the identification of the impact of trapping effects has always been the focus of the modeling study. However, the study results are not very satisfying, due to the modeling difficulty induced by some material and manufacturing process factors, such as unpredictable material qualities, the immature growth process and larger trap densities [61].

Still several trap models have been developed to optimize the modeling accuracy. The following subsections will introduce two of them. It has to be noted, that the following subsections will only focus on drain-lag models, the gate-lag models can be simply achieved by transformation of proposed drain-lag models.

The first proposed model is so-called RC branch type model [82], which not only contributes to model the drain-source current slump due to trapping effects but also takes into account the difference between output conductance extracted from RF characteristic and DC characteristic. Another model [48] employs an external sub-circuit, which determines the effective  $v_{gs}$  due to trap charges, to model the emission and capture processes.

### 1) RC Branch Model

For this simple model, a RC branch is added in parallel the output current sources as shown in Fig. 2.26, it is now often used in some GaN HEMT models, like the Chalmers model. It is obvious that this RC branch works only at high frequency

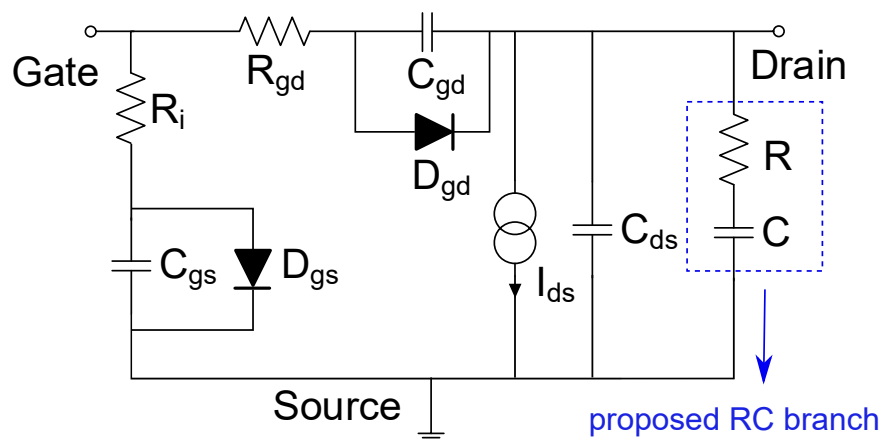


Figure 2.26: Large-signal model with proposed RC branch published in reference [82].

due to the capacitor and brings a correction factor for the transition from DC output conductance to HF output conductance:

$$G_{ds,HF} = G_{ds,DC} + 1/R \quad (2.60)$$

To model the emission time constant, the capacitor value is chosen in order that  $RC = \tau_{emission}$ . However, in the meantime the capture time constant is overestimated to be the same value as the emission time constant, which should be much longer than that for capture process.

Using this model to simulate the small-signal behavior is proved efficient. However, it is no more valid under large-signal condition, because the considered difference between  $G_{ds,HF}$  and  $G_{ds,DC}$  is always constant and equals  $1/R$ , which can induce serious deviations for  $v_{gs}$  close to the pinch-off voltage under large-signal condition.

In Fig. 2.27, the measured pulsed I/V characteristics at  $QV_{ds} = 28$  V and  $QV_{gs} = -2.3$  V is compared with the transient simulations by same conditions using the standard Chalmers model with RC circuit and without RC circuit. It is evident that the model with RC circuit is able to fit the I/V characteristics in high  $v_{gs}$  region by raising the current slope (i.e., the output conductance) of  $1/R$ , however, if  $v_{gs}$  is close to the pinch-off voltage, the constant correction term  $1/R$  will make the simulations inconsistent and results in a negative drain current.

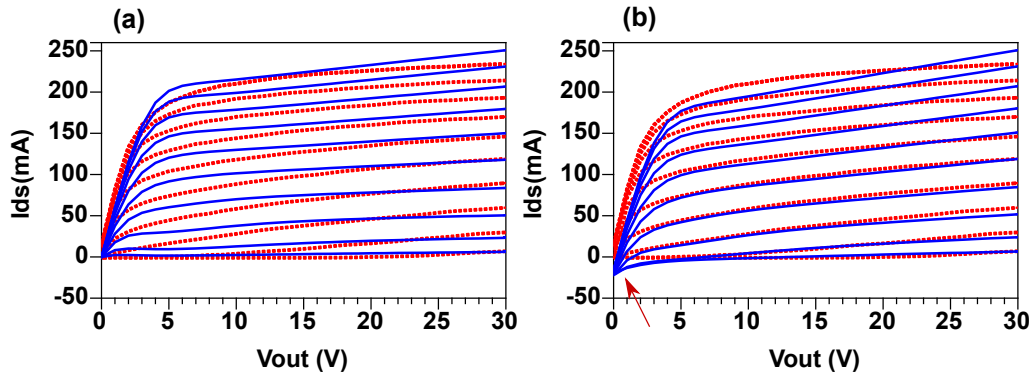


Figure 2.27: Comparison between measured (red dashed lines) and simulated (blue solid lines) pulsed I/V characteristics at  $QV_{ds} = 28$  V and  $QV_{gs} = -2.3$  V using standard Chalmers model (a) without RC branch; (b) with RC branch. The inconsistent region is highlighted.

## 2) The Quéré Drain-Lag Model

In recent years many drain-lag models using external sub-circuits were published, one of them was developed by O. Jardel and R. Quéré [44, 48]. It takes into account both processes of trapping effects: capture process and emission process. Fig. 2.28 shows the equivalent circuit of this model, and it is comprised with two parts: an envelope detector section, which reproduces the asymmetrical time constants for capture and emission process of traps, and a voltage modification section, which determines the effective  $v_{gs}$  due to the trap charges.

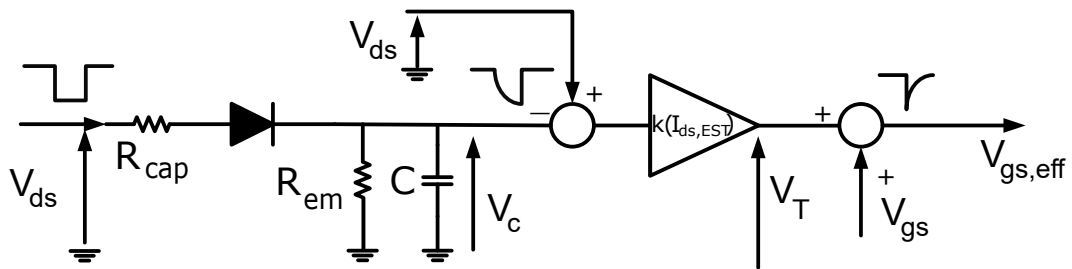


Figure 2.28: Drain-lag sub-circuit: the left part synthesizes the equivalent charge of trap while the right part processes the voltages to generate the actual control voltage  $V_{gs,eff}$  [48].

The first part operates as an envelope detector and can be seen as a “2-path RC branch” model presented previously. If the input voltage  $v_{ds}$  is pulsed up, the diode conducts, the current flows through the resistor  $R_{cap}$  and charges the capacitor  $C$ , the charge time results in  $\tau = R_{cap} \times C$ , which can also represent the time constant for capture process by using small resistance for  $R_{cap}$ . In the case of a negative variation of  $v_{ds}$ , the diode is blocked and the emission process now can be modeled by discharge of the capacitor  $C$  through the resistor  $R_{em}$ , and the discharge time can be calculated as:  $\tau = R_{em} \times C$ . As the emission process is much longer than the capture process, the resistances should be considered as:  $R_{em} \gg R_{cap}$ . The voltage  $V_c$  of the capacitor  $C$  is related to the density of trapped charges.

The second part achieves the prediction of the effective  $v_{gs}$  considering the trap’s contribution. First, the input voltage  $v_{ds}$  is modified by the capacitor voltage  $V_c$ , and the new voltage  $v_{ds} - V_c$  is processed by the amplification factor  $k(I_{ds,EST})$  shown in Fig. 2.28 which is linked to the estimated drain current by:

$$k(I_{ds,EST}) = k \times I_{ds,EST}(V_{gs}) \quad (2.61)$$

with

$$I_{ds,EST}(V_{gs}) = Gm_{EST} \times (v_{gs} - V_p) \quad \text{if } v_{gs} > V_p, \text{ else } 0 \quad (2.62)$$

where  $k$  and  $Gm_{EST}$  are fitting parameters, and voltage  $V_T$  can be defined as:

$$V_T = k(I_{ds,EST}) \times (V_{ds} - V_c) \quad (2.63)$$

Finally, the effective gate voltage  $V_{gs,eff}$  is defined by the following equation:

$$V_{gs,eff} = V_{gs} + k(I_{ds,EST}) \times (V_{ds} - V_c) \quad (2.64)$$

So that the drain current will be expressed as:

$$I_{ds} = f(V_{gs,eff}, V_{ds}) \quad (2.65)$$

As a chronogram published in [81], Fig. 2.29 shows the internal voltages predicted by the sub-circuit in the case of a transient simulation for a drain voltage pulse from 30 V to 10 V, and  $k(I_{ds,EST}) = 0.01$  during a pulse width that is large enough to observe emission and capture process on the simulated intrinsic voltages and drain current. It can be observed that the capacitor voltage  $V_c$  is able to exhibit the slow emission and fast capture process, and the drain-lag model achieves a good prediction of drain current under drain-lag impact.



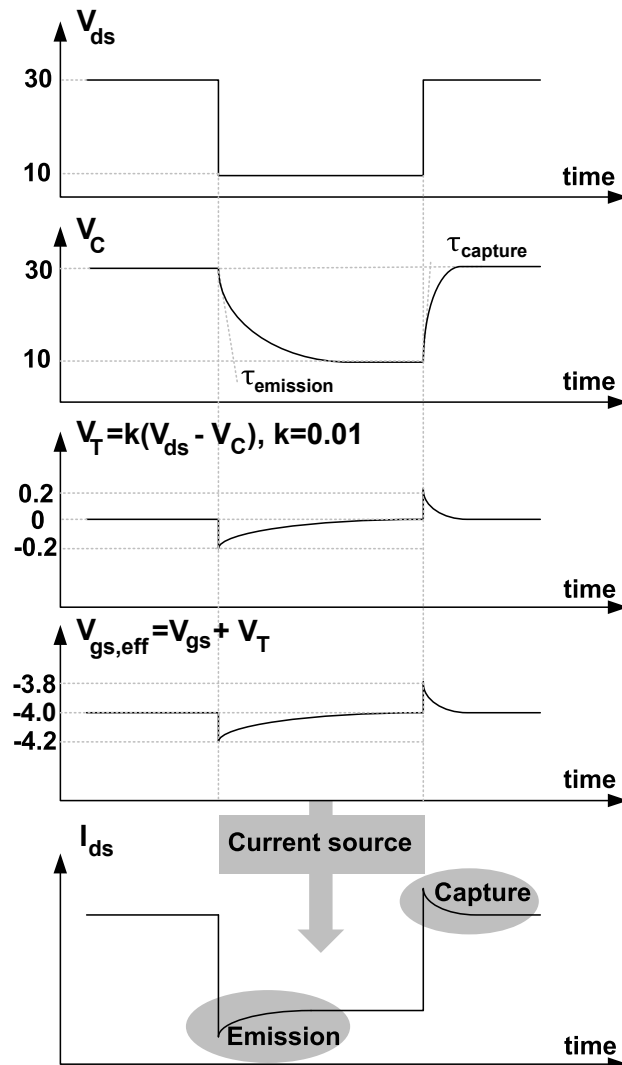


Figure 2.29: Chronogram of internal voltages and drain current in the drain-lag sub-circuit model for a negative drain pulse from 30 V to 10 V [81].



## Chapter 3

# Pulsed S-Parameter Measurements

Nowadays, it is well known that the pulsed measurements are the most relevant characterization technique compared to conventional DC and CW measurements [83–86]. They permit an in-depth characterization of different effects like drain current non-linearity and discrimination of trapping and self-heating effects [87].

In the last decade, pulsed measurements with a short pulse length were used under the assumption that the device is free from the self-heating and drain-lag effects [47]. However, the assumption doesn't correspond with the reality, since the trapping (capture process) time constant normally lies in nanosecond range which is much shorter than the pulse length, while the detrapping (emission process) time constant is of microsecond level which is longer than the pulse length, which means that only the capture process will occur in the pulsed measurements.

This asymmetry of the time constant between emission and capture process allows to understand the fact that the trap states depend on instantaneous values ( $v_{gs}$ ,  $v_{ds}$ ) with a positive variation of  $v_{gs} / v_{ds}$  or remain constant at the quiescent bias point ( $QV_{gs}$ ,  $QV_{ds}$ ) with a negative  $v_{gs} / v_{ds}$  variation. Hence, it can be concluded that the gate trapping state is described by the minimum of the quiescent and the pulsed gate voltages, while the drain trapping state is described by the peak value of the quiescent and the pulsed drain voltages.

This chapter will first focus on the principle of the pulsed measurements. Then, this chapter is dedicated to introduce the pulsed S-parameter measurements setup used in this thesis. Finally, the advantages of modeling GaN HEMTs relying on pulsed measurements will be discussed.

### 3.1 Principle of Pulsed Measurements

The principle of the pulsed measurements is shown in Fig. 3.1. It consists of I/V characteristics and S-parameters measured in quasi-isothermal conditions at given quiescent points ( $QV_{ds} = 0$  V and 28 V,  $QV_{gs} = -1$  V). So, it is possible to define two cases with regard to the  $v_{ds}$  variation.

1. Negative  $v_{ds}$  variation. In this case,  $v_{ds}$  is pulsed from  $QV_{ds} = 28$  V to a lower voltage, i.e.,  $v_{ds} = 14$  V. However, the instantaneous output current does not follow the fast  $v_{ds}$  variation but exhibits a slow current transient due to the long emission time constant of drain-lag effects. Since the pulse length is much shorter than the emission time constant, the current cannot reach its steady-state as shown in Fig. 3.1 with black cross. Moreover, the current should be measured in the middle of the pulse in order to prevent any deviation caused by switching effects at the beginning and the end of the

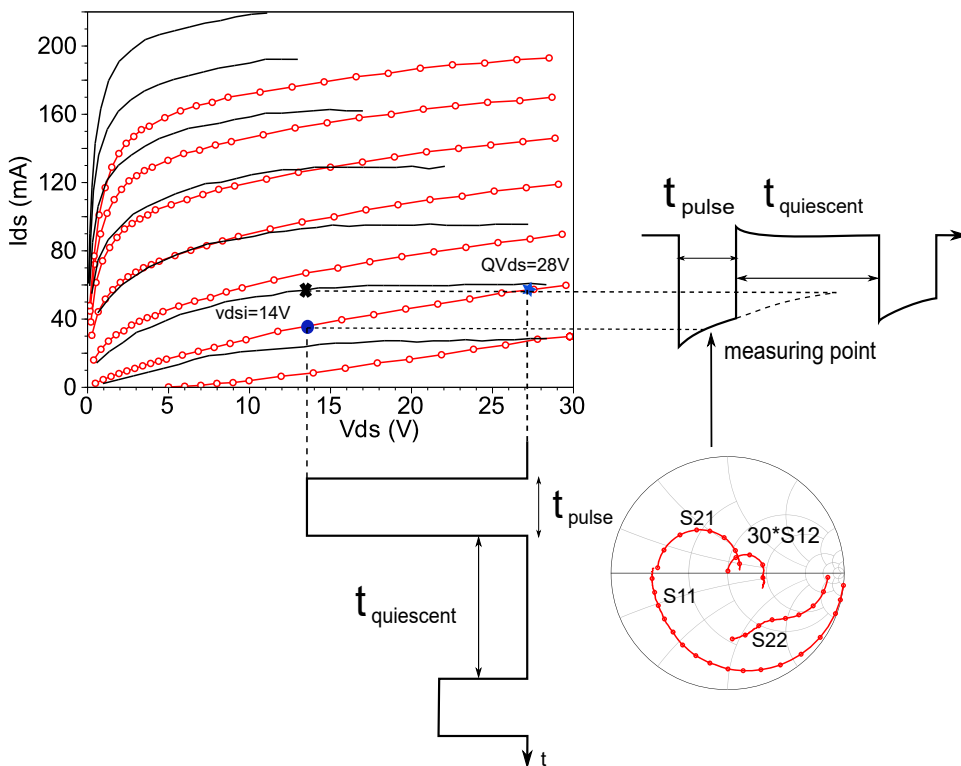


Figure 3.1: Principle of pulsed measurement, the time is not at scale. (black lines: pulsed measurement at  $QV_{ds} = 0$  V, red marked lines: pulsed measurement at  $QV_{ds} = 28$  V).

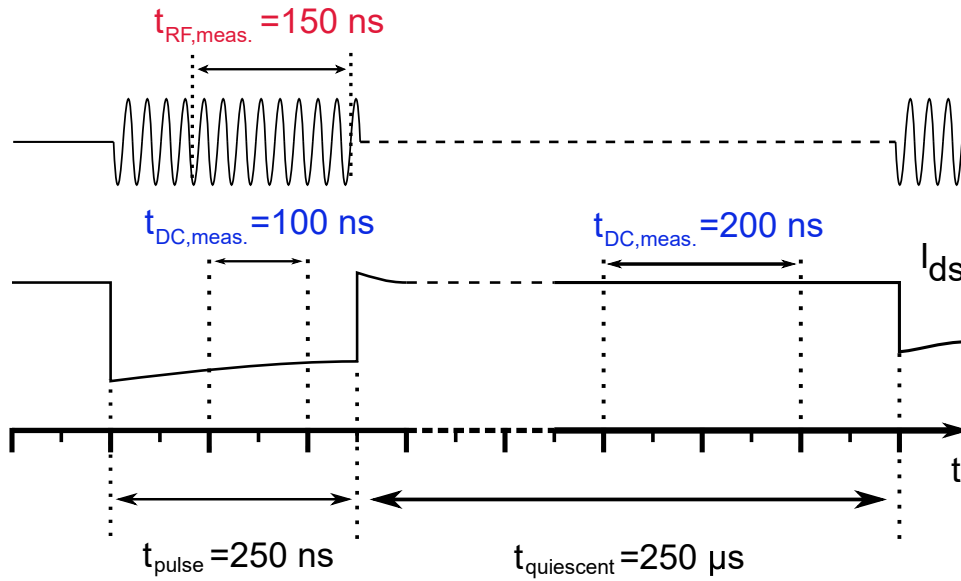


Figure 3.2: Time-domain profile of the used pulsed S-parameter measurements.

pulse.

2. Positive  $v_{ds}$  variation. In this case,  $v_{ds}$  is pulsed from the lower voltage to the steady-state. The response of the current is much faster, which can be explained by a shorter time constant of the respective trapping process, i.e., capture process.

Fig. 3.2 illustrates several important time constants in the adopted multi-bias pulsed S-parameter measurement. This measurement consists of two parts: DC and S-parameter measurements.

For DC measurements, multiple measurements were made within a 100 ns measuring aperture during the pulse and averaged together to generate a single reading.

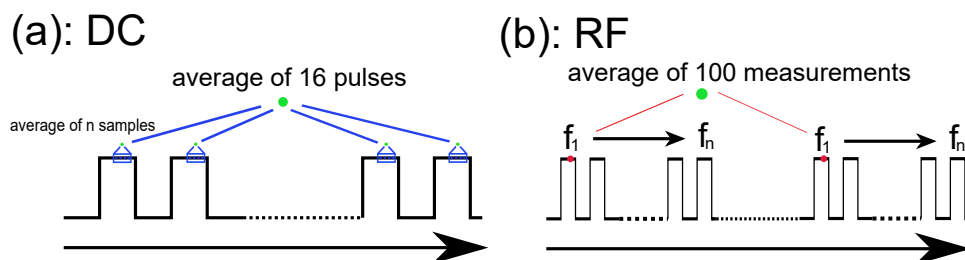


Figure 3.3: Pulse measurement data reading technique (a: DC data reading method, b: RF data reading method).

Following that, the pulse was repeated many times and the final reading takes the average of these pulses as shown in Fig. 3.3(a). The pulsed S-parameter data reading is more complicated. First of all, the pulsed measurement system triggers the VNA measuring as many frequency points as possible within the measuring aperture in one pulse, this continues in the next pulses until all frequency points are measured. Next, in order to improve the accuracy of S-parameter measurement data reading, the frequency sweep should be repeated many times and the readings averaged to get a single measurement value as shown in Fig. 3.3(b). In our case, three frequency points were measured within a 150 ns measuring aperture during a pulse with pulse length of 250 ns. The frequency swept from 400 MHz to 40 GHz in 100 MHz steps were repeated 100 times to generate the final measurement data. Moreover, the DC measurements were also made at the end of the quiescent condition. These measurements are carried out to make sure that the output voltage and current really return to the steady-state.

## 3.2 Pulsed S-Parameter Measurement Test Bench

A schematic of the used multi-bias pulsed S-parameter measurement setup is shown in Fig. 3.4. As seen in this figure, this pulsed measurement system consists of

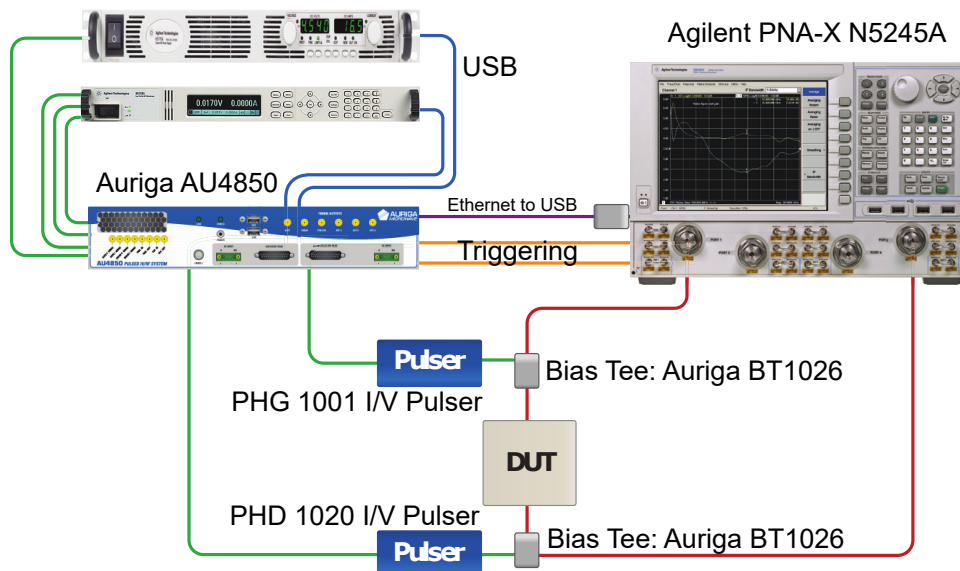


Figure 3.4: Schematic of the used pulsed measurement setup including pulsed I-V and pulsed S-parameter.

several components, e.g., the pulsed I/V and RF characterization system *Auriga AU4850*, a vectorial network analyzer *Agilent PNA-X N5245A*, external power supplies, and two pulser heads.

The Agilent network analyzer *Agilent PNA-X N5245A* was used, since it is fully integrated with the pulsed I/V and RF characterization system *Auriga AU4850*. The *PNA-X* software controls the setup and measurement task while the *AU4850* controls the timing and triggering used to coordinate the pulsed DC and S-parameter measurements. Moreover, the *AU4850* is supplied with two external and interchangeable pulser heads that generate the pulses and allow the pulser circuitry to be located closer to the device under test, minimizing signal degradation due to transmission line effects. Moreover, the *AU4850* comes with four Agilent external power supplies to provide the quiescent and non-quiescent voltages for the gate and drain.

The bias tees (*Auriga BT1026*) used here for the pulsed S-parameter measurement must be capable of handling low pulse-width, high currents and voltages and support very high frequencies (75 ns, 40 GHz, 150 V, and 2 A). The two external pulser heads are *Auriga PHG 1001* ( $\pm 20$  V, 100 mA, and 2 W) and *Auriga PHD 1020* (220 V, 2 A, and 40 W) for gate and drain port, respectively.

### 3.3 Pulsed Measurement Characteristics

For characterizing high-power AlGaIn/GaN HEMT devices, which generally generate unwanted heat known as “self-heating effect” and suffer from trapping effects, several types of device characterization are required. The efficiency of the characterizations mainly depends on capturing the nonlinear dispersion in drain-current. However, under DC condition, it is impossible to separate these effects. Hence, the pulsed measurements tend to be the most fitting characterization technique compared to conventional DC and CW measurements. [83–86]. In this section, the advantages and the limitation of pulsed measurements will be discussed.

#### 3.3.1 Device Self-Heating Reduction

As mentioned before, the pulsed measurements are able to reduce self-heating allowing the device to be modeled under isothermal operating conditions in both their linear and non-linear operating regions. However, this is only correct, if several

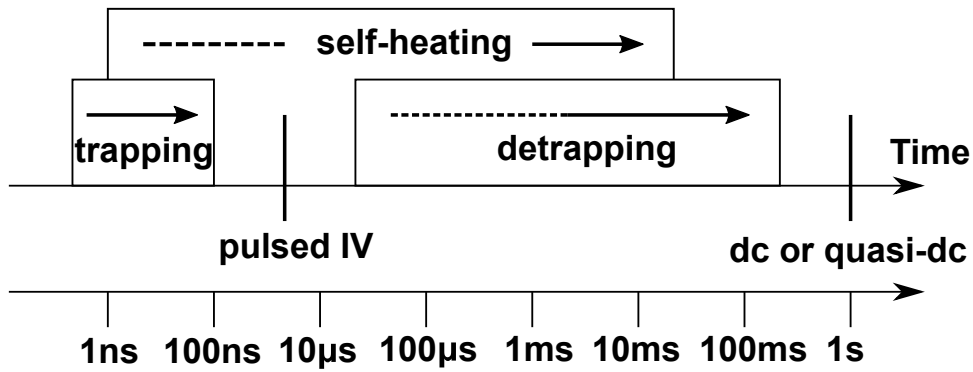


Figure 3.5: Position of the most common measurements in transistor's typical time range [81].

conditions are satisfied for the pulsed measurements:

- The pulse length should be shorter than the time constants associated with self-heating to eliminate self-heating during the measurement pulse [88].

Fig. 3.5 shows the time evolution of different dispersive effects that occur under RF drive [81]. It is evident, the pulse length should be short enough to completely eliminate the self-heating effects, which is impossible. In real cases, a pulse length of 200 ns up to 400 ns will be used to reduce the impact of the self-heating effects. In this work, the pulse length is 250 ns.

- The duration of the quiescent condition should be long enough to make sure the device could return to its steady-state conditions after each measurement pulse.

As seen in Fig. 3.5, the duration of the quiescent condition should lie in microsecond range in order to eliminate the current change induced by self-heating effects during the pulse. However, it is impossible in our case, since the number of the measurement samples in the quiescent condition is limited by the duration of the quiescent condition: the longer the duration of the quiescent condition is, the fewer samples can be placed by the oscilloscope. Hence, the use of the long duration of the quiescent condition will significantly increase the inaccuracy of measurement. In our case, the duty cycle is 0.1 %, which means the duration of the quiescent condition is 250 µs when the pulse length equals 250 ns.

Fig. 3.6 shows the drain-source currents measured at the end the quiescent condition after the pulses with dynamic bias points ( $v_{gs}, v_{ds}$ ). At the end of the quiescent



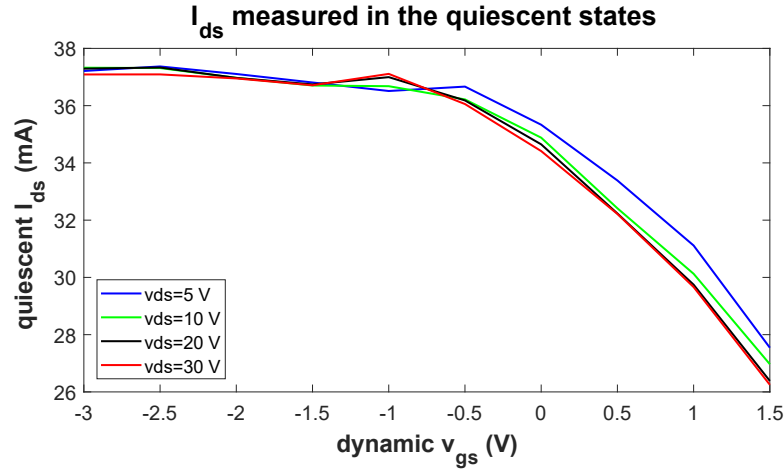


Figure 3.6: Drain-source currents measured at the end of the quiescent condition after after pulses with different dynamic biases ( $v_{gs}, v_{ds}$ ). The pulsed measurement was performed at  $QV_{gs} = -2.3$  V and  $QV_{ds} = 28$  V.

condition, the drain-source current should return to its steady-state, i.e., the current of quiescent bias ( $QV_{gs} = -2.3$  V and  $QV_{ds} = 28$  V). However, it is evident that the drain-source current dramatically decreases with the increase of dynamic  $v_{gs}$  when  $v_{gs} > 0$  V. This phenomenon is mainly due to the self-heating, which occurs during the pulses and cannot be eliminated by the short pulse period. The junction temperature is completely determined by the electrical data at each operating point through the simple equation as shown in Equation 3.1 (for simplicity purposes, the thermal capacitance is neglected here).

$$T_j = T_{amb} + R_{th} \cdot i_{ds} \cdot v_{ds} \quad (3.1)$$

where  $T_{amb}$  is the ambient temperature and equals the room temperature 20 °C in this work,  $R_{th}$  is the thermal resistance and for our DUT equals 30 °C/W. Hence, in the case of dynamic  $v_{ds} = 20$  V, the change of the junction temperature from  $v_{gs} = 0$  V to  $v_{gs} = 1.5$  V can be calculated as:

$$\Delta T_j = R_{th} \cdot \Delta QI_{ds} \cdot QV_{ds} = 5.5 \text{ } ^\circ\text{C} \quad (3.2)$$

However, compared with the normal  $T_j$  in the quiescent condition (52 °C), this change is negligible and will not impact the performance of the device. Fig. 3.7 supports our suggestion.

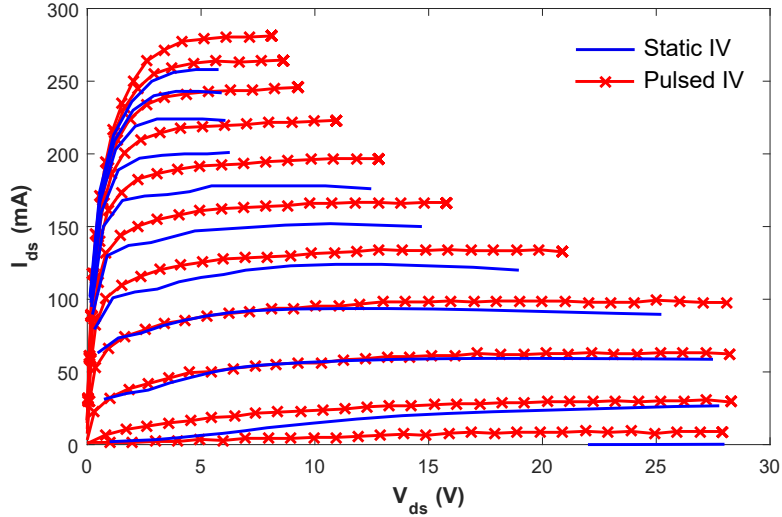


Figure 3.7: Comparison between DC I/V characteristics and pulsed I/V characteristics at  $QV_{gs} = QV_{ds} = 0$  V with 250 ns pulses and 0.1 % duty cycle.

Fig. 3.7 shows a comparison between the DC I/V characteristics and the pulsed I/V characteristics at  $QV_{gs} = QV_{ds} = 0$  V with 250 ns pulses and 0.1 % duty cycle. As expected, the impact of self-heating can be significantly observed in high  $v_{gs}$  and  $v_{ds}$  region of the DC I/V characteristics. In the pulsed I/V characteristics, the impact of self-heating effects is almost impossible to be observed.

### 3.3.2 Traps Isolation

The trap states are normally controlled by the supply voltages, so if we determine a model with pulsed measurements, the trap state should be considered as the same as the trap state under used quiescent bias. In the case of AlGaIn/GaN FETs, this assumption is not entirely correct. However, due to the asymmetry in time constants associated with capture and release of charge traps, a pulsed characterization is not enough in order to keep the trap states fixed. In particular, owing to the fast capturing time constants, the trap state seems to be dependent on the dynamic voltages  $v_{ds}$ ,  $v_{ds}$ .

Fig. 3.8 presents a comparison between three sets of pulsed I/V curves for a constant  $QV_{gs} = -2.3$  V and different values of  $QV_{ds} = 8$  V, 15 V, and 28 V. The impact of trapping effects is clearly seen in all of these three curves. When the dynamic  $v_{ds}$  is pulsed to a value below  $QV_{ds}$  (emission process), the curves show so-called knee-walkout effect, that is more pronounced for higher  $QV_{ds}$ . When the

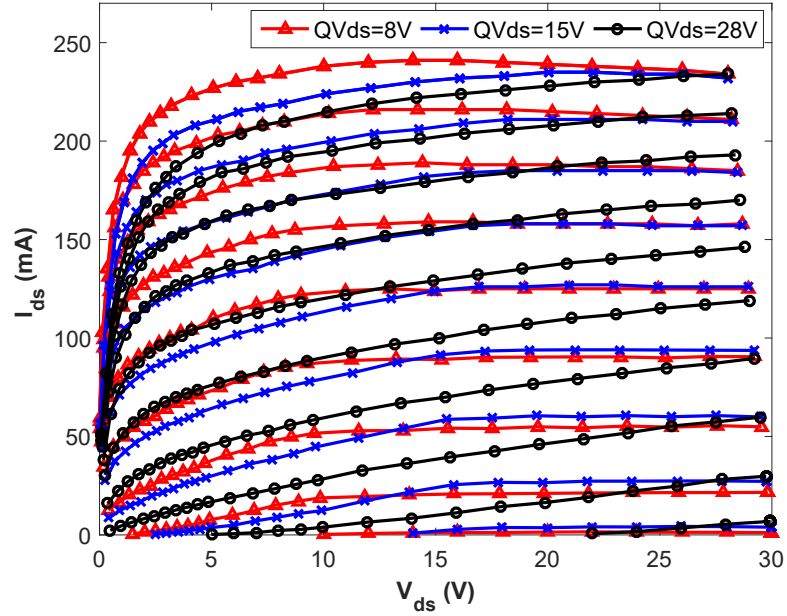


Figure 3.8: Comparison of three sets of pulsed I/V curves for pulse quiescent gate voltage  $QV_{gs} = -2.3$  V and pulse quiescent drain voltages  $QV_{ds} = 8$  V, 15 V, and 28 V.

dynamic  $v_{ds}$  is pulsed to voltages above  $QV_{ds}$  (capture process), the three curves are very similar, as expected from physics [89].

Recently, the dynamic trapping effects observed in pulsed I/V characteristics have also been identified by the double-pulse experiment [90, 91], which not only isolates the trapping effects from thermal effects but also enables the separation of the trapping and detrapping processes.



## Chapter 4

# GaN HEMT Modeling Based on Pulsed S-Parameter Measurements

In GaN HEMT modeling process, the most important and difficult step of the non-linear model extraction is to determine the drain-source current model parameters. In order to predict the I/V characteristic accurately, several types of effects such as self-heating effects and trapping effects have to be included in the model.

However, the status of GaN HEMT trap models can be considered to be quite close to be solved in the academic world [47–52], but still far away from being accessible to circuit designers, since no trap model so far is available in any commercial EDA tool. This leaves us in a situation, where foundries cannot build their design kits easily based on the models provided by the major simulation packages. Also designers face the difficulty that they will not be supplied with GaN HEMTs model parameters, and on the other hand, quickly extracting model parameters the traditional way might not lead to satisfactory accuracy.

Given this situation, it is required to find a way to optimize the accuracy of standard HEMT models applied to GaN HEMT devices. Since we know that the lack of a trapping description in these models prevents the formulation of a generally accurate model, the task is to optimize the model with a certain transistor operation in mind. In the best case, one obtains a good model for a certain application taking into account that it might not be usable under other operation conditions.

Pulsed measurements are normally the key solutions to extract the drain source current model parameters including trapping effects [92]. In this chapter, the parameters of the Chalmers model are extracted by using pulsed S-parameter measure-

ments. The extracted model targets the power amplifier operation of the device at a fixed drain supply voltage (28 V), which is a reasonable approach for many practical applications. The idea behind this work is that basically the DC supply voltages determine the trap states. If the model is determined from pulsed S-parameters using this bias as quiescent bias point, the trap state should be the same as in a power amplifier application. Hence, one would expect high model accuracy, although only for a single bias point.

In the first section, the impact of traps on the extraction of extrinsic parameters and small-signal intrinsic capacitances will be presented. The next section addresses the question to what extent these pulsed S-parameters can be exploited to obtain an accurate model valid for a dedicated bias point. Here, the large-signal modeling process with pulsed S-parameter and its differences to the traditional modeling will be focused on. The resulting large-signal model is then validated by comparing simulation and load-pull measurements.

## 4.1 Small-Signal Modeling

The procedure for the extraction of the small-signal parameters has been presented in Chapter 2. It is based on two S-parameter datasets: “cold-FET” S-parameters for extrinsic parameters and “hot-FET” S-parameters for intrinsic parameters.

As mentioned previously, the use of pulsed measurements ensure a better large-signal model as long as the pulses are kept short enough so that the self-heating and trapping effects will not affect the device characteristics [88]. However, in this section, the aim is to find out whether the traps impact the extraction results of some small-signal equivalent circuit parameters such as the extrinsic parameters and intrinsic capacitances. Hence, several pulsed multi-bias S-parameter measurements with different quiescent bias points of  $QV_{gs} = -2.3$  V and  $QV_{ds} = 8$  V, 15 V, and 28 V will be used to determine the small-signal equivalent circuit of the DUT at different trap states.

### 4.1.1 Extrinsic Parameters

As discussed in Chapter 2, the small-signal modeling starts with the extraction of extrinsic elements, and the procedure for extrinsic parameter extraction is based on

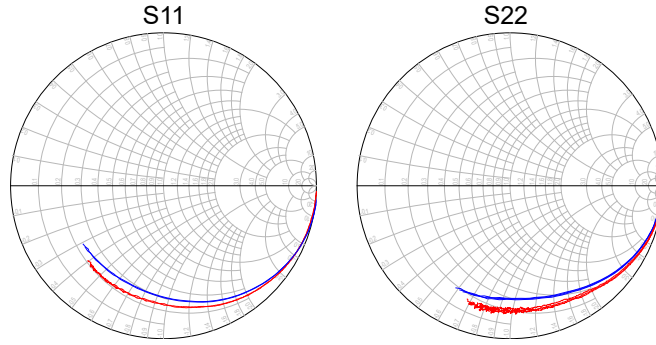


Figure 4.1: Static (blue lines) and pulsed (red lines,  $QV_{gs} = -2.3$  V,  $QV_{ds} = 28$  V) cold S-parameters,  $S_{11}$  and  $S_{22}$ , at  $v_{gs} = -4$  V,  $-6$  V, and  $-8$  V for frequency up to 40 GHz.

S-parameters in “cold-FET” condition. Under this condition, the DUT can be seen as in a passive condition and the intrinsic elements can be easily derived.

#### A): Capacitances ( $C_{pg}$ , $C_{pd}$ ) extraction

At first, the gate and drain pad capacitances,  $C_{pg}$  and  $C_{pd}$ , can be estimated from pinch-off cold-FET S-parameter measurements by using equations (2.2) and (2.3). As an example for one trap state, Fig. 4.1 shows the comparison between the static and pulsed ( $QV_{gs} = -2.3$  V,  $QV_{ds} = 28$  V) pinch off cold S-parameters  $S_{11}$  and  $S_{22}$  at gate voltages below pinch-off for the frequency up to 40 GHz. It can be seen that static and pulsed  $S_{11}$  and  $S_{22}$  show almost the same capacitive behavior at all used gate voltages.

With this in mind, it can be assumed that the determined values of parasitic capacitances using these different S-parameter data should be very close. Fig. 4.2 shows comparison between the  $C_{pg}$  and  $C_{pd}$  extraction results based on static and pulsed measurements at  $QV_{ds} = 28$  V, which supports our suggestion. Furthermore, the detailed values of extracted  $C_{pg}$  and  $C_{pd}$  including those extracted from pulsed measurements at different  $QV_{ds}$  can be found in Table 4.1.

Table 4.1: Extracted values of extrinsic capacitances  $C_{pg}$  and  $C_{pd}$  based on static and pulsed measurements

	static meas.	pulsed meas. $QV_{ds} = 8$ V	pulsed meas. $QV_{ds} = 15$ V	pulsed meas. $QV_{ds} = 28$ V
$C_{pg} = C_{pd}$	5.3 fF	6.3 fF	6.8 fF	6.5 fF

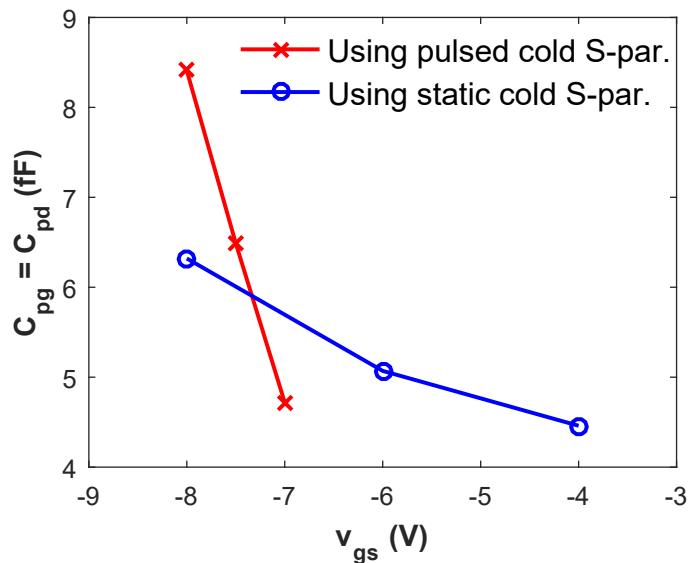


Figure 4.2: Comparison between the  $C_{pg}$  and  $C_{pd}$  extraction results based on static measurements (blue line with circles) and based on pulsed measurements at  $QV_{ds} = 28$  V (red line with x).

### B): Inductances ( $L_g, L_d, L_s$ ) and Resistances ( $R_g, R_d, R_s$ ) extraction

After extracting the parasitic capacitance parameters, the other extrinsic parameters such as inductances ( $L_g, L_d, L_s$ ) and resistances ( $R_g, R_d$ ) can be extracted by using cold S-parameters at positive gate voltages.

Fig. 4.3 shows the static and pulsed cold S-parameters  $S_{11}$  and  $S_{22}$  at  $v_{gs} = 1.9$  V and 2 V for the frequency up to 40 GHz. As can be seen, static and pulsed  $S_{11}$  and  $S_{22}$  are both inductive on the upper-left quadrant of the Smith-chart. The

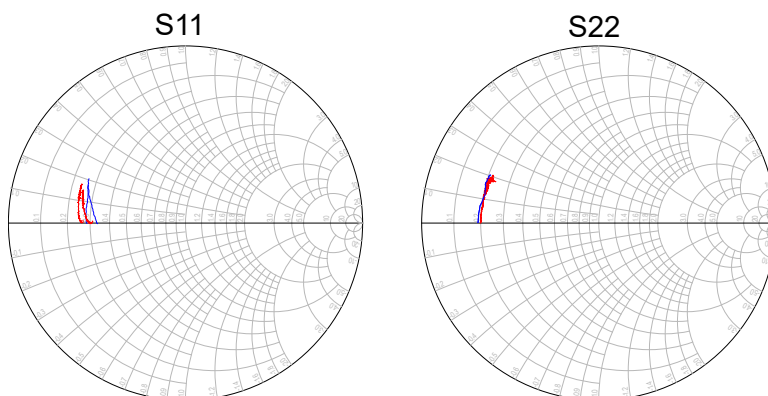


Figure 4.3: Static (blue lines) and pulsed (red lines,  $QV_{gs} = -2.3$  V,  $QV_{ds} = 28$  V) cold S-parameters,  $S_{11}$  and  $S_{22}$ , at  $v_{gs} = 1.9$  V and 2 V for frequency up to 40 GHz.



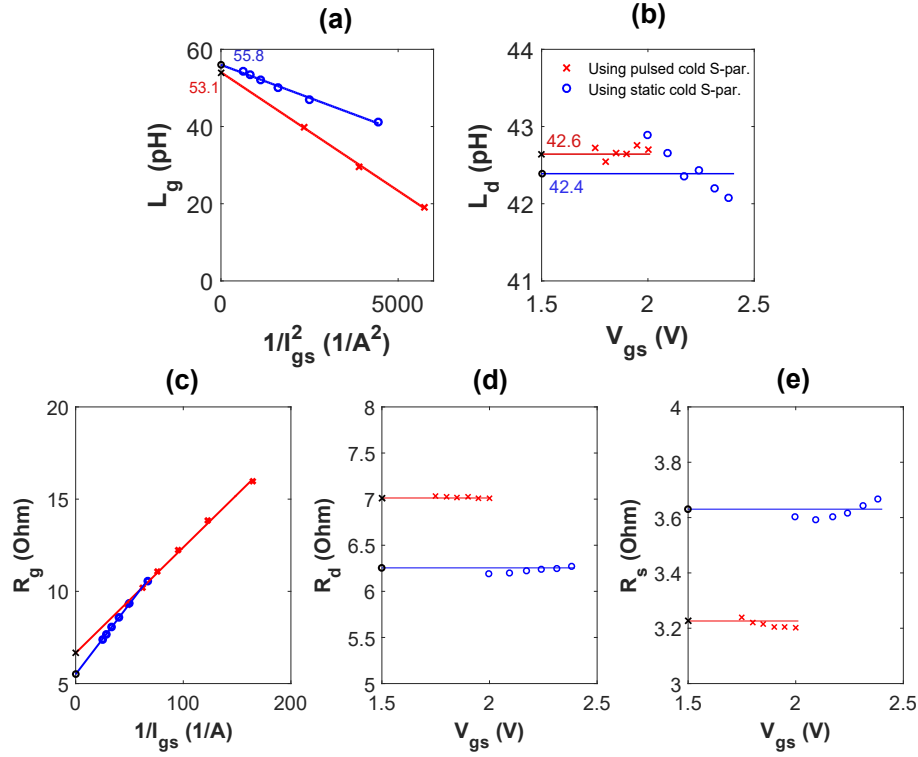


Figure 4.4: Comparison between the extrinsic inductance and resistance extraction results based on static measurements (blue lines and circles) and based on pulsed measurements at  $QV_{ds} = 28$  V (red lines and x).

inductances,  $L_d$  and  $L_g$ , can be identified from the imaginary parts of Z-parameters by using the equations (2.9) and (2.10). It is evident that static and pulsed  $S_{11}$  and  $S_{22}$  present almost the same inductive behavior, so the extracted values of  $L_d$  and  $L_g$  should also be very close. The extraction results of inductances, which values can be found in Figures 4.4(a)(b), validate them.

Moreover, static and pulsed  $S_{11}$  and  $S_{22}$  shown in Fig. 4.3 present the resistance as real part on the Smith chart. Using equations (2.11) and (2.13) allows us to determine the resistances  $R_g$ ,  $R_d$ , and  $R_s$ . Now, we meet the same situation as for inductances, namely the real parts of static and pulsed  $S_{11}$  and  $S_{22}$  are also very similar. Thus, it is clearly shown that the extracted resistances using both kind of S-parameters should also be similar, and this is validated in Figures 4.4(c)(d)(e), which reveal the extracted results by using equations (2.11) and (2.13). Finally, the extrinsic inductances and resistances determined so far are summarized in Table 4.2.

Table 4.2: Extracted values of extrinsic inductances and resistances based on static and pulsed measurements

	static meas.	pulsed meas. $QV_{ds} = 8 \text{ V}$	pulsed meas. $QV_{ds} = 15 \text{ V}$	pulsed meas. $QV_{ds} = 28 \text{ V}$
$L_g$	55.8 pH	48.7 pH	48.7 pH	53.1 pH
$L_d$	42.4 pH	42.3 pH	42.6 pH	42.6 pH
$R_g$	6.1 $\Omega$	5.2 $\Omega$	5.2 $\Omega$	5.1 $\Omega$
$R_d$	6.9 $\Omega$	5.6 $\Omega$	6.0 $\Omega$	6.2 $\Omega$
$R_s$	3.6 $\Omega$	2.9 $\Omega$	3.1 $\Omega$	3.2 $\Omega$

From Table 4.1 and 4.2 it is evident that the choice of the trap state, i.e., quiescent bias, will not influence the extraction results of the parasitic parameters.

#### 4.1.2 Intrinsic Parameters

The bias-dependent intrinsic parameters were then extracted based on the extrinsic parameters already determined. This is a crucial step in GaN HEMT modeling since these parameters will be the initial basis for the final extraction of a nonlinear model.

The proposed extraction process, in terms of the admittance matrix of the intrinsic transistor, was already discussed in Chapter 2. It has to be noted that according to equations (2.16) - (2.21) the intrinsic parameters are also dependent on the frequency. Hence, it is necessary to adopt the S-parameters in the frequency range where a constant and logical value can be achieved for intrinsic parameters.

##### **Intrinsic capacitances and $\tau$ :**

The comparison between the extracted values of the intrinsic capacitances and  $\tau$ , versus  $v_{ds}$ , based on static S-parameter measurements and pulsed S-parameter measurement at  $QV_{ds} = 28\text{V}$  is shown in Fig. 4.5. Furthermore, the comparison between the extracted values based on pulsed S-parameter measurements at different  $QV_{ds}$  is shown in Fig. 4.6.

It can clearly be observed that the difference between intrinsic capacitances  $C_{gs}$ ,

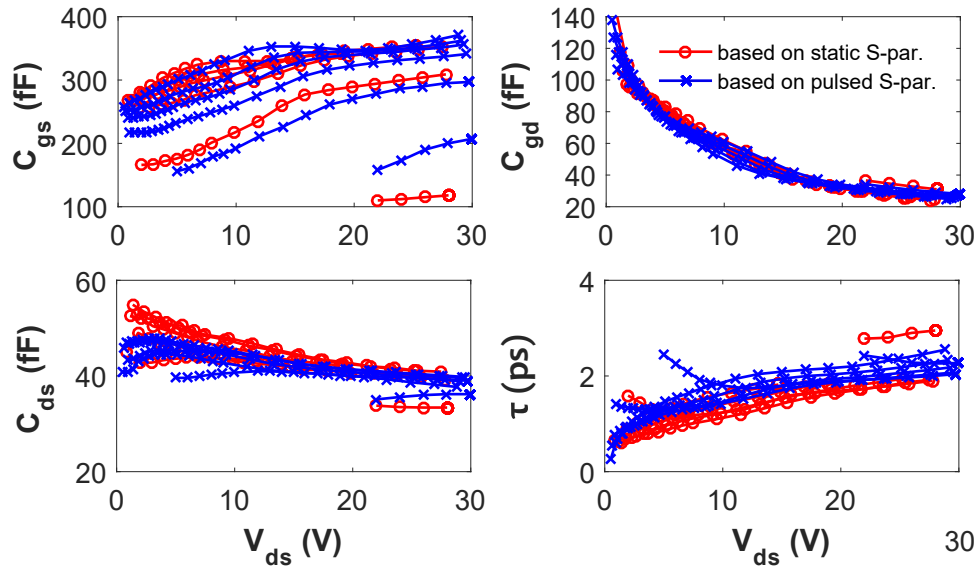


Figure 4.5: Comparison between the extracted values of the small-signal intrinsic capacitances and  $\tau$  versus  $v_{ds}$  based on static measurements (blue lines with x) and based on pulsed measurements at  $QV_{ds} = 28$  V (red lines with circles).

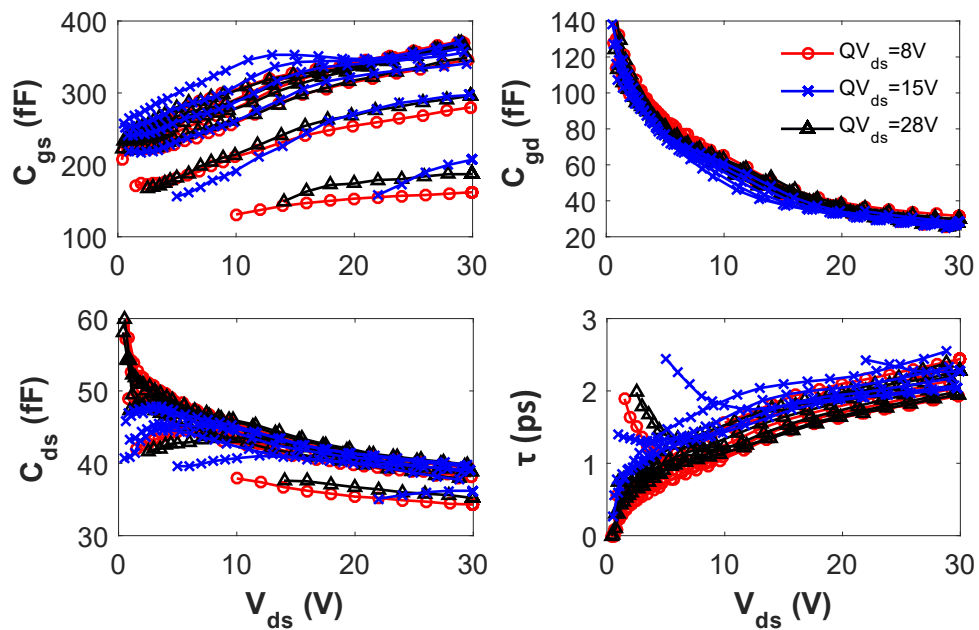


Figure 4.6: Comparison between the extracted values of the intrinsic capacitances and  $\tau$  of small-signal model versus  $v_{ds}$  based on pulsed measurements at  $QV_{ds} = 8$  V (red lines with circles),  $QV_{ds} = 15$  V (blue lines with x),  $QV_{ds} = 28$  V (black lines with triangle).

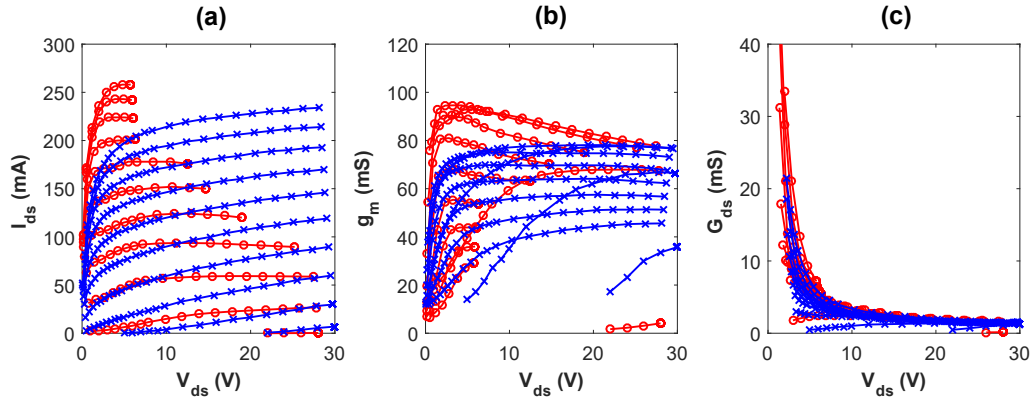


Figure 4.7: Comparison between (a): I/V characteristics, (b) extracted  $g_m$ , (c): extracted  $G_{ds}$  based on static (red lines with circles) and pulsed (blue lines with x,  $QV_{ds} = 28$  V) (blue lines with x) measurements.  $v_{gs}$  is from -3 V to 1.5 V in 0.5 V steps.

$C_{gd}$ ,  $C_{ds}$  and  $\tau$  extracted from static and pulsed S-parameter measurements is not significant. And also can be seen, that the choice of  $QV_{ds}$  for pulsed S-parameter measurements doesn't impact the extraction results of intrinsic capacitances and  $\tau$  of small-signal equivalent circuit.

#### $i_{ds}$ related parameters: $g_m$ and $G_{ds}$ :

Due to the self-heating effects and trapping effects, the deviation between static and pulsed I/V characteristics should be significant as shown in Fig. 4.7(a).  $g_m$

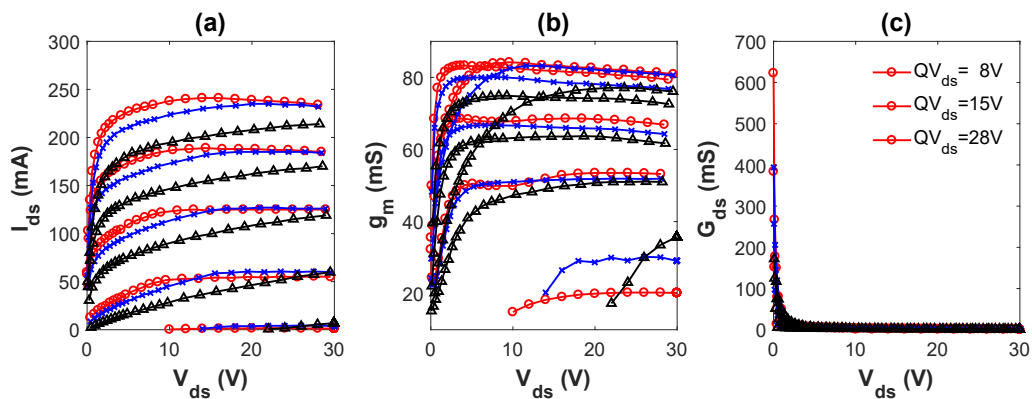


Figure 4.8: Comparison between (a): I/V characteristics, (b) extracted  $g_m$ , (c): extracted  $G_{ds}$  based on pulsed measurements at  $QV_{ds} = 8$  V (red lines with circles),  $QV_{ds} = 15$  V (blue lines with x), and  $QV_{ds} = 28$  V (black lines with triangle).

and  $G_{ds}$  represent the rate of change of the drain current with respect to different quiescent bias points. Hence, the extracted values of  $g_m$  and  $G_{ds}$  from static and pulsed measurements are completely different as shown in Fig. 4.7(b)(c).

For pulsed S-parameter measurements at different  $QV_{ds}$ , the trap states are controlled by the supply voltage, i.e., below  $QV_{ds}$ , they are dependent on  $QV_{ds}$ , so the measured drain currents from different  $QV_{ds}$  in this region should differ from  $QV_{ds}$  to  $QV_{ds}$ ; above  $QV_{ds}$ , the trap states are dependent on dynamic drain voltage, so the measured drain current from different  $QV_{ds}$  at the same dynamic drain voltage should be the same [89]. This rule should also be applicable to  $g_m$  and  $G_{ds}$ , and this can be verified in Fig. 4.8.

### 4.1.3 Small-Signal Model Verification

The small-signal modeling is verified by comparing the simulated S-parameters with the measured S-parameters the models are derived from. The verification is

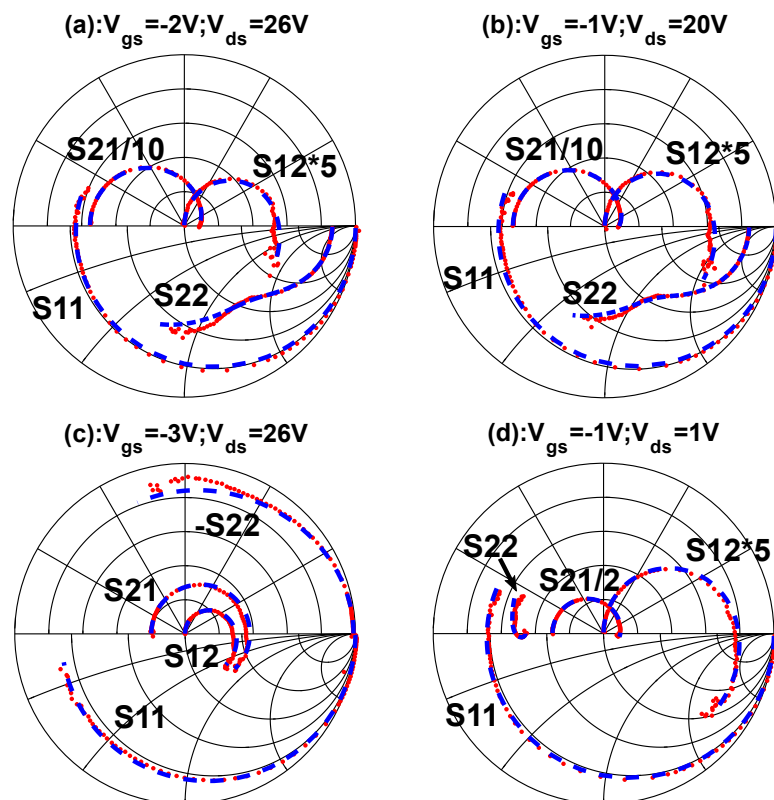


Figure 4.9: Measured (red dots) and modeled (blue dashed lines) static S-parameters from 50 MHz to 50 GHz at given bias points.

required over the complete bias region to check whether the extracted small-signal models based on static and pulsed S-parameters are able to predict the measured static and pulsed S-parameters over the considered operating bias range.

### Small-signal model based on static measurements

Fig. 4.9 shows the measured and modeled static S-parameters at the bias voltages in the pinch-off, ohmic, and saturation regions. The small-signal model is extracted based on static S-parameters.

A good modeling agreement is observed at both active and pinch-off regions. Moreover, the accurate modeling performances of  $S_{11}$  and  $S_{22}$  shown in this figure demonstrate the good agreement of intrinsic capacitances extracted based on the procedure discussed in Section 2.2.2. Moreover, it is well known that  $S_{12}$  and  $S_{21}$  are basically influenced by the drain current. Therefore, the good correspondence with the modeled results indicates that not only the drain current but also its differential information have correctly been represented by the extracted small-signal model.

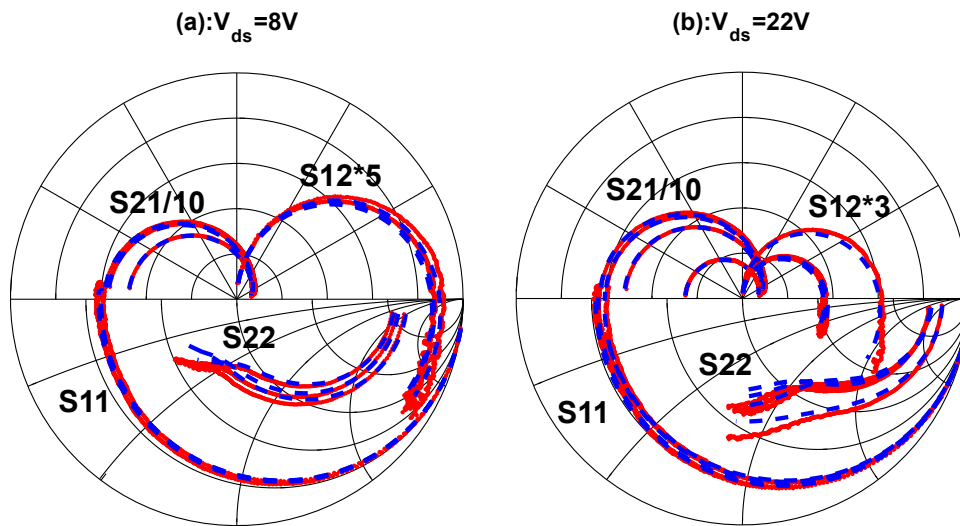


Figure 4.10: Measured (red dots) and modeled (blue dashed lines) pulsed S-parameters at  $QV_{ds} = 15$  V from 400 MHz to 40 GHz at dynamic bias voltages: (a)  $v_{gs} = -2$  V to 0 V in 1 V steps,  $v_{ds} = 8$  V ; (b)  $v_{gs} = -3$  V to 0 V in 1 V steps,  $v_{ds} = 22$  V.

### Small-signal model based on pulsed measurements

As an example of the small-signal model verification with the small-signal model extracted from pulsed S-parameter measurement, Fig. 4.10 shows the measured and modeled pulsed S-parameters at  $QV_{ds} = 15$  V. Here, we focus on the two following regions according to different processes of drain-lag effects, i.e., emission and capture process:

a) if the dynamic  $v_{ds}$  is below the used quiescent drain voltage  $QV_{ds}$ , the drain voltage is pulsed down during a pulse. In this case, emission process predominates for drain-lag-related traps and the traps remain overcharged related to the  $QV_{ds}$ .

b) if the dynamic  $v_{ds}$  is higher than used quiescent drain voltages  $QV_{ds}$ , the drain voltage is now pulsed up during a measurement pulse period. In this case, capture process predominates.

A good fit can be observed at both active and pinch-off regions under each process. The satisfying small-signal performance indicates the suitability of the extraction procedure by using pulsed S-parameter measurements and also the accuracy of extrinsic element values.

## 4.2 Large-Signal Modeling

In this section, two sets of large-signal models, which were derived from the small-signal model extracted from static and pulsed S-parameter measurement, will be presented.

As already discussed in the last chapter, pulsed measurement is understood to be able to freeze traps at quiescent bias point. Hence, the selection of quiescent bias allows us to capture the “real” trap state of a certain transistor operation. In this way, a good modeling accuracy in prediction of the transistor large-signal behavior can be achieved even without a dedicated trap model.

This section addresses the question whether the model based on pulsed S-parameter measurement at  $QV_{ds} = 28$  V achieves a better modeling accuracy in describing the large-signal behavior biased at  $v_{ds} = 28$  V than that based on static measurement. At first, the large-signal modeling results with pulsed S-parameter at  $QV_{ds} = 28$  V will be illustrated, and then the results will be compared with the traditional modeling results.

### 4.2.1 Drain-Source Current Model Parameters

The large-signal model (Chalmers model) extraction procedure has already been described in Section 2.3. The Chalmers drain-source current model parameters were determined by fitting the characteristic curves with the least square algorithm in a Scilab program [68].

For pulsed measurements, the quiescent bias is fixed at a single bias:  $QV_{gs} = -2.3$  V and  $QV_{ds} = 28$  V to provide a fixed trap state in the modeling. In order to reduce self-heating of the devices, the drain-source current was always measured in short pulses. Hence, the pulsed I/V characteristic can reach the high power region while the static I/V characteristics stop before reaching the “hot” region. In this work, the pulsed gate voltage is swept from below pinch-off to +1 V, and the pulsed drain voltage is swept from 0 V to 30 V, thereby covering the relevant part of the output I/V and transfer characteristics field completely. In contrary, the static mea-

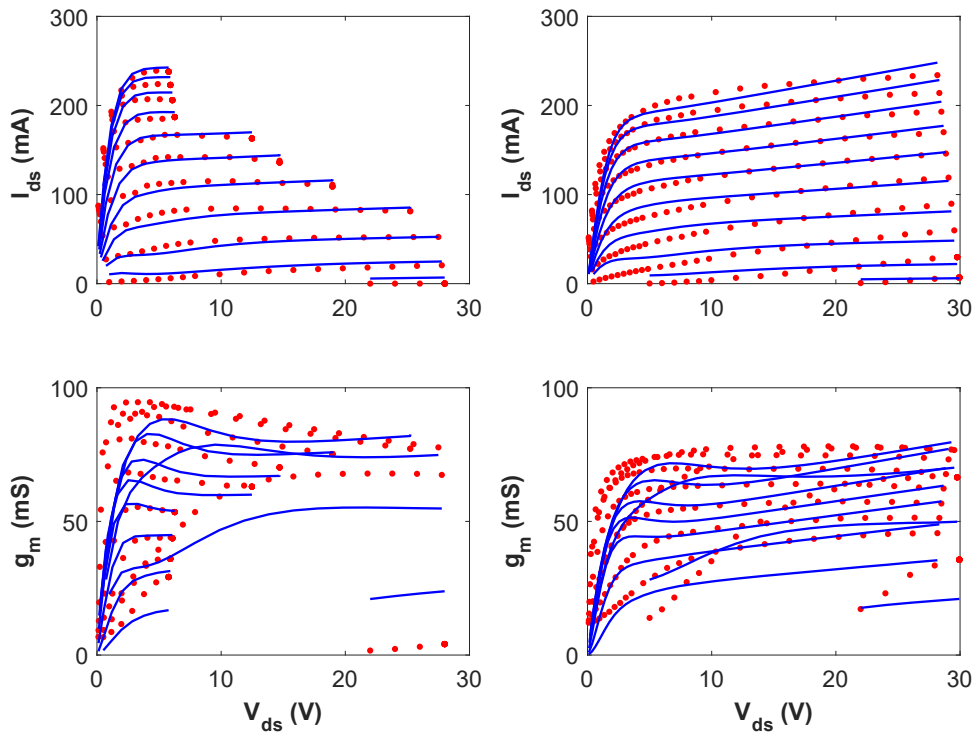


Figure 4.11: Measured (symbols) and modeled (lines)  $i_{ds}$  and  $g_m$  of the  $2 \times 125 \mu\text{m}$  GaN HEMT, described by Angelov current model, and comparison between model based on static S-parameter (at left hand side) and pulsed S-parameter at  $QV_{ds} = 28$  V (at right hand side).



measurements were performed within limited voltage ranges to protect our DUT from being destroyed.

Fig. 4.11 shows large-signal model predictions of  $i_{ds}$  and  $g_m$  based on static S-parameters and pulsed S-parameters together with the DC and small-signal parameters against which the models were fitted. Since the model cannot account for the difference between  $G_m = \partial i_{ds}/\partial v_{gs}$  and  $g_m$  determined from S-parameter measurements, significant deviations between modeled and simulated values are observed.

For each large-signal model, the model parameters given in equations (2.22 - 2.26) were optimized in order to provide best RF prediction without sacrificing too much accuracy concerning the DC current. It is evident that relying on pulsed S-parameters allows a much better fit of  $i_{ds}$  and  $g_m$ .

Moreover, for  $G_{ds}$ , the Chalmers model employs a RC branch parallel to  $i_{ds}$ , which has already been presented in Section 2.4.4, in order to take into account the difference between  $G_{ds}$  under DC and RF condition as follows [38]:

$$\Delta G_{ds} = G_{ds,RF} - G_{ds,DC} = \frac{1}{R_{cmin} + R_c \cdot (1 + \tanh(\psi))} \quad (4.1)$$

where  $R_{cmin}$  is the minimum dispersion resistance measured in saturated voltages and high currents,  $R_c$  is the dispersion resistance for frequency dependent output conductance, and  $\psi$  is already given in equation (2.23). Thus, it is obvious that  $\Delta G_{ds}$  is both  $v_{gs}$ - and  $v_{ds}$ - dependent and the parameters  $R_{cmin}$  and  $R_c$  can be extracted from

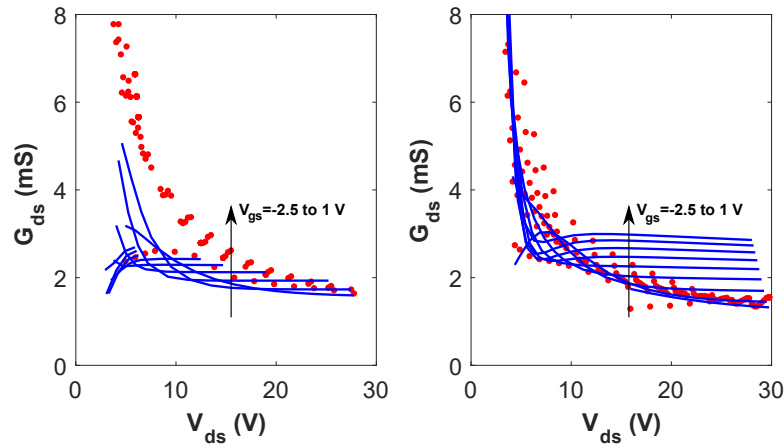


Figure 4.12: Measured (symbols) and modeled (line)  $G_{ds}$  of the  $2 \times 125 \mu\text{m}$  GaN HEMT, and comparison between model based on static S-parameter (at left hand side) and pulsed S-parameter at  $QV_{ds} = 28 \text{ V}$  (at right hand side).

the  $\Delta G_{ds}$  or from the  $G_{ds}$ -related parameters, e.g.,  $S_{22}$ .

In the extraction process  $\Delta G_{ds}$  can be calculated from the difference between  $G_{ds,RF}$  determined from S-parameter measurements and  $G_{ds,DC}$  determined from DC I/V characteristics as  $G_{ds,DC} = \partial i_{ds,DC} / \partial v_{ds}$ . Once the values of  $R_{cmin}$  and  $R_c$  are determined, a correct  $S_{22}$  and  $G_{ds,RF}$  prediction result can be expected to be produced. Fig. 4.12 shows the prediction results of  $G_{ds,RF}$  by using static and pulsed S-parameter measurements. It is evident that the prediction accuracy of  $G_{ds,RF}$  by using static S-parameters is limited in a small  $v_{ds}$  range. On the contrary,  $v_{gs}$  becomes the decisive factor for the prediction of  $G_{ds,RF}$  at high  $v_{ds}$  region by using pulsed S-parameters.

It has to be noted that the thermal resistance and temperature parameters are assumed not to vary too much within a given technology, and therefore are not extracted especially for this transistor under test, i.e., typical values of thermal model parameters were used.

## 4.2.2 Capacitance Model Parameters

The nonlinear functions chosen to fit the extracted gate-source and gate-drain capacitance data are based on the equations given in [36], and the extraction procedure is presented in Section 2.3. The drain-source capacitance  $C_{ds}$  is known to be a very weak function of bias voltage  $v_{gs}$  and  $v_{ds}$ , hence, it has been set to a constant value [36].

Fig. 4.13 shows the comparison between the extracted values of the intrinsic capacitances from standard S-parameter measurements and that from pulsed S-parameter measurements at  $QV_{ds} = 28$  V. As seen in the figure, in both cases the intrinsic capacitances of the transistor can be modeled very well by the Chalmers model formulations. And for both intrinsic capacitances the difference between extracted models from standard S-parameter measurements and pulsed S-parameter measurements is not really significant.

As illustrated in Fig. 4.6, the deviation between the small-signal model intrinsic capacitances extracted from pulsed S-parameters at different  $QV_{ds}$  can be neglected. Hence, we can supply the same values of the capacitance model parameters also for each large-signal model based on pulsed S-parameters.

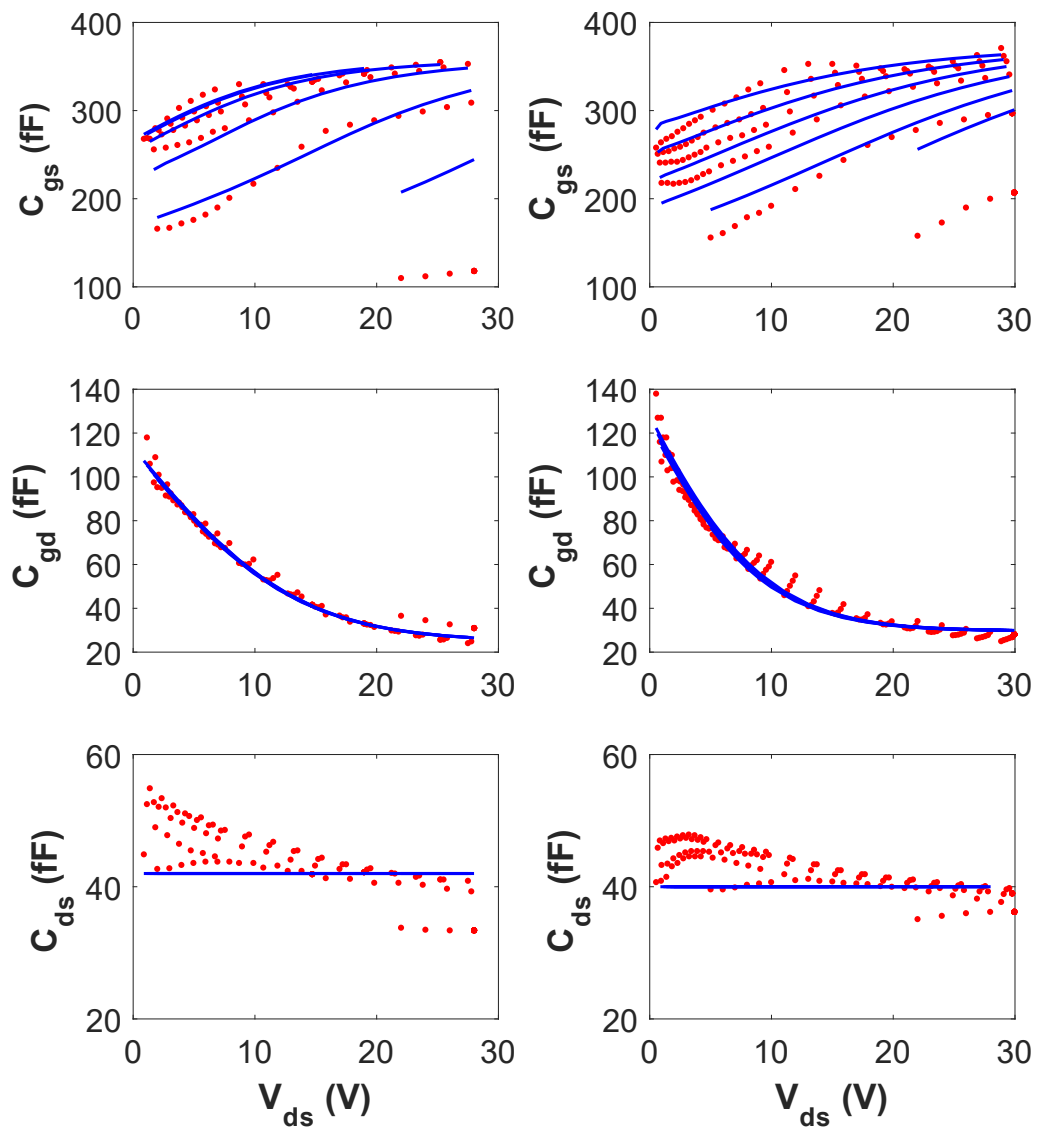


Figure 4.13: Modeled intrinsic capacitances against  $v_{ds}$  extracted from static S-parameter measurements (at left side) and pulsed S-parameter measurements (at right side); small signal model (symbols) and large signal model (lines).

### 4.3 Large Signal Model Verification

Large-signal model verification is the last but very important step in modeling process. This verification should include small-signal as well as large-signal power levels. First, the models are checked whether they are consistent with static/pulsed I/V and S-parameter measurements they have been derived from. Secondly, load-pull simulation is compared with the corresponding measurements. In this section, all simulations were performed in ADS [93] by using a Verilog-A design-kit.

#### 4.3.1 I/V Characteristics

The I/V characteristics can be split into two types: static I/V characteristics and pulsed I/V characteristics. The static I/V characteristics are obtained sweeping values of the gate and drain bias voltages with two supply sources and measuring the static drain-current for each sweep step. These measurements have following limitations: safe operation limitations, i.e., maximum voltage, maximum current, and maximum power, and non-negligible self-heating. Pulsed I/V measurements can overcome the main limitations of the corresponding static measurements. As mentioned in last chapter, pulsed I/V measurements provide a quasi-isothermal condition, since all I/V characteristics can be obtained at a constant device temperature defined by quiescent bias condition and ambient temperature. Hence, these mea-

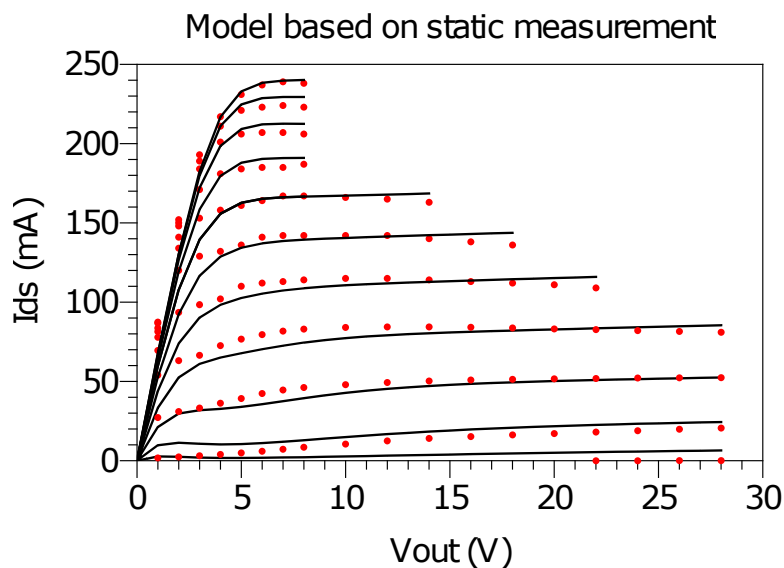


Figure 4.14: Measured (dots) and simulated (lines) static I/V characteristics.

measurements can offer a way to investigate the characteristic of the device in ranges where damage or deterioration can occur [94]. Moreover, the pulsed I/V measurements under appropriate quiescent bias conditions were also used for trapping induced dispersion characterization [47, 95].

### Static I/V Characteristics

The modeling performance of the large-signal model based on static measurements is seen in Fig. 4.14. Here, the comparison between measured and simulated static I/V characteristics is demonstrated. The good agreement between simulation and measurement indicates the ability of the model based on static S-parameters to describe the DC performance of the transistor, and validates the parameter extraction process for the Chalmers  $i_{ds}$  formulation as reviewed in Section 2.3.1.

### Pulsed I/V Characteristics

The large-signal model extracted from pulsed measurements is simulated in transient to reproduce the pulsed I/V characteristics at  $QV_{ds} = 28$  V and  $QV_{gs} = -2.3$  V. By introducing the RC branch parallel to  $i_{ds}$ , the Chalmers model is able to accurately describe the current slump observed in the pulsed I/V characteristics, which is mainly due to the trapping effect. This can be reflected in Fig. 4.15. However,

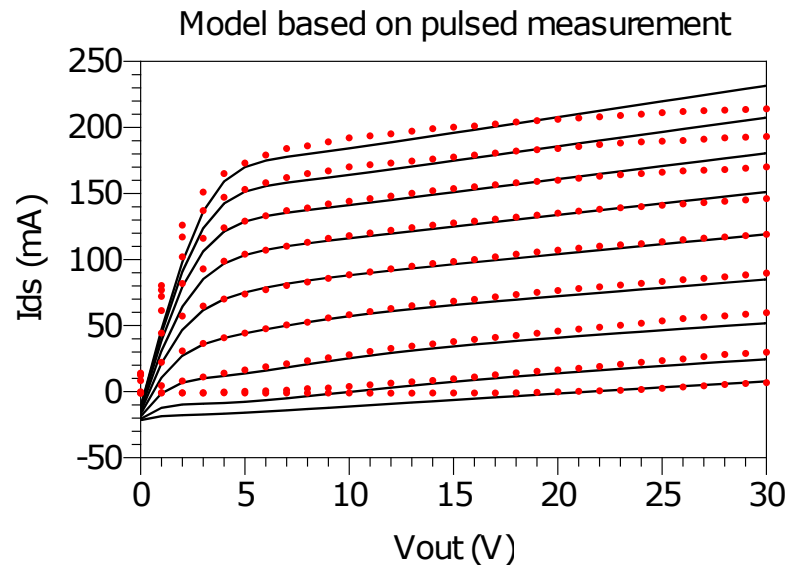


Figure 4.15: Measured (dots) and simulated (lines) pulsed I/V characteristics at  $QV_{ds} = 28$  V and  $QV_{gs} = -2.3$  V.

the current  $i_{ds}$  becomes negative in a part of the simulated I/V network, which is unphysical and inconsistent. The reasons have been already presented in Section 2.4.4. Moreover, the good fit indicates that the drain-current model parameters have been correctly extracted.

### 4.3.2 S-Parameters

#### Static S-Parameters

The static S-parameters were simulated using the model derived from these S-parameters, and the resulting simulation was then compared with measurements. The results are illustrated in Fig. 4.16.

On the one hand, the parameter  $G_{ds}$  has strong influence on the simulation of the output impedance of the large-signal model. As discussed at the end of Section 4.2.1, the parameter  $G_{ds}$  can only be optimized in a limited  $v_{ds}$  range. On the other

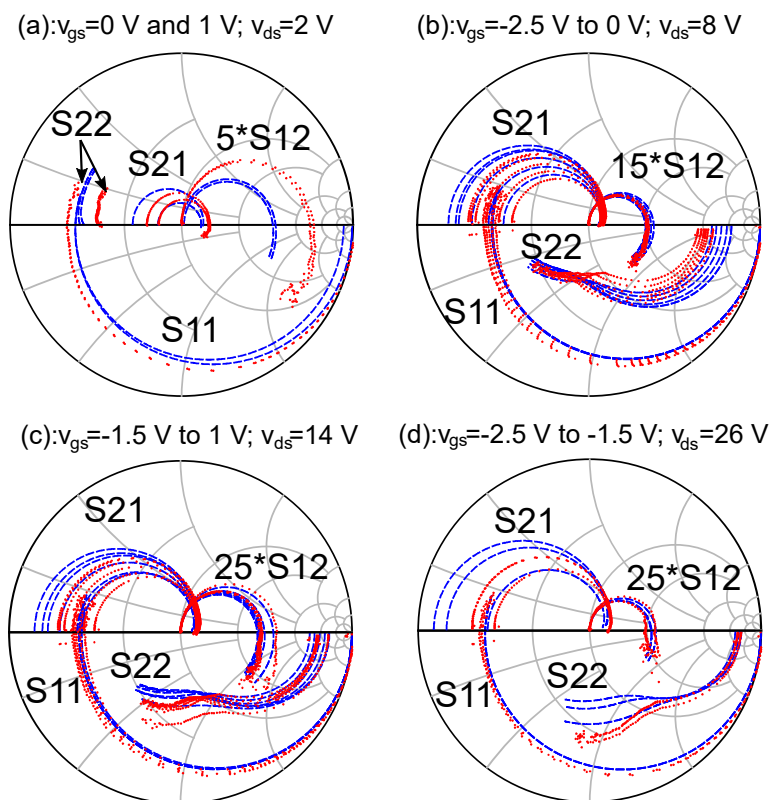


Figure 4.16: Measured (red dots) and simulated (blue dashed lines) static S-parameters from 50 MHz to 50 GHz in the given regions,  $v_{gs}$  is in 0.5 V steps.

hand, the parameters  $C_{gs}$  and  $C_{gd}$  have strong influence on input impedance. Those parameters can be modeled very well by the Chalmers model formulations.

In consequence, simulations of the large-signal model were expected to produce better model agreement with measurements for  $S_{11}$ , related to the simulated input impedance, than for  $S_{22}$ , related to the output impedance. For  $S_{22}$ , a good agreement can only be observed for the bias  $v_{ds} = 14$  and 26 V, where a high accuracy of  $G_{ds}$  prediction can be expected as shown in Fig. 4.12.

For  $S_{21}$ , which is strongly related to the transconductance  $g_m$ , a significant deviation can be observed at all bias points as shown in this figure. This is mainly due to the poor prediction accuracy for  $g_m$  as shown in Fig. 4.11.

### Pulsed S-Parameters

The large-signal model based on the pulsed S-parameters at  $QV_{ds} = 28$  V was verified with the simulations under the same pulse conditions, i.e. with same pulse length and duty cycle. Then, we focus on two regions according to different trap processes of drain-lag effects as already discussed in Section 4.1.3 for small-signal model verification. The comparison results are illustrated in Fig. 4.17.

A good modeling agreement can be observed at both drain voltages. Moreover,

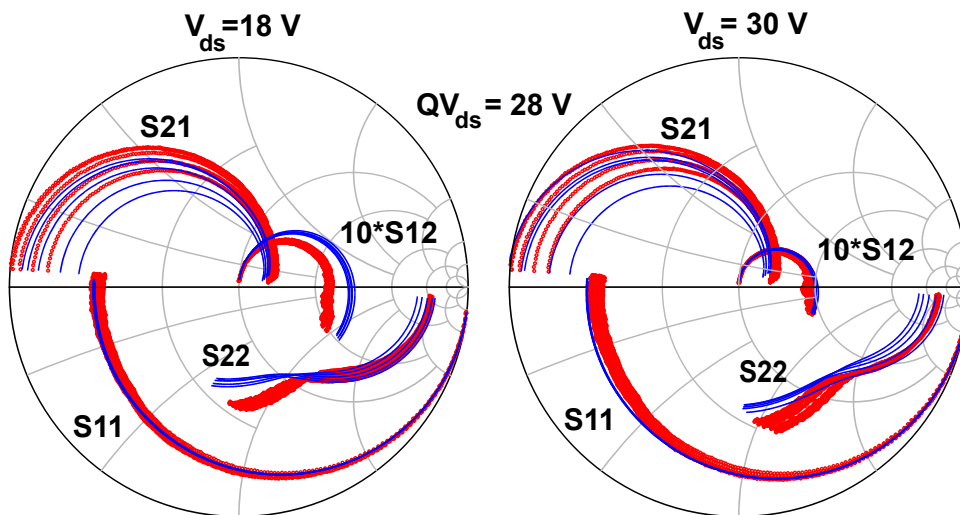


Figure 4.17: Measured (red dots) and simulated (blue lines) pulsed S-parameters from 400 MHz to 40 GHz at  $QV_{ds} = 28$  V in the regions: dynamic  $v_{ds}$  below  $QV_{ds}$  (at left hand side) and dynamic  $v_{ds}$  above  $QV_{ds}$  (at right hand side), for each situation:  $v_{gs} = -2$  V to 0 V in 0.5 V steps.

the accurate modeling performances of  $S_{11}$  at all frequencies and  $S_{22}$  at high frequencies indicate the good agreement of the intrinsic capacitances extracted by means of Chalmers model formulations. The largest disagreements of measured and simulated  $S_{22}$  appear at low frequencies regions, and this indicates the influence of  $v_{gs}$  on  $G_{ds}$  extraction as shown in Fig. 4.12.

It is well known that  $S_{21}$  is basically influenced by the drain current  $i_{ds}$ . Therefore, the good correspondence with the measured results indicates that not only the drain current but also its differential information ( $g_m$ ) has correctly been represented by the Chalmers model.

### 4.3.3 Load-Pull Performance

Load-pull measurements are an experimental technique for direct characterization of large-signal performance of active devices under certain input and output termination impedances. In this techniques, the output and input impedances can be tuned to find an optimal condition that fulfills a particular performance parameter, e.g., maximum output power or maximum power added efficiency (PAE).

In this work, the load-pull measurements were carried out at the fundamental frequency of 8 GHz and at the DUT bias conditions  $V_{ds} = 28$  V;  $V_{gs} = -2.3$  V and  $I_{ds}$  around 30%  $I_{DSS}$ . The source and load impedances used for each measurement were chosen to provide a maximum output power.

Load-pull simulations were then presented and compared with measurements. Fig. 4.18 presents the comparison between measured and modeled gain, power added efficiency (PAE), and mean output current at  $V_{ds} = 28$  V and at a frequency of 8 GHz. In order to ensure that the simulated condition agree with the real situation presented by the measurement setup, the source and load impedances at second harmonic frequency (16 GHz) for 8 GHz were also applied in simulation.

As seen in Fig. 4.18, a good agreement has been achieved for the small-signal gain by using both models. This demonstrates the good performance of prediction of S-parameters and also confirms that the current and charge source were modeled with a good accuracy. In the saturation region, the agreement of the gain modeling by using standard S-parameters is limited. The model always tends to overestimate the gain in this region. These discrepancies can be attributed to the inaccuracy of the model of the current source in the knee region of the static I/V curve (as shown in Fig. 4.14). In this region, the impact of drain-lag effects is more pronounced.



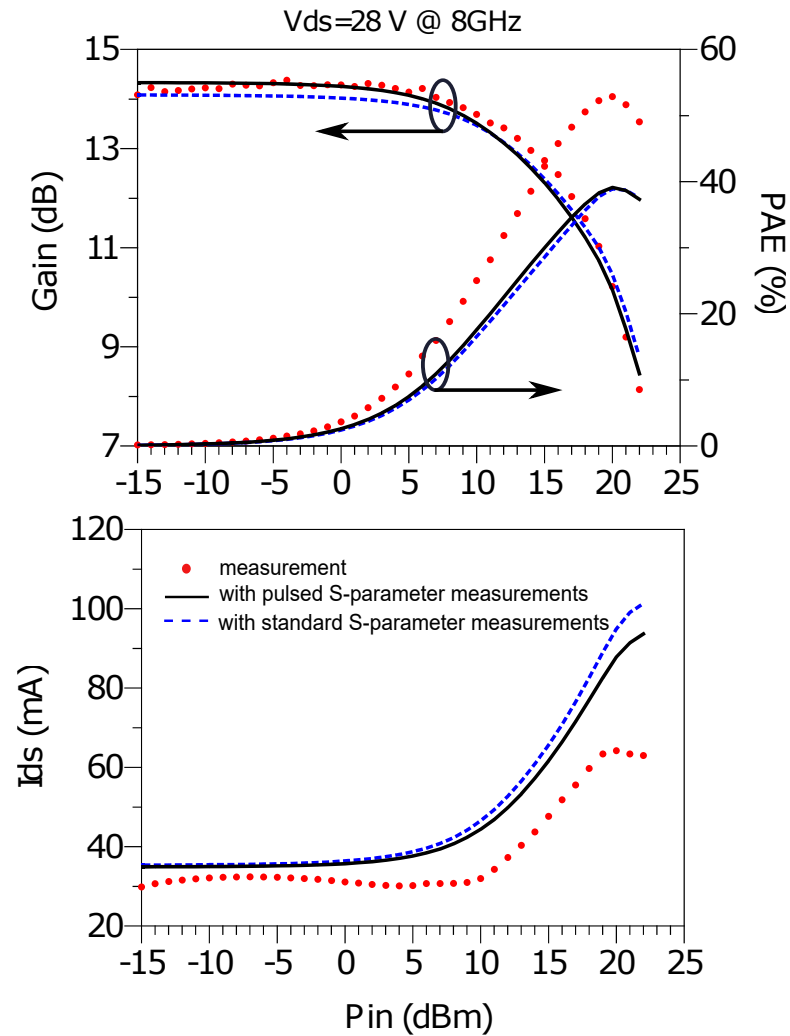


Figure 4.18: Gain, power added efficiency (PAE) and mean dc output current ( $I_{ds}$ ) as a function of input power at frequency of 8 GHz and at bias condition:  $V_{ds} = 28$  V. measurements (red dots) and simulation with model from standard S-parameter measurements (blue dashed lines) and simulation from pulsed S-parameter measurements (black lines)

However, at the same time, the model based on pulsed S-parameters shows a slight improvement in prediction of the gain in the saturation region, which proves that the use of pulsed S-parameters enables an improvement in modeling GaN HEMTs in presence of traps by the Chalmers model that lacks a sophisticated trap description. This can also be validated by the improved modeling results of mean output current in the saturation region.

On the other hand, as another result of poor drain-lag effects modeling, the stan-

standard Chalmers model shows its inability in modeling the PAE, no matter what kind of measurement is used.

## 4.4 Conclusions

In this chapter, the first section addresses the question whether the traps impact the extraction results of the extrinsic parameters and the small-signal capacitances. It is found that the change of the trap state does not influence the resulting values of the extrinsic parameters and the small-signal capacitances.

Next, this chapter addresses the question whether it is possible to model GaN HEMT devices with memory effects by a proven GaN HEMT model, i.e., the Chalmers model, that lacks a sophisticated trap description. It is shown that the Chalmers model is able to yield a good prediction of the transistor performance, if the range of model validity is constrained to a fixed drain voltage and if the model is determined relying on pulsed S-parameters.

At the same time, this chapter also shows the limitation of an approach that relies on the standard Chalmers model. In order to overcome the significant deviation found in predicting the pulsed I/V characteristics and load-pull performance, the trapping effect modeling seems to be indispensable to large signal modeling. In the following chapter, an efficient trap model, which relies on the models based on pulsed S-parameter measurements at different quiescent drain voltages, will be introduced.

# Chapter 5

## Parameter-Scaling Drain-Lag Model

In the last years, a growing interest on modeling trapping effects could clearly be sensed within the microwave community. As a result, various complete trap models [47–52] were published. These models are the most accurate. However, the price to pay is, on one hand, the need for elaborate measurements and the complicated characterization of the trap model, and on the other hand, the use of these models is still not available for circuit designers, since none of the published trap models is yet adopted by commercial circuit simulator vendors.

In this chapter, a simple yet accurate drain-lag model, which aims to circumvent these difficulties while maintaining simulation accuracy, will be presented in detail. The first step of building this model is based on the fact that trap states are controlled by the supply voltages and don't follow the RF signal [96]. This allows to determine a model from pulsed S-parameter measurements that is valid for a single bias point. The improvement of the modeling accuracy has already been proven in the last Chapter. Therefore, different model parameter sets were determined varying the pulse quiescent gate and drain voltage,  $QV_{gs}$  and  $QV_{ds}$ , respectively. This enables us to conclude which  $i_{ds}$  model parameters of the Chalmers model are sensitive to traps. Scaling these model parameters with regard to different trap amplitudes can provide us with a drain-lag model, which is called in this work: parameter-scaling drain-lag model.

The first section will address the extraction of Chalmers (Angelov) model parameters from pulsed S-parameters for different fixed pulse quiescent bias points. Then, it will be shown that only three model parameters need to be adjusted to the trap state, while the rest of the model remains unchanged. The extraction will

be validated through pulsed I/V characteristics, pulsed S-parameters and load-pull measurement.

Next, this chapter presents a drain-lag model, which employs a sub-circuit to take into account the difference between emission and capture time constants.

## 5.1 Large-signal Model Extending

In the last chapter, different Chalmers model parameter sets were extracted with pulsed S-parameters for different fixed pulse quiescent bias points. In this section, it will be shown that only three  $i_{ds}$  model parameters need to be adjusted to the trap state, while the rest of the model remains unchanged. Moreover, it will be shown that these three parameters also show a rather linear dependence on pulse quiescent bias point, which allows for a simple drain-lag model.

### 5.1.1 Extending the Large-signal Model

In the last chapter, only the pulsed S-parameter at  $QV_{ds} = 28$  V was adopted to extract a large-signal model for our DUT. Here, two additional large-signal model parameter sets will be extracted with pulsed S-parameters at  $QV_{ds} = 8$  V and 15 V. According to the extrinsic elements extraction results presented in Table 4.1 and 4.2 and the small-signal intrinsic capacitances extraction results shown in Fig. 4.6, the extracted values of extrinsic elements and capacitance model parameters of large-signal model should be the same for these three large-signal models. Note that the thermal resistance and temperature parameters are assumed not to vary too much within a given technology, and the typical self-heating model was used.

In order to conclude which parameters are sensitive to traps, the three sets of measurements and extracted model parameter sets were compared. As a result, significant variation with  $QV_{ds}$  was observed only for three parameters:  $I_{pk0}$ ,  $\alpha_s$ , and  $\lambda$ .

Starting from the model parameters determined at  $QV_{ds} = 28$  V, model parameters were re-determined for the other pulse quiescent bias points, optimizing only these three parameters and keeping the other parameters constant.

Fig. 5.1 presents the obtained curve-fitting results of I/V curves and transconductance  $g_m$  for several pulse quiescent drain-source voltages. The transconductance

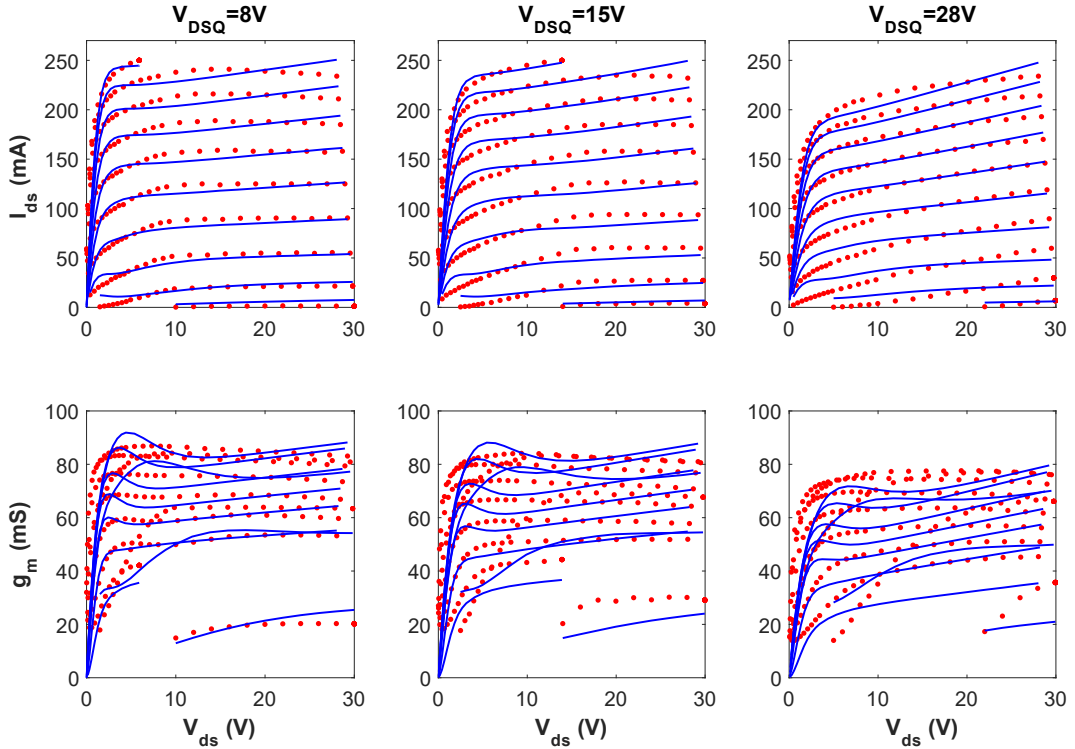


Figure 5.1: Measured (symbols) and modeled (line)  $i_{ds}$  and  $g_m$  of the  $2 \times 125 \mu\text{m}$  GaN HEMT for pulse quiescent gate voltage  $QV_{gs} = -2.3 \text{ V}$ , and pulse quiescent drain voltages  $QV_{ds}$  of  $8 \text{ V}$ ,  $15 \text{ V}$ , and  $28 \text{ V}$ , respectively, described by Chalmers current model.

shown in the figures is taken from the small-signal equivalent circuit rather than from being calculated from the current measurement. The good agreement between simulation and measurement proves that the trap states are indeed frozen for each measurement condition, since the model predicts  $I_{ds}$  and  $g_m$  well even in absence of a trap model. It can also be concluded that the Chalmers model formulas are able to describe  $I_{ds}$  and  $g_m$  reasonably well by using pulsed S-parameters at fixed quiescent bias even though the knee walk-out affects the shape of the I/V curves.

To verify the dependence of the scaled traps-influenced parameters on  $QV_{ds}$ , the model parameter scaling process was further carried out at  $QV_{gs} = -1 \text{ V}$ . Fig. 5.2 and Table 5.1.1 show the extracted values of these trap-influenced parameters against  $QV_{ds}$  for  $QV_{gs} = -2.3 \text{ V}$  and  $-1 \text{ V}$ . It can be concluded that these parameters show a rather linear dependence on the pulse quiescent drain-source voltage which allows for a quite simple mathematical formulation.

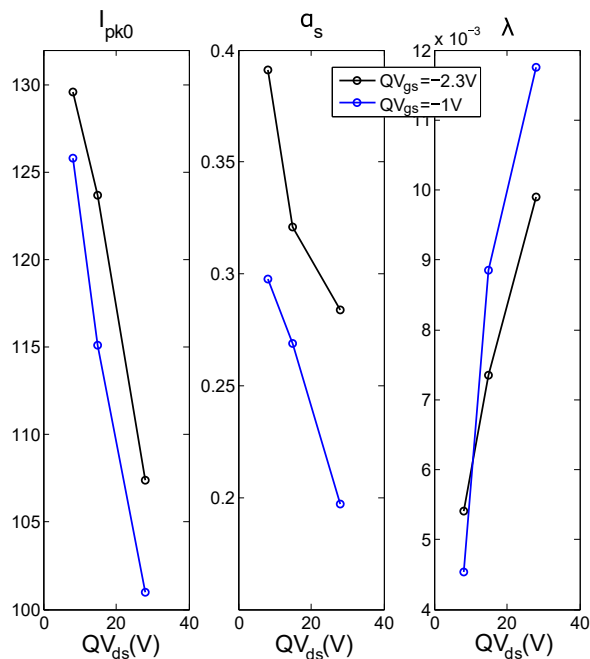


Figure 5.2: Extracted values of the trap-influenced parameters of Chalmers model depending on pulse quiescent drain-source voltage.

Table 5.1: Exact values of the trap-influenced parameters.

Parameter	$V_{GSQ} = -2.3\text{V}$			$V_{GSQ} = -1\text{V}$		
	$(V_{DSQ} =)$			$(V_{DSQ} =)$		
	8	15	28	8	15	28
$I_{pk0}$	129.6	123.7	107.4	125.8	115.1	101
$\alpha_s$	0.391	0.321	0.284	0.2975	0.269	0.197
$\lambda \cdot 10^3$	5.41	7.35	9.9	4.53	8.85	11.75

### 5.1.2 Models with Scaled Parameters Verification

Same as discussed in the last chapter, various simulation with models based on pulsed S-parameters at different quiescent drain-source voltages were carried out, and the simulation results will be compared with measurement data.

#### Pulsed I/V Characteristics

Comparisons of pulsed I/V measurements and simulations with  $QV_{gs} = -2.3\text{V}$  and  $QV_{ds} = 8\text{V}$ ,  $15\text{V}$ , and  $28\text{V}$  are shown in Fig. 5.3. The very good agreement between simulations and measurements in the region when  $v_{ds} < QV_{ds}$  (emission

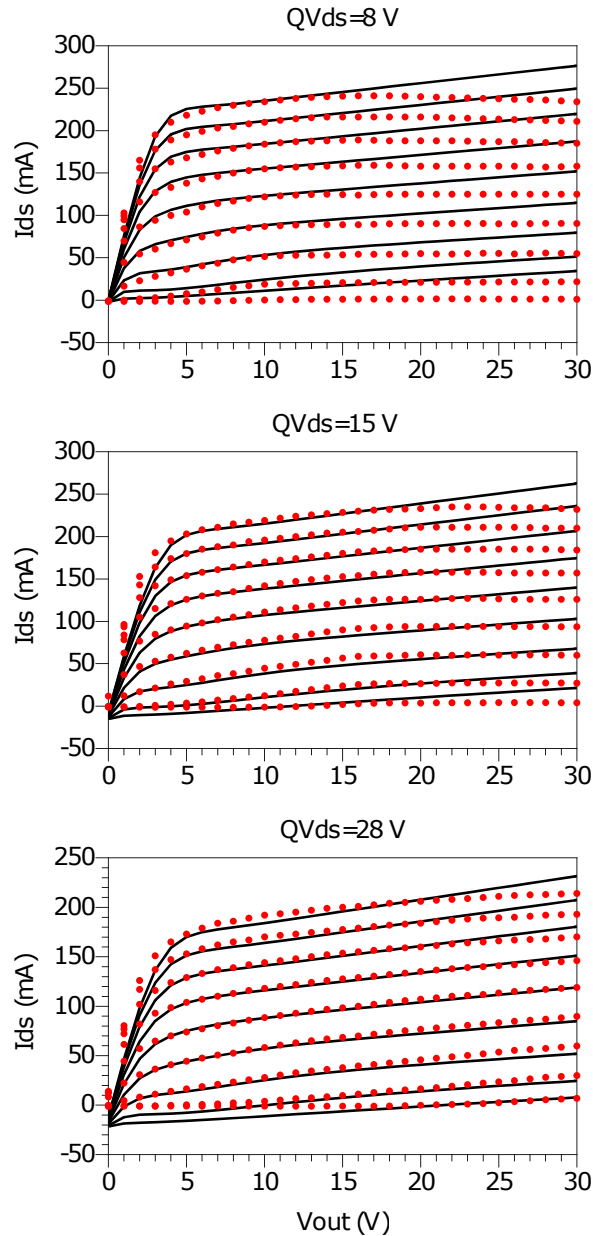


Figure 5.3: Measured (red dots) and simulated (blue lines) pulsed I/V characteristics at  $QV_{gs} = -2.3$  V and  $QV_{ds} = 8$  V, 15 V, and 28 V. For each case:  $v_{gs} = -2$  V to 1.5 V in 0.5 V steps.

process dominants) indicates the ability of the models for describing the current under impact of different trap states, which depend on  $QV_{ds}$  in this region. However, as discussed in Section 2.4.4, the RC branch used in the standard Chalmers model cannot account for the difference between emission and capture process. This is reflected in this figure as the mismatch always occurs when  $v_{ds} > QV_{ds}$ .

### Pulsed S-Parameters

Pulsed S-parameter measurements at  $QV_{gs} = -2.3$  V and  $QV_{ds} = 8$  V, 15 V, and 28 V were presented and compared with the simulations to verify the extracted models with scaled parameter values.

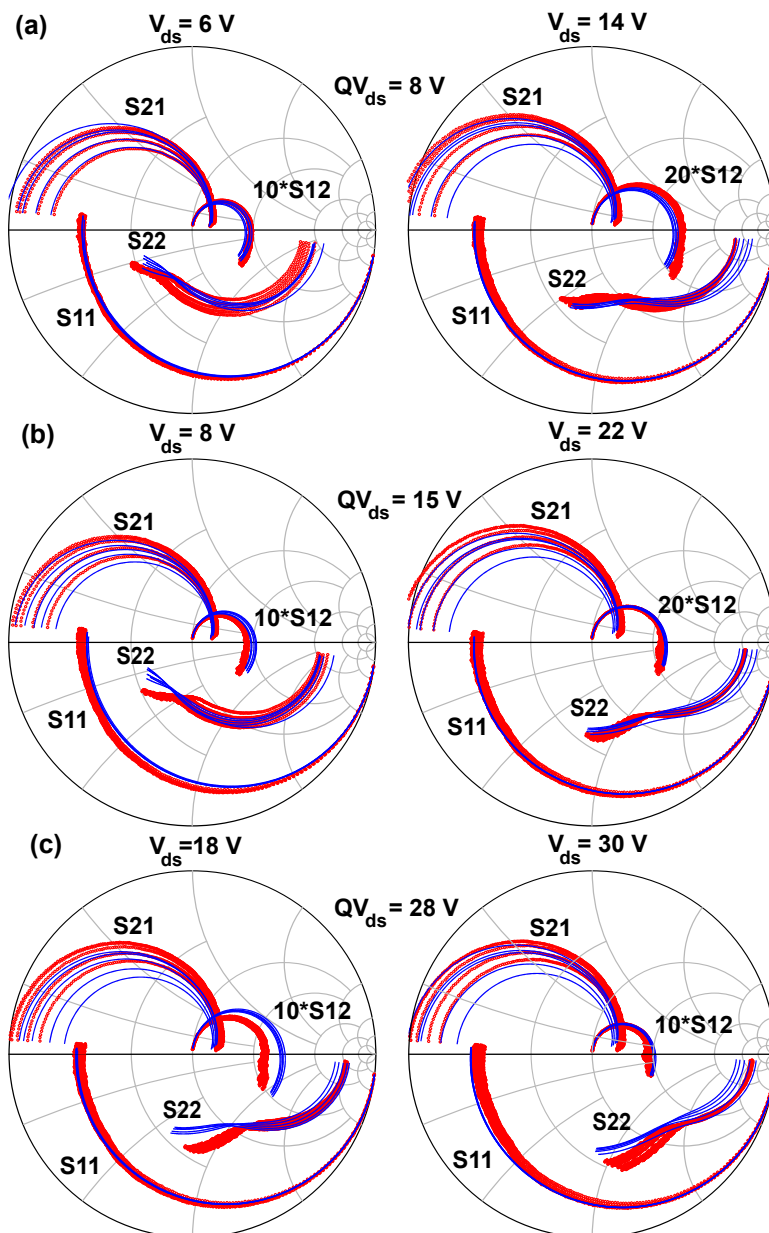


Figure 5.4: Measured (red dots) and simulated (blue lines) pulsed S-parameters from 400 MHz to 40 GHz at  $QV_{gs} = -2.3$  V and  $QV_{ds} = 8$  V, 15 V, and 28 V in the regions:  $v_{ds} < QV_{ds}$  (at left hand side) and  $v_{ds} > QV_{ds}$  (at right hand side), for each situation:  $v_{gs} = -2$  V to 0 V in 0.5 V steps.



Fig. 5.4 shows the comparison results between measured and simulated S-parameters for all of the three models in the frequency range up to 40 GHz at regions: 1)  $v_{ds}$  below  $QV_{ds}$  (at left hand side), and 2)  $v_{ds}$  above  $QV_{ds}$  (at right hand side). It is clearly seen that a good agreement has been achieved for S-parameters except  $S_{22}$  in low-frequency region for each case. As the real part of  $S_{22}$  at the low frequency is strongly related to output conductance  $G_{ds}$ , the mismatch of  $S_{22}$  at low frequencies at different  $v_{gs}$  is mainly due to the mismatch of  $G_{ds}$  for a wide range of  $v_{gs}$  as shown in Fig. 4.12.

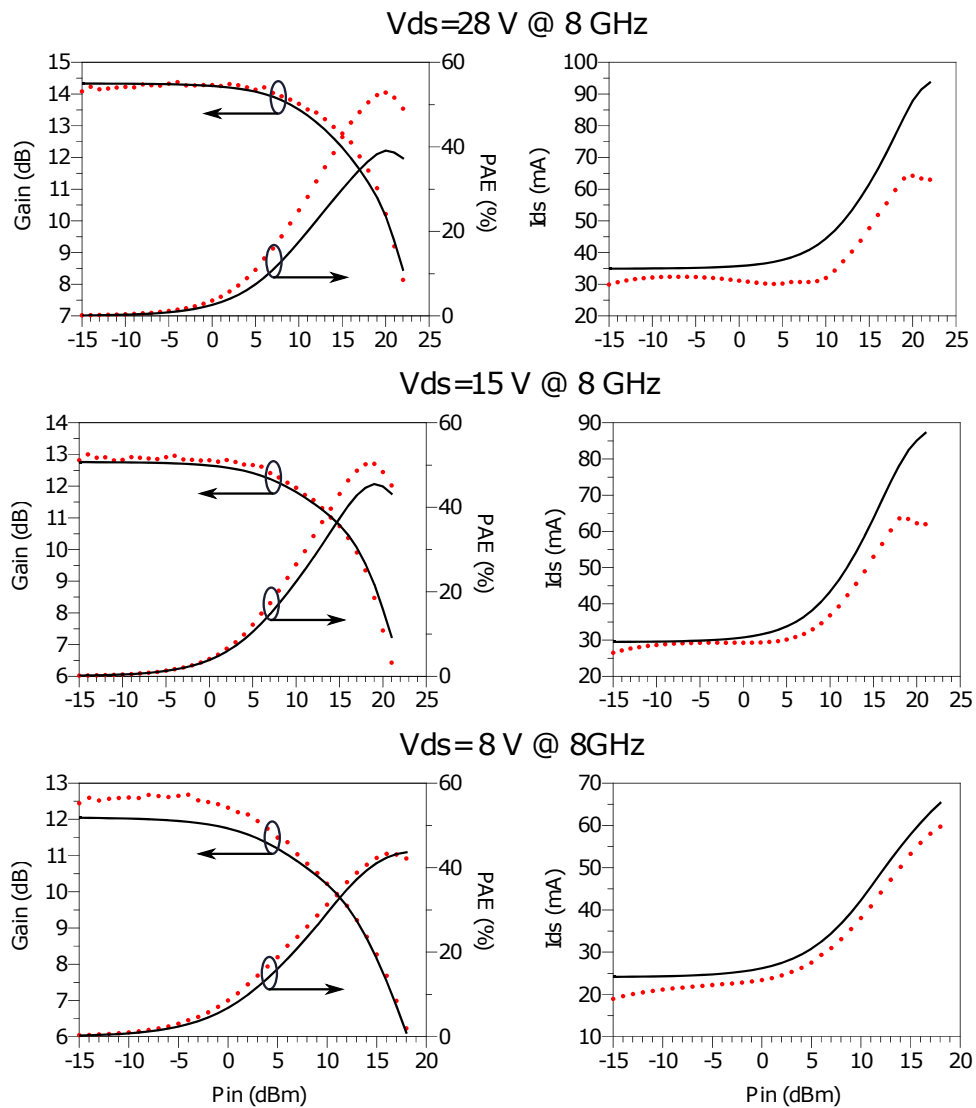


Figure 5.5: Gain, power added efficiency (PAE), and mean output current  $i_{ds}$  as a function of input power ( $P_{in}$ ) at 8 GHz and at  $V_{ds} = 8$  V, 15 V, and 28 V. (Measurements: red dots, simulation: black lines)

## Load Pull Performance

To further verify the models with scaled parameters, load pull measurements at  $V_{ds} = 8$  V, 15 V, and 28 V and at 8 GHz were presented. The source and load impedances were chosen as optimum impedances for providing maximal output power. Furthermore, the impedances at second harmonic were also supplied in the simulation in order to better reproduce the measurement condition.

Fig. 5.5 shows the comparison results between measured and simulated gain, PAE, and mean output current at different bias conditions for  $V_{ds} = 8$  V, 15 V, and 28 V. It is clear that a good agreement has been achieved for small-signal gain, which indicates the models were determined with a certain focus on the model accuracy for power applications at the specific given bias point. However, the disagreement of the PAE and  $I_{ds}$  in saturation region, especially for higher bias condition, can still be clearly observed, which should be ascribed to the absence of an appropriate trap model.

## 5.2 Drain-lag Model based on Scaled Parameters

In the last chapter, it has been shown that the proposed trap model of the standard Chalmers model, i.e., the RC branch parallel to  $i_{ds}$  at the output [56], cannot accurately predict the impact induced by trapping effects. In this section, a novel drain-lag model was described in detail and employed in the Chalmers model instead of the RC branch. It will be shown that the use of this developed drain-lag model overcomes the drawbacks when describing the pulsed I/V characteristics (PIV), i.e., negative  $i_{ds}$  and the poor prediction of the typical kink observed in PIVs. More importantly, this developed drain-lag model significantly improves the modeling accuracy in prediction of the transistor load-pull performance.

### 5.2.1 Model Description

Fig. 5.6 shows the voltage and current transient curves under the impact of drain-lag effects, which normally can be split into two processes: emission and capture process when  $v_{ds}$  is pulsed down or up, respectively.

However, in this work, the whole process of drain-lag is split into the following two processes: lagged-state and steady-state process as highlighted in Fig. 5.6 [49].

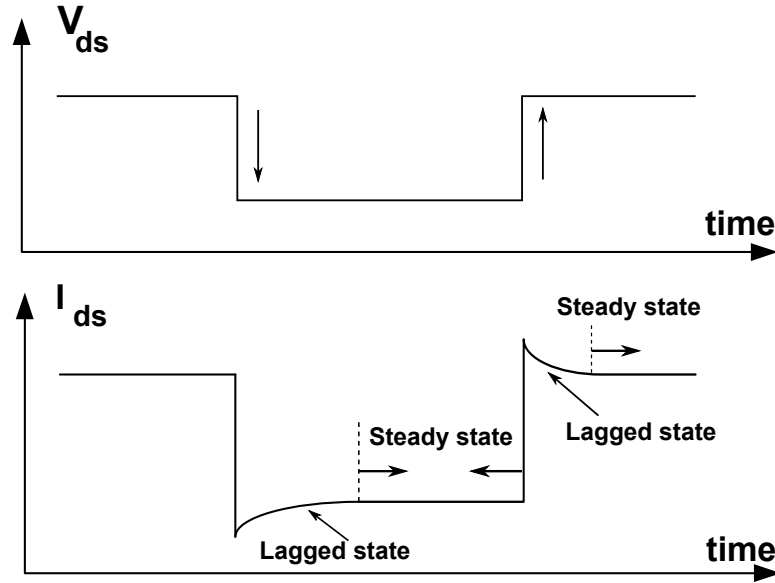


Figure 5.6: output voltage  $v_{ds}$  and output current  $i_{ds}$  as a function of time. Steady-state and lagged-state process are highlighted.

The lagged-state process begins when  $v_{ds}$  is pulsed up or down and finishes at the moment  $i_{ds}$  reaches its stable value, while the steady-state process lasts as long as  $i_{ds}$  stays stable.

In the last section, it has been shown that only three parameters have to be adjusted if the quiescent drain voltage varies:  $I_{pk0}$ ,  $\alpha_s$  and  $\lambda$ . The other parameters can be kept unchanged without a significant loss of accuracy. Moreover, these three parameters show a rather linear dependence on the pulse quiescent drain-source voltage. Using this dependence enables a good prediction of the drain source currents in steady-state process, where the steady traps in this process are controlled by the steady input voltage  $v_{gs}$  and output voltage  $v_{ds}$ . Now, these three trap-dependent parameters can be formulated as:

$$I_{pk0}(v_{ds}) = I_{pk0,cons} \cdot (1 + Tr_{Ipk0} \cdot v_{ds}) \quad (5.1)$$

$$\alpha_s(v_{ds}) = \alpha_{s,cons} \cdot (1 + Tr_{alphas} \cdot v_{ds}) \quad (5.2)$$

$$\lambda(v_{ds}) = \lambda_{cons} \cdot (1 + Tr_{lambda} \cdot v_{ds}) \quad (5.3)$$

where  $Tr_{Ipk0}$ ,  $Tr_{alphas}$ , and  $Tr_{lambda}$  are new fitting parameters to adjust the drain-source currents to different trap states.

However, when  $v_{ds}$  is pulsed up or down, the instantaneous output current  $i_{ds}$

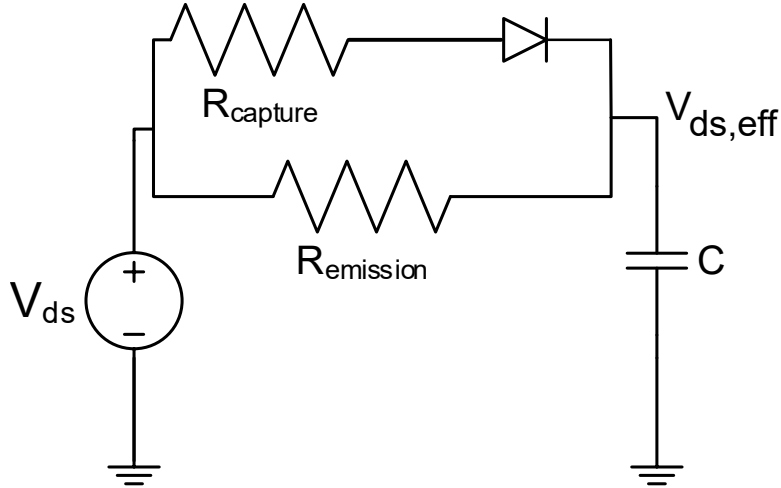


Figure 5.7: Schematic of drain-lag model.

does not follow the fast  $v_{ds}$  variation but exhibits a slow current transient through the whole lagged-state process.

In order to take this into account a sub-circuit shown in Fig. 5.7 was employed, which is the left part of the sub-circuit shown in Fig. 2.28 and is considered to account for the different time constants of the emission and capture process.

Fig. 5.8 shows the behavior of the input voltage  $v_{ds}$  and the output voltage  $v_{ds,eff}$  of this drain-lag sub-circuit, together with the simulated output current  $i_{ds}$ . When  $v_{ds}$  is pulsed from a higher voltage to a lower one, the instantaneous  $i_{ds}$  value first does not change and preserves the trap state related to the previous value of  $v_{ds}$ . After a long time interval determined by the detrapping process,  $i_{ds}$  gradually reaches a value depending on the trap state of the new value of  $v_{ds}$ . On the other hand, when  $v_{ds}$  is pulsed to a higher value, the response is much faster, which can be explained by a shorter time constant of the respective trapping process. With this in mind, the output voltage  $v_{ds,eff}$  of the sub-circuit offers a nice solution to describe the changes in the trap states. As a result, the three voltage-dependent parameters can be defined as:

$$I_{pk0}(v_{ds,eff}) = I_{pk0,cons} \cdot (1 + Tr_{Ipk0} \cdot v_{ds,eff}) \quad (5.4)$$

$$\alpha_s(v_{ds,eff}) = \alpha_{s,cons} \cdot (1 + Tr_{alphas} \cdot v_{ds,eff}) \quad (5.5)$$

$$\lambda(v_{ds,eff}) = \lambda_{cons} \cdot (1 + Tr_{lambda} \cdot v_{ds,eff}) \quad (5.6)$$

and the time constants for these two processes are defined as:

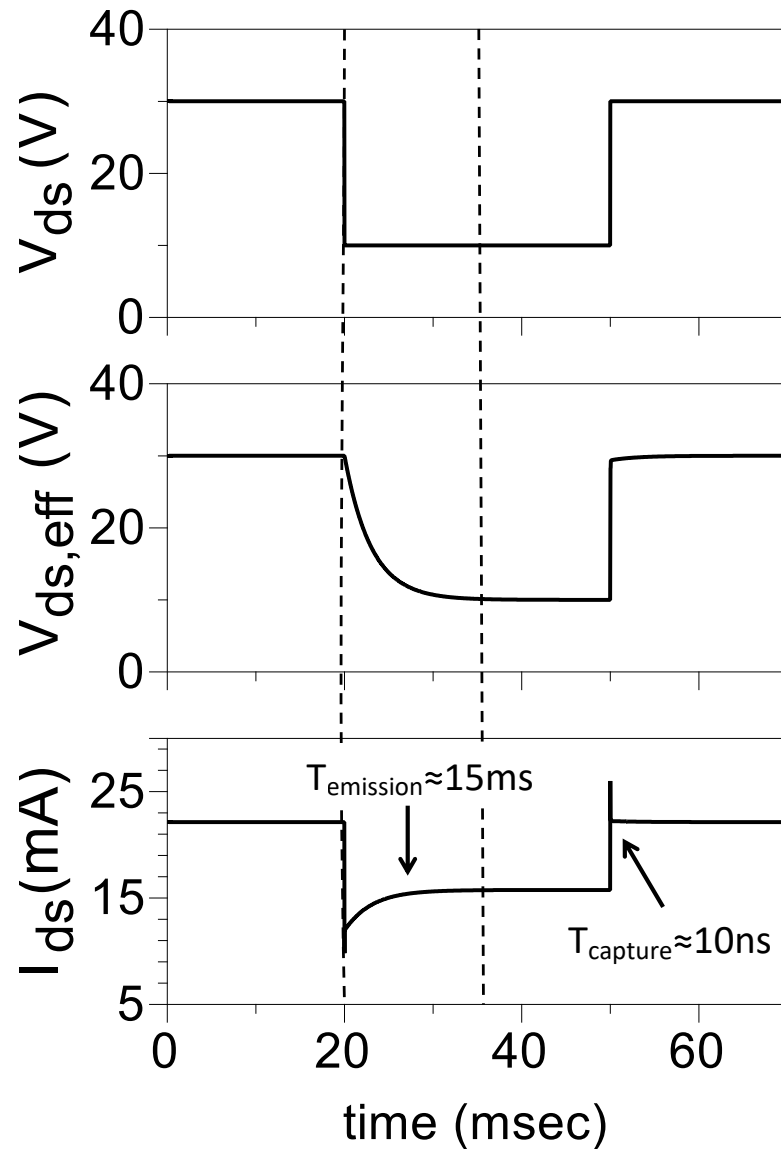


Figure 5.8: Input and output voltage of the drain-lag subcircuit as a function of time and simulated output current, for a drain pulse between 30 V and 10 V.

$$T_{\text{capture}} = R_{\text{capture}} \cdot C \quad (5.7)$$

$$T_{\text{emission}} = R_{\text{emission}} \cdot C \quad (5.8)$$

where  $R_{\text{capture}} \ll R_{\text{emission}}$ .

## 5.2.2 Model Parameter Extraction

Now, an overview of the extraction of the drain-lag model parameters will be given. The trapping time constants, i.e.,  $\tau_{emission}$  and  $\tau_{capture}$ , should be determined by means of measuring the current transients during drain-source voltage pulses. The extraction process and results have been already addressed in detail in [48]. According to these results one does not need to determine the trapping time constants exactly, as long as the emission time constant is much longer than the capture time constant as discussed in [48]. Thus, the emission time constant is set here as  $\tau_{emission} = R_{emission}C = 1 \mu s$ , while the capture time constant is set as  $\tau_{capture} = R_{capture}C = 1 ps$ . Therefore, the number of drain-lag model parameters added to the standard Chalmers model without constant RC branch can be reduced to 3, namely  $Tr_{ipk0}$ ,  $Tr_{alphas}$ , and  $Tr_{lambda}$ .

These parameters are extracted from pulsed S-parameter measurements at different quiescent drain voltages  $QV_{ds} = 8 V, 15 V, \text{ and } 28 V$  and a constant  $QV_{gs} = -2.3 V$ . For each measurement condition, a standard Chalmers model was made by fitting (1) the drain-source current model against the measured drain-source current along the pulsed S-parameter measurement and (2) the transconductance  $g_m$  extracted from the pulsed S-parameter measurements. Only three parameters have to be adjusted if the quiescent drain-source voltage varies:  $I_{pk0}$ ,  $\alpha_s$ , and  $\lambda$  which are proven sensitive to traps. Our investigations revealed that these parameters show a rather linear dependence on the quiescent drain voltage, as plotted in Fig. 5.6. Then the parameters  $Tr_{ipk0}$ ,  $Tr_{alphas}$ , and  $Tr_{lambda}$  can be simply extracted from the slope of the changes of parameters  $I_{pk0}$ ,  $\alpha_s$ , and  $\lambda$  versus  $QV_{ds}$ . The resulting values for these drain-lag model parameters are given in Table 5.2.

Table 5.2: Extracted values of drain-lag model parameters

$Tr_{ipk0}$	$Tr_{alphas}$	$Tr_{lambda}$
-0.008089	-0.01206	0.05817

## 5.2.3 Model Verification

After modeling the drain-lag effects with these scaled parameters, a Verilog-A design kit was developed based on this augmented Chalmers model. To verify the

parameter-scaling drain-lag model, various simulations including pulsed I/V, pulsed S-parameters, load pull performance (under different bias conditions), and low frequency large-signal behavior, are presented and compared with measurement data.

### Pulsed I/V Characteristics

The I/V characteristics of GaN HEMT are always important in both modeling process and during model verification. They indicate the major nonlinearity and show the impact of the dispersion effects. In this work, the output currents were also measured under pulsed conditions together with the pulsed S-parameter measurements. This allows for preventing self-heating and focusing on the dispersion effects.

The pulse repetition rate and pulse width employed in the simulations correspond to the values used in the measurements, i.e., 250 ns and 250  $\mu$ s, respectively, giving a duty cycle of 0.1%.

Fig. 5.9 shows a comparison between measured and simulated pulsed I/V characteristics for quiescent voltages  $QV_{GS} = -2.3$  V and  $QV_{DS} = 8$  V, 15 V, and 28 V.

As seen in this figure, the typical kink can be observed around the quiescent bias point in pulsed I/V characteristics, and it is mainly due to the asymmetry in time constants associated with capture and release of charge in the traps: A normal narrow-width, low-duty-cycle pulsed characterization is sufficient in order to keep both the thermal and trapping state fixed. In particular, owing to the fast (i.e. faster than release) capturing time constants, the trapping state seems to be dependent on the peak values of the instantaneous voltages  $v_{gs}$  and  $v_{ds}$ .

Although the use of the parameter-scaling drain-lag model enables an overall fit despite the high span of drain bias, especially around the quiescent bias and ensures a significant improvement in prediction of the typical kink in the I/V curves and the knee walk-out effect, the deviation between measurements and simulations are still particularly obvious.

### Pulsed S-Parameters

To further verify the parameter-scaling drain-lag model, pulsed S-parameter simulations at different quiescent drain voltages were carried out and compared with the measurements.

Fig. 5.10 shows the measured pulsed S-parameters and the simulation results by using the parameter-scaling drain-lag model at different quiescent drain voltages for

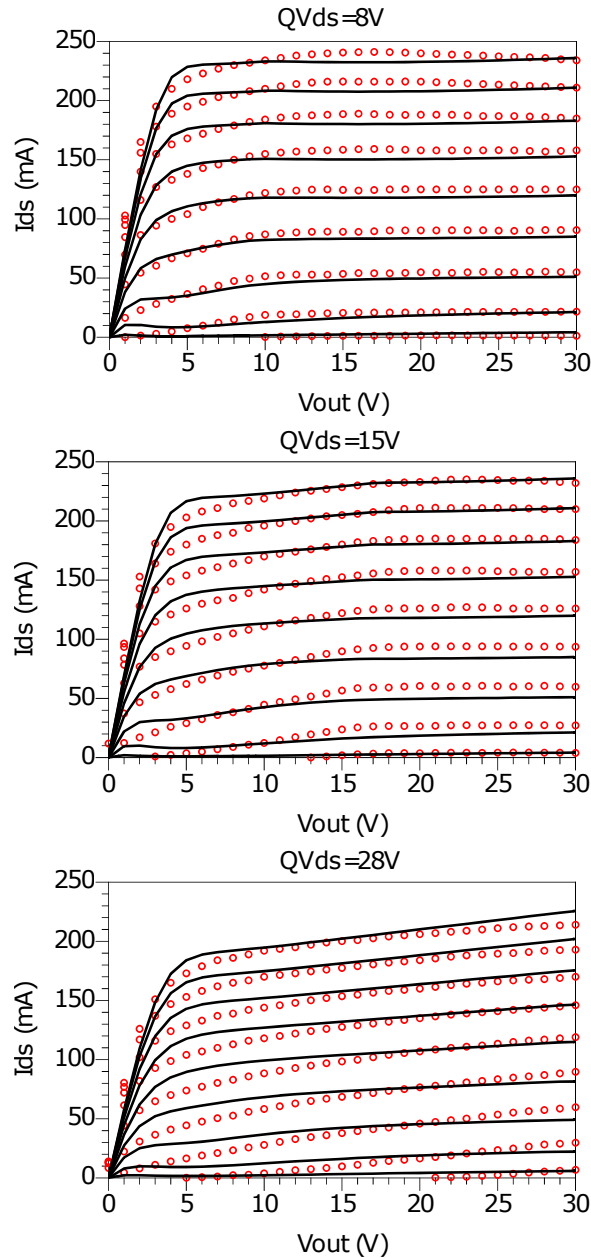


Figure 5.9: Pulsed I/V measurements for  $v_{gs}$  from -3 to 1.5 V in 0.5 V steps at  $QV_{gs} = -2.3$  V and  $QV_{ds} = 8$  V, 15 V, and 28 V, pulse length is 250 ns (symbols), pulsed simulations with the same conditions (lines)

bias conditions  $v_{gs} = -2$  V and  $v_{ds}$  below and above  $QV_{DS}$ . The accurate modeling performances of  $S_{11}$  and  $S_{12}$  for each quiescent condition testify the good agreement of intrinsic capacitances  $C_{gs}$  and  $C_{gd}$ , which were extracted on the basis of the S-parameter measurements and illustrated in Fig 4.13. Moreover, it is well known that



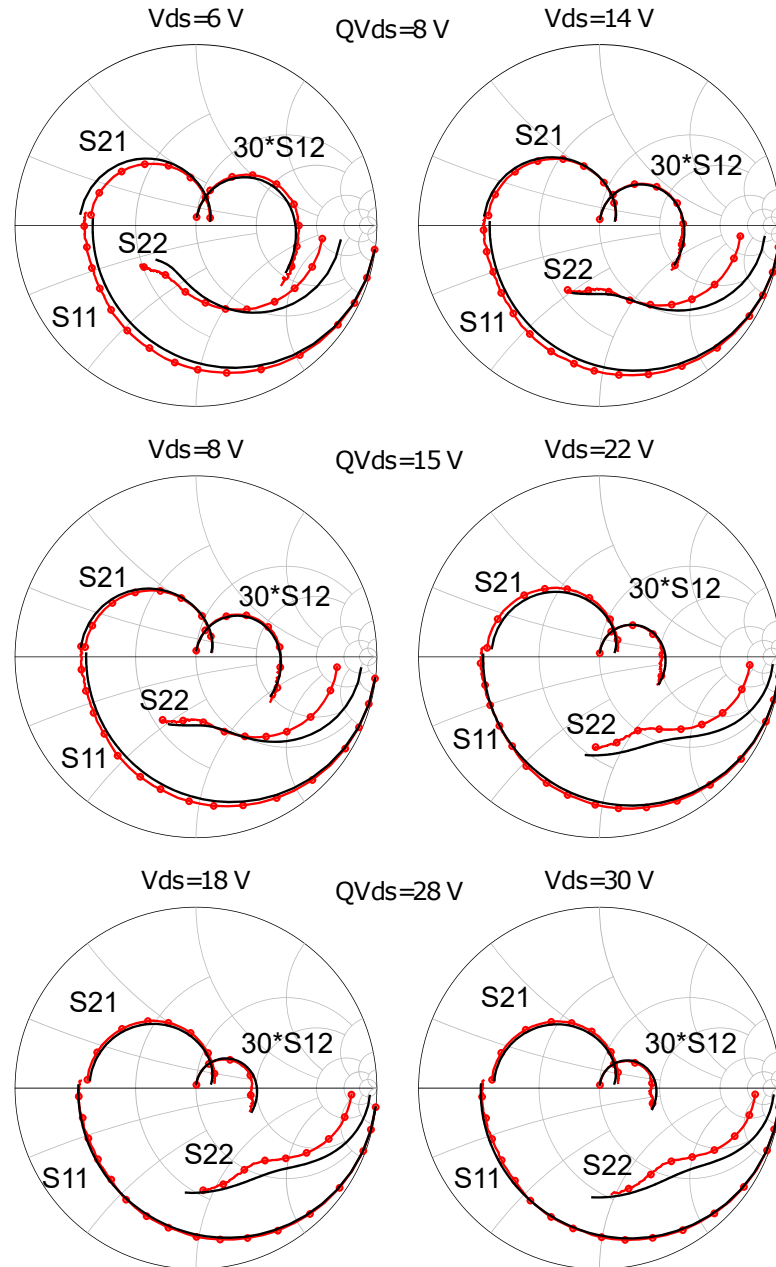


Figure 5.10: Measured (red marked lines) and simulated (black lines) pulsed S-parameters at  $QV_{GS} = -2.3$  V and  $QV_{DS} = 8$  V, 15 V, and 28 V for dynamic bias condition:  $v_{gs} = -2$  V,  $v_{ds}$  below  $QV_{DS}$  (at left hand side) and above  $QV_{DS}$  (at right hand side).

$S_{21}$  is basically influenced by the drain current. Its parameters were extracted on the basis of pulsed I/V measurements and thus are less connected to S-parameter measurements. Therefore, in consequence, simulations of the large-signal models with

the parameter-scaling drain-lag models were expected to provide closer agreements with the measurements for  $S_{11}$  and  $S_{12}$ , which are strongly related to the intrinsic capacitances, than for  $S_{21}$ , related to the simulated transconductance. These expectations correspond to the results illustrated in Fig. 5.10 with comparatively better agreements of simulations for  $S_{11}$  and  $S_{12}$  than for  $S_{21}$ .

On the other hand, the deviation between measured and simulated  $S_{22}$  is particularly obvious. This is due to the absence of RC branch, which can provide a correct term  $\Delta G_{ds} = 1/R$ . The detailed reasons and solutions will be discussed in next section and chapter, respectively.

### Load-Pull Performance

In addition, load-pull measurements with different bias conditions are conducted to further verify the large-signal performances of the Chalmers model with the parameter-scaling drain-lag model.

A comparison between measured and simulated (with RC sub-circuit and with the parameter-scaling drain-lag model) gain, PAE, and mean output current is given at Fig. 5.11, and demonstrates the improvement brought by the new drain-lag model. As seen in this figure, the impact of the trapping effects, in our case mainly the drain-lag effect, can be especially observed at the PAE and mean output current. The standard Chalmers model using RC sub-circuit at output fails to predict this impact, while the parameter-scaling drain-lag model dramatically improves the modeling accuracy in prediction of the decrease of mean output current caused by drain-lag effect.

However, as the Chalmers model with the parameter-scaling drain-lag model suffers from a mismatch in  $S_{22}$ , the agreement of measured and simulated small-signal gain is very limited. The mean  $i_{ds}$  first decreases with increase of the input power as can be illustrated from the  $i_{ds}$  curves at  $V_{ds} = 15$  V and 28 V, and this is a significant consequence of the asymmetric nature of the traps capture and emission processes and cannot be attributed to the thermal effects, which is less modeled by using the parameter-scaling drain-lag model.

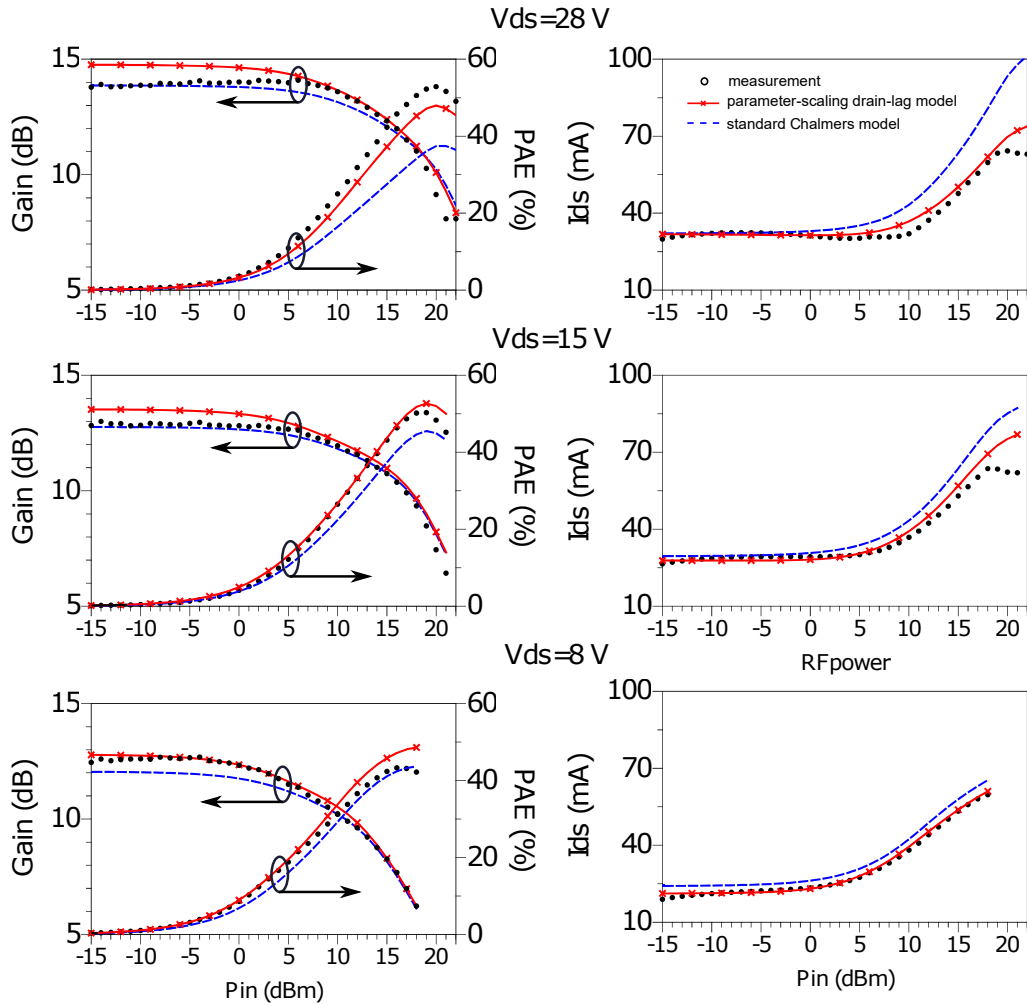


Figure 5.11: Measured (dots) and simulated (lines) gain, PAE, and mean  $I_{ds}$  as a function of input power  $P_{in}$  at 8 GHz for  $v_{ds} = 8$  V, 15 V, and 28V, (black dots: measurements, red marked lines: simulation with the parameter-scaling drain-lag model, blue dashed lines: simulation with standard Chalmers model extracted from pulsed S-parameter measurements at  $QV_{ds} = 8$  V, 15 V, and 28 V, respectively).

### 5.3 Discussion of Model Limitations

In this chapter, a drain-lag model is presented, which is proven to predict device performance well for various trap states. However, the drawbacks of this drain-lag model is particularly obvious:

- The modeling accuracy of Knee-walkout effect is very limited.
- It is of little use in describing the typical kink around the quiescent drain

voltage from pulsed I/V curves.

- It shows its inability in prediction of  $S_{22}$ .

The latter is mainly due to the mismatch of the RF output conductance  $G_{ds,RF}$ . Output conductance  $G_{ds}$  represents the partial derivative of the drain current with respect to the drain voltage. In the standard Chalmers model, a correction term  $\Delta G_{ds}$  to the DC output conductance  $G_{ds,DC}$ , which is given by the model parameters of the main current source found in Equation (2.22), is supplied by an RC branch parallel to  $C_{ds}$ .

For the drain-lag model described in this chapter, the correction term  $\Delta G_{ds}$  is related to the partial derivative of three trap state dependent parameters,  $I_{pk0}$ ,  $\alpha_s$ , and  $\lambda$ , with respect to drain voltage  $v_{ds}$ , e.g., in case of  $I_{pk0}$ :

$$\frac{\partial I_{pk0}(v_{ds,eff})}{\partial v_{ds}} = I_{pk0,cons} \cdot Tr_{I_{pk0}} \cdot \frac{\partial v_{ds,eff}}{\partial v_{ds}} \quad (5.9)$$

where  $v_{ds,eff}$  is a time-relevant parameter and can be expressed as:

$$v_{ds,eff} = \begin{cases} v_{ds}(t_0) - \Delta v_{ds} \cdot (1 - e^{\frac{-t}{\tau_{emission}}}) & \text{if } \Delta v_{ds} < 0 \\ v_{ds}(t_0) - \Delta v_{ds} \cdot (1 - e^{\frac{-t}{\tau_{capture}}}) & \text{if } \Delta v_{ds} > 0 \end{cases} \quad (5.10)$$

In this equation,  $v_{ds}(t_0)$  and  $\Delta v_{ds}$  represent the value of  $v_{ds}$  before  $v_{ds}$  variation and the instantaneous change of  $v_{ds}$ , respectively. Actually, for pulsed measurements, the value of  $v_{ds}(t_0)$  equals the quiescent drain voltage  $QV_{ds}$ , and the value of the time  $t$  equals the used pulse length  $t_{pulse}$ , in this work,  $t_{pulse} = 250ns \ll \tau_{emission}$ . Thus, we have:

$$e^{\frac{-t}{\tau_{emission}}} \approx 1 \quad \Rightarrow \quad v_{ds,eff} \approx QV_{ds} (const.) \quad \text{if } \Delta v_{ds} < 0 \quad (5.11)$$

As a consequence,  $\Delta G_{ds}$  now can be given by:

$$\frac{\partial v_{ds,eff}}{\partial v_{ds}} \approx 0 \quad \Rightarrow \quad \Delta G_{ds} \approx 0 \quad (5.12)$$

Therefore, we can assume that  $G_{ds}$  or  $G_{ds}$ -related parameters, e.g.,  $S_{22}$ , extracted from Chalmers model with the parameter-scaling drain-lag model and Chalmers model without RC branch should be very close. Fig. 5.12 supports our suggestion.

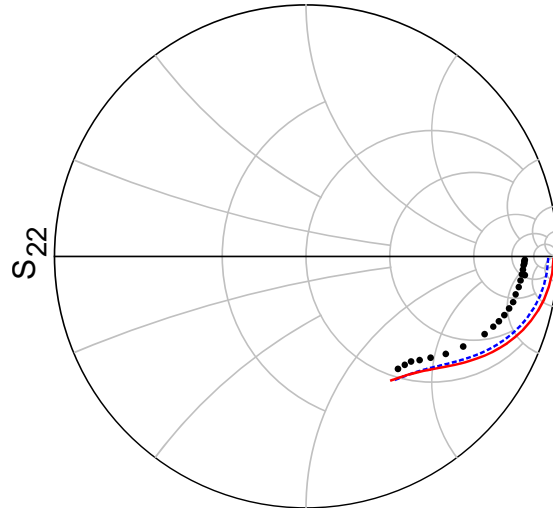


Figure 5.12: Comparison between measured (black dots) and modeled (lines) pulsed S-parameter  $S_{22}$  biased at  $v_{gs} = -2$  V and  $v_{ds} = 14$  V at a quiescent bias point of  $QV_{gs} = -2.3$  V and  $QV_{ds} = 28$  V up to 20 GHz using the Chalmers model (a) without RC branch (red solid line) (b) with the parameter-scaling drain-lag model (blue dashed line).

## 5.4 Conclusions

This chapter addresses a novel drain-lag model to including the trapping effects in the Chalmers model for the large-signal description of GaN HEMTs. Only three model parameters are required to scale with trap state, which allows for an easy interpretation of the impact of trapping on transistor performance. The model shows good accuracy in load-pull simulation over a wide range of drain bias voltages. As an additional benefit, the scaled model parameters can be used to approximately simulate the transistor relying even on a model that lacks a dedicated trap description



# Chapter 6

## Combined Drain-Lag Model

The limitation of this parameter-scaling drain-lag model will also be addressed in this chapter. To overcome this drawback of the parameter-scaling drain-lag model, the Quéré drain-lag model was integrated. A brief review of the Quéré drain-lag model has already been presented in Section 2.4.4. It is shown that this drain-lag model employs a pseudo gate-source voltage at the input of the current source. The pseudo gate-source voltage is related to a fitting parameter  $k$ , which is linked to the amplitude of traps and is assumed to be linearly dependent on the output current [44]. In this chapter, it is shown that instead of the complicated bias dependence of the parameter  $k$  as presented in Quéré drain-lag model, a constant value should bring the same modeling performance, if combined with the parameter-scaling drain-lag model. This can significantly simplify the model parameters extraction process.

Finally, the proposed drain-lag model in this chapter is verified by comparing measured and simulated pulsed I/V characteristics, pulsed S-parameters, load-pull performance under different bias conditions and different load impedances, and low-frequency large-signal behavior.

### 6.1 Model Development

In this section, a streamlined drain-lag model based on the Chalmers model, extracted by means of pulsed S-parameter measurements, is presented. First, the topology of the modified Chalmers model is illustrated. Next, it will be shown that the new model is able to provide a correction term  $\Delta G_{ds}$  in order to take into account the impacts of drain-lag effects.

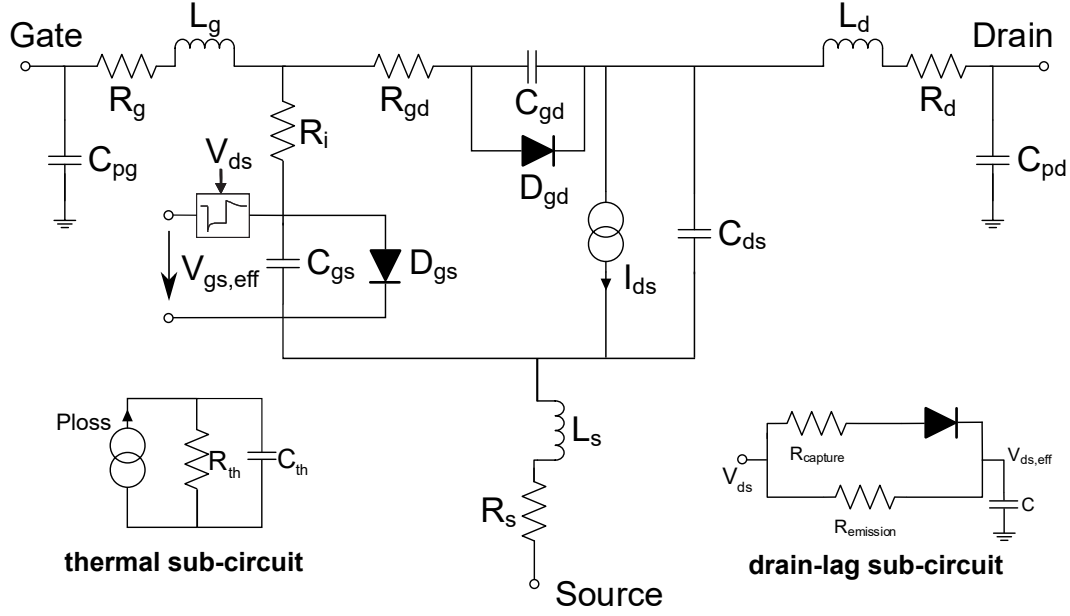


Figure 6.1: Large-signal model topology for GaN HEMT with thermal and trapping sub-circuits.

### 6.1.1 Developed Large-Signal Model Topology

The intrinsic topology of the modified large-signal model for the investigated GaN HEMT is shown in Fig. 6.1. As mentioned previously, this modified large-signal model does not only employ the parameter-scaling drain-lag model, but also adopts the Quéré drain-lag model, which employs a pseudo gate-source voltage at the input of the current source as illustrated in this figure. The detailed drain-lag sub-circuit for the Quéré drain-lag model has been described in Section 2.4.4 and is again shown in Fig. 6.2.

As seen in the figure, there are two input voltages:  $v_{gs}$  and  $v_{ds}$ , and two output voltages, named  $v_{ds,eff}$  and  $v_{gs,eff}$ .  $v_{ds,eff}$  is the output voltage of the “2-path RC circuit”, which takes into account the difference between the capture and emission time constants. Hence, we have:

$$v_{ds,eff} = \begin{cases} v_{ds}(t_0) - \Delta v_{ds} \cdot (1 - e^{-\frac{t}{\tau_{emission}}}) & \text{if } \Delta v_{ds} < 0 \\ v_{ds}(t_0) - \Delta v_{ds} \cdot (1 - e^{-\frac{t}{\tau_{capture}}}) & \text{if } \Delta v_{ds} > 0 \end{cases} \quad (6.1)$$

where  $\tau_{emission} = R_{em} \cdot C$  and  $\tau_{capture} = R_{cap} \cdot C$  are the time constants for emission and capture process, respectively.  $v_{ds}(t_0)$  and  $\Delta v_{ds}$  represent the values of  $v_{ds}$  before



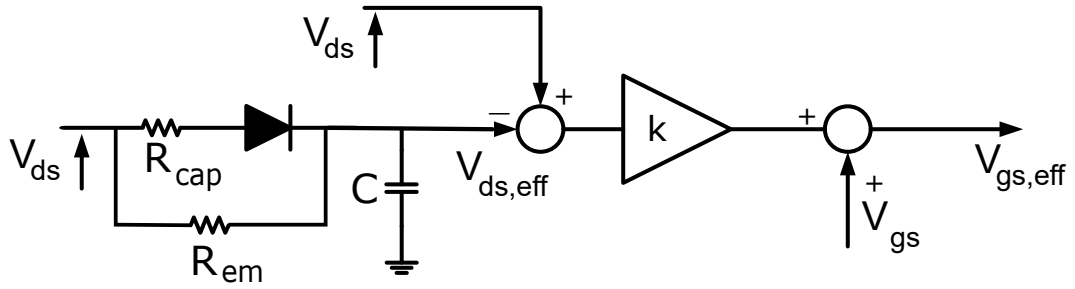


Figure 6.2: The equivalent circuit of drain-lag model with two input voltages:  $v_{gs}$  and  $v_{ds}$ , and two output voltages  $v_{ds,eff}$  and  $v_{gs,eff}$  [44, 48, 81].

$v_{ds}$  variation and the instantaneous change of  $v_{ds}$ , respectively. Actually, for pulsed measurements, the values of the variables  $v_{ds}(t_0)$  and  $\Delta v_{ds}$  in equation (5.10) equal  $QV_{ds}$  and  $QV_{ds} - v_{ds}$ , respectively, and the value of the time  $t$  equals the used pulse length  $t_{pulse}$ , in our case,  $\tau_{capture} \ll t_{pulse} = 250 \text{ ns} \ll \tau_{emission}$ . So we have:

$$e^{\frac{-t_{pulse}}{\tau_{emission}}} \approx 1 \quad \text{and} \quad e^{\frac{-t_{pulse}}{\tau_{capture}}} \approx 0 \quad (6.2)$$

Thus, Equation (6.1) can be rewritten in the following form:

$$v_{ds,eff} \approx \begin{cases} QV_{ds} (const.) & \text{if } \Delta v_{ds} < 0 \\ v_{ds} & \text{if } \Delta v_{ds} > 0 \end{cases} \quad (6.3)$$

Another output voltage  $v_{gs,eff}$  is employed in the model as a pseudo intrinsic gate voltage, which modifies the current source command voltage  $v_{gs}$  to account for the trap contribution and can be formulated as:

$$v_{gs,eff} = k \cdot (v_{ds} - v_{ds,eff}) + v_{gs} \quad (6.4)$$

where  $k$  is a fitting parameter related to the amplitude of traps. Now, the main current source is given by:

$$I_{ds} = I_{pk0}(v_{ds,eff}) \cdot (1 + \tanh(\psi)) \tanh(\alpha \cdot v_{ds}) \cdot (1 + \lambda(v_{ds,eff}) \cdot v_{ds} + L_{sb0} \cdot e^{(v_{dg} - V_{tr})}) \quad (6.5)$$

with

$$\psi = P_1 \cdot (v_{gs,eff} - V_{pkm}) + P_2 \cdot (v_{gs,eff} - V_{pkm})^2 + P_3 \cdot (v_{gs,eff} - V_{pkm})^3 \quad (6.6)$$

$$V_{pkm} = V_{pks} - D_{vpks} + D_{vpks} \cdot \tanh(\alpha_s(v_{ds,eff}) \cdot v_{ds}) \quad (6.7)$$

$$\alpha = \alpha_r + \alpha_s(v_{ds,eff}) \cdot (1 + \tanh(\psi)) \quad (6.8)$$

Moreover, the equations of the parameter-scaling drain-lag model can be described as

$$I_{pk0}(v_{ds,eff}) = I_{pk0,cons} \cdot (1 + Tr_{Ipk0} \cdot v_{ds,eff}) \quad (6.9)$$

$$\alpha_s(v_{ds,eff}) = \alpha_{s,cons} \cdot (1 + Tr_{alphas} \cdot v_{ds,eff}) \quad (6.10)$$

$$\lambda(v_{ds,eff}) = \lambda_{cons} \cdot (1 + Tr_{lambda} \cdot v_{ds,eff}) \quad (6.11)$$

In these equations, only the parameter  $k$  of the Quéré drain-lag model remains to be determined. It is assumed in [44, 48] to be dependent on the estimated output current  $I_{ds,EST}$ . However, the mathematical formulation of the bias dependence of  $k$  is tedious.

The influence of traps should be regarded as an unmodifiable parameter to a transistor. Hence, in order to simplify the expression of  $k$ , the parameter-scaling drain-lag model was adopted to pre-estimate the impact of traps. In this way, the parameter  $k$  is now related to the rest of the impact of traps, which cannot be described by the parameter-scaling drain-lag model. It has been found that the value of  $k$  tends to be constant instead of following a complicated function and the final model can achieve the same or even better model accuracy.

## 6.1.2 Output Conductance Match

In order to overcome the drawback of the parameter-scaling drain-lag model in mismatch of  $S_{22}$ , the Quéré drain-lag model is integrated. Now, the correction term  $\Delta G_{ds}$ , which takes the difference between RF and DC output conductances into account, can be formulated as:

$$\Delta G_{ds} = G_{ds,RF} - G_{ds,DC} = I_{pk0}(v_{ds,eff}) \cdot \frac{A \cdot C}{\cosh^2(\alpha v_{ds})} \cdot (\alpha + \alpha_s(v_{ds,eff})) \cdot v_{ds} \cdot f\left(\frac{\partial v_{gs}}{\partial v_{ds}}\right) + I_{pk0}(v_{ds,eff}) \cdot B \cdot C \cdot f\left(\frac{\partial v_{gs}}{\partial v_{ds}}\right) \quad (6.12)$$

with

$$f\left(\frac{\partial v_{gs}}{\partial v_{ds}}\right) = \frac{1}{\cosh^2(\psi)} \left( P_1 \cdot \frac{\partial v_{gs}}{\partial v_{ds}} + 2 \cdot P_2 \cdot (v_{gs} - V_{pkm}) \cdot \frac{\partial v_{gs}}{\partial v_{ds}} + 3 \cdot P_3 \cdot (v_{gs} - V_{pkm})^2 \cdot \frac{\partial v_{gs}}{\partial v_{ds}} \right) \quad (6.13)$$

where

$$A = 1 + \tanh(\psi) \quad (6.14)$$

$$B = \tanh(\alpha \cdot v_{ds}) \quad (6.15)$$

$$C = 1 + \lambda(v_{ds,eff}) \cdot v_{ds} + L_{sb0} \cdot e^{(v_{dg} - V_{tr})} \quad (6.16)$$

According to Equation (6.3 and 6.4), we have:

$$\frac{\partial v_{gs}}{\partial v_{ds}} = k - k \cdot \frac{\partial v_{ds,eff}}{\partial v_{ds}} = \begin{cases} k & \text{(emission)} \\ 0 & \text{(capture)} \end{cases} \quad (6.17)$$

It is evident that the parameter  $k$  could be simply extracted from the  $G_{ds}$  of equivalent small-signal model, which is known to be strongly influenced by the drain-lag effects [46]. The detailed parameter extraction procedure will be discussed in the next section.

## 6.2 Model Parameter Extraction

The extraction procedure for the parameters  $Tr_{ipk0}$ ,  $Tr_{alphas}$ ,  $Tr_{lambda}$ ,  $\tau_{emission}$  and  $\tau_{capture}$  has been already revealed in last chapter and also in reference [49]. Therefore, only one parameter left to be determined: the parameter  $k$ .

As mentioned before, the parameter  $k$  can be determined by fitting the model against the value  $G_{ds}$  of the small-signal model extracted from pulsed multi-bias S-parameter measurements. Considering the importance of traps for the extraction of  $k$ , it is necessary to determine  $k$  under different trap states. Hence, the pulsed

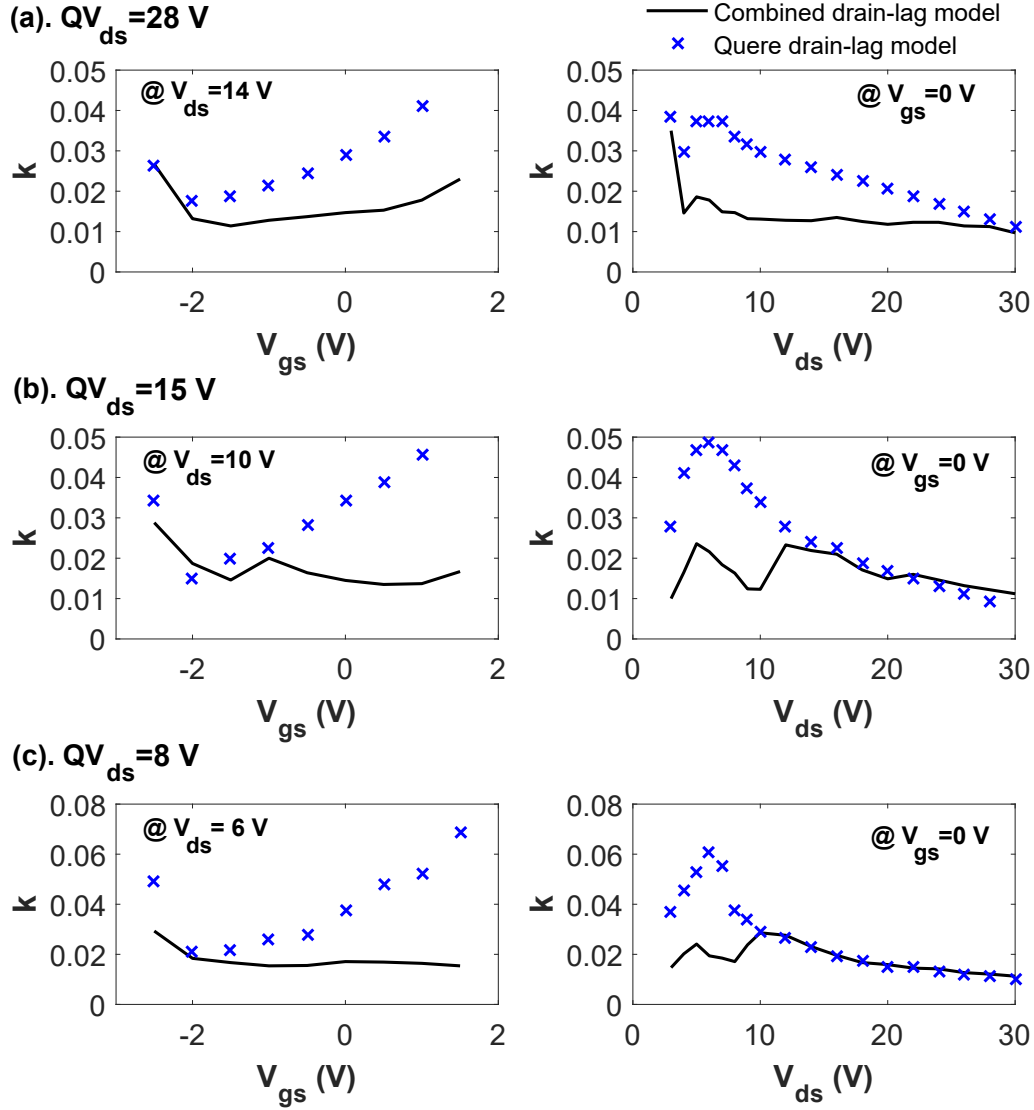


Figure 6.3: Extracted values of  $k$  as a function of  $v_{gs}$  at  $v_{ds}$  below  $QV_{ds}$  (at the left-hand side) and function of  $v_{ds}$  at  $v_{gs} = 0$  V (at the right-hand side).  $k$  is extracted by fitting the model against pulsed  $I_{ds}$  and  $G_{ds}$  at  $QV_{ds} = 28$  V, 15 V, and 8 V. (black solid lines: for combined drain-lag model, blue crosses: for Quéré drain-lag model).

multi-bias S-parameter measurements at different quiescent drain voltages  $QV_{ds} = 8$  V, 15 V, and 28 V are presented here.

Fig. 6.3 shows the extracted values of  $k$  as a function of  $v_{gs}$  and  $v_{ds}$  for the combined drain-lag and the Quéré drain-lag model. From the extracted values of  $k$  against  $v_{gs}$ , it can clearly be observed that the extracted  $k$  for the combined drain-lag model shows a smooth and quasi-constant value for  $v_{gs} > -2$  V at each trap state,

while that for the Quéré drain-lag model rises with increasing  $v_{gs}$ .

In this work, the pulsed measurements with a pulse length of 250 ns were used under the assumption that the device is free from the self-heating and drain-lag effects [47, 52, 97]. However, the assumption doesn't correspond with the reality, since the trapping (capture process) time constant lies normally in nanosecond range that is much shorter than the pulse length, while the detrapping (emission process) time constant is of microsecond level that is longer than the pulse length, which means that only the capture process will occur in the pulsed measurements. With this in mind, the curves of extracted values of  $k$  against  $v_{ds}$  can be split in two cases:

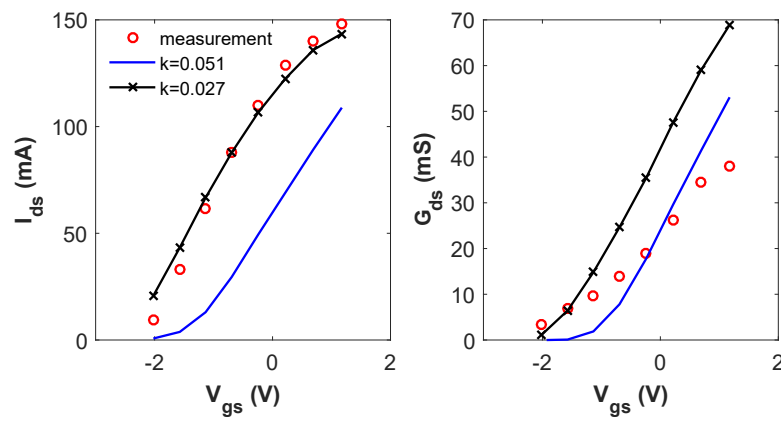


Figure 6.4: Measured (circles) and modeled (lines) pulsed  $I_{ds}$  and  $G_{ds}$  for  $v_{ds} = 3$  V at  $QV_{ds} = 28$  V with different  $k$  extracted by fitting the model against only  $G_{ds}$  (blue lines) and against both  $I_{ds}$  and  $G_{ds}$  (black lines with symbols).

1).  $v_{ds} < QV_{ds}$ : The drain-source voltage is pulsed down during a pulse, and the slow emission process predominates for the traps. In this process, the voltage  $v_{ds,eff}$  in equation (2.64) presents a slow voltage transient from  $QV_{ds}$  to dynamic  $v_{ds}$  and should be considered different from the dynamic  $v_{ds}$  in the short pulse, which puts the parameter  $k$  in a critical position of the  $i_{ds}$  description. Hence, in the extraction of  $k$ , not only extracted  $G_{ds}$  but also measured pulsed  $i_{ds}$  should be accounted for in the region  $v_{ds} < QV_{ds}$ , otherwise a mismatch for the I/V characteristics as shown in Fig. 6.4 may come up. As illustrated in Fig. 6.3, it is evident that the extracted values of  $k$  for combined drain-lag model tend to be constant thanks to the prediction of the behavior of the related traps through the parameter-scaling drain-lag model according to equations (5.1) - (5.3). In contrast, the parameter  $k$  exhibits a rather complicated behavior for the Quéré drain-lag model.

2).  $v_{ds} > QV_{ds}$ : The drain-source voltage is pulsed up. Hence, the fast capture process predominates, and the voltage  $v_{ds,eff}$  changes quickly from  $QV_{ds}$  to dynamic  $v_{ds}$  in the pulse. In this situation, the parameter  $k$  does not influence the output current  $i_{ds}$  any more, and the traps are now dependent on the related dynamic voltages ( $v_{gs}$  and  $v_{ds}$ ), which are same for the combined and the Quéré drain-lag model. Hence, the extracted values of  $k$  are the same.

## 6.3 Model Verification

After modeling the drain-lag effects, the modified Chalmers model including this combined drain-lag model was implemented in a Verilog-A design kit for the ADS simulator [93]. A large-signal model extracted by using the procedure described in this chapter has been validated by comparing the simulations with measurements of a further transistor type.

In this section, model verification results are reported in detail on different bias points and for different types of stimuli, i.e., (1) pulsed I/V characteristics, (2) Pulsed S-parameters, (3) Load-Pull performance at optimum load impedances for max.  $P_{out}$ , and (4) Large-signal measurements at low frequency.

### 6.3.1 Pulsed I/V Characteristics

Fig. 6.5 shows a comparison between modeled pulsed I/V characteristics by using the standard Chalmers model with RC sub-circuit (blue marked lines), the parameter-scaling drain-lag model (gray dashed lines) and the combined drain-lag mode (black solid lines). Here, three standard Chalmers models were separately extracted by using pulsed S-parameter measurements with these different  $QV_{ds}$ , which has been proved in enabling them to achieve a good fit of the pulsed drain current  $i_{ds}$ . However, on one hand, the good fit is confined to  $v_{ds} < QV_{ds}$ , since the process of capture is not considered in the model. On the other hand, the pulsed drain current  $i_{ds}$  becomes negative in a part of the simulated I/V networks, which is non-physical. This is because the correction term  $\Delta G_{ds}$  provided by the RC branch is always constant, even in the low  $v_{gs}$  and low  $v_{ds}$  region.

Although the general fit is acceptable using the parameter-scaling drain-lag model and a good modeling accuracy is achieved around the quiescent bias, the accuracy

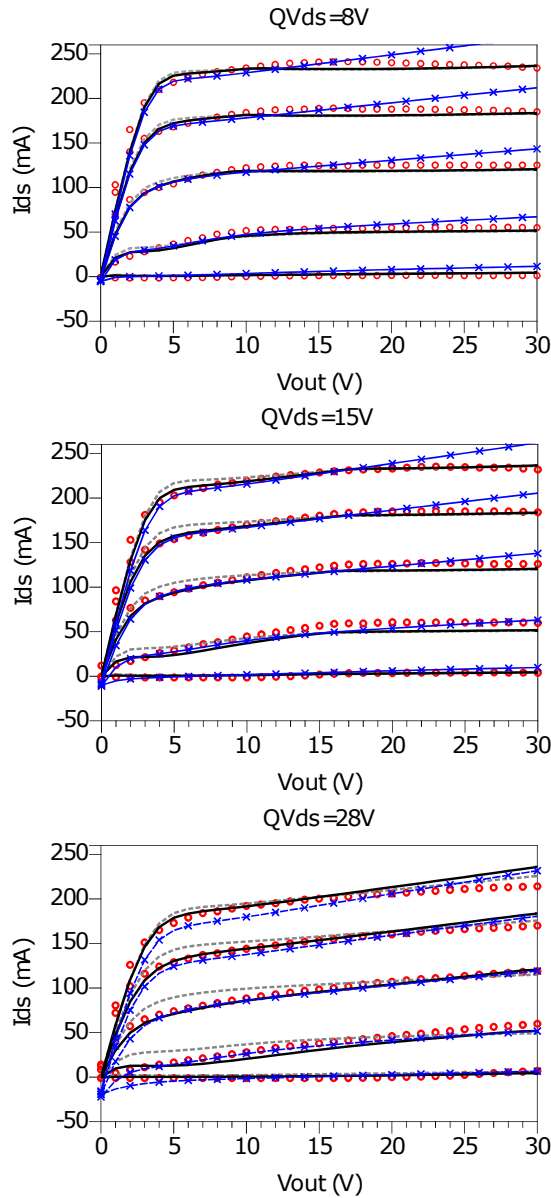


Figure 6.5: Pulsed I/V measurements (symbols) for  $v_{gs}$  from -3 V to 1 V with 1 V steps at  $QV_{ds} = 28$  V, 15 V, and 8 V, pulsed simulations (lines) in the same conditions by using the standard Chalmers models (blue marked lines), the parameter-scaling drain-lag model (gray dashed lines) and the combined drain-lag model (black solid lines).

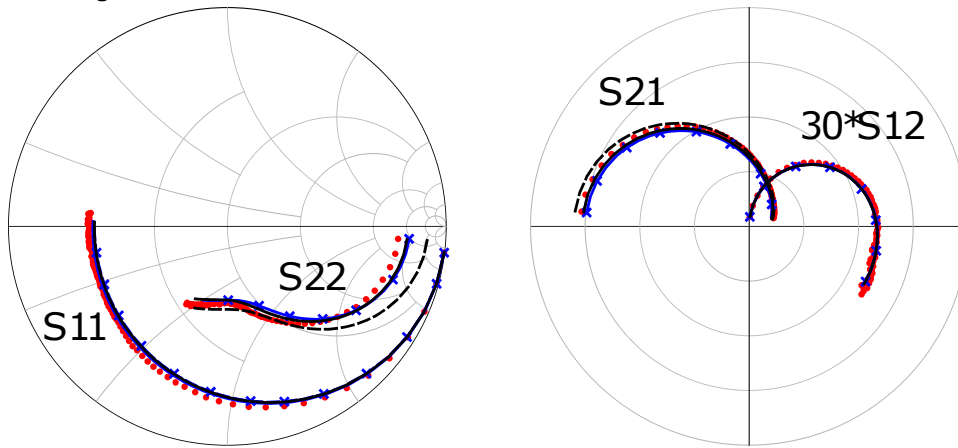
of prediction of typical kink in the pulsed I/V curves observed around  $v_{ds} = QV_{ds}$  is still limited, and, even more pronounced, the model cannot describe the knee walk-out effect. However, these problems of the both models have been obviously solved by using the new drain-lag model described previously.

### 6.3.2 Pulsed S-Parameters

Pulsed S-parameters were measured for each bias of the I/V characteristic illustrated in Fig. 6.5 and also at different quiescent drain voltages  $QV_{ds} = 8$  V, 15 V, and 28 V. To verify the models extracted with these S-parameters, we should focus on the two following regions according to different processes of drain-lag effects:

a) If the dynamic  $v_{ds}$  is below the quiescent drain voltages  $QV_{ds}$ , the drain voltage

(a):  $v_{gs} = -2$  V;  $v_{ds} = 8$  V



(b):  $v_{gs} = -2$  V;  $v_{ds} = 22$  V

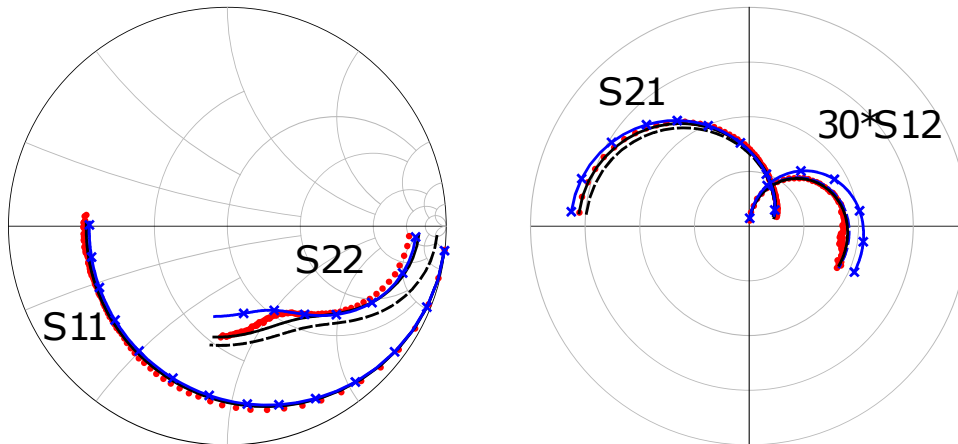


Figure 6.6: Measured (red dots) and simulated (lines) pulsed S-parameters from 400 MHz to 40 GHz for  $QV_{ds} = 15$  V and  $QV_{gs} = -2.3$  V at (a)  $v_{ds} = 8$  V,  $v_{gs} = -2$  V and (b)  $v_{ds} = 22$  V,  $v_{gs} = -2$  V. (blue marked lines: the standard Chalmers model, black dashed lines: the parameter-scaling drain-lag model, black solid lines: the combined drain-lag model).



is reduced during a pulse. In this case, the emission process dominates for drain-lag-related traps and the traps remain overcharged related to the  $QV_{ds}$ . Fig. 6.6(a) shows the measured pulsed S-parameters biased at  $v_{ds} = 8$  V below  $QV_{ds} = 15$  V versus that simulated by the Chalmers model with the standard Chalmers model (blue marked lines), the parameter-scaling drain-lag model (dashed lines), and with the combined drain-lag model (black solid lines). The good modeling performance of  $S_{11}$  and  $S_{12}$  using all of these three models indicate the good agreement of the intrinsic capacitances  $C_{gs}$  and  $C_{gd}$ . Moreover, it is well known that  $S_{21}$  is basically influenced by the drain current. Therefore, the better correspondence with the simulated  $S_{21}$  using the standard Chalmers model and the combined drain-lag model testifies the better drain current modeling accuracy as shown in Fig. 6.5. Moreover, it can clearly be observed that the parameter-scaling drain-lag model fails to predict  $S_{22}$ , which is strongly related to the output conductance  $G_{ds}$ . This problem can be solved if a correction term  $\Delta G_{ds}$  is provided, e.g., by the RC branch of the standard Chalmers model or by the parameter  $k$  of the combined drain-lag model.

*b)* If the dynamic  $v_{ds}$  is higher than the quiescent drain voltages  $QV_{ds}$ , the drain voltage is increased during a measurement pulse period. In this case, the capture process predominates and the response time for the drain voltage change is very short. The S-parameters measured under this condition can be considered very close to the ones measured under static condition without self-heating. Fig. 6.6(b) presents the measured and simulated pulsed S-parameters at  $v_{ds} = 22$  V. The discrepancies between measured and simulated pulsed S-parameters by using the standard Chalmers model further demonstrate its uselessness for the capture process. For the use of the parameter-scaling drain-lag model and the combined drain-lag model, a similar situation of case (a) can clearly be observed: a significantly improved fit for  $S_{22}$  is obtained by using the combined drain-lag model.

### 6.3.3 Load-Pull Performance

To further verify this large-signal model, load-pull measurements at 8 V, 15 V, and 28 V and at 8 GHz were performed. The source and load impedances were chosen as optimum impedances for providing maximum output power. Furthermore, the impedances at second harmonic were also supplied in the simulation in order to better reproduce the measurement condition.

The impact of trapping effects on average output drain-source current, especially

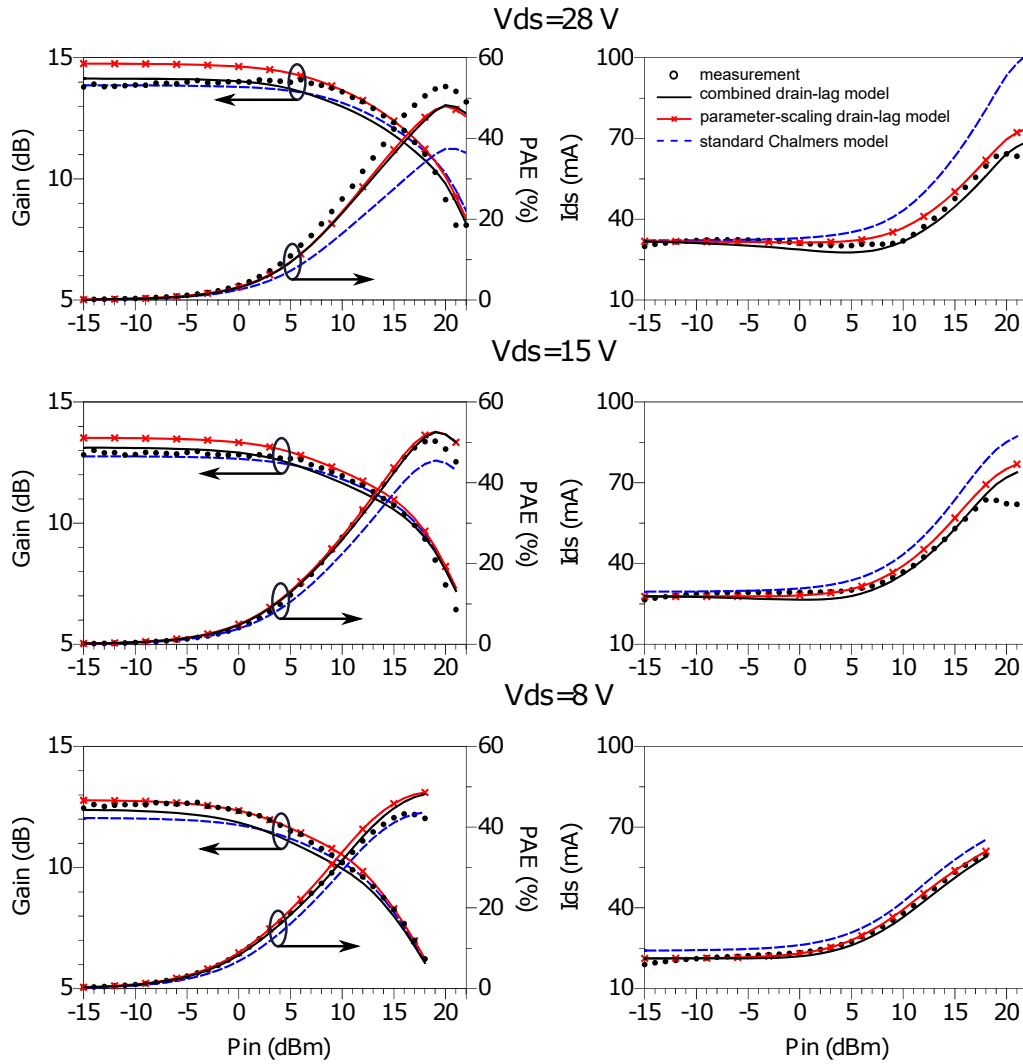


Figure 6.7: Measured and simulated gain, PAE, and mean  $I_{ds}$  as a function of input power  $P_{in}$  at 8 GHz for  $v_{ds} = 28$  V, 15 V, and 8 V, (black dots: measurements, black solid lines: simulation with combined drain-lag model, red marked lines: simulation with the parameter-scaling drain-lag model, blue dashed lines: simulation with standard Chalmers models extracted from pulsed S-parameter measurements at  $QV_{ds} = 28$  V, 15 V, and 8 V, respectively).

drain-lag effects, is particularly obvious, for the trapping effects significantly hamper the achievable output power and degrade the output current. The constant RC branch parallel to  $i_{ds}$ , which was employed in the standard Chalmers model, was supposed to describe this impact of trapping effects. However, as can be seen in Fig. 6.7, its ability to describe the trapping effects is still very limited, although the

used standard models were especially extracted by using pulsed S-parameter measurements with  $QV_{ds}$  same as the bias condition of load-pull measurement, which can improve the modeling accuracy [41].

The parameter-scaling drain-lag model leads to a significant improvement of prediction accuracy for PAE and mean output current, especially at higher  $V_{ds}$  condition, where the impact of drain-lag effects is more pronounced. However, at the same time, further improvements in predicting the mean output current could be expected by using the combined drain-lag model.

Moreover, the parameter-scaling drain-lag model fails to predict the gain in the linear region due to the mismatch of the S-parameters, i.e.,  $S_{22}$  as shown in Fig. 5.12, while a good agreement in predicting the gain in the linear region has been achieved by using the combined drain-lag model.

### 6.3.4 Low-Frequency Large-Signal Behavior

In order to further validate the accuracy of the proposed model under actual operating conditions, large-signal network analyzer (LSNA) measurements [51, 98, 99] were performed at low-frequency (i.e., 2 MHz). This operating frequency, chosen to

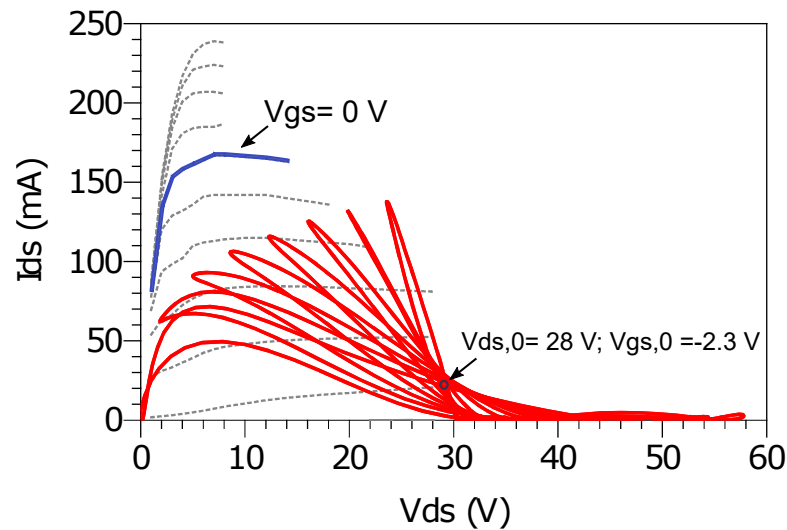


Figure 6.8: The load lines (red solid lines) synthesized during the low-frequency LSNA measurement. A bias point of  $v_{ds,0} = 28$  V and  $v_{gs,0} = -2.3$  V is studied. The measured DC I/V characteristics (dashed lines) are also shown with the I/V characteristic at  $v_{gs,0} = 0$  V is highlighted.

lay above the cut-off frequency of dispersive effects, allows focusing on the correct evaluation of the I/V model, avoiding the presence of linear and nonlinear dynamic effects. In this way the impact of the low-frequency dispersion effect, i.e., mainly the trapping effect, can be well isolated.

Fig. 6.8 illustrates the load lines synthesized during the 2 MHz LSNA measure-

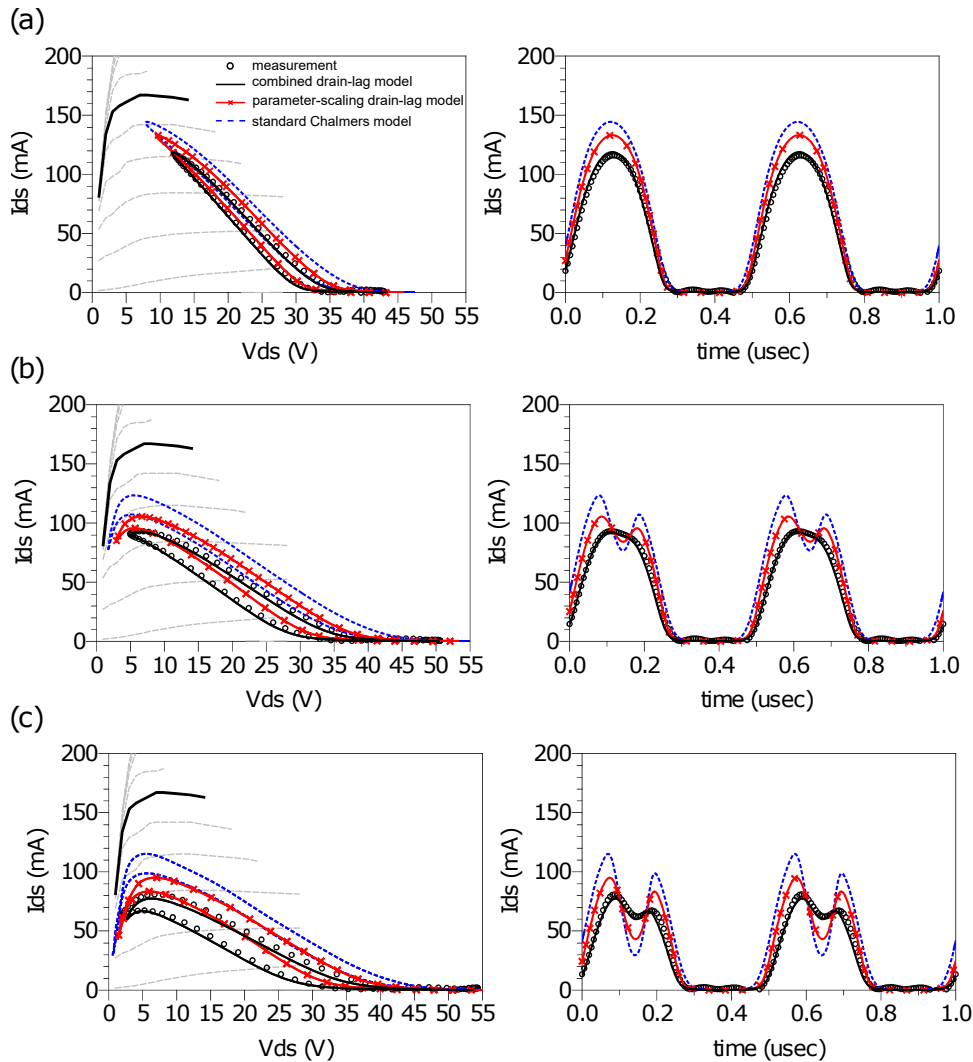


Figure 6.9: Measured (black circles) and simulated (lines) load lines and output current in time-domain waveform under large-signal operation at 2 MHz with drain incident wave with amplitudes of (a): 15 V; (b): 23 V; (c): 27 V; (blue dashed lines: simulation with standard Chalmers model; red marked lines: simulation with the parameter-scaling drain-lag model; black solid lines: simulation with combined drain-lag model).

ments at a bias point of  $v_{ds,0} = 28$  V and  $v_{gs,0} = -2.3$  V. For each load line, the gate incident signal is a sinusoidal wave with a constant amplitude of 1.15 V, chosen to dynamically reach  $v_{gs} = 0$  V (i.e., since the FET input port at 2 MHz behaves as an open circuit, the gate voltage amplitude is twice the gate incident amplitude), whereas the amplitude of the drain incident wave is swept with values from 4 V to 29 V. Compared with the DC I/V characteristic at  $v_{gs,0} = 0$  V, the impact of the dispersive phenomena related to traps can clearly be observed.

Fig. 6.9 shows the comparison between measured and simulated load lines and time-domain output current under large-signal operation at 2 MHz for three different amplitudes of the drain voltage: 15 V, 23 V, and 27 V. The simulations were performed with three different models: the standard Chalmers model; the parameter-scaling drain-lag model and the new proposed drain-lag model. It is evident that the standard Chalmers model shows its limitation in taking into account the difference between output current measured under DC and large-signal conditions, whereas both of the adopted drain-lag models yield an improvement in predicting the output current in the presence of traps. However, the parameter-scaling drain-lag model still overestimates the output currents along the whole load lines, while, at the same time, the combined drain-lag model is able to reproduce the output current with a better level of accuracy.

## 6.4 Conclusion

In this chapter, an improved drain-lag model for GaN HEMTs based on the Chalmers model and pulsed S-parameter measurements is presented. This proposed drain-lag model is combined from two published drain-lag descriptions, not only taking the advantages of both models but also overcoming the drawbacks of both.

It is shown that only four constant model parameters have to be extracted by means of fitting them against the measured pulsed  $i_{ds}$  and the calculated  $i_{ds}$ -related parameters  $g_m$  and  $G_{ds}$ . This greatly simplifies the modeling procedure for the trapping effects.

The proposed drain-lag model has been validated by several types of measurements: pulsed I/V characteristics, pulsed S-parameters, load-pull performance under different conditions, and time-domain output current at low frequency under large-signal condition. Good agreement was found which demonstrates that this

drain-lag model can accurately predict the performance of GaN HEMTs in the presence of trapping effects.

# Chapter 7

## General Conclusions and Future Work

AlGaN/GaN HEMT devices are considered to be very promising candidate for high power and high speed applications, owing to their properties such as high breakdown voltage, high charge density, and high electron mobility. However, the existence of trapping effects limits the wide application of AlGaN/GaN HEMT and especially increases the difficulty of modeling.

Taking into account the shortcomings of the published trap models like unsatisfactory prediction accuracy or complexity of the parameter extraction, a trap model for GaN HEMT based on the Chalmers model is developed. The trapping effects have been characterized using pulsed I/V and S-parameter measurements. The trap model is proven to be able to predict the large-signal behavior of the researched device.

The following paragraphs give a brief summary of this work and outline the general future trend in the characterization and modeling of AlGaN/GaN HEMT.

### 7.1 Key Research Results

This thesis started with the outlining of the motivation for trapping effects modeling of GaN HEMTs. The limitations of the former published trap models have been discussed in detail. On the one hand, some of them, e.g., the RC branch used in the standard Chalmers model [38], are of little use in predicting the whole impact of the trapping effects such as knee-walkout effects and typical kink observed from

PIVs. On the other hand, some of them, e.g., the Quéré trap model published in [48], are able to predict the trapping effects accurately. However, the complexity of their parameters or the parameter extraction procedures excludes them easily from the consideration of the users, mainly the model developers and circuit designers. Hence, the need for a simple yet accurate trap model is still pressing within the modeling research community.

Almost all the published trap models were based on pulsed I/V measurements. These measurements are very efficient to observe the impact of the trapping effect and also to verify the resulting trap models, since they are able to reduce the self-heating and freeze the trap state below used quiescent bias. However, this type measurement also shows its limitation on quantifying the impact of the trapping effects due to the high and non-negligible uncertainty of the current measuring. Given this situation, pulsed multi-bias S-parameter measurements were used in this work. The data reading accuracy of the pulsed S-parameter measurements is secured in Chapter 3 by using proposed data reading strategy. Hence, these measurements enable an accurate extraction of the intrinsic capacitances and the differential information of  $i_{ds}$ , e.g.,  $g_m = \frac{\partial i_{ds}}{\partial v_{gs}}$  and  $G_{ds} = \frac{\partial i_{ds}}{\partial v_{ds}}$  under given trap states. The use of  $g_m$  and  $G_{ds}$  instead of the pulsed  $i_{ds}$  ensures the accurate extraction of the trap-related parameters.

In the first part of Chapter 4, it is found that the extracted values of the bias-independent extrinsic parameters and the small-signal intrinsic capacitances do not vary too much under the impact of different trap states. Following that, it is shown that the standard Chalmers model is able to yield a good prediction of the transistor performance, if the model is determined relying on pulsed S-parameters and if the range of model validity is constrained to a fixed drain voltage. This gives us the chance to extend the model validity to a wide range of bias points, e.g., in our case at bias  $v_{ds}=8$  V, 15 V, and 28V. In this way, by comparing the extracted model parameter sets, the trap-related parameters can be focused in the scope of large-signal modeling.

In Chapter 5, it is found that the parameters  $I_{pk0}$ ,  $\alpha_r$ , and  $\lambda$  are very sensitive to traps and can be determined by different trap states, while the other parameters of the standard Chalmers model can be kept constant with different trap states. Moreover, these three trap-dependent parameters show a rather linear dependence on the trap states controlled by the quiescent bias point, which yields simple scal-



ing rules and easy model implementation. These realized a drain-lag model, named parameter scaling drain-lag model. This drain-lag model relies on scaling of these three trap-dependent parameters with quiescent drain voltage which yields convenient parameter extraction. Moreover, the asymmetry of the emission and capture time constant is also considered by using a “2-path RC branch”. In this way, this drain-lag model is able to rough estimate the knee-walkout effects and typical kink. However, although it has been proven to predict device large-signal performance well for various trap states, significant discrepancies can be clearly observed when comparing the simulated pulsed S-parameters with the measured ones for the real part of  $S_{22}$ , which is strongly influenced by  $G_{ds}$ . This is mainly due to the absence of the RC branch of the standard Chalmers model, which provides a correction term  $\Delta G_{ds}$  to account for the difference between the output conductance obtained from DC I/V measurements and that extracted from small-signal RF characteristics.

In Chapter 6, this drawback was overcome by integrating the Quéré drain-lag model in the parameter-scaling drain-lag model. The Quéré drain-lag model employs a pseudo gate-source voltage at the input of the current source. The pseudo gate-source voltage is related to a fitting parameter  $k$ , which is linked to the amplitude of traps and is assumed to be linearly dependent on the output current. However, our investigations have shown that, instead of the complicated expression of parameter  $k$  as presented in Quéré drain-lag model, a constant value should bring the same modeling performance if combined with the parameter-scaling drain-lag model. This can significantly simplify the model parameters extraction process.

Firstly, the new drain-lag model, named combined drain-lag model, has been validated by pulsed I/V characteristics (PIVs). Good agreement was found which demonstrates that this drain-lag model can accurately predict the impact of trapping effects on PIVs: the knee-walkout effects and the typical kink. Secondly, this drain-lag model was further validated by pulsed S-parameter measurements. It is shown that the integration of the Quéré drain-lag model has efficiently overcome the drawback of the parameter-scaling drain-lag model. Finally, large-signal measurements were used, and the good correspondence between measurements and simulation indicates the validation of the proposed drain-lag model.

## 7.2 Future Works

The following investigations are proposals of future work that outcome of the work reported in this thesis:

- Investigation of the thermal-dependency in the values of the drain-lag model parameters, applying a thermal-trap model [100].
- Investigation of the extraction procedure for thermal model based on pulsed S-parameter measurements at different ambient temperatures. The thermal fitting parameters, which account for the temperature dependency of the non-linear model elements, should be also accurately extracted and included in the model in order to simulate larger device sizes.
- Investigation of the extraction procedure for extrinsic parameters of devices with larger size. The reliability of the extracted values of extrinsic parameters strongly depends on the quality of the “Cold FET” S-parameter measurements. However, these measurements suffer from non-avoidable measurement uncertainty [101]. Therefore, a new extraction procedure should be done in order to provide reliable values for extrinsic parameters.

Measurement-based large-signal modeling techniques will remain as the most practical approach for GaN HEMT modeling in the future. However, accurately modeling requires addressing a number of challenging problems. Many research works have already been made to deal with some issues and some works still remain in the “to-do list”.

# Appendix A

## $i_{ds}$ -Related Parameters

The drain current function of the Chalmers model is given by the following [38]:

$$I_{ds} = I_{pk0} \cdot (1 + \tanh(\psi)) \cdot \tanh(\alpha \cdot V_{ds}) \cdot (1 + \lambda \cdot V_{ds}) \quad (\text{A.1})$$

with

$$\psi = P_{1m} \cdot (V_{gs} - V_{pkm}) + P_2 \cdot (V_{gs} - V_{pkm})^2 + P_3 \cdot (V_{gs} - V_{pkm})^3 \quad (\text{A.2})$$

$$P_{1m} = P_1 \cdot (1 + B_1 / \cosh^2(B_2 \cdot V_{ds})) \quad (\text{A.3})$$

$$V_{pkm} = V_{pks} - D_{vpks} + D_{vpks} \cdot \tanh(\alpha_s \cdot V_{ds}) \quad (\text{A.4})$$

$$\alpha = \alpha_r + \alpha_s \cdot (1 + \tanh(\psi)) \quad (\text{A.5})$$

The output transconductance  $g_m$  is the partial derivative of  $I_{ds}$  to  $V_{gs}$ , while the output conductance  $G_{ds}$  is the partial derivative of  $I_{ds}$  to  $V_{ds}$ . Hence, we have:

$$\begin{aligned} g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \Big|_{V_{ds}=\text{const}} &= I_{pk0} \cdot (1 + \lambda \cdot V_{ds}) \cdot \frac{1}{\cosh^2(\psi)} \cdot (P_{1m} + 2 \cdot P_2 \cdot (V_{gs} - V_{pkm}) + \\ & 3 \cdot P_3 \cdot (V_{gs} - V_{pkm})^2) \cdot (\tanh(\alpha \cdot V_{ds}) + \\ & (1 + \tanh(\psi)) \cdot \frac{\alpha_s \cdot V_{ds}}{\cosh^2(\alpha \cdot V_{ds})}) \end{aligned} \quad (\text{A.6})$$

$$\begin{aligned}
G_{ds} = \frac{\partial I_{ds}}{V_{ds}} \Big|_{V_{gs}=\text{const}} &= I_{pk0} \cdot \frac{(1 + \tanh(\psi)) \cdot \tanh(\alpha \cdot V_{ds})}{\cosh^2(\alpha \cdot V_{ds})} \cdot (\alpha + \alpha_s \cdot V_{ds} \cdot X) + \\
&I_{pk0} \cdot \tanh(\alpha \cdot V_{ds}) \cdot (1 + \lambda \cdot V_{ds}) \cdot X + \\
&I_{pk0} \cdot (1 + \tanh(\psi)) \cdot \tanh(\alpha \cdot V_{ds}) \cdot \lambda
\end{aligned} \tag{A.7}$$

with

$$\begin{aligned}
X = \frac{1}{\cosh^2(\psi)} \cdot \frac{D_{vpks} \cdot \alpha_s}{\cosh^2(\alpha_s \cdot V_{ds})} \cdot (-P_{1m} - 2 \cdot P_2 \cdot (V_{gs} - V_{pkm}) - 3 \cdot P_3 (V_{gs} - V_{pkm})^2 - \\
\frac{2 \cdot B_1 \cdot B_2 \cdot P_1 \cdot \sinh(B_2 \cdot V_{ds})}{\cosh^3(B_2 \cdot V_{ds})})
\end{aligned} \tag{A.8}$$

# Appendix B

## Classical Capacitances and Transcapacitances

The formulations of the Chalmers charge model have been presented in [71] as:

$$Q_{gs} = C_{gs\pi} \cdot V_{gs} + \frac{C_{gs0}}{P_{11}} \cdot (1 - P_{111} + \tanh(\phi_2)) \cdot (\phi_1 + \ln(\cosh(\phi_1)) - Q_{gs0}) + 2 \cdot C_{gs0} \cdot P_{111} \cdot V_{gs} \quad (\text{B.1})$$

$$Q_{gd} = C_{gd\pi} \cdot V_{gd} + \frac{C_{gd0}}{P_{41}} \cdot ((1 - P_{111} + \tanh(\phi_3)) \cdot (\phi_4 + \ln(\cosh(\phi_4)) - Q_{gd0}) + 2 \cdot C_{gd0} \cdot P_{111} \cdot V_{gd}) \quad (\text{B.2})$$

with

$$\phi_1 = P_{10} + P_{11} \cdot V_{gs} + P_{111} \cdot V_{ds} \quad (\text{B.3})$$

$$\phi_2 = P_{20} + P_{21} \cdot V_{ds} \quad (\text{B.4})$$

$$\phi_3 = P_{30} - P_{31} \cdot V_{ds} \quad (\text{B.5})$$

$$\phi_4 = P_{40} + P_{41} \cdot V_{gd} - P_{111} \cdot V_{ds} \quad (\text{B.6})$$

$$Q_{gs0} = P_{10} + P_{111} \cdot V_{ds} + \ln(\cosh(P_{10} + P_{111} \cdot V_{ds})) \quad (\text{B.7})$$

$$Q_{gd0} = P_{40} - P_{111} \cdot V_{ds} + \ln(\cosh(P_{40} - P_{111} \cdot V_{ds})) \quad (\text{B.8})$$

The classical capacitances and the transcapacitances yield:

$$C_{gs,class} = \left. \frac{\partial Q_{gs}}{V_{gs}} \right|_{V_{ds}=const} = C_{gs\pi} + C_{gs0} \cdot (1 + \tanh(\phi_1)) \cdot (1 + \tanh(\phi_2) - P_{111}) + 2 \cdot C_{gs0} \cdot P_{111} \quad (\text{B.9})$$

$$C_{gd,class} = \left. \frac{\partial Q_{gd}}{V_{gd}} \right|_{V_{ds}=const} = C_{gd\pi} + C_{gd0} \cdot (1 + \tanh(\phi_3) - P_{111}) \cdot (1 + \tanh(\phi_4)) + 2 \cdot C_{gd0} \cdot P_{111} \quad (\text{B.10})$$

$$C_{gs,tr} = \left. \frac{\partial Q_{gs}}{V_{ds}} \right|_{V_{gs}=const} = \frac{P_{21} \cdot C_{gs0}}{P_{11} \cdot \cosh^2(\phi_2)} \cdot (\phi_1 + \ln(\cosh(\phi_1)) - Q_{gs0}) + \frac{C_{gs0} \cdot P_{111}}{P_{11}} \cdot (1 + \tanh(\phi_2) - P_{111}) \cdot (\tanh(\phi_1) - \tanh(P_{10} + P_{111} \cdot V_{ds})) \quad (\text{B.11})$$

$$C_{gd,tr} = \left. \frac{\partial Q_{gd}}{V_{ds}} \right|_{V_{gd}=const} = - \frac{P_{31} \cdot C_{gd0}}{P_{41} \cdot \cosh^2(\phi_3)} \cdot (\phi_4 + \ln(\cosh(\phi_4)) - Q_{gd0}) - \frac{C_{gd0} \cdot P_{111}}{P_{41}} \cdot (1 + \tanh(\phi_3) - P_{111}) \cdot (\tanh(\phi_4) - \tanh(P_{40} - P_{111} \cdot V_{ds})) \quad (\text{B.12})$$

# Appendix C

## List of Symbols

$C_B$	fringing capacitance	F
$C_{ds}, C_{gd}, C_{gs}$	Drain-source, gate-drain, and gate-source capacitance	F
$C_{gd,class}, C_{gs,class}$	Gate-drain, and gate-source classical capacitance	F
$C_{gd,tr}, C_{gs,tr}$	Gate-drain, and gate-source transc capacitance	F
$C_j$	Differential capacitance of the Schottky barrier	F
$C_{pd}, C_{pg}$	Parasitic drain and gate pad capacitance	F
$C_{ps}$	Extrinsic feedback capacitance	F
$C_{th}$	Thermal capacitance	F
$E_g$	Bandgap energy	eV
$G_{ds}$	Drain-source conductance	S
$g_m$	Output transconductance	S
$L_d, L_g, L_s$	Drain, gate, and source inductance	H
$Nd^+, Na^-$	Ionized donors and acceptor density	cm <sup>-2</sup>
$n_s$	Sheet charge concentration ( $\sigma/e$ )	cm <sup>-2</sup>
$q$	Electron charge ( $1.6 \cdot 10^{-19}$ )	coulomb
$P_{in}$	Input power	dBm
$P_{out}$	Output power at Fundamental frequency	dBm
PAE	Power Added Efficiency	%
$Q_{gd}, Q_{gs}$	Intrinsic gate-drain and gate-source charge	C
$QV_{ds}, QV_{gs}$	Quiescent drain-source and gate-source voltage	V
$R_c$	Channel resistance	$\Omega$
$R_d, R_g, R_s$	Extrinsic drain, gate, and source resistance	$\Omega$
$R_i$	Gate-source charging resistance	$\Omega$

$R_j$	Differential resistance of the Schottky barrier	$\Omega$
$R_{th}$	Thermal resistance	$^{\circ}\text{C}/\text{W}$
$S_{ij}$	Scattering parameters	
$T$	Temperature	$^{\circ}\text{C}$
$T_{amb}$	Ambient temperature	$^{\circ}\text{C}$
$T_j$	Junction temperature	$^{\circ}\text{C}$
$Y_{ij}$	Admittance parameters	
$Z_{ij}$	Impedance parameters	
$Z_g, Z_d, Z_s$	Intrinsic gate, drain, and source branch impedance	$\Omega$
$v_{ds}, v_{gs}$	Dynamic drain-source and gate-source voltage	$\text{V}$
$\omega$	angular frequency	$\text{rad/s}$
$\tau$	Transit delay time	$\text{s}$
$\tau_{capture}$	Charge capture time constant	$\text{s}$
$\tau_{emission}$	Charge emission time constant	$\text{s}$
$\sigma$	Sheet charge density	$\text{C}/\text{cm}^2$
$v_{thn}$	Electron thermal velocity	$\text{cm/s}$



# Appendix D

## List of Abbreviations and Acronyms

ADS®	Advanced Design System
AlGaN	Aluminium Gallium Nitride
AlN	Aluminium Nitride
CAD	Computer Aided Design
CW	Continuous Wave
dBm	decibel (mW)
DC	Direct Current
DUT	Device Under Test
EDA	Electronic Design Automation
Fe	Iron
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
LNA	Low noise amplifier
LP	Load-Pull
LSNA	Large-Signal Network Analyzer
MESFET	MEtal-Semiconductor FET
PA	Rower Amplifier
PIV	Pulsed I/V characteristics
RF	Radio Frequency
Si	Silicon

SiC	Silicon Carbide
2DEG	Two-Dimensional Electron Gas

# Bibliography

- [1] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, “Two-Dimensional Electron Gases induced by spontaneous and piezoelectric Polarization Charges in N- and Ga-face AlGaN/GaN Heterostructures,” *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222–3233, 1999.
- [2] L. F. Eastman, V. Tilak, J. Smart, B. M. Green, E. M. Chumbes, R. Dimitrov, H. Kim, O. S. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. J. Schaff, and J. R. Shealy, “Undoped AlGaN/GaN HEMTs for microwave power amplification,” *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 479–485, 2001.
- [3] J. S. Moon, M. Micovic, P. Janke, P. Hashimoto, W.-S. Wong, R. D. Widman, L. McCray, A. Kurdoghlian, and C. Nguyen, “GaN/AlGaN HEMTs operating at 20 GHz with continuous-wave power density  $> 6$  W/mm,” *Electronics Letters*, vol. 37, no. 8, p. 528, 2001.
- [4] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, “High-power microwave GaN/AlGaN HEMTs on semi-insulating silicon carbide substrates,” *IEEE Electron Device Letters*, vol. 20, no. 4, pp. 161–163, 1999.
- [5] U. K. Mishra, S. Likun, T. E. Kazior, and Y.-F. Wu, “GaN-Based RF Power Devices and Amplifiers,” *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.
- [6] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, “A Wideband and Compact GaN MMIC Doherty Amplifier

- for Microwave Link Applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 2, pp. 922–930, 2013.
- [7] H. Klockenhoff, R. Behtash, J. Würfl, W. Heinrich, and G. Tränkle, “A Compact 16 Watt X-Band GaN-MMIC Power Amplifier,” in *IEEE MTT-S International Microwave Symposium digest, 2006* (J. Sowers, ed.), pp. 1846–1849, IEEE Operations Center, 2006.
- [8] K. W. Kobayashi, Y. Chen, I. Smorchkova, R. Tsai, M. Wojtowicz, and A. Oki, “A 2 Watt, Sub-dB Noise Figure GaN MMIC LNA-PA Amplifier with Multi-octave Bandwidth from 0.2-8 GHz,” in *2007 IEEE/MTT-S International Microwave Symposium*, pp. 619–622, 2007.
- [9] C. Andrei, O. Bengtsson, R. Doerner, S. A. Chevtchenko, and M. Rudolph, “Robust stacked GaN-based low-noise amplifier MMIC for receiver applications,” in *2015 IEEE MTT-S International Microwave Symposium*, pp. 1–4, IEEE, 2015.
- [10] J.-W. Lee and K. J. Webb, “A Temperature-Dependent Nonlinear Analytic Model for AlGaN–GaN HEMTs on SiC,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 1, pp. 2–9, 2004.
- [11] S. Nuttinck, E. Gebara, J. Laskar, and H. M. Harris, “Study of self-heating effects, temperature-dependent modeling, and pulsed load-pull measurements on GaN HEMTs,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2413–2420, 2001.
- [12] J. P. Teyssier, J. P. Viaud, and R. Quéré, “A new nonlinear I(V) model for FET devices including breakdown effects,” *IEEE Microwave and Guided Wave Letters*, vol. 4, no. 4, pp. 104–106, 1994.
- [13] I. Angelov, V. Desmaris, K. Dynefors, P. A. Nilsson, N. Rorsman, and H. Zirath, “On the large-signal modelling of AlGaIn/GaN HEMTs and SiC MES-FETs,” in *2006 Asia-Pacific Microwave Conference*, pp. 309–312, 2006.
- [14] K. S. Yuk, G. R. Branner, and D. J. McQuate, “A Wideband Multiharmonic Empirical Large-Signal Model for High-Power GaN HEMTs With Self-Heating and Charge-Trapping Effects,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3322–3332, 2009.

- [15] Y. Xu, W. Fu, C. Wang, C. Ren, H. Lu, W. Zheng, X. Yu, B. Yan, and R. Xu, "A scalable GaN HEMT large-signal model for high-efficiency RF power amplifier design," *Journal of Electromagnetic Waves and Applications*, vol. 28, no. 15, pp. 1888–1895, 2014.
- [16] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaIn/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 465–471, 2001.
- [17] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 560–566, 2001.
- [18] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, "Surface-Related Drain Current Dispersion Effects in AlGaIn–GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 51, no. 10, pp. 1554–1561, 2004.
- [19] R. Wu, S. Webster and A. Anwar, "Physics-based intrinsic model for AlGaIn/GaN HEMTs," *MRS Internet Journal of Nitride Semiconductor Research*, vol. 4S1, 1999.
- [20] T. Wada and J. Frey, "Physical basis of short-channel MESFET operation," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 2, pp. 398–411, 1979.
- [21] J. Golio and R. J. Trew, "Profile studies of ion-implanted MESFET's," *IEEE Transactions on Electron Devices*, vol. 30, no. 12, pp. 1844–1849, 1983.
- [22] J. D. Albrecht, P. P. Ruden, S. C. Binari, and M. G. Ancona, "AlGaIn/GaN heterostructure field-effect transistor model including thermal effects," *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2031–2036, 2000.
- [23] Rashmi, A. Kranti, S. Haldar, M. Gupta, and R. S. Gupta, "Comprehensive analysis of small-signal parameters of fully strained and partially relaxed high Al-content lattice mismatched Al/sub m/Ga/sub 1-m/N/GaN HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 607–617, 2003.

- [24] S. Khandelwal and T. A. Fjeldly, "A physics based compact model of I–V and C–V characteristics in AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT devices," *Solid-State Electronics*, vol. 76, pp. 60–66, 2012.
- [25] M. Li and Y. Wang, "2-D Analytical Model for Current–Voltage Characteristics and Transconductance of AlGa<sub>N</sub>/Ga<sub>N</sub> MODFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 261–267, 2008.
- [26] A. Koudymov, M. S. Shur, G. Simin, K. Chu, P. C. Chao, C. Lee, J. Jimenez, and A. Balistreri, "Analytical HFET I–V Model in Presence of Current Collapse," *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 712–720, 2008.
- [27] D. L. John, F. Allerstam, T. Rodle, S. K. Murad, and G. Smit, "A surface-potential based model for Ga<sub>N</sub> HEMTs in RF power amplifier applications," in *VIII* (H. M. Castor, ed.), (New York N.Y.), pp. 8.3.1–8.3.4, Simon & Schuster Books for Young Readers, 2013.
- [28] L. Sang, Y. Xu, R. Cao, Y. Chen, Y. Guo, and R. Xu, "Modeling of Gan Hemt by Using an Improved K-Nearest Neighbors Algorithm," *Journal of Electromagnetic Waves and Applications*, vol. 25, no. 7, pp. 949–959, 2011.
- [29] D. E. Root, S. Fan, and J. Meyer, "Technology Independent Large Signal Non Quasi-Static FET Models by Direct Construction from Automatically Characterized Device Data," in *21st European Microwave Conference, 1991*, pp. 927–932, IEEE, 1991.
- [30] Y. Long, Y. Guo, Z. Zhong, and Y. C. Leong, "A novel table based large signal model for FETs based on non-quasi-static effect high order sources," in *Asia-Pacific Microwave Conference 2011*, pp. 303–306, 2011.
- [31] M. F. Barciela, P. J. Tasker, M. Demmler, and E. Sanchez, "A simplified nonquasi-static table based FET model," in *26th European Microwave Conference, 1996*, pp. 20–23, IEEE, 1996.
- [32] A. H. Zaabab, Q.-J. Zhang, and M. Nakhla, "A neural network modeling approach to circuit optimization and statistical design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 6, pp. 1349–1358, 1995.

- [33] K. Shirakawa, M. Shimiz, N. Okubo, and Y. Daido, "A large-signal characterization of an HEMT using a multilayered neural network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 9, pp. 1630–1633, 1997.
- [34] J. A. Garca, A. Tazn Puente, A. Mediavilla Snchez, I. Santamara, M. Lzaro, C. J. Pantalen, and J. C. Pedro, "Modeling MESFETs and HEMTs intermodulation distortion behavior using a generalized radial basis function network," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 9, no. 3, pp. 261–276, 1999.
- [35] A.-D. Huang, Z. Zhong, W. Wu, and Y.-X. Guo, "An Artificial Neural Network-Based Electrothermal Model for GaN HEMTs With Dynamic Trapping Effects Consideration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 8, pp. 2519–2528, 2016.
- [36] I. Angelov and H. Zirath, "New empirical nonlinear model for HEMT devices," *Electronics Letters*, vol. 28, no. 2, pp. 140–142, 1992.
- [37] I. Angelov, H. Zirath, and N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 12, pp. 2258–2266, 1992.
- [38] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the Chalmers nonlinear HEMT and MESFET model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1664–1674, 1996.
- [39] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, and H. Zirath, "An empirical table-based FET model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2350–2357, 1999.
- [40] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048–1058, 2002.
- [41] P. Luo, O. Bengtsson, and M. Rudolph, "Novel approach to trapping effect modeling based on chalmers model and pulsed S-parameter measurements," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 157–160, 2016.

- [42] W. Curtice, "The Importance of Using Pulsed Current and RF data for Compact Modeling of RF Power Devices," *Workshop on Compact Modeling for RF/Microwave Applications*, 2007.
- [43] S. J. Doo, P. Roblin, S. Lee, D. Chaillot, and M. V. Bossche, "Pulsed-IV pulsed-RF measurements using a large signal network analyzer," in *65th ARFTG Conference digest*, pp. 62–68, IEEE, 2005.
- [44] O. Jardel, F. D. Groote, C. Charbonniaud, T. Reveyrand, J. P. Teyssier, R. Quéré, and D. Floriot, "A Drain-Lag Model for AlGaIn/GaN Power HEMTs," in *IEEE MTT-S International Microwave Symposium, 2007*, pp. 601–604, 2007.
- [45] Lo Shih-Hsien and C.-P. Lee, "Numerical analysis of frequency dispersion of transconductance in GaAs MESFETs," *IEEE Transactions on Electron Devices*, vol. 43, no. 2, pp. 213–219, 1996.
- [46] S. Choi and M. B. Das, "Origin and modeling of the frequency dependent output conductance in microwave GaAs MESFET's with buried p layer," *IEEE Transactions on Electron Devices*, vol. 41, no. 10, pp. 1725–1733, 1994.
- [47] A. Jarndal, B. Bunz, and G. Kompa, "Accurate Large-Signal Modeling of AlGaIn-GaN HEMT Including Trapping and Self-Heating Induced Dispersion," in *Proceedings of the 18th International Symposium on Power Semiconductor Devices & ICs*, pp. 1–4, 2006.
- [48] O. Jardel, F. D. Groote, T. Reveyrand, J. C. Jacquet, C. Charbonniaud, J. P. Teyssier, D. Floriot, and R. Quéré, "An Electrothermal Model for AlGaIn/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2660–2669, 2007.
- [49] P. Luo, O. Bengtsson, and M. Rudolph, "A drain lag model for GaN HEMT based on Chalmers model and pulsed S-parameter measurements," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 240–243, IEEE, 2017.



- [50] L. C. Nunes, J. M. Gomes, P. M. Cabral, and J. C. Pedro, "A new nonlinear model extraction methodology for GaN HEMTs subject to trapping effects," in *2015 IEEE MTT-S International Microwave Symposium*, pp. 1–4, IEEE, 2015.
- [51] A. Raffo, V. Vadalà, D. Schreurs, G. Crupi, G. Avolio, A. Caddemi, and G. Vannini, "Nonlinear Dispersive Modeling of Electron Devices Oriented to GaN Power Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 4, pp. 710–718, 2010.
- [52] J. B. King and T. J. Brazil, "Nonlinear Electrothermal GaN HEMT Model Applied to High-Efficiency Power Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 444–454, 2013.
- [53] O. Hammi and F. M. Ghannouchi, "Comparative study of recent advances in power amplification devices and circuits for wireless communication infrastructure," in *ICECS 2009*, pp. 379–382, IEEE, 2009.
- [54] E. Arnold, M. Golio, M. Miller, and B. Beckwith, "Direct extraction of GaAs MESFET intrinsic element and parasitic inductance values," in *IEEE International Digest on Microwave Symposium*, pp. 359–362, IEEE, 1990.
- [55] M. Berroth and R. Bosch, "High-frequency equivalent circuit of GaAs FETs for large-signal applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 2, pp. 224–229, 1991.
- [56] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the fet small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.
- [57] L. Eastman and U. Mishra, "The toughest transistor yet [gan transistor]?" *IEEE Spectrum*, vol. 39, no. 5, pp. 28–33, 2002.
- [58] R. Lossy, N. Chaturvedi, P. Heymann, J. Wrfl, S. Mller, and K. Khler, "Large Area AlGaIn/GaN HEMTs Grown on Insulating Silicon Carbide Substrates," *physica status solidi (a)*, vol. 194, no. 2, pp. 460–463, 2002.

- [59] J. R. Shealy, V. Kaper, V. Tilak, T. Prunty, J. A. Smart, B. Green, and L. F. Eastman, "An algan/gan high-electron-mobility transistor with an aln sub-buffer layer," *Journal of Physics: Condensed Matter*, vol. 14, no. 13, p. 3499, 2002.
- [60] H. Kang, Q. Wang, H. Xiao, C. Wang, L. Jiang, C. Feng, H. Chen, H. Yin, S. Qu, E. Peng, J. Gong, X. Wang, B. Li, Z. Wang, and X. Hou, "Effects of a GaN cap layer on the reliability of AlGa<sub>N</sub>/Ga<sub>N</sub> Schottky diodes," *physica status solidi (a)*, vol. 212, no. 5, pp. 1158–1161, 2015.
- [61] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, 2000.
- [62] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, "A new and reliable direct parasitic extraction method for MESFETs and HEMTs," in *23rd European Microwave Conference, 1993*, pp. 451–453, IEEE, 1993.
- [63] F. Lenk, *Monolithische GaAs FET- und HBT-Oszillatoren mit verbesserter Transistormodellierung: Zugl.: Berlin, Techn. Univ., Diss., 2003*, vol. 2 of *Innovationen mit Mikrowellen & Licht*. Göttingen: Cuvillier, 1. Aufl. ed., 2004.
- [64] P. M. White and R. M. Healy, "Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from "Cold FET" measurements," *IEEE Microwave and Guided Wave Letters*, vol. 3, no. 12, pp. 453–454, 1993.
- [65] R. B. Marks, "On-wafer millimeter-wave Characterization," in *GAAS 98 Amsterdam Conf. Dig.*, pp. 21–26, 1998.
- [66] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 160–169, 1987.
- [67] W. R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 12, pp. 1383–1394, 1985.

- [68] Scilab 5.4.1, Scilab Enterprises/ESI company, 101 Rue des Solets, 94150 Rungis Complexe, France.
- [69] D. E. Root and B. Hughes, "Principles of Nonlinear Active Device Modeling for Circuit Simulation," in *52nd ARFTG Conference digest*, (Cupertino CA), pp. 1–24, Automatic RF Techniques Group, 1998.
- [70] A. D. Snider, "Charge conservation and the transcapacitance element: An exposition," *IEEE Transactions on Education*, vol. 38, no. 4, pp. 376–379, 1995.
- [71] Angelov (Chalmers) Nonlinear GaAsFET Model Documentation in Advanced Design System (ADS), Keysight Technologies, Inc., Santa Rosa, United States, 2015.
- [72] M. Rocchi, "Status of the surface and bulk parasitic effects limiting the performances of GaAs IC's," *Physica B+C*, vol. 129, no. 1-3, pp. 119–138, 1985.
- [73] M. A. Khan, J. N. Kuznia, M. S. Shur, and Q. C. Chen, "Current/voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias," *Electronics Letters*, vol. 30, no. 25, pp. 2175–2176, 1994.
- [74] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," *Superlattices and Microstructures*, vol. 34, no. 1-2, pp. 33–53, 2003.
- [75] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6414–6419, 2004.
- [76] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review*, vol. 87, no. 5, pp. 835–842, 1952.
- [77] J. E. Sitch and P. N. Robson, "The performance of GaAs field-effect transistors as microwave mixers," *Proceedings of the IEEE*, vol. 61, no. 3, pp. 399–400, 1973.

- [78] T. Itoh and H. Yanai, "Stability of performance and interfacial problems in GaAs MESFET's," *IEEE Transactions on Electron Devices*, vol. 27, no. 6, pp. 1037–1045, 1980.
- [79] N. Scheinberg, R. Bayruns, and R. Goyal, "A low-frequency GaAs MESFET circuit model," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 2, pp. 605–608, 1988.
- [80] T. Mimura, "The early history of the high electron mobility transistor (HEMT)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 780–782, 2002.
- [81] O. Jardel, "Contribution à la modélisation des transistors pour l'amplification de puissance aux fréquences microondes : développement d'un nouveau modèle électrothermique de HEMT AlGa<sub>N</sub>/Ga<sub>N</sub> incluant les effets de pièges," *Ph. D. dissertation, Université de Limoges, FRANCE*, 2008.
- [82] C. Camacho-Peñalosa and C. S. Aitchison, "Modelling frequency dependence of output impedance of a microwave MESFET at low frequencies," *Electronics Letters*, vol. 21, no. 12, pp. 528–529, 1985.
- [83] P. Luo, O. Bengtsson, and M. Rudolph, "Reliable GaN HEMT modeling based on Chalmers model and pulsed S-parameter measurements," in *2016 German Microwave Conference (GeMiC)*, pp. 441–444, 2016.
- [84] F. de Groote, J.-P. Teyssier, T. Gasseling, O. Jardel, and J. Verspecht, "Introduction to measurements for power transistor characterization," *IEEE Microwave Magazine*, vol. 9, no. 3, pp. 70–85, 2008.
- [85] P. McGovern, J. Benedikt, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, "Analysis of DC-RF dispersion in AlGa<sub>N</sub>/Ga<sub>N</sub> HFET's using pulsed I-V and time-domain waveform measurements," in *2005 IEEE MTT-S International Microwave Symposium*, (Piscataway, NJ), pp. 503–506, IEEE, 2005.
- [86] A. Santarelli, R. Cignani, G. P. Gibiino, D. Niessen, P. A. Traverso, C. Florian, C. Lanzieri, A. Nanni, D. Schreurs, and F. Filicori, "Nonlinear charge trapping effects on pulsed I/V characteristics of GaN FETs," in *2013 European Microwave Integrated Circuit Conference*, pp. 1375–1378, 2013.

- [87] Y. P. Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*, vol. 34, no. 1, pp. 149–154, 1967.
- [88] C. P. Baylis and L. P. Dunleavy, "Understanding pulsed IV measurement waveforms," in *11th international symposium on electron devices for microwave and optoelectronic applications*, pp. 223–228, IEEE, 2003.
- [89] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear Transistor Model Parameter Extraction Techniques*. New York: Cambridge University Press, pp. 224–228, 2011.
- [90] A. Santarelli, R. Cignani, G. P. Gibiino, D. Niessen, P. A. Traverso, C. Florian, D. M. M.-P. Schreurs, and F. Filicori, "A Double-Pulse Technique for the Dynamic I/V Characterization of GaN FETs," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 2, pp. 132–134, 2014.
- [91] A. Santarelli, D. Niessen, R. Cignani, G. P. Gibiino, P. A. Traverso, C. Florian, D. M. M.-P. Schreurs, and F. Filicori, "GaN FET Nonlinear Modeling Based on Double Pulse Characteristics," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3262–3273, 2014.
- [92] B. Mallet-Guy, Z. Ouarch, M. Prigent, R. Quéré, and J. Obregon, "Direct extraction of a distributed nonlinear FET model from pulsed I-V/pulsed S-parameter measurements," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 2, pp. 102–104, 1998.
- [93] Advanced Design System (ADS), Keysight Technologies, Inc., Santa Rosa, CA, United States, 2015.
- [94] J. Scott, J. G. Rathmell, A. Parker, and M. Sayed, "Pulsed device measurements and applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2718–2723, 1996.
- [95] C. Charbonniaud, S. Meyer, R. Quéré, and J. P. Teyssier, "Electrothermal and trapping effects characterisation of AlGaIn/GaN HEMTs," in *11th GAAS Symposium*, (Munich), pp. 201–204, 2003.

- [96] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear Transistor Model Parameter Extraction Techniques*. New York: Cambridge University Press, pp. 223–224, 2011.
- [97] A. Jarndal, A. Z. Markos, and G. Kompa, “Improved Modeling of GaN HEMTs on Si Substrate for Design of RF Power Amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 3, pp. 644–651, 2011.
- [98] A. Raffo, A. Santarelli, P. A. Traverso, M. Pagani, G. Vannini, and F. Filicori, “Accurate modeling of electron device I/V characteristics through a simplified large-signal measurement setup,” *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 15, no. 5, pp. 441–452, 2005.
- [99] A. Raffo, V. Vadalà, P. A. Traverso, A. Santarelli, G. Vannini, and F. Filicori, “An innovative two-source large-signal measurement system for the characterization of low-frequency dispersive effects in FETs,” in *Proc. 16th Int. Meas. Confederation TC4 Symp.*, 2008.
- [100] A. Benvegna, O. Jardel, S. Laurent, D. Barataud, M. Meneghini, E. Zanoni, and R. Quéré, “Non-linear electro-thermal AlGaIn/GaN model including large-signal dynamic thermal-trapping effects,” in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1–4, IEEE, 2016.
- [101] G. Kompa and M. Novotny, “Frequency-dependent measurement error analysis and refined fet model parameter extraction including bias-dependent series resistors,” *IEEE Workshop on Experimentally Based FET Device Modeling and Related Nonlinear Circuit Design*, pp. 6.1–6.16, July 1997.

## Publications

### Journal

- (1) **P. Luo**, F. Schnieder, O. Bengtsson, V. Vadalá, A. Raffo, W. Heinrich, and M. Rudolph, “A Streamlined Drain-Lag Model for GaN HEMTs based on Chalmers Model,” submitted to *IEEE Transactions on Microwave Theory and Techniques*.

### Conferences

- (1) **P. Luo**, O. Bengtsson, and M. Rudolph, “Reliable GaN HEMT modeling based on Chalmers model and pulsed S-parameter measurements,” in *2016 German Microwave Conference (GeMiC)*, pp. 441–444, 2016.
- (2) **P. Luo**, O. Bengtsson, and M. Rudolph, “Novel Approach to Trapping Effect modeling based on Chalmers Model and Pulsed S-parameter Measurements,” in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 157–160, 2016.
- (3) **P. Luo**, O. Bengtsson, and M. Rudolph, “A drain lag model for GaN HEMT based on Chalmers model and pulsed S-parameter measurements,” in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 240–243, IEEE, 2017.
- (4) **P. Luo**, F. Schnieder, and M. Rudolph, “Chalmers GaN HEMT Charge Model Revisited,” accepted to *2018 German Microwave Conference (GeMiC)*, 2018.
- (5) **P. Luo**, F. Schnieder, O. Bengtsson, W. Heinrich, and M. Rudolph, “Modeling the Virtual Gate Voltage in Dispersive GaN HEMTs,” accepted to *2018 IEEE MTT-S International Microwave Symposium (IMS)*, 2018.

### Workshop

- (1) **P. Luo**, O. Bengtsson, and M. Rudolph, “GaN HEMT modeling based on pulsed S-parameter measurements,” in *Industry-Academia Workshop on GaN Technology*, Technion - Israel Institute of Technology, 09. Aug. 2016.