

**Material Science for high performance SiGe HBTs:  
Solid-Phase Epitaxy and III-V/SiGe hybrid approaches**

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## **Dedication**

I dedicate this dissertation to my beloved son, Lio Maximilian, heralding one new exciting chapter of my life.



## Abstract

After the age of microelectronics was launched in Bell Labs by Bardeen and Brattain on 23<sup>rd</sup> December 1947, the constant miniaturization of silicon (Si) transistors and circuits up to today led to a unique success story. At its peak are now standing small, fast and reliable multifunctional device systems, which accompany and simplify a great part of our everyday life. However, the complexity of today's microelectronic circuitry is not only driven by complementary metal oxide semiconductor (CMOS) scaling, but also by integration of high performance modules for various applications. One example is given by mixed signal circuitries for wireless and broadband communication systems. These mixed signal circuitries are build up by combining digital CMOS technology with analog silicon-germanium-carbon (SiGe:C) hetero-bipolar transistors (HBT) known as SiGe:C BiCMOS technology. State-of-the-art SiGe:C BiCMOS technologies achieve up to the 500 GHz today. Nevertheless, Si as semiconductor material is approaching more and more its physical limits, whereby novel approaches have to be found to ensure the future development of SiGe:C HBT BiCMOS technology in order to push the maximum frequency further into the Terahertz regime. Based on this task, two novel material science strategies are investigated in this Ph.D. thesis in terms of material growth and defect studies:

**A.) Solid-phase epitaxy (SPE) for emitter and base resistivity:** This technique has been investigated for local engineering of crystallinity in emitter and base layer of already established SiGe:C HBT device technology in order to improve the speed performance. By introducing disilane as new gas source with respect to standard used silane, it is possible to reduce the chemical vapor deposition growth temperature for Si, enabling in turn a differential growth of epitaxial-Si (epi-Si) on Si and amorphous Si (a-Si) on the silicon dioxide (SiO<sub>2</sub>) and silicon nitride (Si<sub>3</sub>N<sub>4</sub>) masks. The so produced requirement for SPE treatments is evaluated for two possible areas of application: **A1.) Emitter region** and **A2.) Base region**. In both cases, SPE techniques are applied to change the standard polycrystalline-Si (poly-Si) emitter and base link area on the SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> masks to a fully epi-Si area in order to lower emitter and base resistivity, respectively.

**B.) III-V/SiGe hybrid device:** The ternary compound semiconductor Indium gallium phosphide (In<sub>1-x</sub>Ga<sub>x</sub>P [ $x = 0 - 1$ ]) is introduced as potential new collector material as part of an advanced III-V/SiGe hybrid HBT device. With InP having a three times higher saturation velocity than Si, and GaP having a two times bigger bandgap than Si, this approach offers the possibility to adjust speed and power performance of HBTs in a flexible way as a function of the In<sub>1-x</sub>Ga<sub>x</sub>P collector chemical composition  $x$ .

The material growth and defect studies in this Ph.D. thesis produced insights, which lead to the following results for future device application:

**A1.) SPE for emitter region:** After investigating the temperature, time and doping concentration dependence on lateral SPE length of in-situ annealed As-doped epi-Si/a-Si test structures, it was possible to crystallize up to 500 nm of a-Si on SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> masks to epi-Si with low defect densities by a combination of 575 °C and 1000 °C postannealing.

**A2.) SPE for base region:** After studying the dependence of time, temperature, thickness, SiO<sub>2</sub>-capping and Ge incorporation on lateral SPE length of in-situ annealed undoped epi-Si/a-Si test structures, it was possible to crystallize up to 450 nm of SiO<sub>2</sub>-capped undoped a-Si on SiO<sub>2</sub> mask to low-defective epi-Si by 570 °C postannealing. Finally, this technique is applied in a SiGe:C base model structure in order to show the possibility to widen the monocrystalline region around the bipolar window, which results in a possibly improved base resistivity.

**B.) GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure:** For pseudomorphic GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure growth, the critical thickness of GaP on Si and maximum thermal budget for GaP deposition is evaluated. A detailed structure and defect characterization study by x-ray diffraction (XRD), atomic force microscopy (AFM), and transmission electron microscopy (TEM) is reported on single crystalline 170 nm GaP/20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure. Results show that 20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub> on Si(001) can be overgrown by 170 nm GaP without affecting the pseudomorphism of the Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) systems. The GaP layer grows however partially relaxed, mainly due to defect nucleation at the GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub> interface during initial island coalescence. The achievement of 2D GaP growth conditions on Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) systems is thus a crucial step for achieving fully pseudomorphic heterostructures. Anti-phase domain-free GaP growth is observed for film thicknesses beyond 70 nm. In addition, no detrimental impurity diffusion could be found in the GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure.

Finally, it is to mention that further investigation and efforts are still needed to push these new approaches to full integration into SiGe:C HBT BiCMOS technology concepts:

**A.) For SPE application:** Electrical studies are needed in frame of full processed devices to evaluate the value and required modifications for process integration.

**B.) For III-V/SiGe hybrid device:** Future work has to focus on improved 2D GaP layer conditions (before introducing InP) in order to prepare truly pseudomorphic GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructures with low defect densities. For this purpose, selective GaP growth studies in local HBT Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) mesa structures are the next step.



## Zusammenfassung

Nach Beginn der Mikroelektronik-Ära in den Bell Labs durch Bardeen und Brattain am 23. Dezember 1947 sorgte die Miniaturisierung von Si-Transistoren und Schaltungen bis heute für eine einzigartige Erfolgsgeschichte. Obenauf stehen nun kleine, schnelle und zuverlässige Multifunktionsbauteile, welche uns alltäglich begleiten und helfen. Allerdings macht die CMOS-Skalierung nicht ausschließlich die Komplexität heutiger mikroelektronischer Schaltungen aus, sondern wird ergänzt durch Integration von Hochleistungsmodulen für verschiedene Anwendungen. Als Beispiel kann man die Mischsignalschaltungen für drahtlose und Breitband-Kommunikationssysteme benennen, welche durch die Kombination von digitaler CMOS- mit analoger SiGe:C HBT-Technologie (auch bekannt als SiGe:C BiCMOS –Technologie) aufgebaut werden und heute bis zu 500 GHz erreichen. Da allerdings Si als Halbleitermaterial mehr und mehr an seine physikalischen Grenzen stößt, müssen neue Ansätze gefunden werden, um eine weitere Entwicklung der SiGe:C HBT BiCMOS-Technologie in Richtung Terahertz-Regime zu gewährleisten. Basierend auf dieser Aufgabe werden zwei neuartige Materialstrategien im Rahmen dieser Doktorarbeit in Form von Materialwachstums- und Defektstudien untersucht:

**A.) Festphasenepitaxie (SPE):** SPE gestattet das lokale Verändern der Kristallinität in Emitter- und Basisschichten von bereits etablierten SiGe:C HBT-Technologien, um deren Geschwindigkeit zu verbessern. Die Einführung des Prozessgases Disilan anstatt des sonst verwendeten Silan ermöglicht die Senkung der CVD-Wachstumstemperatur für Si, wodurch ein differentielles Wachstum von epi-Si auf Si und a-Si auf SiO<sub>2</sub>- und Si<sub>3</sub>N<sub>4</sub>-Masken erfolgt. Diese Voraussetzung zur SPE-Anwendung wird an zwei möglichen Anwendungsbereichen evaluiert: **A1.) Emitterbereich** und **A2.) Basisbereich**. In beiden Fällen wird die SPE angewendet, um die standardmäßigen poly-Si-Bereiche auf den SiO<sub>2</sub>- und Si<sub>3</sub>N<sub>4</sub>-Masken in epi-Si umzuwandeln, was zum Ziel hat, den Emitter- bzw. Basiswiderstand zu senken.

**B.) III-V/SiGe Hybridbauteil:** Der ternäre Verbindungshalbleiter In<sub>1-x</sub>Ga<sub>x</sub>P [x = 0 – 1] wird als potentielles neues Kollektormaterial im Rahmen eines III-V/SiGe Hybridansatzes eingeführt. Mit InP, welches eine dreimal höhere Sättigungsgeschwindigkeit als Si, und GaP, welches ein zweimal größere Bandlücke als Si hat, bietet dieser Ansatz die Möglichkeit, Geschwindigkeit und Leistung des HBTs flexibel als Funktion der chemischen Zusammensetzung x des In<sub>1-x</sub>Ga<sub>x</sub>P anzupassen. Die Materialwachstums- und Defektstudien in dieser Doktorarbeit erbrachten folgende Ergebnisse:

**A1.) SPE für den Emitterbereich:** Nach der Untersuchung der Temperatur-, Zeit- und Dotierungskonzentrationsabhängigkeit auf die laterale SPE-Länge von in-situ

getemperten, As-dotierten epi-Si/a-Si – Teststrukturen war es möglich, 500 nm a-Si auf den SiO<sub>2</sub>- und Si<sub>3</sub>N<sub>4</sub>-Masken zu epi-Si mit geringen Defektdichten zu kristallisieren, indem man eine Temperkombination aus 575 °C und 1000 °C verwendete.

**A2.) SPE für den Basisbereich:** Nach dem Studium der Zeit-, Temperatur-, Dicken-, SiO<sub>2</sub>-Bedeckungs- und Ge-Einlagerungsabhängigkeit auf die L-SPE-Länge von in-situ getemperten, nicht dotierten epi-Si/a-Si–Teststrukturen war es möglich, bis zu 450 nm des SiO<sub>2</sub>-bedeckten, undotierten a-Si auf der SiO<sub>2</sub>-Maske zu epi-Si mit geringen Defektdichten zu kristallisieren, indem man eine Temperung bei 570 °C verwendete. Abschließend wurde mittels einer SiGe:C Basis-Modellstruktur gezeigt, dass SPE die Möglichkeit bietet, den monokristallinen Bereich um das Bipolar-Fenster zu erweitern, was in einer möglichen Verbesserung des Basis-Widerstandes resultieren kann.

**B.) GaP/Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Hetero-Struktur:** Fürs pseudomorphe GaP/Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Hetero-Strukturwachstum wurde die kritische GaP-Schichtdicke auf Si und das maximale thermale Budget für die GaP-Beschichtung ermittelt. Eine einkristalline 170 nm GaP/20 nm Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Hetero-Struktur wird in Bezug auf Struktur und Defekte charakterisiert durch XRD, AFM und TEM. Die Ergebnisse zeigen, dass 20 nm Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) mit 170 nm GaP überwachsen werden kann, ohne den Pseudomorphismus des Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001)-Systems zu beeinflussen. Jedoch kommt es durch Zusammenwachsen der anfänglichen GaP-Inseln zu Defektnukleation an der GaP/Si<sub>0,8</sub>Ge<sub>0,2</sub>-Grenzschicht, wodurch GaP teilweise relaxiert aufwächst. Daher bildet das erfolgreiche 2D GaP-Wachstum auf Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001)-Systemen den entscheidenden Schritt, um eine völlig pseudomorphe Hetero-Struktur zu bilden. Des Weiteren konnte die Abwesenheit von Anti-Phasen-Domänen ab einer GaP-Schichtdicke von 70 nm und keine schädliche Diffusion innerhalb der GaP/Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Hetero-Struktur beobachtet werden.

Abschließend ist zu erwähnen, dass weitere Untersuchungen und Anstrengungen unternommen werden müssen, um diese neuen Ansätze zur Reife einer Integrationsvariante in der SiGe:C HBT BiCMOS-Technologie zu bringen:

**A.) Für SPE-Anwendungen:** Elektrische Studien in Rahmen eines voll prozessierten Bauteils werden benötigt, um den Wert für die Prozessintegration zu bewerten.

**B.) III-V/SiGe Hybridbauteil:** Zukünftige Arbeiten müssen sich (bevor man InP hinzufügt) auf die Verbesserung der 2D GaP-Schichtnukleation fokussieren, um eine wirklich pseudomorphe GaP/Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Hetero-Struktur mit geringen Defektdichten herzustellen. Hierzu sind selektive GaP-Wachstumsstudien in lokalen Si<sub>0,8</sub>Ge<sub>0,2</sub>/Si(001) Mesa-Strukturen der nächste Schritt.

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# **I. Introduction**

## **I.1. “More than Moore” vs. “More Moore” research**

This thesis was prepared at IHP, the Leibniz institute for innovative microelectronics in Frankfurt (Oder), Germany. IHP is an internationally recognized competence center for Silicon-Germanium (SiGe) technologies and performs research and development in the following fields: 1) Silicon (Si)-based systems, 2) Highest-frequency integrated circuits (IC), 3) Technologies for wireless and broadband communication, and 4) Materials for micro- and nanoelectronics.

These research programs are combined in a so called vertical approach; namely the four departments at IHP (Material, Technology, Circuit and System) collaborate and share their expertise within these research topics. The focus of research at the institute is oriented towards solutions relevant for the following applications [1]: 1) Telecommunications, 2) Semiconductor industries, 3) Automotive and aerospace industries, 4) Biotechnology and Telemedicine, and 5) Security and automation technologies.

The research pursues consequently a "More than Moore" strategy referring to the ITRS (International Technology Roadmap for Semiconductors) depicted in Fig. 1 [2]. According to this, IHP does not focus on challenges in miniaturization of Complementary metal oxide semiconductor (CMOS) technologies (known as “More Moore” approach) [3], but on research and development of technology modules for diversification of the existing CMOS technology platform, which considerably extend the functionality to create higher value systems (known as “More than Moore” approach) [4]. Some selected examples for module groups in focus of IHP’s “More than Moore”-strategy are listed in the following:

### **Radio frequency (RF):**

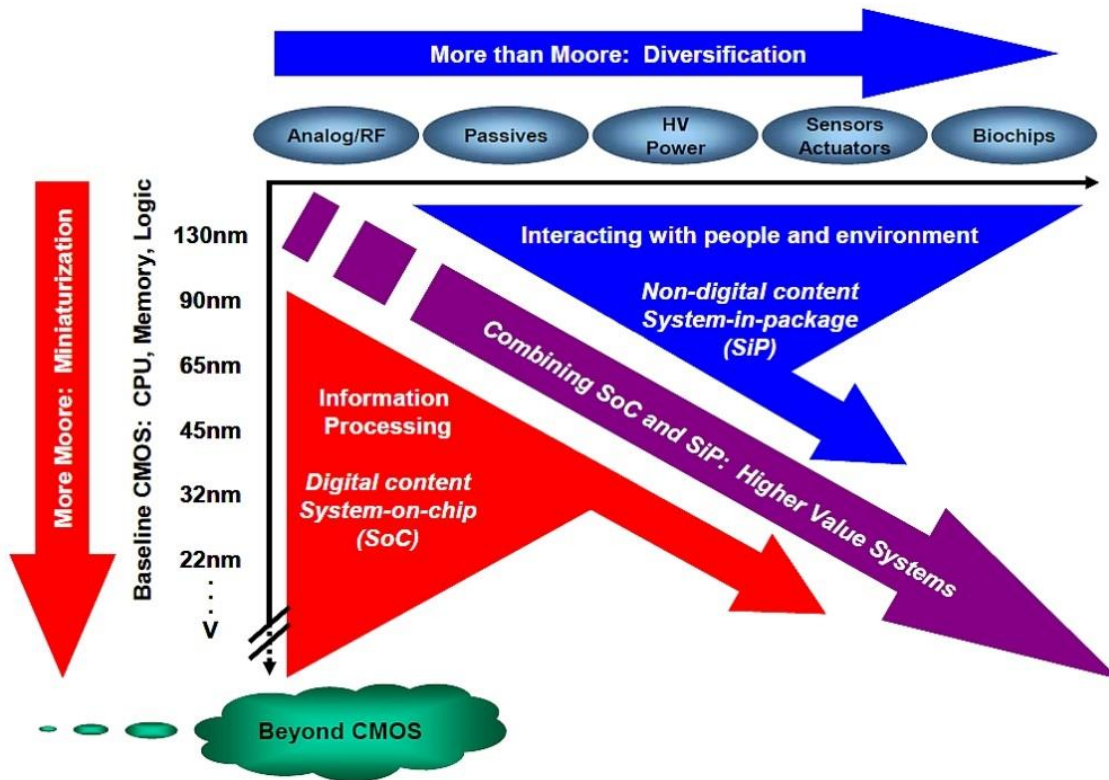
SiGe:C hetero-bipolar transistors (HBT) and Graphene base transistor (GBT) as well as Filters, Antennas, Modulators, Demodulators and RF Micro-electromechanical systems (MEMS) switches [5-11]

### **Photonics:**

Waveguides, Photodiodes, Modulators, Light-emitting diodes (LEDs) and Lasers [12-15]

### **Biomedical:**

Glucose sensors and Surface acoustic wave (SAW) filters [16, 17]



**Fig.1** The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the ITRS: miniaturization of the digital functions ("More Moore") and functional diversification ("More than Moore") [2].

## 1.2. Closing the THz gap

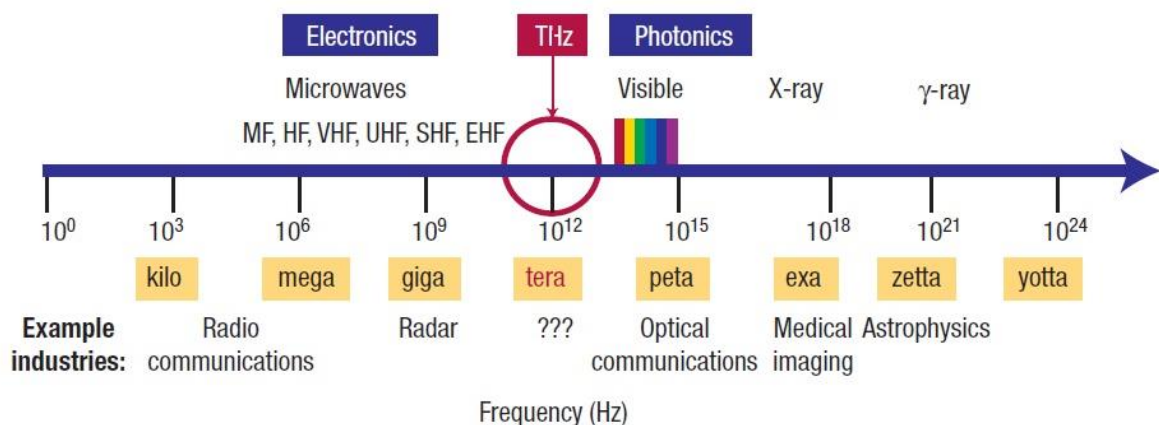
To follow the "More than Moore"-strategy, a monolithic integration approach is pursued at IHP: the integration of modules into  $0.25\ \mu\text{m}$  and  $0.13\ \mu\text{m}$  SiGe:C Bipolar CMOS (BiCMOS) base technologies [1]. This approach allows the combination of high frequency/high performance electronics with the functionality of integrated modules for system-on-chip applications [18]. It is to mention here that different methodologies and techniques exist to achieve full system integration. The two "schools" in microelectronic industry are:

**System-on-chip (SoC):** SoC is a system integration concept that seeks to create numerous system functions (i.e. processors, memory, etc.) by integrating the required active and passive components (i.e. antennas, filter, etc.) onto a single chip. In this way, SoC promises to achieve highest performance and most compact, lightweight systems for industrial mass-production. Nevertheless, challenges like long design times (due to

integration complexities) and high costs (due to integration of active but disparate devices) exist [19].

**System-in-package (SiP):** SiP is a system integration concept using advanced semiconductor packaging to integrate a number of system functions enclosed in a single package. It consists of two or more vertically stacked dies, which can contain several chips (i.e. processor, memories, etc.) combined with other components (i.e. passives, filters, etc.) and assembled on the same substrate. For interconnection of components and dices, fine wires connected to the package and standard off-chip wire bonds or solder bumps are used. SiP is typically applied in systems where space is limited (like mobile phones) or where a monolithic integration is not possible yet. This technique, based on the stacking of various chips, is very flexible and will thus be intensively pursued in future [19].

Following the SoC concept, new network architectures, distributed low resource middleware concepts, new energy-efficient protocols for media access as well as energy-efficient transceivers are investigated and realized at IHP with the goal to enable reliable wireless high-speed data transfer and sensor networks in the future [1]. With this motivation, SiGe:C BiCMOS base technology is constantly moving further towards higher frequencies, approaching step by step the Terahertz (THz) range (between 0.5 up to >1 THz) of the electromagnetic spectrum (Fig. 2) [6, 20-22].



**Fig.2** Sketch of the electromagnetic spectrum indicating the THz range [20].

It is noted that, in order to reach the THz range in the electromagnetic spectrum (red circle in Fig. 2), two different technology approaches are actively pursued in worldwide research and development:

Electronic technology approach: This approach tries to close the THz gap from the electronic side of the electromagnetic spectrum by frequency enhancement. Current technological examples in this field are: 1) HBT oscillators and amplifiers [23-25], 2) THz tunnel diodes [26-28], and 3) Schottky diodes [29-31].

Photonic technology approach: This approach tries to close the THz gap from the photonic side of the electromagnetic spectrum by frequency reduction. Current technological examples in this field are: 1) Optically Pumped THz Lasers [22, 32, 33], 2) Quantum Cascade Laser [22, 34, 35], and 3) Photomixing [22, 36, 37].

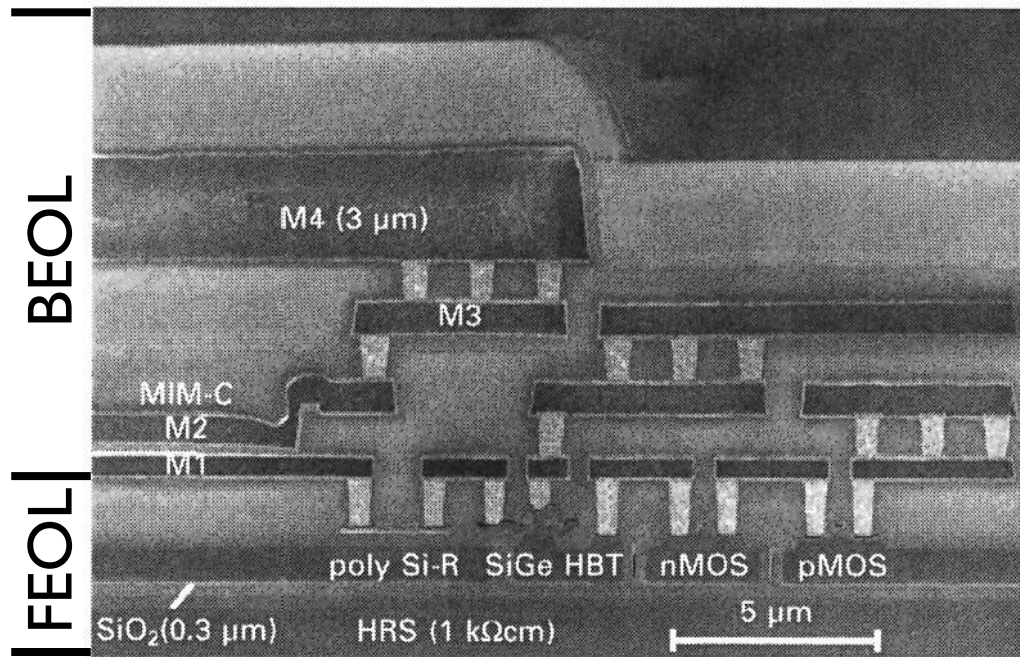
Along with the daunting microelectronic challenge of our twenty-first century - to fulfill the vision of faster and faster wireless broadband communication with more and more operation range supporting large information exchange between people or devices in a minimum of time on a global scale [18] – additional driving forces fueling THz-research exist. Inspiring applications with high impact on a variety of industries are currently discussed [20-22]: 1) Spectroscopic analysis of pharmaceutical products (e.g. composition studies), 2) Detection of explosives and illegal materials (e.g. scanners for airports), 3) Non-hazardous determination of disease (e.g. cancer), 4) Industrial-process monitoring (e.g. quality checks), and 5) Biomolecule detection (e.g. characteristic molecule fingerprints of proteins).

### **1.3 SiGe:C BiCMOS technology**

To meet the demand for wireless and broadband communication, both high-speed digital operation and high-frequency analog operation with sophisticated functions must be implemented simultaneously. From this point of view, the SiGe:C BiCMOS technology has developed from its first appearance in 1987 at IBM [18] today to one of the most promising and evolved concepts to fulfill this requirement. Figure 3 shows exemplary a SEM cross-section image of a typical integrated SiGe:C BiCMOS structure [38]:

**Front-end-of-line (FEOL):** FEOL labels in microelectronics the first part of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned on the Si wafer. FEOL generally covers everything up to (but not including) the deposition of the first metal interconnect layer (M1) [39]. In Figure 3 (from left to right), the polycrystalline (poly-) Si resistor (Si-R), the SiGe:C HBT and the CMOS (including n-channel Metal–oxide–semiconductor (nMOS) and p-channel Metal–oxide–Semiconductor (pMOS)) parts are shown on a 200 mm Silicon-on-Insulator (SOI) wafer, representing

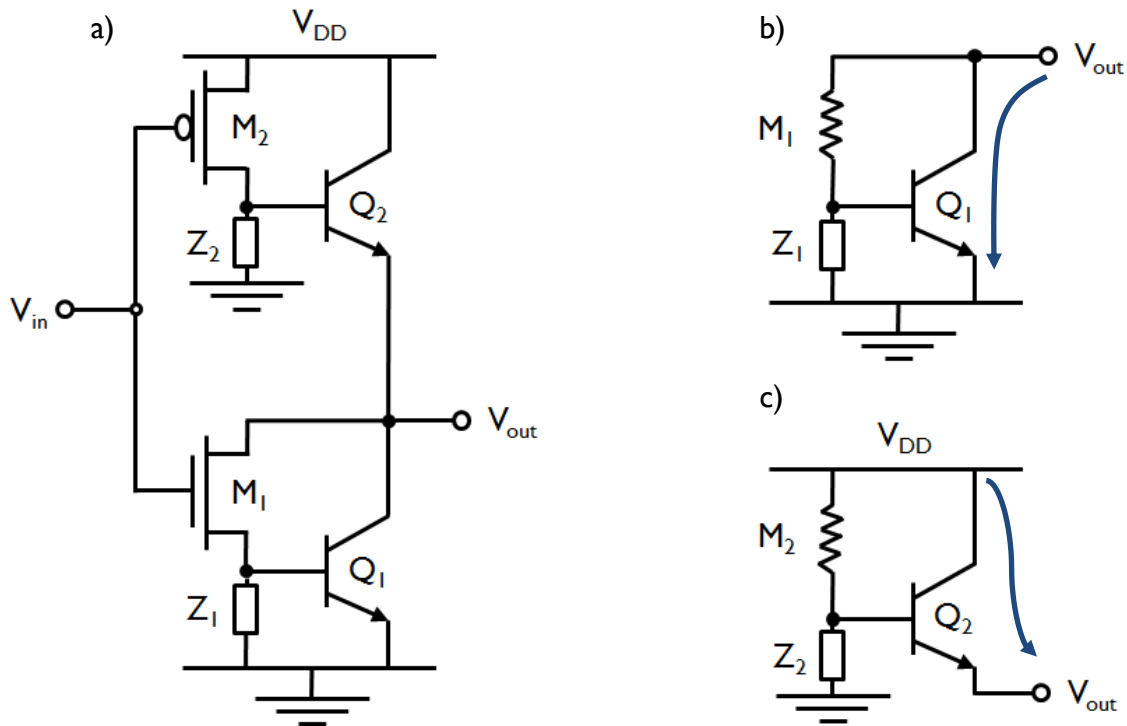




**Fig.3** Cross-sectional SEM image of 0.2  $\mu\text{m}$  self-aligned SiGe HBT, CMOS transistor and polycrystalline (poly-) Si resistor on 200 mm Silicon-on-Insulator (SOI)(1  $\mu\text{m}$ -thick Si on 0.3  $\mu\text{m}$ -thick insulator) wafers on high-resistivity substrate (HRS). Four-level metal (M1-M4) layer structure is used for interconnection [38].

a typical example of a possible FEOL architecture in BiCMOS technology. Device concepts are typically realized in FEOL whenever high quality crystalline material is needed to realize high performance devices (i.p. transistors). Drawback is that expensive Si chip area is consumed.

**Back-end-of-line (BEOL):** BEOL is the second part of IC fabrication where the individual devices of FEOL get interconnected with wiring on the Si wafer. BEOL generally begins when the first layer of metal (M1) is deposited on the wafer. It includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections [39]. In Figure 3, four-level metal (M1-M4) layer structures including a Metal-Insulator-Metal capacitor (MIM-C) representing as an example a possible BEOL setup in BiCMOS technology. Furthermore, BEOL integration of full functional modules (e.g. embedded memories, biosensors...) is of increasing interest to push the application of Si microelectronics to new fields. The benefit of BEOL integration is given by the fact that 3D integration does not consume expensive Si chip area. However, only amorphous or polycrystalline material can thus be realized and only a limited thermal budget can be applied.



**Fig.4** Sketch of a generic BiCMOS inverter (a) and equivalent circuit with high input signal  $V_{in}$  (b) and with a low input signal  $V_{in}$  (c) [41, 42].

Basically, the SiGe:C BiCMOS technology combines CMOS and SiGe:C HBT technology in a single IC on the same chip [40]. A generic BiCMOS inverter, which forms the basic circuit for the development of a generalized BiCMOS logic family, is shown in Figure 4(a). The circuit in Figure 4(a) consist of a nMOS and pMOS transistor ( $M_1$  and  $M_2$ ), two n-p-n-SiGe:C HBTs ( $Q_1$  and  $Q_2$ ) and two impedances operating as loads ( $Z_1$  and  $Z_2$ ). A first observation reveals that both the digital input and the logic operation are realized in CMOS technology. However, SiGe:C HBTs are used for the analog output signal. The functioning of the circuit is as follows:

- When input  $V_{in}$  is high (logic 1, i.e. +5 V (supply voltage  $V_{DD}$ )),  $M_2$  is off so that  $Q_2$  will be non-conducting (Fig. 4(b)). But  $M_1$  turns on and supplies current to the base of  $Q_1$  which conducts and acts as a current sink to the load between  $V_{out}$  and ground (GND) which discharges through it to 0 volts. The  $V_{out}$  falls to 0 volts (GND) plus the saturation voltage  $V_{CE,sat}$  between collector and emitter of  $Q_1$ . In conclusion, a high  $V_{in}$  has been translated to a low  $V_{out}$  [41, 42].
- In the opposite way, with input  $V_{in}$  is low (logic 0, i.e. 0 V (GND)),  $M_1$  is off which keeps  $Q_1$  non-conducting (Fig. 4(c)). However,  $M_2$  is on and supplies base current to  $Q_2$  which conducts and acts as a current source to charge the load between  $V_{out}$  and

GND towards +5 V ( $V_{DD}$ ). The output  $V_{out}$  goes to +5 V less the base to emitter voltage ( $V_{BE}$ ) drop of  $Q_2$ . In conclusion, a low  $V_{in}$  has been translated to a high  $V_{out}$  [41, 42].

In steady-state operation,  $Q_1$  and  $Q_2$  never turn on or off simultaneously, so that lower power consumption is guaranteed. This also results in a push-pull bipolar output stage. The transistors  $M_1$  and  $M_2$ , on the other hand, work furthermore as a phase-splitter, which creates higher input impedance. The impedances  $Z_1$  and  $Z_2$  are used to bias the base-emitter junction of the bipolar transistor and to ensure that base charge is removed when the transistors turn off. For practical designs, the use of resistive elements, shown in Figures 4, are very disadvantageous due to their size. Because of this, slightly modified BiCMOS circuits are normally used where the passive impedances ( $Z_1$  and  $Z_2$ ) are replaced by active impedances (e.g. nMOS transistors) or by a resistor in combination with only one impedance [41, 42].

Due to the intersection of CMOS and SiGe:C HBT technology, the emerged SiGe:C BiCMOS technology gains benefits from both transistor technologies [38, 40, 41]:

Advantages contributed by CMOS: 1) Low-power consumption, 2) Low-power dissipation, 3) Low noise margins, 4) High packing density, and 5) Integration of large complex functions with high yields.

Advantages contributed by SiGe:C HBT: 1) High switching speed at large values of capacitive loads, 2) High current drive per unit area, 3) Good noise performance, 4) High analog output capability, and 5) High input/output speed.

Despite of all these remarkable benefits in SiGe:C BiCMOS technology, there are still disadvantages arising especially from [40, 41]: 1) Speed degradation in the low voltage region, and 2) High production costs due to added process complexity.

Nevertheless, it is difficult (or almost impossible) to meet all above listed performance criteria and to satisfy all market requirements in the same time by one SiGe:C BiCMOS technology. Despite the constantly accompanied trade-off between high-performance versus cost-performance [18], there is not only one BiCMOS process which can address all applications. Each application requires different CMOS/SiGe:C HBT integration concepts to achieve an effective functionality, as described by *N. Stogdale and P. Hunt* in detail [41, 43]:

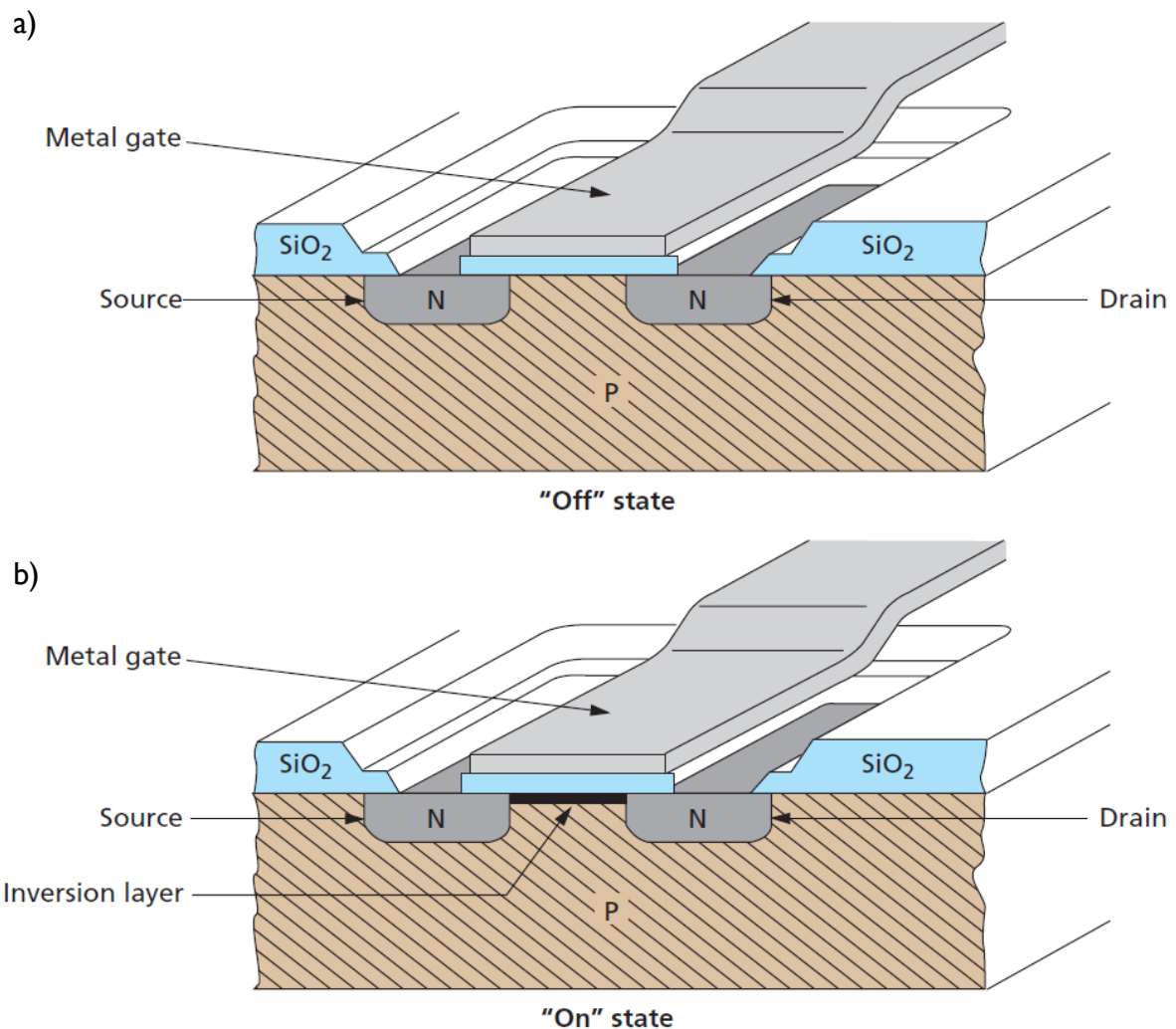
- Good current drive capability: for application to bipolar buffered BiCMOS gates and output stages:
  - Good current drive capability – low collector series resistance, buried layers.
- Good performance in analog applications:
  - High precision analog components, resistors, capacitors, etc.
  - Well controlled device characteristics: Gain, Early voltage, Noise, etc.
  - Tight control of parameters with temperature and operating current.
  - Operating Voltage < 5V.
  - High dynamic range.
- High-speed performance: For applications in Emitter-coupled logic (ECL) bipolar transistors are specifically optimized for low power high speed performance:
  - Very low gate delays and low power delay product.
  - Minimized parasitic resistances and capacitances.
  - Highly advanced processing techniques for minimization of feature sizes.
  - Highly optimized emitter base structure with low transit time.
- Good performance in power switching, smart power applications etc.:
  - Low series resistances; low sensitivity buried layers.
  - High junction breakdown voltage characteristics.
  - Good performance at high currents.

In conclusion, the BiCMOS technology is fundamentally linked to the two device concepts of CMOS and SiGe:C HBT. To gain a full understanding of BiCMOS technology, it is therefore necessary to know the individual transistor physics concepts and their unique characteristics. For this reason, these topics are briefly discussed in the following subsections.

### **1.3.1 CMOS Device Physics**

Looking at history, the basic idea to use a field-effect transistor (FET) as a solid-state amplifier, dates back to Julius Edgar Lilienfeld in 1925 and to Oskar Heil in 1934, who first patented separately from each other the similar FET device. Considering today's overwhelming dominance of CMOS technology in the electronics industry, it occurs somehow ironically, that the practical demonstration of the Bipolar-junction transistor (BJT)

in 1951 preceded that of the metal-oxide-semiconductor field-effect transistor (MOSFET) in 1960 by nine years. The reason for this slow development of a functional FET was due to the large problems in obtaining decent dielectric materials in the Si system. Despite Si has a huge natural advantage in comparison to other semiconductors in this respect, namely to form a very stable oxide, clean-room techniques had to mature to deal with ionic contamination, deionized water, fixed oxide charge and surface state passivation. When in the 1950's high-quality  $\text{SiO}_2$  could be produced on an industrial level and raised as a robust gate dielectric, the MOSFET was presented soon in 1960. Finally, the connection between pMOS and nMOS created in 1963 the famous CMOS, which paved the way to the high-volume, low-power, low-cost, highly integrated microprocessor and the enormous variety of computational engines that exist today [18, 44, 45].



**Fig.5** Sketch of a typical n-channel Si MOSFET in the "off"- (a) and "on"-state (b) [44].

CMOS technology consists of both nMOS and pMOS devices, which belong as MOSFETs to the group of FETs. The FET is a unipolar transistor device, which applies an electric field to control the shape and therefore also the conductivity of a channel of only one type of charge carrier (electrons (n) or holes (p)) in a semiconductor material. Figure 5 shows for instance a typical Si nMOS in the “off”- (a) and “on”-state (b). The base structure of the Si MOSFET consist of two isolated pn-junctions in a Si surface, overlaid first with a thin SiO<sub>2</sub> insulator and then with a conducting metal layer (gate). Most of the FETs are four-terminal electronic devices (one exception is e.g. the Junction-FET (JFET)). The three terminals, called source, drain and gate correspond figuratively to the emitter, collector and base of BJT. The fourth terminal, called the body (or also base, bulk or substrate), is used to bias the transistor into operation. For better I<sub>ON</sub>/I<sub>OFF</sub> ratio, FETs are used in CMOS not in accumulation, but in the inversion regime (Fig. 5(b)). This means that, due to field effect by applying the right voltage polarity, an n-conducting inversion channel conducts the current between source and drain in a p-doped Si(001) substrate. To initiate the field effect, the gate is insulated from the active channel, what causes that no current flows over this terminal. The so created gate potential (or electric field) controls the conductivity of the charge carriers in the active channel and finally the drain current I<sub>D</sub> [44-46]. Therefore, I<sub>D</sub> indicates how fast the load of the circuit can be charged or discharged stating the conclusion that high speed performance in MOSFET technology relies on high I<sub>D</sub>. This figure of merit is given by equation [45]:

$$I_D = \frac{W_z}{L} \mu_n C_{ox} \left( V_G - V_T - \frac{F_{Nd} V_D}{2} \right) V_D \quad (1)$$

where  $W_z$  is the channel width,  $L$  is the channel length,  $\mu_n$  is the charge carrier mobility,  $C_{ox}$  is the insulator capacitance in inversion,  $V_G$  is the gate voltage,  $V_T$  is the threshold voltage,  $V_D$  is the drain voltage and  $F_{Nd}$  is a function of doping concentration and oxide thickness. Regarding these parameters in equation (1), different approaches can be considered to improve I<sub>D</sub>:

- **Higher voltage levels (V<sub>G</sub> and V<sub>D</sub>):**

The industrial need for low power devices for mobile technology [18, 47] and the increased electrical breakdown of highly scaled electronics [45, 46] make this approach less attractive for further MOSFET development.

- **Raise channel width  $W_z$ :**

The major industrial disadvantage in this approach is the accompanying higher cost of valuable chip area by increasing the channel width [18]. One promising way to counteract this problem are three-dimensional gate transistor approaches instead of traditional planar MOSFET technologies [45, 48].

- **Increase majority charge carrier mobility  $\mu_n$ :**

To achieve higher majority charge carrier mobilities, worldwide research and development is focusing now on promising approaches like strained Si- [49], SiGe channel-[50] and III/V channel-technology [51].

- **Transistor scaling to reduce channel length  $L$ :**

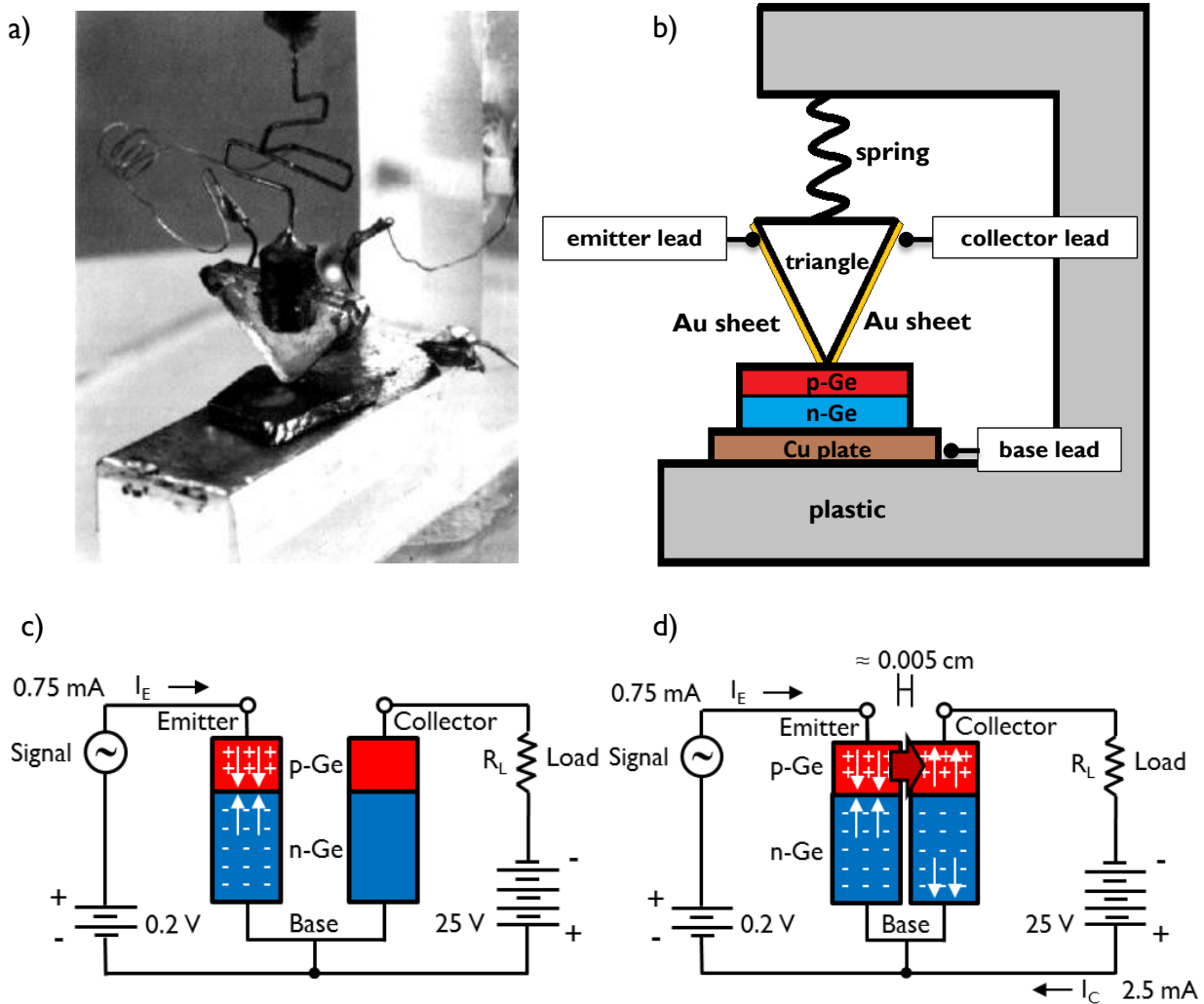
This miniaturization approach has been for a long time the primary mean in Si microelectronic industry (More Moore) [3, 18]. Nevertheless, it has to be kept in mind that scaling reduces transistor area  $A$  and therefore the gate oxide capacitance  $C_{ox}$  simultaneously [52]:

$$C_{ox} = \epsilon_r \epsilon_0 \frac{A}{d} \quad (2)$$

where  $\epsilon_r$  is the relative permittivity of the material and  $\epsilon_0$  is the vacuum permittivity. The long-established counteraction for this unfavourable fact was the constant reduction of insulator thickness  $d$ . Now, the scaling reaches their limits in form of high leakage currents [53]. Over the years, the introduction of high-k dielectric material as gate oxide has been found as an adequate method to control this issue [52, 54].

### 1.3.2 SiGe:C HBT Device Physics

**Point-contact transistor:** Looking at history, it is to mention that the first worldwide built transistor was the bipolar Point-contact transistor realized by Bardeen and Brattain in 1947. This earliest transistor was the precursor of the subsequently-developed BJT in 1951 and SiGe HBT in 1987 [18]. Figure 6 depicts this first bipolar electric device and its operation method [55]:



**Fig.6** Photograph (a) and sketch (b) of the first bipolar point-contact transistor invented by Bardeen and Brattain in Bell Labs 1947. Point-contact transistor circuits with broad (c) and short (d) distance between the two Ge pn-junctions [55-57].

This transistor construction (visible in Fig. 6(a)-(b)) consisted of a plastic triangle with a thin gold (Au) sheet attached to both side surfaces. The Au sheet was split in two pieces to create at the bottom a gap in between. The plastic triangle itself was pressed with a spring on a chunk of electron-rich Ge (n-Ge), which was the reason to call this device the Point-contact transistor. Finally, this used chunk of n-Ge was located on a copper (Cu) plate with a voltage source. As the Ge crystal with the Cu-plate forms the base of this point contact device, this electrode was named later on the base electrode contact. In that way, this device construction produced two electrically isolated Au contacts very close to each other on the surface of the n-Ge crystal. Since n-Ge crystal surfaces were rather defective back in these days, bulk electrons could be easily trapped by a large numbers of surface states, creating

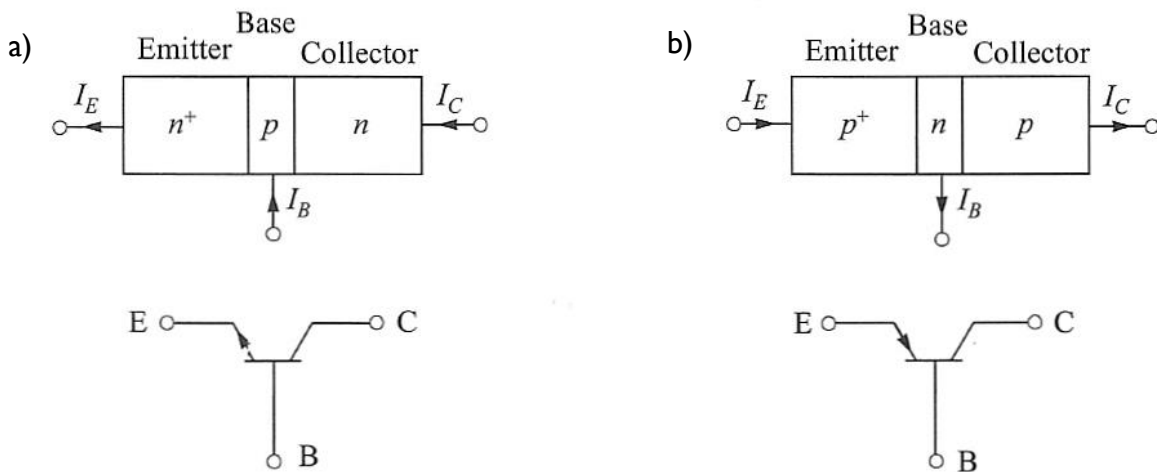


thus a thin p-type inversion layer (p-Ge) next to the surface of the n-Ge chunk. Figuratively spoken, the two Au electrodes contacted in this way two pn-junctions: One was named the emitter-base (EB) and the other was called the collector-base (CB) circuit (Fig. 6(c)). If now the distance between these two pn-junctions was large, these two circuits would act independently (Fig. 6(c)). During operation, the EB circuit was forward-biased with a small current (e.g. 0.75 mA) by applying a small positive potential (e.g. 0.2 V) at the emitter contact. Otherwise, the CB circuit was in the same time reversed-biased (i.e. no current flows) by applying a bigger positive potential (e.g. 25 V) between collector and base contact. However, since the two Au sheets were very close to each other (about 0.005 cm in the classical device), the two existing circuits influenced each other (Fig. 6(d)). In the forward-biased EB circuit, holes injected into p-Ge traveled partly over the adjacent p-type inversion layers into the p-Ge of the reversed-biased CB circuit. These additional positive charge carriers cause a reduction in the effective negative collector voltage and thus the band bending of the pn-junction there. In consequence, due to the bigger potential drop (e.g. 25 V) in the reversed-biased CB circuit, a bigger current (e.g. 2.5 mA) to flow. In other words, a small current (e.g. 0.75 mA) controls a bigger one (e.g. 2.5 mA). This amplification effect is the fundamental mechanism in bipolar transistor devices. For example, a small EB current from microphone can drive a light bulb in the CB circuit to follow the music [45, 46, 55-57].

**Hetero-bipolar transistor:** It is to mention that, Ge was used at first as semiconductor material of choice back in the days, due to the possibility to grow Ge crystals with high purity. Furthermore, due to the extraordinarily large diffusion length of minority carriers in Ge, it allowed to prepare functional devices despite the large device dimension in early days. Even though the first transistor was fabricated in Ge, Si emerged very fast as the dominant semiconductor material after having improved Si crystal growth methods and Si microstructure processing [18, 44]. Already in 1954, the first Si BJT was presented by Teal [18]. The first diffused Si BJT followed in 1956, and the first epitaxial grown Si BJT was finally reported in 1960 [58, 59]. Since 1987, there was a renaissance of Ge in form of the first functional SiGe HBT demonstrated by IBM [60]. These pioneering works opened the way to the further evolution of HBT devices: From the first SiGe HBT demonstrated using chemical vapor deposition (CVD) growth technique in 1989 [61], over the discovery in 1996 that incorporating small amounts of carbon (C) into a SiGe base epitaxial layer strongly retards the diffusion of the Boron (B) doping during subsequent thermal cycles [62],

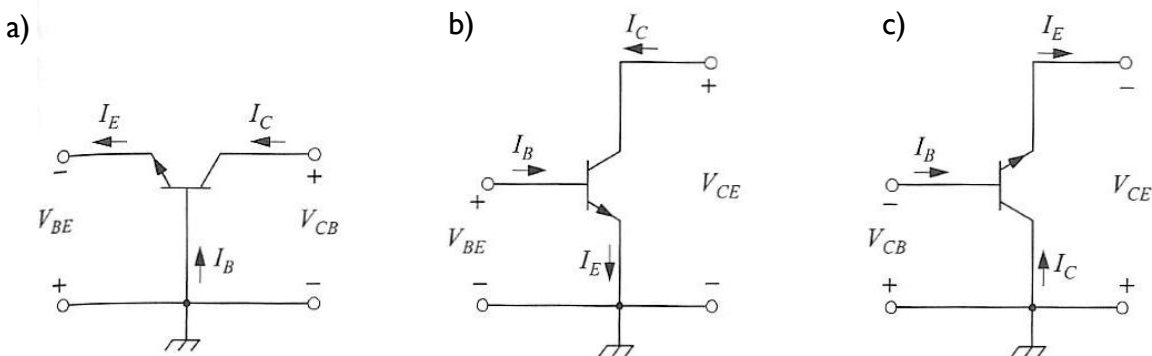
up to the first high-performance, fully integrated SiGe:C HBT technology reported in 1999 [63]. In the following, bipolar device physics is reviewed to set the basis for the approaches used in this thesis to improve HBT performance.

**Device Physics:** There are two kinds of bipolar devices conceivable: the n-p-n type which has a p-type base and n-type emitter and collector, and the p-n-p type which has an n-type base and p-type emitter and collector [45, 46]. Figure 7 depicts the symbols and nomenclatures for both bipolar transistor types:

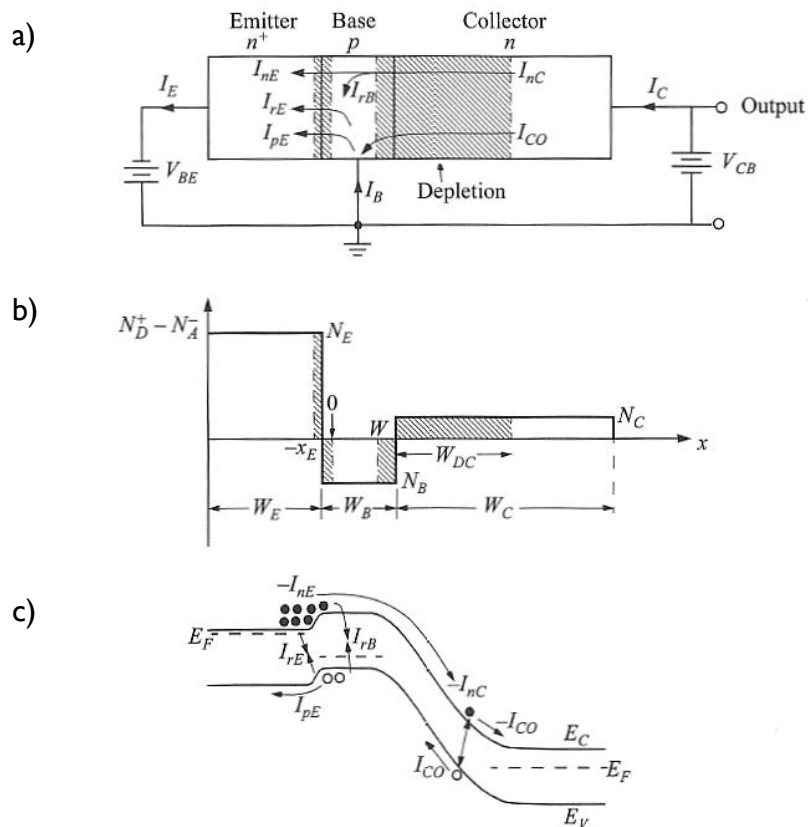


**Fig.7** Symbols and nomenclatures of **(a)** n-p-n transistor and **(b)** p-n-p transistor.  $I_E$ ,  $I_B$  and  $I_C$  are the emitter, base and collector current, respectively [45].

The arrows indicate the conventional technical direction of current flow under normal operation condition, i.e. a forward-biased EB junction and a reverse-biased CB junction. In this section, only the standard n-p-n type bipolar transistor will be considered here, because the vertical n-p-n type is predominantly used today in all high-speed digital circuits. The reason for this is given by the much higher charge carrier mobility of electrons in contrast to



**Fig.8** Three circuit configuration of n-p-n transistors in normal mode: **(a)** common-base, **(b)** common-emitter, and **(c)** common-collector [45].



**Fig.9** An n-p-n type HBT biased in the normal operating condition. **(a)** Concentration and biases in common-base configuration. **(b)** Doping profiles and critical dimensions with abrupt impurity distribution. **(c)** Energy-band diagram. Current components are shown in **(a)** and **(c)**. Note that in **(c)**, flow of electrons is negative current because of negative charge [45].

holes in Si-based materials [18, 45, 46]. Depending on which lead is common to input and output circuits, three circuit configurations are known to connect a bipolar transistor: common-base, common-emitter and common-collector configuration (visible in Fig. 8).

Figure 9 shows interrelated sketches of an n-p-n type bipolar transistor, displaying connection and biases in common-base configuration (a), doping profiles and critical dimensions with abrupt impurity distributions (b) and the band diagram (c) [45]. In order to define the three terminal currents  $I_E$ ,  $I_B$  and  $I_C$ , it is helpful to describe first the different current components existing in the normal operation condition:

Electron injection current from the emitter into the neutral base ( $I_{nE}$ ): Simply spoken, a bipolar transistor device consists of two interconnected pn-junctions, over which an electron current flows from the emitter through the base into the collector. Due to the electron transport over the p-type base, the BJT is also classified as a minority carrier

device. Based on this, one important diffusion electron current component is  $I_{nE}$  between  $x = 0$  and  $x = W$  (visible in Fig.9(a)-(b)). The other one, known as  $I_{nC}$ , consequently is the amount of electrons actually reaching the collector in the end. The ratio between  $I_{nE}$  and  $I_{nC}$  is called the base transport factor  $\alpha_T$ . It is defined as [45]:

$$\alpha_T = \frac{I_{nC}}{I_{nE}} \quad (3)$$

Assuming no current loss through recombination in the neutral base ( $I_{rB}$ ), it can be estimated that  $I_{nE} \approx I_{nC}$ , or  $\alpha_T \approx 1$ . In this case  $I_{nE}$  and  $I_{nC}$  can be defined as [45]:

$$I_{nE} \approx I_{nC} \approx \frac{2A_E D_n Q_B}{W^2} \quad (4)$$

where  $A_E$  is the cross-sectional area of the EB junction,  $D_n$  is the diffusion coefficient for electrons and  $W$  is the natural base thickness.  $Q_B$  is the injected excess charge in the base and defined as [45]:

$$Q_B = q \int_0^W [n_p(x) - n_{p0}] dx \approx \frac{qW n_{p0}}{2} e^{\frac{qV_{EB}}{kT}} \quad (5)$$

where  $q$  is unit electron charge,  $n_p$  is the electron concentration in p-type semiconductor (minority carriers), and  $n_{p0}$  is  $n_p$  in thermal equilibrium.

In Si bipolar transistor technique, there are two common ways known to improve  $\alpha_T$  towards unity in order to increase  $I_{nC}$  [18, 45, 46, 64]: 1) Replacing the uniform doping in the base layer by a graded one, and 2) Introducing Ge content with different profiles into the base layer.

Because of this, the electronic band structure in the base layer can be engineered so that an additional built-in electric field is created there, enhancing the electron transport by extra drift action [45, 46]. Because introducing Ge into the base changes the built-in drift field in the base more effectively than a graded doping profile and allows in addition to reduce the conduction band offset between emitter and base, this technique paved the way for the HBT success over the BJT. For reasons of clarity, these important aspects of HBTs will be discussed at the end of this section in more detail.

Hole injection current from the base into the emitter ( $I_{pE}$ ): In reality,  $\alpha_T$  is usually smaller than unity due to  $I_{rB}$ , and other current components (beside  $I_{nE}$  and  $I_{nC}$ ), which also have to be taken into account. One of this components is the hole diffusion current  $I_{pE}$ , which is the main component of  $I_B$ . Its equation follows the hole distribution and current of a regular pn-junction [45]:

$$I_{pE} = \frac{A_E D_{pE} p_{n0E}}{W_E} \left[ e^{\frac{qV_{EB}}{kT}} - 1 \right] \quad (6)$$

where  $D_{pE}$  is the diffusion coefficient for holes in the emitter,  $p_{n0E}$  is the hole concentration in n-type emitter (minority carriers) in thermal equilibrium, and  $W_E$  is the total emitter width. It is to note here that  $I_{pE}$  corresponds well to the I-V characteristic of a typical pn-junction and is very much determined by the parameters of the receiving side (in this case the emitter side).

Recombination current at EB junction ( $I_{rE}$ ): Another component for base current is the recombination current  $I_{rE}$ . This current is proportional to [45]:

$$I_{rE} \propto \frac{1}{\tau} e^{\frac{qV_{EB}}{m_f kT}} \quad (7)$$

where  $m_f$  is a fitting factor (usually close to two). The factor  $1/\tau$  is the effective minority-carrier lifetime in n-type emitter. This term combines the (in indirect semiconductor dominating) *Shockley-Read-Hall electron-hole generation-recombination process* and the *Auger recombination*, which occurs when holes are injected into an  $n^+$ -doped emitter and recombine there by transferring the energy to another free electron [45, 46].

Reverse current at CB junction ( $I_{c0}$ ): Finally, we consider the reverse  $I_{c0}$ , which is given by [45]:

$$I_{c0} \approx A_C q \left( \frac{D_{pC} p_{n0C}}{W_C - W_{DC}} + \frac{D_n n_{p0}}{W} \right) \quad (8)$$

where  $A_C$  is the CB cross-sectional area,  $D_{pC}$  is the diffusion coefficient for holes in the collector,  $p_{n0C}$  is the hole concentration in n-type collector (minority carriers) in thermal equilibrium,  $W_C$  is the total collector width, and  $W_{DC}$  is the depletion width of the collector side.

Current Gain: After consideration of all different current components, the three terminal currents  $I_E$ ,  $I_B$  and  $I_C$  can be formulated with the help of Fig. 9 and Kirchhoff's law (equation (9)) as follows [45]:

$$I_E = I_C + I_B \quad (9)$$

$$I_E = I_{nE} + I_{rE} + I_{pE} \quad (10)$$

$$I_B = I_{pE} + I_{rE} + (I_{nE} - I_{nC}) - I_{CO} \quad (11)$$

$$I_C = I_{nC} + I_{CO} \quad (12)$$

After determining the terms for all terminal currents, it is possible to introduce two more important parameters: The common-base current gain  $h_{FB}$  (or  $\alpha_0$ ) and the common-emitter current gain  $h_{FE}$  (or  $\beta_0$ ), which express the unique amplifying feature of bipolar transistors (remember the point contact transistor part). Both values are roughly given by [45, 46, 64]:

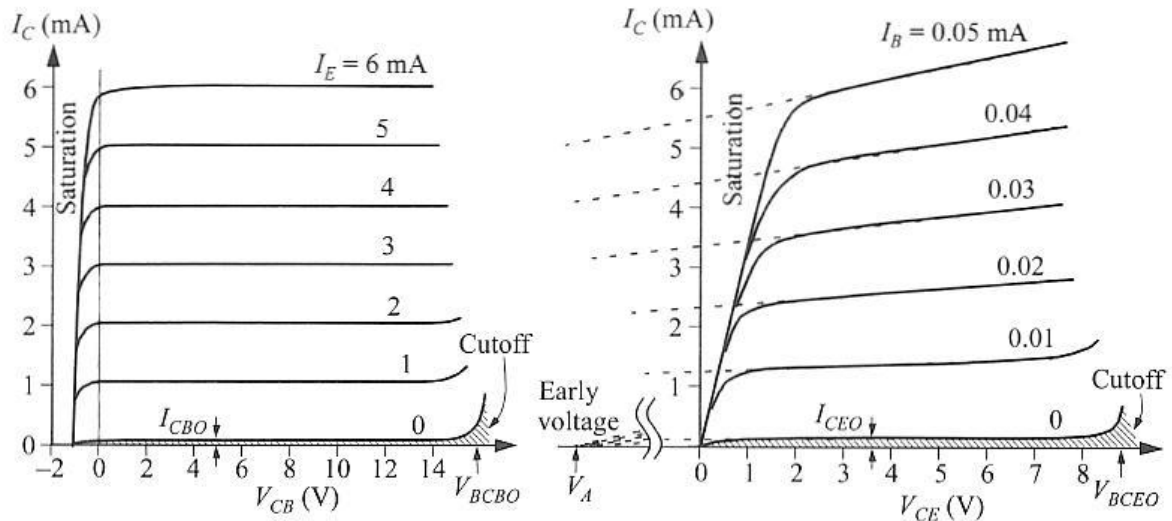
$$h_{FB} \equiv \alpha_0 \equiv \gamma \alpha_T = \frac{I_{nE} I_{nC}}{I_E I_{nE}} \approx \frac{I_C}{I_E} \quad (13)$$

$$h_{FE} \equiv \beta_0 \equiv \frac{\alpha_0}{1 - \alpha_0} \approx \frac{I_C}{I_B} \quad (14)$$

where  $\gamma$  is the emitter injection efficiency. Targeting in today's well-designed bipolar transistor a value of  $\alpha_0$  close to unity, values for  $\beta_0$  are much larger than one. For example if  $\alpha_0$  is 0.99,  $\beta_0$  is 99; and if  $\alpha_0$  is 0.998,  $\beta_0$  is 499 [45].

Output Characteristics: Next, we take a closer look on Fig. 10, which depict the I-V characteristics of an n-p-n bipolar transistor connected in two different circuit configurations:

First, we start with the idealized *common-base configuration* (see Fig. 8(a), Fig. 10(a)), where  $I_C$  is practically equal  $I_E$ , because  $\alpha_0$  is close to unity. Additionally,  $I_C$  does not change over a wide range of  $V_{CB}$  values (this means that all electrons from the emitter are effectively injected in the collector over wide  $V_{CB}$  range) and does not even vary down to zero volts for  $V_{CB}$ . This means that, even at zero volts for  $V_{CB}$  (but a finite  $V_{BE}$  value), excess electrons from the base are still extracted by the collector. For negative  $V_{CB}$ , the CB junction switches from reverse biased to forward biased, letting the bipolar transistor enter the saturation mode.



**Fig.10** Output characteristic of an n-p-n bipolar transistor in **(a)** common-base configuration, and **(b)** common-emitter configuration. Breakdown voltage and Early voltage  $V_A$  are indicated [45].

In this mode, the electron concentration at  $x = W$  (remember Fig. 9(b)) increases strongly up to a level at  $x = 0$ , reducing significantly the diffusion current through the neutral base and causing  $I_C$  to drop rapidly to zero. The collector saturation current  $I_{CB0}$  is measured with the emitter open-circuit, which means that the emitter junction is short-circuited ( $V_{BE} = 0$ ). In this state,  $I_E$  is zero that reduces the amount of electrons at  $x = 0$  and the electron gradient towards  $x = W$ . This is the reason why  $I_{CB0}$  is smaller than the ordinary reverse current of a pn-junction (whose value is given by equation (8)). As  $V_{CB}$  increases to the collector-base open-emitter breakdown voltage  $V_{BCB0}$  value,  $I_C$  starts to increase rapidly due to the avalanche breakdown of the CB junction. For a very narrow base width or a base with relatively low doping, the breakdown may also occur by the punch-through effect. This means that the neutral base width is reduced to zero and the collector depletion region is in direct contact with the emitter depletion region. At this point, the collector is effectively short-circuited to the emitter and a large current can flow [45, 46, 64].

Now, we consider the idealized *common-emitter configuration* (see Fig. 8(b), Fig. 10(b)). In this case, the voltage  $V_{CE}$  is divided between two junctions to give the EB junction a smaller forward bias, and the CB junction a larger reverse bias in normal operation mode. Due to large reversed biased CB junction, the excess electron density at  $x = W$  is very low. Otherwise at  $x = 0$ , the excess electron density reaches very large values due to (even small) forward biased EB junction. Because of the exponential dependence, even small changes in

$V_{BE}$  (or better  $I_B$ ) are enough to change the excess electron density at  $x = 0$  and subsequently increase/decrease  $I_C$  by a large value (corresponding to  $\beta_0$  above). Remarkably,  $I_C$  increases slightly by raising  $V_{CE}$ . This observable effect is called the *Early-Effect* and originated from the enlargement of CB depletion region with increasing  $V_{CE}$ . As the result, the neutral base width  $W$  decreases, causing on the one hand a lesser chance for recombination within the base and on the other hand an increased electron gradient across the base. Both factors results in both higher  $I_C$  and higher  $\beta_0$ , simultaneously. For a bipolar transistor with base width  $W_B$  much larger than the depletion region in the base, the Early voltage is given by [45, 46, 64]:

$$V_A \approx \frac{qD_n(W_B)n_i^2(W_B)W_B}{\epsilon_s} \int_0^{W_B} \frac{N_B(x)}{D_n(x)n_i^2(x)} dx \quad (15)$$

$$\approx \frac{qN_B W_B^2}{\epsilon_s}$$

for a uniform base (where  $\epsilon_s$  is the permittivity of the semiconductor and  $n_i$  the intrinsic carrier concentration). The Early voltage  $V_A$  can be determined by extrapolating to the point where the output curves meet (visible on the left in Fig. 10(b)). However, when  $V_{CE}$  is decreased below a certain value ( $\approx 1$  V for Si BJTs),  $I_C$  falls rapidly to zero. Similar to the common-base configuration, the CB junction will switch from reverse bias to forward bias and drive the bipolar transistor into saturation mode, if  $V_{CE}$  is further reduced. The collector saturation current  $I_{CE0}$  is measured with the base open-circuit, which is the  $I_C$  with zero base current. Here,  $I_{CE0}$  is much larger than  $I_{CB0}$ , because the open base physically floats to a slightly positive potential, increasing the electron concentration and its diffusion gradient in the base. Similar to the common-base configuration, an avalanche breakdown appears in the CB junction after reaching a certain high  $V_{CE}$  value ( $V_{BCE0}$ ). Interestingly,  $V_{BCE0}$  is much smaller than the junction breakdown voltage  $V_{BCB0}$ , due to the positive feedback from the bipolar gain [45].

High frequency properties: Next, we present shortly the main aspects of the microwave characteristics for bipolar transistors. One of the most important parameter is the transit cutoff frequency  $f_T$ . This parameter can be defined as the frequency at which  $\beta_0$  is unity. For any transistor using the equivalent circuit of Fig. 11(a),  $f_T$  can be described by the following expression [45]:

$$f_T = \frac{g_m}{2\pi C_{in}} \quad (16)$$



where  $g_m$  is the transconductance and  $C'_{in}$  the total input capacitance. In BJT (Fig. 11(b)-(c)), the components of  $C'_{in}$  are represented by the sum of [45]:

$$C'_{in} = C'_{par} + C'_{dn} + C'_{dp} + C'_{DE} + C'_{DC} + C'_{sc} \quad (17)$$

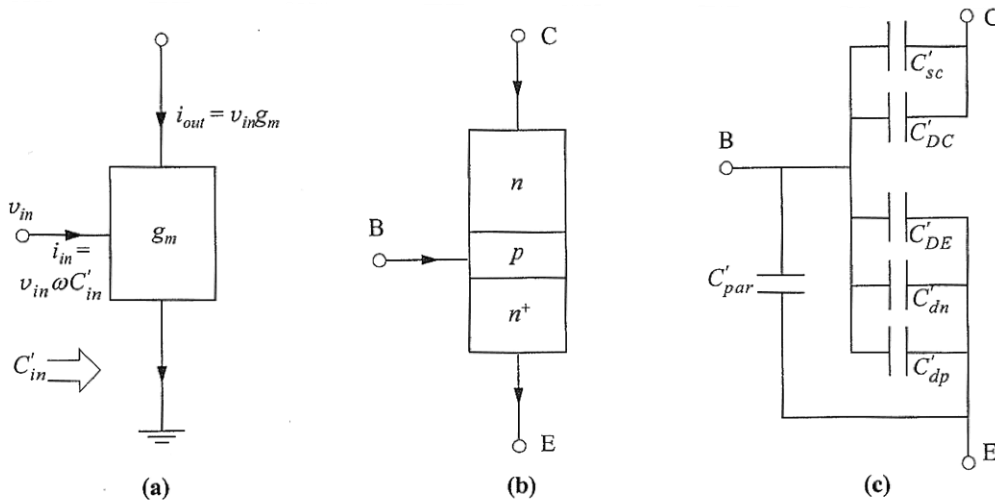
where  $C'_{par}$  is the parasitic capacitance,  $C'_{dn}$  is the diffusion capacitance due to electrons in the base,  $C'_{dp}$  is the diffusion capacitance due to holes into emitter,  $C'_{DE}$  is the emitter-base depletion capacitance,  $C'_{DC}$  is the collector-base depletion capacitance and  $C'_{sc}$  is the space-charge capacitance in the collector due to the injected electrons. Considering the transit time  $\tau$  as the individual charging time or delay time associated with each capacitance  $C'/g_m$ ,  $f_T$  can be rewritten as [45, 64]:

$$f_T = \frac{1}{2\pi \sum (C'/g_m)} = \frac{1}{2\pi \sum \tau} \quad (18)$$

revealing  $f_T$  as inverse of the sum of transit times which takes an electron to travel from the emitter to the collector contacts. Entering the equations for  $C'_{dn}$ ,  $C'_{dp}$  and  $C'_{sc}$  from the literature, the overall transit cutoff frequency can be finally defined as [45]:

$$f_T = \left\{ 2\pi \left[ \frac{kT(C'_{par} + C'_{DE} + C'_{DC})}{qI_C} + \frac{W^2}{\eta D_n} + \frac{W_E W}{\theta D_n} + \frac{W_{DC}}{2v_{sat}} + R_C C'_{DC} \right] \right\}^{-1} \quad (19)$$

where  $\eta$  and  $\theta$  are design parameters,  $W$  is the natural base width,  $W_E$  is the emitter width,  $W_{DC}$  is the collector-base space charge width,  $v_{sat}$  is the saturation velocity in  $W_{DC}$  and  $R_C$  is the total collector resistance [18, 46, 65].



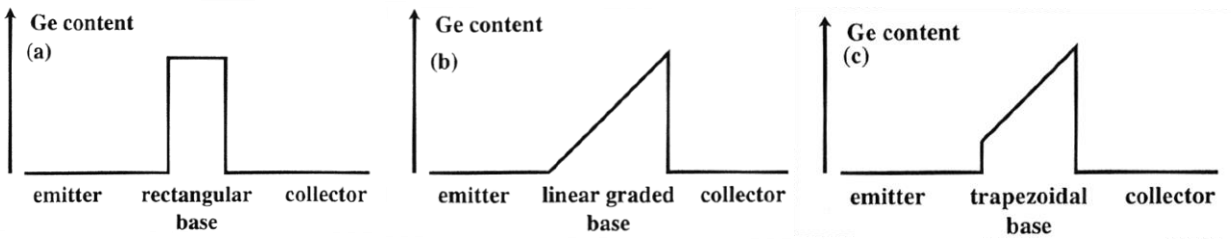
**Fig.11** Schematic circuits to analyse  $f_T$ : **(a)** A transistor having  $g_m$  and  $C'_{in}$ . **(b)** Representation of n-p-n HBT, and **(c)** its input capacitance components [45].

Another important figure-of-merit which characterizes the speed of the transistor is the maximum frequency of oscillation  $f_{max}$  and is defined as [45]:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C'_C}} \quad (20)$$

with  $R_B$  being the total base resistance and  $C'_C$  the total collector capacitance [64].

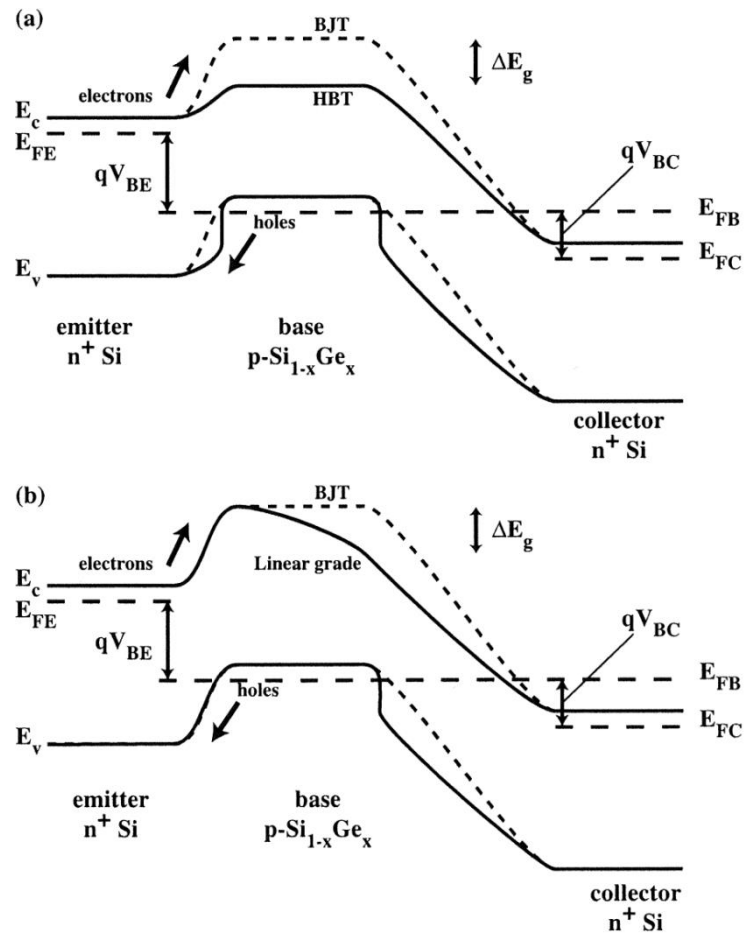
SiGe HBT versus Si BJT: Up to this point, the presented theoretical background corresponds to both BJT and HBT. To explain the historical success of the HBT over the BJT, we have finally to consider the effects of introducing Ge into the base layer, creating in this way a hetero-junction bipolar transistor device. In general, three main designs of adding Ge into the base of a HBT exist, as depicted in Fig. 12: The rectangular or box SiGe base (a), the linearly graded SiGe base (b) and the trapezoidal SiGe base (c), which is a compromise between the two designs named in advance [64]:



**Fig.12** The three main Ge base profiles for SiGe HBTs. **(a)** the rectangular or box SiGe base, **(b)** the linearly graded SiGe base and **(c)** the trapezoidal SiGe base [64].

Depending on the used Ge profiles, the main parameters of the HBT will be modified in different ways, creating individual benefits for the operation of the device. In Fig. 13, the band structure modifications of both rectangular (a) and the linearly graded (b) Ge profiles are shown [64]. The most obvious advancement by using a rectangular Ge base profile with respect to a standard BJT is the decrease in height of the conduction band in the base (see Fig 13(a)). This results in a reduced potential barrier at EB and CB junction, increasing  $I_C$ ,  $V_A$  and emitter transit time  $\tau_E$  by a factor  $e^{\frac{\Delta E_g}{k_B T}}$  [64]. Certainly,  $\Delta E_g$  depends on the Ge content  $x$ , and is given at low Ge content by [64]:

$$\Delta E_g = 0.0206x^2 - 0.43x [eV] \quad (21)$$



**Fig.13 (a)** The band structure for a Si BJT and a rectangular Ge base profile HBT. **(b)** The band structure for a Si BJT and a linearly Ge graded SiGe HBT [64].

Unlike the Ge rectangular profile HBT, the linearly graded Ge base profile (see Fig. 13(b)) introduces a slanting base conduction band, creating an additional built-in drift field that accelerates the electrons across the base, reducing the base transit time  $\tau_b$ , improving  $\alpha_T$  and increases the bipolar gains ( $\alpha_0$  and  $\beta_0$ ). To benefit from both lower base conduction band and the additional built-in electric drift field, modern SiGe:C HBTs often use a trapezoidal base profile, which is simply a compromise of the Ge rectangular profile and the linearly graded Ge base profile (see Fig. 12(c)). However, process engineers often trade off the enhanced  $\beta_0$  and  $I_C$  for higher base doping concentration  $N_B$ , which allows thinner  $W_B$  and reduced  $R_B$ . Thereby,  $\tau_b$  will be reduced, what increases again in turn  $f_T$  and  $f_{max}$  [64].

## I.4. Goals of this thesis

Today's high-speed SiGe:C HBT BiCMOS technology can be fabricated up to  $f_T/f_{max}$ /common-emitter breakdown voltage ( $V_{BCE0}$ ) values of 300 GHz/500 GHz/1.6 eV and a minimum Current Mode Logic ring oscillator gate delay of 2.0 ps [25]. In order to fulfill the constant needs for ever faster SiGe:C HBTs with an adequate high power performance, it can be expected that future developments will further improve the frequency values entering into the THz regime [18, 23-25]. At the moment, different possible approaches are known which focus on fulfilling these tasks. Some of them are listed in the following [18]:

**Scaling of emitter area:** Aggressively scaling of the emitter area ( $W_E$ ), and therefore  $C_{BE}$  ( $= C'_{par} + C'_{dn} + C'_{dp} + C'_{DE}$  (Fig. 11)), results by the following equation

$$\tau_E = \frac{kT C_{BE}}{q I_C} \quad (22)$$

in a reduced emitter delay  $\tau_E$ . Considering equation (18) and the fact that  $W_E$  can be relatively easily scaled, it can be postulated that this mean will be used in future for  $f_T$  improvement [18].

**Base optimization:** The base transit time  $\tau_B$  is limited by the transit across  $W$  and the velocity of carriers to exit the base at the CB space charge region ( $v_{exit}$ ). Considering the following equation

$$\tau_B = \frac{kT}{\Delta E_{Ge}} \left( \frac{W^2}{\eta D_n} + \frac{W}{v_{exit}} \right) \quad (23)$$

where  $\Delta E_{Ge}$  is the grading in the base bandgap energy due to the introduced Ge content,  $\tau_B$  can be reduced by continuous shrinking of  $W$  using new process techniques (e.g. a combination of reduced thermal cycle) and by increased Ge content in the base to enhance the additional built-in electric drift field. This modification opens also the opportunity to improve  $f_T$  following equation (18) [18, 67].

**Reducing collector– base capacitance  $C_{CB}$ :** Considering the collector delay  $\tau_C$  component, given by

$$\tau_C = \left( R_E + R_C + \frac{kT}{q I_C} \right) C_{BC} \quad (24)$$

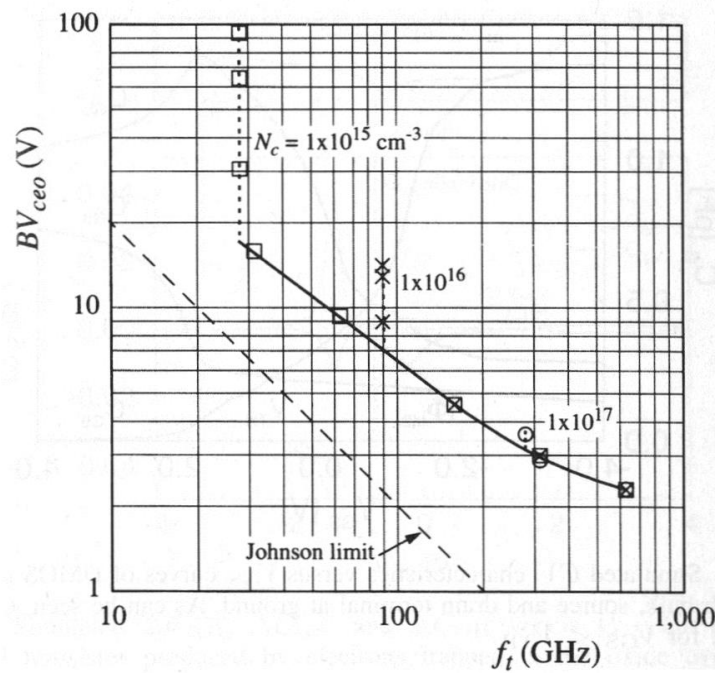
and equation (18), it is possible to improve  $f_T$  by reducing  $C_{CB}$  ( $= C'_{sc} + C'_{DC}$  (Fig. 10)) by scaling the active CB capacitance area using today's improved device geometry and using structures like the raised extrinsic base to reduce the CB capacitance per unit area [18, 67].

**Increasing collector doping  $N_C$ :** Considering again equation (24), it is also favorable to increase  $N_C$  by e.g. vertical collector scaling in order to increase  $I_C$  and to push out the Kirk effect<sup>1</sup> what also reduces  $R_C$ . In consequence,  $\tau_C$  can be reduced and  $f_T$  increased following equation (18) [18].

**Increasing saturation velocity  $v_{sat}$ :** The transit time  $\tau_{CB}$  through the CB space charge region  $W_{DC}$  is given by

$$\tau_{CB} = \frac{W_{DC}}{2 v_{sat}} \quad (25)$$

It is a significant impediment for improving speed performance of future SiGe:C HBT's. Because  $v_{sat}$  is a material property and not easily influenced by the production process, SiGe:C HBT device designers are limited by the given carrier mobility for both electrons and holes in Si. Therefore, new ways towards new materials (i.e. III-V-HBTs) are under investigation to overcome this fundamental limit in speed performance [18].



**Fig.14** A plot showing the Johnson limit and the revised fundamental limit on  $f_T$  and  $V_{BCE0}$  for modern bipolar devices. Dotted lines represent regimes where collector depletion width ( $X_C$ ) < collector width ( $W_C$ ) when unbiased (so  $f_T$  is constant), but  $X_C > W_C$  (reach through) at breakdown. Solid line represents regimes where  $X_C > W_C$  (reach through) for both biased and unbiased [66].

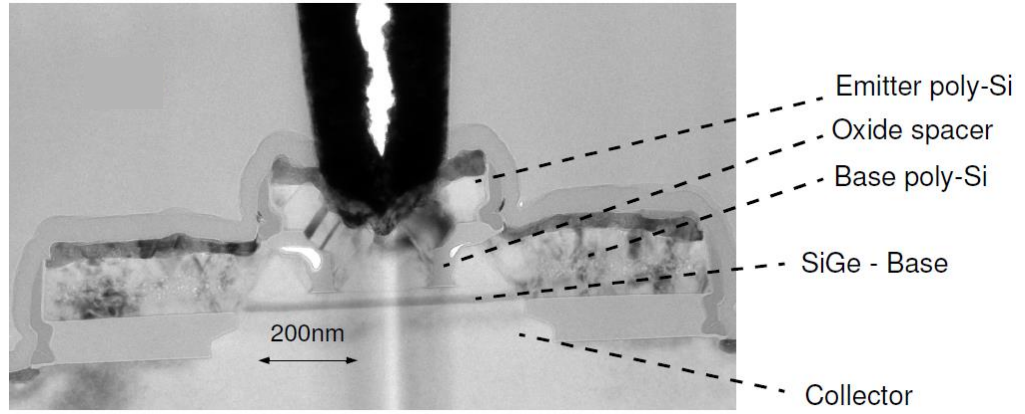
<sup>1</sup> High-field-relocation phenomenon in modern HBTs with lightly doped collector region, where the high-field region moves from the CB junction towards the collector  $n^+$ -substrate under high-current condition [45].

At the end, it is also to mention that another major problem still remains in SiGe:C HBT device technology, which will become more and more dominant with increasing speed performance. The three important parameters  $f_T$ ,  $V_{BCE0}$  and  $V_A$  are closely linked in form of a reciprocal relationship between the  $f_T$  and both  $V_{BCE0}$  and  $V_A$ . If the base and emitter profile of a HBT is constant,  $f_T$  can be improved by increasing  $N_C$  as well as making the collector shorter by decreasing the collector epitaxial layer thickness. Both of these methods result in a favorable delay of the Kirk effect onset [45, 67]. However, a disadvantage of increasing  $N_C$  lies in the decrease of  $V_A$  due to increased base-width modulation and the increase of impact ionization which lowers consequently  $V_{BCE0}$ . In addition, the reduction in collector epi-layer thickness also increases impact ionization due to the higher electrical field from the same voltage over a shorter distance. This shown trade-off behavior between  $f_T$  and both  $V_{BCE0}$  and  $V_A$  has been first characterized as the Johnson Limit [66-68, 88]. Figure 14 show the revised fundamental limit on  $f_T$  and  $V_{BCE0}$  for modern bipolar devices, where for a fixed  $N_C$ , as the collector width is reduced,  $V_{BCE0}$  decreases and  $f_T$  increases [66]. This material related characteristic makes it difficult to combine high-speed with high-power performance for pure SiGe:C HBTs for future improvements and developments.

For this reason, the goal of this thesis is to find novel approaches to ensure further improvement of the SiGe:C HBT technology towards high-speed and high-power performance in order to close the THz gap. Based on this task, two strategies were investigated in this work:

#### **1.4.1 Solid-phase epitaxy for emitter and base resistivity**

Solid-phase epitaxy (SPE) technique is used for local engineering of crystallinity in emitter and base layer of already established SiGe:C HBT device technology. Figure 15 shows a TEM micrograph of a current SiGe:C HBT device [25]. This approach offers an additional alternative to the above presented “scaling of emitter area” and “base optimization” approaches in order to improve HBT speed performance. By introducing disilane ( $Si_2H_6$ ) as new growth gas source with respect to standard used silane ( $SiH_4$ ) at IHP, it is possible to reduce the CVD growth temperature for Si, enabling in turn a differential growth of epitaxial-Si (epi-Si) on Si and amorphous Si (a-Si) (instead of poly-Si) on the  $SiO_2$  and  $Si_3N_4$  masks. More basis background about the used SPE technique will be introduced directly in 3.1.1. .



**Fig.15** TEM cross section of current SiGe:C HBT with  $f_T/f_{max}/V_{BCE0} = 300 \text{ GHz}/500 \text{ GHz}/1.6 \text{ V}$  [25]

The so produced requirement for SPE treatments has been evaluated for two possible areas of application:

**Emitter region:** By changing the standard poly-Si emitter (see Fig. 15) to a fully epi-Si emitter using SPE techniques, the emitter contact resistance  $R_{Ec}$  and the bulk emitter resistance  $R_{Eb}$  can be reduced which results by the following relationship [81]

$$R_E = R_{Ec} + R_{Eb} \quad (26)$$

in turn in a lower total emitter resistance  $R_E$ . A lower  $R_E$  concurrently increases  $I_E$ , improving (according to Kirchhoff's Law (remember equation (9)) in the end also  $I_C$ . Considering equation (18) and (19), increasing  $I_C$  will finally lead to higher  $f_T$  and  $f_{max}$  values.

**Base region:** By changing the standard poly-Si base link region on the mask (see Fig.15) to epi-Si using SPE techniques, the base contact resistance  $R_{Bc}$  and the external base link resistance  $R_{Be}$  following relationship [81, 133]

$$R_B = R_{Bc} + R_{Be} + R_{Bi} \quad (27)$$

can be reduced, resulting in turn in a lower  $R_B$ . Thereby,  $R_{Bi}$  is the internal base resistance under the emitter (pinched base). As already shown in equation (19), a reduction in  $R_B$  directly improves  $f_{max}$ .

#### 1.4.2 III-V/SiGe hybrid device: $\text{In}_{1-x}\text{Ga}_x\text{P}$ collector

The ternary compound semiconductor Indium gallium phosphide ( $\text{In}_{1-x}\text{Ga}_x\text{P}$  [ $x = 0 - 1$ ]) will be introduced as potential new collector material as part of an advanced III-V/SiGe

hybrid HBT device. Table I shows the main physical parameters of the binary materials Indium phosphide (InP) and Gallium phosphide (GaP) at 300 K, important for SiGe HBT speed and power performance increase, in comparison to Si [90]:

	Si	InP	GaP
Bandgap [eV]	1.12	1.33	2.26
Breakdown voltage [ $V\text{ cm}^{-1}$ ]	$3 \times 10^5$	$5 \times 10^5$	$1 \times 10^6$
Electron mobility [ $\text{cm}^2\text{ V}^{-1}\text{ s}^{-1}$ ]	1400	5400	250
Saturation velocity [cm/s]	$1 \times 10^7$	$3 \times 10^7$	$1 \times 10^7$
Lattice constant [nm]	0.5431	0.5869	0.5451

**Tab.I** Important physical parameters of Si, InP and GaP (at 300 K) for SiGe HBT high frequency and power performance increase as well as heterostructure growth [90].

On the one hand, InP has a three times higher saturation velocity  $v_{\text{sat}}$  than Si [90], following the above presented “increasing saturation velocity  $v_{\text{sat}}$ ” approach. On the other hand, the wide bandgap semiconductor GaP has a two times bigger bandgap than Si [90], which decreases impact ionisation rates in the collector [45, 46]. This offers a higher  $V_{\text{BCE0}}$  threshold and the possibility to run hence the HBT device under higher  $I_C$ , leading in the end to a higher power and speed performance (see equation (19)). In other words, ternary  $\text{In}_{1-x}\text{Ga}_x\text{P}$  systems as potential collector material provide the vision to adjust speed ( $f_T$ ;  $f_{\text{max}}$ ) and power ( $V_{\text{BCE0}}$ ;  $I_C$ ) of HBTs in a flexible way as a function of the  $\text{In}_{1-x}\text{Ga}_x\text{P}$  collector chemical composition  $x$  [90].

In the following, this Ph.D. thesis will evaluate the potential of these two new material approaches for next generations of future SiGe:C HBT BiCMOS technology.



## 2. Experimental part

### 2.1. Thin film growth techniques

In this thesis, two different epitaxial growth techniques have been used and will be therefore briefly presented in the following:

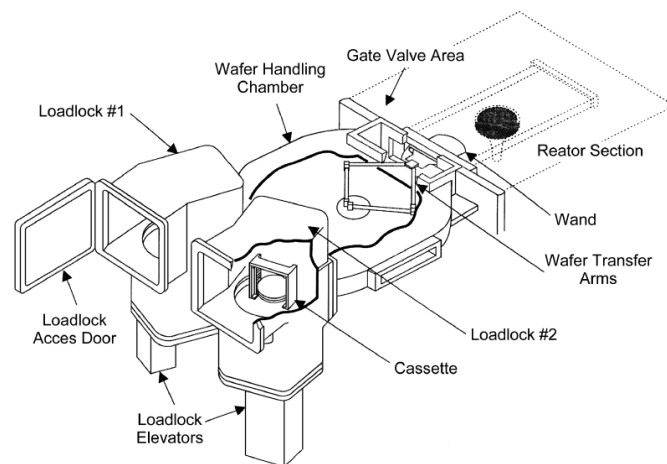
**Reduced pressure chemical vapor deposition:** The reduced pressure chemical vapor deposition (RPCVD) is a subtype of the CVD growth technique, where the pressure of the reactor can be varied from atmospheric down to practically 10 Torr. Otherwise, RPCVD follows the known CVD process mechanism: Chemical precursors are transported in the vapor phase to a heated substrate and form there an overlayer by decomposition, adsorption and surface reaction. CVD has many noticeable advantages over physical vapor deposition techniques like e.g. molecular beam epitaxy (MBE) or sputtering. High throughput, purity, accurate and reproducible thin film deposition as well as low cost of operation are the main features. Another important and unique feature of CVD is the homogeneous thin film deposition on three-dimensional structures with high aspect ratio. All these advantages made by now CVD the major method of film deposition for the semiconductor industry, which certainly is a mass-production market. However, this growth technique has also some disadvantages in the way of in-situ monitoring of thin film growth and due to costs to develop the needed precursor chemistry. More details to this frequently developed growth technique can be found in various reviews in the literature [18, 38, 99, 100].

Figure 16 shows a cleanroom image (a) and a technical sketch (b) of the ASM Epsilon 2000™ single wafer RPCVD reactor (similar to the one in IHP's cleanroom), which has been used in this thesis for Si/Ge growth and in-situ annealing experiments. This RPCVD model is designed for deposition on 200 mm (8 inch) Si wafers and consists of three main parts: The two load-locks, the wafer handling section and the process quartz chamber. The wafer handling section is equipped with a quartz wand Bernoulli arm to automatically transfer single wafers from the load-locks onto a silicon carbide coated graphite susceptor in the process chamber and vice versa. To avoid oxygen contamination during handling and storage, the two load locks and the wafer handling chamber are always purged with nitrogen (N<sub>2</sub>) gas. Additionally, the two load locks can be pumped down and backfilled for entering and removing racks with 25 wafers. The susceptor itself consists of two parts: an outer fixed

a)



b)

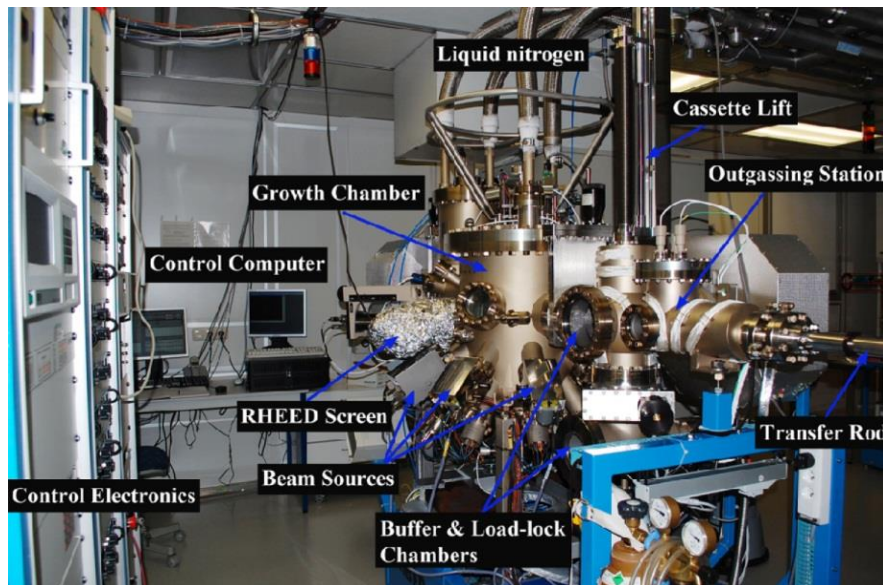


**Fig.16** Picture of an ASM Epsilon 2000™ single wafer RPCVD reactor in a cleanroom **(a)** and the corresponding schematic illustration **(b)** [97].

body and an inner rotating plate, on which the wafer is positioned during the processing. The wafers have to be rotated during the CVD process to ensure a homogeneous deposition of material. Two sets of halogen tungsten lamps, located at top- and downside of the quartz glass chamber provide the susceptor with thermal radiation and enable growth and rapid thermal adjustments in the range of 300 – 1200 °C. Via pneumatic valves in the gate valve area, the following process gases can be injected into the reactor:  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$  and dichlorosilane ( $\text{SiCl}_2\text{H}_2$ ) as the Si sources, 1.5% germane ( $\text{GeH}_4$ ) in hydrogen ( $\text{H}_2$ ) as Ge source and 5% methylsilane ( $\text{SiH}_3\text{CH}_3$ ) in  $\text{H}_2$  as C source. Diborane ( $\text{B}_2\text{H}_6$ ), Arsine ( $\text{AsH}_3$ ) and Phosphine ( $\text{PH}_3$ ) gas are available as B, As and P doping sources, which can be introduced into the reactor by direct injection for high doping or by dilution in  $\text{H}_2$  for low doping concentrations.  $\text{H}_2$  and  $\text{N}_2$  are serving as carrier and purge gas sources in the process chamber. Finally, hydrochloric acid ( $\text{HCl}$ ) is used for process chamber etching and as process gas in the selective epitaxy. In order to reduce  $\text{O}_2$  contamination in the epitaxial layers,

both HCl and H<sub>2</sub> gas pipes are equipped with an in-line purifier unit. The used gases during the process will be exhausted and neutralized in a scrubber and later disposed in a burner [97, 98].

**Gas-source molecular beam epitaxy:** The gas-source molecular beam epitaxy (GSMBE) is a variation of the MBE growth technique, where gases instead of solid source materials are used in part or entirely as sources for growth materials typically in an ultra-high vacuum (UHV). Otherwise, all MBE systems have the same underlying process mechanism: Molecular beams in form of fluxes of evaporated or cracked growth material and dopant species are directed on a heated substrate and react there towards an (e.g. epitaxial) overlayer. Compared to other growth techniques like e.g. CVD, MBE systems have the advantage to grow ultra-pure layers with atomic monolayer precision and to monitor the whole growth process in the same time in-situ by e.g. reflection high energy electron diffraction (RHEED). This fact makes MBE a favorite tool for versatile research efforts in the field of model system studies. Nevertheless, disadvantages also exist due to low throughputs and a limited three-dimensional coverage during the growth process. A lot of reviews in literature already refer to this growth technique, enabling better insight and more details [101, 102].



**Fig.17** Picture of a Riber Compact 21T GSMBE reactor in a cleanroom [103].

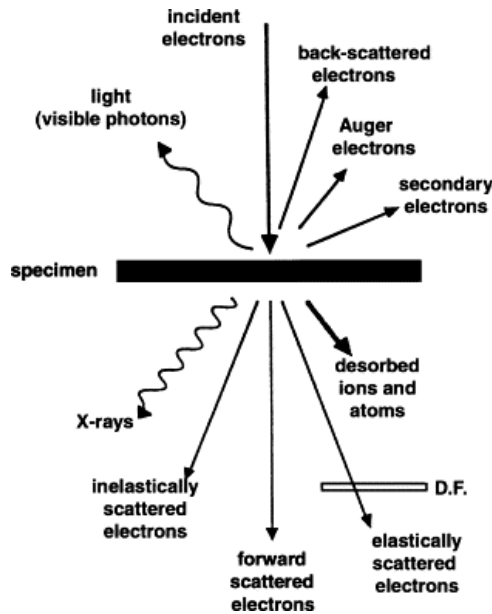
Figure 17 shows the Riber Compact 21T GSMBE, which has been used in this thesis for GaP growth at HU Berlin. This depicted GSMBE system possesses a loading chamber, a buffer chamber and a growth chamber. In the loading chamber, a UHV environment in the range of 10<sup>-8</sup> Torr is created and maintained by a small turbo and a membrane pump. For

loading, the substrates can be directly put as 3 inch wafer or can be inserted as pieces by using a special sample holder into the loading cassette. Afterwards, a remote controlled cassette lift can transfer the substrates from the loading chamber to the buffer chamber. An ion pump ensures UHV in the range of  $10^{-10}$  Torr in the buffer chamber. Before passing one substrate by a manual transfer rod through the lock into the growth chamber, the substrate will be brought for outgassing to the heating station. The annealing generally runs for two hours at 200 °C. Finally, the annealed substrate can be introduced to the growth chamber and placed in the middle of the chamber on a heatable substrate holder. An UHV condition of  $10^{-9}$  Torr is maintained in the growth chamber by a powerful turbo and ion pump. Additionally, a liquid nitrogen cooling system, which surrounds the inner chamber surface, is helping to reduce the number of remaining impurities by freezing them out on the cold reactor wall. For an eventual deoxidation of the substrate surface, the sample can be heated by a filament on the substrate holder up to 750 °C. For material growth, the growth chamber is equipped with solid and gas source beam systems containing effusion and cracking cells. The molecular beams, created by applying temperature to the sources, can be digitally controlled by thermocouples and mechanical shutters. The solid source materials Indium (In), Gallium (Ga), Aluminum (Al) as group III-elements, Si as n dopant, and Manganese (Mn) as p dopant or for diluted magnetic semiconductor (DMS) materials are available by effusion cells. Antimony (Sb) as group V-element is accessible by a cracking cell. Other group V-elements, like Arsenic (As) and Phosphor (P) are available over  $\text{AsH}_3$  and  $\text{PH}_3$  gas sources, which in general are thermally cracked at 920 °C. The group V fluxes are controlled by mass flow controller [103, 104].

## 2.2. Characterization techniques

For characterization of prepared and processed samples in this study, a number of different investigation methods have been employed. For completeness, all used investigation methods will be presented briefly in the following:

**Scanning electron microscopy (SEM):** SEM is a technique for generating high-resolution images by microscopy. Unlike the light microscopy, SEM uses shorter wavelengths in form of a focused high-energy electron beam (primary electron beam) to scan the sample. These highly accelerated electrons collide with the atoms on the surface and produce a series of different signals. Figure 18 shows a schematic overview of all possible occurring physical processes in the SEM setup when the electron beam hits the sample [105]:



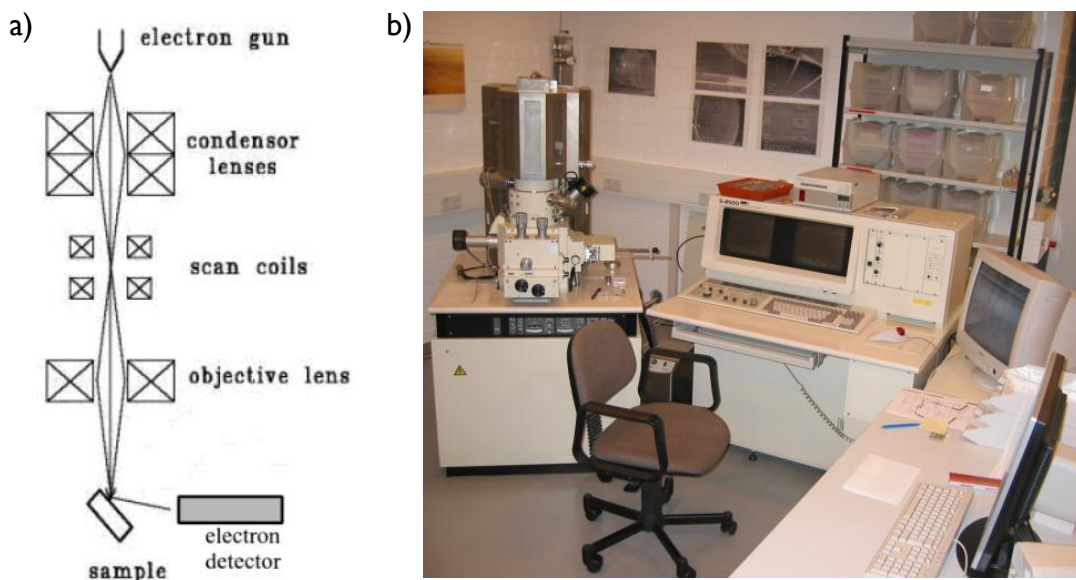
**Fig.18** Schematic of the information from elastically and inelastically scattered electrons during the electron beam–sample interactions [105].

To understand this technique, it is helpful to remind that these highly accelerated electrons have three different options to interact with the sample surface: They can either a) pass through the sample without any interaction, or b) be scattered elastically or c) be scattered inelastically. While elastic scattering only changes the direction of the electrons, inelastic scattering also transmits energy, which may cause a direct emission of surface electrons or excite them into discrete shells. In the second case, additional emissions in form of secondary electrons (SE), Auger and Photoelectrons or X-ray radiation are the result. For SEM images, usually SE and backscattered electrons (BSE) are important. These electrons can be collected by suitable detectors (with a usually positive voltage of 10 - 100 V) and converted by computer assisted image processing in two- and three-dimensional SEM pictures. The topography and morphology depicted in these generated pictures are created by the number of electrons that reach the secondary electron detector from any point on the scanned surface and by the local variation in electron intensity, respectively [105-108].

Figure 19(a) shows a schematic design of a scanning electron microscope. In principle, the construction of the SEM differs only slightly from that of an optical microscope. However, instead of light and optical lenses, SEM uses an electron beam and electromagnetic lenses. The electron beam is generated in an electron gun fitted with a tungsten filament cathode and has generally excitation energies of 100 – 400 keV. Tungsten is generally used

on the one side due to its highest melting point and lowest vapor pressure of all metals, and on the other side due to its low cost. By condenser lenses, the now created electron beam is subsequently collimated in order to precisely focus the beam on the sample. Special scan coils, which produce inducing magnetic fields, enable a raster-type movement of the beam over the sample. Finally, the via computer controllable objective lens collimates the electron beam again and indicate the image scale by setting the focal length in the given object distance. More details about this characterization method can be found in literature [106-108].

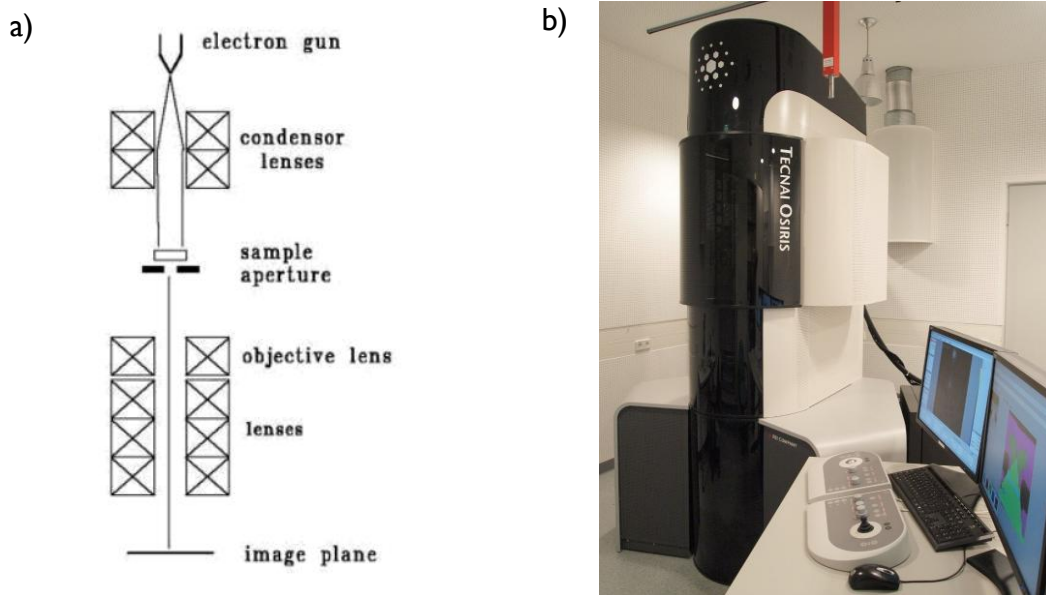
For all SEM analysis in this thesis, the Hitachi S-4500 SEM System operating with an operation voltage of 25 keV was used at IHP (depicted in Fig. 19(b)).



**Fig.19** (a) Simplified illustration of a SEM setup. (b) Hitachi S-4500 SEM System used in this thesis [106, 107].

**Transmission electron microscopy (TEM):** TEM is, in comparison to the already mentioned SEM, basically another operation mode for electron microscopes, in which electron beams are being used to achieve resolutions in the range of 0.2 nm and smaller. The theoretical background of this measurement method is similar to that of the SEM, whereas the TEM shows significant differences in operation and construction. The most striking difference between a TEM and SEM microscope is that electrons are used for detection, which have irradiated through the sample before. For this purpose, the sample must be correspondingly thin (typically < 300 nm). For preparation of such thin cross-section samples

(called lamella), generally a focused ion beam (FIB) system or mechanical grinding and polishing followed by an argon (Ar) ion milling process is used. To ensure the stability and localization during the TEM measurement, the prepared TEM lamella is placed on a special TEM grid. If these requirements are met, the sample cross-section can be measured by setting an adequate acceleration voltage for the electron beam. Typical acceleration voltages of TEM microscopes are 80 kV to 400 kV. It should be considered here that the higher the atomic number of the atoms of the sample and the lower the adjustable acceleration voltage is, the thinner must be the prepared TEM lamella [106-110].



**Fig.20** (a) Simplified illustration of a TEM setup. (b) FEI Tecnai Osiris TEM System used in this thesis [106, 107].

Figure 20 shows a schematic design of a transmission electron microscope. Accelerated and emitted from the electron gun, the primary electrons will be deflected afterwards by a condenser lens system so that they fall approximately parallel (plane wave) onto the desired sample section and uniformly illuminate it. Within the sample, the primary electrons are scattered or diffracted differently, which may change their direction of movement (see Fig. 18). However, electrons leaving the sample at the same angle (transmission) will be focused by objective lenses at one point in the focal plane. Via a subsequent projective lens system, the intermediate image of the objective lens is further amplified and afterwards depicted on the detector (image plane). As detector generally acts on the one hand a phosphor screen coated with fluorescent zinc sulfide for

direct viewing, or on the other hand a photo-active film or a charge-coupled device (CCD) camera for recording a TEM image. By modification of the projective lens system, it is also possible to amplify the focal plane of the objective lens instead of the intermediate image. This technique results in an electron diffraction image, which allows the determination of the crystal structure and the layer thicknesses of the sample (named selected area (electron) diffraction (SAD or SAED)) [106-110].

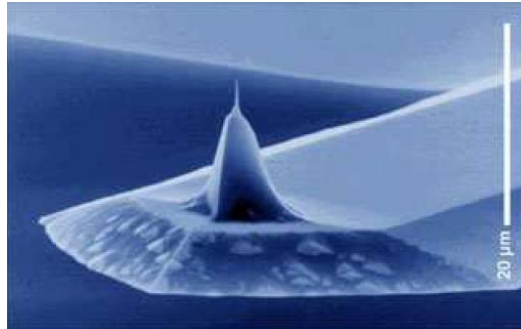
Next, the high-resolution transmission electron microscopy (HRTEM) and the associated dark field (DF) imaging technique are to be mentioned as important TEM characterization modes used in this thesis. These imaging modes enable studies of samples in order to investigate the crystallographic structure, defects and polarity on the atomic level. The method for HRTEM image creation is based on the use of the information-carrying phase contrast, which is generated by the electron wave interference in the image plane. In DF HRTEM imaging, however, the unscattered electron beam is excluded from the image creation by tilting the incident beam until almost only a diffracted beam passes through the aperture in the objective lens to the image plane (see Fig. 20(a)). Thereby, it is possible to detect only the diffracted intensity coming from one single collection of diffracting planes in relation to sample position and tilt. The DF HRTEM images generated in this way allow highlighting lattice defects, like e.g. anti-phase domains (APD), by tilting the sample slightly off the Bragg condition. More details about this characterization method and their different modes for material science studies can be found in literature [106-112].

Finally, TEM can also be combined with energy dispersive x-ray (EDX) spectroscopy in order to investigate the cross-sectional chemical composition of specimen with high lateral resolution (TEM-EDX). Therefore, the x-ray excitation for EDX is introduced by electrons accelerated from the electron gun of the TEM setup towards lamella. Afterwards, an additional installed EDX detector (e.g. Silicon Drift Detector (SDD)) inside the TEM system maps all x-ray signals relating to elements (down to boron) and position. The TEM-EDX technique is used in this thesis to give a first assessment of possible migration behavior during heterostructure growth [106, 107].

In this thesis, the FEI Tecnai Osiris TEM System operating at 200 kV was used for all standard HRTEM and TEM-EDX analysis at IHP (depicted in Fig. 20(b)). For APD defect characterization, DF HRTEM imaging was performed in a JEOL 3010 UHV TEM operating at 300 kV at Paul-Drude-Institute for solid-state electronics in Berlin.



**Atomic force microscopy (AFM):** AFM is one of the scanning probe microscopy techniques that allow studies of surface structures up to a resolution down to the atomic scale. Therefore, a very fine probe tip is used, which moves line by line over the sample and interacts locally with the sample surface as a function of distance [106, 107, 115]. One example of an AFM tip is shown in Fig. 21.



**Fig.21** SEM of a micro-machined silicon cantilever with an integrated tip pointing in the [001] crystal direction [113].

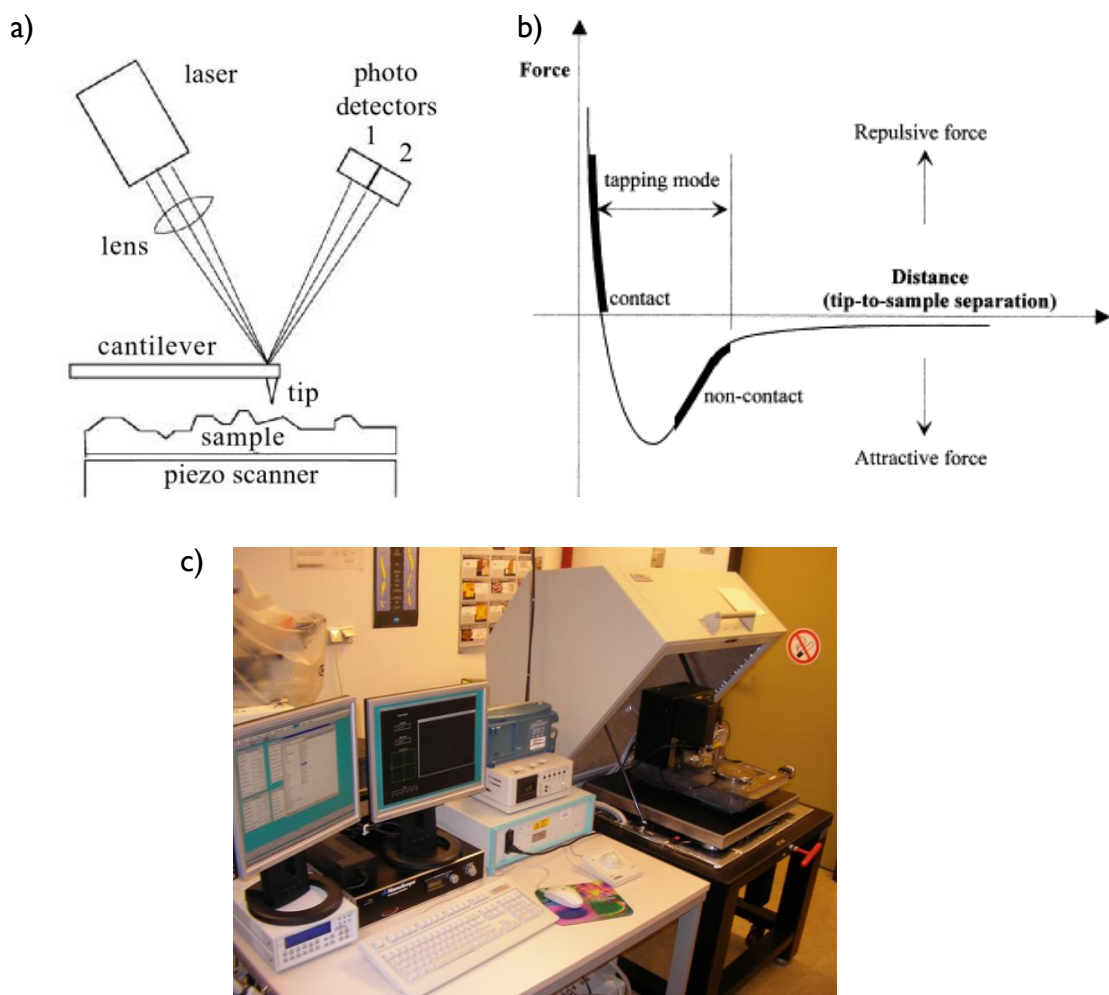
Figure 22(a) illustrates a schematic design of an AFM setup. The raster-type movement of the probe tip over the sample surface is done by piezo elements. These piezo elements are special crystals, which form under pressure an electric dipole moment due to the mechanical-introduced movement of charges in the unit cells. However, the reverse effect (known as electrostriction) is used here, in which the piezoelectric crystals expand depending on the polarity of the applied voltage. For position detection serves a laser beam which is directed first to the back side of the cantilever and is afterwards detected by a position-sensitive photodiode. When approaching, the probe tip is brought into contact with the sample surface at a certain height due to attractive Van der Waals forces. Upon further approximation, the repulsive electrostatic interactions outweigh [106, 107, 115]. This is empirically shown in the well-known Lennard-Jones potential depicted in Fig. 22(b).

The resolution of the AFM is limited by three factors: Firstly, the resolution depends on the set step size between the single measuring points. Secondly, the shape of the chosen probe tip has major impact on the resolution. Finally, the nature of the sample and of the medium between the probe tip and the sample surface are important, because they determine the type and range of the acting forces. The AFM technique can be used in different modes: The contact mode, the tapping mode<sup>TM</sup> or the lateral force mode. Due to the fact that only the tapping mode was used in this thesis, only this operation mode will be

introduced here. More information and details about this characterization method and their different modes can be found in literature [106, 107, 115].

In the tapping mode<sup>TM</sup> (also known as intermittent contact mode), the cantilever is set with a high force constant offset into vertical oscillation with amplitude of 20 - 100 nm near its resonant frequency of 200 - 400 kHz. In the same time, the piezoelectric element is used to control the height of the cantilever above the sample. In this way, it is possible to measure the topography of a sample by recording the variations in the amplitude between the probe tip and the sample surface due to the changing distances between each other. It is noted that the tapping mode reduces the probability to damage the probe tip and the sample surface in comparison to the contact mode [106, 107, 115].

For all AFM analysis in this thesis, the VEECO Digital Instruments Dimension 5000 AFM System was used at IHP (depicted in Fig. 22(c)).



**Fig.22** (a) Simplified illustration of an AFM setup. (b) Force–distance curve following the Lennard-Jones potential. (c) VEECO Digital Instruments Dimension 5000 AFM System used in this thesis [106, 107, 114].

**X-ray diffraction (XRD):** XRD is a non-destructive analytical technique, which is mainly used to investigate the crystallographic structure of solid-state materials. This method is based on the coherent diffraction of x-ray waves (electro-magnetic waves in the range of 120 eV to 120 keV) at periodic arrangements of atoms in crystalline solids [116, 118].

Scattering by single free electron: When only considering the scattering by a single free electron, the situation can be described by the Thomson scattering. In this process, the incoming transversal electro-magnetic wave (or x-ray beam) induces an electric field, which forces the electrons of the atom to accelerate and thus to radiate with the frequency equal to the frequency of the incoming wave. Its intensity  $I_e$  measured at distance  $R$  and under angle  $\phi$  to the incoming wave can be written using the Thomson scattering equation [116, 108]:

$$I_e = I_0 \frac{e^4}{m^2 c^4 R^2} \left( \frac{1 + \cos^2 \phi}{2} \right) \quad (28)$$

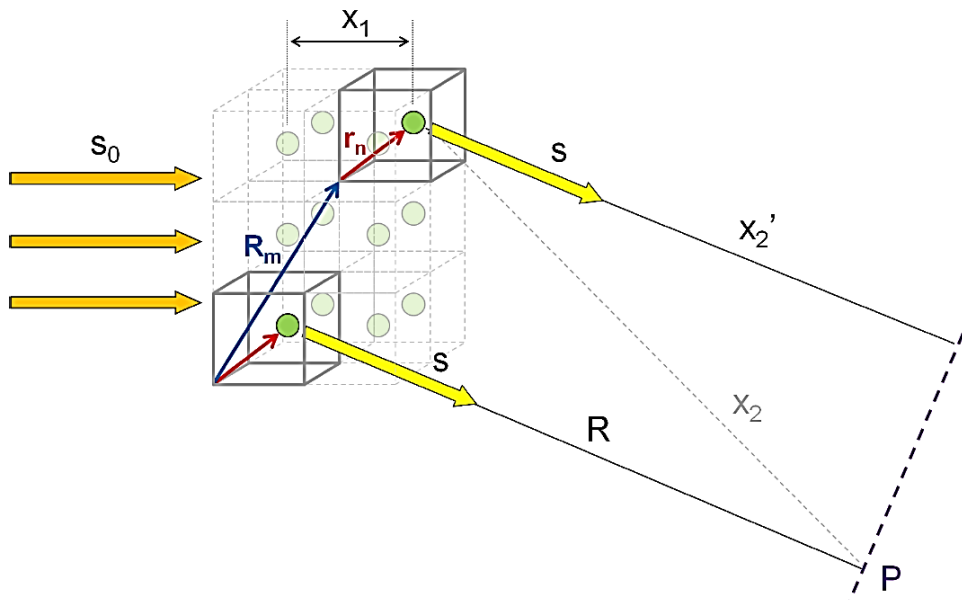
where  $I_0$  is the intensity of the unpolarized incoming wave and  $(1 + \cos^2 \phi)/2$  its polarization factor. Interestingly, with the electron charge  $e$ , the electron mass  $m$  and the speed of light  $c$ , the prefactor  $\frac{e^4}{m^2 c^4}$  is on the order of  $10^{-26} \text{ cm}^2$ . This means that the intensity of x-ray waves scattering at one electron tends to zero and is thus very inefficient. In addition, the mass of a proton is at least 1836 times bigger than the mass of an electron, what causes, in consequence, a  $10^{-6}$  lower  $I_e$  in comparison to scattering at an electron. This is the reason why scattering at the nucleus is neglected and only the electrons are considered in XRD. However,  $I_e$  has to be increased to measurable quantities to record XRD spectra. This is usually the case by increasing the amount of electrons (scattering centers) due to the fact that volume material is investigated (e.g. one mole of matter contains approximately  $10^{23}$  electrons). Certainly, one should consider that a random distribution of these additional scattering centers leads only to a white noise signal, since no defined phase-dependence is obtained between the secondary x-ray waves. Another possibility to increase  $I_e$  is to use high-brilliance synchrotron radiation sources to investigate structure and defects in case of ultra-thin films and nanostructures [116, 118].

Diffraction at single crystalline structures: Next the diffraction at single crystalline structures is considered. A single crystalline structure consists of unit cells which are periodically repeated in all three directions of space. Since the distance of the periodic atomic arrangements are in the range of the x-ray wavelength, the

crystal lattice planes of the crystalline structure act as diffraction gratings and the Bragg condition is applied:

$$n\lambda = 2d \cdot \sin\theta \quad (29)$$

where  $n$  is an integer,  $\lambda$  is the wavelength of incident wave,  $d$  is the spacing between the planes in the atomic lattice, and  $\theta$  is the angle between the incident ray and the scattering planes. In consequence, x-rays exposed to a small crystal gives rise to constructive and destructive interference of the elastic scattered wave, creating a characteristic diffraction pattern. To explain this effect, two additional factors must be taken into account: the structure factor  $F$  and the lattice factor  $G$ . Figure 23 shows, for illustration, a sketch of the diffraction of a parallel primary beam by a small crystal [116 -118]:



**Fig.23** Schematic diffraction of a parallel primary beam by a small crystal [116, 118].

Because of the assumption that the crystal is small in comparison to the distance  $R$  to the point of observation, the primary and scattered beam can be treated by the plane-wave approximation, and hence  $(x_1 + x_2) \rightarrow (x_1 + x_2')$ . From a chosen origin,  $R_m$  is the translation vector of the unit cell at the origin to another identical unit cell in the same crystal structure. The vector  $r_n$  corresponds to the position of one atom inside the unit cell, measured from the unit cell origin. Using these two variables, any atom position in the crystal structure can be described by  $R_m + r_n$ . X-rays with the wavelength  $\lambda$ , which are scattered from a crystal with  $N_i a_i$  ( $i = 1; 2; 3$ ) unit cells along  $a_i$  crystal axes, have an intensity  $I$  at the point  $P$  of observation given by [116, 118]:

$$I = I_e F^2 G^2 \quad (30)$$

where

$$F = \sum_n f_n e^{\left(\frac{2\pi i}{\lambda}\right)(s-s_0)r_n} \quad (31)$$

and

$$G^2 = \frac{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)N_1a_1 \right]}{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)a_1 \right]} \frac{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)N_2a_2 \right]}{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)a_2 \right]} \frac{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)N_3a_3 \right]}{\sin^2 \left[ \left(\frac{\pi}{\lambda}\right)(s-s_0)a_3 \right]} \quad (32)$$

Here,  $s_0$  and  $s$  are the unit vectors which correspond to the propagation direction of primary and scattered beam, respectively. The atomic form factor  $f_n$  in equation (31) is a measure of the scattering amplitude of a x-ray beam by the electron distribution (electron cloud) of the atom. For this reason, the scattering amplitude of x-rays increases for example with the atomic number  $Z$  of the atoms in the specimen. Together with  $f_n$  and  $r_n$ ,  $F$  possesses the only information about atomic positioning in the equations above and play therefore an important role in determining the crystal structure. This is the reason, why it is accordingly called structure factor. Equation (32) describes  $G$  which corresponds (by definition) to the periodicity of the crystal and is therefore called the lattice factor. Here, it is clearly visible that the shape of the observed signal strongly depends on the number of unit cells  $N_i$ . For higher  $N_i$ , the peak height generally increases and its full width at half maximum (FWHM) decreases. In conclusion,  $G$  is determined by the spatial dimensions of the unit cell and thus the size as well as the long-range order within the crystal. Therefore, constructive interference only occurs when the three terms of  $G$  are simultaneously close to their maxima. This fact lead to the XRD selection rules and is mathematically described by the Laue equations [116, 118]:

$$\frac{\pi}{\lambda}(s-s_0)a_1 = h\pi \quad (33)$$

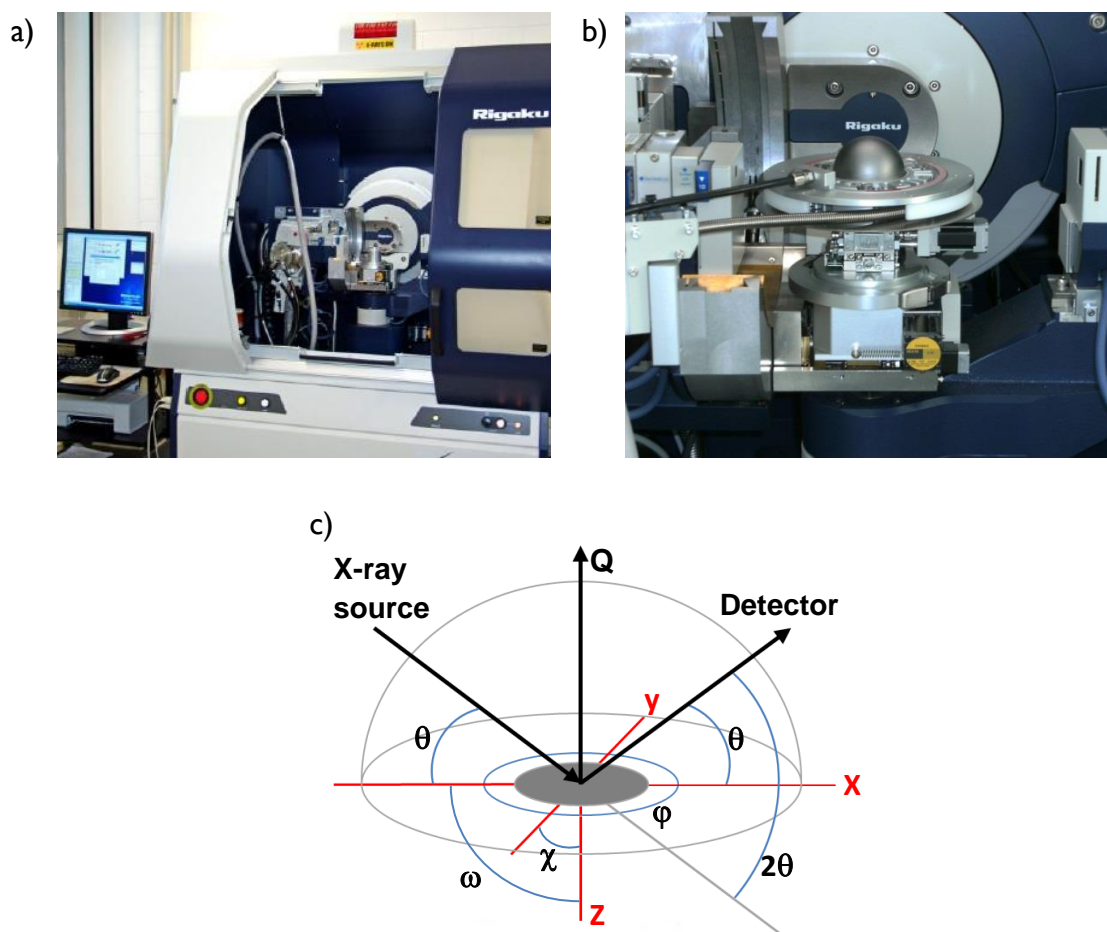
$$\frac{\pi}{\lambda}(s-s_0)a_2 = k\pi \quad (34)$$

$$\frac{\pi}{\lambda}(s-s_0)a_3 = l\pi \quad (35)$$

where  $h$ ,  $k$ , and  $l$  are integer numbers. Since a diffracted beam exits only if the three Laue equations are simultaneously satisfied, these three equations together are equivalent to Bragg law (equation (29)). More information and details about this characterization

method and their different applications can be found in literature [116, 117].

For all XRD analysis in this thesis, the RIGAKU SmartLab diffractometer equipped with a 9 kW rotating Cu anode ( $\text{Cu}_{\alpha} = 0.1541 \text{ nm}$ ) was used at IHP (depicted in Fig. 24(a)). An

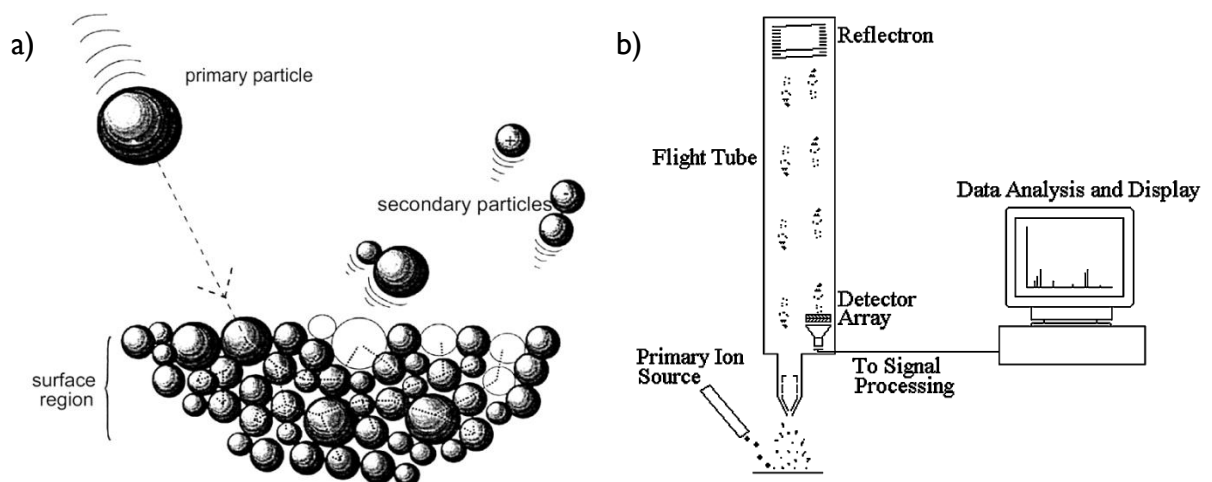


**Fig.24** (a) RIGAKU SmartLab diffractometer and (b) ANTON PAAR DHS 1100 furnace mounted on the SmartLab diffractometer used in this thesis. (c) Schematic illustration of XRD measurement setup with all associated angles and axis.

ANTON PAAR DHS 1100 furnace was mounted on the SmartLab diffractometer to perform in-situ temperature dependent XRD studies under 1 bar  $\text{N}_2$  atmosphere, (shown in Fig. 24(b)). For better understanding of the used XRD measurement modes, Figure 24(c) depicts a schematic illustration of the XRD setup with all the associated angles and axes: For both specular  $\theta/2\theta$  and in-plane XRD measurements, the position of the x-ray source and the detector can be changed with the help of sample and diffractometer rotation axes. For special measurement modes (e.g. reciprocal space mapping (RSM) and pole figures (PF)), the sample can be tilted along the beam direction (along the x-axis) by angle  $\omega$  and perpendicular to the beam direction (along the y-axis) by angle  $\chi$ , respectively. In addition,

the sample can also be rotated around itself by angle  $\varphi$ . All measured samples were adjusted in such a way that the normal of the (004) net plane (coincidentally, the z-axis in Fig. 24(c)) is parallel to the  $\varphi$ -axis of the diffractometer. This allows to measure (004) diffraction curves under symmetrical as well as asymmetrical Bragg condition depending on the chosen  $\varphi$ -direction. High resolution XRD curves were recorded using a Ge(400)x2 collimator crystal behind a x-ray mirror and a Ge(220)x2 crystal analyzer. Both specular  $\theta/2\theta$  and in-plane XRD measurements were performed with a  $0.114^\circ$  soller slit on the detector side. PFs were measured without crystal collimator and  $0.5^\circ$  soller slits on source and detector side.

**Secondary ion mass spectrometry (SIMS):** The static SIMS is a semi-destructive and surface-sensitive analytical method. Different types of this measurement technique exist. For instance, Time-of-Flight SIMS (ToF-SIMS) emerged in the last decades as the most dominant variant for the field of material and surface science. In the static SIMS method (as in ToF-SIMS) a pulsed energetic beam of primary particles, usually ions (i.e. Ar<sup>+</sup>, Ga<sup>+</sup>, Cs<sup>+</sup>) or neutrals, is used, which is focused on the sample surface. Figure 25(a) shows a schematic diagram of the processes on the surface after the impact of the primary beam [140]:



**Fig.25** (a) Schematic diagram of the surface process during SIMS measurement. (b) Simplified illustration of a ToF-SIMS setup [138, 140].

The focused, high energy (between 1 and 25 keV) primary beam initiates a bombardment of the sample surface with primary particles (ions or neutrals), in which the particle energy is transferred to the atoms of the sample by billiard-like collisional processes. This generates a cascade of collisions between the atoms in the sample, causing some of them to return to

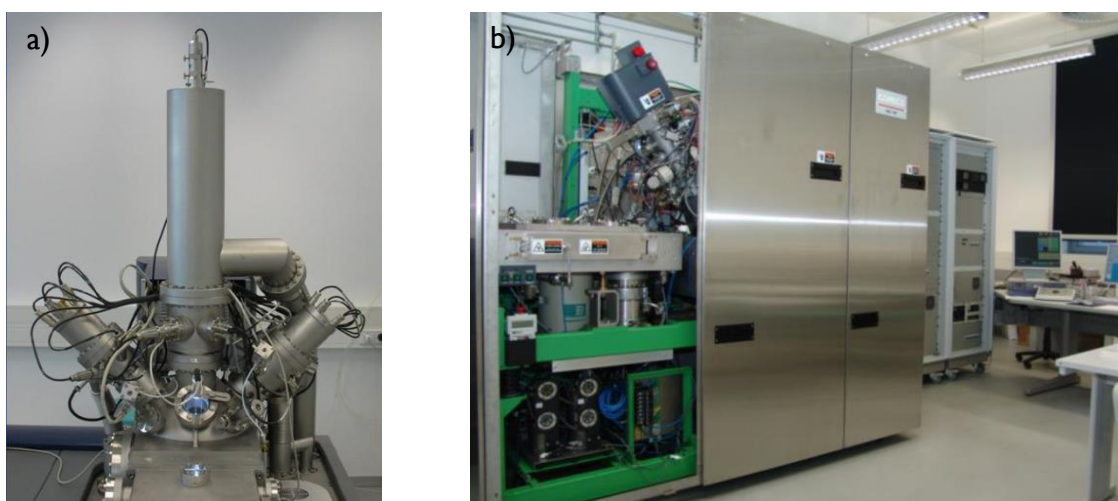
the surface, which result in the end in emission of neutral or ionised atoms and atom clusters (named secondary particles). Figure 25(b) illustrates as example the special feature of ToF-SIMS with respect to static SIMS [140]. For detection, the static SIMS uses a quadrupole mass spectrometer. However, in ToF-SIMS, the emitted secondary ion particles are accelerated into a flight tube, where individual ion masses can be separated based upon the time it takes the ion to leave the sample surface and arrive at the detector array. The mass  $m$  of each ion with charge  $q$  can be extracted from the time-of-flight  $t$  [139, 141]:

$$t = L \sqrt{\frac{m}{2qU_e}} \Leftrightarrow m = 2qU_e \left(\frac{t}{L}\right)^2 \quad (36)$$

where  $L$  is the length of the analyser,  $U_e$  is the acceleration voltage. Three operational modes are available using ToF-SIMS: surface spectroscopy, surface imaging and depth profiling. Due to the fact that only the depth profiling was used in this thesis, only this operation mode will be introduced in the following. More information and details about this characterization method and their different modes can be found in literature [139, 140].

For depth profiling, an additional high current sputter beam (i.e. O or Cs in our case) is applied together with the pulsed ion beam (i.e.  $\text{Bi}_1$ ,  $\text{Bi}_3$  and  $\text{Bi}_3^{++}$  ions/clusters in our case). In this way, the investigated sample is continuously eroded and the intensity of the masses of interest can be displayed as a function of the depth in a depth profile [139].

For all depth profile and concentration measurements in this thesis, the ION-TOF 5 ToF-SIMS and CAMECA IMS WF SIMS system were used at IHP (depicted in Fig. 26(b)&(c)).



**Fig.26** (a) ION-TOF 5 ToF-SIMS system and (b) CAMECA IMS WF SIMS used in this thesis.

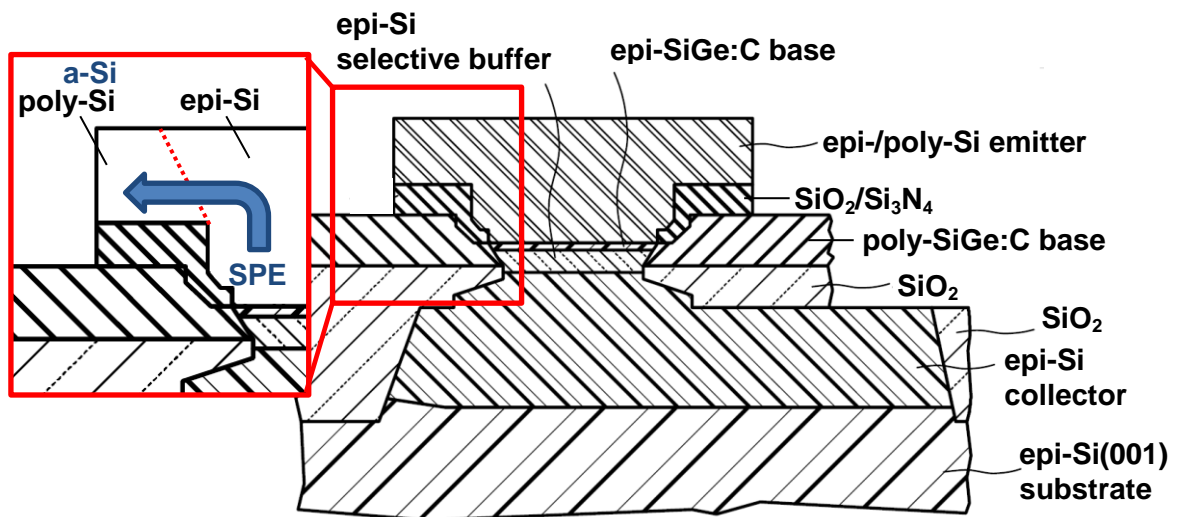


## 2.3. Sample preparation

In this paragraph, the sample preparation for the SPE and the  $\text{In}_{1-x}\text{Ga}_x\text{P}$  growth studies are presented. This includes the applied growth system, substrate choice and cleaning as well as the material deposition and the sample characterisation by the above introduced growth and measurement techniques.

### 2.3.1 SPE growth studies

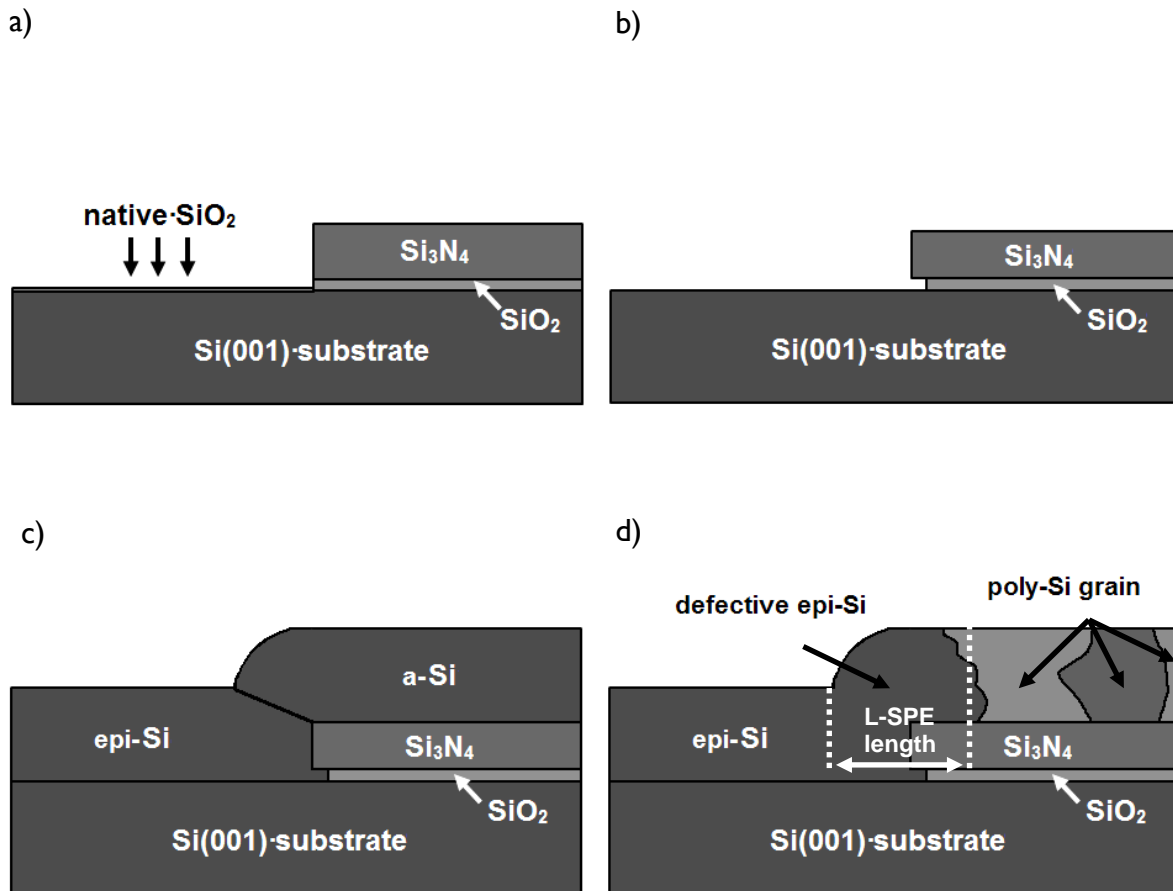
**For emitter region:** For better understanding of the following workflow, Figure 27 shows a schematic diagram of Figure 15 in order to clarify the future scope of the SPE technique on IHP's HBT n-type emitter area [25, 135]:



**Fig.27** Schematic diagram of in Fig. 15 depicted IHP's HBT construction. The inset (in red frame) enlarged the scope of the SPE in the epi-/poly-Si emitter area. Red dotted line indicates the transition border between epi- and poly-Si and between epi- and a-Si during differential Si growth with  $\text{SiH}_4$  and  $\text{Si}_2\text{H}_6$  gas, respectively. Bold blue arrow shows the desired lateral SPE direction [25, 135].

As mentioned before in section 1.4.1, the standard  $\text{SiH}_4$  grown emitters produce during differential Si deposition by RPCVD in the channel window an epi-Si and on the  $\text{SiO}_2/\text{Si}_3\text{N}_4$ -mask a poly-Si area (see inset in Fig. 27). However, the use of  $\text{Si}_2\text{H}_6$  combined with lower deposition temperatures changes the poly-Si on the  $\text{SiO}_2/\text{Si}_3\text{N}_4$ - mask to a-Si (written in blue in Fig. 27). This enables the application of SPE techniques in order to create a lateral crystal overgrowth and finally a fully epi-Si n-type emitter (indicated by bold blue

arrow in Fig. 27 inset). In order to find appropriate process conditions for SPE, experiments on the following model structures were carried out.



**Fig.28** Schematic diagrams of used  $\text{SiO}_2/\text{Si}_3\text{N}_4$ -patterned  $\text{Si}(001)$  substrate **(a)** before and **(b)** after cleaning procedure. Schematic illustration of **(c)** sample as-deposited with  $\text{Si}_2\text{H}_6$  at  $575^\circ\text{C}$  and **(d)** sample deposited with  $\text{Si}_2\text{H}_6$  at  $575^\circ\text{C}$  followed by postannealing [119].

As-doped a-Si/epi-Si deposition: The deposition of a-Si/epi-Si as well as the SPE procedure was carried out by using the lamp-heated ASM 2000 RPCVD single wafer system (see section 2.1). As substrates, on-oriented  $\text{Si}(001)$  wafers (200 mm size) with a combined mask of 15 nm  $\text{SiO}_2$  with 50 nm  $\text{Si}_3\text{N}_4$  on top were used (shown in Fig. 28(a)). Before deposition, the patterned Si wafers were chemically cleaned in a standard Radio Corporation of America (RCA) solution (including a HF last clean). This procedure removes the native  $\text{SiO}_2$  in the window area. Additionally, a small underetching of the  $\text{Si}_3\text{N}_4/\text{SiO}_2$ -mask is observed (see Fig. 28(b)). After loading the substrates into the RPCVD reactor, prebaking at  $850^\circ\text{C}$  in  $\text{H}_2$  was performed to remove the regrown native oxide, followed by the deposition process.  $\text{H}_2$  was applied as carrier gas for  $\text{Si}_2\text{H}_6$  as reactant gas and  $\text{AsH}_3$  as dopant gas source. For the

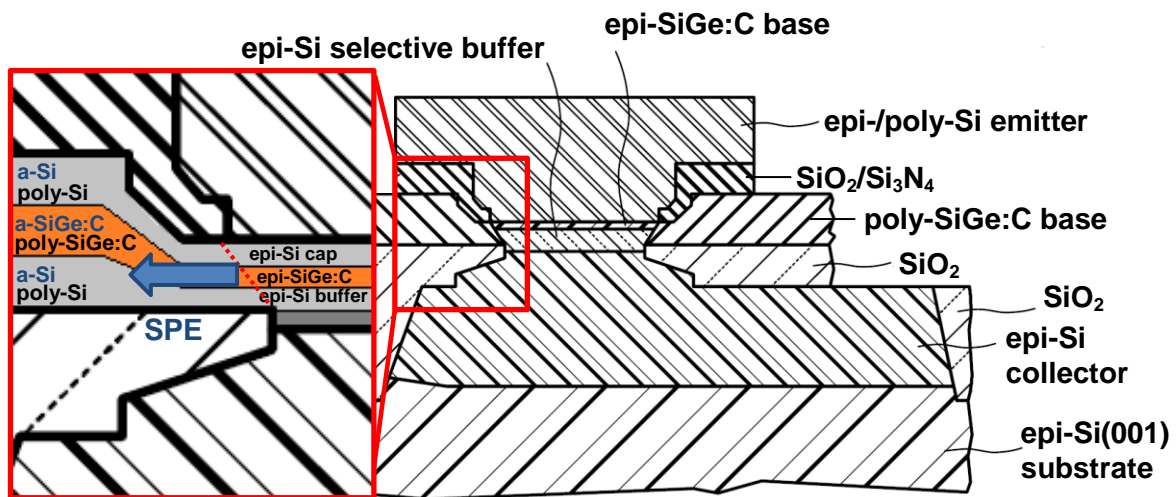
deposition process, 575 °C and 550 °C were chosen as growth temperatures to study the impact of temperature on the initial state poly-grain formation on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>-mask. In both cases, the thickness of deposited As-doped Si was adjusted to 140 nm epi-Si on Si in the window area. In the same time 200 nm thick As-doped a-Si were grown on SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>-mask (Fig. 28(c)). This difference in the thickness of the entire deposited As-doped Si film is due to the different growth rate of epi-Si and a-Si (see Fig. 86 in Appendix).

SPE: Lateral SPE (L-SPE) overgrowth of the deposited As-doped a-Si on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>-mask was induced by postannealing the samples in-situ inside the RPCVD chamber (visible in Fig. 28(d)). Two different experimental conditions were investigated there: One high temperature annealing in the range of 700 – 1000 °C for 60 sec and one low temperature annealing at 575 °C for up to 120 min. During the SPE process, the samples remained always under steady H<sub>2</sub>-flow and were kept at a reduced pressure range. The doping concentration in the above-mentioned two experimental conditions were also altered in order to investigate the influence of the As doping on SPE.

Sample Characterization: The concentration profile of As-dopant in Si was measured by SIMS method. Cross section TEM and SEM were applied to investigate the crystal quality particularly in the high temperature experiment and the mean L-SPE crystallisation length in all experiments. The L-SPE domain length was determined starting from the edge of the epitaxial grown Si until transition to the simultaneously formed poly-Si grain domain on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>-mask (indicated in Fig. 28(d)). Because the crystallisation front of the L-SPE is not straight and parallel to the sidewall, we determined also a variation interval by angle view SEM images. The selective vapor phase etching of a-Si by HCl was performed at 575 °C at atmospheric pressure to emphasize and analyse the poly-grain growth on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>-mask [120]. More information about the used measurement techniques and tools can be found in section 2.2.

**For base region:** For better understanding of the following workflow, Figure 29 shows a schematic diagram of Figure 15 in order to clarify the future scope of the SPE technique in the first place on IHP's HBT undoped Si base cap layer and finally on the whole undoped Si-buffer/p-doped SiGe:C base/undoped Si-cap layer stack [25, 135].

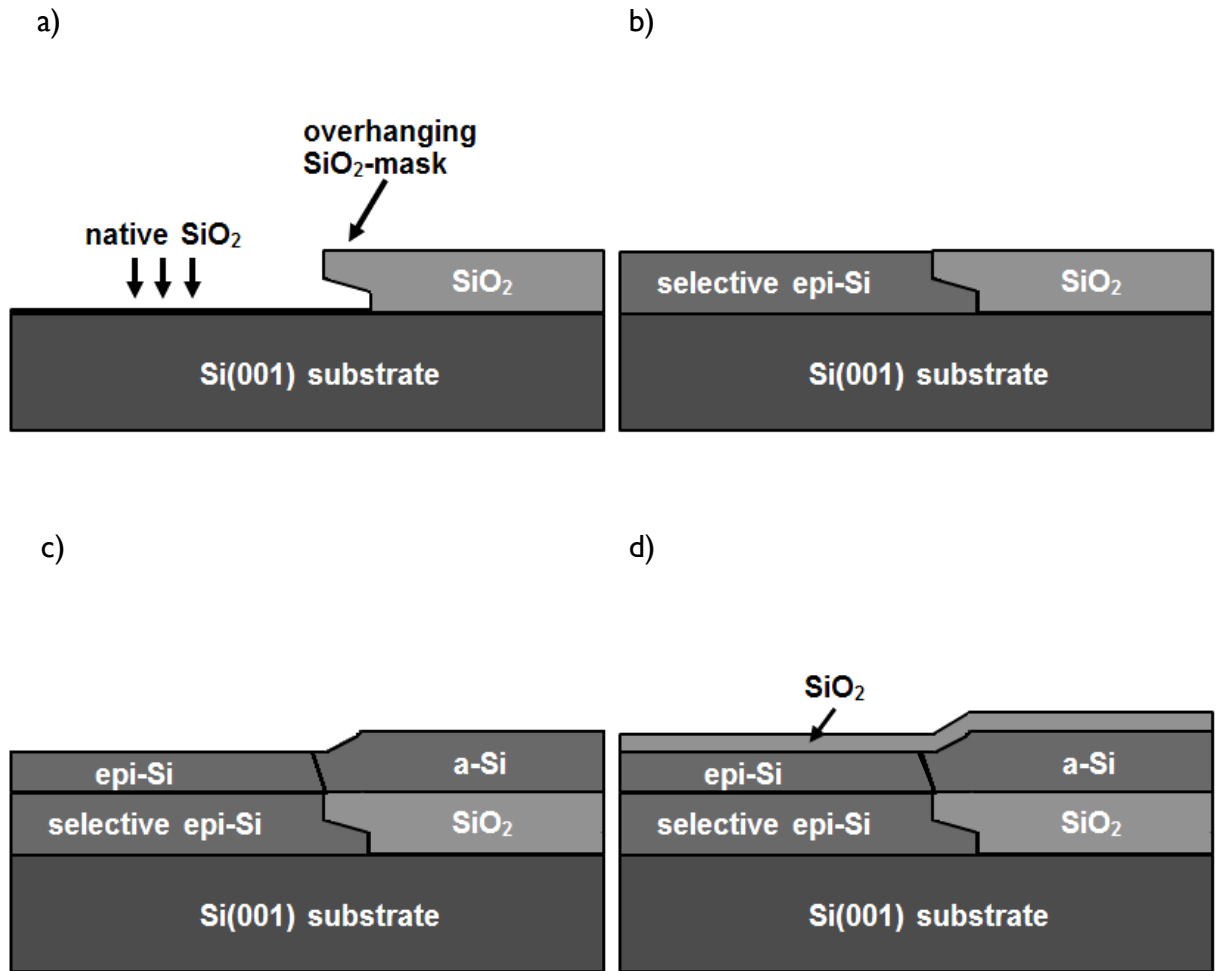
As mentioned before in section 1.4.1, the standard SiH<sub>4</sub> grown base stack (consisting of undoped Si buffer layer, p-type SiGe:C base and undoped Si cap layer) produce during differential Si and SiGe:C deposition by RPCVD in the channel window an



**Fig.29** Schematic diagram of in Fig. 15 depicted IHP's HBT construction. The inset (in red frame) enlarged the scope of the SPE in the epi-/poly-Si base area. Red dotted line indicates the transition border between epi- and poly-Si and between epi- and a-Si during differential Si growth with  $\text{SiH}_4$  and  $\text{Si}_2\text{H}_6$  gas, respectively. Bold blue arrow shows desired lateral SPE direction [25, 135].

epi-Si/epi-SiGe:C/epi-Si and on the  $\text{SiO}_2$ -mask a poly-Si/poly-SiGe:C/poly-Si area (see inset in Fig. 29). However, the use of  $\text{Si}_2\text{H}_6$  combined with lower deposition temperatures changes the poly-Si/poly-SiGe:C/poly-Si on the  $\text{SiO}_2$ -mask to a-Si/a-SiGe:C/a-Si (blue written in Fig. 29). This enables the application of SPE techniques in order to create a lateral crystal overgrowth in order to change the base link region on the  $\text{SiO}_2$ -mask to an epitaxial base layer stack (indicated by bold blue arrow in Fig. 29 inset). The experiments started with the investigation of appropriate process conditions for SPE of undoped Si on the following model structures. Optimised process conditions were transferred in the end for the whole base layer stack.

Undoped a-Si/epi-Si deposition: Similar to the previously described emitter part, both deposition processes of a-Si/epi-Si and SPE of deposited a-Si on  $\text{SiO}_2$ -mask were also carried out by using the same lamp-heated single wafer RPCVD system (see section 2.1). As substrates, on-oriented Si(001) wafers (200 mm size) with an 80 nm thick  $\text{SiO}_2$ -mask on top and a model bipolar window structure with overhanging sidewall for current HBT technology of IHP were used (depicted in Fig. 30(a)) [25]. Before a-Si/epi-Si deposition, the patterned Si(001) wafers were chemically cleaned in a standard RCA solution (including a HF last clean) and selective epi Si (sel. epi-Si) was deposited into the bipolar window at 800 °C by RPCVD using a  $\text{H}_2\text{-H}_2\text{SiCl}_2\text{-HCl}$  gas mixture to planarize the surface of the wafers (see Fig. 30(b)). After this preparation, the actual a-Si/epi-Si deposition could be performed. For



**Fig.30** Schematic diagrams of used SiO<sub>2</sub>-patterned Si(001) substrate with overhanging mask **(a)** before and **(b)** after cleaning procedure and selective Si deposition. **(c)** Schematic illustration of as-deposited sample at 575 °C using Si<sub>2</sub>H<sub>6</sub>. **(d)** Schematic illustration of as-deposited sample at 575 °C using Si<sub>2</sub>H<sub>6</sub> Si gas source with 10 nm SiO<sub>2</sub>-cap [25, 121].

this purpose, the patterned Si(001) wafers were again chemically cleaned in a standard RCA solution (combined with HF last clean). Afterwards, the wet-cleaned Si(001) wafers were loaded into the RPCVD reactor and baked at 850 °C in H<sub>2</sub> in order to form an oxygen-free Si surface. After this step, up to 180 nm Si was deposited differentially at 550 °C using H<sub>2</sub>-Si<sub>2</sub>H<sub>6</sub> gas mixture, creating epi-Si and a-Si on Si and SiO<sub>2</sub> mask, respectively (see Fig. 30(c)). The growth temperature at 550 °C with respect to 575 °C has been chosen due to the higher epitaxial quality of Si<sub>2</sub>H<sub>6</sub>-deposited epi-Si layers on Si at lower temperatures. In contrast to the emitter area, the requirements for crystal quality of base epitaxy in SiGe:C HBTs is much higher. As an optional intermediate process step, the a-Si/epi-Si surface of some samples were fixed by capping with 10 nm SiO<sub>2</sub> deposited at 400 °C by plasma

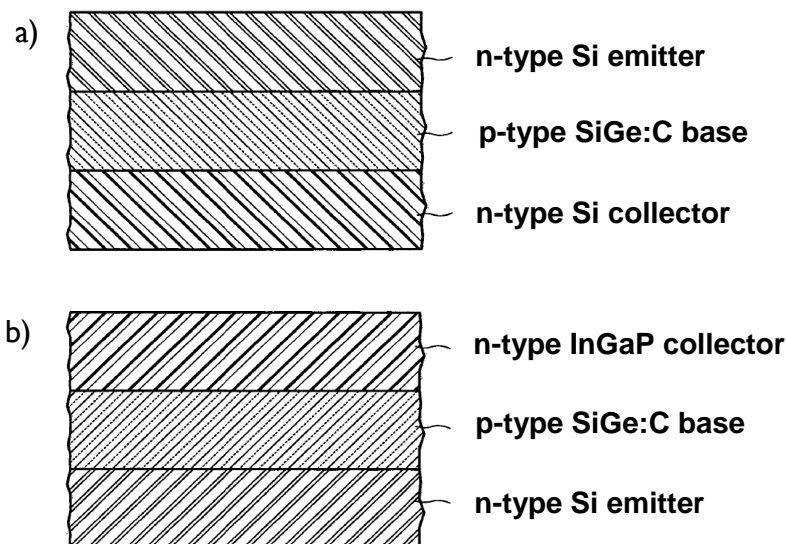
enhanced CVD in order to investigate the influence of surface migration effects on SPE (sketched in Fig.30(d)).

SPE: Directly after a-Si/epi-Si deposition, SPE was induced by in-situ postannealing of the as-deposited samples in the RPCVD chamber. For investigation, postannealing times, temperatures and the deposited a-Si thickness on SiO<sub>2</sub> mask were varied. The RPCVD reactor was always kept under steady H<sub>2</sub>-flow and at reduced pressure during the SPE process.

Sample Characterization: TEM and SEM were used to evaluate the crystallinity and the mean L-SPE crystallization length (see Fig. 28(d)). For the SEM analysis, selective etching of a-Si and poly-Si based on Godbey solution was performed to emphasize the crystallized epi-Si domain and poly-Si grains on the SiO<sub>2</sub>-mask [119, 122-123]. More information about the used measurement techniques and tools can be found in section 2.2.

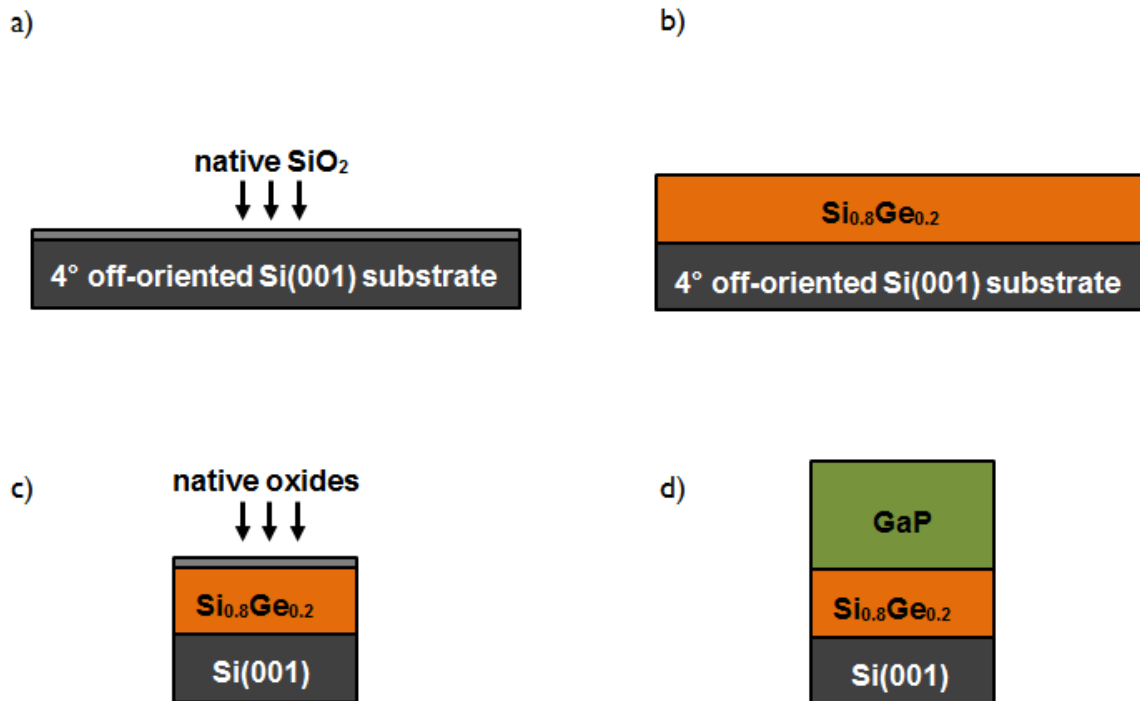
### 2.3.2 In<sub>1-x</sub>Ga<sub>x</sub>P growth studies

For better understanding of the following workflow, it is important to take a closer look into the possible realization of the approach mentioned in section 1.4.2. Figure 31 shows two simplified schematic diagrams of n-p-n type HBTs: One standard HBT stack used in more complex form in today's HBTs (Fig. 31(a)) and another HBT stack inherit with the III-V/SiGe-hybrid collector device approach (Fig. 31(b)) [135]:



**Fig.31** Simplified schematic diagrams of n-p-n HBTs: (a) Standard HBT stack used in more complex form in today's HBTs and (b) HBT stack needed for realization of III-V/SiGe-hybrid collector device [135].

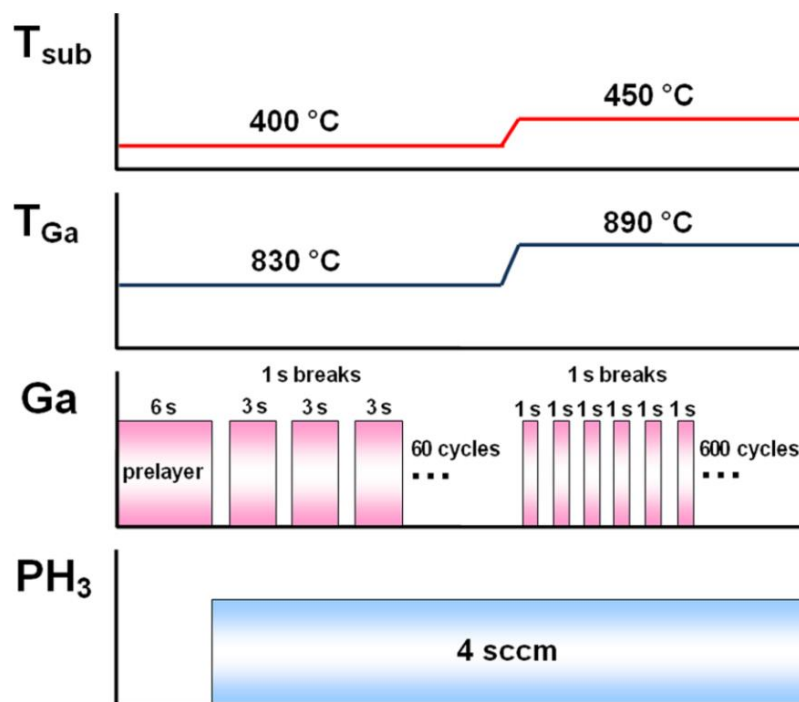
As visible in the diagrams in Fig. 31, in contrast to the standard HBT stack (Fig. 31(a)), collector and emitter are reversed in the III-V/SiGe-hybrid collector device concept (compare Fig. 31(b)). This device modification is probably needed due to the low thermal budget of III-V semiconductor materials (i.e.  $>550^{\circ}\text{C}$  results in GaP decomposition) [136, 137]. For  $\text{SiH}_4$ -based Si and SiGe:C deposition as well as for doping activation, processes with generally higher temperature are required (up to  $1000^{\circ}\text{C}$ ), which would consequently lead to a damage of the III-V layer [18, 25, 45, 46]. For this reason, the layer order with collector on top is maintained in the following heteroepitaxy growth experiments. Finally, it is to mention that GaP was chosen as starting point in the framework of this III-V heterostructure growth study due to its small lattice mismatch with respect to Si (0.36% at 300 K) (Tab. 1).



**Fig.32** Schematic diagrams describing the work flow during the III-V heterostructure growth study with GaP. **(a)** Not cleaned  $4^{\circ}$  off-oriented (towards  $\langle 110 \rangle$  Si(001) substrate. **(b)** Sample after cleaning and 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$  deposition using RPCVD at IHP. **(c)** As-deposited  $4^{\circ}$  off-oriented  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrates cut in  $1 \times 1 \text{ cm}^2$  pieces after transport and before cleaning at HU Berlin. **(d)** GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure after 270 nm deposition of GaP using GSMBE at HU Berlin [90].

SiGe deposition: The deposition of SiGe was performed by the lamp-heated RPCVD single wafer system at IHP (see section 2.1). As substrate material, Si(001) wafers (200 mm size) with  $4^{\circ}$  off- (towards  $\langle 110 \rangle$ ) orientation were used (depicted in Fig. 32(a)). Before executing SiGe growth, the Si(001) substrates were wet chemically cleaned in a standard

RCA solution. After wet-cleaning, the surface of the Si(001) substrate was covered by a defined SiO<sub>2</sub> layer, which was removed in the following by initiating a prebake inside the RPCVD reactor at 1000 °C for 10 min in H<sub>2</sub>. This rather long annealing time was necessary to additionally ensure the creation of preferred double atomic steps on the surface [124-126]. Next, 20 nm pseudomorphic Si<sub>0.8</sub>Ge<sub>0.2</sub> (i.e. 20% Ge-content in SiGe) were grown by RPCVD on top of Si(001) wafers at 600 °C growth temperature and 80 Torr chamber pressure. As carrier gas H<sub>2</sub> was applied for the reactant gas sources SiH<sub>4</sub> and GeH<sub>4</sub> (see Fig. 32(b)) [90].



**Fig.33** Deposition process for 170 nm GaP growth on pseudomorphic 4° off-oriented Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001), displaying substrate temperature ( $T_{\text{sub}}$ ), Ga crucible temperature ( $T_{\text{Ga}}$ ), Ga pulse program, and PH<sub>3</sub> gas flow. [90].

GaP deposition: Before GaP deposition using GSMBE, the at IHP prepared 4° off-oriented 200 mm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrates have to be cut in 1x1 cm<sup>2</sup> pieces and transferred to HU Berlin. After transport to HU Berlin, a native oxide layer is formed again on top of the Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrates. Therefore, the samples were again wet chemically cleaned in standard RCA solution (with HF last clean) and then placed in the GSMBE system for two bake outs. The first bake out at 200 °C took place in the loading chamber for 1 hour in order to remove remaining moisture. The second bake-out was performed in the growth chamber at 800 °C for 15 min with the intention to remove eventual SiO<sub>2</sub> debris and to ensure again the creation of preferred double atomic steps on the 4° off-oriented Si<sub>0.8</sub>Ge<sub>0.2</sub> surface. Using off-oriented substrates (associated with a bake-out) is a well-known method



to reduce APD formation during III/V-deposition on Si(001) [92-94, 124, 125, 129, 131, 132]. After these pretreatments, 170 nm GaP was finally deposited on top of Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrates using PH<sub>3</sub> thermally cracked at 920 °C and elemental Ga as source materials (see Fig. 32(d)). The temperature and dose profile of the GaP growth procedure is shown in Fig. 33 [90]. The GaP deposition process was started with the creation of a 2-monolayer (ML) Ga prelayer by opening the shutter for 6 sec at Ga temperature ( $T_{\text{Ga}}$ ) of 830 °C and substrate temperature ( $T_{\text{sub}}$ ) of 400 °C. Afterwards, continuous gas flow of 4 sccm PH<sub>3</sub> was applied. Further GaP growth was initiated by two successive growth steps: In the first low-flux growth step, the adjusted  $T_{\text{Ga}}$  and  $T_{\text{sub}}$  parameters were kept constant and a growth cycle with a 3 sec open Ga shutter and a subsequent one sec break for altogether 60 cycles was used to grow a closed GaP seed layer. In the second high-flux growth step for faster GaP growth the temperature for Ga crucible and substrate were increased to 890 °C and 450 °C respectively, using this time a growth cycle with a rotation of one sec open Ga shutter and a subsequent one sec break for all 600 remaining cycles [90].

Sample Characterization: XRD was applied on the GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure to investigate the epitaxial relationship, the strain relaxation degree and microtwin (MT) defects. By using an additional furnace, which was mounted on the XRD, it was possible to perform a thermal expansion coefficient study. AFM and TEM were used to gain additional information about surface topography, crystal quality and defect formation. DF HRTEM imaging was performed to analyze presence and distribution of APDs. More information about the used measurement techniques and tools can be found in section 2.2.

### 3. Result part

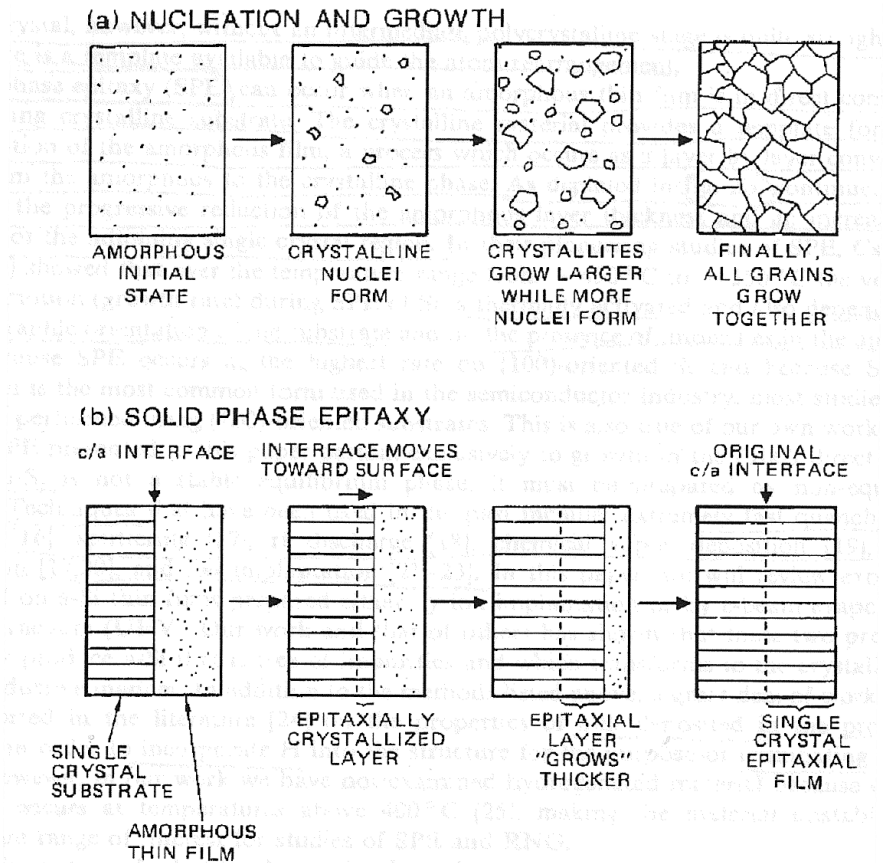
#### 3.1. Solid-phase epitaxy for emitter and base resistivity

##### 3.1.1 Solid-Phase Epitaxy

The introduction of  $\text{Si}_2\text{H}_6$  (instead of standard  $\text{SiH}_4$ ) as RPCVD process gas in hand with SPE applications forms the core of this result part (remember 1.4.1). For better understanding of the following SPE results, a brief overview of this crystal growth technique is cited here.

As special growth technique, SPE was firstly reported in 1968 by Meyer et al. [69]. Thereto, the tendency of a-Si to crystallize under certain annealing condition was utilized. This tendency appears due to the fact that the free energy (also called Gibbs free energy or free enthalpy) is much lower for the crystalline state than for the amorphous state. It is known that Si forms in solid strongly covalent, directional bonds arranged in a tetrahedral configuration in order to create the condition of minimum free energy. If now this arrangement is extended in three dimensions, the diamond lattice characteristics of epi-Si can be formed. Since the free energy can be decreased by any kind of crystallization, two different effects can appear in the a-Si layer: On the one hand, the nucleation of clusters can take place in the free-standing area, leading into growth of randomly distributed grains and finally in creation of a polycrystalline film. On the other side, SPE can occur in presence of a crystalline template, reordering the amorphous layer structurally onto the crystalline template layer by layer to a monocrystalline layer with the same epitaxial relationship. Figure 34 depict these two solid-phase crystallization processes in a-Si. In conclusion, annealing of a-Si films can produce different kind of effects ranging from epitaxial crystallization (e.g. in SPE) to a complex combination of other solid-phase transformations (e.g. random nucleation and growth (RNS), precipitation, phase separation and defect-enhanced diffusion). Which of these phenomena occur, depend on the applied process parameters (i.e. temperature, pressure, gas environment, specimen...) [70, 142].

The appearing phenomenon is not only determined by the applied process parameters. Pioneering SPE studies revealed that also the velocity of a sharp crystal/amorphous interface towards the free surface (also called SPE growth rate velocity) is thermally activated, and depends on crystallographic orientation of the surface, on non-hydrostatic stress effects, on



**Fig.34** Schematic illustration of solid-phase crystallization processes in a-Si. **(a)** Random nucleation and growth, **(b)** solid-phase epitaxy [70].

presence of hydrogen and on doping [70, 142]. The most important process parameters for SPE are briefly described in the following:

**Implication of temperature:** The influence of temperature over a wide range on the vertical SPE (V-SPE) growth rate velocity can be described by an Arrhenius-type expression [70]:

$$v = v_0 \cdot e^{\left(\frac{-E_a}{k_B T}\right)} \quad (37)$$

where  $v$  is the SPE growth rate velocity,  $E_a$  is the activation energy,  $k_B$  is the Boltzmann's constant, and  $T$  is the temperature. The temperature dependence of SPE in intrinsic films can thus be characterized by a single  $E_a$ , 2.7 eV for Si and 2.0 eV for Ge. In contrast,  $E_a$  for RNS is 4.0 eV. Due to the higher  $E_a$  of RNS relative to SPE, random nucleation becomes a more predominant factor in annealing processes at higher temperatures [70, 142].

**Implications of substrate and orientation:** The SPE growth rate velocity is also dependent to the orientation of the underlying substrate. Studies investigated that e.g. in Si the SPE growth rate velocity changes by about a factor of 20 as the interface orientation is varied. The fastest value was achieved, if the substrate is oriented near (001) and the slowest, if it is oriented near (111). Additionally, studies for SPE growth into lateral direction using patterned substrates revealed that the SPE growth rate velocity along the [010] direction (also called L-SPE) is fourth to eighth times smaller in comparison to the [001] direction (also called V-SPE) [72, 142].

**Implications of the non-hydrostatic stress effect:** By applying non-hydrostatic stress effects, in form of uniaxial tension or uniaxial compression, the SPE growth rate velocity in Si can be enhanced or reduced, respectively. The theoretical explanation for these phenomena is that e.g. tension in the plane of the (001) interface opens up more space for atoms (or better defect) migration towards the interface, enhancing their mobility in the [001] direction only and finally the V-SPE growth rate [142].

**Implications of hydrogen presence:** The SPE growth rate velocity is also affected by hydrogen at the crystal/amorphous interface, which can be already situated there from the beginning or diffuse during annealing through the amorphous layer to this position. The presence of hydrogen retards the SPE growth rate velocity by passivation of dangling bonds, thus reducing the number of crystallization sides available at the crystal/amorphous interface [70, 71].

**Implication of doping:** Depending on intentionally added impurity concentration and dopant material in a-Si films, the character and kinetics of SPE growth can be changed. In the literature can be found that at concentrations  $> 0.1$  at.-% the presence of group III- and group V-dopants can greatly increase the SPE growth rate velocity, whereas non-doping impurities like O, N and C significantly reduce the SPE growth rate velocity. However, if the impurity concentration exceed about 0.3 at.-%, processes such as impurity segregation and precipitation can alter again the crystallization kinetics to the extent that impurities, which increase the SPE growth rate velocity at lower concentrations, can actually retard the rate. These processes are strongly dependent on the applied SPE growth temperature and the diffusion rate of the used dopant material in a-Si. The exact theoretical backgrounds to these processes are still a matter of debate. The most common explanation for dopant-induced enhancement or degradation of SPE growth rate velocity is that the population or mobility of

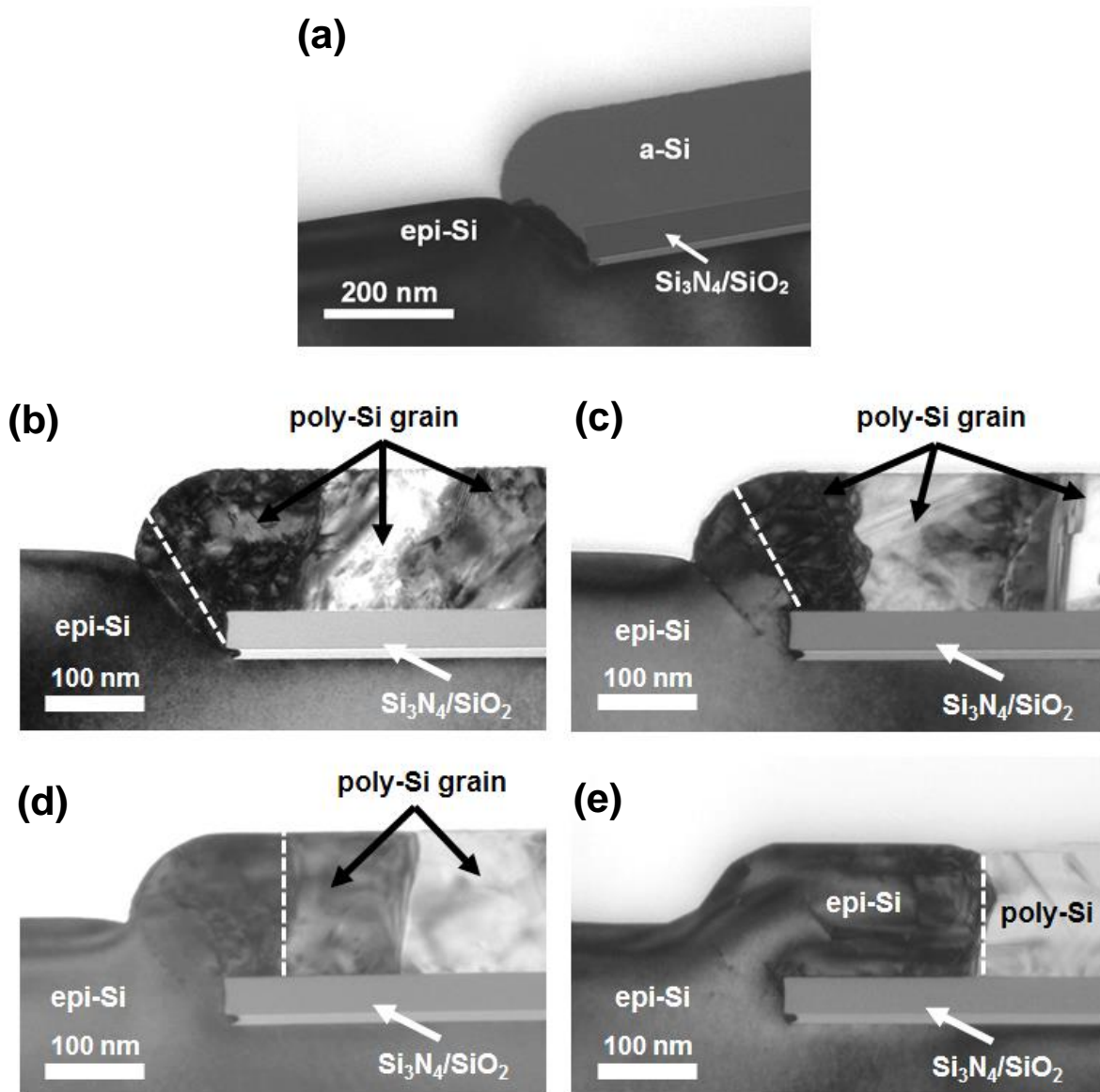
charged dangling bonds at the crystal/amorphous interface could respond to the doping concentration [70, 142].

Using SPE for amorphous to crystalline phase transition is meanwhile a well-known method for reshaping crystal structure during device fabrication. Due to its potential for various applications, e.g. for removal of damage and defects in as-deposited structures, for electrical activation of dopant atoms in as-deposited layers, for realizing silicon-on-insulator (SOI) structures suitable for three-dimensional large scale integrated circuits [72, 73] and for applications like the improvement of polycrystalline silicon thin-film transistor (TFT) technology [74, 75], this method has been under steady investigation. Several experimental results have been reported on vertical and lateral solid-phase crystallization of a-Si so far. These works describe the deposition and preparation of a-Si films on Si and insulating substrates (e.g. SiO<sub>2</sub> or glass) by sputtering [76], vacuum evaporation [72], electron beam [73], and by ion implantation [77], or CVD systems [75, 78, 79]. Two different postannealing methods for formation of epi- and/or poly-Si have been mainly applied: Furnace annealing under non-reactive gas (N<sub>2</sub>, H<sub>2</sub> or Ar) atmosphere [78] and the direct in situ annealing in the deposition vacuum chamber [74, 79]. Because of the low temperature used (about 400 – 600 °C) compared to conventional epitaxial growth or liquid phase techniques, such as laser annealing and a movable-strip heater, which use temperature in the 900 – 1200 °C range, SPE techniques arise still interest for device purposes [78, 80].

### 3.1.2 Experimental studies for emitter application

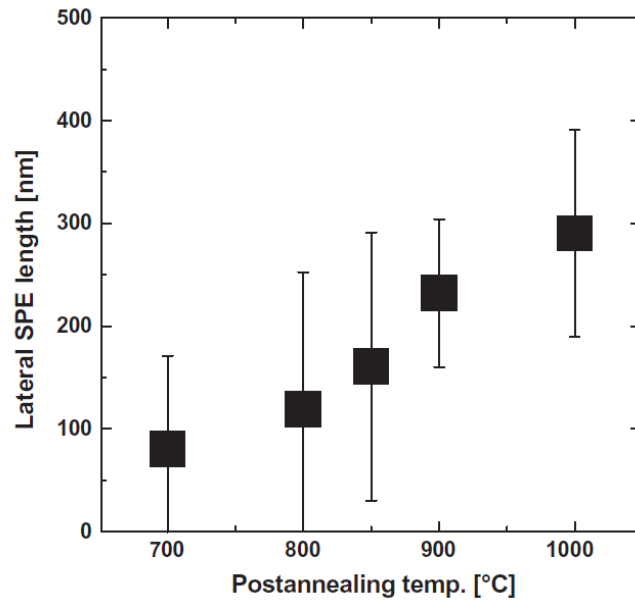
First area of SPE application in this Ph.D. thesis is the highly As-doped Si emitter part of the HBT. Like introduced in 1.4.1, the motivation is to crystallize the Si<sub>2</sub>H<sub>6</sub>-grown a-Si on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>-mask (remember 2.3.1) in order to create a highly As-doped pure epi-Si emitter in contrast to the standard poly-Si emitter grown by SiH<sub>4</sub> (see Fig. 13). In order to investigate this approach, systematic experiments has been undertaken to study the lateral epitaxial overgrowth on the SiO<sub>2</sub>-mask initiated by in-situ SPE inside the RPCVD reactor.

**Temperature dependence:** First, the temperature dependence on L-SPE overgrowth (or length) was investigated. Figure 35 above shows cross-section TEM images of samples as-deposited at 575 °C and postannealed at 700 °C, 800 °C, 900 °C and 1000 °C for 60 sec, respectively. Through the initiation of in-situ postannealing between 700 and 1000 °C for 60 sec in the RPCVD chamber, the earlier a-Si was crystallized: On the one

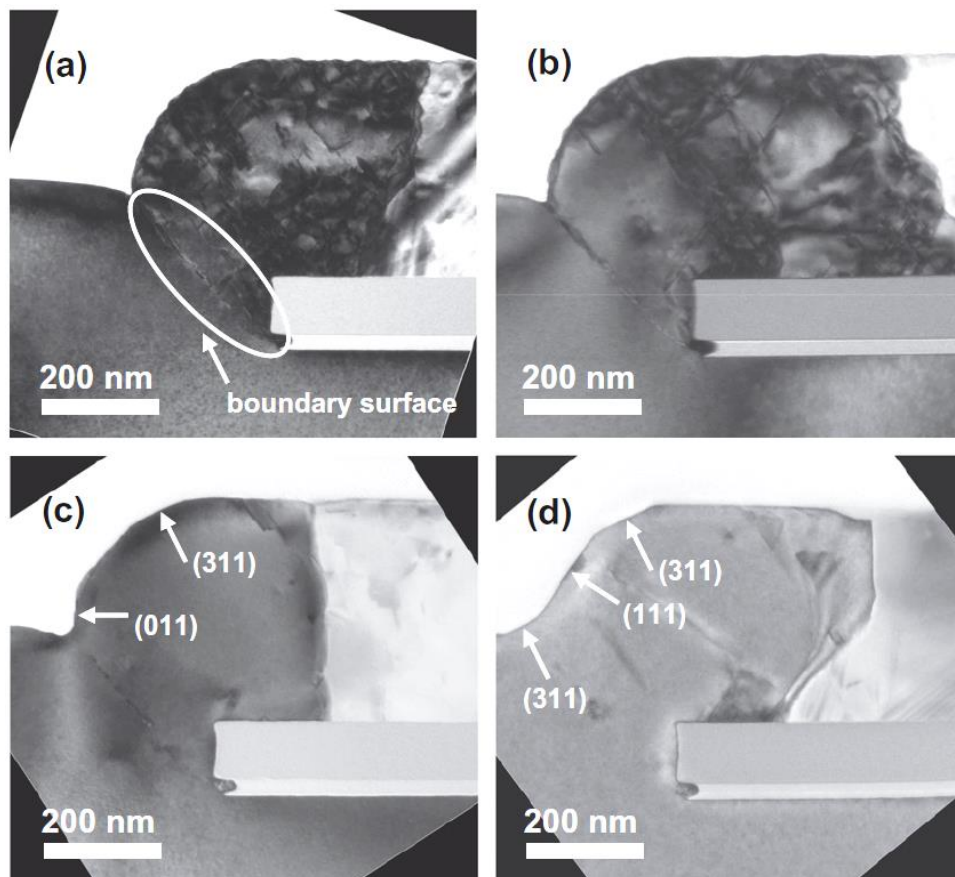


**Fig.35** Cross-section TEM images of samples as-deposited at 575°C (a) and postannealed at 700 °C (b), 800 °C (c), 900 °C (d) and 1000 °C (e) for 60 sec. The dashed lines indicate the individual lateral crystallisation fronts after applying SPE [119].

hand, poly-Si grains were formed on the  $\text{SiO}_2/\text{Si}_3\text{N}_4$ -mask by random crystallisation of introduced growth of nuclei seeds. On the other hand, a-Si was also crystallized by SPE into lateral direction near the sidewall of the mask window. The TEM study revealed that at higher postannealing temperatures the grain size of crystallized poly-Si grains on the mask became larger. One possible interpretation is that Si atoms possess an increased vibration-induced mobility in the solid-phase due to the higher temperature, which favors especially the grain growth rate over the nucleation rate. Figure 36 summarizes the in Fig. 35 observed variation of the L-SPE domain length crystallized by postannealing as a function of the applied



**Fig.36** L-SPE length of crystallized epi-Si vs. postannealing temperature. Annealing time is 60 sec. Si growth temperature was 575 °C. As concentration is  $3 \times 10^{20}/\text{cm}^3$  [119].



**Fig.37** Cross section TEM close-up images of transition area from window to mask after depositing Si at 575 °C and postannealing at (a) 700 °C (b) 800 °C (c) 900 °C and (d) 1000 °C for 60 sec. As-concentration is  $3 \times 10^{20}/\text{cm}^3$ . [119].

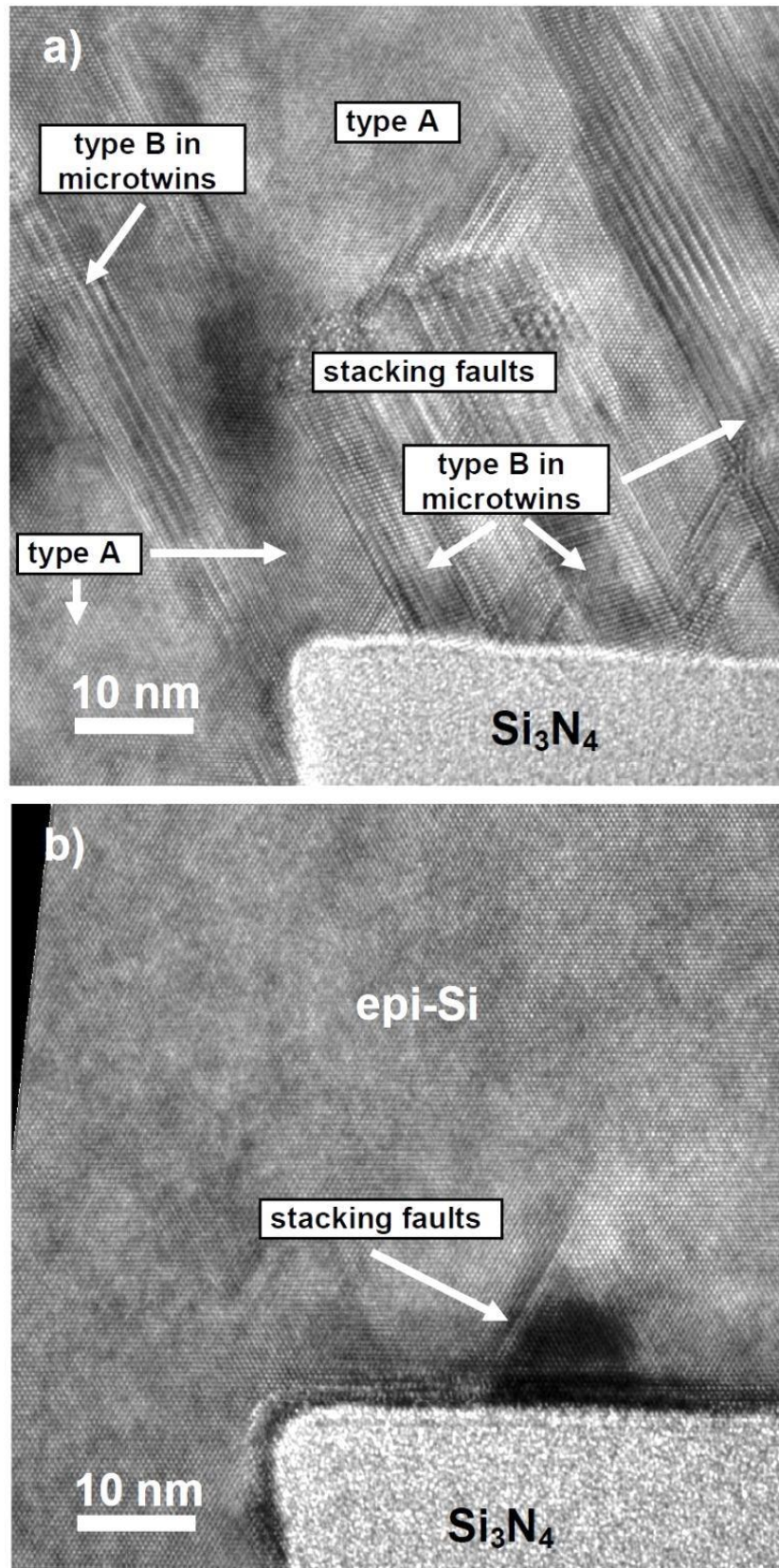
annealing temperature in the range between 700 and 1000 °C. As result, Fig. 36 reveals that the L-SPE length continuously grew with increasing annealing temperature [119].

**TEM crystallinity and defect study:** To discuss crystallinity of crystallized epi-Si domain at the sidewall and on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$  mask in more detail, close-up cross section TEM images after 700 °C, 800 °C, 900 °C and 1000 °C for 60 sec annealing are shown in Fig. 37, respectively. It can be observed that the SPE crystallized epi-Si domain exhibits a high defect density at lower annealing temperatures (Fig. 37(a), (b)), which are reduced by using higher annealing temperatures (Fig. 37(c), (d)). The same thermal behaviour could be observed for the presence of a defect induced boundary surface between the former epi-Si and a-Si domain (shown by oval in Fig. 37(a)). At higher annealing temperature on the sidewall we could also notice facet formation beginning at 900 °C (Fig. 37(c)). (011) and (311) facets are clearly visible and the surface between the facets seems to be reshaping. At postannealing at 1000 °C (Fig. 37(d)), (111) facet is formed under the (311) facet and the (011) facet is replaced by an additional (311) facet. All these facets form only when enough energy is available to reform the surface to an energetic lower condition [119, 134].

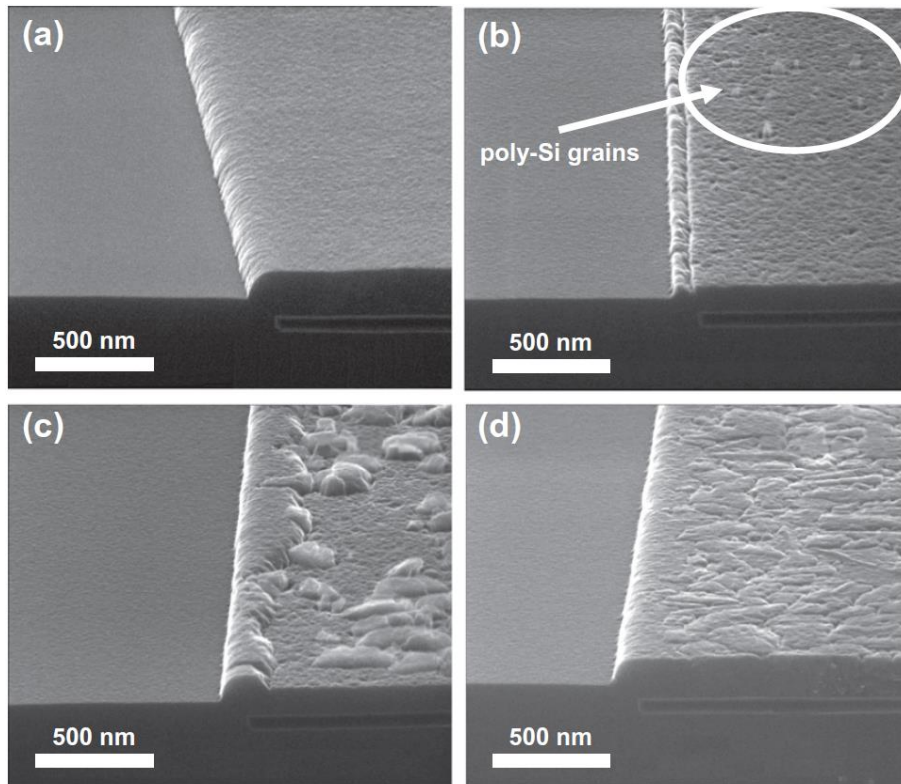
To determine the type of defects in the crystallized epi-Si, HRTEM images of the samples annealed at 800 °C and 1000 °C are shown above (Fig. 38(a), (b)), respectively. In Figure 38(a), many defects are observed in epi-Si domain crystallized by L-SPE at 800 °C, which could be identified as stacking faults (SFs). Due to the SFs the crystal orientation of the defective epi-Si is switching between substrate orientation (type A) and another orientation (type B). These two different orientations are better known as stacking twins or MTs [90, 143]. They are rotated by 180° around a {111} axis, what implies that no clear statement about the orientation of the crystallized SPE region to the Si (001) substrate can be made at lower annealing temperatures. Unlike at higher annealing temperature (e.g. 1000 °C (Fig. 38(b))) we see a clear reduction of defect density; only near the interface to the  $\text{Si}_3\text{N}_4$  mask some SFs remain. The observed sample has the same orientation to the Si (001) substrate and shows no additional types of orientations [119].

**Time dependence:** Next, postannealing at 575°C for longer time intervals was investigated to reduce crystallization kinetics of direct transition from a-Si to poly-Si to the benefit of a-Si to epi-Si interface formation. Figure 39 shows angle view (10°) SEM pictures of as-deposited (Fig. 39(a)) as well as postannealed (0, 0.5 and 2 hours) samples followed by HCl selective etching of a-Si (Fig. 39(b)-(d)). L-SPE length of the samples shown in Fig. 39 as function of time is depicted in Fig. 40. By postannealing at 575 °C, clear reduction of direct

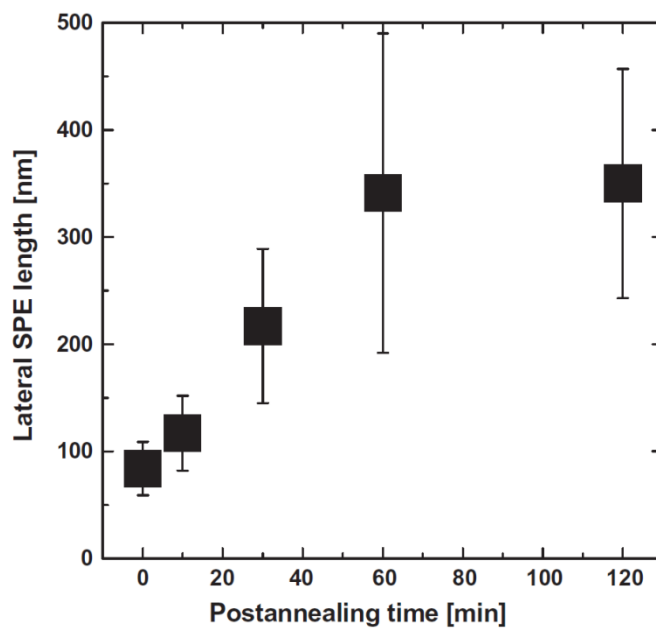




**Fig.38** HRTEM images of SPE crystallized Si on mask of samples deposited at 575°C followed by postannealed at (a) 800 °C and (b) 1000 °C. As concentration is  $3 \times 10^{20}/\text{cm}^3$  [119].



**Fig.39** Cross section SEM pictures of as-deposited **(a)**, with following HCl etching **(b)**, with postannealed (0.5 and 2 hours) and following HCl etched samples **(c and d)**. To emphasize grain formation on mask, selective etching of a-Si at 575 °C was performed. Si growth temperature was 575 °C and As concentration is  $3 \times 10^{20}/\text{cm}^3$  [119].

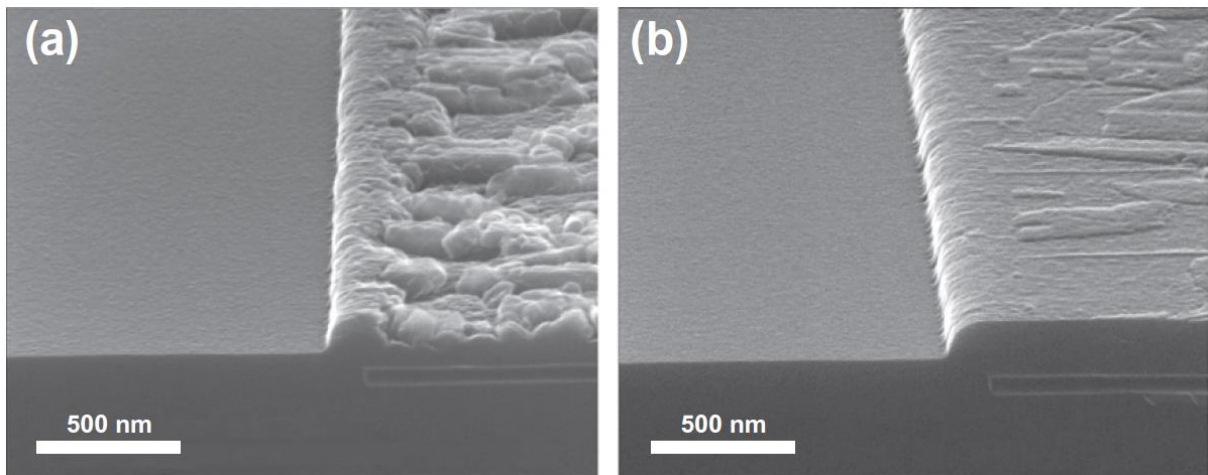


**Fig.40** L-SPE length of crystallized epi-Si vs. postannealing time at 575 °C. Si growth temperature was 575 °C. As concentration is  $3 \times 10^{20}/\text{cm}^3$  [119].

poly-Si formation from a-Si was observed (Fig. 39(a)-(c)). However, that some poly-Si grains (shown by oval in Fig. 39(b)) are already formed and remained before applying postannealing procedure. With increasing time L-SPE domain near the sidewall and poly-grain on the mask grew up and saturate after 1 hour. After that time the separated grown epi-Si and poly-Si grain parts start finally to meet each other and further growth will be retarded (Fig. 39(b)-(d), Fig. 40) [119].

**As concentration dependence:** Next, the influence of As doping concentration in a-Si on L-SPE length is discussed. It is to mention here that the a-Si growth temperature was lowered from 575 °C to 550 °C in this study to prevent possible poly-Si nucleus formation on mask during Si growth (previously highlighted in Fig. 39(b)). Preliminary experiments revealed a low enough influence of As doping on a-Si etch rate, what enabled selective etching of a-Si and poly-Si based on Godbey solution to distinguish the epitaxial domain and a-Si part [119].

To investigate the influence of As doping concentration in a-Si on L-SPE length, As concentration was varied at fixed deposition temperature of 550 °C. Afterwards, samples have been postannealed at 575 °C for 2 hours to initiate solid-phase crystallization. Figure 41 shows, for example, cross section SEM images of two samples with (a) higher ( $4 \times 10^{20}/\text{cm}^3$ ) and (b) lower ( $2 \times 10^{20}/\text{cm}^3$ ) As concentration after applying the postannealing procedure:

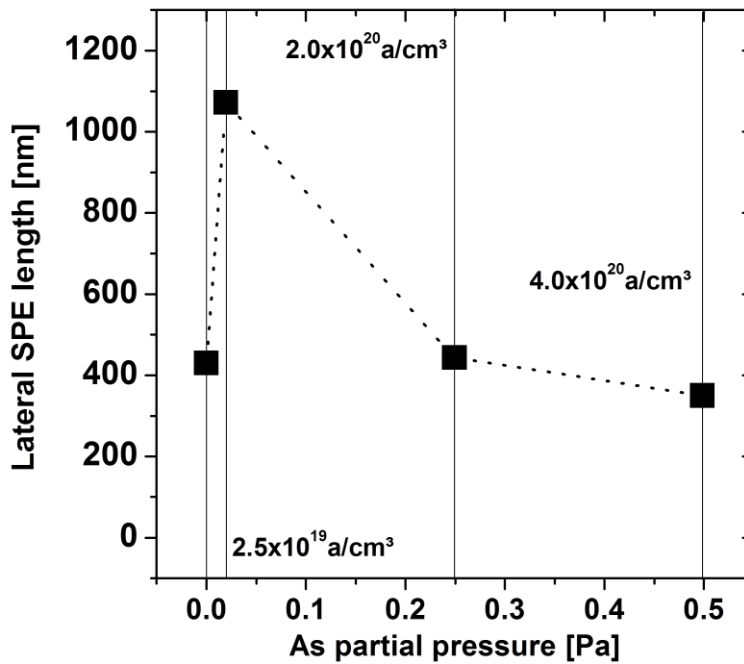


**Fig.41** Cross section SEM pictures of with (a) higher ( $4 \times 10^{20}/\text{cm}^3$ ) and (b) lower ( $2 \times 10^{20}/\text{cm}^3$ ) As concentration grown samples after 2 h annealing at 575 °C. To emphasize grain formation on mask, selective etching of a-Si was performed. Si growth temperature was 550°C [119].

Figure 41 shows that the crystallization behavior of a-Si to epi-Si as well as a-Si to poly-Si are enhanced at the lower As concentration level, resulting in a larger length of L-SPE domain as

well as poly-Si grains on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$ -mask. The observed crystallization behavior can be explained in two possible ways: The first explanation deals with the special SPE growth behavior of As-doped a-Si to epi-Si. Most doping impurities (like for instance P in a-Si [144]) usually enhance the SPE rate and length up to doping concentrations approaching their solid solubility limit. However, *Olsen and Roth* reported first that in As-implanted a-Si the maximum SPE rate and length is located well below the limit in solid solubility. Due to this asymmetry, they suggested that another effect than the simple SPE process takes place. Assuming that the SPE process is controlled in part by the vacancy concentration at the epi-/a-Si interface, As-vacancy-As complexes  $[\text{As}^+-\text{V}_2^--\text{As}^+]$  at the epi-/a-Si interface could be formed at high As concentrations, which would reduce the number of vacancies at the interface. In consequence, the velocity at the epi-/a-Si interface, thus the migration mobility of Si atoms would then increase as the concentration of these complexes is reduced [70, 71, 144]. This means for our case that, at lower As concentrations, the L-SPE rate of a-Si to epi-Si is increased, resulting in larger grown epi-Si domains on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$  mask. The second explanation addresses the formation behavior of random poly grains on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$  mask. Figure 41(b) shows that at lower As concentrations the poly-Si grain size on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$  mask increases. This observation indicates therefore a reduced number of formed random poly grain seeds on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$ -mask for lower As-doped a-Si as well as for undoped a-Si specimen. This means for our case that the L-SPE growth can precede more before being stopped by meeting the separated grown epi-Si and poly-Si grain parts. Accordingly, this described crystallization behavior also results in a larger grown epi-Si domain on the  $\text{Si}_3\text{N}_4/\text{SiO}_2$  mask [119].

For further investigation of the crystallization behavior at 575 °C (for 2 hours) additional experiments have been performed with even lower As concentrations ( $2.5 \times 10^{19}$  atoms/cm<sup>3</sup> and no As doping). The summary of all average L-SPE length results with respect to As concentration is shown in Fig. 42. Figure 42 shows an on-going increase in L-SPE length by reducing As concentration from  $4.0 \times 10^{20}$  atoms/cm<sup>3</sup> to  $2.5 \times 10^{19}$  atoms/cm<sup>3</sup>, supporting the in Fig. 41 observed tendency of enhanced L-SPE length at lower As doping concentration. This tendency abruptly ends when the As concentration is reduced to zero. Due to the observed fact that the poly-Si grain size increases continually from high As concentrations to undoped condition, this behavior can be only attributed to observations that small amounts of impurities (> 0.1 at.-%) enhance the SPE rate and length with respect to undoped a-Si [70, 142]. Thus, it has to be noted that the As asymmetry in L-SPE of a-Si

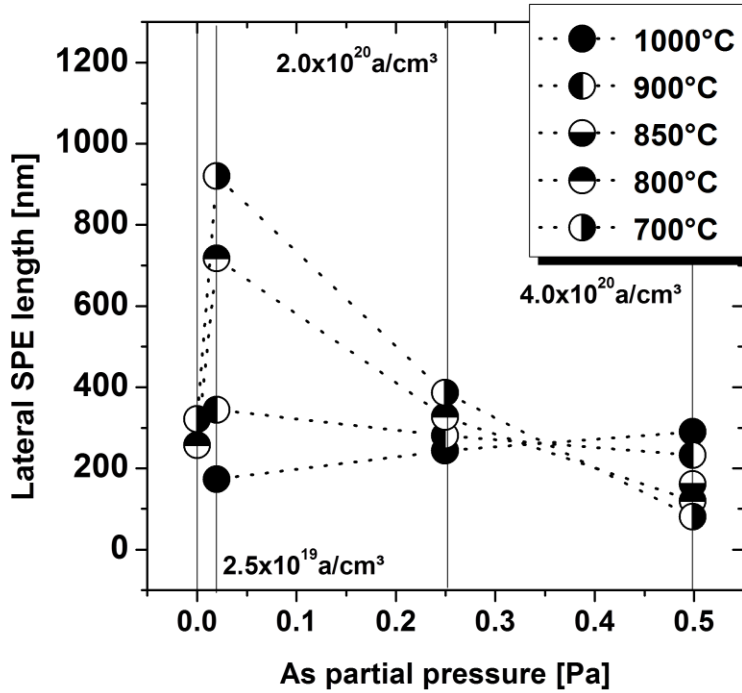


**Fig.42** L-SPE length of crystallized epi-Si vs. As partial pressure annealed at 575 °C for 2 hours. Si growth temperature was 550 °C.

only appears after As doping levels beyond  $2.5 \times 10^{19}$  atom/cm<sup>3</sup>.

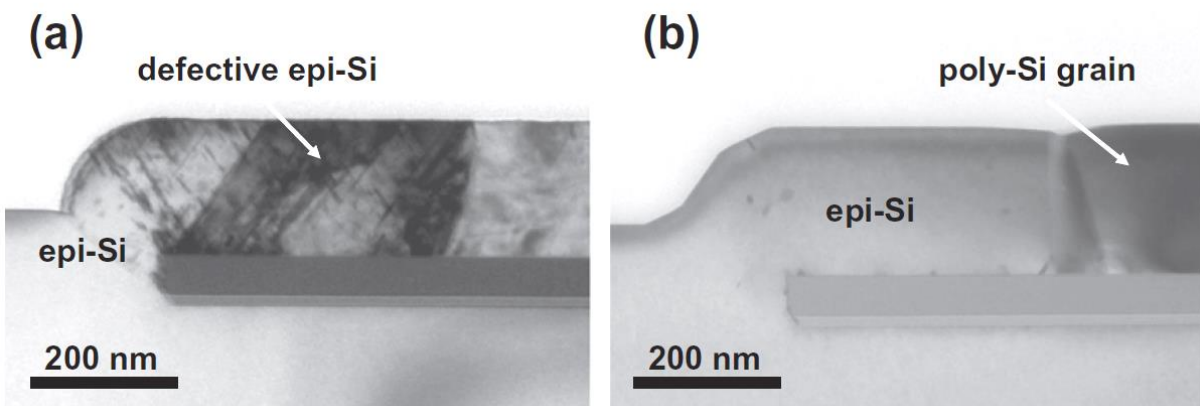
In order to complete the As concentration dependence study, additional experiments with higher postannealing conditions and shorter annealing time (700 – 1000 °C for 60 sec) has also been performed. The results of this part of the study are depicted in Fig. 43. The following conclusions can be drawn from these results:

Firstly, for annealing temperatures between 700 °C – 800 °C, similar dependence like for the case with 575 °C for 2 hours (Fig. 42) can be observed. However, in this temperature area, lower L-SPE length maxima have been achieved for As concentration of  $2.5 \times 10^{19}$  atom/cm<sup>3</sup> with respect to the 575 °C case. This reduced L-SPE lengths at higher temperatures can be explained due to faster growth of poly-Si grains in contrast to L-SPE epi-Si domain on the Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> mask in this temperature range, which hamper further L-SPE growth. Secondly, for annealing temperatures at 900 °C – 1000 °C, the crystallization behavior does not follow anymore the dependence observed in the 575 °C case. While for an annealing temperature of 900 °C the L-SPE length is still slightly decreasing with increasing As concentration, the L-SPE length is continuously increasing at 1000 °C with increasing As concentration. However, despite of the observed increase in L-SPE length



**Fig.43** L-SPE length of crystallized epi-Si vs. As partial pressure annealed at different temperatures for 60 sec. Si growth temperature was 550 °C.

with increasing As concentration, it is to be noted that the achieved L-SPE length maxima values at 1000 °C cannot compete with the values at lower annealing temperatures at As concentration of  $2.5 \times 10^{19} \text{ atom/cm}^3$ . One possible explanation for this behavior is given by *Olsen and Roth*. At 1000 °C the As diffusion in Si could be so high, which results in reduced  $[\text{As}^+ - \text{V}_2^- - \text{As}^+]$  complex creation at the epi-/a-Si interface, which albeit is responsible for lower SPE rates and lengths at high As concentrations.

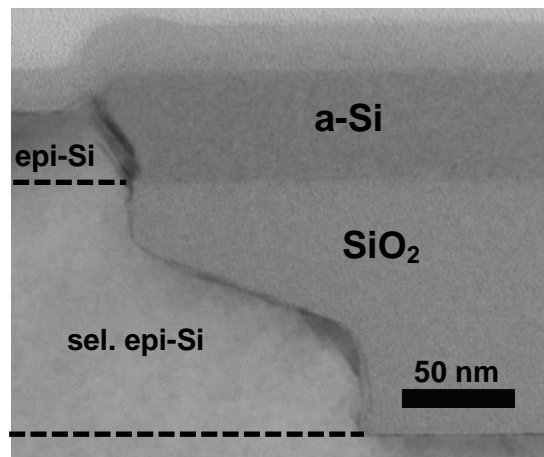


**Fig.44** Crystallized sidewall after postannealing at 575°C, 2 hours (a) and healing annealing step at 1000 °C, 60 sec (b). Si growth temperature was 550 °C and As concentration is  $2 \times 10^{20} / \text{cm}^3$  [119].

After an adequate reduction of As concentration, 500 nm of lateral crystallized epi-Si domain on the sidewall was formed using postannealing at 575 °C for 2 hours, but misfit dislocations (MDs) still remain in the epi-Si domain as expected from the insights discussed here before (Fig. 44(a)). The crystalline quality of the epi-Si domain could be improved by additional annealing step at 1000 °C for 60 sec (Fig. 44(b)). By the combination of two step postannealing at 575 °C and 1000 °C an improvement of L-SPE length and quality of epi-Si on SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>-masks has been demonstrated [119].

### 3.1.3. Experimental studies for base application

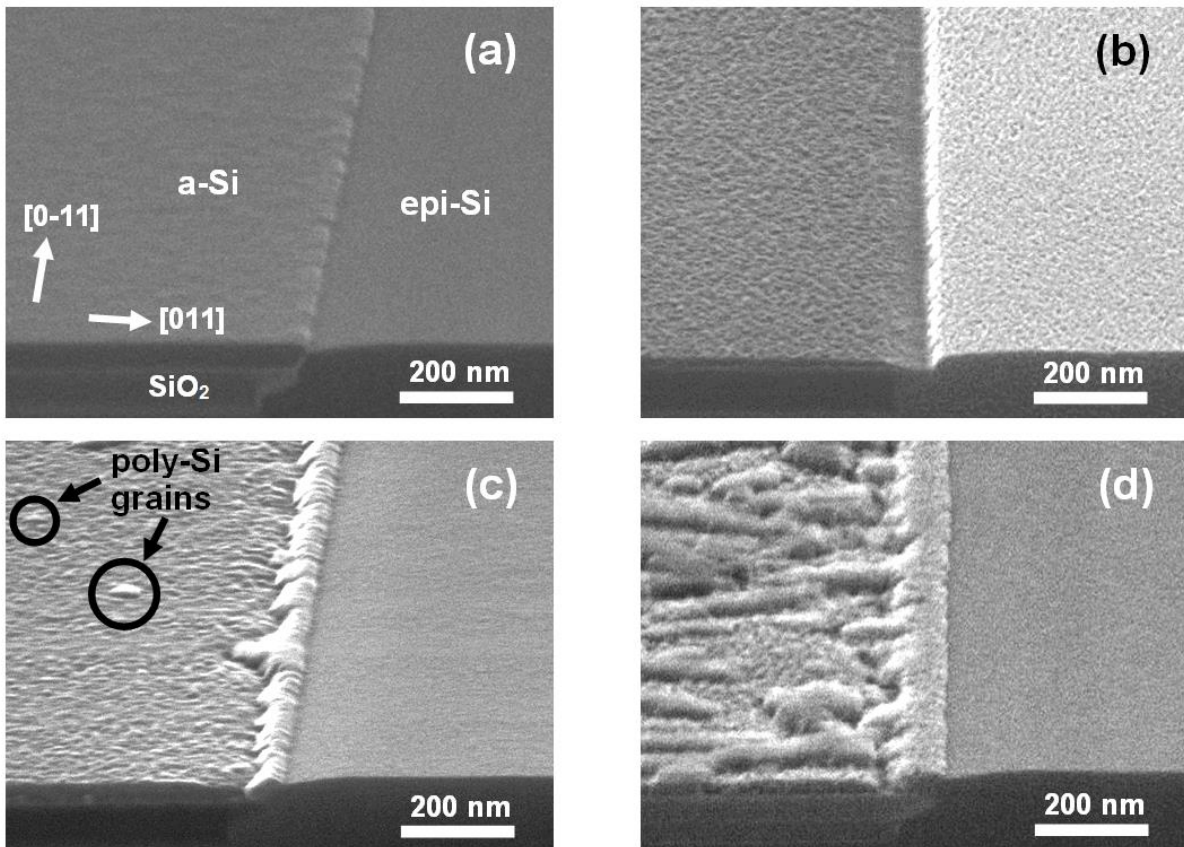
Second area of SPE application in this Ph.D. thesis is the SiGe:C base part of the HBT. Like introduced in 1.4.1, in order to reduce the base link resistivity, the creation of a pure epitaxial undoped Si-buffer/B-doped SiGe:C base/undoped Si-cap base layer stack on SiO<sub>2</sub>-mask (remember 2.3.1) in contrast to the standard polycrystalline equivalents grown by SiH<sub>4</sub> (see Fig. 15) is investigated. For this, the SPE technique has been used to study in the first place the crystallization of Si<sub>2</sub>H<sub>6</sub>-grown, undoped a-Si on SiO<sub>2</sub>-masks depicted in Fig. 45 and Fig. 46(a). Finally, the SPE application on the full undoped Si-buffer/B-doped SiGe:C base/undoped Si-cap base layer stack. In the following, the results of this SPE study performed in-situ inside the RPCVD reactor are presented [121].



**Fig.45** Cross-section TEM Schematic illustration of as-deposited sample at 575 °C using Si<sub>2</sub>H<sub>6</sub> as Si gas source. A-Si thickness on SiO<sub>2</sub> mask is 50 nm.

**Time and temperature dependence:** Before introducing the SPE process, selective etching on as-deposited samples was performed indicating no crystallization of a-Si

at the sidewall or formation of poly-Si grain seeds on the mask during deposition process, like shown in Fig. 46(b). By applying in-situ postannealing at 550 °C in the RPCVD chamber, a-Si was crystallized laterally near the sidewall of the mask window (Fig. 46(c)). On SiO<sub>2</sub> mask few scattered poly-Si grains could be observed originating from random crystallization of grown nuclei seeds there. With increasing postannealing time, crystallized Si domain near the sidewall grew up. Additionally, poly-Si grain formation and poly-Si grain size becomes larger on the mask (Fig. 46(d)) [121].

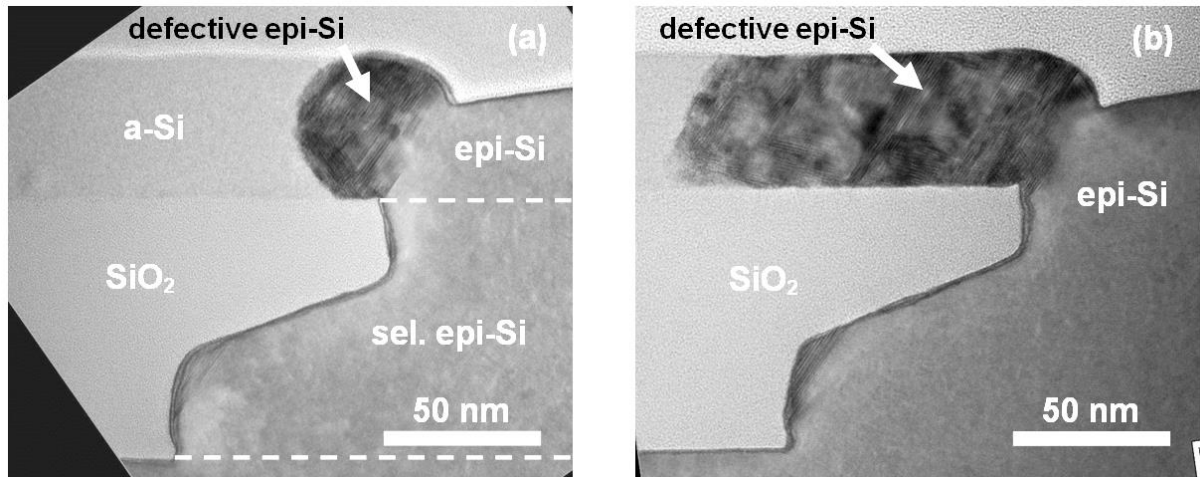


**Fig.46** Angle view (10°) SEM pictures of as-deposited (a), with following Godbey etching (b), as well as postannealed at 550 °C (2 hours and 5 hours) and Godbey etched samples (c)-(d). Si thickness on mask is 50 nm. Godbey etching of a-Si was performed at room temperature [121].

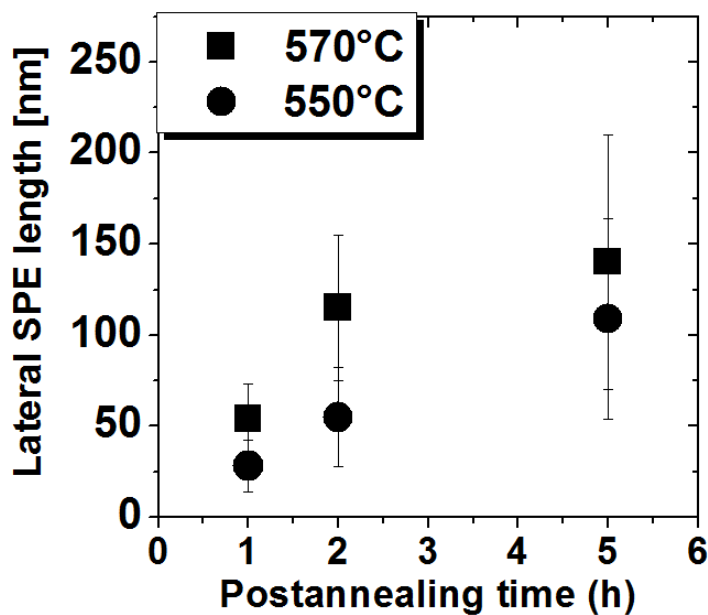
To determine both crystallinity of crystallized epi-Si domain and their dependence on various postannealing temperatures, cross-section TEM images after 550 °C and 570 °C for 2 hours are shown in Fig. 47, respectively. This postannealing temperature region was chosen due to preliminary experimental results with higher postannealing temperatures, which showed an undesirable increase in surface roughness and a SPE obstructing full formation of poly-Si on the mask. Figure 47(a) revealed that the before in SEM observed crystallized Si domain near the sidewall (Fig. 46(c)) is epi-Si, but exhibits still a lot of defects.



Increasing postannealing temperature from 550 °C to 570 °C extends the L-SPE length of crystallized epi-Si, but does not improve the crystallinity after postannealing (Fig. 47(b)). For both cases, a-Si domain is still remaining on the SiO<sub>2</sub>-mask. Therefore, the L-SPE rate is increased by increasing the temperature. In Figure 48, L-SPE length is improved with increasing postannealing time. As discussed in Fig. 47, higher postannealing temperature results in higher L-SPE rate, but in the case of 5 hours postannealing, the temperature



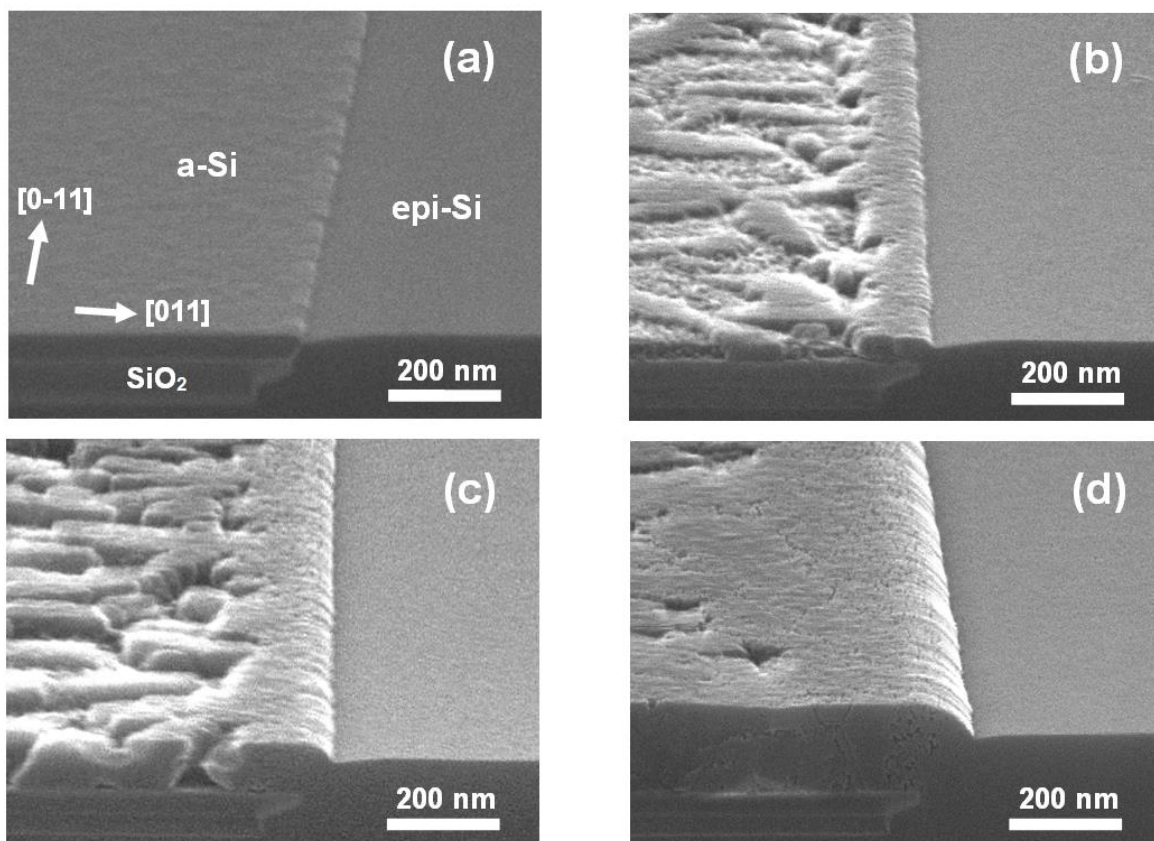
**Fig.47** Cross section TEM images of samples postannealed at 550 °C (a) and at 570 °C (b) for 2 hours. Si thickness on mask is 50 nm [121].



**Fig.48** Lateral SPE length evaluated by TEM/SEM vs postannealing time for 550 °C and 570 °C postannealing temperature. Si thickness on mask is 50 nm [121].

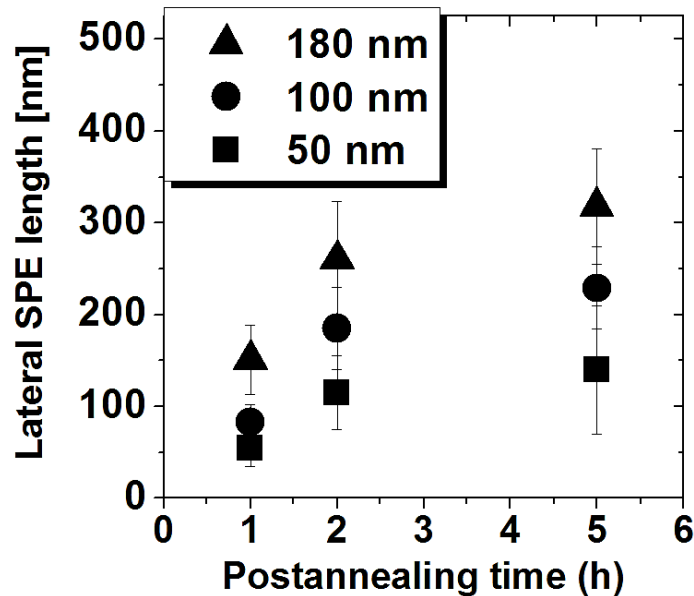
dependence becomes smaller. It is expected that further improvement in L-SPE length will be retarded due to possible obstructing poly-grain formation on mask. The maximum L-SPE lengths after 5 hours are  $109 \text{ nm} \pm 55 \text{ nm}$  and  $140 \text{ nm} \pm 70 \text{ nm}$  for postannealing at  $550 \text{ }^\circ\text{C}$  and  $570 \text{ }^\circ\text{C}$ , respectively [121].

**Thickness dependence:** Next, the influence of a-Si layer thickness deposited on  $\text{SiO}_2$ -mask on the L-SPE length of crystallized epi-Si domain is discussed. Figure 49 shows angle view SEM pictures of as-deposited sample (Fig. 49(a)) as well as samples postannealed at  $570 \text{ }^\circ\text{C}$  for 2 hours with various a-Si thicknesses (50 nm, 100 nm and 180 nm) on the mask (Fig. 49(b)–(d)). To visualize L-SPE length and poly-Si formation on mask after applying postannealing, etching in Godbey solution was performed. The introduced SPE process lead to growth of crystallized epi-Si domain near the sidewall and poly-Si grains on the mask, as observed before in Fig. 46. For larger a-Si layer thicknesses on mask, the L-SPE length of crystallized epi-Si is increased. The developed poly-Si grains become also larger for thicker a-Si (Fig. 49(b)–(d)) and they are almost coalesced at 180 nm (Fig. 49(d)) [121].



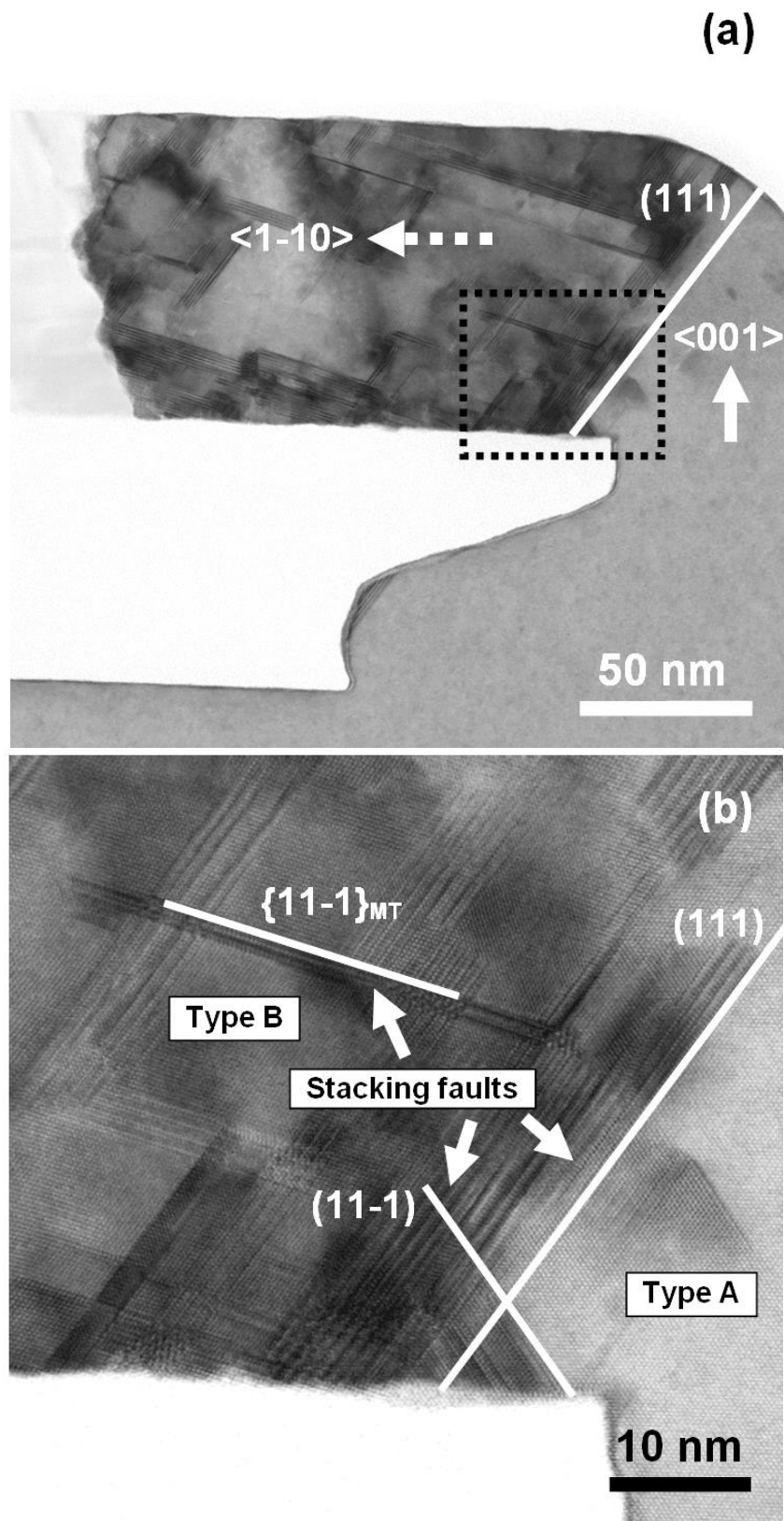
**Fig.49** Angle view ( $10^\circ$ ) SEM pictures of as-deposited (a) as well as postannealed at  $570 \text{ }^\circ\text{C}$  for 2 hours and Godbey etched samples with 50 nm (b), 100 nm (c) and 180 nm (d) Si thickness on mask. Si growth temperature was  $550 \text{ }^\circ\text{C}$ . Godbey etching of a-Si was performed at room temperature [121].

L-SPE lengths determined from Fig. 49 as well as from 1 hour and 5 hour postannealing experiments are summarized as function of postannealing time in Fig. 50. However, even with increasing postannealing time, the maximum length of L-SPE seems to be limited because of the crystallization front of epi-Si domain reaches to the randomly growing poly-Si grains [121].



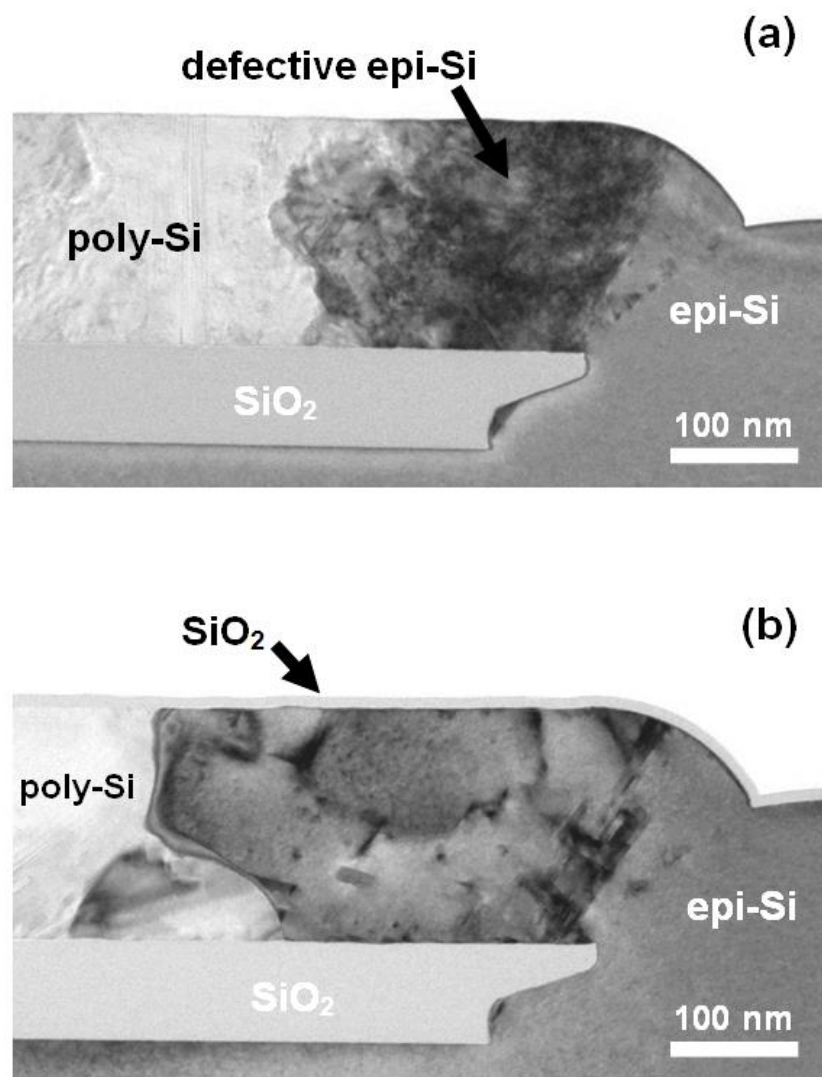
**Fig.50** Lateral SPE length vs postannealing time at 570 °C for 50 nm, 100 nm and 180 nm Si thicknesses on mask evaluated by TEM/SEM [121].

**TEM defect study:** To discuss the crystallinity of by SPE crystallized epi-Si domain in more detail as well as the appearing types of defects, cross section HRTEM images of a sample with a-Si thickness of 100 nm on mask annealed at 570 °C for 5 hours are displayed in Fig. 51. In Figure 51(a), the crystallized epi-Si at the inside of the mask window shows a high crystal quality with only few defects. This result indicates a well achievable V-SPE along the  $\langle 001 \rangle$  direction (bold arrow) with a low defect density. Otherwise, many defects appear in epi-Si domain crystallized on the  $\text{SiO}_2$  mask, which could be identified as SFs. It seems to be more difficult to achieve a concurrent L-SPE along the  $\langle 1-10 \rangle$  direction (dashed arrow) on the  $\text{SiO}_2$  mask. Figure 51(b) shows an enlarged high resolution TEM image of dashed rectangle in Fig. 51(a). The boundary surface between low and high defect density is close to the (111) surface, which is a preferred orientation for MT formation [121, 143].



**Fig.51** Cross section TEM image (a) HRTEM close-up image (b) of crystallized sidewall after postannealing at 570 °C for 5 hours. Si thickness on mask is 100 nm [121].

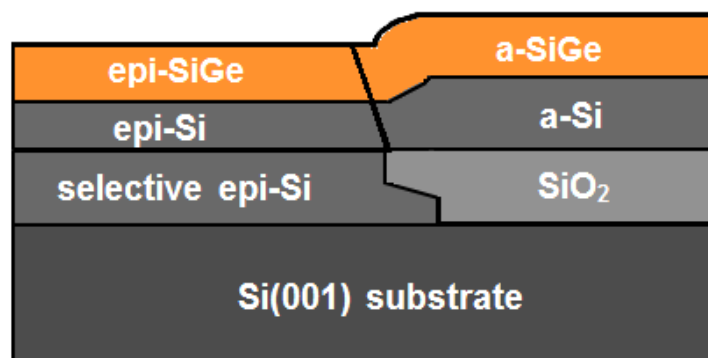
A closer look at the defective epi-Si part on the mask revealed existing SFs oriented along the  $\{111\}$  lattice planes. These SFs can cause a microtwinning effect by switching between substrate orientation (type A) and another orientation (type B), which is rotated by  $180^\circ$  around a  $\{111\}$ -axis. A close examination of Fig. 51(b) shows additional  $\{11\bar{1}\}_{MT}$  oriented SFs, which rotated by  $180^\circ$  around the  $(111)$ -axis to the original  $(11\bar{1})$  SFs. Because these SFs are connected to corresponding lattice planes with the same orientation, the appearance of  $\{11\bar{1}\}_{MT}$  oriented SFs can only originate from a microtwinning effect and is a clear evidence for a presence of MT formation [121, 145].



**Fig.52** Cross section TEM of crystallized sidewall after postannealing at 570 °C for 5 hours for uncovered (a) and with 10 nm SiO<sub>2</sub> capped (b) samples. Si thickness on mask is 180 nm [121].

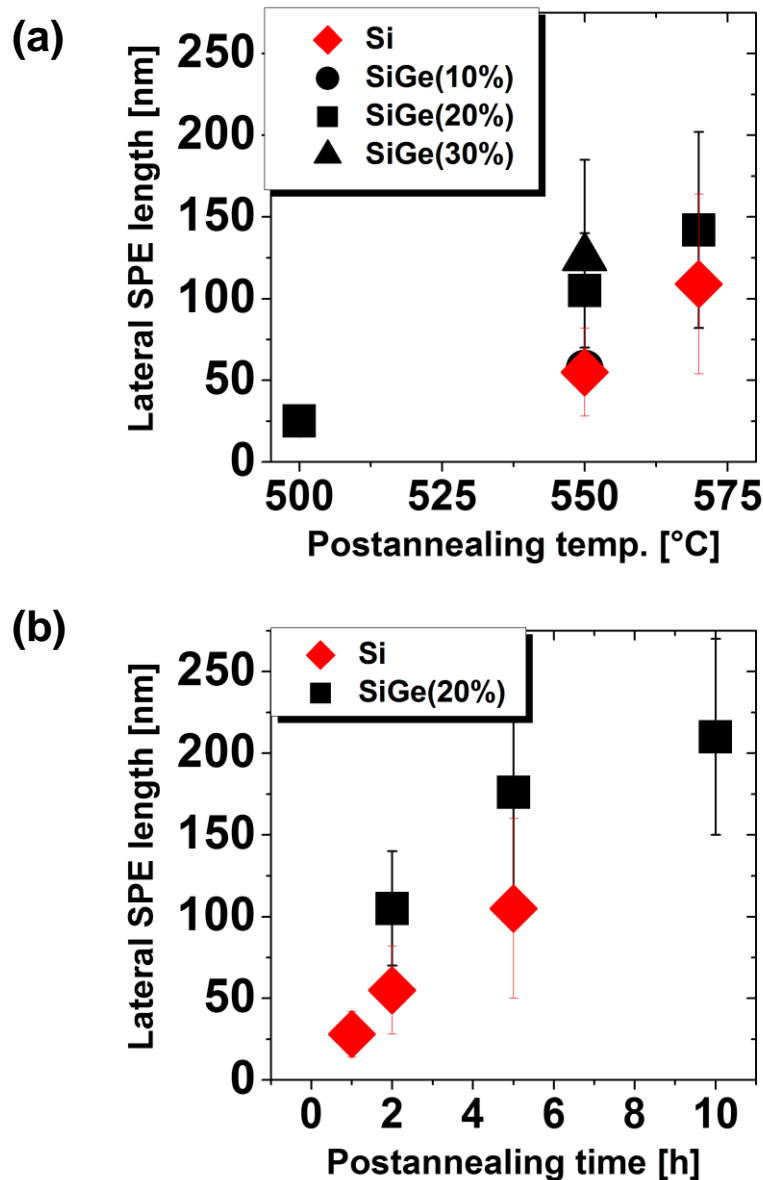
**Effect of surface migration on SPE:** To investigate the influence of surface migration effects of Si atoms on L-SPE length and crystallinity, results of samples capped with 10 nm SiO<sub>2</sub> with uncovered samples were compared. Figure 52 above shows exemplary cross section TEM images of uncovered (a) and capped (b) samples with 180 nm a-Si thickness on mask postannealed at 570 °C for 5 hours. After postannealing for 5 hours, epi-Si crystallized in both cases by SPE near the sidewall and a concurrent full poly-Si formation occurred on the mask. A comparison showed that the L-SPE length of the capped sample is increased reaching 450 nm. However, the crystallized epi-Si on sidewall and mask in both samples is defective, but it seems that the defect density in the capped sample is reduced. After all, no surface migration effects due to the postannealing process could be determined by TEM/SEM analysis. Impact of the surface migration seems to be low. The reason for the difference in crystallinity of uncapped and SiO<sub>2</sub>-capped samples is at the moment not fully understood and under current investigation. One possible explanation could be a change in the temperature condition of the postannealing experiments (e.g. by a reduced cooling effect of H<sub>2</sub> gas running normally at high flow over sample surface during the postannealing experiments) due to the capping with SiO<sub>2</sub> [121].

**Effect of Ge introduction in a-Si on SPE:** Before applying SPE on undoped Si-buffer/p-doped SiGe:C base/undoped Si-cap base layer stack, the influence of Ge in a-Si on L-SPE length in form of a-Si<sub>1-x</sub>Ge<sub>x</sub> [x = 0 – 1] layers has also to be investigated. For this, similar SPE experiments like above have been performed for epi-/a-Si<sub>1-x</sub>Ge<sub>x</sub> layers on top of epi-/a-Si buffer layers on epi-Si and SiO<sub>2</sub> mask, respectively (Fig. 53).



**Fig.53** Schematic diagrams of used SiO<sub>2</sub>-patterned Si(001) substrate with overhanging mask as-deposited at 550 °C with a-Si and a-Si<sub>1-x</sub>Ge<sub>x</sub>. A-Si and a-Si<sub>1-x</sub>Ge<sub>x</sub> thickness on SiO<sub>2</sub> mask are about 50 nm.

The temperature, Ge-concentration and time dependence results of these additional studies are summarized in Fig. 54:



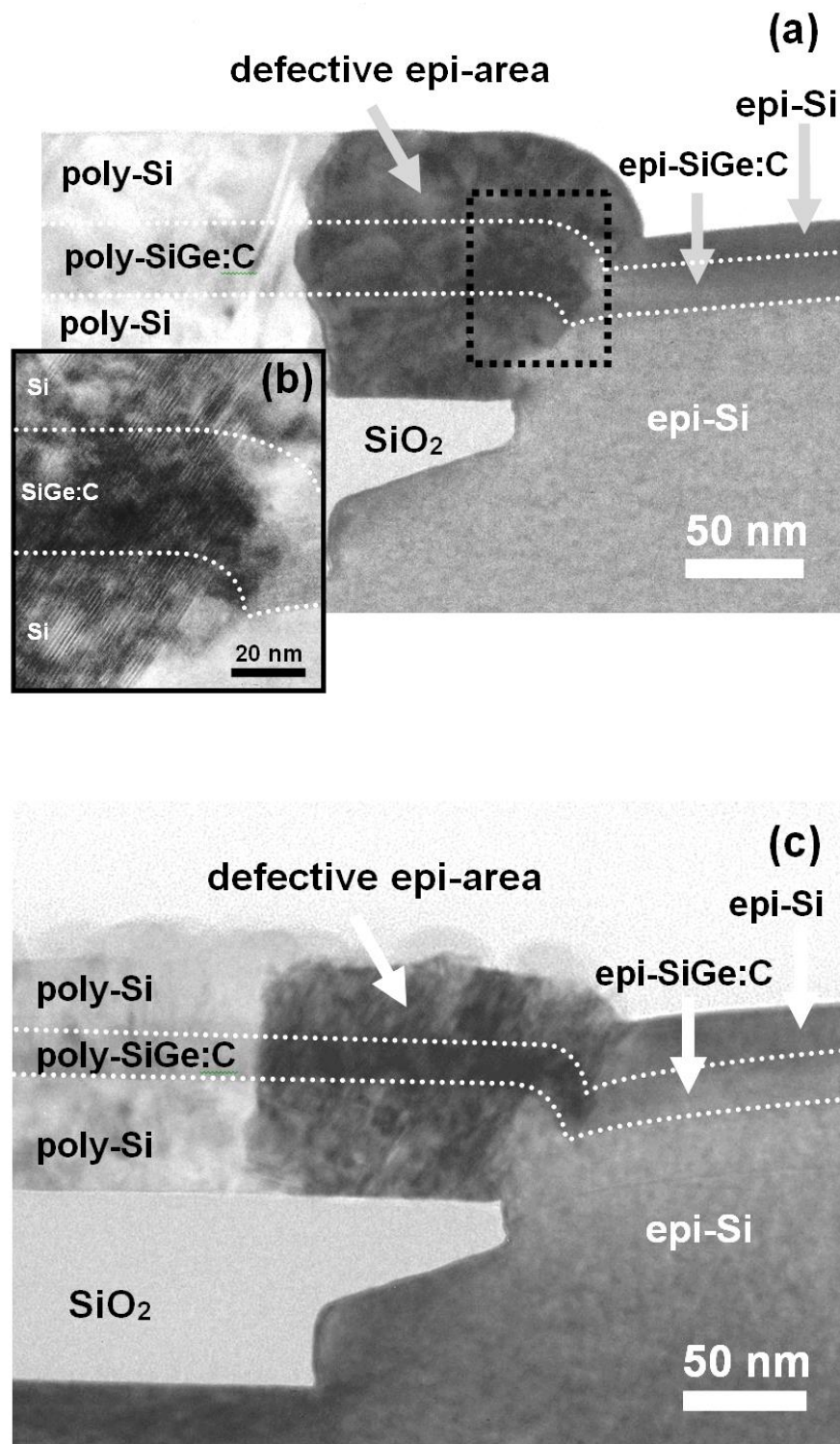
**Fig.54** Lateral SPE length of  $\text{Si}_{1-x}\text{Ge}_x$  layers on mask vs (a) postannealing temperatures for different Ge-concentrations and (b) postannealing times for  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and pure Si, respectively. For temperature dependence study, the postannealing time is 2 hours and for time dependence study, the postannealing temperature and Ge-concentration are 550 °C and 20%, respectively. A-Si and a-  $\text{Si}_{0.8}\text{Ge}_{0.2}$  thickness on  $\text{SiO}_2$ -mask are about 50 nm.

Figure 54(a) shows that the L-SPE length of crystallized a- $\text{Si}_{1-x}\text{Ge}_x$  on mask increases with postannealing temperature and Ge concentration. Comparing these SPE results for SiGe with respect to pure Si layers (red data points in Fig. 54 extracted from Fig. 48) generates the following insights:

Firstly, the introduction of small amount of Ge (e.g. 10%) seems not to affect the L-SPE length in comparison to pure Si after 2 hours postannealing at 550 °C. Secondly, at a Ge content of 20% an increase in L-SPE length can be observed at both 550 °C and 575 °C postannealing temperatures. However, the enhanced L-SPE length values are still in the error range of the pure Si values. Finally, at higher Ge concentrations (e.g. 30%) the L-SPE length clearly increases to values beyond achievable values for pure Si. Figure 54(b) depicts the L-SPE length of  $\text{Si}_{1-x}\text{Ge}_x$  and pure Si in dependence of postannealing time at 550 °C with 20% Ge concentration. Like in the pure Si case (red data points in Fig. 54 extracted from Fig. 48), the L-SPE length for SiGe with 20% Ge-content increases with increasing postannealing time. However, the average L-SPE length values of SiGe with 20% Ge-content are visibly higher in comparison to pure Si. In conclusion, Ge incorporation of more than 20% in a-Si as a- $\text{Si}_{1-x}\text{Ge}_x$  alloy improves the achievable L-SPE length after postannealing treatment. However, similar to pure Si experiment, it was found that the L-SPE growth seems also to be limited due to randomly grown poly grains on the mask. Nevertheless, the maximum in L-SPE length is about 100 nm higher with respect to pure Si, which implies that the numbers of random poly grain seeds and/or the growth rate of random poly grains on the mask are reduced in favor of L-SPE growth rate.

**SPE application on model SiGe:C HBT base stack:** By using all collected insights, the SPE is tested for model SiGe:C HBT base stack. For model SiGe:C HBT base, a Si-buffer/SiGe:C base/Si-cap layer stack is used. Figure 55 shows cross section TEM images of the sample applying SPE by postannealing at 570 °C for 5 hours after full SiGe:C HBT layer stack deposition (a) and direct after Si-buffer deposition (c). By full SiGe:C HBT layer stack deposition without intermediate annealing (Fig. 55(a)), both SiGe:C and Si grow as amorphous layers on sidewall and mask. The postannealing enables SPE of 140 nm for both SiGe:C and Si simultaneously without increasing surface roughness. Because the Si buffer and Si cap layer thickness is each about 50 nm on the mask, an achieved L-SPE length of 140 nm seems to correspond well to the L-SPE length results of 50 nm thick a-Si introduced before in Fig. 50. The crystallized epi-area contains a high amount of defects. Fig. 55(b) shows an enlarged HRTEM image of dashed rectangle in Fig. 55(a). A closer look at the defective epi-area on the mask revealed that the majority of appearing defects here are also SFs oriented along the  $\{111\}$  lattice planes (similar to Fig. 51(b)). After all, no clear difference in defect formation and distribution between SPE results of deposited single layer





**Fig.55** Cross section TEM images (a, c) and high resolution TEM close-up image (b) of by SPE crystallized bipolar window sidewall after full HBT base process containing Si-buffer/SiGe:C base/Si-cap layer deposition. SPE steps were applied after Si-buffer deposition (a) and after full base layer stack (c) at 570 °C for 5 hours. [121].

Si (Fig. 52(a)) and HBT base stack (Fig. 55(a)) could be found. In contrary, by applying SPE direct after Si-buffer deposition (Fig. 55(c)), the following SiGe:C and Si-cap layer grow as epitaxial layer on the epitaxial crystallized a-Si buffer domain. Because the Si buffer is also about 50 nm thick and the following lateral crystallization length of SiGe:C and Si cap layer depends on the L-SPE length (of the Si buffer, the total achievable L-SPE length here is limited to the same value range as in Fig. 55(a)). Because the crystallized buffer Si is defective containing similar SF formations as in Fig. 55(a), the deposited SiGe:C and Si-cap layers are also defective. During SiGe:C base and Si-cap layer deposition large polycrystalline grain formation occurs resulting eventually in surface roughing. However, epitaxial growth of SiGe:C base and Si-cap layer stack offers same growth rate as that in the window resulting in a preferred lower step height at the edge on the mask window. These preliminary results confirm the possibility to use SPE techniques to widen the monocrystalline region around the bipolar window [121].

### **3.2. III-V/SiGe hybrid device: $\text{In}_{1-x}\text{Ga}_x\text{P}$ collector**

In the following, the results of a theoretical evaluation of  $\text{In}_{1-x}\text{Ga}_x\text{P}$  as potential collector material in SiGe:C HBTs will be presented at first. Subsequently, the general and special aspects of III-V heteroepitaxy on Si and GaP heteroepitaxy on SiGe/Si will be addressed, respectively. Finally, the results of a growth and characterization study of GaP/SiGe/Si(001) heterostructures will be shown as a starting point for evaluating  $\text{In}_{1-x}\text{Ga}_x\text{P}$  as a potential collector material in SiGe:C HBTs. GaP was chosen as starting material due to its small lattice mismatch with respect to Si (0.36% at 300 K) (see Tab I in section 1.4.2).

#### **3.2.1 Semiconductor Physics of $\text{In}_{1-x}\text{Ga}_x\text{P}$ HBT collector**

As briefly mentioned in section 1.4.2, the ternary compound semiconductor  $\text{In}_{1-x}\text{Ga}_x\text{P}$  was chosen as potential collector material in this work due to its advantages in terms of higher electron carrier mobility and saturation velocity as well as bigger bandgap in comparison to Si (Tab. I). Here, a qualitative semiconductor physics discussion will be given in more detail to demonstrate how these material parameters will positively affect the speed and power performance of HBTs.

**Speed performance:** The transit cutoff frequency  $f_T$  (see equation (19)) was introduced in section 1.3.2 as figure of merit for speed performance in HBTs. In the following, the relationship of the carrier mobility  $\mu$  and the saturation velocity  $v_{sat}$  with respect to  $f_T$  will be addressed:

Carrier mobility: The carrier mobility  $\mu$  is defined by the Matthiessen's Rule, which reads as follows [45, 46]:

$$\mu = \left( \frac{1}{\mu_{ph}} + \frac{1}{\mu_{ion}} \right)^{-1} \quad (38)$$

where  $\mu_{ph}$  and  $\mu_{ion}$  are the carrier mobilities taking the acoustic phonon interaction and ionized impurities into account, respectively. By neglecting the constants in the equations for  $\mu_{ph}$  and  $\mu_{ion}$ , it is possible to extract the following important relationships [45]:

$$\mu_{ph} \propto \frac{1}{m^{*\frac{5}{2}} T^{\frac{3}{2}}} \quad \mu_{ion} \propto \frac{T^{\frac{3}{2}}}{N_{ion} m^{*\frac{1}{2}}} \quad (39)$$

where  $m^*$  is the charge carrier effective mass and  $N_{ion}$  is the ionized impurity density. For polar semiconductors like  $In_{1-x}Ga_xP$  the optical phonon scattering is significant, so that  $\mu$  strongly depends on  $T$  and  $m^*$ . Since the mobility is here dominated by scattering, it can be connected to the mean free path  $\lambda_m$  by [45]:

$$\mu = \frac{q \cdot \lambda_m}{\sqrt{3kTm^*}} \quad (40)$$

As consequence, lower  $m^*$  and  $T$  will improve  $\mu$ . Since  $m^*$  is a material related parameter, the reason for the enhanced  $\mu$  values with respect to Si is based on the electronic band structure properties (see Tab. 2). One sees that effective masses and mobilities are not for all  $In_{1-x}Ga_xP$  ( $x = 0 - 1$ ) compositions better than for Si. It is noted that the In-rich compositions (i.e. InP) always produce superior values. As discussed further below, Ga-rich compositions are not optimal for speed but rather for power performance of HBTs.

To display the influence of  $\mu$  to the speed performance of HBTs (or better  $f_T$ ), the relationship between  $\mu$  and the collector current  $I_C$  has to be considered. At low current densities,  $f_T$  increases with  $I_C$  as predicted in equation (19). In this regime  $I_C$  is carried mainly by the drift component through the CB-junction towards collector area, so that [45]:

	$\text{In}_{1-x}\text{Ga}_x\text{P} (x = 0-1)$	Si
Effective electron masses ( $m_i$ )	1.12 - 0.08 $m_0$	0.98 $m_0$
Effective electron masses ( $m_t$ )	0.22 – 0.08 $m_0$	0.19 $m_0$
Effective hole masses ( $m_h$ )	0.79 – 0.6 $m_0$	0.49 $m_0$
Effective hole masses ( $m_{hp}$ )	0.14 – 0.09 $m_0$	0.16 $m_0$
Mobility electrons	$\leq 250 - 5400 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$	$\leq 1400 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$
Mobility holes	$\leq 150 - 200 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$	$\leq 450 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$
Saturation velocity	$1 \times 10^7 - 3 \times 10^7 \text{ cm/s}$	$1 \times 10^7 \text{ cm/s}$

**Tab.2** Effective carrier masses, carrier mobilities and saturation velocities of Si and  $\text{In}_{1-x}\text{Ga}_x\text{P}$  at 300 K [45, 83].

$$I_C \approx qN_c\mu_n^{CB}E_{bc}A \quad (41)$$

where  $E_{bc}$  is the build-in electric field in the collector epitaxial layer,  $q$  is the electrical charge,  $N_c$  is the charge carrier density in collector and  $A$  is the unit area and  $\mu_n^{CB}$  is the electron charge carrier mobility in the CB-junction. Since the CB-junction is reversed biased and the collector is usually much lower doped than the base in HBTs, the collector-sided depletion region is much larger than the base-sided depletion region in the pn-junction. Therefore, the collector material (and its mobility) is more dominant, so that:

$$\mu_n^{CB} \approx \mu_n^C \quad (42)$$

where  $\mu_n^C$  is the electron charge carrier mobility of the collector material. To conclude, In-rich compositions of a  $\text{In}_{1-x}\text{Ga}_x\text{P}$  ( $x = 0 - 1$ ) collector have with respect to Si collector noticeable lower  $m^*$ . This enhancement will lead to higher  $\mu_n^C$ , which results in a positive impact on  $\tau_{CB}$ ,  $I_C$  and finally on the speed performance ( $f_T$ ) of a HBT.

Saturation velocity: The drift velocity  $v_D$  is defined for low electrical fields by the following equation [45, 46]:

$$v_D = \mu \cdot E \quad (43)$$

In the case of high electrical fields, the charge carriers gain on the one hand increasing kinetic energy, but on the other hand the optical phonon scattering becomes more effective, which causes the charge carriers again to loose energy. This results in the fact that  $v_D$  reaches a

saturation value  $v_{sat}$  [45, 46]:

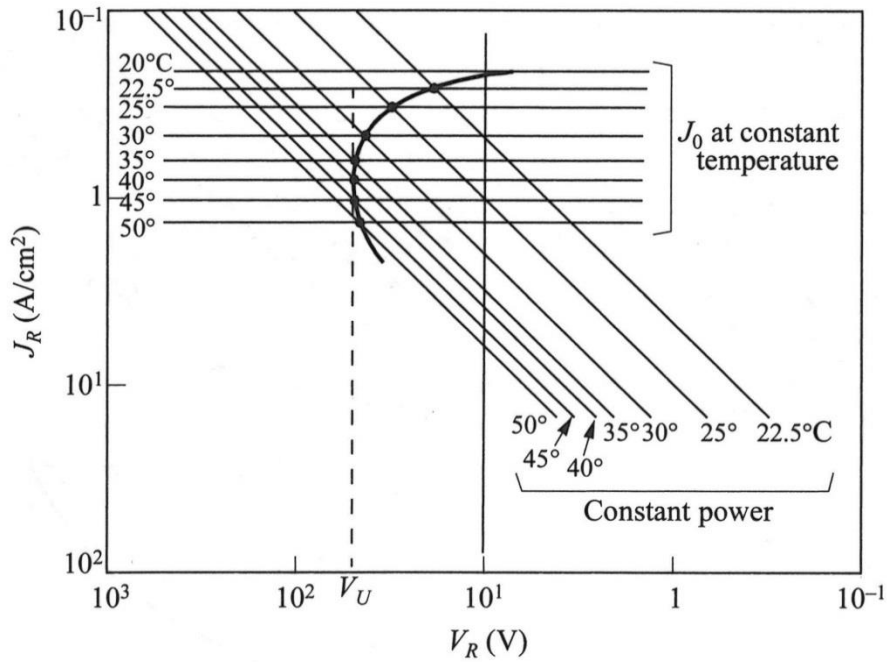
$$v_{sat} = \sqrt{\frac{8E_{ph}}{3\pi m^*}} \quad (44)$$

where  $E_{ph}$  is the optical-phonon energy. In conclusion, beside the already discussed material related parameter  $m^*$ ,  $E_{ph}$  is decisive and needs to be situated high in energy so that  $v_{sat}$  can reach values superior to Si. Therefore, In-rich compositions of a  $\text{In}_{1-x}\text{Ga}_x\text{P}$  ( $x = 0 - 1$ ) collector will lead to higher  $v_{sat}$  with respect to Si collector, which directly results in a positive impact on  $f_T$  of a HBT (see Equation (19) & section 1.4).

**Power performance:** The figures of merit for power performance in HBTs are the breakdown voltages  $V_{BCB0}$  and  $V_{BCE0}$  introduced in section 1.3.2. For better understanding, the different breakdown mechanisms in reversed biased pn-junctions (comparable with the reversed biased CB-junction in HBTs under normal operation;  $V_{CB} \gg 0$  V) will be briefly addressed:

**Breakdown mechanisms:** Three main different breakdown mechanisms exist:

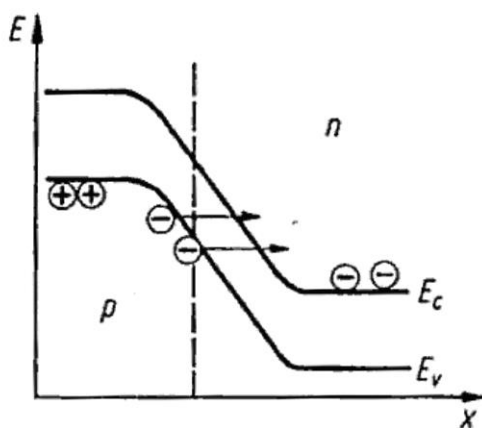
Thermal breakdown: The power dissipation, created in the space charge region of the pn-junction by reverse current at increasing reverse voltage, will be converted into heat and will increase the pn-junction temperature (depending on thermal conductivity of the device material and the cooling of the device). In turn, the increasing temperature results in increased electron-hole pair creation and thus increased reverse current. This vicious circle finally causes device breakdown. This temperature dependence of the reverse current is depicted in the log-log plotted reverse I-V characteristics of Fig. 56 [45]. The reverse current densities at a constant temperature are represented by a family of horizontal lines  $J_0$ . It is seen that the reserve current increases with increasing pn-junction temperature. The power (or heat) dissipation hyperbolas are given by the I-V product and are shown as sloped straight lines. It is seen that for example for  $V_R = 10$  V, the power dissipation strongly increases with pn-junction temperature. For a specific thermal resistance between pn-junction and heat sink, each value for power corresponds to one specific temperature ( $I \cdot V = \text{const.}$ ), so that the power hyperbolas have also temperature values as parameter. The points in Fig. 56 result as intersections of reverse I-V characteristics and power hyperbolas at the same temperature. As long as with increasing  $V_R$  also  $I_R$  increases, the pn-junction is stable. However, when for increasing  $I_R$ ,  $V_R$  also starts to drop, the pn-junction starts



**Fig.56** Reverse I-V characteristics of thermal breakdown [45].

to heat up and the vicious circle of self-destruction sets in. Because of the heat dissipation at high reverse voltage, the characteristic shows a negative differential resistance. If a turnover voltage  $V_U$  is reached at a specific temperature, the current increases strongly with decreasing voltage. In this case, the pn-junction starts to destroy itself [45, 146].

Zener breakdown: Under a high reverse voltage, the depletion region of the pn-junction expands resulting in a high electric field across the pn-junction. At a sufficiently strong



**Fig.57** Zener effect [146].

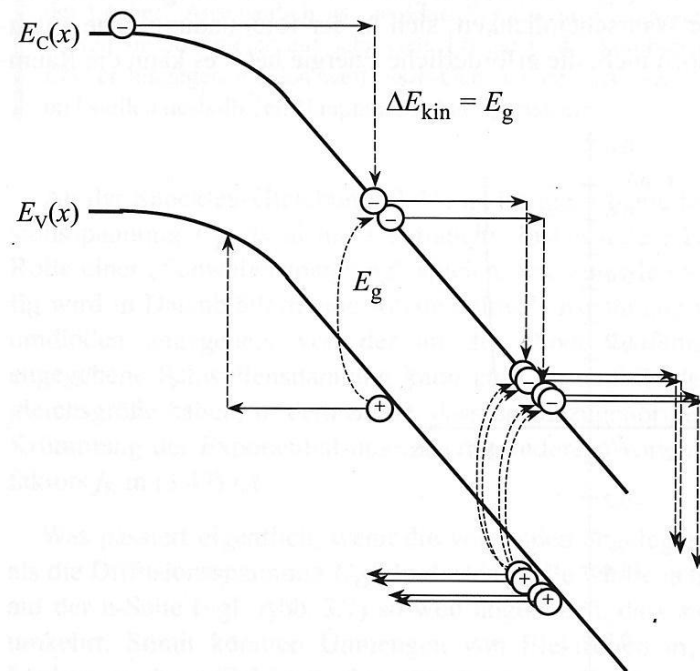
electric field, the electrons from the valence band of a p-type semiconductor can directly tunnel to the conduction band of an n-type semiconductor, increasing thus the number of free charge carriers. This special tunneling effect is known as Zener effect (Fig. 57). This sudden generation of free charge carriers rapidly increases the reverse current and finally causes the Zener breakdown. Since the bandgaps  $E_g$  (in e.g. Si and GaAs) decrease with increasing temperature, the breakdown voltage will decrease due to the

tunnel effect. The tunnel current  $J_t$  can be described as [45]:

$$J_t = \frac{\sqrt{2m^*} q^3 E \cdot V_R}{4\pi^2 \hbar^2 \sqrt{E_g}} \exp \left[ -\frac{4\sqrt{2m^*} E_g^{\frac{3}{2}}}{3qE\hbar} \right] \quad (45)$$

where  $V_R$  is the reverse voltage and  $E$  is the field inside the pn-junction. Finally, it is to mention that, in comparison to thermal breakdown and avalanche breakdown, the Zener breakdown does not destroy the device [146].

**Avalanche breakdown:** The avalanche breakdown (or impact ionization) is the most common and important breakdown mechanism in pn-junctions. Under a high reverse voltage, the introduced high electrical field will accelerate the charge carriers (i.e. electrons and holes) and strongly increase in this way their kinetic energy  $E_{kin}$ . If the charge carriers do not effectively transfer the received  $E_{kin}$  by collisions to the crystal lattice and  $E_{kin}$  finally reaches the scale of  $E_g$ , an additional electron-hole pair can be generated in the pn-junction. The so created electron-hole pairs will also be accelerated in the high electrical field, leading to further generation of additional electron-hole pairs and an avalanche-like increase of free charge carrier results. The avalanche effect is shown in Fig. 58 [45, 146, 147].

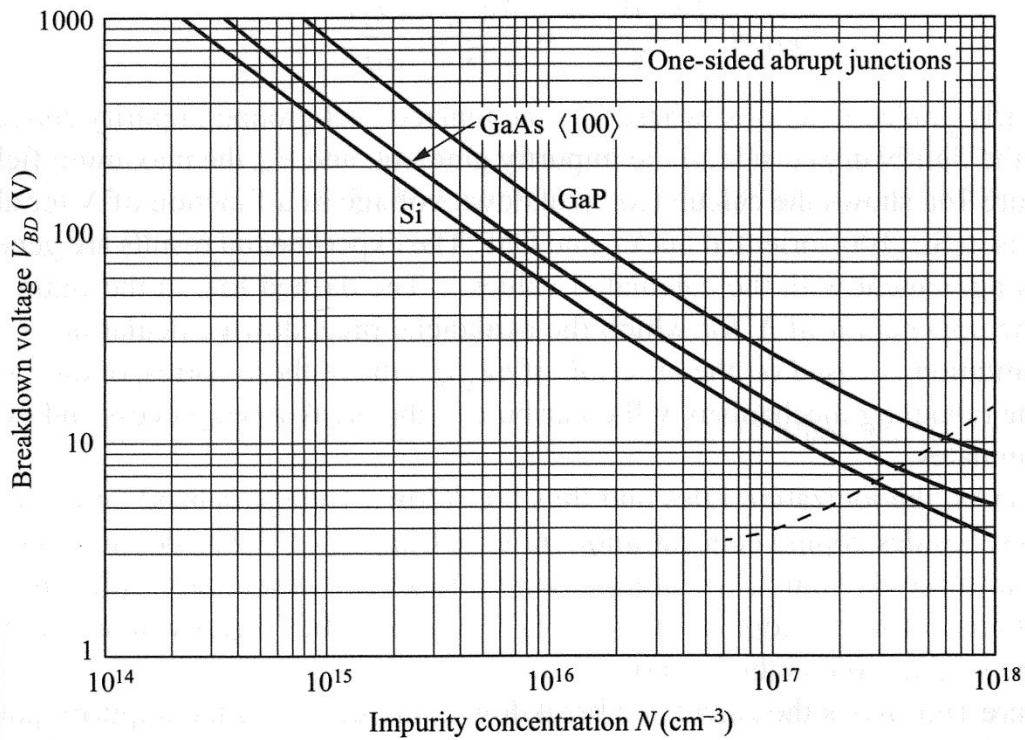


**Fig.58** Creation of electron-hole pairs due to avalanche effect [147].

In the end, the strong increase in free charge carriers, increases the reverse current exponentially and causes the called avalanche breakdown. In comparison to the Zener

breakdown, the avalanche breakdown voltage increases with increasing temperature due to higher accompanied phonon-electron interaction with the lattice. As a result, the charge carriers need a longer migration distance to accumulate enough  $E_{kin}$  to generate additional electron-hole pairs and the avalanche effect will be reduced.

**Impact of higher bandgap  $E_g$  on breakdown voltage  $V_{BD}$ :** From the previous paragraph, it is known that the avalanche effect appears under high electric fields, when the energy of the charge carriers reaches  $\approx E_g$  above the corresponding thermal equilibrium value, causing in the end device breakdown. Figure 59 shows  $V_{BD}$  for semiconductor materials (Si, GaAs<100> and GaP) with different  $E_g$  (1.12 eV, 1.42 eV and 2.24 eV [83]) for one-sided abrupt junctions in relation to the impurity concentration  $N$  [45]:



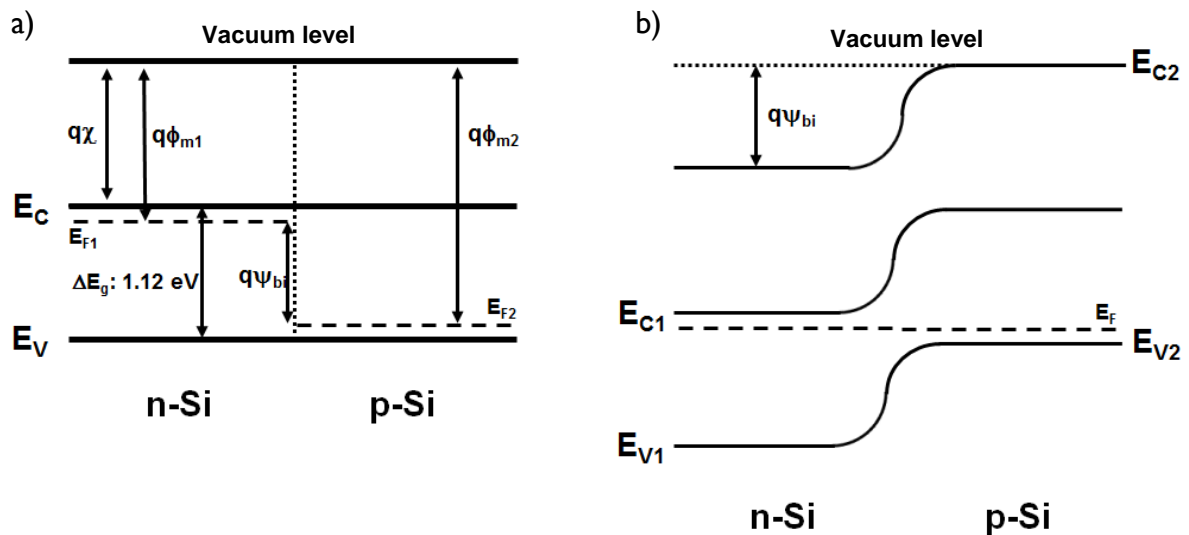
**Fig.59** Breakdown voltage in Si, <100>-oriented GaAs, and GaP for one-sided abrupt junctions vs. impurity concentration [45].

Consequently, Fig. 59 depicts that the semiconductor materials with higher  $E_g$  have higher breakdown voltages (e.g. GaP in comparison to Si) and therefore a higher thresholds against the avalanche breakdown. Furthermore,  $V_{BD}$  decreases with  $1/N$  due to the increasing number of free charge carriers triggering the avalanche breakdown effect. It is to be noted that the case of a one-sided abrupt GaP pn-junction is not identical to the case of a  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{GaP}$  base-collector pn-heterojunction. However, the qualitative conclusion is clear:



An electron entering from a p-doped  $\text{Si}_{0.8}\text{Ge}_{0.2}$  base region into an n-doped GaP collector material will create much less avalanche events than for identical conditions in an n-type Si collector. Thus, for an  $\text{In}_{1-x}\text{Ga}_x\text{P}$  ( $x = 0 - 1$ ) collector, the Ga-rich composition range is, due to the bigger bandgap with respect to InP and Si (see Tab. 1), of interest to increase HBT power performance.

**Band structure alignment:** At last, a theoretical evaluation of band alignment and band structure of n-GaP/p- $\text{Si}_{0.8}\text{Ge}_{0.2}$ /n-Si(001) heterostructure has been performed in order to investigate their suitability for HBT application. For this, the *Anderson illustration model* and the theoretical calculation by *Van de Walle and Martin* have been used [148-150]. For reasons of clarity, the differences in band structure depiction of homo- and heterojunctions after *Anderson* will be presented step-by-step in the following: First, a simple n-Si/p-Si junction by *Anderson illustration model* is considered in Fig. 60:

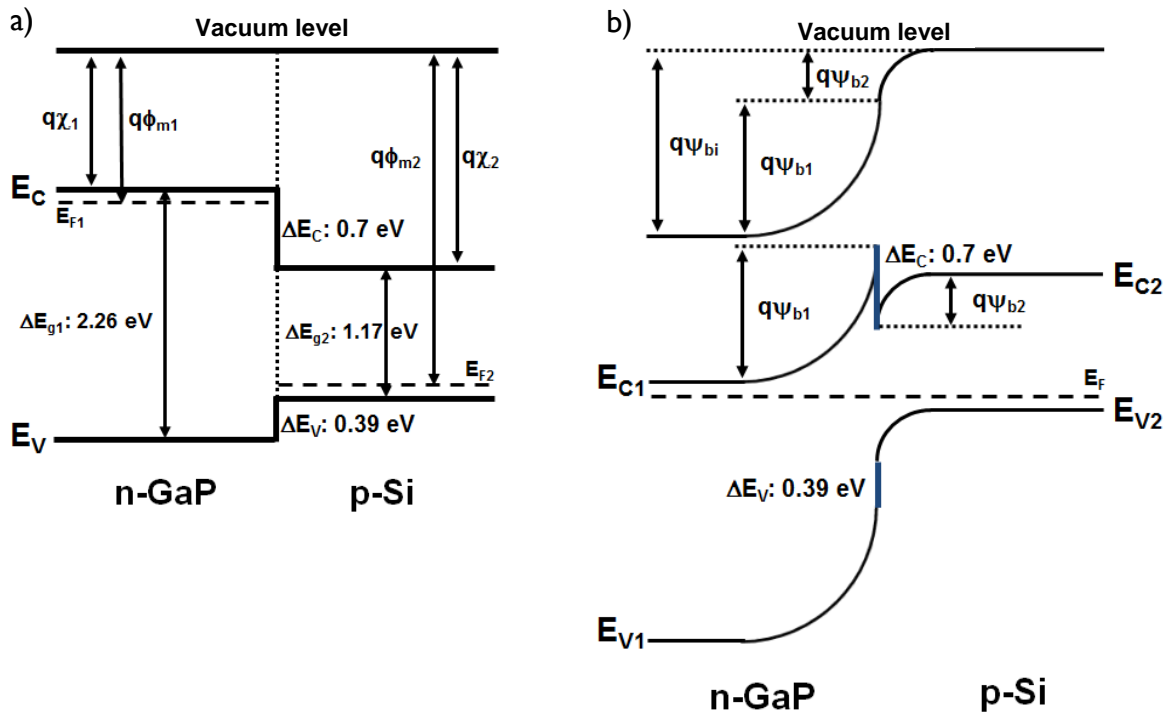


**Fig.60** Energy-band diagrams for (a) two isolated n-Si and p-Si semiconductors and (b) their idealized homojunction at thermal equilibrium [45, 148].

Figure 60(a) shows the energy-band diagrams for two isolated n-Si and p-Si semiconductors. Both semiconductors are assumed to have the same  $E_g$  and the same doping concentration. However, the work functions  $\phi_m$  is different due to the different Fermi levels of n-Si ( $E_{F1}$ ) and p-Si ( $E_{F2}$ ). The parameters  $\phi_m$  and  $\chi$  (i.e. electron affinity) are defined as the energy required to remove an electron from the Fermi level  $E_F$  and from the bottom of the conduction band  $E_C$ , respectively, to the vacuum level outside the material [45]. In homojunctions, the built-in potential  $\psi_{bi}$  is simply given by the difference between  $E_{F1}$  and  $E_{F2}$ . Knowing the parameters

for  $E_g$ ,  $\phi_m$  and  $\chi$  [83], enables to construct a band energy diagram of this n-Si/p-Si homojunction by the *Anderson illustration model* in thermal equilibrium ( $E_{F1} = E_{F2}$ ) (Fig. 60(b)) [148]. It is noted that the build-in potential  $\psi_{bi}$  is given in homojunctions by the different doping and thus Fermi-energy positions in n- and p-side. This is different in heterojunctions due to the different band energy positions.

Next, a heterojunction will be considered in contrast to the n-Si/p-Si homojunction. For this, an n-GaP/p-Si junction by *Anderson illustration model* is considered in Fig. 61:



**Fig.61** Energy-band diagrams for (a) two isolated n-GaP and p-Si semiconductors and (b) their idealized heterojunction at thermal equilibrium [45, 148, 150].

Figure 61(a) depicts energy-band diagrams for two isolated n-GaP and p-Si semiconductors. Because of the different semiconductor materials, in addition to  $\phi_m$  and  $\chi$ , also  $E_g$  varies in this case. The difference in  $E_g$  results in the formation of conduction-band edges  $\Delta E_C$  and valence-band edges  $\Delta E_V$  between the two semiconductors. For the determination of  $\Delta E_C$ ,  $\Delta E_V$  and  $E_g$ , the values calculated by *Van de Waale and Martin*, applying their local-density-functional pseudopotential formalism and model-solid approach, are used [149, 150]. If now a junction between n-GaP and p-Si is formed, the band energy diagram by the *Anderson illustration model* at equilibrium will look like Fig. 61(b) [45, 148]. In contrast to the n-Si/p-Si homojunction at equilibrium (Fig. 60(b)), band discontinuities appear in the n-GaP/p-Si

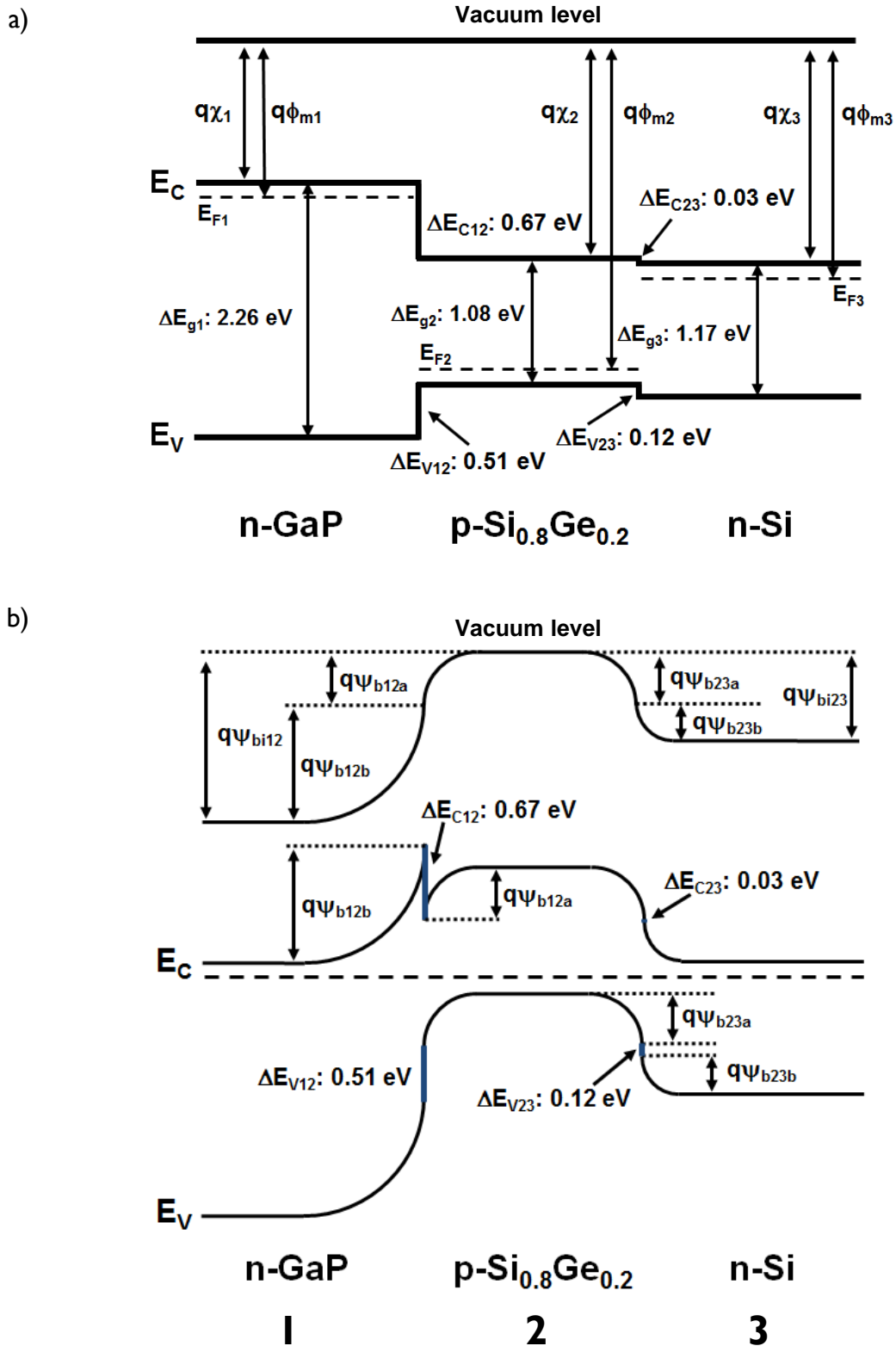
heterojunction at equilibrium (marked as blue lines in Fig. 61(b)), due to presence of  $\Delta E_C$  and  $\Delta E_V$ . The total  $\psi_{bi}$  in this case is given by the sum of the partial build-in potentials  $\psi_{b1}$  and  $\psi_{b2}$ , where  $\psi_{b1}$  and  $\psi_{b2}$  are the electrostatic potentials supported at equilibrium by semiconductor 1 and 2, respectively [45]. The values of these potentials are related to the doping concentration of the two semiconductors 1 (here: GaP) and 2 (here: Si). By comparing Fig 61(b) with other assessments of n-GaP/p-Si band energy diagrams in literature, a good agreement can be found. All depictions of the n-GaP/p-Si band energy diagram show a staggered heterojunction [125, 148-150, 153, 154]. Only in the case of  $\Delta E_C$  and  $\Delta E_V$  difference can be found due to the various theoretical model used for their estimation. Table 3 shows an overview of the most common theoretical approaches and their calculated values:

Literature	Theoretical model	$\Delta E_V$ [eV]	$\Delta E_C$ [eV]
<i>Van de Walle &amp; Martin</i> [149, 150]	LDPF/MSA theory	0.39	0.70
<i>Harrison &amp; Wright</i> [125, 154]	LCAO theory	0.46	0.68
<i>Anderson</i> [148]	Electron affinity rule	0.33	0.81
<i>Frensley &amp; Kroemer</i> [153]	SCP theory	0.18	0.96

**Tab.3** Overview of most common theoretical models for estimation of conduction-band edges  $\Delta E_C$  and valence-band edges  $\Delta E_V$  in n-GaP/p-Si heterojunction band energy diagrams. Theoretical models are the local-density-functional pseudopotential formalism and the model-solid approach (LDPF/MSA), the linear combination of atomic orbitals (LCAO), electron affinity rule and the self-consistent pseudopotential (SCP) [125, 148-150, 153, 154].

The values of  $\Delta E_C$  and  $\Delta E_V$  calculated by *Van de Waale* and *Martin* has been used in this thesis, because all other models rely on information about bulk alone, and do not provide a complete description of the electron distribution at the interface like in *Van de Waale* and *Martin*'s approach [149, 150].

Finally, band alignment and band structure of n-GaP/p-Si<sub>0.8</sub>Ge<sub>0.2</sub>/n-Si(001) heterostructure will be discussed. Using the *Anderson illustration model* and the calculated values of *Van de Waale* and *Martin* for  $\Delta E_C$ ,  $\Delta E_V$  and  $E_g$ , the band energy diagram for this double heterojunction device could be estimated and is shown in Fig. 62 [148, 150]. It has to be noted that, for simplification of Fig. 62, all layers (n-GaP, p-Si<sub>0.8</sub>Ge<sub>0.2</sub> and n-Si) are assumed to have the same doping concentrations and the p-Si<sub>0.8</sub>Ge<sub>0.2</sub> layer has a Ge-box profile.



**Fig.62** Energy-band diagrams for (a) three isolated n-GaP, p-Si<sub>0.8</sub>Ge<sub>0.2</sub> and p-Si semiconductors and (b) their idealized double heterojunction at thermal equilibrium [45, 148, 150]

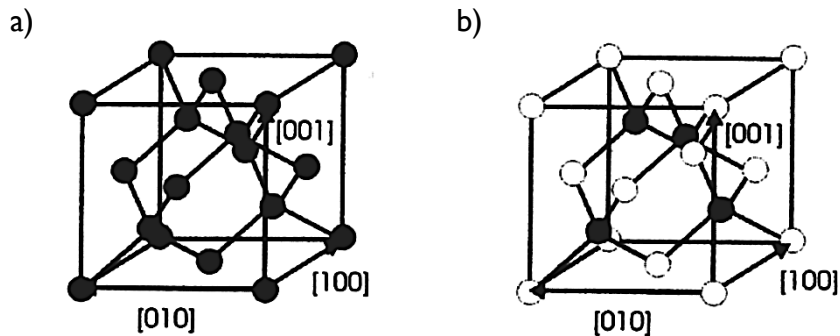
The comparison of energy-band diagrams of the n-GaP/p-Si<sub>0.8</sub>Ge<sub>0.2</sub>/n-Si(001) heterostructure (Fig. 62(b)) at thermal equilibrium and a standard n-Si/p-SiGe:C/n-Si(001) HBT (see Fig.13) at thermal equilibrium results in the following insights:

Firstly, the general arrangement of band offsets of an n-GaP collector/p-Si<sub>0.8</sub>Ge<sub>0.2</sub> base/n-Si emitter double HBT meet the requirement for a functional III-V/SiGe hybrid device. Secondly, n-GaP as possible new collector material introduces two new aspects in comparison to standard n-Si collector material. On the one hand, the visibly wider band gap reduces the avalanche effect like already mentioned above. On the other hand, a larger band bending of  $E_C$  at the CB-junction is generated with respect to n-Si collector due to the larger  $\Delta E_{C12}$ . This will result in a higher potential drop for electrons moving towards the collector and will consequently raise the drift velocity, which increase in turn the speed performance of the HBT. Thirdly, the band discontinuity in  $E_C$  at the CB-junction creates a vertical barrier for electrons moving towards collector. This vertical barrier has to be eliminated in order to prevent reflection and trapping mechanism, and in consequence  $I_C$  reduction. It is known that band discontinuity can be reduced or even eliminated by slow variation of material composition within the depletion regions, like demonstrated in section 1.3.2 as graded SiGe:C base HBT [45]. Equally, using a graded Ge base profile in n-GaP/p-Si<sub>0.8</sub>Ge<sub>0.2</sub>/n-Si(001) HBT will additionally introduce a slanting base in  $E_C$ , creating a beneficial built-in drift field for electron transport towards the collector.

### 3.2.2 General aspects of III-V heteroepitaxy on silicon

Up to today, promising work has been published on epitaxial growth studies of GaP on Si. Besides many international groups, like T.J. Grassman et al. [91], T. Soga et al. [92], Y. Takagi et al. [93] and A. Létoublon et al. [94], there are especially the research groups of K. Volz et al. [95] and T. Hannappel et al. [96] to be mentioned for their GaP pioneering work in Germany. These two German groups focused their activity on Metal organic CVD (MOCVD) deposition of defect free nucleation and thin layers of GaP on Si for the implementation of optoelectronic devices on Si (e.g. III/V-based lasers, light-emitting diodes (LEDs) and solar cells). As known from these (and several other III-V materials on group IV) growth studies, a number of challenges arise for achieving high quality III-V heterostructures on Si, which will be briefly presented in the following:

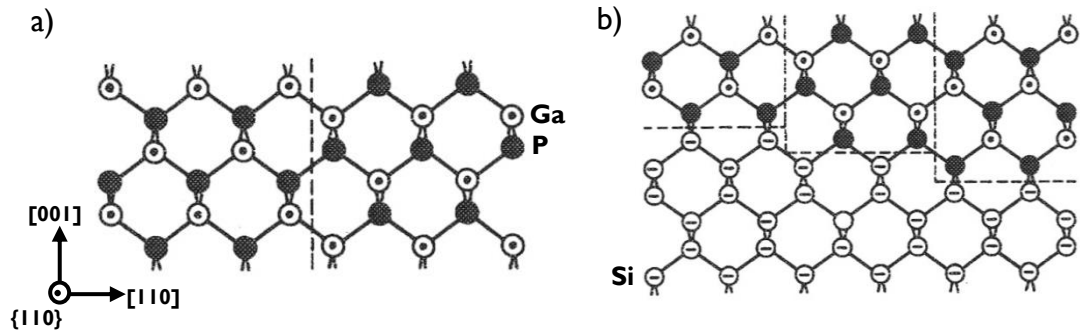
**Charge neutrality of heterointerface:** First, it has to be considered that Si and Ge crystallize in diamond structure, creating a non-polar crystal structure (depicted in Fig. 63(a)).



**Fig.63** Schematic structure diagrams of diamond **(a)** and zinc blende **(b)** unit cells [155].

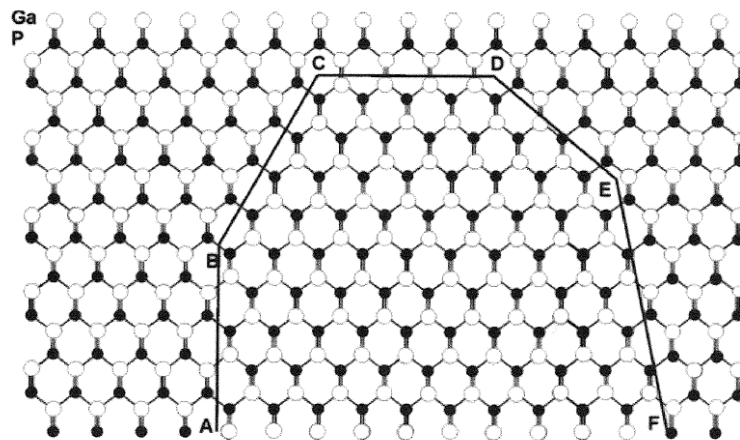
This crystal structure consists of two inter-penetrating face centered cubic (fcc) lattices; one displaced from the other by a translation vector of  $a/4\langle 111 \rangle$ . In contrast, GaP crystallizes as III-V compound semiconductor in the zinc blende structure (Fig. 63(b)), whose structure is a subgroup of the diamond structure. This is true, because one of the fcc sublattices is occupied by only group III-atoms and the other one is occupied only by group V-atoms, creating in this way the possibility of polar crystal structure growth [155]. By deposition of polar GaP(001) thin films on i.e. unpolar Si(001) substrates, a heteropolar interface is created. Due to the Ga-P- (or P-Ga-) stacking sequence in the deposited GaP layer, an aligned dipole exists, which increases strongly with thickness layer by layer. Starting from the heterostructure interface, this results in the build-up of an electrical field increasing with layer thickness. In consequence of the presence of such huge fields, an idealized atomic arrangement at the interface during growth will not be stable and the interface will reconstruct in a complex manner, increasing potentially defect generation at the interface. To cancel this electrostatic diverging energy term, different stabilizing approaches exist. One possibility is for example to use different surface and interface reconstructions (e.g. Si(110) and Si(211)) to achieve charge neutral heterointerfaces [125, 155, 156, 158].

**Anti-phase disorder:** The anti-phase (AP) disorder describes a crystallographic defect, which emerges due to atomic arrangement errors during growth of III-V compound semiconductors on group IV-substrates. Figure 64 illustrates schematic diagrams of AP disorder in GaP/Si heterostructures [89, 155]:



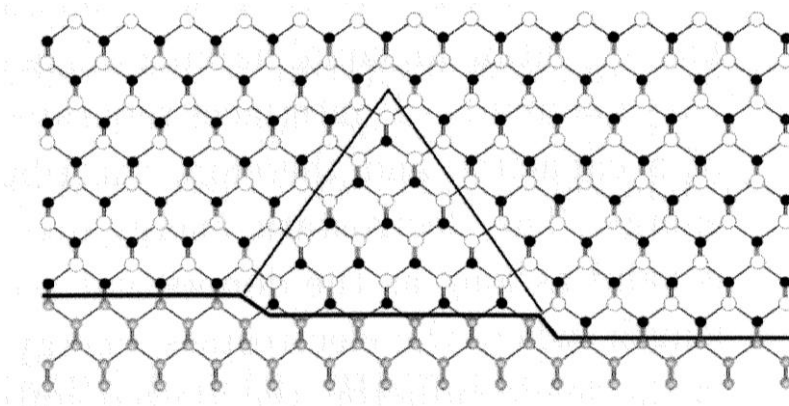
**Fig.64** Anti-phase disorder in zinc blende structure. **(a)** APB lying on a  $\{110\}$  plane originating from non-uniform initial monolayer. **(b)** APB lying on a  $\{110\}$  plane, originating from a monolayer high step of Si surface [89, 155].

Because two compounds (group III-atoms and group V-atoms) are simultaneously involved in the growth process, crystal domains with reversed polarity (e.g. Si-Ga-P-Ga-P... and Si-P-Ga-P-Ga... arrangements along  $[001]$  direction) can form during initial island nucleation phase instead of a perfect lattice system. These crystal domains are known under the term APDs and are limited by anti-phase boundaries (APBs; highlighted by the dashed lines in Fig. 64). In general, two different reasons for anti-phase disorder exist: First, the III-V compound semiconductor nucleates on an atomically smooth group IV surface, but not with the same initial monolayer (e.g. for GaP, it is called Ga- or P-first layer areas) (depicted in Fig. 64(a)). Secondly, the presence of monolayer high steps (or odd number of atomic layer steps) on the substrate aid the formation of APDs (depicted in Fig. 64(b)) [89, 155]. Adjacent APDs can have their APBs on various crystallographic planes. All possible orientations are shown in Fig. 65 [155]:



**Fig.65** APBs in zinc blende structure. APBs on different crystallographic planes: AB parallel to  $\{110\}$ , BC parallel to  $\{111\}$ , CD parallel to  $\{100\}$ , DE parallel to  $\{211\}$  and EF parallel to  $\{311\}$  [155].

Figure 65 reveals the existence of APBs, which are stoichiometric (i.e. equal number of cation-cation and anion-anion bonds between APDs exists) on  $\{110\}$  planes (AB), and non-stoichiometric on  $\{211\}$  (DE) and  $\{311\}$  (EF) planes. Additionally, APBs can also be situated on the  $\{111\}$  planes (BC) or the  $\{100\}$  planes (CD), which are built up with only one pair of false bonds (e.g. Ga-Ga or P-P) [155]. Theoretical calculations of APB formation energies for the  $\{100\}$ ,  $\{110\}$ ,  $\{111\}$  and  $\{211\}$  planes showed that the  $\{211\}$  and  $\{110\}$  APBs will be preferentially formed with respect to the  $\{111\}$  or  $\{100\}$  plane due to energetic reasons [157]. Nevertheless, the  $\{111\}$  APBs have a special characteristic: If two propagating  $\{111\}$  APBs meet each other, it results in the self-annihilation of the APBs and the limitation of the APD. This situation is depicted in Fig. 66 [155]:



**Fig.66** Self-annihilation of two  $\{111\}$  APBs with false Ga-Ga bonds [155].

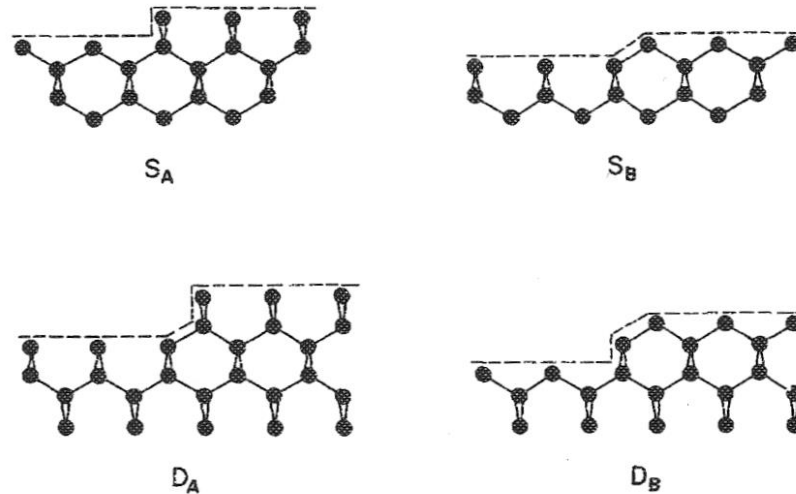
In contrast, APBs situated on  $\{110\}$  planes in (001) orientated epitaxial layers are more detrimental because these defects thread through the whole layer. The anti-phase disorder creates electronic states in the bandgap of the compound semiconductor, which act as charge traps for charge carriers and contribute thus to charge carrier scattering. Because of this, the anti-phase disorder has to be suppressed or avoided before device integration or further overgrowth. At the moment, three methods are mainly used to deal with anti-phase disorder in deposited III-V compound semiconductors on Si and Ge:

Different substrate orientations: This method uses the fact that III-V-materials form different number of dangling bonds to the Si and Ge surface. On ideal, higher-indexed Si or Ge substrates (e.g. (211), (311), (411) and (511)), the surface atoms belong to one of two sublattices. Thereby, surface atoms on one of the sublattice form two dangling bonds, while those on the other sublattice form only one dangling bond. It is shown in literature that the group V atoms bond to those with two dangling bonds, whereas group III atoms to those



with only one dangling bond. Thus, a defined atomic arrangement is created on the surface and APDs will be suppressed [125, 155].

Off-oriented Si(001) towards [110] direction: On the thermodynamical stable Si(001)-(2x1) reconstructed surface, the Si dimers on two terraces separated by a monolayer or double layer step form two 90° (2x1) rotation domains. Figure 67 illustrates the four possible step configurations [89]:

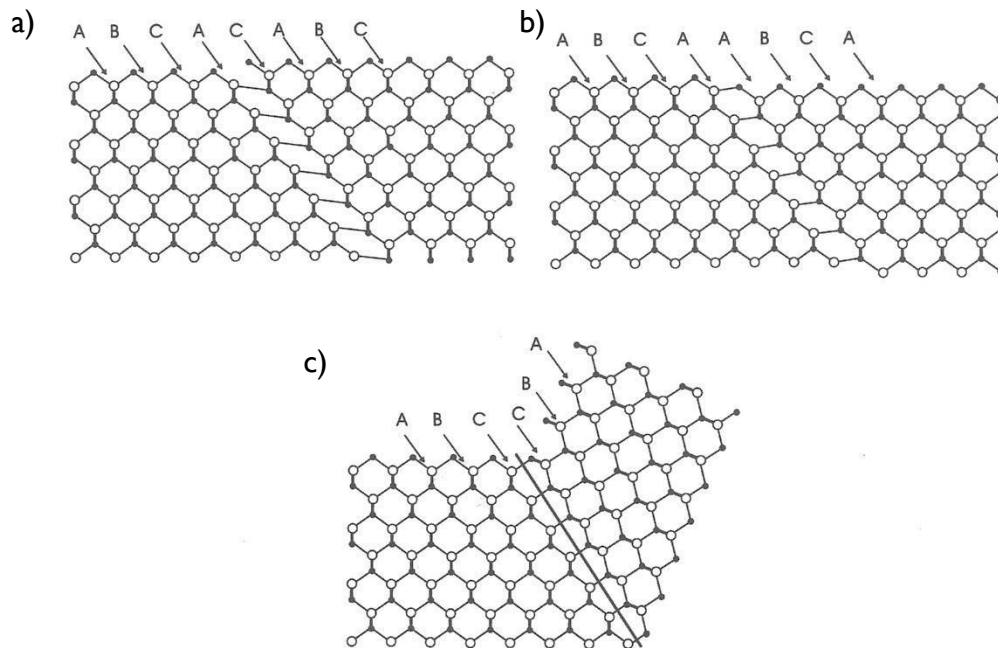


**Fig.67** Monolayer step with step edge parallel ( $S_A$ )/perpendicular ( $S_B$ ) to dimerization direction and double layer steps with step edge parallel ( $D_A$ )/perpendicular ( $D_B$ ) to the surface dimerization direction [89].

The most common orientation on on-oriented Si(001) surfaces is the monolayer step with step edge parallel ( $S_A$ ) to the dimerization direction. As mentioned before, monolayer steps promote the formation of APDs. By using (2-8°) off-oriented (towards [110] direction) Si(001) substrates, the monolayer steps on the Si and Ge surface can be suppressed in favor of double layer steps (or even number of atomic layer steps), resulting finally in APD-free III-V layer growth. As the double layer steps ( $D_A$ ,  $D_B$ ) are thermodynamically more stable than monolayer steps ( $S_A$ ,  $S_B$ ), the off-oriented Si(001) substrates are usually annealed at 850 °C – 1000 °C for 10 min – 30 min in order to create these surface structures [92, 93, 155]

High temperature annealing of on-oriented Si(001) surface: This method is similar to the previous one, but does not use off-oriented Si(001) substrates. In literature, the creation of perfect double steps even on on-oriented Si(001) surfaces by long high temperature annealing processes (> 950°C for >10 min) has been recently demonstrated [95, 155], as these steps are thermodynamically more stable.

**Growth defects:** Perfect heteroepitaxial overgrowth of a lattice mismatched III-V semiconductor for technology applications is generally a daunting task. Due to different factors, like e.g. wrong process parameters, unwanted impurities and coalescence processes of 3D islands during growth, growth defects can arise in the deposited layer. The most prominent planar growth defects in zinc blende crystals are shown in Fig. 68 [155]:



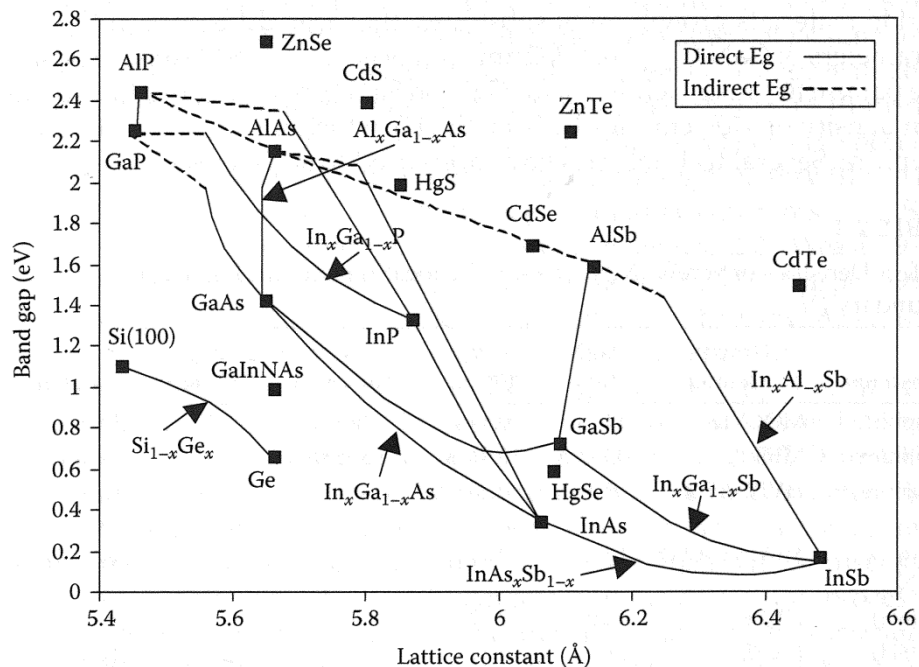
**Fig.68** Planar defects of zinc blende crystal: **(a)** intrinsic stacking fault, **(b)** extrinsic stacking fault and **(c)** microtwin [155].

Assuming the normal stacking order ABCABCABC along  $\langle 111 \rangle$  directions, the stacking disorder is depicted as ABCA\_CABC (B-plane missing) known as intrinsic SF and as ABCA\_A\_B\_C\_A (additional A-plane inserted) known as extrinsic SF (Fig. 68(a, b)). Different causes exist for the SF formation in a zinc blende crystal structure [159]: 1) Dissociation of perfect dislocation in partials, 2) Deposition errors on  $\{111\}$  planes, 3) Coalescence of grown islands with different stacking sequences, and 4) Precipitates in the crystal.

However, if one part of the crystal is rotated by  $60^\circ$  around a  $\langle 111 \rangle$  rotation axis, it will join with the other part on the  $\{111\}$  plane to form a volume defect, called rotation twin or microtwin. This defect has a mirror symmetric stacking order of ABCBA (Fig. 68(c)). SFs are called low energy defects, because no broken bonds or false bonds are created. MTs however may cause more severe crystal damage when embedded in the otherwise perfect

epitaxial layer. The optimization of cleaning and growth process to guarantee 2D film growth is a key issue in order to suppress SFs and MTs [143, 155, 160].

**Lattice mismatch and critical layer thickness:** If the lattice parameters of both the grown film and the substrate are perfectly matched, they will bind during growth without any interfacial strain, creating an epitaxial overgrowth without any MD defects. This can be observed e.g. in homoepitaxy of Si on Si substrates. Nevertheless, in the world of heteroepitaxy (i.e. lattice mismatched heterostructure growth of epitaxial film on foreign substrates), this condition is generally not fulfilled, leading to challenges of growing defect-free heterostructures. Figure 69 depicts the lattice constants and bandgaps of conventional compound and diamond semiconductors.



**Fig.69** The lattice constants and bandgaps of conventional compound and diamond semiconductors at 300 K [161].

Resulting crystallographic lattice mismatch parameters can thus easily be extracted [161]. If the lattice mismatch is small ( $\ll 4\%$ ), heteroepitaxial films often grow in the initial phase pseudomorphically on the substrate. This means that the grown layer adopts the in-plane lattice constant of the substrate, resulting in a distortion of the grown heteroepitaxial crystal. This strained condition can be maintained up to a critical layer thickness  $h_{crit}$ , where it becomes energetically favorable for the grown layer to plastically relax by creating defects

in the heterostructure [118]. Due to the general high lattice mismatch of III-V materials with respect to Si and Ge, the critical layer thickness  $h_{crit}$  is for these cases only in the range of some monolayers (e.g. GaAs on Si: approximately 4 monolayers for 4.1% lattice mismatch at 300 K) to some tenth of nanometers (e.g. GaP on Si: 45 – 95 nm for 0.36% lattice mismatch at 300 K) at the most. To counteract this issue, the additional integration of e.g. step graded buffer layers in the heterostructure (to overcome the lattice mismatch) is a known approach [162]. Another possibility is the usage of the special feature of the ternary compound semiconductor: By changing the composition of ternary compound semiconductor (e.g.  $In_xG_{1-x}P$ ), the lattice constant, the bandgap and thus the optoelectronic properties of the semiconductors (direct or indirect) can be engineered in the desired way [90, 155, 161].

**Mismatch in thermal expansion coefficients:** Another serious problem for III-V material growth on Si is the large thermal mismatch. When the deposited layer and substrate have different rates of thermal expansion and contraction, the deposited layer can experience considerable tensile or compressive stress during temperature cycle, leading to layer bending, crack formation, delamination or even complete wafer cracking. Table 4 shows as examples the coefficients of thermal expansion (CTE) of Si, Ge, InP, GaP and GaAs at 300 K [161].

Materials	CTE ( $\times 10^{-6} K^{-1}$ )
Si	3.59
Ge	5.78
InP	4.60
GaP	5.30
GaAs	5.40

**Tab.4** Coefficients of thermal expansion values (CTE) of Si, Ge, InP, GaP and GaAs at 300 K [83, 90, 161].

To prevent negative effects due to thermal mismatch, thermal mismatch strain engineering approaches need to be developed (in particular for thick ( $> \mu m$ )) heterostructures. One possible approach is the use of buffer layers of III-V and IV materials with CTE values, which are located between those of the original heterostructure materials (e.g. for GaAs on Si heteroepitaxy, InP or SiGe are suitable intermediate buffer layers for thermal mismatch

engineering (see Tab.4)) [161]. Another possibility is to introduce an additional layer into the heterostructure (e.g. Si pre-deposited on  $\text{Al}_2\text{O}_3$  (sapphire) before GaP growth), which counteracts the stress of different CTEs by bending the system in the opposite direction [163]. It is noted that the thermal mismatch problem is important for virtual substrate engineering where  $\mu\text{m}$ -thick films of alternative semiconductors are integrated on Si wafers on a global scale. However, it is not a major issue for selective  $\text{In}_{1-x}\text{Ga}_x\text{P}$  integration on local device areas with thickness of a few hundred nanometers at maximum.

**Interdiffusion:** The interdiffusion between the III-V material and the substrate is another issue, which has to be taken into account for creation of III-V device structures on Si and Ge (e.g. pn-junctions and HBTs with abrupt pn-junctions). Device structures with required defined doping profiles will suffer from unwanted electrical parasitics, if an atomic interchange across the interface happens during the growth process (also called auto-doping). For example, in a grown GaP/Si(001) heterostructure, Ga-atoms act as p-type and P-atoms as n-type dopants in the Si substrate. Otherwise, Si acts an n-type dopant in the GaP layer, because the ionization energy for Si as donor on Ga lattice position is much lower (0.085 eV) than for Si as acceptor on P lattice position (0.210 eV) [164]. To maintain defined doping characteristics of III-V/SiGe hybrid devices, it is thus useful to work with low thermal budget processes and to monitor the interface diffusion (e.g. by ToF-SIMS control studies) [45, 155, 161].

### 3.2.3 Special aspects of GaP/SiGe/Si(001) heteroepitaxy

As mentioned in the beginning of this paragraph, this part of the thesis deals with GaP heteroepitaxy on SiGe/Si(001) substrates in order to create in future a III-V/SiGe hybrid HBT devices. To be as close as possible to current SiGe HBT designs [5, 6], the thickness and Ge content of the pseudomorphic SiGe base layer were set in this thesis to 20 nm and 20%, respectively. Unlike the GaP growth on Si, much less work has been done for integration of GaP on SiGe so far. Only some papers reported device related integration and studies based on this heterostructure: Examples are the works of E.A. Fitzgerald et al. [162] and A.M. Carlin et al. [165], in which a relaxed graded SiGe buffer system is used for high-quality growth of InGaP or GaP on Si substrates for LED and Solar cell applications, respectively. However, our novel approach for a III-V/SiGe hybrid HBT device faces additional challenges compared to those previous studies of GaP on Si growth:

### **Material science issues:**

GaP heterostructure growth on  $\text{Si}_{0.8}\text{Ge}_{0.2}$  surfaces: First of all, the process parameters working for GaP deposition on Si substrates cannot be directly transferred one-by-one for the GaP deposition on SiGe substrates. For instance, the standard high temperature annealing for removing native oxides and creating double high steps on the surface during the cleaning and preparation procedure has to be modified due to the lower melting point of Ge (938.3 °C) in comparison to Si [83, 90]. Too high annealing temperature will thus result in unwanted surface migration and roughening effect of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer. Another important point to mention is the different atomic composition of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  surface with respect to Si. Knowing e.g. that Ge has a reduced energy barrier for hydrogen migration and especially desorption, the H-terminated  $\text{Si}_{0.8}\text{Ge}_{0.2}$  surface after wet cleaning is easier to activate (i.e. more free dangling bonds on the surface) by temperature with respect to Si. Thus, at the same temperature, this produces a more reactive growing  $\text{Si}_{0.8}\text{Ge}_{0.2}$  surface and can lead to different process dynamics during GaP/  $\text{Si}_{0.8}\text{Ge}_{0.2}$  heteroepitaxy in comparison to GaP growth on pure Si [166].

Pseudomorphism of GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001) heterostructure: In order to achieve best electron transport results in HBT devices, the heterostructure (consisting of emitter, base and collector) in the channel region (i.e. epitaxial part inside the  $\text{SiO}_2$ -mask window (see Fig. 28 & Fig. 29)) has to be pseudomorphic to the Si(001) substrate. This means that, in comparison to the study by *Fitzgerald et al.* [162], the use of relaxed SiGe buffer systems is not feasible due to undesired charge trapping effects of defects, etc. The desired GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001) heterostructure has thus to be perfectly aligned with respect to the in-plane lattice constant of the Si substrate. Therefore, care must be taken on the one hand that the thermal budget and accumulated strain during the GaP deposition does not reach a level, where the pseudomorphic grown  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer on Si relaxes. On the other hand, the needed pseudomorphism of GaP on top of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  holds another challenge due to the (already mentioned) small  $h_{\text{crit}}$  value (<100 nm). Typical HBT designs require a collector thickness in the range of several hundred nanometers, but scaled concepts with limited collector thickness are also discussed [18, 25, 45, 167].

High-quality interfaces: In contrast to applications in the field of LEDs and solar cells, where only the functional  $\text{In}_{1-x}\text{Ga}_x\text{P}$  layer is active and the buffer is just a passive element for growth, HBT devices need perfect epitaxial and defect-free interface (at the EC and CB

junction). Otherwise, containing defects will act as effective traps for charge carriers, which will increase the parasitics and in the end will considerably decrease the HBT performance. Unfortunately (like mentioned before), the deposition of III-V compound semiconductors on Si, Ge and accordingly also  $\text{Si}_{0.8}\text{Ge}_{0.2}$  causes several problems, which easily introduce crystalline defects (like APDs, SFs, MTs and MDs) into the deposited III-V layer and the interface with respect to growth of  $\text{Si}_{0.8}\text{Ge}_{0.2}$  on Si. Experiences from the literature show that these defects are hard to control and complete defect elimination at the III-V/SiGe interface region is probably very difficult [18, 89, 91-95, 125, 127-132, 168, 169].

**Process integration:** In the end, we take an outlook on possible challenges, which arise in process integration of  $\text{In}_{1-x}\text{Ga}_x\text{P}$  collectors in future III-V/SiGe hybrid HBT devices. It is here to mention that solving the problems above in the frame of this heterostructure growth studies mark only the start of a longer research and development process on the way to integrate III-V/SiGe hybrid HBT devices into Si microelectronics.

Selective deposition and etching of III-V on Si: Obviously, growing an InGaP/SiGe/Si(001) heterostructure is not enough to create a technology-relevant III-V/SiGe hybrid HBT device. The heterostructure has to be embedded into the established BiCMOS platform using lithography, selective growth and etching techniques. At this point, another big challenge arises: Like most III-V materials,  $\text{In}_{1-x}\text{Ga}_x\text{P}$  has no decent grown oxide, which could be used for patterning (unlike e.g.  $\text{SiO}_2$  for Si). Therefore, standard  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$  masks have to be used in combination with selective deposition recipes. In the literature, recent selective growth studies of III-V materials on Si and Ge (e.g. GaAs and InP on Ge; InSb on Si) were reported using MBE and MOCVD growth techniques, in which a successful selectivity on  $\text{SiO}_2$  patterned substrates has been achieved [170, 171]. However, the improvement of III-V crystal quality (concerning e.g. segregation, defects, facet formation and roughness) is today still an area of research and development for possible industrial application. Nevertheless, using patterned mesa structures for III-V heteroepitaxy is advantageous with respect to the planar global case, as it is expected that the arms of dislocations threading through the layer and moving by the so introduced strain field will be stopped at the window sidewalls and will be thus trapped at the  $\text{SiO}_2$  mask. This approach is known e.g. under the aspect ratio trapping (ART)-approach [172-175]. Another method for device structuring is for example the selective etching. Unfortunately, this technique is not a suitable option to circumvent the selective growth challenge of III-V materials. Like in the case of GaP, most III-V materials

have almost no etchant for selective removal to SiO<sub>2</sub> or consist of chemicals (i.e. Br/CH<sub>3</sub>OH(solvent), K<sub>3</sub>[Fe(CN)<sub>6</sub>]), that are inappropriate for applications in Si CMOS microelectronic production lines [176, 177].

Heat conduction: Today, modern transistor structures increases more and more in performance and decreases more and more in size. This trend results in an increasing self-heating problem, which degrades the function and the lifetime of the semiconductor device. Table 5 shows exemplary the thermal conductivity (TC) of Si, Ge, InP, GaP and GaAs at 300 K [83]:

Materials	TC (W cm <sup>-1</sup> K <sup>-1</sup> )
Si	1.30
Ge	0.58
InP	0.68
GaP	1.10
GaAs	0.55

**Tab.5** Thermal conductivity values (TC) of Si, Ge, InP, GaP and GaAs at 300 K [83].

Depicted in Tab. 5, III-V compound semiconductors are in general poor thermal conductors with respect to Si, which might result in additional local heat accumulation during III-V/SiGe HBT device operation [18].

Doping of III-V materials: Besides the above mentioned issue of auto-doping of III-V materials on Si and Ge by interdiffusion, the doping of III-V compound semiconductors itself is in some parts quite different with respect to pure group IV materials. The first possibility (rather similar approach to group IV doping) is to replace the group III atoms by group II atoms and the group V atoms by group VI atoms in order to create acceptors and donors, respectively. Another possibility is the amphoteric doping by replacing both the group III and group V atoms by group IV atoms, where they act as a donor on the group III-site and as an acceptor on a group V-site, simultaneously. In literature, various dopants are reported for these cases (e.g. Be, Mg, Si, Sn, Se and Te) in a doping concentration range of  $2 \times 10^{17} \text{ cm}^{-3}$  –  $1.2 \times 10^{19} \text{ cm}^{-3}$  [169, 178, 179]. Finally, doping can be achieved also by replacing the atoms of the III-V material by an isoelectronic atom (i.e. for example changing a group III element by some other group III element). For pure semiconductors of group IV, this effect is negligible, but in III-V materials this procedure results in local potential differences



due to changes in the ionic bindings of the material.

It is to mention that for a highly doped n-type InGaP collector ( $> 1 \times 10^{17} \text{ cm}^{-3}$ ) as part of a III-V/SiGe hybrid HBT device, it is crucial to evaluate the best doping technique with respect to dopant diffusion, achievable active doping levels and Si CMOS compatibility.

### 3.2.4 Experimental studies

**Lattice mismatch and critical thickness of GaP on Si:** The evaluation study of  $\text{In}_{1-x}\text{Ga}_x\text{P} / \text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures for potential HBT applications starts with the theoretical consideration of lattice misfit and critical thickness for pseudomorphic GaP growth on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrates. The first parameter to consider is the natural lattice misfit  $f$  between two different materials defined by *Matthews* [180]:

$$f = \frac{a - b}{b} \quad (46)$$

where  $a$  and  $b$  are lattice constants of overgrowth and substrate, respectively. Since 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$  grow pseudomorphically on Si(001) substrates, the natural misfit can be calculated between GaP and Si(001) (Lattice constants are listed in Tab.I.). With a determined natural misfit of 0.36%, the average distance  $p_d$  between two MD defects [180],

$$p_d = \frac{a}{f} = \frac{ab}{a - b} \quad (47)$$

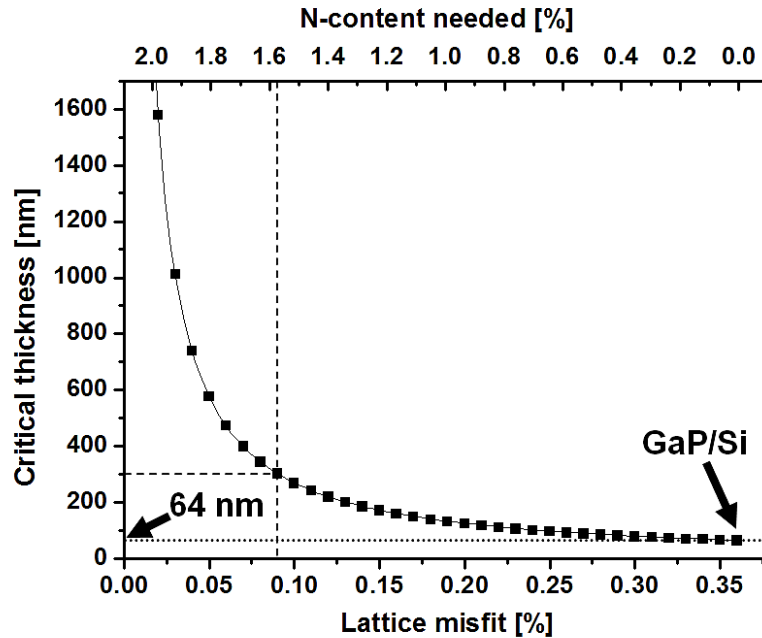
results in a value of 152 nm for relaxed GaP on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$ . It is noted that the lateral misfit of GaP on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures is quite low and the average MD distance quite high, nevertheless the task to grow pseudomorphic GaP on  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  is challenging.

A further important heteroepitaxy parameter is the critical thickness  $h_{\text{crit}}$  for GaP growth on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrates. Following the approach of *Fischer et al.*,  $h_{\text{crit}}$  is given by [181]:

$$f = \frac{b \cdot \cos \lambda}{2 \cdot h_{\text{crit}}} \cdot \left( 1 + \left( \frac{1 - (\nu/4)}{4\pi \cdot \cos^2 \lambda \cdot \cos \phi \cdot (1 + \nu_x)} \right) \ln \left( \frac{h_{\text{crit}}}{b} \right) \right) \quad (48)$$

where  $f$  is the lattice misfit,  $b$  is the magnitude of the Burgers vector of the dislocations ( $\frac{1}{2} a \langle 110 \rangle$  in fcc lattices, inclined at  $45^\circ$  to (001) [27]),  $\nu_x$  is the Poisson ratio,  $\lambda$  the angle

between the Burgers vector and the  $\langle 110 \rangle$  dislocation lines, and  $\phi$  is the angle between the  $\langle 111 \rangle$  slip plane normal and the  $\langle 110 \rangle$  azimuthal axis. Figure 70 shows  $h_{crit}$  values of GaP on Si(001) for different lattice mismatch calculated from the equilibrium theory for strain relaxation in metastable heteroepitaxial semiconductor structures [90]:

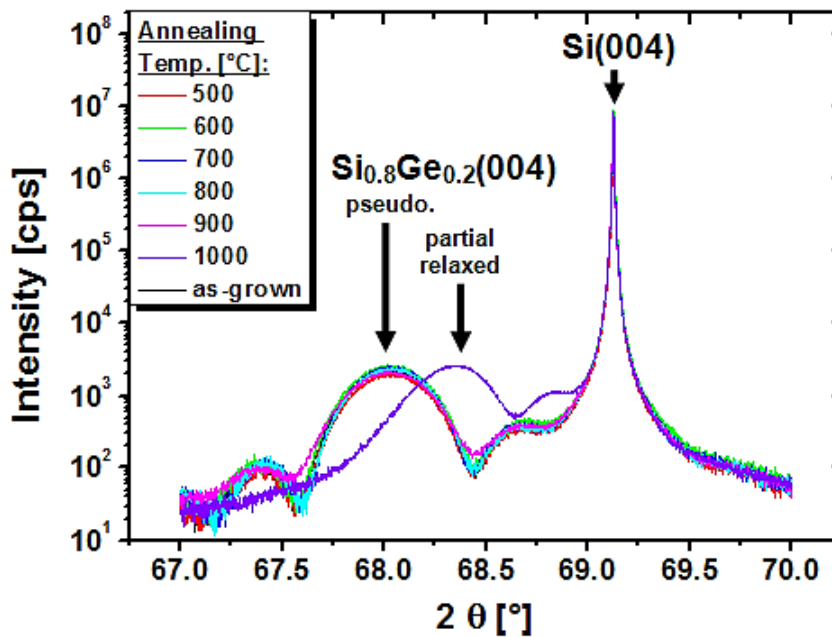


**Fig.70** Critical thickness  $h_{crit}$  vs lattice misfit as a function of N-content in  $\text{GaP}_{1-x}\text{N}_x$  ( $x = 0 - 0.02$ ) systems [90].

Under the assumption that pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}$  on Si(001) counts together as one layer with the in-plane lattice constant of Si, and inserting appropriate material parameters in the equation above ( $f = 0.0036$ ,  $b = 3.840 \text{ \AA}$ ,  $\nu = 0.31$ ,  $\cos\lambda = 0.5$  and  $\cos\phi = 0.816$  for growth on Si(001) surfaces [83]), the value of  $h_{crit}$  for GaP is 64 nm (Fig. 70). In published experimental data for GaP/Si(001) systems,  $h_{crit}$  is reported to vary between 45 and 95 nm [182][183], which corresponds well in magnitude to our theoretical result. However, it should be noted that the calculated result here is a thermodynamical value. Experimental observations show usually higher values of  $h_{crit}$  due to kinetic hindrance for defect injection in pseudomorphic layers. Nevertheless, the value of  $h_{crit}$  for GaP might be too low, as typical HBT designs require a collector thickness in the range of several hundred nanometres [18, 25, 45, 167]. Hence, it is interesting to point out that nitrogen incorporation in GaP can be used to reduce the misfit between  $\text{GaP}_{1-y}\text{N}_y$  and Si(001), which substantially increase  $h_{crit}$ . Figure 70 shows the decrease of lattice mismatch as a function of N-content in  $\text{GaP}_{1-y}\text{N}_y$  systems. For example,  $h_{crit}$  moves to  $\approx 300 \text{ nm}$  for  $\approx 1.57 \%$  N incorporation lattice mismatch

of  $\text{GaP}_{1-y}\text{N}_y$  with Si decreases to 0.09. It is noted that P substitution by N is responsible for the decrease of the  $\text{GaP}_{1-y}\text{N}_y$  lattice parameter with respect to GaP, but also more complex electronic properties are affected by N incorporation [90, 184, 185].

**Investigation of thermal budget:** In order to ensure that the thermal budget during GaP growth does not induce relaxation processes in the pseudomorphic 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrate, an XRD thermal budget study was performed. For this purpose, samples with 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$  pseudomorphically grown on Si(001) substrates were annealed in a temperature range from 500 °C to 1000 °C for 30 min in  $\text{N}_2$  atmosphere using an ex-situ furnace (introduced in section 2.2). Subsequently, specular  $\theta/2\theta$  XRD measurements were performed to investigate changes in the  $\text{Si}_{0.8}\text{Ge}_{0.2}(004)$  diffraction curves of the annealed samples with respect to the as-grown sample. By this method, it is possible to detect relaxation processes in the present heterostructure. Figure 71 summarizes the results of the thermal budget study [90]:



**Fig.71** Specular  $\theta/2\theta$  XRD scans of as-grown  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  samples and after annealing at 500 – 1000 °C in  $\text{N}_2$  atmosphere. Process pressure and annealing time were 1 atm and 30 min, respectively [90].

For a better comparison of  $\text{Si}_{0.8}\text{Ge}_{0.2}(004)$  peak position changes relative to the Si(004) peak, the collected XRD curves were aligned to the Si(004) peak position at as-grown condition. The samples, annealed between 500 °C – 900 °C, show no shift in the (004) Bragg peak position of the pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}$ . At 900 °C, however, an increase at the diffraction

minima of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  Bragg peak fringes could be observed. When the temperature increases further to 1000 °C, a clear change in the  $\text{Si}_{0.8}\text{Ge}_{0.2}(004)$  peak position towards a larger angle closer to the Si(004) peak is visible. In conclusion, three insights can be gained from this thermal budget study: Firstly, no relaxation occurred on the samples after applying a thermal budget of up to 800 °C. The 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure substrate for GaP deposition remained pseudomorphic. Secondly, the increase at the diffraction minima of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  Bragg peak fringes at 900 °C indicates the onset of relaxation processes due to MD generation at the  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  interface. Thirdly, the degree of relaxation of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer increases strongly between 900 °C and 1000 °C. At 1000 °C, a value of about 60% relaxation is reached. This observed behavior is a typical example for relaxation processes in pseudomorphic SiGe/Si layers during annealing procedures [186]. These gained insights consequently imply for the GaP growth on 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  that the growth temperature must not exceed 800 °C to maintain pseudomorphism of the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer on Si(001) [90].

In the following, the experimental results of 170 nm GaP on 20 nm pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures will be presented:

**Epitaxy relationship and relaxation characterization:** For determination of the pseudomorphic character of the  $\text{GaP}/\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure, a specular  $\theta/2\theta$  XRD measurements near the Si(004) Bragg peak position was performed. The result is depicted in Fig. 72. Compared to Fig. 71, a broad GaP(004) reflection is visible, which is neither situated at its bulk position nor at the value estimated with the help of the Poisson ratio for pseudomorphic GaP ( $\nu_x = 0.31$  [83]). The relation between off-plane ( $a_1$ ), in-plane ( $a_0$ ), and bulk ( $a$ ) lattice constant can be calculated with the Poisson ratio  $\nu_x$  by the equation [90, 187]:

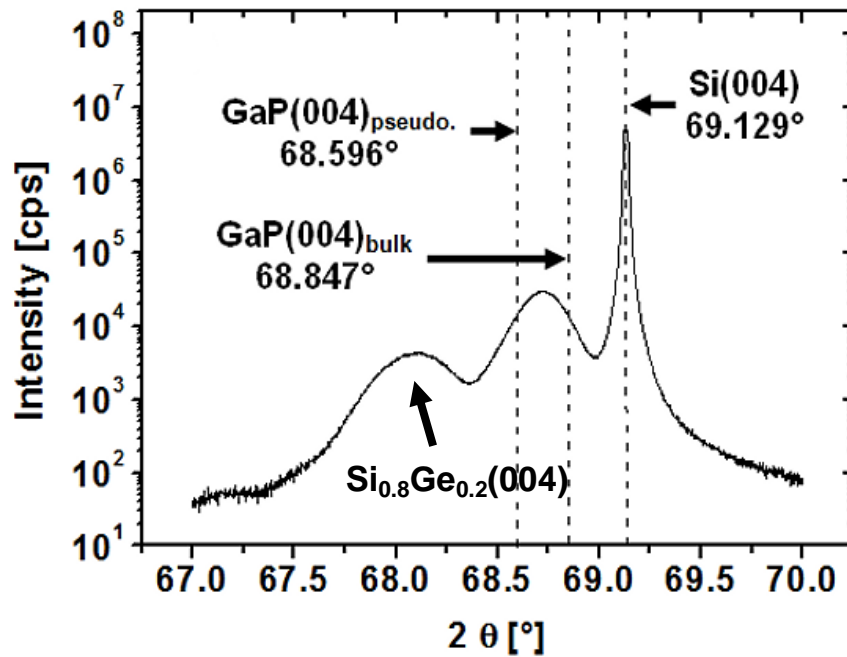
$$\frac{(a_1 - a)}{a} = \frac{(a_0 - a)}{a} \cdot \frac{-2\nu_x}{(1 - \nu_x)} \quad (49)$$

with

$$a_1 = a \cdot (1 + K_X) - a_0 K_X \quad (50)$$

or

$$K_X = \frac{2\nu_x}{(1 - \nu_x)} \quad (51)$$

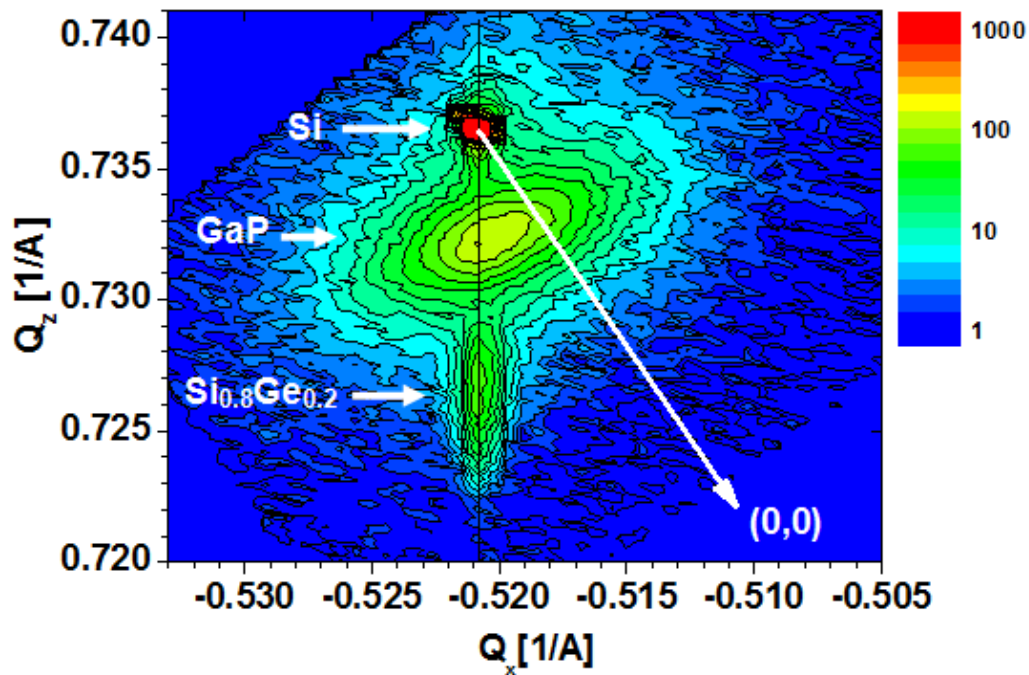


**Fig.72** Specular  $\theta/2\theta$  XRD measurement after 170 nm GaP deposition on 20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrate [90].

This result indicates that the 170 nm deposited GaP layer is crystalline and (001) oriented, but contains structural defects and grows partially relaxed on the Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrate. Interestingly, the Si<sub>0.8</sub>Ge<sub>0.2</sub>(004) Bragg peak position shows a slight shift to larger angles after GaP deposition. Considering the position and width of the GaP(004) peak in close vicinity to the Si<sub>0.8</sub>Ge<sub>0.2</sub>(004) reflection, this slight shift can be explained by mutual interference of the thickness fringes of both layers [90].

To confirm that 20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) is still pseudomorphic despite the misfit strain exerted by 170 nm GaP, RSM of the asymmetric ( $\bar{2}\bar{2}4$ ) reflections of Si, GaP and Si<sub>0.8</sub>Ge<sub>0.2</sub> was performed and is shown in Fig 73. It should be noted for reasons of clarity that the Q<sub>z</sub>-axis in Fig. 73 is parallel to (004) net plane normal and the Q<sub>x</sub>-axis is perpendicular to Q<sub>z</sub> in the diffraction plane. Figure 73 shows a sharp Si( $\bar{2}\bar{2}4$ ) signal from the high quality Si(001) substrate. The Si<sub>0.8</sub>Ge<sub>0.2</sub>( $\bar{2}\bar{2}4$ ) reflection shows otherwise a lower signal intensity and exhibits an ellipsoidal shape. The small full width at half maximum (FWHM) in Q<sub>x</sub> direction is comparable to Si( $\bar{2}\bar{2}4$ ), indicating a high crystal quality of the SiGe layer. The bigger FWHM in Q<sub>z</sub> direction is due to the finite Si<sub>0.8</sub>Ge<sub>0.2</sub> layer thickness of 20 nm. The Q<sub>x</sub> positions of the Si<sub>0.8</sub>Ge<sub>0.2</sub>( $\bar{2}\bar{2}4$ ) and the Si( $\bar{2}\bar{2}4$ ) reflection are identical, demonstrating that both layers have the same in-plane lattice constant. A full relaxation of Si<sub>0.8</sub>Ge<sub>0.2</sub> would otherwise be

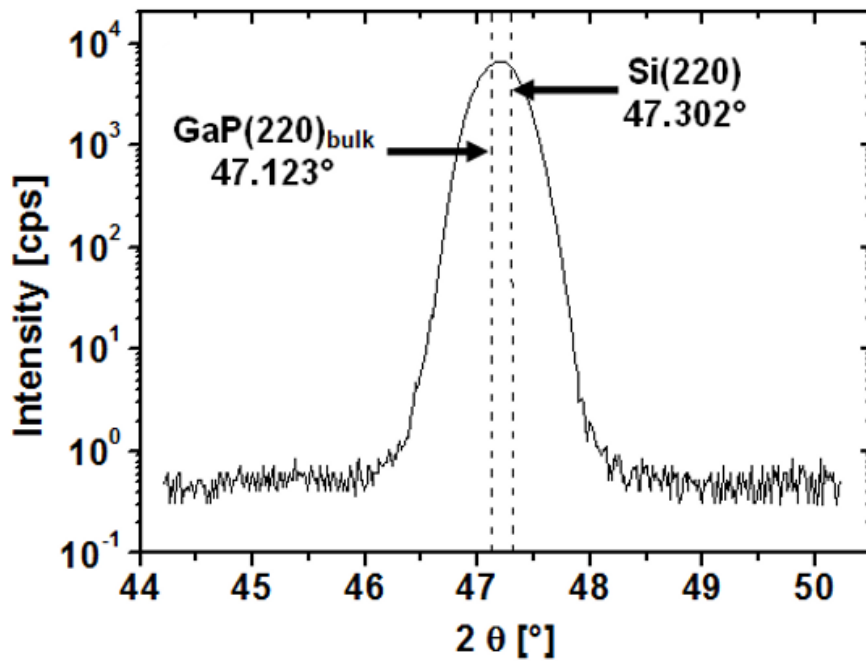
expressed by  $Q_x$  peak shift to a position between Si( $\bar{2}24$ ) peak position and the (0,0) origin direction of reciprocal space (indicated by arrow in Fig. 73) [90].



**Fig.73** RSM of asymmetric ( $\bar{2}24$ ) reflections of Si, GaP, and  $Si_{0.8}Ge_{0.2}$  measured for the 170 nm GaP/20 nm  $Si_{0.8}Ge_{0.2}$ /Si(001) sample. [90].

As a result, no relaxation processes has taken place so that the 20 nm  $Si_{0.8}Ge_{0.2}$  layer remains pseudomorphic on Si(001) after 170 nm GaP deposition. This result is positive for a potential HBT collector application of GaP, which requires a stable pseudomorphic base layer enduring a deposition of several hundred nanometres of collector material on top [18, 25, 45, 167]. In contrast, the deposited GaP layer is characterised by a broad GaP( $\bar{2}24$ ) reflection with diffusive scattering, suggesting the presence of structural defects [188]. In addition, GaP( $\bar{2}24$ )  $Q_x$  position is partly shifted (towards arrow in Fig. 73), confirming a partial relaxation of the deposited GaP layer [90].

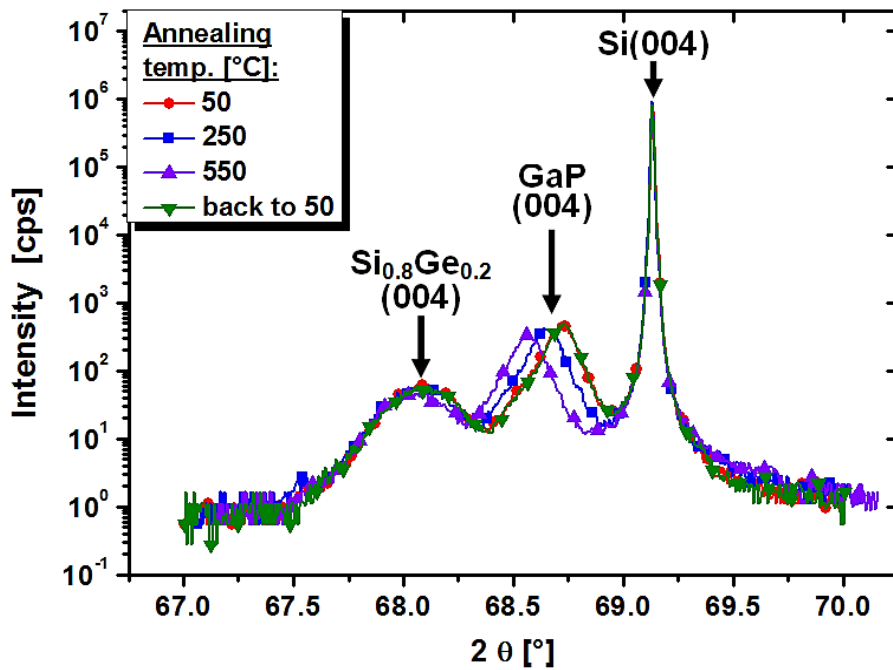
To determine the relaxation degree in detail, in-plane measurement of the Si(220) Bragg peak position were also performed and is depicted in Fig. 74. After all, from the GaP(004) out of plane and GaP(220) in-plane peak positions, strain relaxation degree of about 40% was determined for the 170 nm thick GaP film. It is noted, that the experimentally derived Poisson ratio of 0.33, using the in- and out of plane lattice constants, fits well to literature [83, 90, 189].



**Fig.74** In-plane (220) XRD measurement after 170 nm GaP deposition on 20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) substrate [90].

In conclusion, the epitaxial relationship of the single crystalline heterostructure is given by GaP[001];<110> || Si<sub>0.8</sub>Ge<sub>0.2</sub>[001];<110> || Si[001];<110>. While the pseudomorphism of the 20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) system is maintained during heteroepitaxial overgrowth of 170 nm GaP, the GaP structure itself grows partially relaxed by about 40% [90].

**Thermal expansion coefficient study:** A possible origin of the partial GaP relaxation is the lattice mismatch between GaP and the pseudomorphic Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001), which additionally increases at higher temperature due to different coefficients of thermal expansion (CTE). Therefore, we studied the impact of different CTE on the relaxation behavior of a 170 nm GaP/20 nm Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructure. For this purpose, the sample was placed in a furnace on the SmartLab diffractometer under 1 bar N<sub>2</sub> atmosphere (see section 2.2). The sample was heated in 50 °C steps up to 550 °C and in-situ θ/2θ XRD measurements were performed after 15 min annealing time at every step. Higher postannealing temperatures are not suitable, because uncovered GaP layers start to decompose [190, 191]. After cooling down back to 50 °C, a final θ/2θ XRD measurement was carried out. Figure 75 shows only the 50 °C, 250 °C, 550 °C and the back to 50 °C results of this experiment for the sake of clarity [90]:

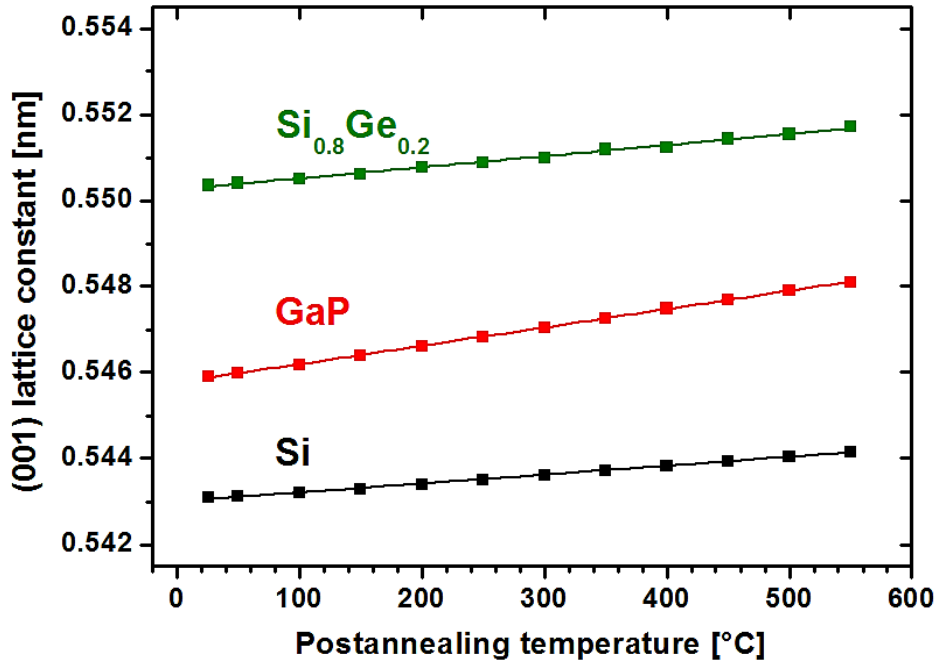


**Fig.75** Specular  $\theta/2\theta$  XRD scan of 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  postannealed at 50 °C, 250 °C, 550 °C and cooled down back to 50 °C. Postannealing applied under  $\text{N}_2$  atmosphere at a pressure of 1 atm [90].

Due to increasing annealing temperatures, the (004) peak positions of Si,  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and GaP will shift according to their CTE values to smaller angles. However, for a better comparison and depiction of GaP(004) and  $\text{Si}_{0.8}\text{Ge}_{0.2}$ (004) peak position changes relative to the Si(004) peak, the collected XRD curves were aligned to the Si(004) peak position at 50 °C in Fig. 75. Two main insights were drawn from these data: First, the graphs before and after the applied annealing procedure perfectly superimpose. Supposed that the relaxation of GaP occurs at the growth temperature of 450 °C by generation of MDs, the 100 °C higher temperature in this experiment and following by higher misfit should lead to a continuation of the relaxation process. However, this is not the case and this probably points to the fact that the observed partial relaxation of grown GaP layer originates not from plastic relaxation due to defect insertion into the closed GaP film, but rather from growth defects. Secondly, the GaP(004) peak position changes with increasing temperature over a higher angular range than the  $\text{Si}_{0.8}\text{Ge}_{0.2}$ (004) Bragg peak, pointing to a higher GaP CTE value [90].

To derive the CTE values, we plot in Fig. 76 the out of plane lattice constant of Si,  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and GaP from the out of plane high temperature in-situ XRD study [90]:





**Fig.76** (001) lattice constants of GaP, Si<sub>0.8</sub>Ge<sub>0.2</sub>, and Si layers vs. temperature [90].

As all out of plane lattice constant values of all three layer materials increase linearly with raising annealing temperature, the linear CTE values were extracted by using the equation [90, 187]:

$$CTE_{Si} = \frac{\Delta a_{Si}}{a_{Si}} \cdot \frac{1}{\Delta T} \quad (52)$$

where  $a$  is the lattice constant at 300 K and  $\Delta a$  the change with increasing temperature. A CTE value of  $(3.8 \pm 0.7) \cdot 10^{-6} \text{ K}^{-1}$  was found for Si, which agrees (within the error range) with literature for free standing bulk Si ( $3.6 \cdot 10^{-6} \text{ K}^{-1}$ ) [187]. To derive the CTE values of the thin GaP and Si<sub>0.8</sub>Ge<sub>0.2</sub> layers, we must correct for the influence of the bulk Si substrate by the equation [90, 187]:

$$CTE_X = \frac{1}{\Delta T} \cdot \left( \frac{a_{1,X,T_1} + (a_{0,X,T_0} + a_{Si,T_0} \cdot CTE_{Si} \cdot \Delta T) \cdot K_X}{a_{X,T_0} \cdot (1 + K_X)} - 1 \right) \quad (53)$$

with

$$K_X = \frac{2 \nu_X}{(1 - \nu_X)} \quad (54)$$

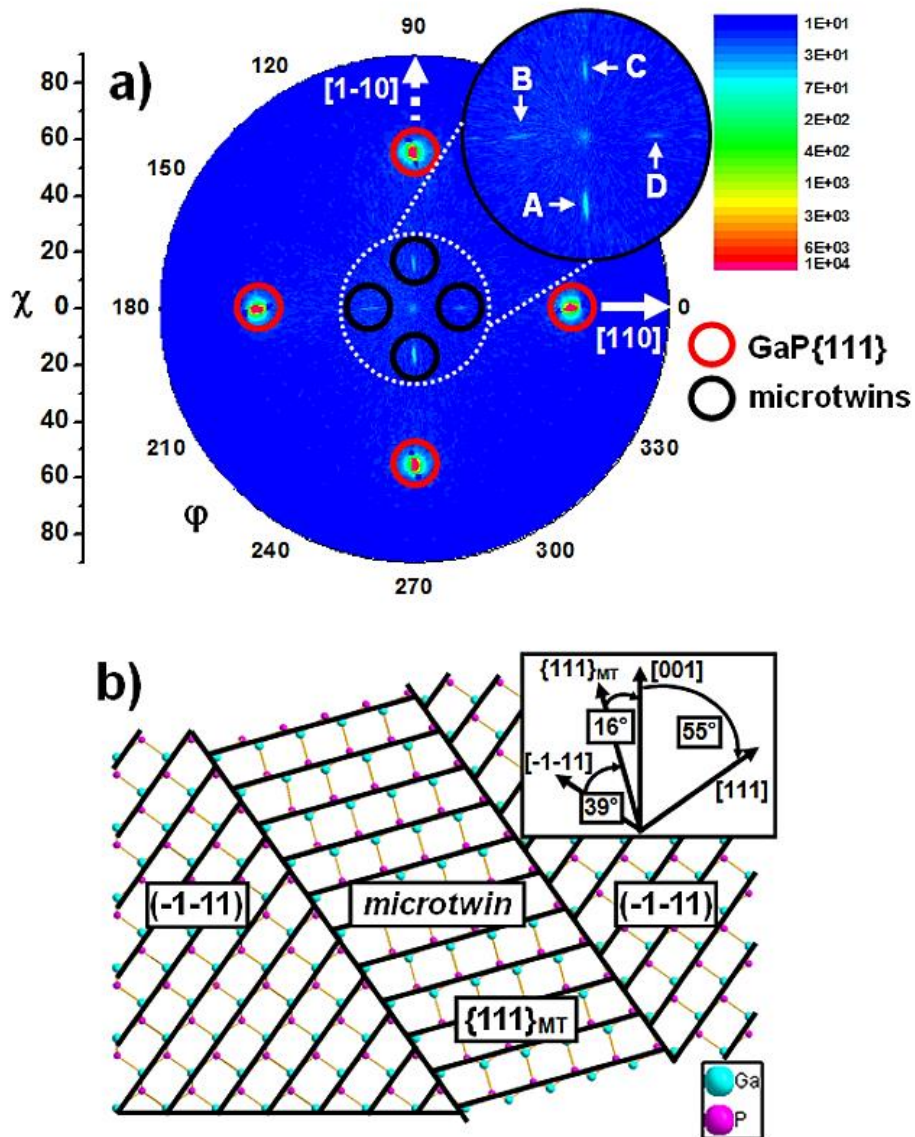
where  $a_{l,x,T_1}$  is the out of plane lattice constant at  $T_1$ ,  $a_{0,x,T_0}$  is the in-plane lattice constant at  $T_0$  and  $a_{x,T_0}$  is the value of the bulk lattice constant at  $T_0$  of the top layers ( $x$  either  $\text{Si}_{0.8}\text{Ge}_{0.2}$  or GaP).  $a_{\text{Si},T_0}$  and  $\text{CTE}_{\text{Si},T_0}$  are the lattice constant and the linear CTE of the Si substrate at  $T_0$ , respectively. The Poisson ratio  $\nu_x$  of the top layer material used in this calculation was taken from literature (0.28 for  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and 0.33 for GaP [83]). Using the in-plane lattice constant of Si(001) for pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}$  on top and the in-plane lattice constant for GaP measured at 300 K (see Fig. 71), it is possible to derive the linear CTE related to free-standing bulk material averaged over the range from RT to 550 °C as  $\text{CTE}_{\text{Si}_{0.8}\text{Ge}_{0.2}} = (4.1 \pm 0.7) \cdot 10^{-6} \text{ K}^{-1}$  and  $\text{CTE}_{\text{GaP}} = (5.9 \pm 0.7) \cdot 10^{-6} \text{ K}^{-1}$  [90].

In conclusion, although GaP exhibits a higher CTE than  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and Si, no additional plastic relaxation occurred by the thermal budget applied during the high temperature treatment (up to 550°C; 15 min). Therefore, the observed partial relaxation of 170 nm GaP cannot be explained by lattice mismatch effects only and has to follow a different relaxation process mechanism, as discussed further below [90].

**XRD defect study:** Relaxation processes in semiconductor films are caused by different kinds of defect formation. Plastic relaxations occur due to growth of closed films beyond  $h_{\text{crit}}$ , creating MDs on the heterostructure interface after for example defect insertion by half loop nucleation. A different possible relaxation mechanism in semiconductor films are due to coalescence processes of initial 3D islands during growth, which are susceptible to form growth defects like SFs and MTs [91, 192]. To learn more about the influence of these growth defects on the partial relaxation of the GaP structure, XRD was applied for defect characterization. To verify the presence of MTs in the GaP(001) layer [145], a XRD GaP(111) PF study was carried out on the same 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001) sample, which was annealed in the thermal expansion coefficient study. Figure 77(a) shows the result of the PF measurement. Due to the fourfold symmetry, four symmetric GaP(111) Bragg peaks at  $\chi \approx 55^\circ$  were measured (indicated by the red circles), corresponding to the sketched angle between GaP(001) surface orientation and  $\{111\}$  GaP lattice planes in Fig. 77(b). Additionally, four also symmetrically orientated GaP $\{111\}$  Bragg peaks with far lower intensity were detected at  $\chi \approx 16^\circ$  (indicated by black circles and by close-up), matching the sketched angle between  $\{111\}_{\text{MT}}$  planes of MTs and [001] surface normal in Fig. 77(b) [90].

In summary, it can be stated that MT formation in the grown GaP(001) layer

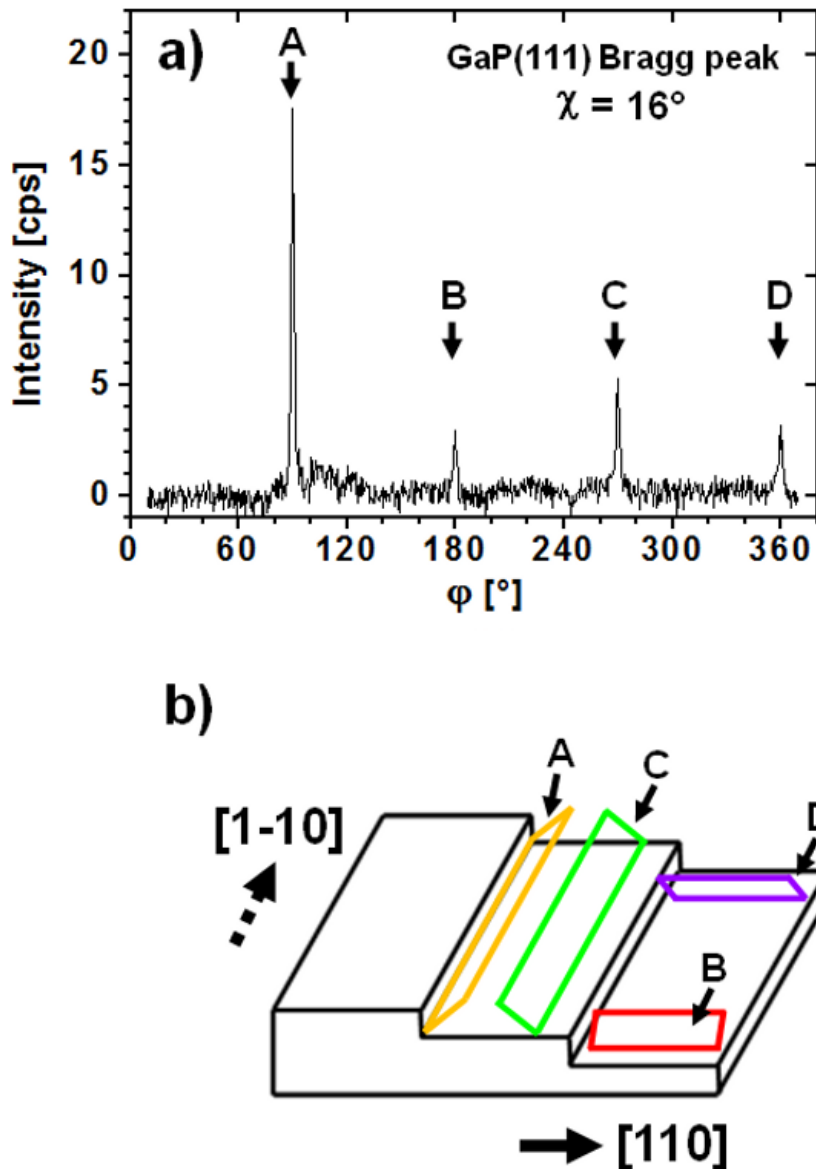
appears, creating additional  $\{111\}_{MT}$  planes, which are tilted by  $39^\circ$  in  $\chi$ -direction away from the original  $\{111\}$  planes of the ideal GaP film structure (Fig. 77(b)) [90, 143, 187].



**Fig.77** (a) XRD PF measurement adjusted on the GaP(111) reflection performed after postannealing of a 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  sample at  $550^\circ\text{C}$  for 15 min under 1 atm  $\text{N}_2$ . (b) Sketch of MT formation in (001) oriented GaP layers [90].

To study the MT formation in GaP layer in more detail, a circular  $\phi$ -scan ( $0 - 360^\circ$ ) at fixed position  $\chi = 16^\circ$  and on the  $2\theta$  value of  $\text{GaP}(111)_{MT}$  was performed. Figure 78(a) clearly depicts an anisotropic MT nucleation behavior [90]:

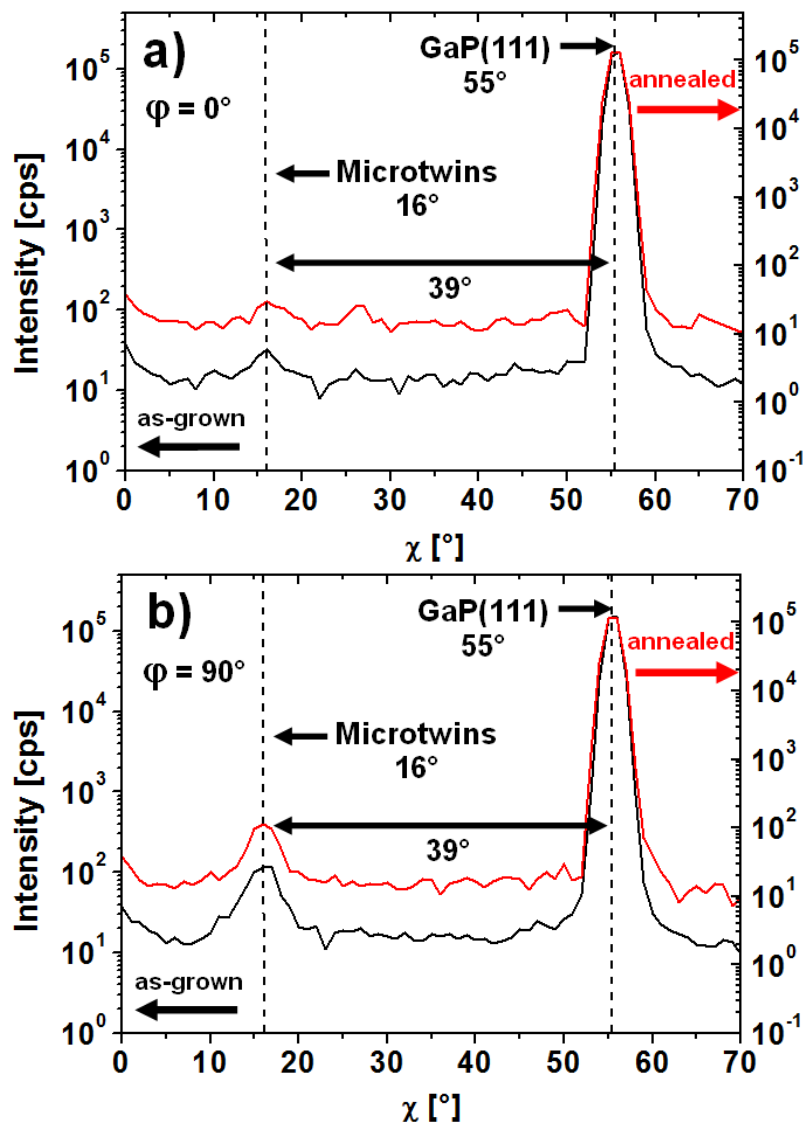
MT density is generally higher along  $[110]$  direction (bold arrow in Fig. 77(a) & Fig. 78(b); A & C) than along  $[1\bar{1}0]$  direction (dashed arrow in Fig. 77(a) & Fig. 78(b); B & D).



**Fig.78 (a)** XRD  $\phi$ -scan on GaP(111) Bragg reflection at  $\chi = 16^\circ$ . **(b)** Schematic sketch of MT orientation with respect to  $4^\circ$  off-oriented substrates [90].

Taking the use of a  $4^\circ$  off-orientated Si(001) substrate into account (Fig. 78(b)), it is thus demonstrated that MT formation along the  $[110]$  double step direction (solid arrow directions) is higher in comparison to the  $[1\bar{1}0]$  direction parallel to the step edge (dashed arrow directions). For example, the highest amount of MTs (A) emerge therefore along the  $[110]$  direction oriented away from the double steps. It is noted that this anisotropic behavior of the MT formation in GSMBE grown GaP on  $4^\circ$  off-oriented  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  is different from the results observed for GaP on Si grown by MOCVD [90, 193].

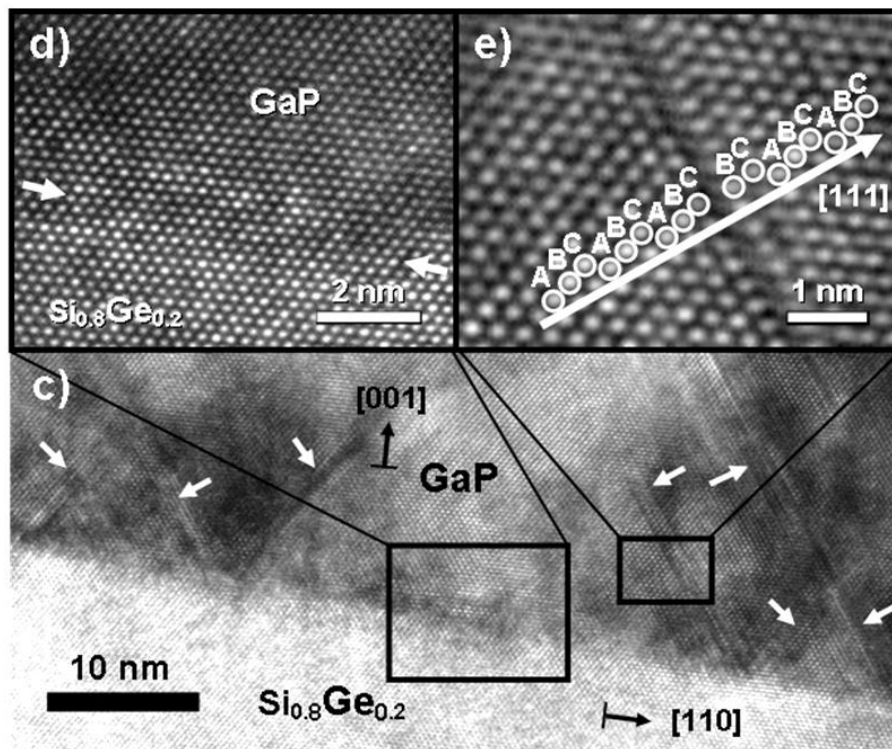
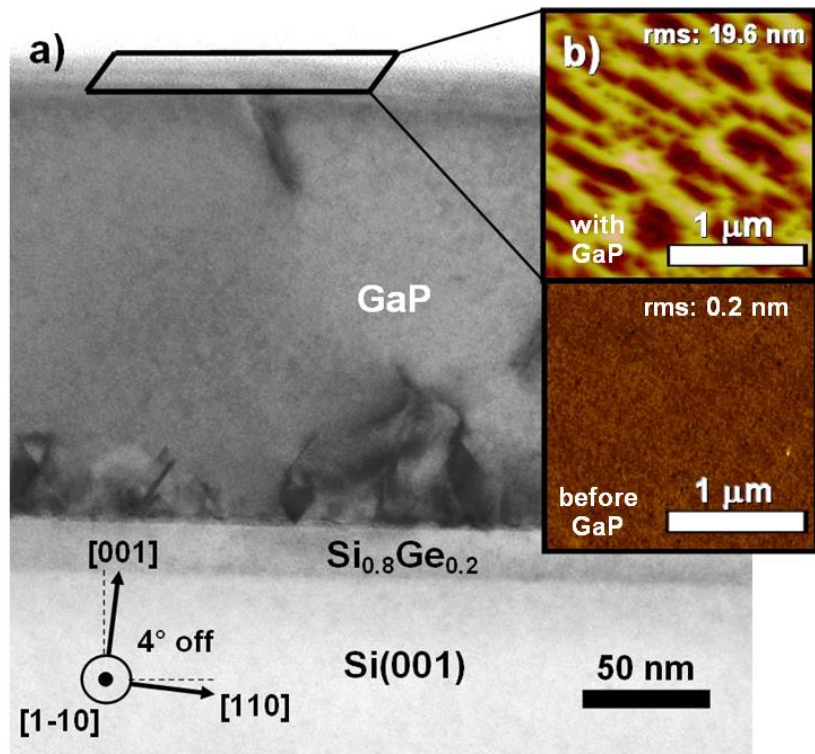
Finally, the MT concentration and anisotropic behaviour after the annealing process were compared with preliminary as-grown XRD datasets. Figure 79 shows an example of two XRD line scans ( $\chi = 0 - 70^\circ$ ) along  $[110]$  direction (bold arrow in Fig. 77(a) & Fig. 78(b); C) and along the  $[1\bar{1}0]$  direction (dashed arrow in Fig. 77(a) & Fig. 78(b); D). Investigating all orientation directions, no difference in MT concentration and anisotropic behavior were found comparing annealed and as-grown samples. This result confirms that the above applied postannealing process does not reduce the number of existing MTs. It is noted that one possible and recently reported approach for future attempts to remove MTs could be laser annealing [194].



**Fig.79** XRD line scans along the (a) dashed  $[110]$  ( $\varphi = 0^\circ$ ) and (b) solid  $[1\bar{1}0]$  ( $\varphi = 90^\circ$ ) arrow direction in Fig. 75(a) extracted from PF datasets of postannealed (red lines) and as-grown (black lines) 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  samples.

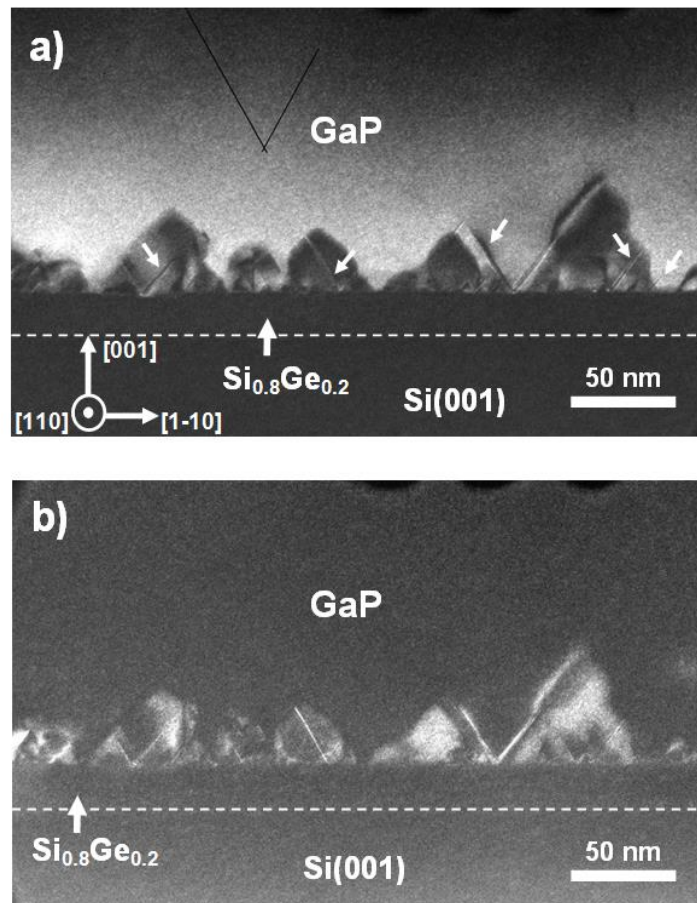
**TEM defect study:** For a further investigation of the defect structure in the deposited 170 nm thick GaP layers on top of the 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrate, a cross section TEM study was carried out. Figure 80(a) shows the TEM images of the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$   $4^\circ$ -off oriented heterostructure projected along the  $\langle 1\bar{1}0 \rangle$  azimuth (parallel to the step edges). The TEM image indicates a very high crystal quality of the Si(001) substrate and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer combined with very sharp interface between these two layers without any visible defects (or residual oxide interfacial layers). Furthermore, Fig. 80(a) depicts a crystalline and continuous GaP layer grown on top of  $\text{Si}_{0.8}\text{Ge}_{0.2}$ . However, AFM images in Fig. 80(b) show over a bigger scale ( $2 \times 2 \mu\text{m}^2$ ) an increase in surface root mean squared (rms) roughness after GaP deposition from 0.2 nm to 19.6 nm. Most interestingly, the interface between GaP and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  is more defective than the upper GaP part. Most of these observed defects are annihilated after about 70 nm GaP thickness. Only a few defects, situated on  $\{111\}$  glide planes, are located at larger thicknesses or even reach the surface. This TEM result reports strong evidence that these defects are mainly growth defects. Such growth defects do not nucleate by plastic relaxation of strained, closed 2D thin film structures, but mostly during the coalescence process of a film structure formed by initial 3D island nucleation processes [90, 95, 192, 193].

To determine the interface quality between GaP and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  in more detail, a HRTEM image is shown in Fig. 80(c). Firstly, an enlarged section of the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface is displayed in Fig. 80(d) to demonstrate the high quality of the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  heteroepitaxy. Due to the weak contrast, no clear GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface transition (indicated by arrows) and no double step characteristics resulting from the use of  $4^\circ$ -off oriented substrates can be identified. Secondly, Figure 80(c) demonstrates in addition that the GaP interface layer contains SFs on GaP $\{111\}$  planes (also indicated by arrows). Some of these propagating SFs are annihilated after their creation near the interface by building a triangular structure that inhibits further expansion of this defect. Figure 80(e) shows as an example an intrinsic SF on a (111) plane. Assuming the normal stacking order ABCABCABC along  $[111]$  direction, stacking disorder is depicted as ABC\_BCABCA (A-plane missing). It is noted that no clear indication of MDs were found in our HRTEM images for the 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure. This is expected because, due to the small lattice mismatch, MDs are separated by about 152 nm for fully relaxed GaP on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  and even larger distances are expected for partially relaxed GaP layers [180].



**Fig.80** Cross section TEM image (a) and AFM surface images (before and after GaP deposition) (b) of 170 nm GaP on pseudomorphic 4° off-oriented Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001). High resolution TEM image of the interface region between Si<sub>0.8</sub>Ge<sub>0.2</sub> and GaP layers (c), as well as close-up images of a well grown interface area (d) and an intrinsic stacking fault (open circles labelled with ABC show stacking order along the {111} direction) (e) [90].

Next, APD defect characterization of the deposited 170 nm GaP layers was performed using the  $\{002\}$  DF TEM imaging technique. It is known that  $\{002\}$  reflections are especially sensitive to APDs, revealing this defect type in form of reversed contrast changes [95, 128, 193]. Figure 81 shows a cross section DF HRTEM image pair of the 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure projected along the  $4^\circ$  miscut direction ( $\langle 110 \rangle$  azimuth) taken by slightly tilted  $(002)$  (Fig. 81(a)) and  $(00\bar{2})$  (Fig. 81(b)) reflections [90].

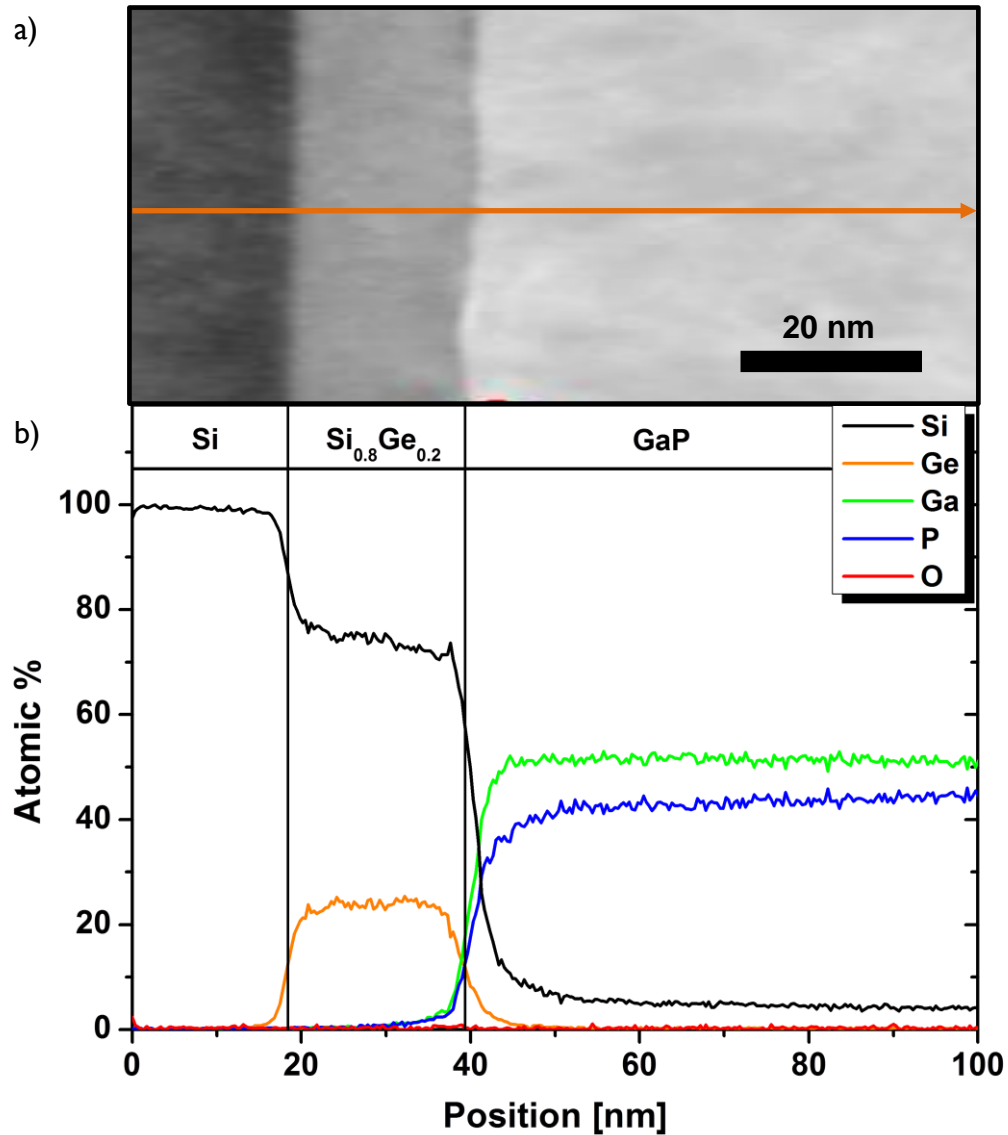


**Fig.81** Cross section DF HRTEM image pair of APDs at the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface of the 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure taken by slightly tilted  $(002)$  (a) and  $(00\bar{2})$  (b) reflection [90].

This dark field image pair confirms the presence of APDs in the GaP layer in form of triangular shaped structures located near the defective GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface by the characteristic contrast change. The APDs are limited by APBs, forming mainly  $\{111\}$  and  $\{211\}$  facets. According to theoretical calculations,  $\{211\}$  facets are energetically favored over  $\{111\}$  facets [193]. However, observed APDs disappear by self-annihilation of crossed APBs



after about 70 nm GaP thickness. It is mentioned that, besides APD detection, SF's are found inside and outside of APDs (indicate by arrows in Fig. 81(a)). It is noted that APD defect free growth of GaP after about 70 nm in our study on 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure corresponds well to similar results for GaP on Si [95, 128, 193]. Differences in APD defect nucleation might however exist and require further investigation [90].



**Fig.82** (a) Cross-section TEM image of deposited 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure. Orange line depicts EDX line-scan direction. (b) Result of EDX line-scan measurement.

Finally, a TEM-EDX line-scan measurement was performed in order to estimate possible impurity migration behavior in the deposited 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure during the material growth processes. Figure 82(a) shows the TEM image of

the heterostructure highlighting the applied EDX line-scan direction as orange line. The corresponding EDX data is illustrated in atomic-% as function of position in Fig. 82(b). The EDX spectra allow the following insights: Firstly, the sharp  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  interface indicate no migration of Ge atoms into  $\text{Si}(001)$  substrate as well as Si atoms into  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer. Otherwise, also a significant change in the atomic composition of  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer could be observed in the last case, but the Si concentration drops fast to the expected  $\approx 80\%$  in  $\text{Si}_{0.8}\text{Ge}_{0.2}$  though. Secondly, the  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{GaP}$  interface suffers in contrary from diffusion of Si into the GaP. This observed behavior of Si migration can result in an n-type doping of the GaP layer. Albeit Si can be an amphoteric dopant material, in GaP the n-type is dominant due to the much lower ionization energy for Si as donor on Ga lattice position (0.085 eV) with respect to Si as acceptor on P lattice position (0.210 eV) [164]. Since the GaP collector is under normal n-p-n HBT design already n-type doped, this fact seems not to be crucial. However, more important is that no significant migration of Ga- and P-atoms into the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer was detected by EDX, which would otherwise negatively influence the p-type  $\text{Si}_{0.8}\text{Ge}_{0.2}$  base layer in HBTs. In conclusion, the TEM-EDX study on as-deposited  $\text{GaP}/\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures point to stable interfaces. However, in particular electrical test studies need to corroborate these first material science studies.

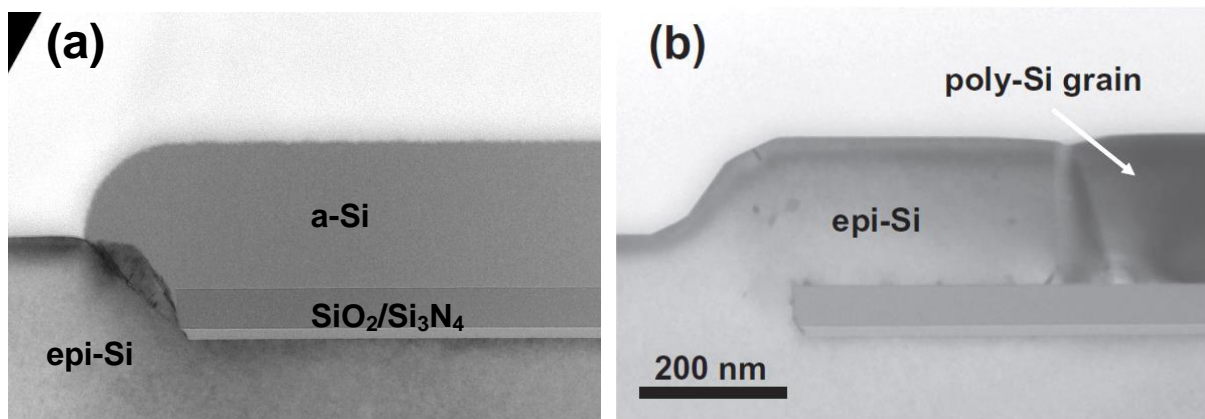
## 4. Summary & Outlook

The discovery of the first transistor device on 23<sup>rd</sup> December 1947 by Bardeen and Brattain in Bell Labs, started the age of microelectronics, which led to a unique success story up to today and constant miniaturization of Si microelectronics. State-of-the-art Si microelectronic devices accompany and simplify the greater part of our everyday life in form of small, fast and reliable multifunctional systems. However, it must be mentioned that the complexity of today's microelectronic circuitry is not only driven by CMOS scaling, but also by integration of high performance modules for various applications. An example is given by wireless and broadband communication systems, where mixed signal circuitries are built up by combining digital CMOS with analog SiGe:C HBTs known as SiGe:C BiCMOS technology. Today, SiGe:C BiCMOS technology can be demonstrated up to the 500 GHz range. However, Si as semiconductor is approaching more and more its physical limits, novel research approaches are needed to ensure further developments in SiGe:C HBT BiCMOS technology with the goal to push the maximum frequency further into the Terahertz regime. Based on this task, two novel material science approaches have been investigated in this Ph.D. thesis in form of material growth and defect studies:

**A.) SPE for emitter and base resistivity:** The SPE technique has been used to crystallize doped and undoped a-Si and a-SiGe, deposited using disilane gas source instead of silane, on SiO<sub>2</sub>- and Si<sub>3</sub>N<sub>4</sub>-masks in order to create a fully epi-Si emitter and base link region, respectively. This approach promises a possible reduction in emitter and base resistivity, resulting in an enhanced speed performance. The results of the first part of the Ph.D. thesis can be summarized as follows:

**AI.) SPE for emitter region:** SPE has been investigated as crystallization technique in the frame of a material growth study of As-doped a-Si deposited on SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> patterned Si (001) wafers by a RPCVD reactor using a H<sub>2</sub>-Si<sub>2</sub>H<sub>6</sub> gas system with AsH<sub>3</sub>. SPE was induced by in-situ postannealing directly after the deposition process inside the RPCVD reactor. By postannealing at 700–1000 °C, a-Si was crystallized and epi-Si/poly-Si was formed on the mask. Near the sidewall of the mask window, a-Si was crystallized epitaxially in lateral direction and forms an epi-Si domain. The grain size of crystallized poly-Si and the epi-Si domain near the sidewall becomes larger at higher postannealing temperatures. Observing the defect density of the epi-Si domain, consisting mainly of SFs, it is to mention

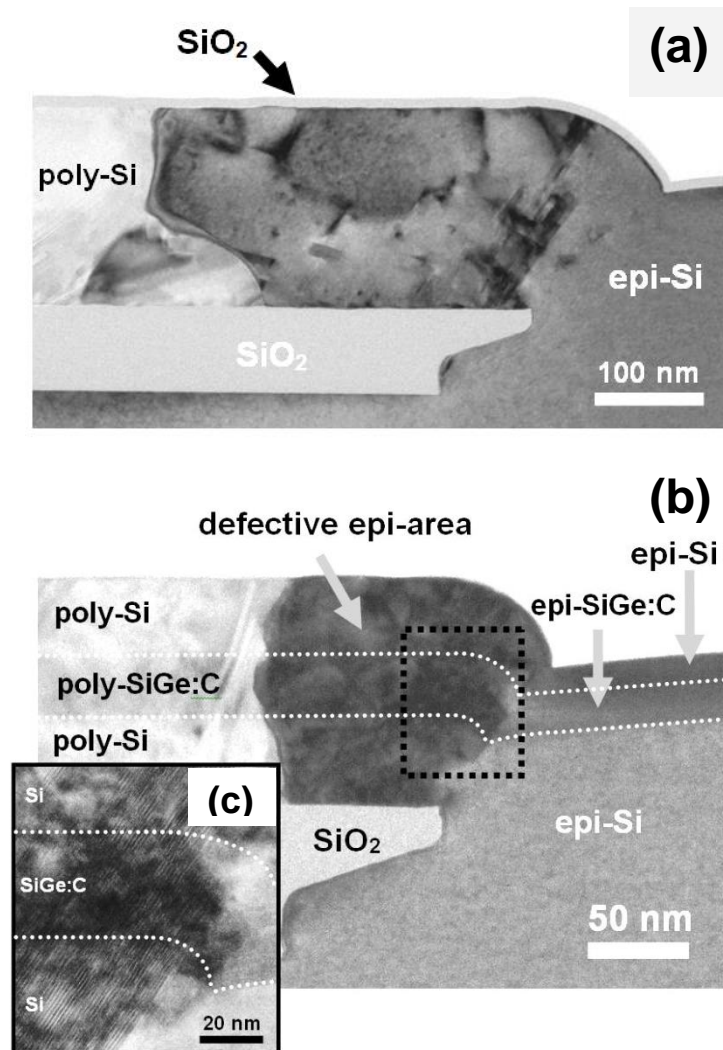
that the defect density was strongly reduced at higher postannealing temperature. The crystal orientation is the same as the Si (001) substrate and a facet formation has appeared at the sidewall surface. Otherwise, using postannealing temperatures of 575 °C, a direct poly-Si growth from a-Si seems to be suppressed and the epi-Si domain near the sidewall grew also laterally with increasing postannealing time. For both higher and lower postannealing temperature regions (700 – 1000 °C and 575 °C), the crystallization is inhibited as As concentration in the a-Si layer raises. L-SPE up to 500 nm on the mask has been demonstrated by a combination of postannealing at 575 °C and 1000 °C [119] (Fig. 83).



**Fig.83** (a) Cross-section TEM image of As-doped a-Si deposited on SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> patterned Si (001) wafers using Si<sub>2</sub>H<sub>6</sub> gas source at 550 °C. (b) Crystallized sidewall after two step postannealing procedure at 575 °C for 2 hours and at 1000°C for 60 sec, respectively. As concentration is  $2 \times 10^{20}/\text{cm}^3$  [119].

**A2.) SPE for base region:** SPE has been investigated as crystallization technique in the frame of a material growth study of undoped a-Si deposited by a RPCVD reactor on SiO<sub>2</sub> patterned Si(001) wafer using a H<sub>2</sub>-Si<sub>2</sub>H<sub>6</sub> gas mixture. SPE was induced by in-situ postannealing directly after the deposition process inside the RPCVD reactor. The L-SPE length of crystallized undoped Si on SiO<sub>2</sub>-mask and the crystallinity were studied by TEM/SEM characterization for various postannealing times, postannealing temperatures and a-Si thicknesses on SiO<sub>2</sub>-mask. Initially, the results showed an increase in L-SPE growth for longer postannealing times, higher postannealing temperatures and larger Si thicknesses on mask. However, TEM defect studies displayed a defective epitaxial state of SPE crystallized Si with a significant higher defect density on the SiO<sub>2</sub>-mask than inside the mask window. By using a SiO<sub>2</sub>-cap on samples with 180 nm Si thickness on the SiO<sub>2</sub>-mask followed by postannealing at 570 °C for 5 hours, an L-SPE length of epi-Si up to 450 nm could be achieved on the SiO<sub>2</sub>- mask (Fig. 84(a)). Finally, after investigating the influence of Ge in a-Si

on SPE, SPE was applied for model SiGe:C HBT base stack, resulting in a L-SPE length of defective epi-Si up to 140 nm on SiO<sub>2</sub>-mask (Fig. 84(b, c) [121]).



**Fig.84** (a) Cross section TEM of crystallized sidewall after postannealing at 570 °C for 5 hours with 10 nm SiO<sub>2</sub> capped samples. Si thickness on mask is 180 nm. Cross section TEM images (b) and high resolution TEM close-up image (c) of by SPE crystallized bipolar window sidewall after full HBT base process containing Si-buffer/SiGe:C base/Si-cap layer deposition. SPE steps were applied after Si-buffer deposition at 570 °C for 5 hours. [121].

**B.) III-V/SiGe hybrid device:** The ternary compound semiconductor In<sub>1-x</sub>Ga<sub>x</sub>P [x = 0 – 1] has been introduced as potential new collector material as part of an advanced III-V/SiGe hybrid HBT device concept. With InP having a three times higher saturation velocity than Si, and GaP having a two times bigger bandgap than Si, this approach offers the possibility to adjust speed and power performance of HBTs in a flexible way as a function of the In<sub>1-x</sub>Ga<sub>x</sub>P collector chemical composition x. The results of this second part of the

Ph.D. thesis deals with a heterostructure growth study of GaP on pseudomorphic 4° off-oriented  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  substrates, using a combination of RPCVD for SiGe and GSMBE for GaP deposition, in order to develop a wide bandgap GaP collector concept for future SiGe:C HBTs. The following main results were reported:

1. Theoretical model calculations were applied to evaluate the feasibility of the approach to prepare truly pseudomorphic GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures suitable for HBT applications. It is found that the calculated critical thickness of about 64 nm for GaP on pseudomorphic  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  might be too low for a HBT wide bandgap collector application. Consequently, nitrogen incorporation in GaP can be a viable way for increasing the critical GaP thickness.

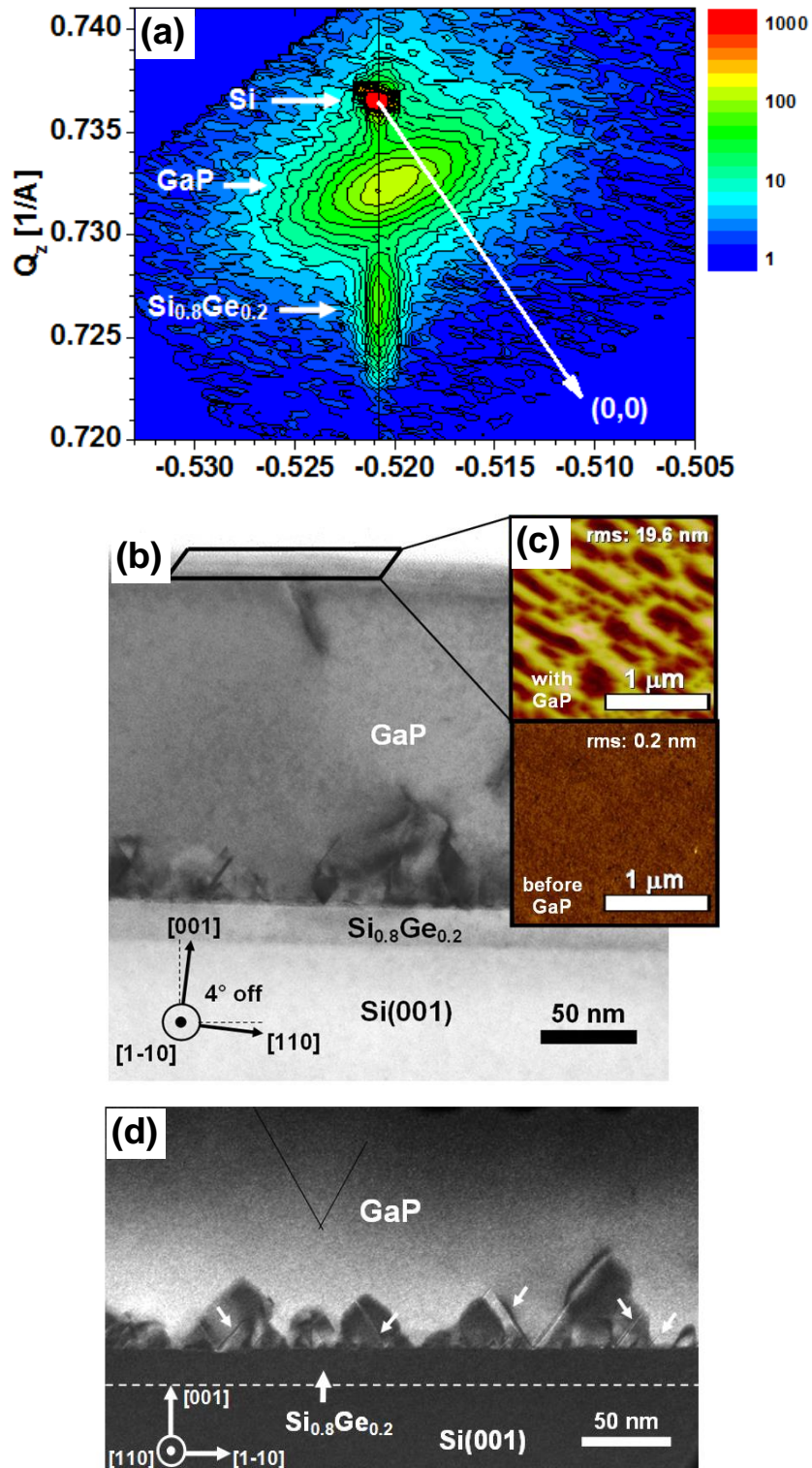
2. To determine the maximal thermal budget for GaP overgrowth on pseudomorphic 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$ , a detailed XRD analysis was performed. A maximal GaP growth temperature of 800 °C was identified, because plastic relaxation of pseudomorphic 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  starts beyond this process temperature.

3. XRD was used to characterize the epitaxial relationship and structure quality of the 170nm GaP/20nm  $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructure system. The epitaxial relationship of the monocrystalline heterostructure is given by  $\text{GaP}[001]; <110> || \text{Si}_{0.8}\text{Ge}_{0.2}[001]; <110> || \text{Si}[001]; <110>$ . However, we did not succeed to establish growth conditions for fully pseudomorphic growth of the heterostructure: Although the 20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$  base stays pseudomorphic underneath 170 nm GaP, the GaP layer grows partially relaxed (40%) (Fig. 85(a)).

4. XRD and TEM revealed that the partial relaxation is due to the presence of mainly SFs and MTs, and are primarily located at the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface region. This result in combination with high temperature XRD studies, which revealed no plastic relaxation within the applied thermal budget, point to the formation of so-called growth defects during the initial 3D island nucleation of the GaP film as the main origin of the partial relaxation process in the GaP thin film (Fig. 85(b)&(c)).

5. APD-free GaP growth is observed for layer thicknesses beyond 70 nm, in line with the literature for GaP on Si (Fig. 85(d)).

6. TEM-EDX measurements show no detrimental diffusion in the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}(001)$  heterostructures, which confirms the required presence of stable interfaces for HBT application.



**Fig.85** (a) RSM of asymmetric  $(\bar{2}24)$  reflections of Si, GaP, and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  measured for the 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001) sample. (b) Cross section TEM image (c) and AFM surface images (before and after GaP deposition) of 170 nm GaP on pseudomorphic  $4^\circ$  off-oriented  $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001). (d) Cross section dark field HRTEM image of APDs at the GaP/ $\text{Si}_{0.8}\text{Ge}_{0.2}$  interface of the 170 nm GaP/20 nm  $\text{Si}_{0.8}\text{Ge}_{0.2}$ /Si(001) heterostructure taken by slightly tilted (0 0 2) reflection  $[90]$ .

To evaluate the benefit of these two presented novel approaches in this Ph.D. thesis for SiGe:C HBT BiCMOS technology, this work only marks the beginning of a research and development process in order to reach full device integration. For each approach, additional efforts and dedicated studies have to be done in the future:

**A.) SPE for emitter and base resistivity:** The next step will be to use the insights of the here presented model emitter and base SPE studies to generate a process flow for full device application. Therefore, a standard SiGe:C HBT BiCMOS process has to be chosen and each area of application (emitter or base) has to be carefully varied and adjusted to apply the SPE technique. In both cases, the full epi-Si emitter and the full epi-Si/epi-SiGe base link region approach, resistivity measurements (of emitter  $R_E$  and external base  $R_{Be}$ ) has to be done and compared with resistivity data of the standard SiGe:C HBT BiCMOS process flow in order to evaluate possible improvements. At the same time, the other electrical parameters and parasitics has also to be monitored, because only improving the resistivity on the cost of other main features (e.g. doping profile, capacitances, etc.) will be not the desired solution for future SiGe:C HBTs development. These SPE studies on full processed wafers for standard SiGe:C HBT BiCMOS production are currently underway at IHP cleanroom facility.

**B.) III-V/SiGe hybrid device:** At first, future work will focus on improved 2D GaP layer growth conditions in order to prepare truly pseudomorphic GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructures with low defect densities. Pseudomorphism as well as low defect densities, especially at the CB junction, are essential to generate a working HBT device with low parasitics. For this purpose, (selective) GaP heteroepitaxy studies in local HBT Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) mesa structures are currently under way by GSMBE and MOCVD. After that, the next steps will be the creation of n-p-n doping profiles in the GaP/Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si(001) heterostructures and the identification of adequate electrical contacts in order to measure the I-V characteristic of this III-V/SiGe hybrid device.



## 5. Scientific visibility

### Publications in peer-reviewed journals

1. **O. Skibitzki**, A. Paszuk, F. Hatami, P. Zaumseil, Y. Yamamoto, M.A. Schubert, B. Tillack, W.T. Masselink, T. Hannappel, and T. Schroeder, *Lattice-engineered SiGe-buffer on Si(001) for GaP integration*, J. Appl. Phys. (to be submitted) (2013).
2. **O. Skibitzki**, F. Hatami, Y. Yamamoto, P. Zaumseil, A. Trampert, M.A. Schubert, B. Tillack, W.T. Masselink, and T. Schroeder, *GaP collector development for SiGe heterojunction bipolar transistor performance increase: A heterostructure growth study*, J. Appl. Phys. **111**, 0735515 (2012).
3. **O. Skibitzki**, Y. Yamamoto, M.A. Schubert, and B. Tillack, *Solid-phase epitaxy of undoped amorphous silicon by in-situ postannealing*, Thin Solid Films **520**, 3271 (2012)
4. **O. Skibitzki**, Y. Yamamoto, M.A. Schubert, G. Weidner, and B. Tillack, *Solid-phase epitaxy of amorphous silicon films by in situ postannealing using RPCVD*, Solid-State Electronics **60**, 13 (2011).

### Own patents

1. **O. Skibitzki** and T. Schroeder, *Siliziumbasierter Heterobipolartransistor mit einer Kollektorschicht aus einem III-V Halbleiter*, IHP.360.10, DE-Patentanmeldung am 18.02.2011, AZ: 10 2011 004 411.6.

### Own presentations at conferences and courses

1. **O. Skibitzki**, A. Paszuk, F. Hatami, P. Zaumseil, Y. Yamamoto, M.A. Schubert, B. Tillack, W.T. Masselink, T. Hannappel, and T. Schroeder, *GaP virtual substrates by lattice-engineered SiGe-buffer on Si(001)*, Oral presentation (accepted), E-MRS 2013 Fall Meeting, Warsaw, September 16 - 20, 2013, Poland.
2. **O. Skibitzki**, F. Hatami, Y. Yamamoto, P. Zaumseil, A. Trampert, M.A. Schubert, B. Tillack, W.T. Masselink, and T. Schroeder, *Heterostructure Growth Study for GaP Collector Material Integration in Future SiGe HBTs*, Poster presentation, Wilhelm and Else Heraeus Physics School "Microelectronics for Society - More than Moore Expands More Moore", Bad Honnef, June 10 - 16, 2012, Germany.

3. **O. Skibitzki**, F. Hatami, Y. Yamamoto, P. Zaumseil, A. Trampert, M.A. Schubert, B. Tillack, W.T. Masselink, and T. Schroeder, *Heterostructure Growth Study for GaP Collector Integration in SiGe HBT Technology*, Oral presentation, DPG Frühjahrstagung, Berlin, March 25 - 30, 2012, Germany.
4. **O. Skibitzki**, F. Hatami, Y. Yamamoto, P. Zaumseil, A. Trampert, M.A. Schubert, B. Tillack, W.T. Masselink, and T. Schroeder, *GaP Collector Development for SiGe HBT Performance Increase: A Heterostructure Growth Study*, Oral presentation, 8<sup>th</sup> Autumn School on X-Ray Scattering from Surfaces and Thin Layers, Smolenice, October 04 – 07, 2011, Slovakia.
5. **O. Skibitzki**, F. Hatami, Y. Yamamoto, P. Zaumseil, A. Trampert, M.A. Schubert, B. Tillack, W.T. Masselink, and T. Schroeder, *GaP Heterostructure Growth Study for Future SiGe HBT Performance Increase*, Oral presentation, 7th International Conference on Si Epitaxy and Heterostructures (ICSI-7), Leuven, August 28 – September 1, 2011, Belgium.
6. **O. Skibitzki**, Y. Yamamoto, M.A. Schubert, and B. Tillack, *Solid-Phase Epitaxy of Undoped Amorphous Silicon by in-situ Postannealing*, Poster presentation, 7th International Conference on Si Epitaxy and Heterostructures (ICSI-7), Leuven, August 28 – September 1, 2011, Belgium.
7. **O. Skibitzki**, Y. Yamamoto, M.A. Schubert, and B. Tillack, *In-Situ Solid-Phase Epitaxy of Amorphous Silicon Deposited by RPCVD*, Oral presentation, ASM User Meeting, Munich, October 23, 2010, Germany.
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## List of abbreviations

<b>2D</b>	Two-dimensional
<b>3D</b>	Three-dimensional
<b>A</b>	Area
<b>A<sub>C</sub></b>	Cross-sectional area of collector-base junction
<b>A<sub>E</sub></b>	Cross-sectional area of emitter-base junction
<b>a</b>	Lattice constant of overgrowth / Bulk lattice constant
<b>a<sub>0</sub></b>	Off-plane lattice constant
<b>a<sub>1</sub></b>	In-plane lattice constant
<b>AFM</b>	Atomic force microscopy
<b>Al</b>	Aluminium
<b>Al<sub>2</sub>O<sub>3</sub></b>	Sapphire
<b>AP</b>	Anti-phase
<b>APB</b>	Anti-phase boundary
<b>APD</b>	Anti-phase domain
<b>Ar</b>	Argon
<b>ART</b>	Aspect ratio trapping approach
<b>As</b>	Arsenic
<b>AsH<sub>3</sub></b>	Arsine
<b>a-Si</b>	Amorphous Silicon
<b>Au</b>	Gold
<b>B</b>	Boron
<b>b</b>	Lattice constant of substrate / Burger's vector
<b>Be</b>	Beryllium
<b>B<sub>2</sub>H<sub>6</sub></b>	Diborane
<b>BEOL</b>	Back-end-of-line
<b>BiCMOS</b>	Bipolar complementary metal oxide semiconductor
<b>Bi</b>	Bismuth
<b>BJT</b>	Bipolar-junction transistor
<b>Br</b>	Bromine
<b>BSE</b>	Backscattered electrons
<b>C</b>	Carbon
<b>c</b>	Speed of light

$C'_C$	Total collector capacitance
$C'_{DE}$	Emitter-base depletion capacitance
$C'_{DC}$	Collector-base depletion capacitance
$C'_{dn}$	Diffusion capacitance due to electrons in base
$C'_{dp}$	Diffusion capacitance due to holes in emitter
$C'_{in}$	Total input capacitance
$C'_{par}$	Parasitic capacitance
$C'_{sc}$	Space-charge capacitance in collector due to injected electrons
$C_{CB}$	Collector-base capacitance
$C_{OX}$	Insulator capacitance in inversion
<b>CB</b>	Collector-base
<b>CCD</b>	Charge-coupled device
<b>CH<sub>3</sub>OH</b>	Methanol
<b>CMOS</b>	Complementary metal oxide semiconductor
<b>Cs</b>	Caesium
<b>CTE</b>	Coefficients of thermal expansion
<b>Cu</b>	Copper
<b>CVD</b>	Chemical vapor deposition
<b>d</b>	Thickness
$D_A, D_B$	Double layer steps
$D_N$	Diffusion coefficient for electrons
$D_{pC}$	Diffusion coefficient for holes in the collector
$D_{pE}$	Diffusion coefficient for holes in the emitter
<b>DF</b>	Dark field
<b>DMS</b>	Diluted magnetic semiconductor
<b>E</b>	Electric field
$E_a$	Activation energy
$E_{bC}$	Build-in electric field in collector
$E_C$	Conduction band
$E_F$	Fermi level
$E_g$	Band gap
$E_{ph}$	Optical-phonon energy
$E_V$	Valence band
<b>EB</b>	Emitter-base

<b>EC</b>	Emitter-collector
<b>ECL</b>	Emitter-coupled logic
<b>EDX</b>	Energy dispersive x-ray spectroscopy
<b>epi-Si</b>	Monocrystalline Silicon
<b>f</b>	Natural lattice misfit
<b>f<sub>n</sub></b>	Atomic form factor
<b>F<sub>Nd</sub></b>	Function of doping concentration and oxide thickness
<b>f<sub>T</sub></b>	Transit cutoff frequency
<b>f<sub>max</sub></b>	Maximum frequency of oscillation
<b>FEOL</b>	Front-end-of-line
<b>FET</b>	Field-effect transistor
<b>FIB</b>	Focused ion beam
<b>FWHM</b>	Full width at half maximum
<b>G</b>	Lattice factor
<b>g<sub>m</sub></b>	Transconductance
<b>Ga</b>	Gallium
<b>GaP</b>	Gallium phosphide
<b>GBT</b>	Graphene base transistor
<b>Ge</b>	Germanium
<b>GeH<sub>4</sub></b>	Germane
<b>GND</b>	Ground
<b>GSMBE</b>	Gas source molecular beam epitaxy
<b>H</b>	Hydrogen
<b>h</b>	Integer number
<b>h<sub>crit</sub></b>	Critical layer thickness
<b>h<sub>FB</sub></b>	Common-base current gain
<b>h<sub>FE</sub></b>	Common-emitter current gain
<b>HBT</b>	Hetero-bipolar transistor
<b>HCl</b>	Hydrochloric acid
<b>HF</b>	Hydrofluoric acid
<b>HRTEM</b>	High resolution transmission electron microscopy
<b>I</b>	Current
<b>I<sub>0</sub></b>	Intensity of unpolarized incoming wave
<b>I<sub>B</sub></b>	Base current

$I_C$	Collector current
$I_{C0}$	Reverse current at collector-base junction
$I_{CB0}$	Collector saturation current
$I_D$	Transduced drain current
$I_E$	Emitter current
$I_e$	Intensity of radiating electrons
$I_{nC}$	Electron current which actually reach the collector
$I_{nE}$	Electron injection current from the emitter into the neutral base
$I_{pE}$	Hole injection current from base to the emitter
$I_{rB}$	Recombination current in neutral base
$I_{rE}$	Recombination current at emitter-base junction
$I_{ON}$	Switch-on current
$I_{OFF}$	Switch-off current
<b>IC</b>	Integrated circuits
<b>In</b>	Indium
<b>In<sub>1-x</sub>Ga<sub>x</sub>P</b>	Indium gallium phosphide
<b>InP</b>	Indium phosphide
<b>ITRS</b>	International Technology Roadmap for Semiconductors
$J_0$	Reverse current density at constant temperature
<b>JFET</b>	Junction field-effect transistor
<b>k</b>	Integer number
$k_B$	Boltzmann's constant
<b>K<sub>3</sub>[Fe(CN)<sub>6</sub>]</b>	Potassium ferricyanide
<b>L</b>	Channel length
<b>l</b>	Integer number
<b>LCAO</b>	Linear combination of atomic orbitals
<b>LDPF</b>	Local-density-functional pseudopotential formalism
<b>LED</b>	Light-emitting diodes
<b>L-SPE</b>	Lateral solid-phase epitaxy
<b>M</b>	Metal layer
<b>m</b>	Mass
$m_f$	Fitting factor
<b>MBE</b>	Molecular beam epitaxy
<b>MD</b>	Misfit dislocation

<b>MEMS</b>	Microelectromechanical systems
<b>Mg</b>	Magnesium
<b>ML</b>	Monolayer
<b>MIM-C</b>	Metal-insulator-metal capacitor
<b>Mn</b>	Manganese
<b>MOCVD</b>	Metal organic chemical vapor deposition
<b>MSA</b>	Model-solid approach
<b>MT</b>	Microtwin
<b>MOSFET</b>	Metal-oxide-semiconductor field-effect transistor
<b>N</b>	Nitrogen
<b>n</b>	Electron concentration / n-type semiconductor with donor impurity
<b>n<sup>+</sup></b>	Heavy electron doped material
<b>N<sub>C</sub></b>	Charge carrier density in collector
<b>n<sub>i</sub></b>	Intrinsic carrier concentration
<b>n<sub>p</sub></b>	Electron concentration in p-type semiconductor
<b>n<sub>p0</sub></b>	n <sub>p</sub> in thermal equilibrium
<b>N<sub>ion</sub></b>	Ionized impurity density
<b>n-Ge</b>	Electron doped/rich Germanium
<b>nMOS</b>	n-channel Metal-oxide-semiconductor
<b>O</b>	Oxygen
<b>P</b>	Phosphorus
<b>p</b>	Hole concentration / p-type semiconductor with acceptor impurity
<b>p<sub>d</sub></b>	Average distance between two misfit dislocation defects
<b>PF</b>	Pole figure
<b>p-Ge</b>	Hole doped/rich Germanium
<b>PH<sub>3</sub></b>	Phosphine
<b>φ<sub>m</sub></b>	Work function
<b>ψ<sub>bi</sub></b>	Build-in potential
<b>pMOS</b>	p-channel Metal-oxide-semiconductor
<b>p<sub>n0E</sub></b>	Hole concentration in n-type emitter in thermal equilibrium
<b>p<sub>n0C</sub></b>	Hole concentration in n-type collector in thermal equilibrium
<b>poly-Si</b>	Polycrystalline silicon
<b>Q</b>	n-p-n SiGe:C HBT
<b>q</b>	(Unit) Charge

<b><math>Q_B</math></b>	Injected excess charge in the base
<b>R</b>	Distance
<b><math>R_B</math></b>	Total base resistance
<b><math>R_{Bc}</math></b>	Base contact resistance
<b><math>R_{Be}</math></b>	External base link resistance
<b><math>R_C</math></b>	Total collector resistance
<b><math>R_E</math></b>	Total emitter resistance
<b><math>R_{Eb}</math></b>	Emitter bulk resistance
<b><math>R_{Ec}</math></b>	Emitter contact resistance
<b><math>R_m</math></b>	Translation vector of a unit cell
<b><math>r_n</math></b>	Vector corresponding to position of one atom inside unit cell
<b>RCA</b>	Radio Corporation of America
<b>RF</b>	Radio frequency
<b>RHEED</b>	Reflection high-energy electron diffraction
<b>RNS</b>	Random nucleation and growth
<b>RPCVD</b>	Reduced pressure chemical vapor deposition
<b>RSM</b>	Reciprocal space mapping
<b>RTA</b>	Rapid thermal annealing
<b><math>S_A, S_B</math></b>	Monolayer steps
<b>SA(E)D</b>	Selected area (electron) diffraction
<b>SAW</b>	Surface acoustic wave
<b>Sb</b>	Antimony
<b>SCP</b>	Self-consistent pseudopotential
<b>SDD</b>	Silicon Drift Detector
<b>SE</b>	Secondary electrons
<b>Se</b>	Selenium
<b>SEM</b>	Scanning electron microscopy
<b>SF</b>	Stacking faults
<b>Si</b>	Silicon
<b><math>SiCl_2H_2</math></b>	Dichlorosilane
<b>SiGe</b>	Silicon-Germanium
<b><math>SiH_4</math></b>	Silane
<b><math>Si_2H_6</math></b>	Disilane
<b><math>SiH_3CH_3</math></b>	Methylsilane



<b>SIMS</b>	Secondary ion mass spectroscopy
<b>Si<sub>3</sub>N<sub>4</sub></b>	Silicon nitride
<b>SiO<sub>2</sub></b>	Silicon dioxide
<b>SiP</b>	System-in-Package
<b>Sn</b>	Tin
<b>SoC</b>	System-on-Chip
<b>SOI</b>	Silicon-on-insulator
<b>SPE</b>	Solid-phase epitaxy
<b>T</b>	Temperature
<b>T<sub>Ga</sub></b>	Ga crucible temperature
<b>T<sub>sub</sub></b>	Substrate temperature
<b>TC</b>	Thermal conductivity
<b>Te</b>	Tellurium
<b>TEM</b>	Transmission electron microscopy
<b>TFT</b>	Thin-film transistor
<b>ToF-SIMS</b>	Time-of-Flight secondary ion mass spectroscopy
<b>U<sub>e</sub></b>	Acceleration voltage
<b>UHV</b>	Ultra-high vacuum
<b>V</b>	Voltage
<b>V<sub>A</sub></b>	Early voltage
<b>V<sub>BE</sub></b>	Base-emitter voltage
<b>V<sub>BCB0</sub></b>	Collector-base open-emitter breakdown voltage
<b>V<sub>BCE0</sub></b>	Collector-emitter open-base breakdown voltage
<b>V<sub>BD</sub></b>	Breakdown voltage
<b>V<sub>CB</sub></b>	Collector-base voltage
<b>V<sub>CE</sub></b>	Collector-emitter voltage
<b>V<sub>CE, sat</sub></b>	Collector-emitter saturation voltage
<b>V<sub>D</sub></b>	Drain voltage
<b>V<sub>DD</sub></b>	Supply voltage
<b>V<sub>G</sub></b>	Gate voltage
<b>V<sub>in</sub></b>	Input voltage/signal
<b>V<sub>out</sub></b>	Output voltage/signal
<b>V<sub>R</sub></b>	Reverse voltage
<b>V<sub>T</sub></b>	Threshold voltage

<b>V<sub>U</sub></b>	Turnover voltage
<b>V-SPE</b>	Vertical solid-phase epitaxy
<b>W</b>	Neutral base width
<b>W<sub>B</sub></b>	Base width
<b>W<sub>C</sub></b>	Collector width
<b>W<sub>DC</sub></b>	Depletion width of collector side
<b>W<sub>E</sub></b>	Emitter width
<b>W<sub>Z</sub></b>	Channel width
<b>X<sub>C</sub></b>	Collector depletion width
<b>XRD</b>	X-ray diffraction
<b>Z</b>	Impedance

$\alpha_0$	Common-base current gain
$\alpha_T$	Base transport factor
$\beta_0$	Common-emitter current gain
$\gamma$	Emitter injection efficiency
$\epsilon_0$	Vacuum permittivity
$\epsilon_r$	Relative permittivity of a material
$\epsilon_s$	Permittivity of the semiconductor
$\eta$	Design parameter
$\theta$	Design parameter
$\lambda$	Wavelength
$\lambda_m$	Mean free path
$\mu$	Charge carrier mobility
$\mu_{ion}$	Charge carrier mobility taking ionized impurities into account
$\mu_{ph}$	Charge carrier mobility taking acoustic phonon interactions into account
$\mu_n$	Electron charge carrier mobility
$\mu_n^C$	Electron charge carrier mobility of collector material
$\mu_n^{CB}$	Electron charge carrier mobility in collector-base junction
$v$	Velocity (of SPE)
$v_D$	Drift velocity
$v_{sat}$	Saturation velocity

$\nu_x$	Poisson ratio
$\tau$	Transit time
$\tau_B$	Base transit time
$\tau_C$	Collector transit time
$\tau_{CB}$	Collector-base transit time
$\tau_E$	Emitter transit time
$\chi$	Electron affinity

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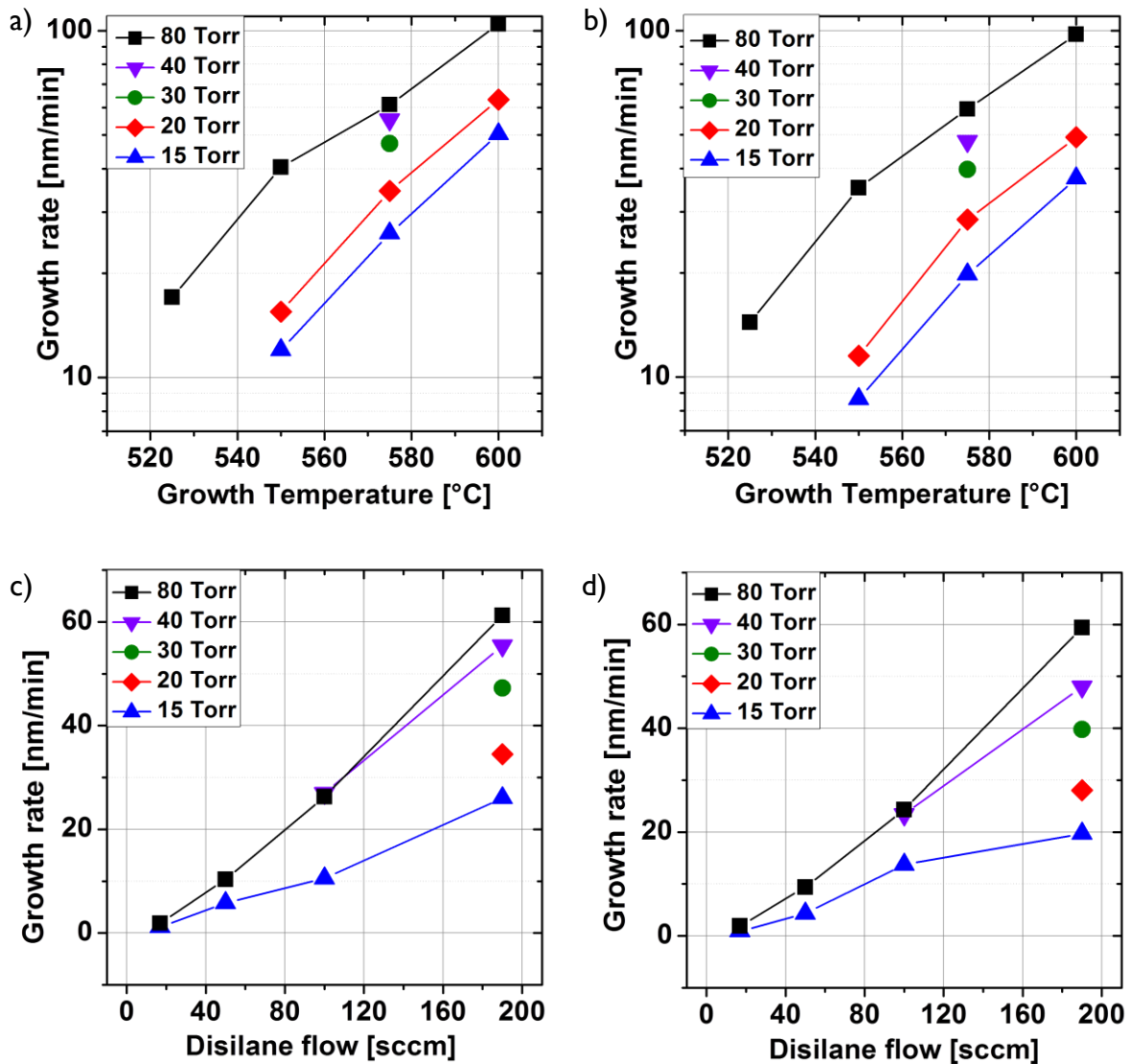
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## Appendix:

### Disilane growth parameters



**Fig.86** Growth temperature vs. growth rate for varies total pressures for a-Si (a) and epi-Si (b) growth. Disilane flow is 190 sccm. Disilane flow vs. growth rate for varies total pressures for a-Si (c) and epi-Si (d) growth. Growth temperature is 575 °C.