High-Speed Data Capturing Components for Super Resolution Maximum Length Binary Sequence UWB Radar

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by

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Abstract

Within framework of UKoLoS project the new Super Resolution Maximum Length Binary Sequence UWB Radar (M-sequence radar) was developed.

The radar consists of an M-sequence generator, transmitter front-end, receiver front-end, data capturing device and data processing blocks, whose design responsibilities were carried out by four institutions. In this thesis the design and measurements of the data capturing device components is described.

Logically the data capturing device can be divided into three parts; a capturing part, realized with the high-speed analog-to-digital converter, a predictor, realized with the high-speed digital-to-analog converter and a subtraction amplifier, which in this particular work is integrated into the receiver front-end.

The main challenge of the work is to implement the A/D converter, which works at full speed of the radar. Despite the radar architecture allows capturing data with undersampling, it leads to waste of transmitted energy. Therefore the ADC has to capture reflected signal with the full system clock rate of 10 GHz and should have a full Nyquist 5 GHz effective resolution bandwidth.

Implementation of the conventional 4-bit full flash ADC with specified bandwidth is not possible in the IHP SiGe BiCMOS technology because some critical blocks, namely the reference network, can not achieve 5 GHz effective resolution bandwidth. To overcome this problem a new configuration of the differential reference network is proposed. The new reference network has a segmented, free configurable

architecture. As extreme case it can be realized as a full parallel network and in such configuration the maximal bandwidth can be achieved. The proposed network was implemented in the A/D converter and measured. The bandwidth of the ADC with new network is several times higher than the bandwidth of the conventional ADC,while keeping power dissipation the same. Further the proposed network has possibility to equalize the bandwidth in each output node and in that way optimize overall power dissipation. The other advantage is the possibility of electronic calibration of separate voltage shift in the network.

The second component of the data capturing device is the D/A converter, which is required to have the accuracy which corresponds to full accuracy of the data capturing device, better than 0.2% in our case. Measurements showed that error due to mismatch of the components was 10 times higher than required. To meet the accuracy specification an external off-line calibration of the DAC was implemented. Using calibration the predictor errors less than 0.15% were achieved.

Schnelle Komponenten des Datenerfassungsblocks für ein Super Resolution Maximum Length Binary Sequence UWB Radar-System

von

Yevgen Borokhovych

Abstrakt

Im Rahmen des UKoLoS Projektes ist ein neues "Super Resolution Maximum Length Binary Sequence UWB Radar"-System (M-sequence radar) enwickelt worden.

Das System besteht aus einen M-sequence-Generator, einer Sende- und einer Empfangsstruktur, einem Datenerfassungs- und einem Datenverarbeitungsblock. Die einzelnen Komponenten sind von vier verschiedenen Projektpartnern entwickelt worden. In dieser Arbeit wird der Entwicklungsprozess des Datenerfassungsblocks sowie die zugehörigen Messergebnisse vorgestellt.

Der logische Aufbau des Datenerfassungsblocks lässt sich in zwei Teile gliedern. Der erste Teil dient der Datenerfassung und ist als schneller Analog-Digital-Wandler ausgeführt. Der zweite Teil haben die Funktion des Prädiktors. Dieser besteht aus einem schnellen Digital-Analog-Wandler und einer subtrahierenden Verstärkungseinheit.

Der Schwerpunkt dieser Arbeit liegt in der Implementierung eines Analog-Digital-Wandlers, der bei voller Taktfrequenz des Radar-Systems von 10 GHz arbeitet. Obwohl die Architektur des Radar-Systems eine Datenerfassung bei Unterabtastung erlaubt, führt dies zum partiellen Verlust der gesendeten Energie. Daher soll der Analog-Digital-Wandler der Datenerfassungseinheit bei einer Abtastrate arbeiten, die der Taktfrequenz des Radar-Systems entspricht.

Die übliche Implementierung des Analog-Digital-Wandlers als 4-bit full flash ist technologiebedingt nicht realisierbar, da die spezifizierte Bandbreite von 5GHz für das

Referenznetzwerk in der eingesetzten 0.25-µm SiGe BiCMOS Technologie nicht erreicht werden kann. Als Lösungsansatz wird eine neue Konfiguration für das differentielle Referenznetzwerk vorgeschlagen. Dieses Netzwerk weist eine segmentierte Architektur auf. Im Grenzfall kann es als voll paralleles Netzwerk implementiert werden. Die vorgeschlagene Topologie des Netzwerks wurde in dem Analog-Digital-Wandler des Datenerfassungsblocks angewendet. Die sich ergebende Bandbreite des so implementierten Analog-Digital Wandlers ist bei gleichem Leistungsverbrauch höher als die Bandbreite eines Standard-Wandlers,. Das Schaltungsprinzip des eingesetzten Referenznetzwerks ermöglicht eine Angleichung der Bandbreite einzelner Segmente und somit die Optimierung des Leistungsverbrauchs. Ein weiterer Vorteil ist die Möglichkeit den Spannungsabfall für jedes Segment separat elektronisch Kalibrieren zu können.

Der Digital-Analog-Wandler, der als Prädiktor zum Einsatz kommt, soll eine Genauigkeit haben, die der des gesamten Datenerfassungsblocks entspricht. In dem hier vorgestellten System bedeutet dies eine Abweichung von weniger als 0.2%.

Die Messungen haben gezeigt, dass der Fehler um einen Faktor 10 höher ist als in den Spezifikationen gefordert wird. Um den Anforderungen gerecht zu werden, wurde eine externe Kalibrierung implementiert. Hierdurch konnte der Fehler auf 0.15% reduziert werden.

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Introduction

Due to the good penetration to most substances ultra-wideband radars are well suited to detect or image hidden objects. They can be used in different fields such as: medicine, non-destructive material testing etc.

In order to approach the physical limits of ultra-wideband detection and imaging, super resolution techniques have to be applied for processing the captured data. Super resolution techniques are usually based on signal or system models that allow extrapolation up to a certain degree of the behaviour of the test objects which is beyond the actual measurements [1].

These techniques are very sensitive to any kind of noise. In case of data gathering in UWB radar, random perturbations occur mainly due to an additive noise, which corrupts the magnitude of the signal and due to jitter, which affects the instance of signal capturing.

Imaging requires data collection from different locations in space. If the targets behave stationary, the data may be captured sequentially by relocating the radars (synthetic aperture principle). If this is not the case as e.g. for many medical applications, all data must be gathered in parallel which requires a radar array of sufficient size. The operation of UWB-arrays is a challenging task since exact timing, high measurement speed and robustness against mutual interference are very important.

In this thesis, the maximum length binary sequence radar (M-Sequence radar) concept which meets these requirements will be introduced and design of data capturing device sub-components will be described.

Organization of Thesis

The first part of Chapter 1 will give brief general overview of the UWB radars, their advantages and disadvantages over conventional radars. Emphasis is put on pulse

compression methods. The second part of the chapter will describe a new maximum length binary sequence (M-sequence) UWB radar concept for super resolution imaging. Some system considerations and component specifications will be given in this part.

The second, third and fourth chapters deal with implementation of the data capturing components of the M-sequence radar.

The second chapter focuses on the design of the high-speed track-and-hold amplifier. The chapter will give overview of the modern high-speed architectures and presents the design of two different variants of the THA. Both designs are targeting high-speed applications. The first design was aimed to operate with low power dissipation; in the second design the accuracy and speed were prioritized at costs of power.

The third chapter deals with A/D converter design. Several architectures were investigated and the full flash architecture, which is the fastest, is selected for implementation. A new reference network for overcoming technological limitation and achieving better speed characteristic while keeping power dissipation the same is described in detail. The theoretical considerations were proven by comparison of conventional ADC and proposed ADC with the new reference network; both were designed in the same technology and partly had the same building blocks.

In the fourth chapter the predictor, based on a high-speed D/A converter is described. The speed of low GHz range is not very challenging for D/A converter, but high accuracy is. The design of the DAC together with external off-line calibration is described. The calibration is designed in a way suitable to be easily implemented on-chip.

The last, fifth chapter concludes the thesis. It summarizes primary achievements and gives brief overview of the future work.

Chapter 1. Introduction of New UWB Radar Concept

1.1 Advantages of UWB Radar

Historically, most radar systems use narrowband signal frequencies modulating a sinusoidal carrier signal. Narrowband signals limit the information capability of radio systems, because the amount of the information transmitted in a unit of time is proportional to the bandwidth. Increasing the system's information capacity requires expanding its bandwidth.

As the pulse volume of the signal gets smaller, the informational content of the UWB radar is increased; e.g. when the length of a pulse changes from 1 μs to 1 ns, the depth of the pulse volume decreases from 300 m to 30 cm.

The UWB radar's reduced pulse length has following advantages:

- Improved accuracy of target detection.
- Better distinguished target, because the received signal carries the information not only about the target as a whole but also about its separate parts.
- Reduced effects of passive interference from rain, mist, aerosols, metalized strips, etc., on the radar; because the scattering cross section of interference source within a small pulse volume is reduced relative to the target scattering cross section.
- Improved stability during observing targets at low elevation angles. This is because the main signals, and any ground return signals, arrive at the antenna at different times, which enables their selection.

- A narrow antenna pattern by changing the radiated signal characteristics.
- Improved immunity to external narrowband electromagnetic radiation effects and noise.

1.2 Types of UWB Radars

There are two principal types of UWB receivers: short-duration impulse radars and long-duration pulse-compression radars.

Receiving short-duration UWB signals and preserving the waveform is a major problem for impulse radar design, especially when the reflected signal must be analyzed to measure target characteristics. The speed of analog-to-digital converter (ADC) limits the signal bandwidth for single-pass signal digitization. Insufficient sample points can degrade system performance and introduce system errors. One solution is to divide, or channel the wideband signal in either frequency or time and then perform signal digitization with many ADCs.

Long-range target detection requires more energy than impulse radar systems can provide. One practical approach is to use a wide-bandwidth waveform and pulse compression coding methods. Pulse compression can provide the fine range resolution of impulse signals with the high signal energy of conventional narrowband radars. Because range resolution depends solely on the bandwidth, encoding can increase the signal bandwidth to give wideband signal resolution the long-duration, low-power, and high-energy signals needed for long-range target detection [2].

Pulse compression techniques improve the signal-to-noise ratio (SNR) in radar receivers [3]. Conventional radar with an unmodulated pulse signal has a bandwidth of $1/\tau$, where τ is the signal duration. It is possible to improve the SNR and signal detection by using spread spectrum technique to increase the bandwidth beyond $1/\tau$. Radar detection requires that the return signal exceed the receiver noise level, which

includes the receiver noise due to bandwidth, radar clutter returns and interference from other radars, jammers, transmitters.

There are some additional advantages in using pulse-compression signals. Increasing the signal bandwidth by coding provides a unique return signal, which lets the receiver reject other signals. Signal encoding permits several different radars to use the same spectrum without mutual interference. The correlation detection process turns long-duration low-power signal energy into a shorter higher-power pulse, and it suppresses random noise and unwanted signals. The resulting correlator output has a higher signal-to-noise ratio than it would have with a long-duration narrowband received signal. The integrating process in correlation reduces noise levels because of the low coincidence between the reference signals, random noise, and interference. However, some minimum received signal power must be present to provide a correlated output spike that exceeds the noise floor and receiver detection threshold. When the transmitted signal is reflected by random clutter, the overlapping signals will appear as noise, which will not be correlated or produce a detectable output.

1.3 Overview of Pulse Compression Methods

1.3.1 Linear frequency modulated chirp

The linear frequency modulated (linear FM) chirp depicted in Fig. 1.1a-c, is the simplest form of pulse compression signals. The matched filter output and sidelobe structure of the linear FM chirp are shown in Fig. 1.1d. The linear FM chirp is a widely used pulse compression signal, because it is easy to generate, and insensitive to Doppler shifts. Also, there are mature and proven methodologies to generate the signal.

But, linear FM chirp signals have also disadvantages: such as, excessive range-Doppler cross coupling results when the Doppler shifted signal is correlated, and hence shows a different time of arrival. Overcoming the range Doppler error requires knowing, or determining, the range, or Doppler, by other means. Linear pulse

compression also gives high range (time) sidelobes. This requires setting a high threshold level. Smaller targets may get lost in the time sidelobes [3].

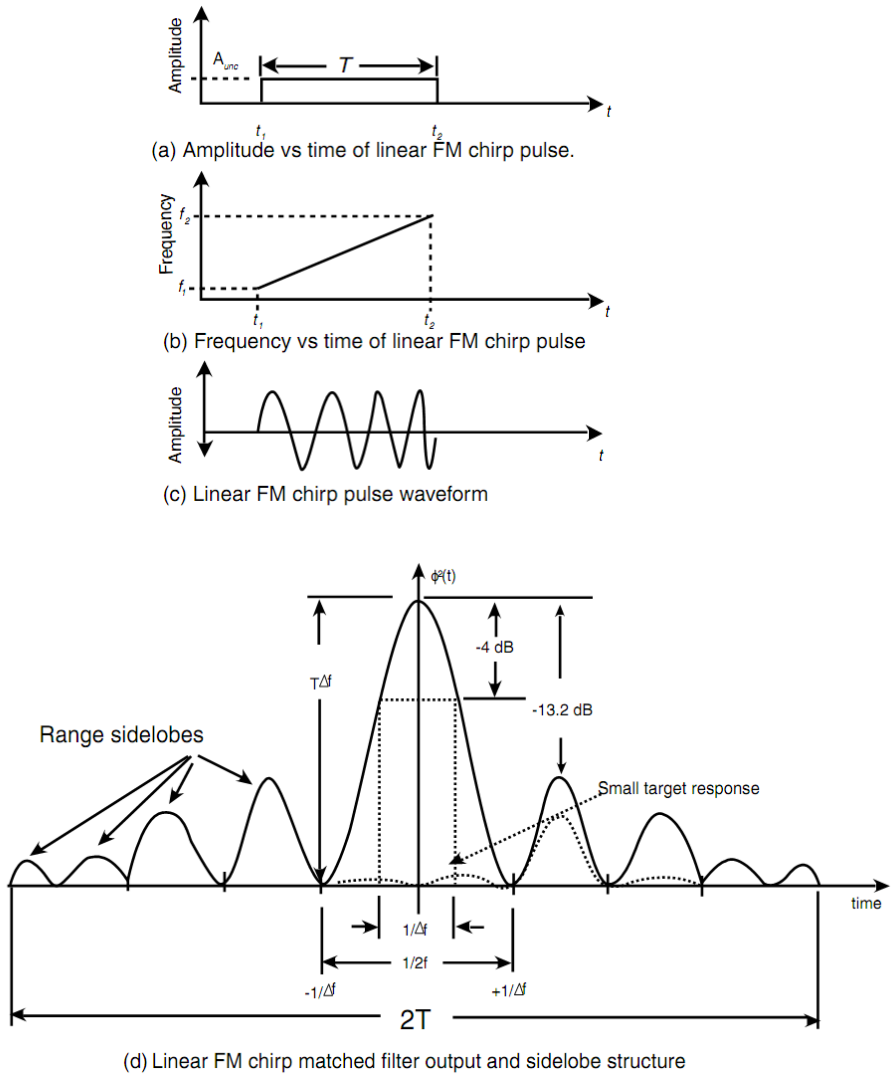


Fig. 1.1 Linear chirp.

Nonlinear chirp is a way to suppress time sidelobes. Nonlinear FM chirp signal has several advantages. It does not need time or frequency weighting for sidelobe suppression, because the FM modulation of the waveform provides the desired amplitude spectrum. It provides matched filter reception and low sidelobes that are compatible in design and it eliminates signal-to-noise losses associated with weighting.

However, nonlinear FM chirp signal also has disadvantages. It requires a more complex system, and there has been limited development in nonlinear-FM generator devices era. It requires a separate FM modulation design for each amplitude spectrum to achieve the required sidelobe level [3].

1.3.2 Barker codes

Barker codes are binary phase codes that have equal time sidelobes, whose power levels are equal to $PSL = 20 \cdot \lg(1/N)$, where N is the code length, and the maximum output is normalized to 1 [4]. The Barker code's advantages are minimum possible sidelobe energy which is uniformly distributed. But its 13-bit maximum size [5] limits the SNR improvement in radar applications.

1.3.3 Pseudo-random codes

Generating pseudorandom sequences (PN codes) is another approach to signal coding for pulse compression with lower sidelobes. PN codes are easy to generate, they have good sidelobe properties, and they are easily changed algorithmically. Maximal-length PN codes (maximal-length sequences, or simply *M*-sequences) are the most useful.

There are some considerations about PN-codes, some of which are mentioned below:

- For a large $N = 2^n - 1$, the peak sidelobe is approximately $PSL \approx \sqrt{1/N}$ in voltage when the signal is normalized to 1 [3]. The values depend on the particular sequence.
- For a continuous, periodic flow of PN codes through a matched filter, the output is a periodic peak response of N (in voltage) and a flat range sidelobe response of -1.
- PN codes are appropriate for pulsed radar applications in which a few closely spaced targets are expected in the field of view.

- PN codes use either a fully tapped delay line or bank of shift registers for each code bit to compress the signal at all ranges. Therefore, pseudorandom M-sequences are more popular in communication systems and continuous wave radar applications than in pulsed radar applications.

1.4 Advanced Architecture of UWB Radar

1.4.1 M-sequence technique

The M-sequence technique is closely related to the impulse technique and combines its advantages, such as simple implementation, high measurement speed, with advantages of the sine wave approach, such as high stability, low crest factor signals [6]. It is applicable to periodic signals having a large instantaneous bandwidth, where the data are captured in under-sampled condition in order to reduce data throughput. However, the two important issues, which are related to the type of stimulus signal and the method to control the sampling instant, are decisive differences compared to the impulse technique.

Fig. 1.2 illustrates the fundamental approach of the M-Sequence UWB System [7]. A fast digital shift-register with an appropriate feedback provides an M-Sequence with a bandwidth up to several gigahertz range. In contrast to the classical impulse technique, the M-Sequence distributes its energy over the complete measurement time. Thus, the signal amplitude could be comparatively low even if a large amount of power is required in order to achieve a certain SNR. As in the pulse method the wideband measurement signal is captured in under-sampling condition and the sampling event is controlled by a simple binary divider.

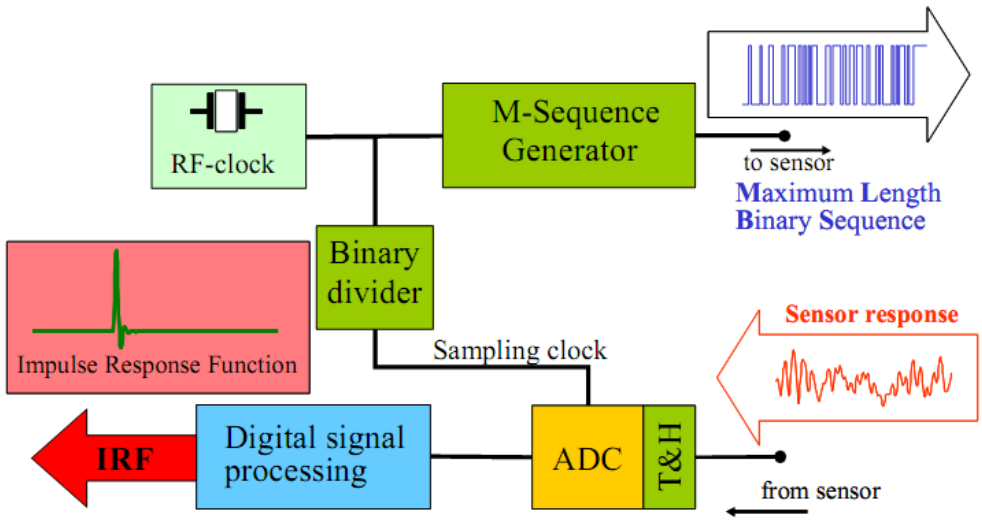


Fig. 1.2 Basic structure of M-Sequence UWB system.

M-Sequence technique is very well suited for operating with different capturing rates without changing the system. Only ratio between frequency of M-Sequence generator and frequency of data capturing device should be adopted. Higher ratio leads to waste of the transmitted energy and less sensitive system.

Basically the M-Sequence sensor captures one data point at each chip of the sequence. Since the M-sequence is periodic the capturing of different data points could be done at different periods.

Fig. 1.3 illustrates several periods of transmitted and received signals with captured data points. The data points, marked with red dots, with the different numbers could be captured over different periods without losing information.

From these data points an impulse response function (IRF) could be calculated. Resorting captured data from Fig. 1.3 in the way as shown in Fig. 1.4, the amplitude variation of received data could be observed on horizontal line. Assuming slow variation of the test scenario from period to period, the measured amplitude varies also slowly and mainly due to the noise. Therefore it is possible to predict the value of the next measured point. After subtracting predicted value from received value, only the prediction error should be captured by ADC and processed.

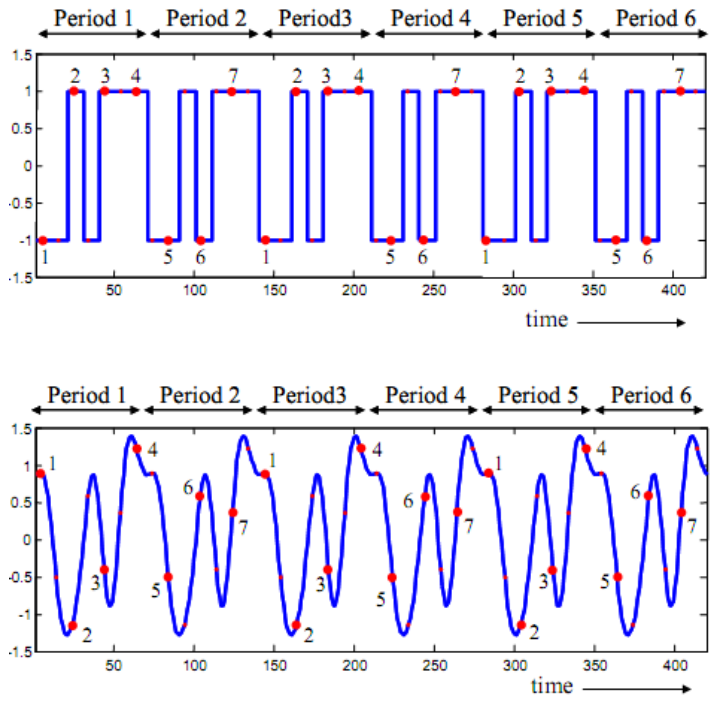


Fig. 1.3 Sub-sampling approach of an UWB M-Sequence sensor.

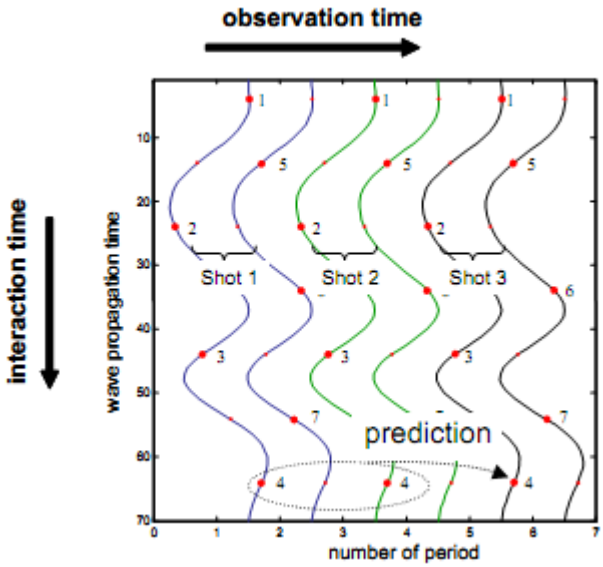


Fig. 1.4 Wiggel-plot with resorted measurement data.

1.4.2 M-Sequence UWB radar with prediction

The localization of the objects with *cm*-precision requires wide bandwidth and high sensitivity. For instance, the required bandwidth for imaging of human chest is about 10 GHz. Because of high loss in the human tissue, the sensitivity should be also very high. The measurements are made with an array of small antennas. The cross-talk between components tends to saturate receiver and also decrease the sensitivity.

A key technique to improve the sensitivity of an UWB system, which works at undersampled rate, is to increase the data capturing rate up to full speed of the system. Since about 80% of the signal energy is located in the first Nyquist zone [6], the undersampled capturing of the data results in a huge energy loss, and hence an inefficient receiver. This situation is even more severe as the transmit power of UWB devices is limited. It is possible to gather data with an enormous speed of tens of GS/s. However it is not possible to handle these data continuously and the effort of operating such a system (in terms of costs and power dissipation) is not acceptable.

The solution suited for sensor purposes is an M-Sequence approach in conjunction with a high-speed feedback loop in the receiver as depicted in Fig. 1.5 [8].

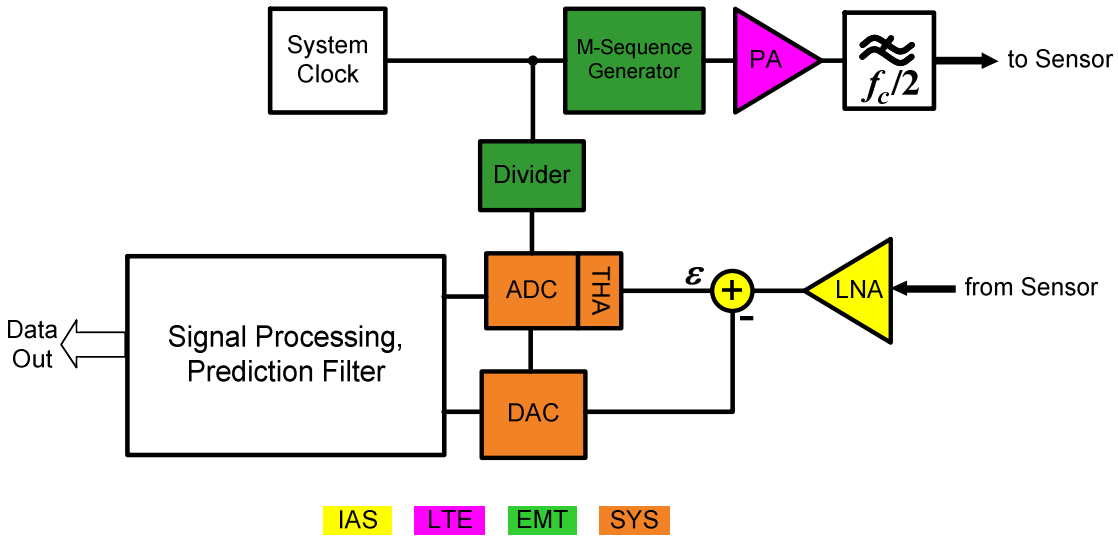


Fig. 1.5 Structure of an M-sequence feedback approach. Different colors are indicating working areas of the different partners.

The idea is to use a sub-ranging capturing device, a DAC for predicting the target value and an ADC for capturing the difference between received and predicted values. It is much more efficient in terms of power and hardware because the ADC with lower resolution can be used. The resolution of this sub-ranging device is $N_{ADC} + N_{DAC}$, where N_{ADC} is the resolution of A/D converter, and N_{DAC} is the resolution of D/A converter. The high-speed processing will finally lead to a high-dynamic measurement function (e.g. impulse response function) at a reasonable repetition rate which can be handled by usual processing systems (e.g. PCs or FPGA).

To summarize the benefits of the feedback loop, it can be said that it serves:

- To decrease the resolution of the ADC.
- To increase the resolution of the data capturing device.
- To increase the data capturing rate from undersampled to Nyquist.
- To increase the maximum receive voltage.
- To reduce the effective data throughput at the receiver output.
- To subtract the narrow band interference from the captured signal.

But it will also introduce additional challenges to designing appropriate RF-sub-circuits, fast digital capturing and data processing.

1.4.3 Derivation of components specifications from system specifications

The key features that describe the performance of the radar are: spatial resolution in range δ_r, observation range R (unambiguity range), and its sensitivity to detect weak reflecting objects.

The spatial resolution is inversely proportional to the bandwidth and equal to

$$\delta_r = \frac{c}{2 \cdot BW} \tag{1.1}$$

where BW is the bandwidth and c is the speed of the light.

Observation range (unambiguous range) is given by:

$$R = \frac{1}{2} c \cdot T \tag{1.2}$$

where T is a time window.

Sensitivity or detection limit describes the capability to find small scattering amplitudes in the impulse-response function (IRF) that are caused either from small scatters with poor dielectric contrast or by propagation loss. The signal could be detected if it excesses the random noise. The ratio of maximum detectable signal (A_{max}) to effective value of random noise (x_{eff}) is the signal to noise ratio (L_n) [9]:

$$L_n = 20 \cdot \lg\left(\frac{A_{\max}}{x_{eff}}\right) \tag{1.3}$$

A_{max} corresponds to the attenuation of the strongest transmission path, e.g. antenna breakthrough or surface reflection. The effective value of the noise could be reduced by averaging, deconvolution or error correction.

SNR of the M-Sequence sensor could be also expressed through length of the M-sequence and the resolution of the capturing device [9]:

$$L_n = 6 \cdot ENOB_{ADC+DAC} + 3 \cdot n + 10 \cdot \lg\left(p_{avg}\right) \tag{1.4}$$

where $ENOB_{ADC+DAC}$ is the effective resolution of the capturing system, n is the M-Sequence length, p_{avg} is the averaging factor.

Analyzing weight coefficients in the equation (1.4) makes it apparent that the resolution of the capturing device has the biggest influence on total SNR. Increasing the length of M-Sequence is also increasing SNR, but it also leads to increase the amount of data which should be processed.

As was mentioned before the system is aimed to work with *cm*-precision. From formula (1.1) it is easy to calculate that the bandwidth should be in the GHz range, more specifically, 5 GHz to have 3 cm resolution. Practical length of the M-sequence is 9-10 bits.

Targeting 80 dB SNR of the whole system, the number of bits of the capturing device could be calculated by equation (1.4). Taking average number equal to 1, the resolution of the capturing device $N_{ADC+DAC}$ should be 9 bits.

The capturing device of the system described in Fig. 1.5 consists of A/D and D/A converters. As is shown above, the total resolution is the sum of the resolutions of both converters.

To calculate separate resolutions of the both converters the conversion efficiency should be compared. The conversion efficiency is the energy required to make one conversion; the lower the energy, the more efficient the converter is. Energy per conversion step is a common Figure of Merit (FoM) for A/D and D/A converters and usually calculated by formula:

$$FoM = \frac{P_{diss}}{2 \cdot 2^{ENOB} \cdot BW} \tag{1.5}$$

The ratio between FoM_{ADC} and FoM_{DAC} depends on given technology and implementation of each converter. For our case, the ratio of 4 is taken (1.6):

$$\frac{FoM_{ADC}}{FoM_{DAC}} = 4 \tag{1.6}$$

Our goal is to minimize the power dissipation without losing the accuracy. To find the proper ratio between resolution of the ADC and resolution of the DAC, the equations (1.5) and (1.6) are combined and rewritten as:

$$P_{ADC+DAC} = 2 \cdot FoM_{ADC} \cdot BW \cdot \left(2^{N_{ADC}} + \frac{1}{4} \cdot 2^{9-N_{ADC}} \right) \tag{1.7}$$

where N_{ADC} and N_{DAC} are the nominal resolution of the ADC and DAC respectively.

Function $P_{ADC+DAC}\left(N_{ADC}\right)$ has minimum if N_{ADC} is equal to 3.5. Assuming that the effective number of bit is lower than nominal, the resolution of the ADC is selected to be 4 bits. Accordingly the DAC resolution N_{DAC} is equal to 5 bits.

1.5 Goals of the Work

The goal of this project is to develop and implement a new concept of M-Sequence UWB Radar. Since the content of such work exceeds the requirements of one thesis study which should be completed in the project time frame, the work is realized by four groups working in parallel on different areas of focus. The allocation of the tasks to different groups is shown in Fig. 1.5, where each colour represents a different group. Our focus is on A/D and D/A circuits; it is depicted in orange and abbreviated as "SYS".

Within the frame of this work, high-speed A/D and D/A converters, which are the main building blocks of a data capturing device, should be designed, developed and tested to satisfy the requirements. In following phases of the project, they will be assembled together with the other sub-blocks to build the complete radar system.

The specifications of these converters are summarized in Table I.

Table I. Target specification of the A/D and D/A converters.

Parameter	ADC	DAC
Sample rate	10 GS/s	10 GS/s
Bandwidth	5 GHz	5 GHz
Resolution	4 bit	5 bit
Static accuracy	< 1LSB < 6.25 %	< 0.625 LSB < 0.2 %
Dynamic range	1 V_{p-p}	0.5 V_{p-p}
Calibration	–	off-chip
P_{diss}	min	min

Chapter 2. Implementation of Track-and-Hold Amplifier

2.1 Overview of High-Speed THA's Architectures

2.1.1 Parameters of the THA

The track-and-hold amplifier (THA) is a crucial component of the ADCs. It performs the continuous-time to discrete-time conversion of the A/D function, and provides a temporary constant output to subsequent stages. Often, the THA performance is the bottleneck in A/D converters that are operating at the technological limits. Power dissipation is another important criterion in THA design, making it even more difficult to achieve high speed with accuracy.

There are four groups of specifications that describe basic THA operation: track mode, track to hold transition, hold mode, hold to track transition [10]. These specifications are summarized in Table II.

Table II. THA specifications.

	Track Mode	Track-to-Hold Transition	Hold Mode	Hold-to-Track Transition
Static	• Offset • Gain Error • Nonlinearity	• Pedestal • Pedestal Nonlinearity	• Droop Rate • Dielectric Absorption	
Dynamic	• Settling Time • Bandwidth • Slew Rate • Distortion • Noise	• Aperture Delay Time • Aperture Jitter • Switching Transient • Settling Time	• Feedthrough • Distortion • Noise	• Acquisition Time • Switching Transient

The parameters in Table II can be analyzed in two groups: static and dynamic. Generally maximization of parameters in the one group leads to degradation of parameters in the second group. For instance it is difficult to achieve a low droop rate keeping high bandwidth, or to achieve a small pedestal error and keep short acquisition time.

Besides these parameters, the power dissipation has tendency to increase with maximizing the static performance and drastically increases with the higher speed.

2.1.2 Open-loop THA based on Switched Emitter Follower

The target for the operation speed of track-and-hold amplifier is GS/s range. Therefore, the open-loop architecture is the best choice for achieving maximum speed.

One of such architectures was proposed by Vorenkamp and based on the switched emitter follower (SEF) [11]. The main advantage of the SEF is its compatibleness with 3 V supply voltage. The other switch configuration which is

widely used in past is based on the diode bridge [12], and needs voltage supply to be more than 2.8 V plus the input rage [13].

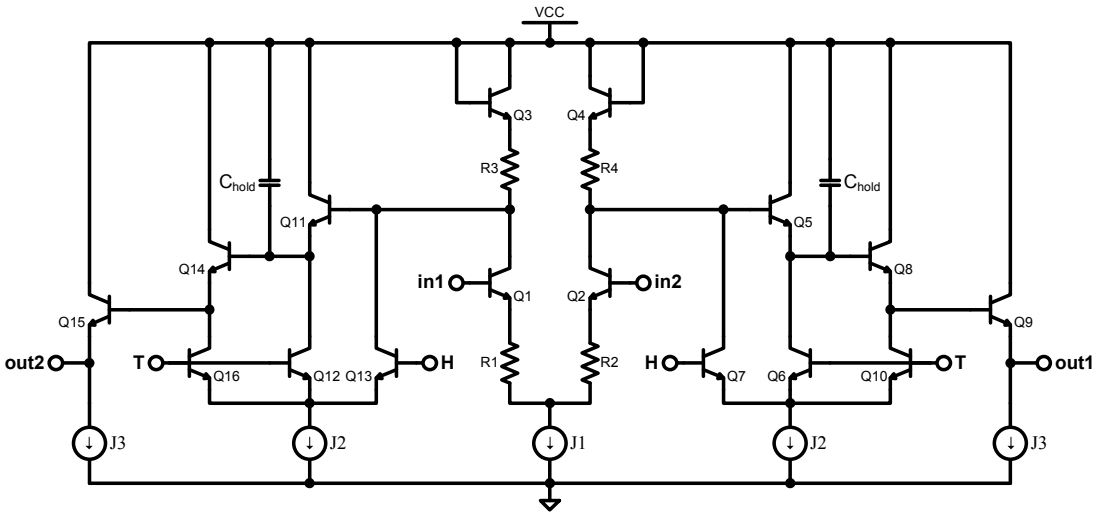


Fig. 2.1 THA proposed by Vorenkamp.

The core of the proposed THA is depicted in Fig. 2.1. It consists of:

- An input buffer; differential stage with emitter degeneration.
- Two switched emitter followers.
- Output buffers.

The output buffer depicted in the Fig. 2.1 is pseudo-differential, but it can be implemented like the input buffer, the differential pair with degeneration. In this case the circuit would be fully differential.

Two diode-connected transistors *Q3* and *Q4* in the input buffer compensate modulation of the base-emitter voltage (V_{be}) of the input stage. These transistors generally could be omitted with the consequence of losing accuracy.

Additional capacitances, not shown in Fig. 2.1, can be connected between outputs of the input buffer and inverse outputs of the SEF [11]. These capacitances serve to suppress feedthrough and their values ideally should be equal to parasitic base-emitter capacitance of transistors *Q5* (*Q11*).

Advantages of this architecture, such as high-speed and simplicity, are already mentioned. These advantages also give rise to some disadvantages. The simplicity and possibility to omit an additional compensation limit the accuracy of the amplifier. Vorenkamp, with his work in [11], has achieved 10 bits effective resolution at hundred MHz, the resolution at GHz range drops drastically. Depending on the implementation, the accuracy is mostly in the range of 6-8 bits [14][15].

2.1.3 THA with improved feedthrough suppression

At high frequencies the hold mode feedthrough can destroy the performance of the THA. The value of the feedthrough A_f is dependent on the relation between the parasitic capacitance C_{be} and the hold capacitance C_H and is expressed by formula [11]:

$$A_f = \frac{C_{be}}{C_H + C_{be}} \tag{2.1}$$

In the modern high-speed THAs the hold capacitor is usually small in order to get higher bandwidth and save power. The voltage, stored in hold capacitance, is changed during hold phase due to the parasitic junction capacitance C_{be} which is exposed to high frequency alternating input. The change can reach value of tens millivolt.

A methodology, first proposed by Bernd Prégardier in [16] and further improved by Thorsten Baumheinrich in [17], serves the purpose of suppressing the input feedthrough during hold phase.

An idea is to make input of the switch constant during the hold phase. Here, switch refers to the circuit which conducts/isolates the input buffer from the hold capacitor. The input of the switch would be constant if the sum of direct and inverse signals would be applied on the switch during hold phase. This sum is equal to zero and no feedthrough would be observed.

A practical implementation is schematically shown in Fig. 2.2. Outputs of the two input buffers, main and auxiliary, are cross-connected and applied to the switch. During the track phase the auxiliary input buffer is disconnected and connected only

during the hold phase. Both buffers work together in return-to-zero mode, thus during the track phase the analog input is applied on the switch, and during the hold phase – the constant zero signal is applied.

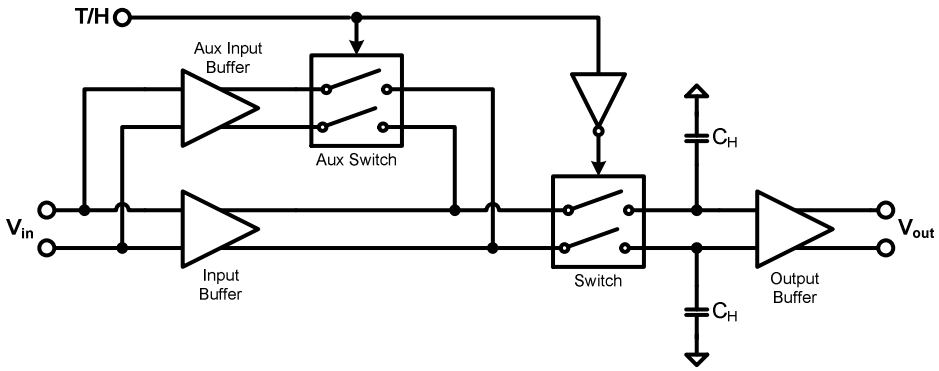


Fig. 2.2 Block-diagram of THA with additional feedthrough suppression.

The disadvantage of this architecture is a requirement of additional circuitry such as auxiliary input buffer that increases power dissipation and requires more complicated implementation of the input buffer itself due to possible need of the additional voltage headroom.

2.1.4 Quasi-differential THA proposed by Fiocchi

Further improvement to the Vorenkamp's THA was proposed by Fiocchi et al. in [18]. The authors proposed several modifications. First one is related to the input buffer. Differential pair as the input buffer suffers from modulation of the base-emitter voltage *(V_{be})*. Diode-connected transistors (*Q3*, *Q4* in Fig. 2.1) only partly compensate nonlinearity caused by this modulation [18]. Fiocchi et al. have proposed to use a high-gain amplifier with negative feedback which has unity closed-loop gain. Fig. 2.3 illustrates proposed input buffer and switch. The input buffer is a differential pair with current source as active load; the switched emitter follower is similar to SEF proposed by Vorenkamp. The difference is the clamping transistor Q_{clp}, which fixes output voltage of the input buffer one V_{be} below the input during the hold phase. The clamping transistor allows minimizing the timing constant and achieving a higher bandwidth.

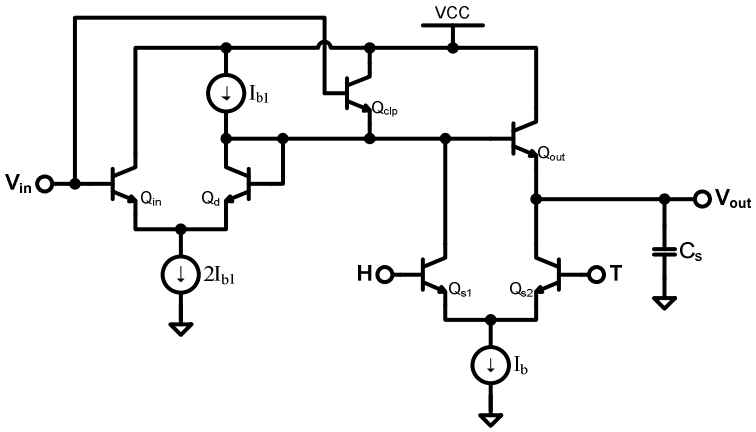


Fig. 2.3 Input buffer and switch.

The configuration depicted in Fig. 2.3 suffers from high hold-mode feedthrough because the input voltage V_{in} is directly connected to the base of the clamping transistor. Fiocchi proposed to insert an additional SEF between input V_{in} and base of the Q_{clp}. The auxiliary switch works in phase with the main switch and in hold mode fixes voltage on the base of Q_{clp} at a constant value. Thus the feedthrough is greatly suppressed. Fig. 2.4 shows the full schematic of the THA including auxiliary switch and output buffer.

This type of the THA has good performance in terms of the speed and accuracy, but it also has some implementation challenges. First of all the design is pseudo-differential. Positive and inverse inputs are processed independently. It means that suppression of the even harmonics relies on matching of the components. The second problem is the high-gain input buffer. Usually it is implemented with an active load using complementary devices. But in the bipolar technologies *p-n-p* devices are seldom available because of cost reasons. Substitution of *p-n-p* devices with *pmos* is not an efficient solution at high frequencies.

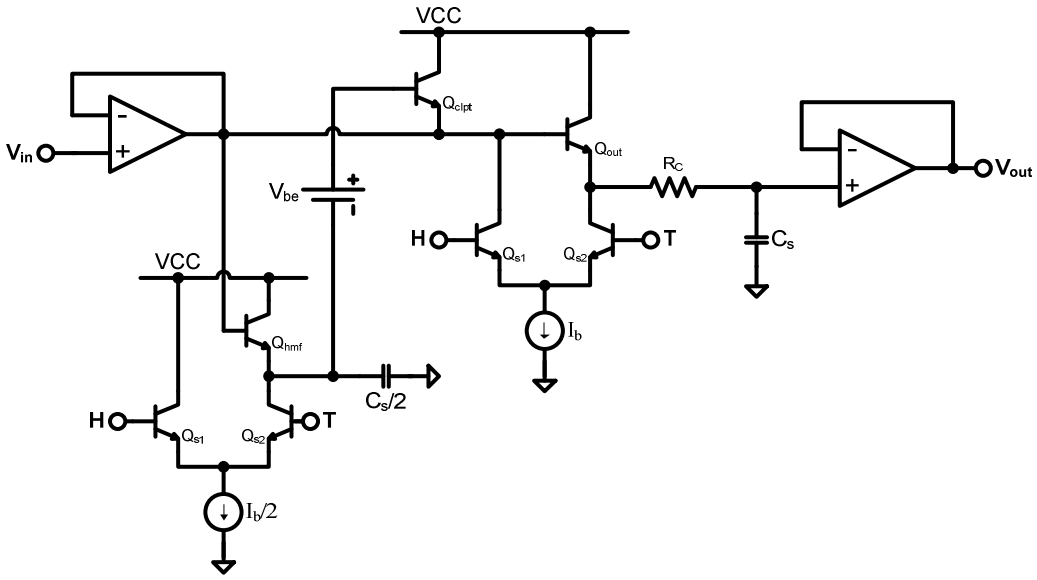


Fig. 2.4 Full schematic of THA proposed by Fiocchi.

2.1.5 Choice of THA architecture

Some A/D converters, such as full flash or folding, do not need the THA because of its parallel structure and simultaneous sampling. But if included in the converter, the THA can relax requirements of the ADC with the cost of additional effort to design the THA itself. There is no simple answer whether the THA is needed or not. The majority of recent works [19][20][21] show that the THA is useful for achieving a high performance. Still, in several designs [22][23][24], where very high performance is also achieved, the THA is not used.

Table III summarizes modern high-speed THAs in bipolar BiCMOS technology. It is difficult to define a trend to select an appropriate architecture; each amplifier has its own set of parameters and was implemented in different technologies. Normalization of parameters using a figure of merit is also not very useful, because architectures have strengths and weaknesses.

A key parameter to select the appropriate THA architecture is the target resolution of the analog-to-digital converter. Aiming 4-bit ADC the open-loop THA based on the switched emitter follower can be the best choice. This architecture can

achieve ~5-7 bits resolution at high sampling rate that is enough for the 4-bit ADC, has low power dissipation, low supply voltage and small die area. Additional attention should be paid for the hold mode feedthrough and droop rate.

Table III. State of the art of high-speed THAs.

Input, V	Input Freq., GHz	Sample Rate, GS/s	THD, dB	ENOB, bit	Power Dis., mW	Ref.
-12 dBm	7	30	29	4.5	270	[14]
1	2	18	32.3	5.1	128	[15]
0.8	0.9	2		8	550	[25]
1	0.6	1.2		8	0.46	[26]
0.6	8	4		6	550	[12]
1	10 7 2	40 18 12	32.1 44.0 50.0	5.1 7.0 8.1	560	[27]
1	1.5 3	12.5	52.4 49.5	8.4 7.9	700	[28]
2	3	10		7.6	800	[29]
	10 19	40	29 27	4.5 4.2	540	[30]

2.2 Implementation of Low Power THA for GS/s Range

2.2.1 Sub-stages design of THA

Generally a track-and-hold amplifier consists of three stages:

- Input buffer – is an input circuitry, which decouple input signal and the switch.
- Switching circuitry (switch) with a storage element, hold capacitor.
- Output buffer – is the circuitry to decouple storage capacitor from following stage.

2.2.1.1 Input buffer

The input buffer, being only a buffering stage, ideally should not change the input signal. It means that the input buffer should have enough bandwidth to work over desired frequency range and a high linearity to deliver the undistorted signal.

There are two common implementations of the input buffer: open-loop amplifier [11], [16] and closed loop amplifier [18]. A simplified implementation of the closed-loop amplifier is shown in Fig. 2.5a. It consists of differential state loaded with a current mirror.

The close-loop gain is set to 1 with a negative feedback; therefore the output signal is a replica of the input. This configuration is very linear but suffers from some drawbacks that limit its usage.

Firstly the amplifier in Fig. 2.5a is single-ended and both even and odd harmonics are present. Second and most significant drawback is the implementation of an active load. The *p-n-p* transistors are not available in the IHP technology. They could

be substituted with *pmos* transistors. Unfortunately the speed of the *pmos* devices quickly degrades at high-frequencies. Some additional techniques, such as an inductive peaking could solve this problem, as described in [28]. But on-chip inductors occupy huge amount of space. The difficulties of the implementation make usage of the closed-loop input buffer impractical.

In contrary the open-loop architecture is easy to implement and it has enough linearity to be used for the medium-resolution A/D converter.

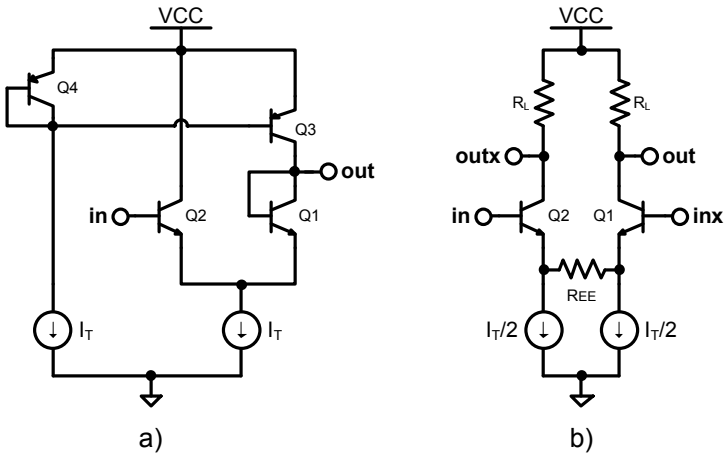


Fig. 2.5 a) Closed-loop unity gain input buffer, b) Open-loop input buffer: differential pair with emitter degeneration.

A typical implementation of the open-loop input buffer is shown in Fig. 2.5 b). It is a convenient differential pair with emitter degeneration for increasing linear region.

A linearity of the open-loop differential buffer can be calculated by estimating the third order harmonic distortion which is [31]:

$$HD_3 \approx \frac{A_1^2}{48 \cdot V_T^2 \left(g_m R_E + 1 \right)^3} \tag{2.2}$$

where:

V_T is the thermal voltage;

A_1 is the amplitude of the input signal;

R_E is the emitter-degeneration resistance.

In order to compensate the modulation of the base-emitter voltage diode-connected transistors could be added between the load resistors and supply node; they are not depicted in Fig. 2.5b. Additional headroom, which is required for the diodes, leads to increased power dissipation. If the low power dissipation has higher priority and the specified resolution is up to 7 bit, these diodes could be omitted.

2.2.1.2 Switching circuitry

A switching circuitry (further switch) consists of the switch itself and a storage element – the hold capacitor. The switch based on SEF proposed in [11] is a good solution for the high-speed THAs. The schematic of this switch is depicted in Fig. 2.6.

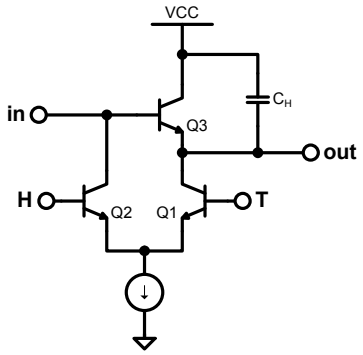


Fig. 2.6 Switched emitter follower.

The design of the switch is always a search of the compromise between speed and accuracy. The speed of the switch is determined by the ratio of the hold capacitance *(C_H)* and switch current *(I_{sw})*. The formula (2.3) shows general relationship between them, where *dt* is the acquisition time.

$$I_{sw} = C_H \cdot \frac{dV_{C_H}}{dt} \tag{2.3}$$

The acquisition time is the maximum time required to acquire a new input voltage once a sample command has been given (Fig. 2.7). The signal is acquired when it has been settled within a specified error around its target value of output voltage. The

maximum acquisition time occurs when the hold capacitor must be charged to a full-scale voltage change.

It is apparent from the formula (2.3) that lower the hold capacitance is, lower the current of the switch to achieve target speed characteristics will be. But the value of hold capacitance directly affects other parameters, such as droop rate and pedestal offset (also called pedestal error).

A parasitic collector-base capacitance C_{cb} between the base of *Q1* and the hold capacitor causes a charge (pedestal) error. The magnitude of the charge error depends from the value of the hold (C_H) and parasitic (C_{cb}) capacitors and calculated by [32]:

$$Q_\varepsilon = \Delta V_{TH} \frac{C_H \cdot C_{cb}}{C_H + C_{cb}} \tag{2.4}$$

where ΔV_{TH} is the amplitude of the switching voltage applied on the base of *Q1*

The pedestal offset $V_{pedestal}$ can be determined by:

$$V_{pedestal} = \frac{Q_\varepsilon}{C_H} = \Delta V_{TH} \frac{C_{cb}}{C_H + C_{cb}} \tag{2.5}$$

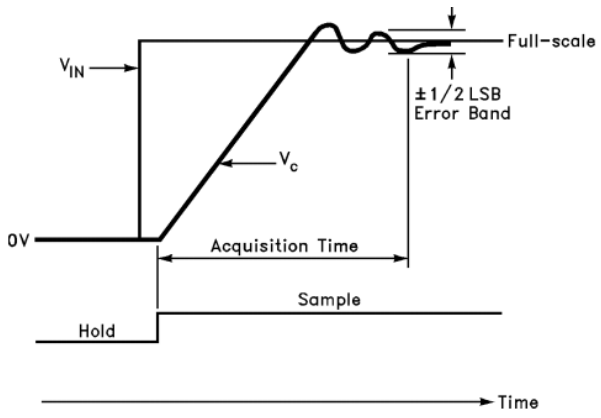


Fig. 2.7 Acquisition time of the THA.

The droop rate is the rate at which the output voltage is changing due to leakage from the hold capacitor. For the high-speed circuits, it is usually expressed in *mV/nS* and calculated by equation:

$$\frac{dV_{C_H}}{dt} = \frac{I_L}{C_H} \tag{2.6}$$

where I_L is the leakage current.

Both pedestal error and droop rate are inverse proportional to the value C_H of the hold capacitance, therefore to assure error-free functionality of the THA the value of the capacitor has to be maximized.

For calculation the value of the hold capacitor the following parameters are specified:

- Input range : 1 V_{p-p}
- Sample rate: 10 GS/s
- Target resolution: 8 bit

Using formulas (2.3), (2.5) and (2.6) and assuming the leakage current 30 µA it can be calculated that the minimum value of the hold capacitance is 300 fF. Current of the switch, which is required for proper work, is approximately equal to 3.5 mA.

In hold mode a feedthrough of the input signal will add additional error to the stored voltage. This happens due to parasitic base-emitter capacitance in the switch transistor *Q3*. The feedthrough could be decreased by adding a feed-forward capacitance C_{ff} between output of the switch and inverse output of the input buffer. This capacitance is shown in the full schematic of the THA in Fig. 2.10 on page 32. The suppression of the feedthrough is maximal if the feed-forward capacitance is equal to the parasitic capacitance $C_{be_{Q3}}$. In practice it is realized by connecting four transistors as depicted in Fig. 2.8. The transistors are identical to *Q3* and resulting capacitance is equal to base-emitter capacitance $C_{be_{Q3}}$.

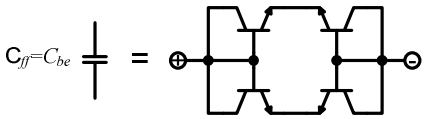


Fig. 2.8 Implementation of feed-forward capacitor.

Fig. 2.9 a) and b) demonstrate operations of the THA in track and hold-mode, respectively. In the track mode, when the track signal is high, transistors *Q3* and *Q6* are switched off. The input signal passes through the input buffer and emitter follower *Q5 (Q8)* to the output, charging/discharging hold capacitor C_H. In the hold mode, when the hold signal is high and track is respectively low, transistors *Q4*, *Q5 (Q7*, *Q8)* are off. Current *I2 (I3)* flows through the input buffer and makes additional voltage drop at the resistor R_L (Fig. 2.9b). This additional voltage drop turns emitter follower *Q5 (Q8)* off. The output voltage is kept constant and equal to the voltage stored in the hold capacitor.

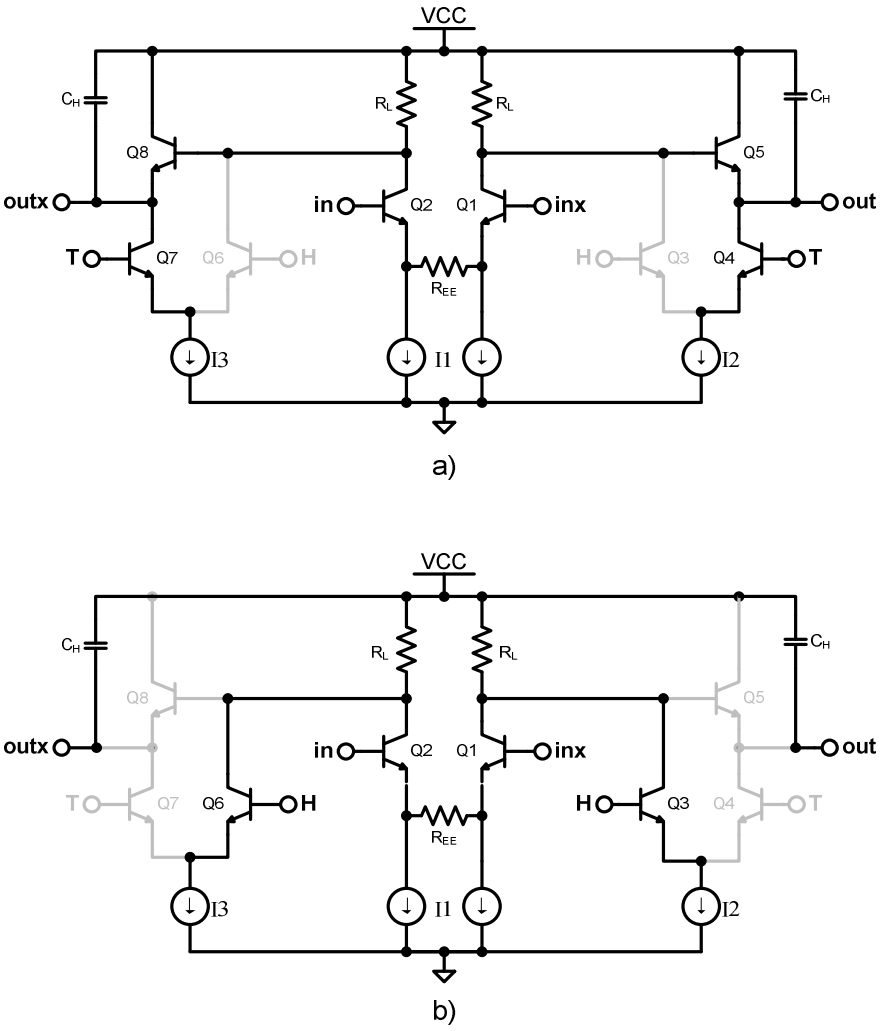


Fig. 2.9 Operation of THA in: a) track mode, b) hold mode

2.2.1.3 Output buffer

The THA is placed in front of the A/D converter. The input stage of the high-speed A/D converter is quite powerful because it should drive a bank of the comparators. Direct connection of the ADC to the switch will cause a high leakage current and increase requirements to the switch. To have a buffer stage between the THA output and ADC input, hence to decouple the switch from the following stage, an output buffer is required.

In this work, an emitter follower was used as output buffer. It has good linearity, good driving capabilities and works at high speed.

Although the output buffer has to prevent the switch from being loaded, it has non zero leakage current which flows into the base of transistor *Q9 (Q11)*. To compensate this leakage current an additional compensation was implemented. An idea is to inject the same amount of current which flows out, into the hold capacitor. The compensation circuitry is depicted at the full THA schematic in Fig. 2.10; it consists of transistors *Q10, M1, M2 (Q12, M3, M4)*. The transistor *Q10 (Q12)* provides reference current equal to the base current of *Q9(Q11)* to the current mirror *M1-M2 (M3-M4)*. The reference current is mirrored and injected into the base of *Q9(Q11)*, and thereby the leakage current of the hold capacitor is compensated.

Speed characteristics of the compensation circuitry do not play a crucial role. The current of the current source of the output buffer is modulated from sample to sample by its input as:

$$\Delta I_{4,5} = \frac{\Delta V_{C_H}}{r_{o,I_{4,5}}} \tag{2.7}$$

where ΔV_{C_H} is the a change of the stored voltage and $r_{o,I_{4,5}}$ are the output resistances of the current sources $I_{4,5}$. The modulation of the leakage current is β times lower (2.8) and approaching to zero, assuming high β and high output resistance.

$$\Delta I_{Q_{b_{9,11}}} = \frac{\Delta V_{C_H}}{\beta \cdot r_{o,I_{4,5}}} \tag{2.8}$$

Therefore AC component of the leakage current can be neglected and only DC component has to be compensated.

50 Ohm test buffers were added only for testing purposes. They are simple common-emitter amplifiers with emitter degeneration and linearization diodes.

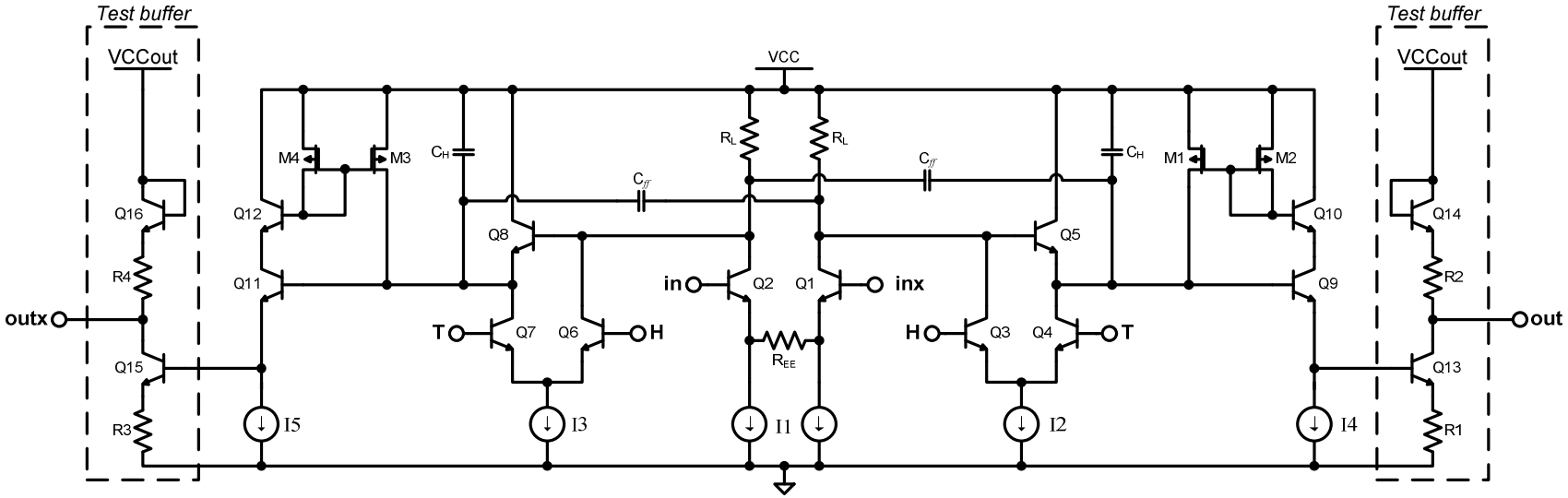


Fig. 2.10 Full schematic of the THA.

2.2.2 Experimental results

The track-and-hold amplifier has been realized in a 0.25μm 190 GHz SiGe HBT BiCMOS technology. It occupies an area of 0.5 mm^2 including pads; the core part of the circuit, which excludes clock and test buffers, is 50x100 μm^2. Fig. 2.11 shows the chip microphotograph of the THA.

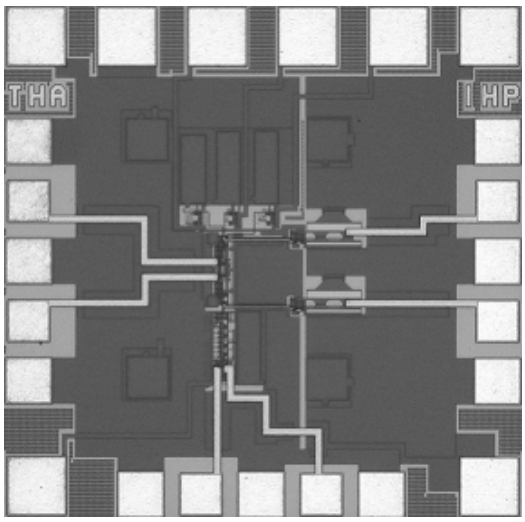


Fig. 2.11 THA test chip micrograph.

The test chip was wire-bonded on a ceramic test board for the measurement. Functionality of the circuit was tested with a high-speed Agilent Infiniium 86100b sampling oscilloscope. The circuit operates up to 15 GS/s sampling rate. That is illustrated in Fig. 2.12, where the oscilloscope plot of THA output at f_{in} = 1.5 GHz, f_s = 15 GHz is depicted.

To measure THA in frequency domain the DUT has to be connected to the spectrum analyzer. Another possibility is to collect data in time domain during several periods and apply Fourier transformation on it, but no high-speed capturing device was available. Unfortunately, only one 180° hybrid and no phase tuner was available for measurement in the required frequency range. Due to this limitation, the differential circuit has been operated in single-ended mode during measurements.

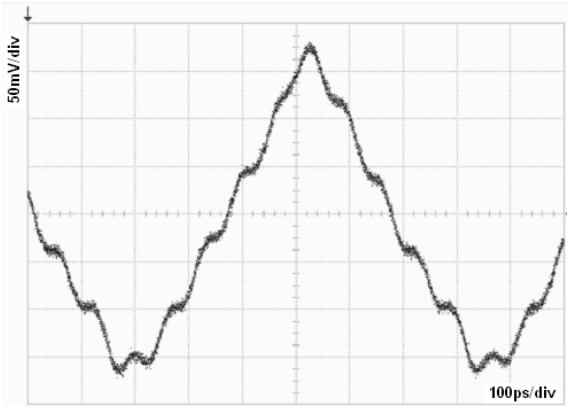


Fig. 2.12 Differential output of the THA at f_{in} = 1.5 GHz, f_s = 15 GHz.

The frequency domain measurement set-up is shown in Fig. 2.13. The input of the THA was driven differentially. The external clock signal was single-ended. This was partly compensated by internal clock buffers, which internally reconstruct differential signal from the single-ended signal. Reconstructed differential signal has longer rise/fall time that potentially increases acquisition time during switching from hold to track mode; and could cause error in stored signal during transition from track to hold mode because of slow turning off the switch. Only the positive output was connected to the spectrum analyzer. The inverse output was terminated to 50 Ω.

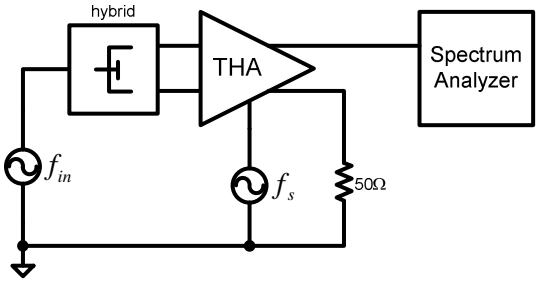


Fig. 2.13 Measurement setup for characterizing THA in frequency domain.

Fig. 2.14 shows the measured output spectrum of the single-ended THA at an input frequency (f_{in}) of 1 GHz and a sampling rate (f_s) of 9.99 GS/s. As expected, the second harmonic of the output signal dominates the total harmonic distortion (THD) and causes a large overestimation of the THD. Such single-ended measurement certainly underestimates the performance of the differential circuit.

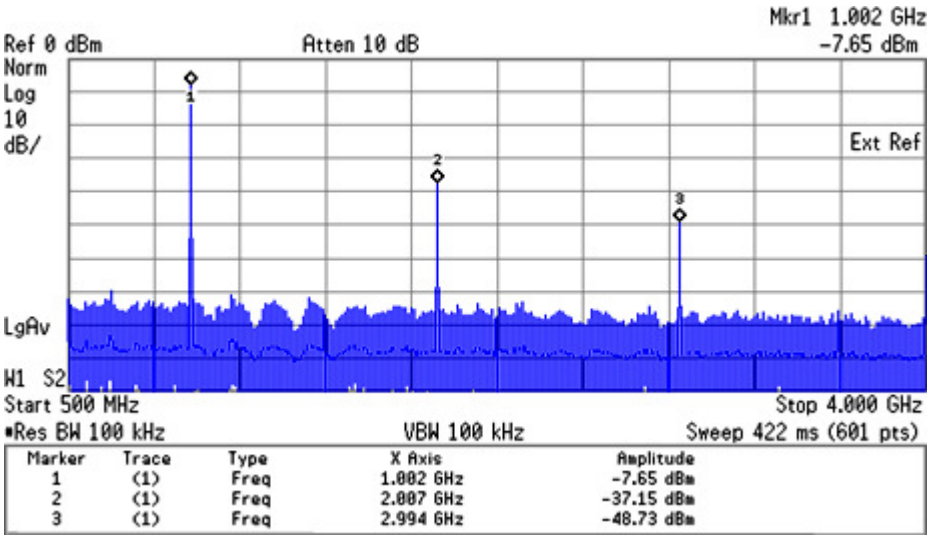


Fig. 2.14 Spectrum of the single-ended output signal.

To obtain a more realistic value for the power level of the second harmonic of the differential output, the measurements have been extrapolated to differential mode using simulation results. Fig. 2.15 gives a comparison of the measured data with the results of a post-layout simulation, both for the single-ended output case.

The post-layout simulation results of the first and third harmonics have very good correspondence with measured values. The second harmonic is suppressed by 40 dB by switching from single-ended to differential mode. There are no arguments that circuit might behave differently during measurements. For safety concerns, the value of 40 dB was halved before being used for estimation of the THD. The expected value of the second harmonic is marked with a green triangle in Fig. 2.15. Formulation of the THD shows that it has strong dependence on third harmonic. The calculated value of the THD is – 41 dBc. It corresponds to an effective number of bits (ENOB) of 6.8 bits.

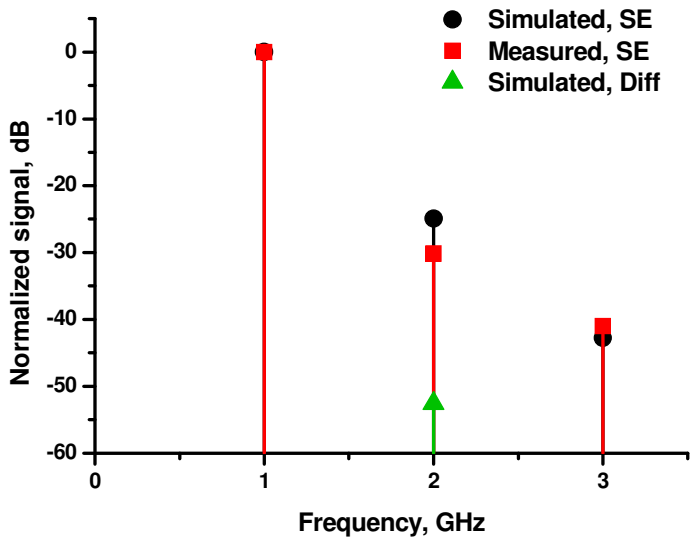


Fig. 2.15 Single-ended measurement, simulation and extrapolation at f_{in} = 1 GHz, f_s = 9.99 GHz.

The main parameters of the THA are summarized in Table IV. Table V compares this work with similar THA designs in Si and SiGe technologies. The present THA's power dissipation is less than ten percent of that of any other high-speed THAs listed in the table. It does not achieve the accuracy and speed of the enhanced Fiocchi THA implemented in the same technology [28], but still, it is the second fastest THA on silicon with ENOB greater than 6 bits, known to the author, and it is much more power efficient than other high-speed THAs.

Table IV. Summary of the THA characteristics.

Process	SiGe HBT, f_T = 190 GHz
Input range	1 $V_{p\text{-}p}$ differential
Sampling rate	10 GHz
Differential droop rate	<10 mV/ns
THD at f_{in} = 1 GHz, f_s = 9.99 GHz	41 dBc
Bandwidth	2.5 GHz
Supply voltage	3.3 V
THA core power dissipation	30 mW
Total power dissipation	70 mW
Die size, with bond pads	0.5 mm^2

Table V. Comparison with published Si/SiGe high-speed THAs.

f_{sample}, GHz	f_{in}, GHz	Input, V_{pp}	ENOB, bit	BW, GHz	Supply, V	P_{diss}, W	Process/f_T, GHz	Ref.
2	0.9	0.8	8	0.9	-3.3	0.55	SiGe/65	[25]
12.1	1.5	1	8	5.5	3.5	0.7	SiGe/200	[28]
1.2	0.6	1	8	2	+2/-5	0.46	Si/25	[26]
4	8	0.6	6	10	5.2	0.55	SiGe/45	[12]
10	1	1	6.8[1]	2.7	3.3	0.03[2]	SiGe/200	this work

[1] Extrapolated from the measured single-ended signal.

[2] Test buffers and clock driver (40 mW) are not included.

2.2.3 Improved THA

The measurements on the amplifier described above, showed that the bandwidth of the THA is limited.

The second problem was the high clock feedthrough at GHz frequencies. Moreover despite THA can logically be divided to input buffer, switch and output buffer, the input buffer and switch could not be considered independently from each other. As it is described above, in hold mode the input buffer and the switch are sharing the same load and they could not be optimized independently.

Further work has been done to improve the THA for achieving higher bandwidth together with higher linearity. It was also proven by measurement that the used architecture is well suited for high-speed and has potential for achieving better performance.

Therefore the work was concentrated in two directions:

- Increasing the bandwidth by reducing RC constants in the signal path.
- Minimizing feedthrough.

The biggest RC constant is created by load resistor R_L of input buffer and hold capacitor C_H. It is a bottleneck for the high-speed signal which has to be optimized. Other parasitic capacitances are much lower and could be neglected.

There is not too much freedom to minimize R_L and C_H values. As already shown above, the hold capacitance could not be less that 300 fF to assure 8 bit accuracy. The only possibility is to reduce load resistance of the input buffer by accordingly increasing the tail current.

The feedthrough minimization was achieved by two means. First, a direct suppression was added. Second, the SEF was modified to achieve better performance including better feedthrough suppression.

As described above, Pregardier in [26] proposed to add an auxiliary input buffer which will suppress the feedthrough in hold mode. This input buffer is depicted in Fig. 2.16, where the whole schematic without clock and test buffers is shown. Auxiliary

and main buffers share the same load R_L but they have cross-coupled outputs. The switches *Q5-Q6* and *Q7-Q8* disconnect auxiliary buffer from the main buffer during track mode, and connect during hold mode.

At transistor level the suppression works as the following: during the track phase a current I_1 of the attenuator flows through the transistor *Q5* and *Q8* and does not make any influence on the output of the differential pair *Q1-Q2.* In the hold mode current *I1* of auxiliary buffer flows through the transistors *Q6*, *Q7* and through the load resistors R_L of the main input buffer. Because the main and auxiliary buffers are cross-connected, the output of the main buffer is pulled to zero and is kept constant during whole hold phase.

The next modification is related to the switched emitter follower. The SEF proposed in [11] was modified accordingly to SEF proposed in [33]. The difference is an additional emitter follower stage *Q12(Q16)* with clamping resistor R_H. In this configuration current I_2 of the switch flows not trough the load resistor R_L of the input buffer, but through the resistor R_H and transistor *Q12 (Q16).* A voltage drop on R_H turns off transistor *Q11(Q15).* Switch in this configuration has better rejecting properties, i.e. feedthrough is lower. Also it prevents input buffer from being saturated.

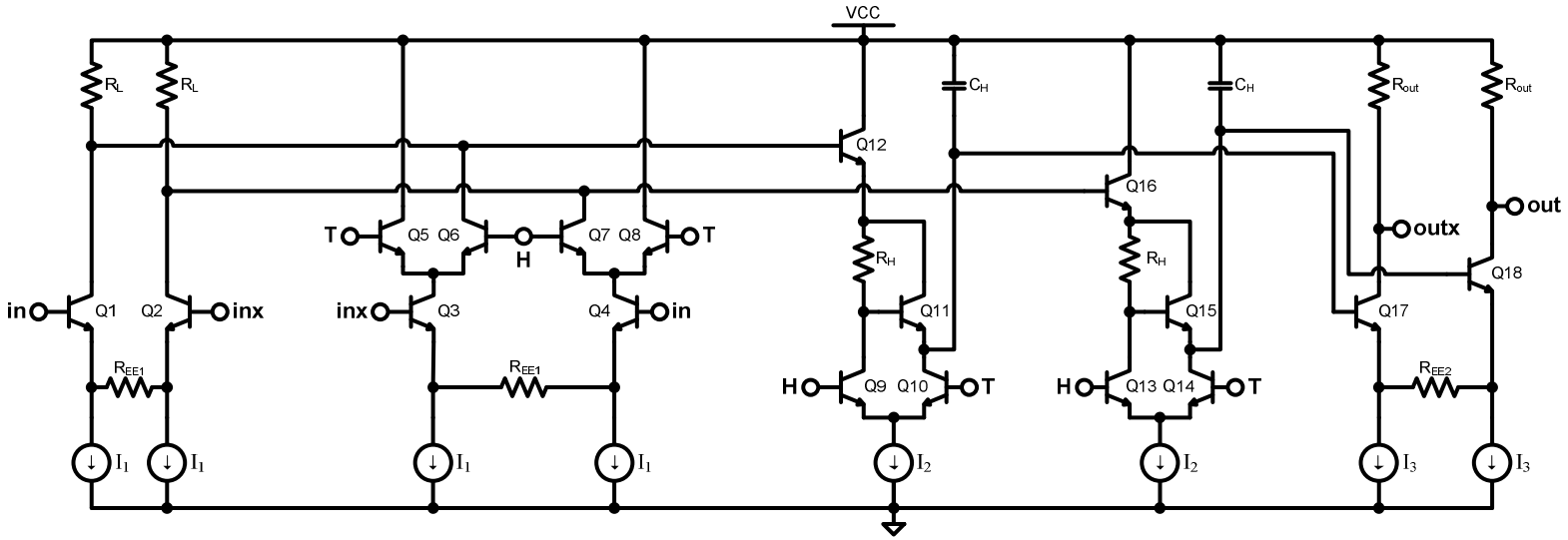


Fig. 2.16 Schematic of the improved THA. Test and clock buffer are not included.

2.2.3.1 Measurement results

The THA was implemented in 130 nm SiGe BiCMOS experimental technology. An active part occupied approximately 200x200 µm; it is comparable with size of the two test pads. Fig. 2.17 shows the chip micrograph of the whole test chip.

The measurement set-up is similar to the set-up depicted in Fig. 2.13 with difference that instead of the single-ended spectrum analyzer, a high-speed real time Tektronics TDS6154C oscilloscope has been used. The oscilloscope has four high-speed inputs that allow simultaneous capturing both positive and inverse outputs of the amplifier. It gives us the advantage of the real estimation the differential circuit performance while increasing the measurement error from the oscilloscope. The captured data was post-processed with MATLAB®. As a result, the THA characterization in frequency domain was done by capturing a long data sequence and performing Fourier transformation on it.

Fig. 2.18a illustrates functionality of the THA in track/hold mode. The 1 GHz sine signal was applied to the input of the circuit; the sample rate was 10 GS/s. The second figure, Fig. 2.18b shows the feedthrough in the hold mode. To observe it, the input frequency was fixed at 3 GHz; our frequency of interest, and the sample rate was selected to be half of the input frequency for observing the whole period.

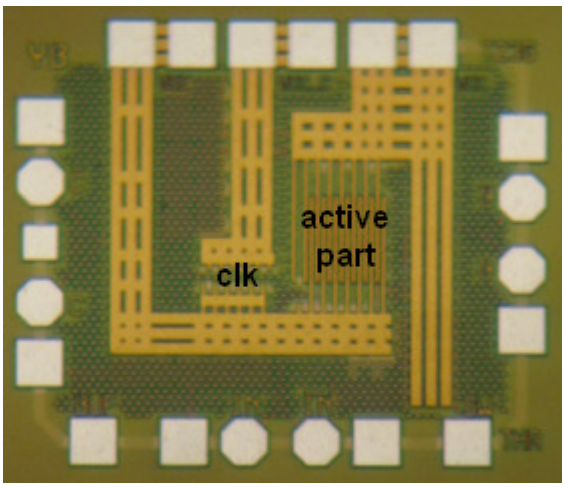


Fig. 2.17 THA chip micrograph.

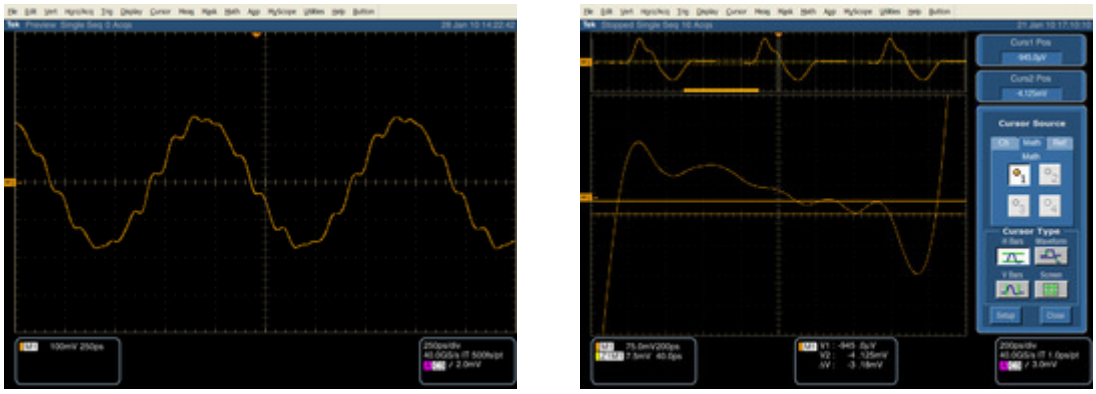


Fig. 2.18 a) Transfer function of 1 GHz input signal at 10 GS/s sample rate, b) Feedthrough at3 GHz input.

Fig. 2.18b shows the whole output curve (upper curve) with the zoomed in view of the region of interest (lower curve). The quasi-constant output signal has 3 GHz ripple and decay over time. 3 GHz ripple is the feedthrough and its amplitude is 3.8 mV. The amplitude of the input signal is 1 $V_{p\text{-}p}$; the rejection rate is more than 48 dB.

For the characterization in frequency domain several periods of the output signal, like depicted in Fig. 2.18a were captured. 100-200 periods are enough to achieve reasonable accuracy of measurement. Collecting more data will change the power of harmonics less than 0.1 dB, which is comparable with the error of the oscilloscope. The captured output signal in time domain was transformed into frequency domain by Fourier transformation. The total harmonic distortion (THD) is a measure of the linearity of the output signal and can be calculated by:

$$THD = 20 \cdot \lg \left(\frac{\sqrt{\sum_{k=2}^{\infty} A_k^2}}{A_1} \right) \tag{2.9}$$

where A_1 is the *rms* value of fundamental signal, and A_k – are the *rms* values of the harmonics. In practice only a finite number of harmonics are taken into account.

The total harmonic distortion values of the three different chips were measured. From THD value the effective number of bit was calculated by:

$$ENOB = (THD - 1.76)/6.02 \tag{2.10}$$

The results are depicted in Fig. 2.19, where ENOB over frequency range up to 3 GHz is given. The simulation results are also presented in Fig. 2.19. With this plot, it can be observed that there is good agreement between simulation and measurement results. The circuit shows an unexpected behaviour at higher frequencies; the linearity is increasing instead of decreasing. This effect could be easily explained by limited bandwidth of the oscilloscope. The fundamental harmonic is not attenuated but higher harmonics are. It leads to increasing the THD. Because of this, the THA was measured only up to 3 GHz input frequency.

There is also an artifact at frequency 2.5 GHz. It can be explained only due to some parasitic influence of the test board and/or equipment but not the particular THA implementation. Track-and-hold amplifier does not contain any components that are expected to present a specific behaviour at the frequency.

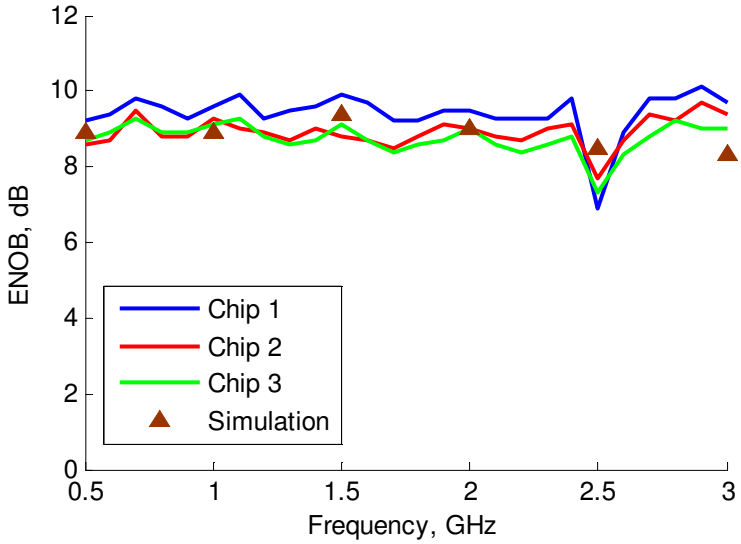


Fig. 2.19 ENOB values versus input frequency (several chips).

Performance comparison of the THA with modern high-speed competitors is given in Table VI. Apart from working in gigahertz range, all chips have very different characteristic. To compare them a figure of merit (FoM) is useful. For the data

converters the commonly referred figure of merit shows the quantity of energy required for a conversion step, is expressed in Joule, and is calculated by:

$$FoM = \frac{P_{diss}}{2 \cdot f_{in} \cdot 2^{ENOB}} \tag{2.11}$$

where P_{diss} is a dissipated power, f_{in} is an input frequency and $ENOB$ is an effective number of bit. Since the THA is used in front of the data converter, the same equation was used to calculate FoM value of THAs. The track-and-hold amplifier is always aimed to be integrated in data converter; therefore power dissipation of the test and clock buffer could be excluded from calculation of the FoM value. But not all published results at Table VI include complete information how FoM was calculated. To avoid misunderstanding, the FoM value of this work was calculated including test and clock buffers. In the brackets the “pure” FoM value is also given. Table VI is visualized in Fig. 2.20, where conversion effectiveness of all amplifiers are depicted.

Table VI. Comparison of high-speed THAs.

Input, V_{p-p}	f_{in}, GHz	f_{clk}, GHz	THD, dB	ENOB	Power, mW	FoM, pJ	Ref.
1	10 3 2	40 18 12	32.4 44.2 50.5	5.1 7 8.1	560	0.82 0.7 0.51	[27]
1	1.5 3	12.5	52.4 49.5	8.4 7.9	700	0.69 0.48	[28]
	10 19	40	29 27	4.5 4.2	540	1.17 0.78	[30]
-12 dBm	7	30	29	4.5	270	0.84	[14]
1	2	18	32.3	5.1	128	0.95	[15]
2	3	10		7.6	800	0.68	[29]
1	3	10	50	8	325 (140[1])	0.21 (0.09[1])	this work

[1] Without test and clock buffers

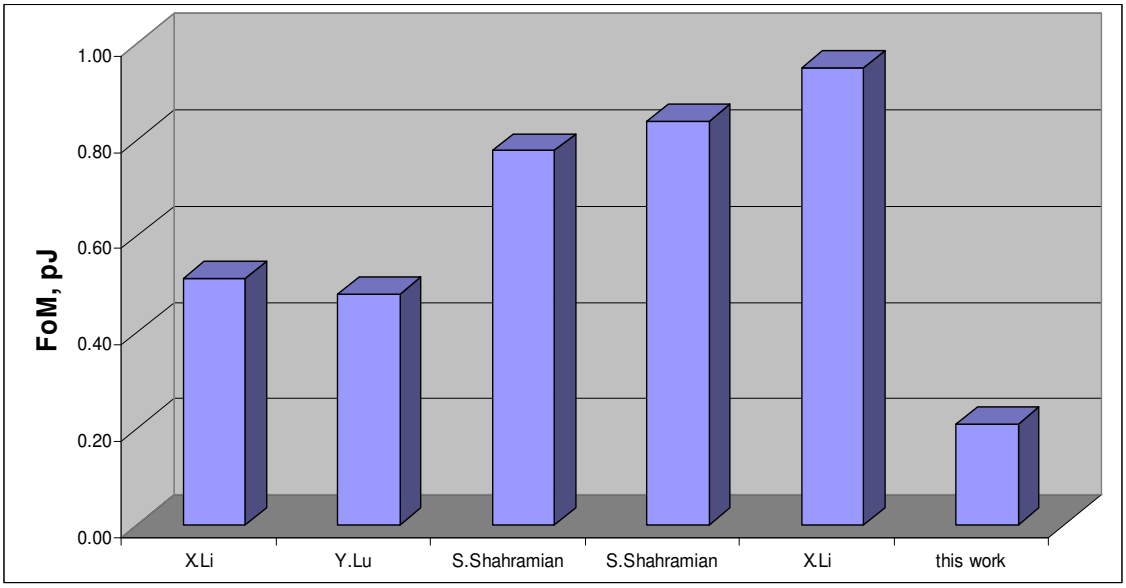


Fig. 2.20 FoM values of modern THAs.

2.3 Conclusion

Two designs of the track-and-hold amplifier were presented in this chapter. Both amplifiers are very effective in terms of power/accuracy. They have lowest FoM value among competitors.

The strength of the first amplifier [34] is power dissipation in GS/s range. It dissipates less than 10% of power of nearest competitor (Table V, page 37). The low power dissipation was achieved by using low tail currents in input buffer and switched emitter followers (SEF) together with small hold capacitance to achieve a high speed. The output buffers of THA have to drive powerful input stage of the A/D converter. Strong output buffers cause a big leakage current, which discharge the hold capacitor and change stored voltage during hold period. To prevent this, a leakage current compensation technique was implemented in the output buffers. Using this technique, the low power and good accuracy has been achieved. Due to operation with low supply voltage and low power dissipation, the track-and-hold amplifier is very well suited to integration in low-resolution A/D converter.

The second THA was improved in several directions. First, the bandwidth was increased to 3 GHz. Second, together with the higher bandwidth the resolution was increased to 8 bit. To achieve better resolution a direct feedthrough suppression using additional input buffer was implemented. The switched emitter follower was also modified for better speed performance. The current path in SEF was isolated from the input buffer. The input buffer and SEF do not share the same load as in [34] to prevent the input buffer from saturation. The THA is now suitable to be integrated in high-speed medium-resolution A/D converters.

Chapter 3. Implementation of High-Speed Analog-to-Digital Converters

3.1 Overview of High-Speed ADC's Architectures

3.1.1 Full flash ADC

The fastest and simplest architecture of the A/D converters is well-known under the name “full flash”. The full flash converter simultaneously compares input signal with set of reference signals and immediately gives a result. The architecture owes its name to its instantaneous operation. Fig. 3.1 shows the basic block-diagram of the full flash converter. The full flash converter consist of a reference network – the block where the reference signals are generated, which is not included in Fig. 3.1; a bank of comparators – the block to digitize the input signal and encoder circuitry – the block, where the thermometer output of the comparators is corrected and encoded into desired format.

The full flash ADC can achieve GHz range and there are several papers that report such performance [19][20][21][35][36]. This architecture is most often used for the fastest converters. A more detailed comparison of high-speed converter is given in Table VII on page 60. Along with the speed the full flash ADC has other advantages, such as the regularity in structure which, as consequence, yields a lower design complexity. It benefits from avoiding long interconnections, except the clock lines, and there is no complex signal processing with different propagation delays that requires an additional synchronization. But disadvantages are also very significant. The number of

comparators is doubled with increasing resolution by one bit. The power and the die area are also doubled. Strictly speaking the power dissipation grows by more than a factor two, because increasing resolution by one bit doubles the number of the comparators, but the power of the clock tree is not linearly dependent on resolution. The clock tree nonlinearly grows with resolution and, in GHz range, becomes a considerable part of the whole power budget. It limits practical implementation of the full flash architecture to low-resolution converters. At Table VII (page 60) it is apparent that the resolutions of present converters usually lay in the range of 3-5 bits.

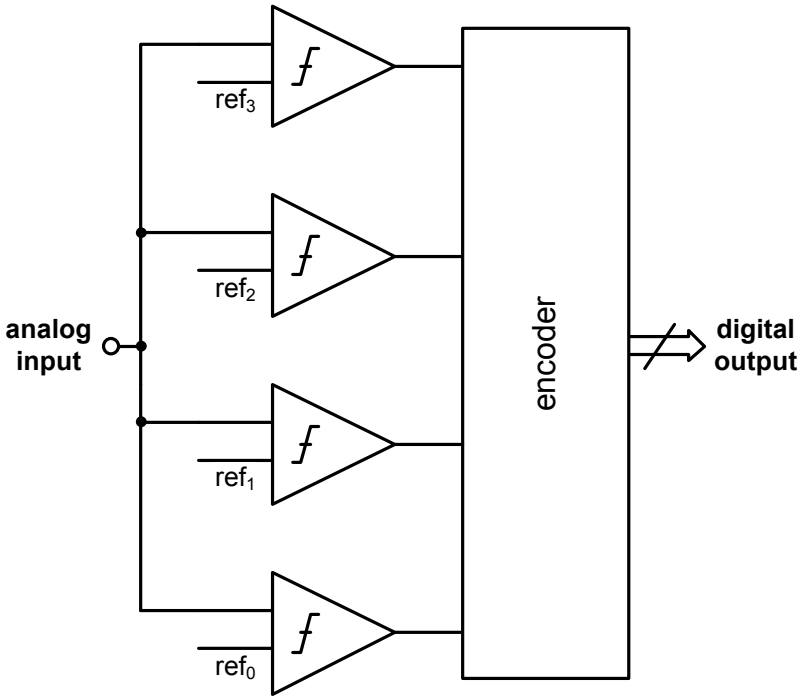


Fig. 3.1 Full flash ADC.

3.1.2 Folding-interpolated ADC

Another type of the converters which incorporates the parallel conversion is the folding-interpolated ADC. There are two ideas behind this structure. The first is to transform the input signal in such a way that input can be digitized with less number of comparators than in full-flash architecture. And the second is to obtain information from

adjacent stages, in other words to interpolate. Strictly speaking, the interpolation could be used in full flash ADC also.

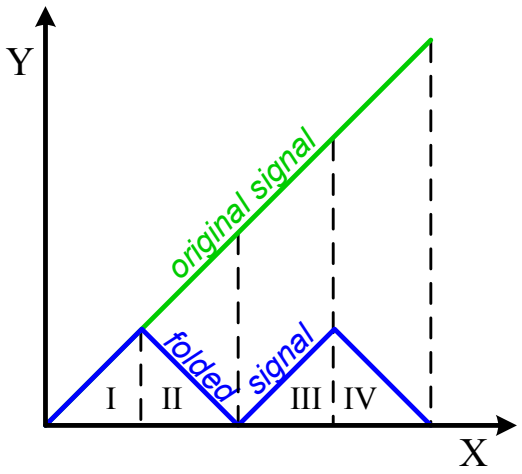


Fig. 3.2 Folding of the signal.

A transformation of the input signal is shown in Fig. 3.2. The standard 1-D signal (original signal, green line), which contains information only in Y-direction, would be converted (folded) into 2-D signal (folded signal, blue line). The folded signal is informative in both directions: X-axis contains information about MSBs; Y-axis – about LSBs. Now for digitizing the input which corresponds to MSBs, $2^{n_{MSB}}-1$ comparators are needed, and for digitizing input which corresponds to LSBs, $2^{n_{LSB}}-1$ comparators are needed, where n_{MSB} is the number of the most significant bits (MSB), n_{LSB} is the number of the less significant bits (LSB) and total resolution is $n = n_{MSB} + n_{LSB}$. The part of ADC which converts the MSBs is usually called coarse quantizer; the part which converts LSBs is called fine quantizer. For the ADC depicted in Fig. 3.4 which has 3 coarse bits and 5 fine bits, the total number of comparator is 7+31=38 instead of 255 which would be needed for the full flash architecture.

The conversion of the normal signal into folded signal is usually done by a folding amplifier (FA). The number of the folds corresponds to the number folding amplifiers.

The benefit of the direct folding of the input signal, as depicted in Fig. 3.2 is quite poor. Folded architecture requires less comparators for quantization but more folding amplifiers. It is due to the case that the quantization in the folding ADC is performed in two steps: with FAs and with comparators. The pure folding ADCs do not need comparator at all; they would be substituted with folding amplifiers.

To omit some folding amplifiers, the technique which is called interpolation is used. The interpolation technique is schematically shown in Fig. 3.3. Fig. 3.3a shows a straightforward solution in which signals in nodes 1-4 are amplified by appropriate amplifiers A1-A4. The output waveform is presented in Fig. 3.3c. Since comparator detects only zero-crossing of the input it is not necessary to use four amplifiers. The output of amplifier A1 and A4 could be interpolated with resistor divider as shown in Fig. 3.3b. The interpolated output will have different shape but it crosses zero at the same point as non-interpolated output in Fig. 3.3c.

Along with possibility to reduce the number of folding amplifier, this technique has other advantages:

- Interpolation is fully passive, i.e. does not require additional power.
- Mismatches of components are averaged, therefore static errors are lower.

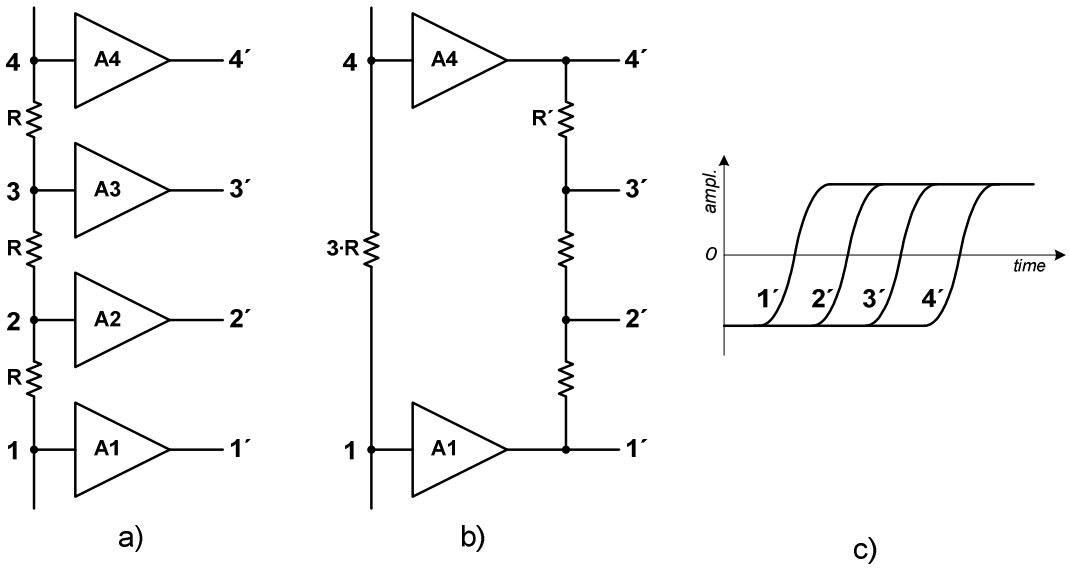


Fig. 3.3 Principle of interpolation: a) Implementation without interpolation; b) Implementation with interpolation of two middle outputs; c) Idealized output waveform.

The disadvantage of the technique is the decrease in bandwidth due to the additional *RC*-chain. Limited bandwidth is critical especially in folding A/D converters. The folding of the input signal means increasing it frequency proportionally to the number of folds. For instance the folded signal (blue) in Fig. 3.2 has four times higher frequency than original one (green). In a typical folding-interpolating ADC [37], the folding factor is 8 which means that internal frequency is 8 times higher than the input frequency.

As is mentioned above, the folding ADC like full flash ADC incorporates the parallel conversion. The block diagram of the 8-bit converter is depicted in Fig. 3.4. An analog input signal goes to track-and-hold amplifier, which in general is not necessary, but it relaxes requirements for the folding amplifier. In the analog preprocessing block the input signal is folded with FAs and interpolated as described above. The output of this block looks similar to the output shown in Fig. 3.3c and represents 32 signals, that cross zero with step of 1 LSB. 32 signals contain 5 bits information and are digitized with a 5-bit flash ADC. Three MSB are digitized in parallel with an additional 3-bit coarse ADC. Because of the lower complexity the 3-bit coarse ADC has a lower propagation delay than the 5-bit fine A/D converter. In some implementations [37], the

coarse ADC is located directly after THA. It results in a time shift between coarse and fine bits. To correct this shift, the propagation delay of the coarse and fine paths of the input signal should be equalized. In the ADC depicted in Fig. 3.4 the coarse ADC takes its input from the analog preprocessing block that would eliminate the propagation delay of the analog preprocessing block. But still synchronization of the digital outputs could be required.

Simultaneous conversion of all bits makes the folding-interpolating ADC a high-speed converter. On the other hand, sophisticated analog preprocessing and high-internal frequency limit both resolution and speed of such converter to mid-range. The conversion speed generally is lower than the speed which could be obtained with a full flash ADC.

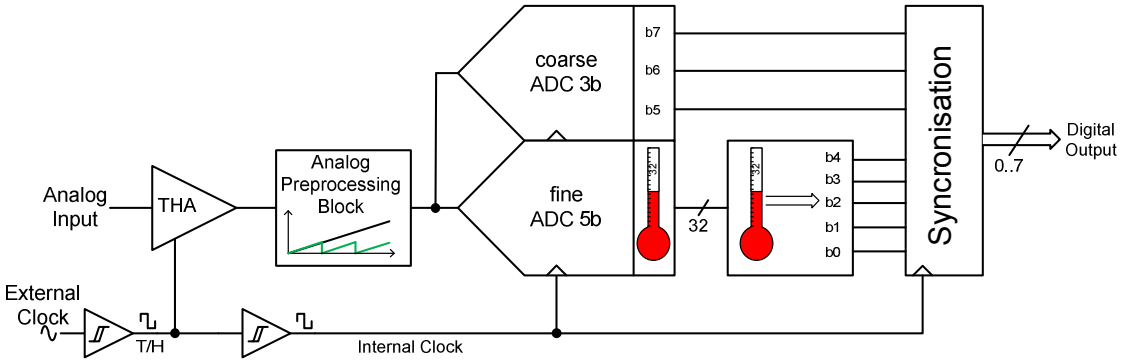


Fig. 3.4 Block-diagram of the 8-bit Folding-Interpolating ADC.

3.1.3 Pipeline ADC

The third type of ADCs, pipeline ADCs, refer to multi-step converters. As is clear from the name, the conversion is done in a “pipe” in several clock cycles. The pipeline ADC consists of N conversion stages (Fig. 3.5). Each stage has k-bit resolution. Total theoretical resolution is $N \cdot k$. Practically the resolution is lower, because some bits are redundant and are used for error correction. Outputs of all stages are collected and corrected digitally.

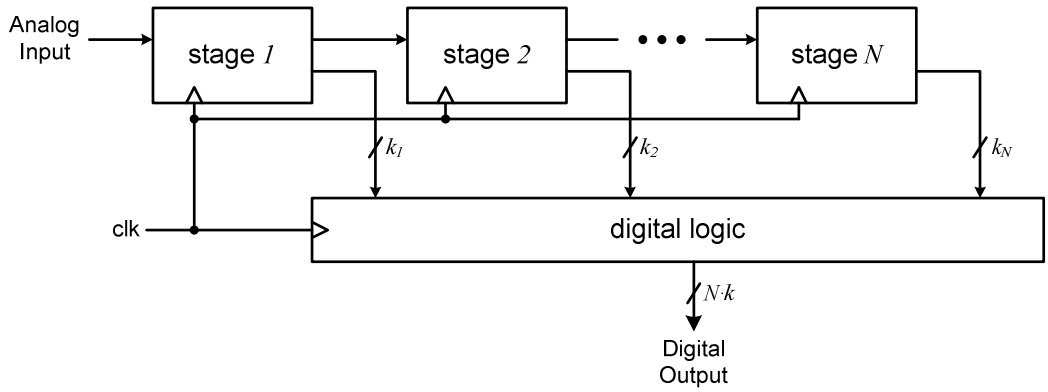


Fig. 3.5 Pipeline architecture.

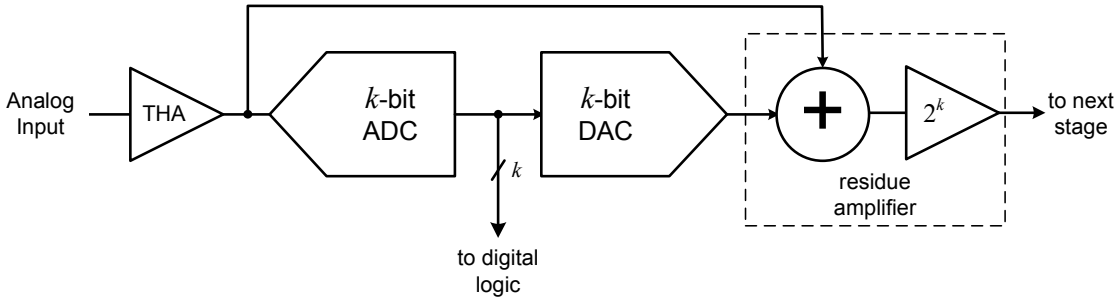


Fig. 3.6 Block diagram of the pipeline stage.

The pipeline stage is schematically shown in Fig. 3.6. It consists of a track-and-hold amplifier, an ADC, a DAC and a residue amplifier. Each stage work as described below:

- The analog input signal is converted to a quasi-constant signal by the THA.
- The ADC digitizes output of THA and produces a *k*-bit output.
- The DAC converts the *k*-bit digital signal again into an analog signal.
- The difference between analog signals after THA and DAC output is a quantization error, which is also called residue. It is processed by the residue amplifier.
- To keep the same dynamic range for all stages, the residue is multiplied by a factor of 2^k.
- The *k*-bit ADC output is saved in digital logic.

All outputs are collected and stored in the digital part. After *N* cycles, when the input signal is sequentially converted by all conversion stages, the complete digital representation of the input signal is available.

In spite of relative simplicity, the pipeline ADC has some challenging blocks which limit the conversion speed. Despite the low resolution of separate stages, the track-and-hold amplifiers, DAC and residue amplifiers should have accuracy which corresponds to full $N \cdot k$ resolution of the ADC. This condition is to be met in order to preserve information for the following stages. Typically a pipeline ADC works in the range of 8-12 bits with hundreds megahertz sample rate.

3.1.4 Successive approximation ADC

An example of the multi-cycle converter is a successive approximation ADC (SAR-ADC). The SAR-ADC implements a binary search algorithm exploiting information about values of previous MSBs. A typical block-diagram of SAR-ADC is shown in Fig. 3.7. It consists of a THA, a comparator, a DAC and a successive approximation register (SAR). The last one controls the binary search algorithm. Generally a SAR-ADC needs $n+1$ clock cycles for digitizing analog signal, where *n* is the resolution of converter. *n* cycles are needed for the conversion and *1* cycle is needed for the sampling by the THA. Therefore the resolution and sample rate of the ADC determine the internal sample rate of the converter. All components should be able to work with high internal clock that limits overall performance of the ADC.

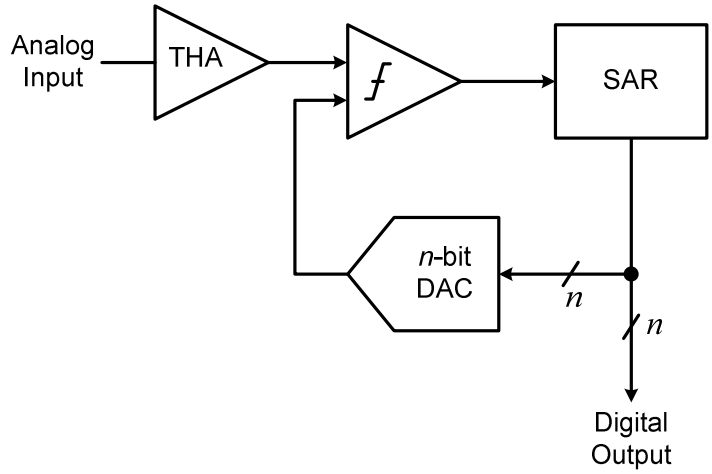


Fig. 3.7 SAR-ADC architecture.

3.1.5 Time-interleaved ADC

The SAR-ADC works with a high internal clock rate but provides an output only once per several clock cycles, hence the sample rate of the converter is lower. Combining several converters in parallel, a higher sample rate could be achieved. The increasing of the sample rate is proportional to the number of the parallel connected ADCs. This configuration is called a time-interleaved ADC, whose block-diagram is depicted in Fig. 3.8. Basically, time-interleaved ADC consists of an analog demultiplexer, which commutates an analog signal to parallel connected sub-ADCs; sub-ADCs, and a digital multiplexer which combines the digital outputs from sub-ADCs. The digital MUX is very often not required in high-speed converters, because further digital processing would be done in parallel with lower speed. Analog DEMUX could be implemented using several parallel THA, which have shifted track/hold phases.

Any type of Nyquist ADC could be used as sub-converter, but SAR-ADC having inherently internal sample rate *n*-times higher than sample rate of whole converter, is best suited to be used in time-interleaved architecture.

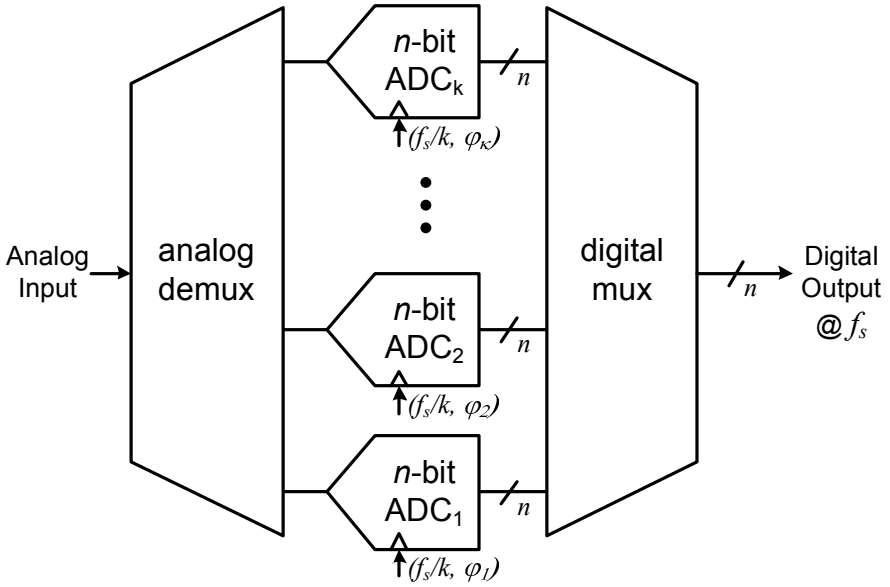


Fig. 3.8 Time-interleaved ADC.

3.1.6 Error compensation in ADCs

Describing all possible errors for all ADC architectures and their compensation techniques are not within the scope of this work. However several errors, which are mainly inherent in high-speed ADCs, will be described. Significant errors which occur during digitizing usually occur in the analog part of the converter. Unfortunately only limited number of possible errors can be compensated using additional techniques.

Errors could be divided in two groups. The first group refers to errors due to device mismatch. The second group refers to errors due to limited performance of the components, usually due to limited gain especially at high frequencies.

Each group will be considered separately. For the one step ADCs, such as full flash ADCs and folding-interpolated ADCs, the reference network (Fig. 3.10, page 64) is mostly affected by device mismatches. The voltage difference of the taps depends on the current of the buffer (I_{EF}), common for the series connected taps, and tap resistance (R). The whole dynamic range $V_{p\text{-}p}$, which is calculated by (3.1), can be calibrated by adjusting the current I_{EF}.

$$V_{p-p} = I_{EF} \cdot \mathrm{R} \cdot N \tag{3.1}$$

where N is a number of taps.

The voltage of separate tap could be adjusted only by changing the tap resistance. Since all resistors are serially connected, it is impossible to change current of the one resistor without changing current of the adjacent resistors in the line.

The resistor is a passive component and its value could be changed also passively. A well known industrial method is trimming. Geometry of the resistor is trimmed until the required resistance value is achieved. The disadvantage of this method is external postprocessing which has to be done after chip fabrication.

In contrary, errors due to the limited gain of the stages could be partly compensated electronically by an additional circuitry. But as the gain could not be infinite, the correction could not guarantee 100% error free results. And, of course, the additional correction by adding active circuitry costs an additional power and an area that is not desirable.

The comparator is a circuit which digitizes the analog signal. Problems of conversion related to the comparator are metastability and bubbles (sparkle codes). It results in limited gain of a preamplifier and comparator amplification stage. Metastability is generally unavoidable and will happen independently of how much gain comparator has.

A probability of the metastability error is calculated by [38]:

$$P_{error} = \frac{2V_{logic}}{A_p \cdot A \cdot V_{LSB}} e^{\frac{-(A-1)\cdot T}{RC}} \tag{3.2}$$

where:

V_{LSB} is the quantum size at comparator input in volts;

V_{logic} is the minimum valid logic level comparator must generate;

A is the comparator unlatched gain;

A_p is the preamplifier gain;

T is the maximum time period allowed for the comparator to make correct decision;

RC is the time constant of the comparator.

From (3.2), it is apparent that probability of the metastability errors is decreased with increasing the gain of preamplifier and comparator but never could be zero because the gain would never reach infinity. The gain of comparator is only one parameter which can be optimized to get better performance for given ADC configuration. Other parameters such as V_{LSB}, T are dependent on resolution and target speed of the converter and can not be adjusted.

The gain could be increased in two ways: increasing the number of the preamplifiers or using several latches in series. As shown in [39] it is impractical to use more than 3 amplification stages. If the desired probability of the metastability errors could not be simply achieved by increasing the gain, two or more stage comparators are connected in master-slave configuration.

3.1.7 Choice of A/D converter architecture

Table VII lists the state of the art of the high-speed ADCs and shows a predominance of the full flash architectures among high-speed ADCs in the low resolution region. The second candidate is the time-interleaved SAR-ADC. Despite the best results represented in [40] and in [41], it is less preferable because of the low target resolution (4 bits). The SAR-ADC implemented in modern technology could work at sample rate ~1-1.5 GS/s. Implementing 4-bit SAR-ADC, one would have a converter with 5-7.5 GS/s internal sampling rate, and connecting several (4 or 5) 4-bit converters in parallel would result in converter with sampling rate ~7.5 GS/s. It is possible to connect more ADCs in parallel and to achieve a higher sampling rate of 10 GS/s. But the clock signals of the separate ADCs are no more based on the internal clock.

The precise generation and control of such multi-clocks can be done with a delay locked loop (DLL). But the DLL contributes in the total power budget by increasing it. Without DLL the parameters of different clocks would vary due to technological mismatch and during operation with variation of the temperature. It may result in loss of information of the input signal. Moreover the distribution of the

separate clocks on long distances is quite challenging task which also requires an additional power.

Analyzing advantages and disadvantages of the above described architectures and targeting a 4-bit ADC, with more than 10 GS/s sample rate and effective resolution bandwidth more than 5 GHz, it can be concluded that full flash architecture is a best choice.

Table VII. State of the art of high-speed ADCs.

Sample Rate, GS/s	Resolution, bits	ENOB, bits	ERBW, GHz	Power, W	FoM, pJ	Technology	Type	Ref.
10	5	> 4.1		3.6	47	0.18 µm SiGe, BiCMOS	flash	[19]
8	4	4	4	0.5	3.9	SiGe	flash	[35]
40	3	2.8	20	3.8	13.6	0.12 µm SiGe	flash	[21]
20	8	4.6	6.6	9	28	0.18 µm, CMOS	inter. pipeline	[42]
22	5	3.5	7	3	19	0.13 µm SiGe, BiCMOS	flash	[36]
24	6	3.5	12	1.2	4.4	90 nm, CMOS	inter. SAR	[40]
20	3		4.2	2.36	8.5	0.12 µm SiGe	flash	[20]
56	8	6.4	15	2	0.8	65 nm, CMOS	inter. SAR	[41]

3.2 Implementation of 10 GS/s 4-bit ADC

3.2.1 Block-diagram of ADC

The block diagram of full flash ADC, which is implemented in this work, is shown in Fig. 3.9. For simplicity THA and reference network are shown differentially;

digital part is shown single-ended. In reality all blocks are differential including clock and test buffers.

The track-and-hold amplifier is placed in front of the converter. It relaxes requirements to the preamplifier and helps to achieve better sensitivity of the comparator. The design of the THA is already described in the previous chapter. The version of THA [34], which could work at 3 V supply voltage, was selected to be implemented in the converter. The THA described in [34] has lower bandwidth, which does not meet target of 5 GHz. THA, integrated in ADC, was redesigned to achieve bandwidth of 5 GHz and 5 bit resolution.

Design of the separate parts of the converters, such as reference network, comparator and encoder are described in the next paragraphs.

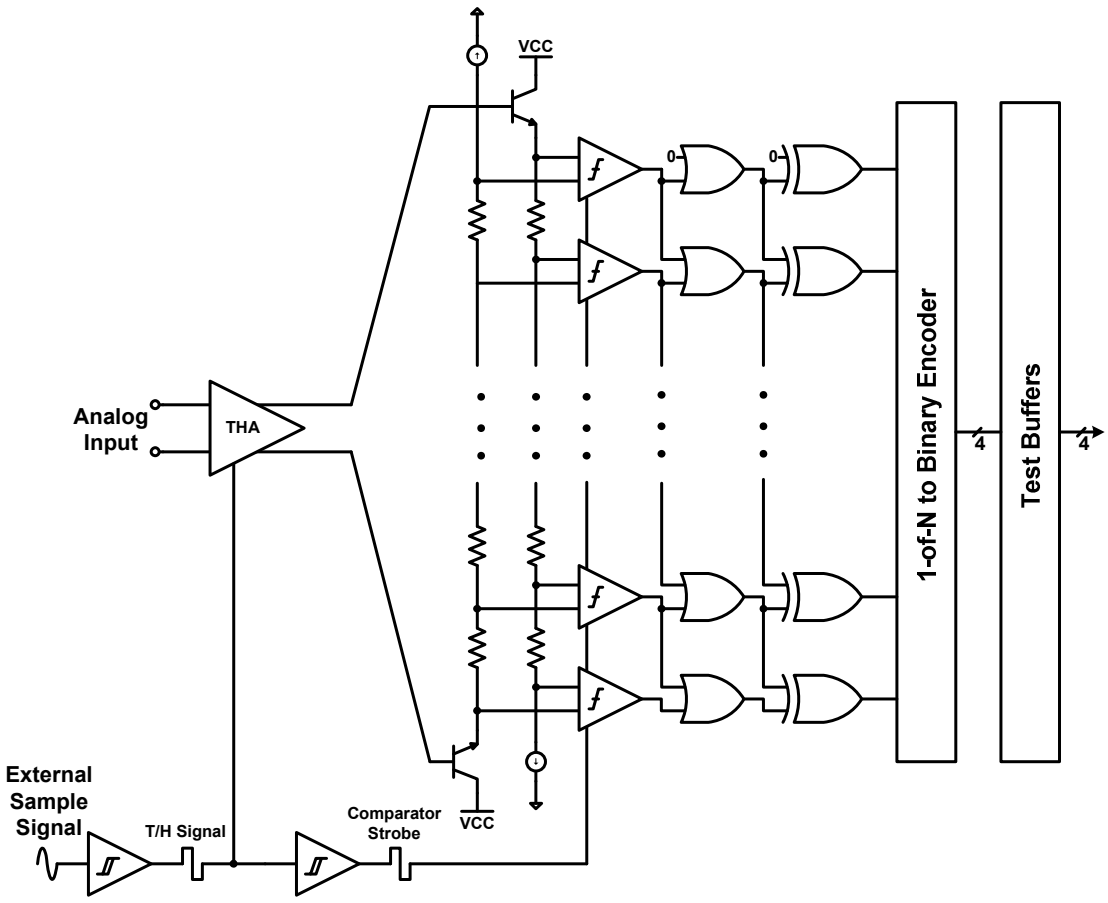


Fig. 3.9 Block diagram of the full flash ADC.

3.2.2 Reference network

A reference network, which follows the THA, provides equidistant reference signals that will be further processed by bank of comparators.

There are two conventional implementation of the reference network. First, the simplest way is a Kelvin divider or resistor ladder. The resistor ladder is connected between two reference sources: one source sets the maximal input value of the ADC, second sets the minimal value. Outputs of the divider are connected to the negative input of the comparators, positive input connected to the input signal.

The advantage such reference network is its high-speed; the input signal is compared with constant DC signal, and therefore performance is limited only by comparators. But this divider suffers from several drawbacks. First one is the dc-bowing. It occurs in the ADC with bipolar comparators due to non-zero base current. The base current of input stage changes quantization levels and leads to the errors. To compensate it, an additional current should be injected into resistor ladder or resistor values should be adjusted accordingly.

Second drawback of this network is the feedthrough from analog input of the comparator to resistor ladder. Some portion of analog input comes from the input of comparator through parasitic capacitors to the resistor ladder and adds some alternating components. This error is proportional to the square of the number of comparators [43]. At high frequencies if the number of comparator is large, the feedthrough could be significant.

The third disadvantage is the clock feedthrough. Impact of the clock feedthrough is proportional to the output impedance difference between reference network and preceding ADC circuit [44]. This impact could by expressed as a dynamic offset [44]:

$$V_{doffset} = I_b \cdot \left[\frac{1}{\frac{1}{R_c} + \frac{1}{R_{in}}\left(1 + \frac{C_s}{C_\mu}\right)} - \frac{1}{\frac{1}{R_c} + \frac{1}{R_{ref}}\left(1 + \frac{C_s}{C_\mu}\right)} \right] \tag{3.3}$$

where:

R_{in} is the output impedance of the preceding circuit (input source);

R_{ref} is the output impedance of the reference network;

R_c is the load of the preamplifier;

C_s is the collector-substrate capacitance;

C_μ is the collector-base capacitance.

The output impedances of the resistor ladder and input source are usually not equal; therefore the dynamic offset is not zero.

A second conventional configuration of the reference network is a differential configuration. The differential reference network is depicted on block diagram in Fig. 3.9 and separately shown in Fig. 3.10. It consists of two branches; each has a driver, which is loaded with a chain of serially connected tap resistors. In this example the driver is emitter follower with resistors in the emitter. Both branches are equal, only outputs of negative branch are “inverted” or mirrored with respect to the middle point.

The reference network produces a set of signals whose shape is equal to the shape of the input signal and DC-level of those signals are shifted by 1 LSB. A systematic generation of the reference signals is illustrated in Fig. 3.11. The set of reference signals is going to the bank of comparators as depicted in Fig. 3.9.

The differential network does not suffer from dc-bowing, because the sum of currents that flow from each differential output node is constant. The feedthrough is also compensated by using differential input.

But the bandwidth becomes a bottleneck. The reference network has to drive a big capacitive load caused by the bank of comparators. In the full flash ADC it is one of the main problems, because the number of comparators is doubled by increasing of the resolution by 1 bit.

The second problem of such network is non-equal transfer characteristic of the output nodes.

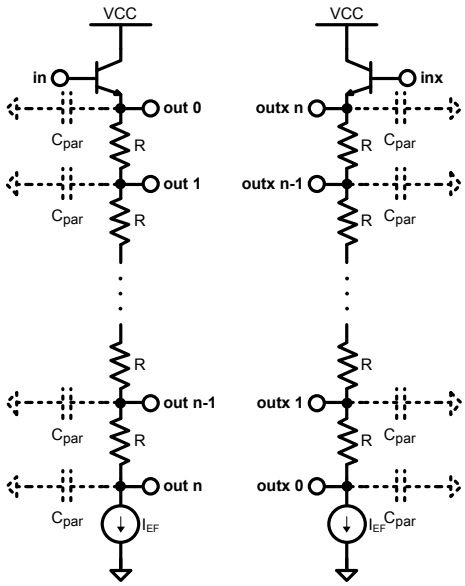


Fig. 3.10 Differential reference network.

The half-network in Fig. 3.10 is a distributed *RC* line. For the uniform distributed lossless *RC* line the voltage in any point *V(x,t)* can be found by solving second-order differential equation [45]:

$$rc \cdot \frac{\partial V(x,t)}{\partial t} = \frac{\partial^2 V(x,t)}{\partial x^2} \tag{3.4}$$

where:

r is a unit resistance,

c is a unit capacitance.

Use Laplace transform the (3.4) is written as:

$$\frac{\partial^2 V(x,s)}{\partial x^2} - srcV(x,s) = 0 \tag{3.5}$$

The general solution is:

$$V(x,s) = A_1 \sinh\left(x\sqrt{src}\right) + B_1 \cosh\left(x\sqrt{src}\right) \tag{3.6}$$

where A_1 and B_1 coefficients that can be found using the boundary conditions.

The analytical solution in time domain is quite complicated. For the qualitative estimation of the bandwidth, the half-network would be considered as series of independent *RC*-chains.

The transfer function in node *out 1* is:

$$\frac{V_{out1}}{V_{in}} = \frac{1}{1 + j\omega RC_{par}} \tag{3.7}$$

where C_{par} is a total parasitic capacitance in node *out 1*. The parasitic resistances of the network were neglected. For any node *out k* the transfer function is calculated by:

$$\frac{V_{out\,k}}{V_{in}} = \frac{1}{\left(1 + j\omega RC_{par}\right)^{k}} \tag{3.8}$$

Equation (3.8) shows that output nodes have different transfer functions. Solving it, a break (cutoff) frequency for different outputs can be calculated. The plot of normalized break frequency (*RC=1*) versus output number is shown in Fig. 3.12.

Furthermore, since the power *k* for extreme nodes in formula (3.8) is equal to the number of comparators in ADC, and the number of comparators is dependent on the resolution of the converter, the bandwidth of the reference network is also dependent on the converter resolution.

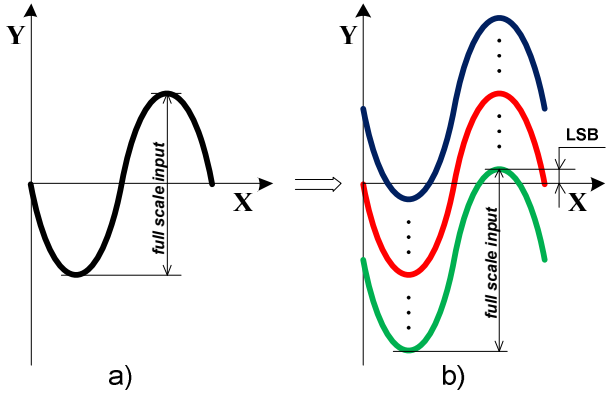


Fig. 3.11 Function of reference network: a) Input signal at the input of reference network, b) Set of signals shifted in 1 LSB at the output of reference network.

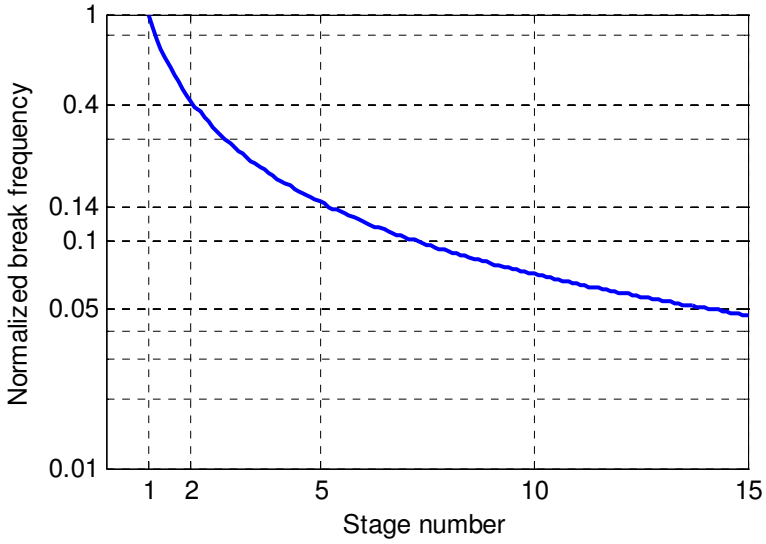


Fig. 3.12 Normalized break frequencies for different output nodes of reference network.

Maximization of the network bandwidth can be achieved by minimizing values R and C_{par}. Parasitic capacitance C_{par} is a sum of input capacitance of the comparator C_{in} and parasitic capacitance of the resistor C_R

$$C_{par} = C_{in} + C_R \tag{3.9}$$

The input capacitance of comparator is mostly defined by technology and can not be changed, especially if min-size transistors are used.

The parasitic capacitance of the resistor is proportional to the geometrical size. The value C_R can be changed, but the $R \cdot C_R$ constant will not change for the constant voltage drop on resistor.

3.2.3 Proposed bandwidth enhancement technique

Drawbacks of conventional differential reference network are mainly because of its serial configuration, changes in one component affect the others. This inherent property of the serial connection makes individual adjustments and compensations impossible.

To overcome that limitation a new configuration is proposed. The idea is to build the resistor network in segmented serial-parallel configuration and substitute one driver (emitter follower) with several drivers, connected in parallel. The whole set of resistors is grouped in *l* segments, each segment contains *m* resistors.

$$l \cdot m \geq n \tag{3.10}$$

A general segmentation of resistors is shown in Fig. 3.13. For the sake of better understanding all current sources and all resistors, except first resistor in the segment, have the same value.

The main condition to be satisfied in the network is to keep the voltage step between adjacent outputs equal to 1 LSB. This condition is actually to be met for the conventional network also. This can be easily reached by scaling the value of the first resistor in the segment. The value of the first resistor is calculated by:

$$R_{1,i} = \left[\left(k-1 \right) \cdot m + 1 \right] \cdot R \tag{3.11}$$

where *k* is a segment number, *m* is a number of resistors in the segment, *R* is a unity resistance. All other resistors have value *R*.

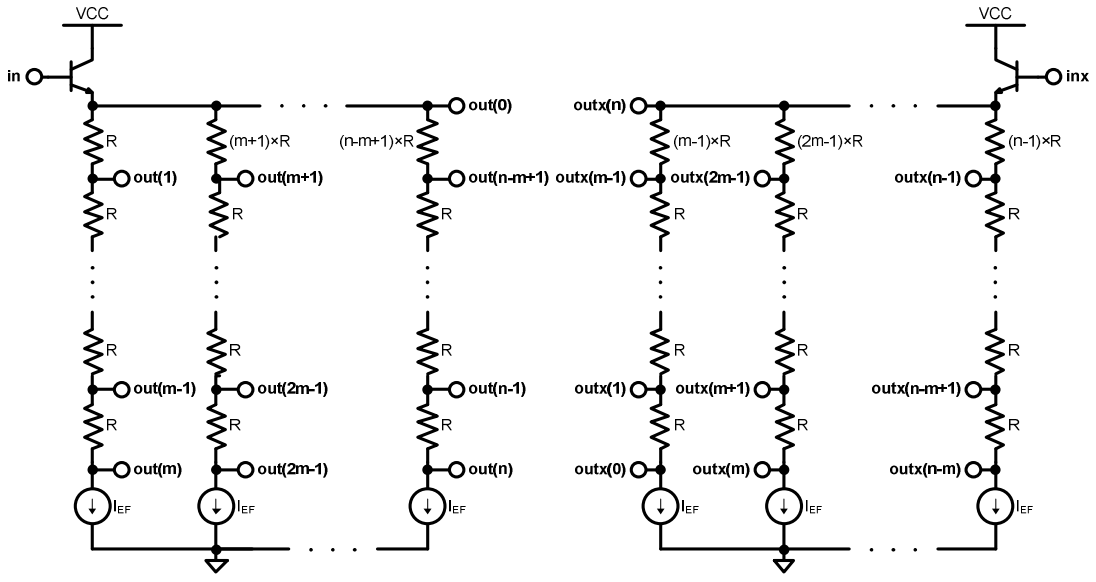


Fig. 3.13 Proposed segmented differential reference network (general case).

A big advantage of proposed reference network is its flexibility. Variety of configurations is more thoroughly described in [46]. For this work, two extreme cases are interesting:

- First case, if network consists of only one segment, then the proposed network is identical to conventional network (Fig. 3.10).
- Second case, if segments contain only one resistor then the network is full parallel. Fig. 3.14 illustrates this configuration.

For the practical implementation targeting max bandwidth, the full parallel network is most interesting.

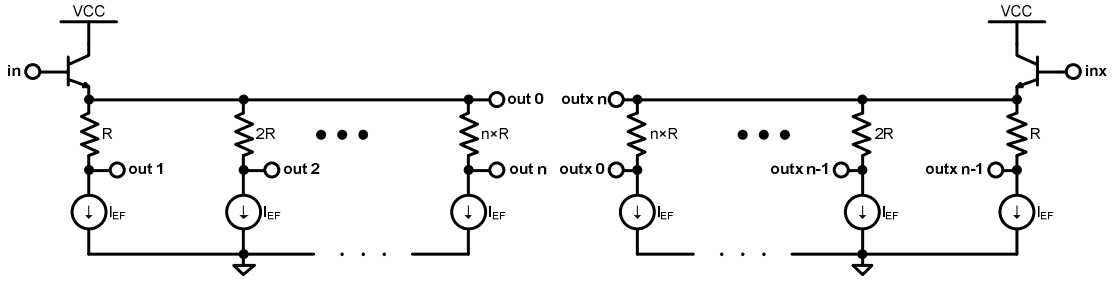


Fig. 3.14 Most practical configuration of the network with one resistor in the segment.

The transfer function for the parallel network in node *k* is:

$$\frac{V'_{out\,k}}{V_{in}} = \frac{1}{1 + j\omega \cdot k \cdot R \cdot C'_{par}} \tag{3.12}$$

Comparing with (3.8), the bandwidth is inversely proportional to the node number instead of power of node number as in (3.8).

The parasitic capacitance C'_{par} is the sum of the input capacitance of comparator C_{in} and the parasitic capacitance of resistor C'_R

$$C'_{par} = C_{in} + C'_R \tag{3.13}$$

The value C'_R is proportional to the resistor width. The resistor width should be enough to conduct a current without overheating of the component. The parallel network has *n* parallel drivers; therefore the current of each driver is *n* times lower than

current of driver in the serial network. Therefore the value C_R' is n times lower than the value C_R:

$$C_R' = \frac{C_R}{n} \tag{3.14}$$

Another feature of the segmented network is the flexibility of choosing component values. The maximum flexibility is also achieved for the parallel case. Freezing the voltage step to 1 LSB, all other parameters, such as resistor values and driver currents, can be adjusted independently. Fig. 3.14 shows the case when all driver currents are equal. In practice it is more useful not to keep the currents in all segments equal, but equalize a bandwidth in each node. It can be done by redistributing the current from branches which has higher bandwidth to the branches with lower bandwidth. With this approach, the optimum power dissipation and highest bandwidth for given power is achieved. Possibility of independent adjustment of each segment is another big advantage of proposed network.

The configuration of the reference network with max segmentation (Fig. 3.14) enables good possibilities for electronic calibration of the voltage shift in individual segments. The calibration of separate components of the conventional network is limited due to its serial configuration. In the case depicted in Fig. 3.14 the voltage drop in all taps can be easily calibrated adding additional current source in parallel to the main current sources. Fig. 3.15 shows possible connection of additional current sources I_1.

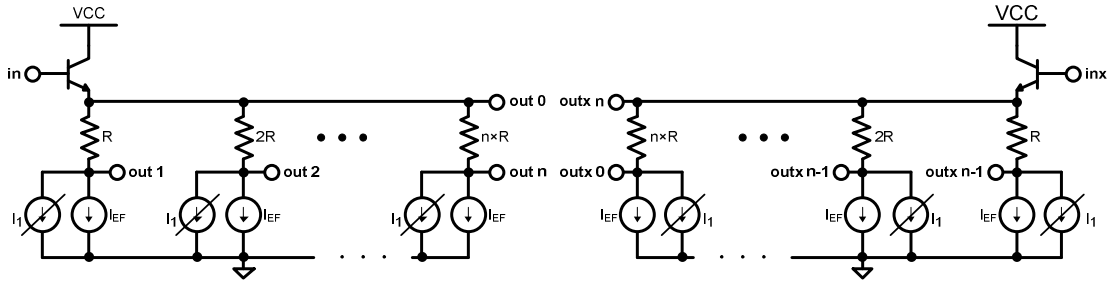


Fig. 3.15 Possible calibration scheme of the parallel network.

Along with advantages, the new network has some drawbacks. Flexibility of adjusting different parameters requires a different geometry for different resistors. In case of conventional network all resistors have the same value and the same geometry. Proper layout minimizes mismatches between them. The proposed network can not benefit from this feature. The matching of the components relies only on technological tolerances.

The LSB voltage could be expressed as:

$$V_{LSB} = \left(R + \Delta R + R_{par}\right) \cdot \left(I + \Delta I\right) \tag{3.15}$$

where ΔR is the manufacturing error of resistor R, R_{par} is the parasitic resistance, and ΔI is the manufacturing error of current source I. In well matched conventional serial network the terms ΔR and ΔI are constant, because all resistors have the same direction and geometry. A differential nonlinearity, which is the difference of voltage steps from the mean value, is:

$$DNL_{serial} = V_{LSB} - \overline{V}_{LSB} = R_{par} \cdot \left(I + \Delta I\right) \tag{3.16}$$

In the full parallel network terms ΔR and ΔI are random values for the different segments. And the differential nonlinearity is:

$$DNL_{parallel} = R_{par} \cdot \left(I + \Delta I\right) + \Delta I \cdot R + \Delta R \cdot \left(I + \Delta I\right) \tag{3.17}$$

Neglecting second order error $\Delta R \cdot \Delta I$, the equation (3.17) could be simplified to:

$$DNL_{parallel} \approx R_{par} \cdot \left(I + \Delta I\right) + \Delta I \cdot R + \Delta R \cdot I \tag{3.18}$$

The effect of random errors on the transfer curve is similar to the effect of quantization noise on the transfer curve of the A/D converter; the noise power representing the random errors can be added to the error power caused by quantization [47] and can be formulated as:

$$\mathrm{SNR}_{Q+error} = 10 \lg \left(\frac{2^{2n-3}}{\frac{1}{12} + \sigma^2} \right) \tag{3.19}$$

where σ is the standard deviation of the random errors. For an A/D converter this is equal to the standard deviation of the integral nonlinearity (INL) of each individual code. Subtracting the quantization noise from equation (3.19) results in the reduction of SNR caused by INL errors:

$$\mathrm{SNR}_{INL} = 10\lg\left(\frac{1}{1+12\cdot\sigma^2}\right) \tag{3.20}$$

When these *INL* errors are random errors with a Gaussian distribution, the relation between σ of the errors and the maximum *INL* is given by:

$$\sigma^2 = \frac{INL^2}{\alpha^2} \tag{3.21}$$

where α is the threshold value of the probability that the maximum random error remains within the acceptable ±*INL* limits. Combining (3.20) and (3.21) will result in the reduction of SNR caused by random Gaussian distributed INL errors:

$$\mathrm{SNR}_{INL} = -10\lg\left(1+12\cdot\frac{INL^2}{\alpha^2}\right) \tag{3.22}$$

Fig. 3.16 shows reduction of SNR versus value of *INL* for different α. A typical value of α is 3..5. The worst case, $\alpha=1$, occurs when *INL* changing is maximal from code to code.

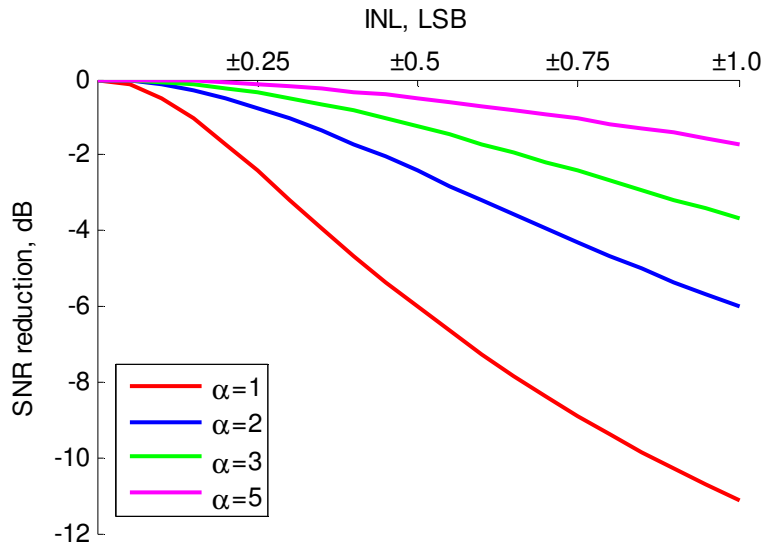


Fig. 3.16 Effect of INL on reduction of SNR.

3.2.4 Design of comparator

3.2.4.1 General performance considerations

Signals from the reference network are input to a bank of *n* comparators. Comparators decide if the differential input is above or below zero.

Generally a comparator works in two phases: track (or sample) phase, where the input signal is tracked and amplified; latch (or hold) phase, where the tracked signal is regeneratively amplified and held until next track phase. Fig. 3.17 illustrates differential latch outputs during track and hold phases. A simplest version of comparator could be realized with one latch.

The speed of the latch is determined by two factors: recovery time (t_{rec}) during track mode and regeneration time (t_{reg}) during hold mode (Fig. 3.17). Recovery time is the time to change output of the latch from saturated (digital) state to middle point. Regeneration time is the time which the latch needs to achieve the output swing.

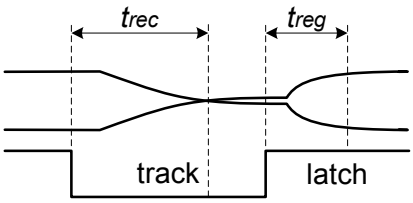


Fig. 3.17 Differential outputs of the latch during track/hold phases.

To calculate recovery time the latch in track mode is to be considered as a differential amplifier which amplifies signal from previous stage. Collector currents I_{C1} and I_{C2} of differential pair are [48]:

$$I_{C1} = \frac{\alpha_F I_{EE}}{1+\exp\left(-V_{in}/V_T\right)} \tag{3.23}$$

$$I_{C2} = \frac{\alpha_F I_{EE}}{1+\exp\left(V_{in}/V_T\right)} \tag{3.24}$$

$$I_{C2} = I_{C1} + \alpha_F I_{EE} \cdot \tanh\left(-V_{in}/2V_T\right) \tag{3.25}$$

For time $t \geq 0$ the output voltages are [49]:

$$V_{o1} = VCC - \alpha_F I_{EE} R_L - \left(I_{C1} R_L - \alpha_F I_{EE} R_L\right) \cdot \left[1 - \exp\left(-\frac{t}{R_L C_\Sigma}\right)\right] \tag{3.26}$$

$$V_{o2} = VCC - I_{C2} R_L \cdot \left[1 - \exp\left(-\frac{t}{R_L C_\Sigma}\right)\right] \tag{3.27}$$

where R_L is the load resistance of differential pair, I_{EE} is the tail current and C_Σ is the total parasitic capacitance in output node. Recovery time is the time needed for output to reach from V_{o1} to V_{o2}. By equating (3.26) to (3.27) and solving for current, the recovery time can be found.

With (3.25) to substitute I_{C2}

$$VCC-\alpha_F I_{EE} R_L-\left(I_{C1}R_L-\alpha_F I_{EE}R_L\right)\cdot\left[1-\exp\left(-\frac{t}{R_L C_\Sigma}\right)\right]= \\ VCC-\left[I_{C1}R_L-\alpha_F I_{EE}R_L\tanh\left(-V_{in}/2V_T\right)\right]\cdot\left[1-\exp\left(-\frac{t}{R_L C_\Sigma}\right)\right] \tag{3.28}$$

and further simplification:

$$-\alpha_F I_{EE}R_L+\alpha_F I_{EE}R_L\cdot\left[1-\exp\left(-\frac{t}{R_L C_\Sigma}\right)\right]= \\ \alpha_F I_{EE}R_L\cdot\tanh\left(-V_{in}/2V_T\right)\cdot\left[1-\exp\left(-\frac{t}{R_L C_\Sigma}\right)\right] \tag{3.29}$$

$$-\exp\left(-\frac{t}{R_L C_\Sigma}\right)=\tanh\left(-V_{in}/2V_T\right)\cdot\left[1-\exp\left(-\frac{t}{R_L C_\Sigma}\right)\right] \tag{3.30}$$

the recovery time is:

$$t_{rec}=R_L C_\Sigma\cdot\ln\left(1+\frac{1}{\tanh\left(V_{in}/2V_T\right)}\right) \tag{3.31}$$

From (3.31), it is apparent that recovery time is dependent on load resistors and parasitic capacitance.

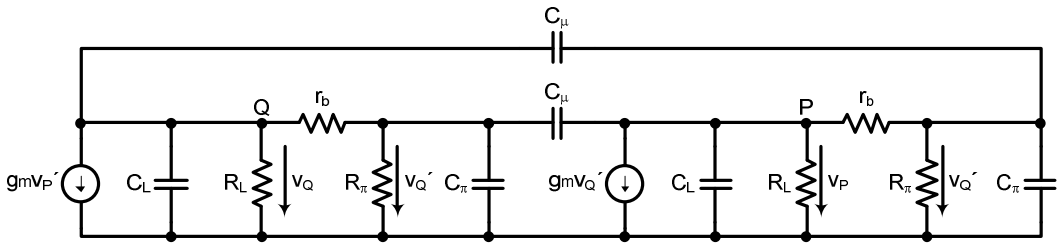


Fig. 3.18 Small-signal equivalent of the latch.

For calculation of the regeneration time a small-signal equivalent of the latch (Fig. 3.18) can be used. The characteristic equation in *s*-domain is [49]:

$$s^2 r_b \left(C_L C_\mu + C_\pi C_\mu + C_L C_\pi \right) + \\ + s \left[C_\pi \left(1 + \frac{r_b}{R_L} - g_m r_b \right) + C_\mu \left(4 + \frac{r_b}{R_L} - g_m r \right) + C_L \right] - \\ - \left(g_m - \frac{1}{R_L} - \frac{1}{r_\pi} \right) = 0 \tag{3.32}$$

An approximate solution for regeneration response is:

$$V_{od} = A_L V_{in} \exp\left(t / \tau_{reg} \right) \tag{3.33}$$

with a regeneration time constant:

$$\tau_{reg} = \frac{C_\pi \left(r_b + R_L \right) + C_\mu \left[4R_L + r_b \left(g_m R_L + 1 \right) \right] + C_L R_L}{g_m R_L - 1} \tag{3.34}$$

when $R_L \gg r_b$ the regeneration constant could be reduced to

$$\tau_{reg} = \frac{C_\Sigma}{g_m} \left(\frac{g_m R_L}{g_m R_L - 1} \right) \tag{3.35}$$

where $C_\Sigma = C_\pi + C_L + 4C_\mu$.

From (3.33) it is apparent that the regeneration time is dependent on the input signal. The input signal can take any value from zero to max. It is evident that for the input signals in vicinity of zero the output would not reach its saturation values and stay somewhere in between. This is called a metastable state. Dividing the output voltage V_{od} to the input voltage V_{in} an effective gain during regeneration phase can be obtained:

$$A_{ef} = A_L \exp\left(t / \tau_{reg} \right) \tag{3.36}$$

A single latch stage can seldom provide the desired error-free functionality. By adding a preamplifier in front of the comparator the effective gain is increased by A_{pre} times, where A_{pre} is the gain of preamplifier. From (3.2) it can be seen that the probability of occurrence of metastable state is inversely proportional to the effective gain. For further decreasing the probability of metastability errors a second slave latch is used. Then the effective gain becomes:

$$A_{ef2} = A_{pre} \cdot A_{L1} \cdot \exp\left(t / \tau_{reg1} \right) \cdot A_{L2} \cdot \exp\left(t / \tau_{reg2} \right) \tag{3.37}$$

3.2.4.2 Preamplifier

The role of the preamplifier for the comparator is twofold: it works as a limiting amplifier and it provides an additional amplification of the input signal. Another important function of the preamplifier is isolating the reference network from kick-back noise, produced by the latch.

The reference signals are spread in the range of $-V_{p-p}+1LSB$ to $V_{p-p}-1LSB$ with 1 LSB step (Fig. 3.19a,b). The worst case for the latch occurs when the input signal changes from full scale to *1 LSB*. This is called overdrive condition and is the most stressful condition for the latch to recognize the transition. To achieve the best performance the signal before the latch should be limited and amplified. Ideal outputs after preamplifiers, which are input to latches, have a steep slope and are depicted in Fig. 3.19c in bold.

For the preamplifier often a differential pair is used. It provides the desired gain with high bandwidth. The isolating properties are also good. An emitter follower which is sometimes used at the end of the amplifying stage would equalize output impedance and minimize dynamic offset of comparator [44]. The only weak point of the differential pair is its limiting capabilities.

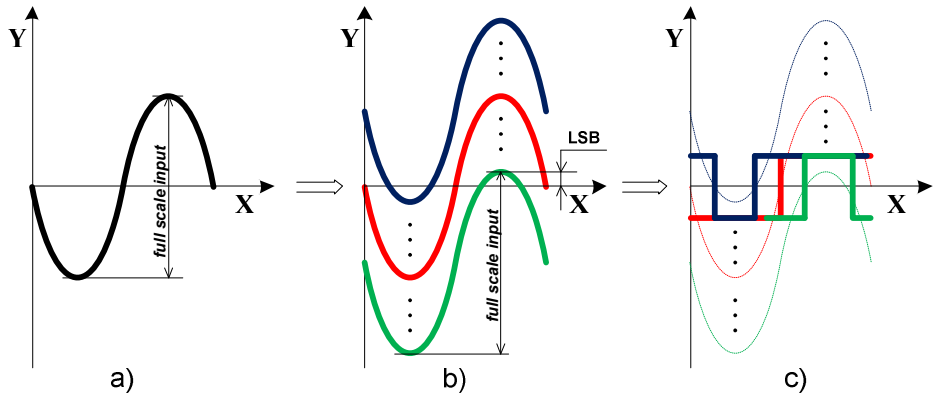


Fig. 3.19 Signal's path through reference network and preamplifier: a) Input signal. b) Output of reference network, signals shifted in 1 LSB. c) Ideal outputs of preamplifiers (in bold).

Another solution is the Cherry-Hooper Amplifier with Emitter Follower Feedback (CHEF). It is widely used in optical circuits. A schematic of the Cherry-Hooper amplifier with EF feedback is depicted in Fig. 3.20.

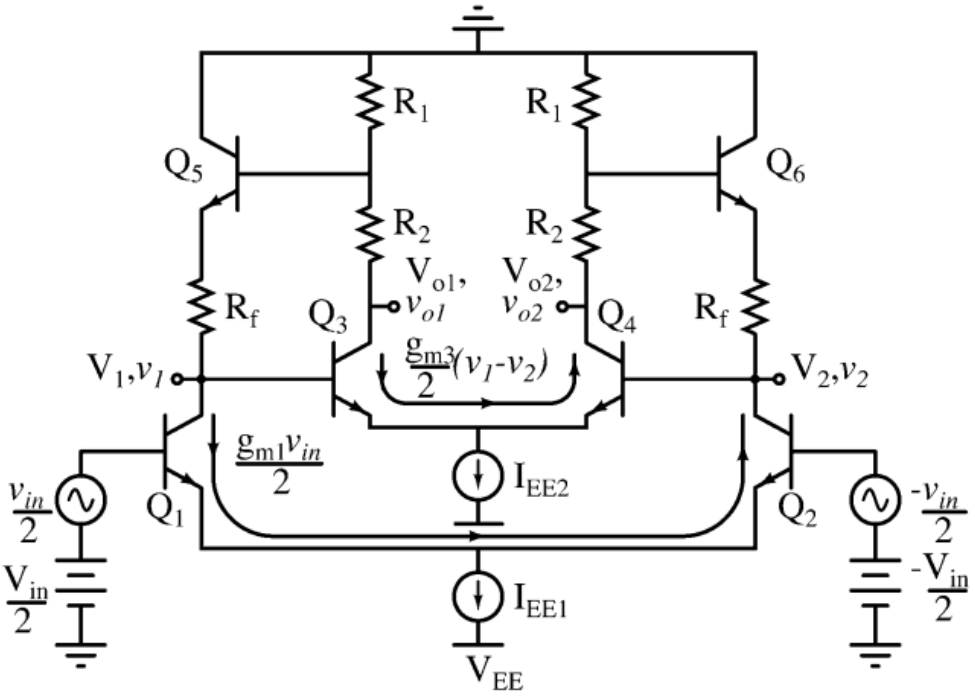


Fig. 3.20 Cherry-Hooper amplifier with emitter-follower feedback.

The output voltage of the CHEF could be calculated by [50]:

$$V_{o1} - V_{o2} \cong \left(R_1 + R_2\right) I_{EE2} \cdot \tanh\left(\frac{V_2 - V_1}{2V_T}\right) \tag{3.38}$$

where:

$$
\begin{aligned}
V_1 - V_2 \cong\ & R_1 I_{EE2} \cdot \tanh\left(\frac{v_2 - v_1}{2V_T}\right) \\
& + R_f I_{EE1} \cdot \tanh\left(\frac{-V_{in}}{2V_T}\right) \\
& + V_T \cdot \ln\left(\frac{I_{EE1}}{1+e^{V_{in}/V_T}} + \frac{I_{EE2}}{\beta_{DC}\left(1+e^{(v_1-v_2)/V_T}\right)}\right) \\
& - V_T \cdot \ln\left(\frac{I_{EE1}}{1+e^{-V_{in}/V_T}} + \frac{I_{EE2}}{\beta_{DC}\left(1+e^{(v_2-v_1)/V_T}\right)}\right)
\end{aligned}
\tag{3.39}
$$

Simulation results for small signal gain and bandwidth of the CHEF preamplifier and latch are shown in Fig. 3.21. Both analytical expression of gain (3.38) and simulation results in Fig. 3.21 are not applicable for the large-signal overdriven input.

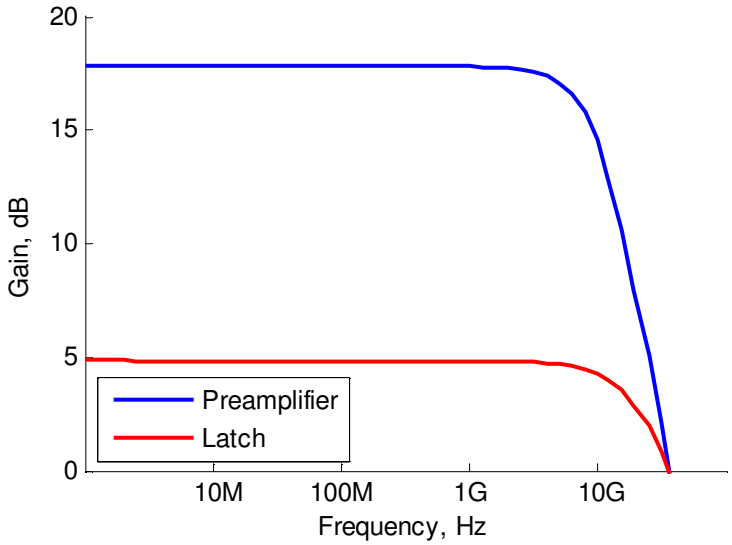


Fig. 3.21 Bandwidths of preamplifier and latch.

The large-signal sensitivity of the whole comparator was simulated at high frequency instead of the small-signal gain. The results are given in Fig. 3.22. In this case the sensitivity is defined as the minimum input voltage V_{min}, for the case that input changes from $V_{p\text{-}p}$ to $-V_{min}$, at which digital switching of the comparator takes place. Fig. 3.22 shows the input sensitivity from 5 GHz to 10 GHz. The sensitivity is rapidly

degraded with frequency and starting from 6 GHz is worse than 0.5 LSB In the range of 5 GHz the comparator works well.

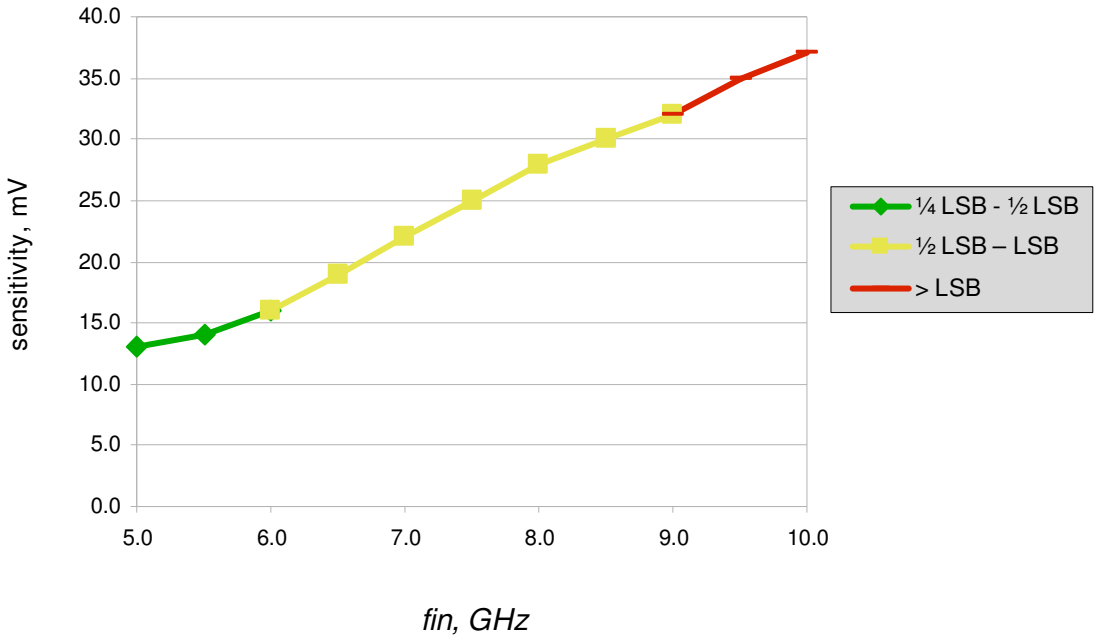


Fig. 3.22 Sensitivity of comparator under overdriven condition.

3.2.4.3 Latch

Some general considerations about speed of the latch is given above. They are valid for any implementation.

In high-speed range there are two well-known implementations of bipolar latches: conventional low-clocking and high-clocking latch. The high-clocking latch, depicted in Fig. 3.23, has advantage of a reduced kick-back noise. The input differential pair is not switched on/off and kick-back noise is added during switching cascade transistors *Q5-Q6*. But adding cascade device require additional voltage headroom, what is not preferable for keeping power dissipation low. Cheery-Hooper preamplifier performs good isolation of the latch from the reference network. Therefore the conventional low-clocking latch was implemented.

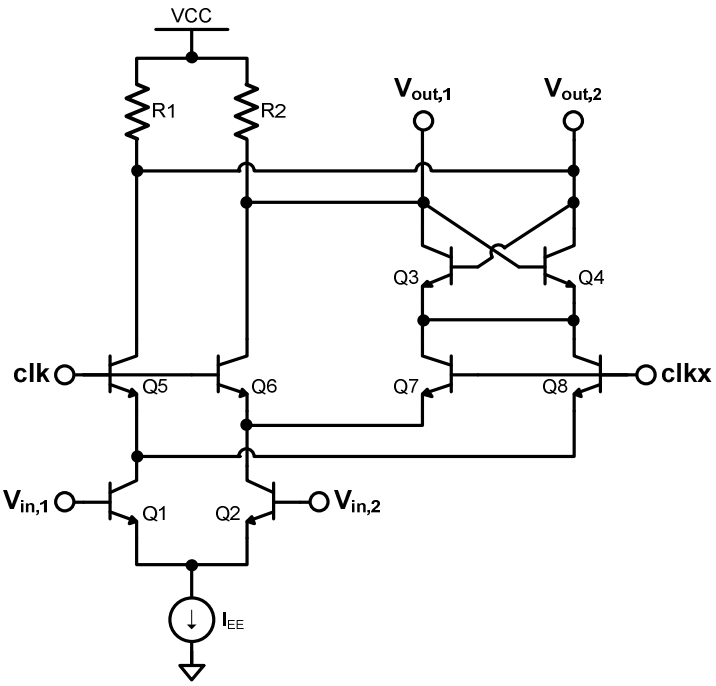


Fig. 3.23 High-clocking latch.

A whole master-slave comparator with preamplifier is shown in Fig. 3.24. A master latch has auxiliary current source I_{aux}. This current source prevents the cross-coupled differential pair from being completely switched off and so keeps the base-emitter capacitance charged. The time to charge this capacitance is decreased and as a result the overall speed of the latch is increased. The I_{aux} has to be sufficiently small because it adds hysteresis which decreases sensitivity. Setting value of I_{aux} equal to 10 % of I_{EE2} is a good compromise between speed and sensitivity. In the slave latch there is no auxiliary current source because input signal of slave latch has relatively big amplitude and auxiliary current source does not have strong influence as in the case of the master latch.

In order to save power some possible improvements, such as emitter follower at the output, were omitted [43].

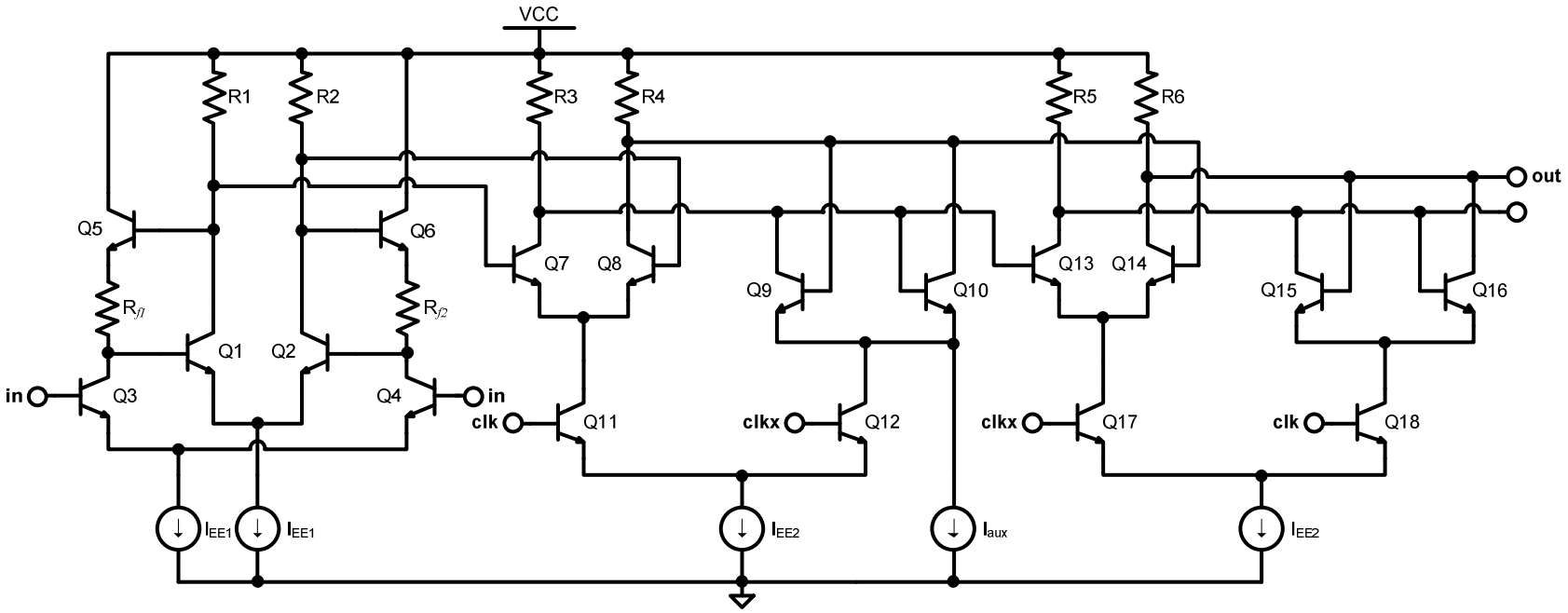


Fig. 3.24 Master-slave comparator, full schematic.

3.2.5 Encoder

Thermometer code produced by comparators is input to the encoding circuitry (encoder). The encoder is logically divided in two parts: a correction logic and a thermometer-to-binary encoder. The correction logic serves to detect and correct errors in the thermometer code. It consists of a set of correction cells, which analyze comparator outputs. There are many different implementations of correction cells. Most known are voting cell (Fig. 3.25a), and, a more complicated one, pseudo-majority cell (Fig. 3.25b). An AND-gate can be also used for the simplest implementation of correction.

The ability to correct errors is directly proportional to the number of analyzed outputs and hence to the complexity of the cells. At high frequencies sophisticated cells dissipate huge amount of power and often can not satisfy speed requirements due to latency of the gates. Therefore a simple AND-gate was used in this design. States of two adjacent comparators are analyzed and only one erroneous output ("bubble") can be corrected. Two adjacent 'bubble' will cause an error in the binary output code.

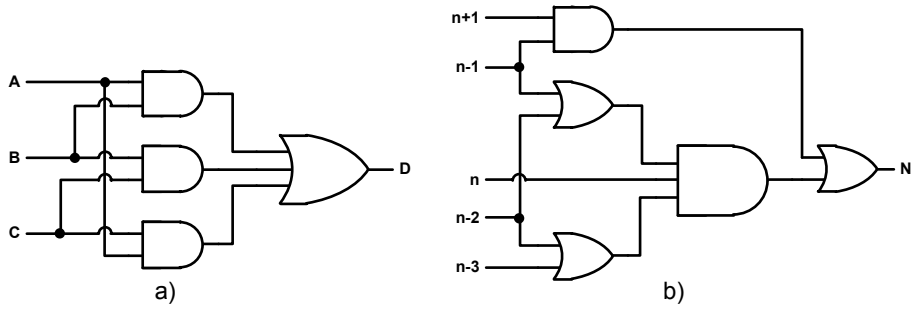


Fig. 3.25 a) Voting cell, b) Pseudo-Majority gate circuit.

Together with bubble correction, codes which are more error-stable than binary code, can be used. Most of them are based on modification of Gray code. This modification is usually done in the direction to simplify encoding, which causes loosing error reduction property. For example Quasi-Gray code can be converted into binary with a lower delay but it has higher maximum position error and higher mean position error [51] or as in [51], half-gray encoder has lower maximum and mean errors but

more complicated coding/encoding scheme. The big disadvantage of Gray and modified Gray codes is the difficulty to perform arithmetic operation on it. Commonly the codes are converted into binary code for processing. For systems, which have limited processing capabilities, real-time conversion into binary code might be impossible. One of the examples of such system is the oscilloscope, which was planned to be used for the measurement of the ADC. To preserve possibility of testing ADC outputs with oscilloscope, the binary code was used in this design.

Encoding into binary code is done with a ROM look-up table. Address is applied to the input of ROM table. According to the address the appropriate code from the table is read and written to the output. The address is coded with a position code which is obtained from the thermometer code by XOR operation of adjacent stages.

The ROM table is implemented using wired-OR technique. This technique needs much less power but it does not support differential mode. Internal logical operations in the ROM are done in single-ended mode. Fig. 3.26 shows configuration of the portion of the ROM table responsible for selecting less significant bit.

The configuration of the ROM table allows to find both positive and inverse value of the bits independently. For instance; left odd switches *(XOR 1 ... XOR 2^n-1)* in Fig. 3.26 are used to obtain the positive value of LSB, right even switches *(XOR 2 ... XOR 2^n)* are used to obtain the inverse value of LSB. This feature is used to build differential output from two single-ended (positive and inverse).

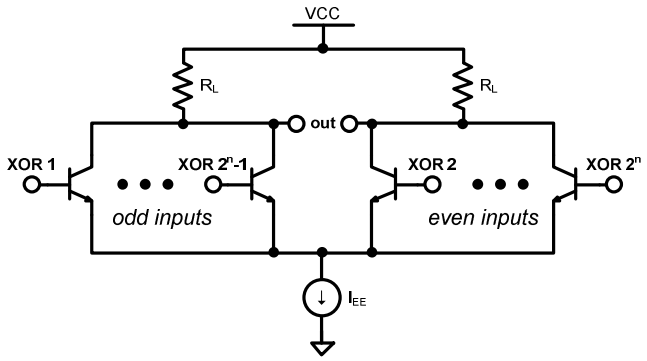


Fig. 3.26 Configuration of wired-OR gate for conversion 1-of-N code to LSB.

3.2.6 Layout

Random and graded process parameter variations cause severe nonlinearities in the static output characteristics of the ADC. A proper layout can relax impact of graded errors. The technique which makes the circuit robust to graded mismatches is called the common centroid technique. Critical components are split into several sub-components and those sub-components are placed around common symmetry axis. But this technique has some limitations. When min-size transistors are used for speed and power purposes, the bipolar devices are impossible to split into several parts.

Because the common centroid layout can not be implemented for the ADC, the main attention was paid to keep propagation paths nearly the same for positive and inverse signals. It is achieved by making the layout of differential stages symmetrical according to their symmetry lines. This is illustrated in Fig. 3.27, where a layout of the comparator (Fig. 3.24) without preamplifier is shown. Three symmetry lines for the master part of the comparator are shown with red dash-dotted lines. The differential pairs are located around those lines. Unwanted components such as parasitic degenerating resistors and parasitic capacitors are the same for the positive and inverse half-circuits.

Adjacent stages are placed on the same position in Y-direction with minimum allowed distance in X-direction. Thereby stage interconnections are shortest and have the same length.

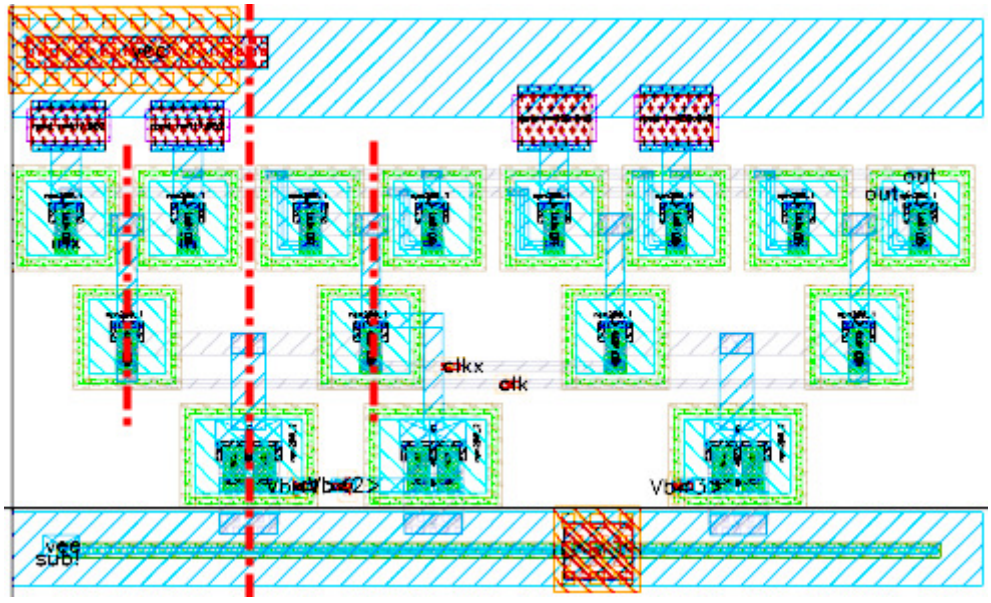


Fig. 3.27 Layout of comparator (without preamplifier)

3.2.7 Experimental results of ADC

Two versions of 4-bit analog-to-digital converters were implemented and tested. First A/D converter (ADC1) is in full correspondence with the block-diagram depicted in Fig. 3.9. It has THA and uses conventional one segmented reference network. Second A/D converter (ADC2) has new parallel reference network; the THA was omitted; other blocks are the same as in ADC1. It is almost ideal condition to prove advantages and disadvantages of proposed improvements.

Chip micrographs of both ADCs are depicted in Fig. 3.28. A standard pad frame with 6 RF probes at east, south, and west and 13x DC probe at north was used for the measurement. The size of each chip, defined by the pad frame, is equal to 1.5x1.5 mm^2. The active area is much smaller and is 500x700 μm^2 for ADC1 and 400x700 μm^2 for ADC2. Comparison between active areas of converters shows that new reference network occupies smaller area.

Chips were characterized with help of 20 GS/s 4 channels Tektroniks real-time oscilloscopes. The oscilloscope was used as capturing device. Because of lack of high-

speed logic analyzer it was used for both low-speed measurements and high-speed measurements. The captured data were read and analyzed with MatLab.

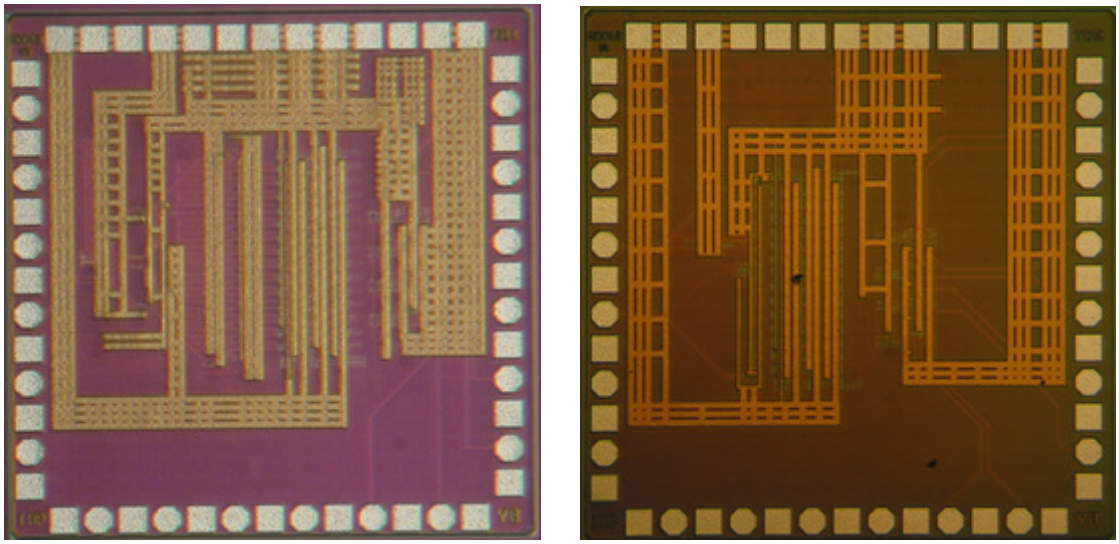


Fig. 3.28 ADC1 and ADC 2 chip micrographs.

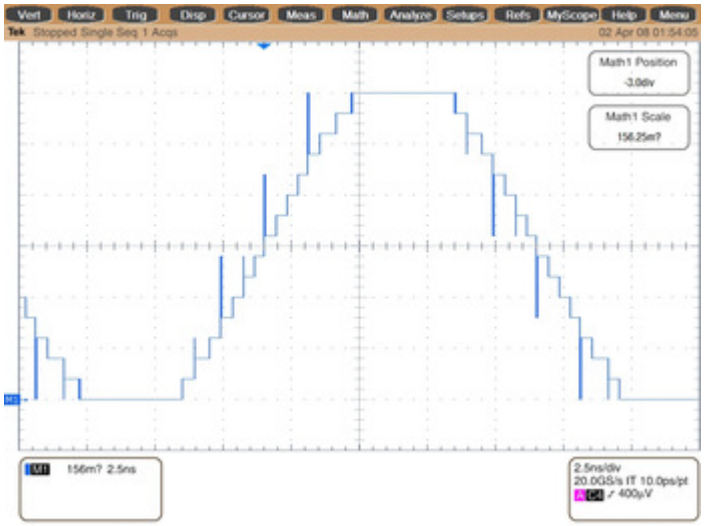
3.2.7.1 Static measurements

For characterizing the static performance of the ADCs, a low frequency 50 MHz sine signal was applied to the input of the converters at 5 GS/s sample rate. Reconstructed outputs of the converters are shown in Fig. 3.29 a) and b). Both outputs have glitches that occur due to non ideal simultaneous zero crossing of the outputs. The glitches are shorter than the conversion period, they take place for duration of 25-50 pS. Thorough testing of the output cables showed that even two "identical" cables have a ~30 pS time mismatch at the frequency of 5 GHz. It means that output skew error in range of 50 pS could be related to both skew error of A/D converter itself and/or errors because of measurement equipment.

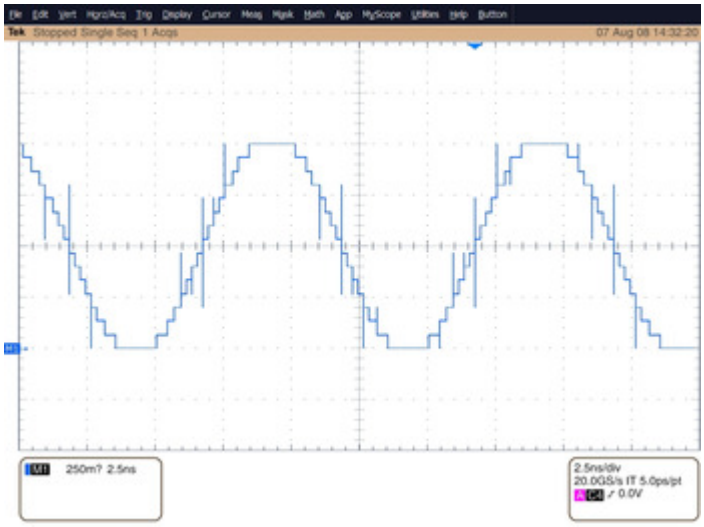
A static performance of the first chip ADC1 was inspected visually by observing output transfer characteristic. Visual observation shows that there are no missed codes in transfer function. Stairs are distributed equally, the width of the stairs changes from *min* width in the middle to *max* at the upper and lower parts of output signal, as it should be expected for the sine wave input signal.

The static characteristic of the second converter ADC2 was measured using histogram testing method [52]. Several periods of the output signal, like depicted in Fig. 3.29 b) were statistically analyzed. A deviation of a transition from the mean value (DNL) was calculated for each step. A cumulative sum of differential errors represents integral nonlinearity (INL). DNL and INL of ADC2 for each code are depicted in Fig. 3.30.

Both of the curves are located in range ±0.5 LSB. Only the code #4 has INL error 0.53 LSB that is slightly more than 0.5 LSB. As described above the ADC2 has inherently worse static behavior.



a)



b)

Fig. 3.29 Transfer function of the: a) ADC1 and b) ADC2

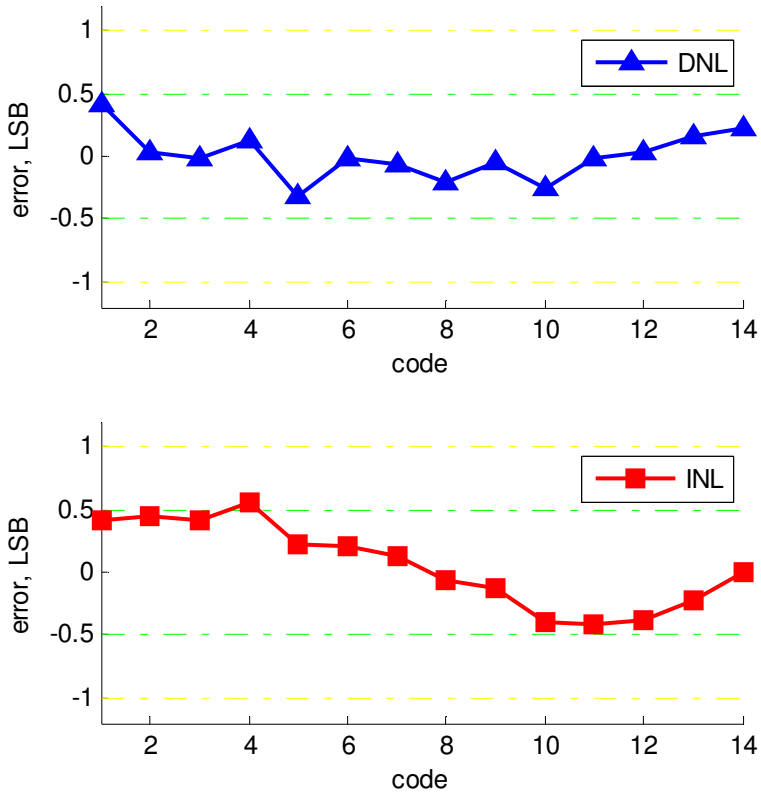


Fig. 3.30 DNL and INL from histogram testing of ADC2.

3.2.7.2 Dynamic measurements

Signal-to-noise and distortion ratio (SINAD) of the test circuits was measured over frequency range up to 6 GHz at constant sample rate 15.01 GS/s. Small frequency offset 10 MHz was made to accumulate quantization error over whole dynamic range. The results of the measurements are presented in Fig. 3.31, which shows SINAD of ADC1 and ADC2 up to input frequency of 6 GHz. Dashed lines show level where SINAD drops 3 dB below its value at low frequencies.

Analysis of the results represents correspondence with the theoretical calculations given above. ADC1 has better SINAD value at low frequencies because of its good matched reference network. But at the higher frequencies the reference network becomes a bottleneck. The performance of the converter rapidly degrades. Converter

has 2 GHz effective bandwidth, but could be used up to 5 GHz input, if lower effective resolution is acceptable.

The behaviour of the ADC2 is also predicted by theory. The worse value of SINAD at low frequencies is a result of higher random errors in the reference network. But ADC2 shows stable performance over whole frequency range up to 6 GHz. Converter does not work for frequencies higher than 6 GHz because of the ROM look-up table.

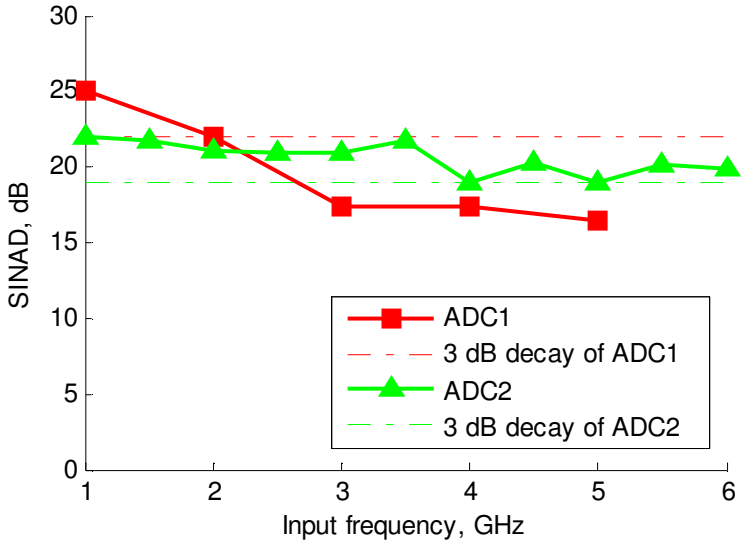


Fig. 3.31 Measured SINAD over frequency range up to 6 GHz.

3.3 Conclusion

Two A/D converters were designed and measured. Their parameters and comparison with state of the art ADCs are summarized in Table VIII. Parameters in Table VIII are taken from papers "as is" and sometimes they do not strictly correspond to definition given in "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters" [52].

The first ADC [53] can not achieve desired high-speed performance because the reference network does not have enough effective bandwidth at target frequency 5 GHz.

To overcome this limitation a new segmented configuration of the reference network was proposed. The segmented reference network can be implemented in several configurations. The fastest configuration, namely full parallel network, was successfully implemented in the second ADC [54]. Other possible configurations are described in the patent application [46].

With new parallel network the effective resolution bandwidth was increased by 3 times compared to that of [53]. To summarize advantages of proposed reference network, it can be said to have:

- Higher bandwidth for same power dissipation.
- Flexible configuration.
- Possibility to equalize bandwidth for different taps.
- Optimal power distribution scheme for the each tap, therefore min power dissipation at given speed.
- Possibility of electronic calibration of the separate reference voltage.

Converter with new network does not achieve best energy efficiency among other competitors. The converter reported in [41] is the best one, but it is implemented in modern CMOS technology. Comparing designs in the same technology, the conversion efficiency (FoM) is improved by ~2 times. The ADC with new reference network fully meets the target specifications and is ready to be integrated in the whole M-sequence radar system.

Table VIII. Comparison of high-speed ADCs.

Sample Rate, GS/s	Resolution, bits	ENOB, bits	ERBW, GHz	Power, W	FoM, pJ	Technology	Type	Ref.
10	5	> 4.1		3.6	47	0.18 µm SiGe, BiCMOS	flash	[19]
8	4	4	4	0.5	3.9	SiGe	flash	[35]
40	3	2.8	20	3.8	13.6	0.12 µm SiGe	flash	[21]
20	8	4.6	6.6	9	28	0.18 µm, CMOS	inter. pipeline	[42]
22	5	3.5	7	3	19	0.13 µm SiGe, BiCMOS	flash	[36]
24	6	3.5	12	1.2	4.4	90 nm, CMOS	inter. SAR	[40]
20	3		4.2	2.36	8.5	0.12 µm SiGe	flash	[20]
56	8	6.4	15	2	0.8	65 nm, CMOS	inter. SAR	[41]
15	4	3.4	2	0.6	14	0.25 µm SiGe BiCMOS	flash	[53]
15	4	3	6	0.75	7.8	0.25 µm SiGe BiCMOS	flash	[54]

Chapter 4. 5-bit, 10 GS/s DAC with 0.2 % Static Accuracy

4.1 Overview of the DAC's Architectures

There are a number of DAC architectures that can be divided in several classes [13]. These classes are:

- Resistor-based.
- Capacitor-based.
- Current source-based.

Resistor-based and capacitor-based DACs utilize binary weighted resistors and capacitors, respectively. The large value of passive components limits bandwidth of the converter and makes it impractical using those architectures in high-frequency range. An exception is an R-2R architecture, which can be related to the both resistor-based and current source based classes simultaneously and is suitable for high-speed DACs.

The third class, current source based DAC architectures, is well suited for GHz range. Several typical architectures of high-speed DACs are described in the next paragraphs.

4.1.1 Unary architecture

A unary-weighted architecture is a one of the simplest architectures of the DACs. Such a DAC, depicted in Fig. 4.1, consists of $N = 2^n - 1$ current sources which are connected or disconnected by the switches to the summing node, where n is the

resolution of the DAC. Unary converter has a regular structure with identical current sources. Therefore it has minimum errors resulting from mismatch of the components or their different speed characteristics. A standard input of the DAC is a binary code, and to control current switches the binary input should be converted into thermometer code. Complexity of such encoding grows exponentially with the number of bits. Inevitably, the power and area also follow this exponential growth and become factors which limit the resolution of feasible unary DAC architecture to 8 bits or even less. Another drawback arises from the size of decoding logic. The thermometer input has to be synchronized, that requires *N* latches. The clock feedthrough from latches propagates through the current switches and appears at the output as glitches.

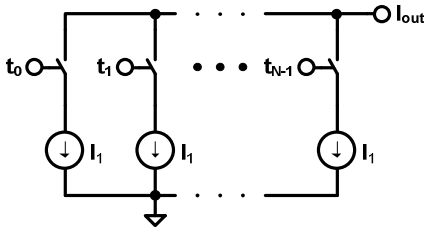


Fig. 4.1 Unary-weighted architecture.

4.1.2 Binary architecture

Combining unary distributed current sources in the form of binary-weighted groups or simply substituting them with the binary-weighted current sources, the binary architecture, as shown in Fig. 4.2, would be obtained. The switches are controlled directly by the binary code and therefore do not require any encoding. This is potentially the most power efficient architecture. The problem of this architecture is the difference in switching speeds. Since the current is scaled exponentially, the switches work under different conditions. This leads to glitches which become the main drawback of the binary architecture.

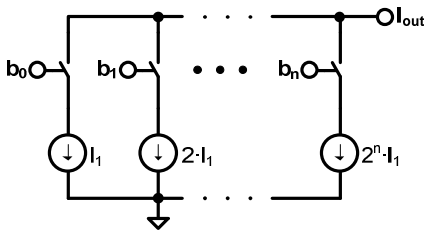


Fig. 4.2 Binary weighted architecture.

4.1.3 R-2R architecture

According to [13] the R-2R DAC belongs to resistor based DACs. Implementing a summing node as R-2R ladder as depicted in Fig. 4.3, high-speed performance can be achieved. The advantage of the R-2R architecture is good matching of the components. *n*-bit R-2R DAC needs *n* equal current sources and load resistors with values *R* and *2R* which can be easily built from two *R* resistors connected in series. Therefore it has lower glitches than binary DAC. The drawback is lower bandwidth and wasting 50% of the switch current.

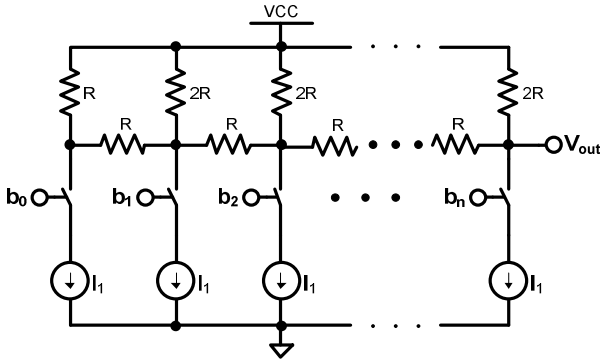


Fig. 4.3 R-2R architecture.

4.1.4 Segmented architecture

Binary and R-2R architectures have minimum digital logic, but lager glitches, worse DNL and INL and do not have intrinsic monotonicity as unary architecture. On

the other hand the resolution of a feasible unary DAC is limited to 4-5 bits. To benefit from the advantages of different architectures and simultaneously keep error and complexity small, the segmented architecture is preferred. Segmentation means implementation of MSBs in one configuration and LSB in the other. Of course the number of segments is not limited to two, and any sub-architecture could be used.

4.1.5 Calibration of DAC

Components of the DAC such as resistors or current sources can be affected by random errors. The fluctuations effecting component performance are not predictable and can be corrected after manufacturing. There are two ways to correct them: passive correction — trimming or fusing and electronic calibration. If the resistors are manufactured above the passivation layer of the chip or openings in passivation layer above the resistors are realized, their value can be trimmed with a laser. But trimming is expensive and not always available. Another possibility is using fuses to open/close interconnections between passive elements. In this case each resistor is a compound resistor, which consists of several unity resistors connected through the fuses. By means of blowing the fuse the target resistance value could be adjusted.

The passive correction suffers from the drawback that it can be done only once and it needs special layout preparation and technology support.

In contrary to this, the electronic calibration does not need special technology. It can work in two modes: background and off-line modes. The electronic calibration can compensate also slow variations, such as temperature drift.

The background calibration corrects errors of the DAC during normal operation of the device. To perform the off-line calibration the conversion process should be interrupted. During electronic calibration voltage controlled or current controlled current sources (VCCS or CCCS) are adjusted to desired values. As a control device the low speed high-resolution DAC can be used.

4.1.6 Choice of DAC architecture

In Table IX the state of the art of high-speed DACs is given. Converters are implemented in different architectures. Further analysis shows that 3-bit DAC [55] has unary configuration, while DACs with higher resolution have binary or segmented architectures.

The pure unary architecture, despite all its advantages, is not a good solution for 5-bit DAC because of its need for a large decoding logic. Other "pure" architectures, R-2R and binary also are not well suited for target converter because of their accuracy issues. By combining best features of architectures it is possible to achieve a good compromise between high performance, low power dissipation and complexity.

Due to the reasons described above, the most significant bits were implemented with unary architecture. The less significant bits could be implemented either in binary or in R-2R configuration. The binary configuration has higher bandwidth. But switches which work with different currents and therefore with different speed, will cause additional distortion. In contrast the R-2R configuration having lower bandwidth employs identical design of the current sources which reduce matching efforts and make this architecture potentially more accurate. The target bandwidth of 5GHz could be achieved with *R-2R* configuration in IHP technology. Therefore the segmented architecture with 2 unary bits and 3 R-2R bits was chosen.

Table IX. State of the art of high-speed DACs.

Sample rate, GS/s	NOB	Dyn. Range, V	SFDR, dB	Power, W	Type	Tech.	Ref.
22	6	1.3	35	2	segmented	SiGe 0.13 µm	[56]
20	6		19	0.36	binary	SiGe 0.18 µm	[55]
40	3		20	0.66	unary	SiGe 0.12 µm	[21]
20	6	1	28	1	binary	SiGe 0.25 µm	[57]

4.2 Implementation of 5-bit DAC

4.2.1 Accuracy consideration

The DAC basically consist of a decoding logic and a bank of current switches which connect/disconnect the bank of current sources to/from summing node.

The static accuracy (INL) of the unary converter depends on the output resistance R_0 of current source [13] as:

$$INL(k) = \frac{k\left[1+\alpha\left(2^n-1\right)\right]}{1+\alpha k} - k; k = 0..2^n - 1 \tag{4.1}$$

where $\alpha \approx R_L / R_O$, R_L is the load resistance, and R_O is the current source output resistance.

INL has a maximum at the mid-scale and is approximately equal to:

$$INL_{max} \approx \alpha \cdot 2^{2n-2} \tag{4.2}$$

In order on obtain *INL<1 LSB* it is necessary to use the current source with output resistance:

$$R_O \geq R_L \cdot 2^{2n-2} \tag{4.3}$$

The segmented architecture relaxes requirements for the output resistance, because the lower number of the current sources is connected in parallel to the load. For the simplicity the unary configuration as worst case is considered further.

Design of the particular current source mainly depends on available voltage headroom. For 3 Volt supply voltage, a bipolar current source with emitter degeneration can be used. There is no headroom for a cascode stage, which could help to achieve higher output resistance.

The current source with emitter degeneration has output resistance [48]:

$$R_O \simeq \mathrm{r}_O \left(1 + g_m R_E\right) \tag{4.4}$$

where r_O is output resistance of the simple current source without degeneration:

$$r_O = \frac{V_{EF}}{I} \tag{4.5}$$

and V_{EF} is the Forward Early voltage.

A typical example for IHP SG25H1 technology is as follows;

V_{EF}=*30 V*. The current of current source is *I=1 mA*, and the load resistor R_L=*100 Ω*.

Calculation of the output resistance of current source for the 5-bit DAC at the room temperature gives:

$$R_O = \frac{30V}{1mA}\left(1 + \frac{1mA}{26mV} \cdot 300\Omega\right) \approx 375k\Omega \tag{4.6}$$

It is higher than the value of 25 kΩ, which can be calculated from (4.3).

Another source of errors is process variation of degeneration resistor of current source. Variation of the resistors has an effect on the current and on the DNL and INL eventually.

In IHP technology, the resistor value is calculated by the formula given in the process specification:

$$R = \frac{l \cdot R_{sheet}}{w_{eff}} + \frac{2R_{Zspec}}{w_{eff}} + \frac{2R_{Cspec}}{N_{cont}} \tag{4.7}$$

where:

R_{sheet} is the sheet resistance;

l is the length of the resistor;

w_{eff} is the effective width of the resistor;

R_{Zspec} is the specific resistance contact between silicide and poly region;

R_{Cspec} is the specific resistance of the contact;

Equation (4.7) is valid for the resistors of rectangular shape and is not suitable for calculation of resistance value of complicate shape with several bends.

The variations of the parameters, according to IHP process specification are:

R_{sheet}: -10% .. +10%

R_{Zspec}: -12% .. +12%

R_{Cspec}: -60% .. +100%

For wide resistors last two terms of equation (4.7) become significantly small and the first term is decisive.

To compensate for possible error, a voltage controlled current source is used in the current switch (CS). The block diagram of CS is depicted in Fig. 4.4. It consists of a differential pair, which acts as switch and VCCS. The current source is controlled by a 10-bit µDAC. The input value of µDAC is applied externally via SPI-slave interface.

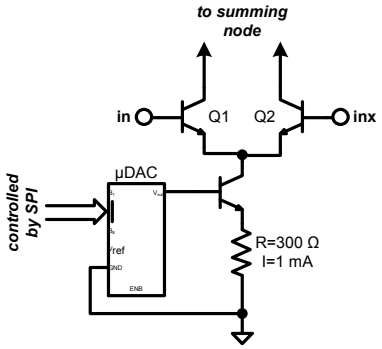


Fig. 4.4 Differential current switch.

Segmented 5-bit DAC with a 2-bit unary sub-DAC and 3-bit R-2R sub-DAC needs 6 current switches. The R-2R sub-DAC has binary input, therefore no decoding is necessary. In contrary the unary sub-DAC has a unary input and needs a binary-to-unary decoder, whose truth table is given in Table X. The unary code in Table X is slightly different from the usual thermometer code, which is used in the full flash ADCs. But the main condition, that the number is coded by the numbers of "1" is preserved. Shifting each even row in left direction, allows to reduce the complexity of the decoder two times.

Table X. Conversion table of 2-bit binary-to-unary code.

Binary code		Unary code		
b1	**b0**	**t2**	**t1**	**t0**
0	0	0	0	0
0	1	0	0	1
1	0	1	1	0
1	1	1	1	1

The complete block-diagram of the DAC is depicted in Fig. 4.5. The DAC consists of the binary-to-unary encoder of 2 MSBs, retiming circuitry and 6 current switches. The retiming circuitry is necessary to synchronize the direct LSBs and decoded MSBs.

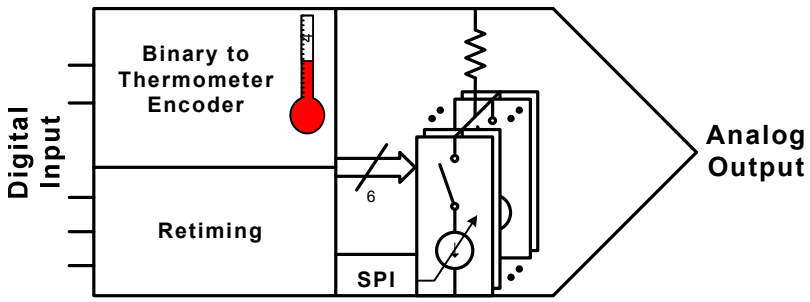


Fig. 4.5 Block-diagram of 5-bit DAC.

4.2.2 Off-chip calibration

Generally calibration means comparison with a known, precise value and correction according to comparison results. In case of the DAC it means that the output should be compared with an "ideal" value. For off-chip calibration it is assumed that the "ideal" reference value would be supplied externally. It has the advantage of freely choosing the reference values, hence overcoming possible reference accuracy problems.

The whole calibration procedure of comparing, making decision and controlling VCCS via SPI is targeted to be integrated on a single chip in future phases of the project.

The external off-line calibration system of the DAC should satisfy following requirements:

1. It should be able to provide reference signal with accuracy higher than desired accuracy of the DUT or as alternative: the system should measure output of DUT with accuracy high enough.
2. It should provide SPI-Master.
3. It should be able to control inputs of DAC under test.
4. It should implement automatic calibration loop for each bit.
5. It should be implementable for on-chip calibration in the future versions.
6. High speed performance is not required.
7. The calibration should be off-line.

Inspection of the DAC outputs should be realized by a high-resolution ADC. The ADC will provide the measurement of the output ready in digital form for processing.

The calibration algorithm itself can be implemented with a processor or with an FPGA. But for further integration it is better to use the FPGA. A calibration algorithm written in VHDL and translated into FPGA could be easily adopted and synthesized as a digital block.

It can be concluded that the FPGA is best suited for the task of off-chip calibration. Another argument for the FPGA is that reference source 1-bit ΔΣ-DAC could also be produced by the FPGA. Together with a first-order low-pass filter and an accurate comparator, which should be realized on-chip, ΔΣ-DAC works as a precise A/D converter.

4.2.2.1 Calibration algorithm

The proposed calibration scheme is depicted in Fig. 4.6. It is implemented with Spartan-3AN Starter Kit board. Spartan-3AN Starter Kit was selected because of two reasons: it has LVDS I/O; it has built in 14-bit ADC and 14-bit DAC, which can be used as reference.

Shortly, the calibration algorithm could be characterized as successive approximation of DAC output to the reference value. Detailed calibration flow of each current source is as the following:

1. Current source under calibration (CSUC) is disconnected from the summing node. For this, the corresponding digital input is applied to the DAC.
2. The analog output of the DAC is measured and stored in memory as “zero-value”. The measurement is performed with 14-bit ADC on FPGA board.
3. The CSUC is connected to the summing node.

4. According to binary search algorithm, the MSB of µDAC is set to "1".
5. The output of ADC is measured again and difference between the stored "zero-value" and the measured value is calculated.
6. Depending on this difference the decision about value of the MSB of µDAC is made.
7. Steps 4-6 are repeated for rest 9 bits of µDAC.
8. Steps 1-7 are repeated for each current source.

The calibration algorithm is realized in VHLD and translated into Spartan-3AN Starter Kit board. The state machine of whole calibration algorithm is given in Appendix A. For simplicity the calibration of only one current source is shown in detail, others are in closed form.

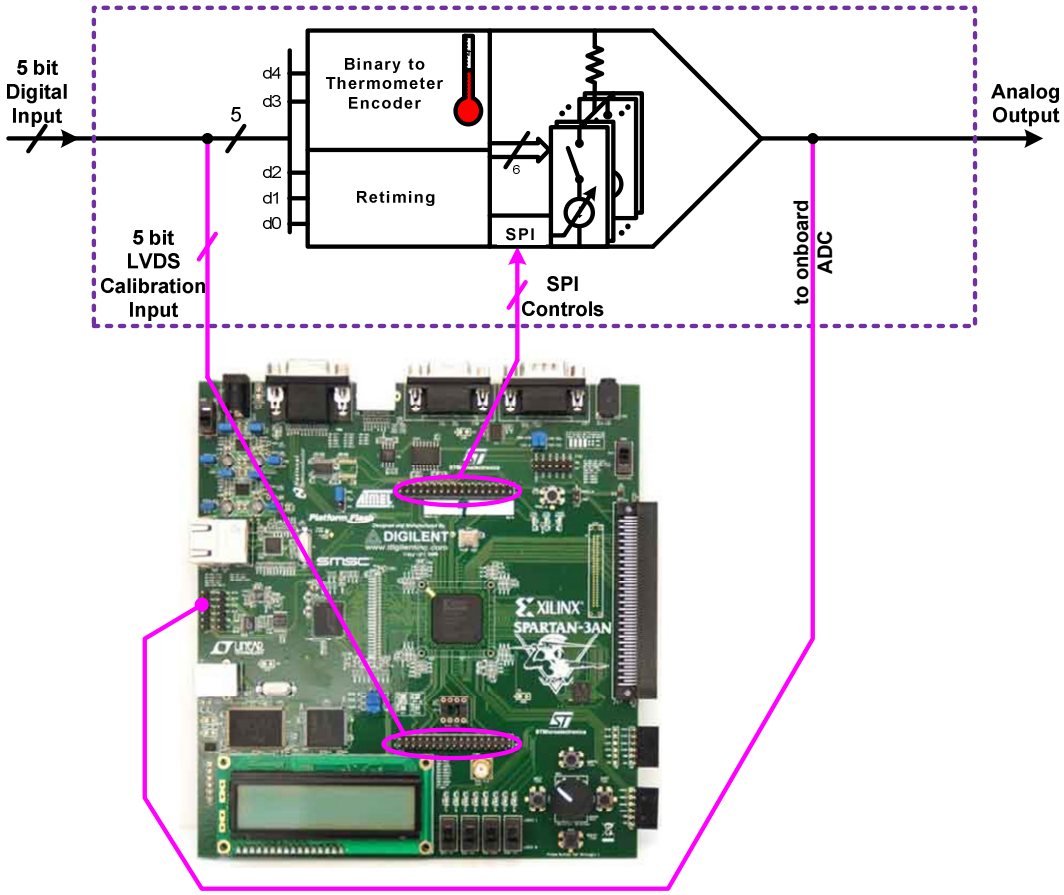


Fig. 4.6 Off-chip calibration of the DAC.

4.3 Experimental results

4.3.1 Static measurements

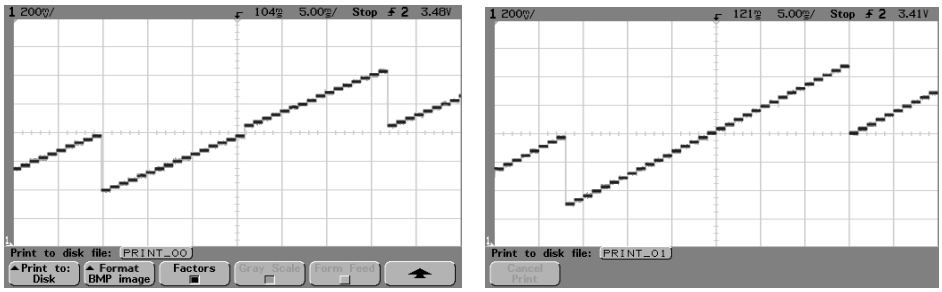
The DAC test chip was implemented in SiGe 0.25µm BiCMOS IHP technology. The chip was mounted on a test board and connected to the FPGA board. The output of the DAC was examined with low-speed oscilloscope.

The uncalibrated output is shown in Fig. 4.7 a). It is impossible to evaluate all errors optically but there is visible big transition in the middle of the output curve. The calibrated output, shown in Fig. 4.7 b), has no visible artifacts over the whole range.

Static parameters as INL and DNL of uncalibrated and calibrated outputs were also measured numerically. The results are given in Fig. 4.8.

Analyzing the uncalibrated DNL values, it can be noticed that converter has quite constant DNL errors with exception in the middle of the range. Quasi-constant positive DNLs are accumulated in INL values, which exceed 0.5 LSB. The maximum error in code #16 reach 2.4%, that is more than 10 times higher than maximal target error. After calibration the errors were reduced to value below 0.15%. The distribution of the errors over input range is shown in Fig. 4.9.

The DAC with errors bellow 0.2 % can be used in the capturing device with overall resolution of 9 bit.



a) b)

Fig. 4.7 Uncalibrated and calibrated outputs of the DAC.

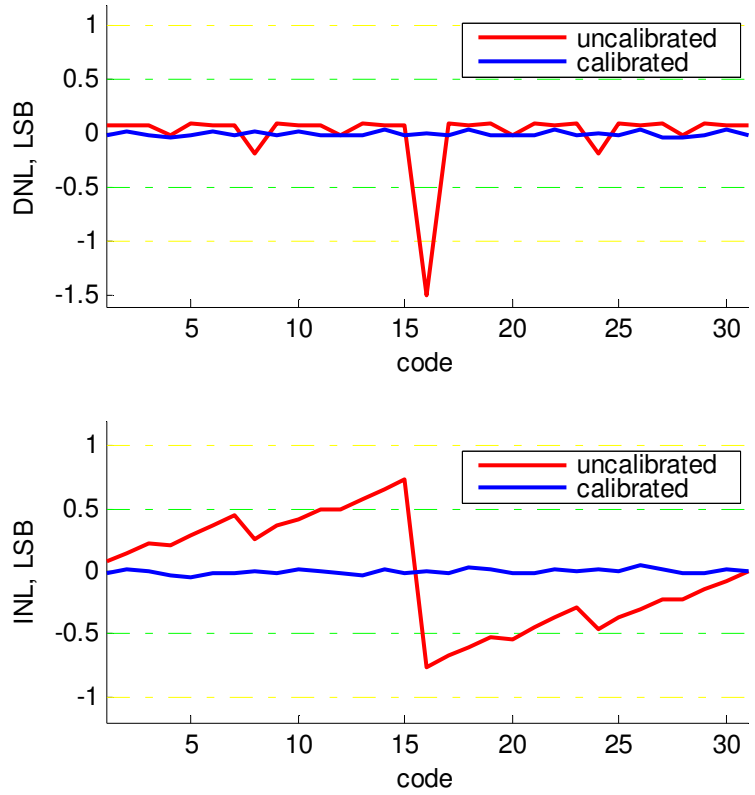


Fig. 4.8 DNL and INL of uncalibrated and calibrated DAC output.

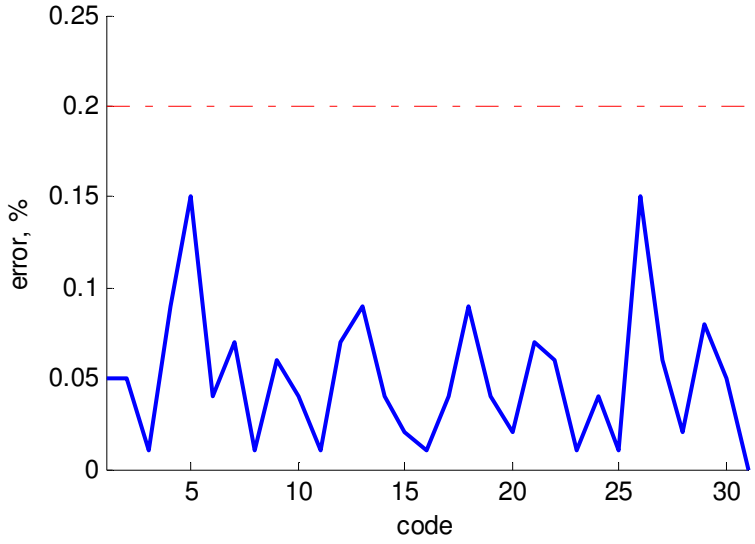


Fig. 4.9 Static accuracy of the calibrated DAC.

4.3.2 Dynamic measurements

For measuring spurious free dynamic range (SFDR) a 5-bit digital sine signal has to be applied on the input of the DAC. Unfortunately we do not have possibility to apply the digital sine in GHz frequencies. Only one possibility available in our lab is to connect the 4 bit ADC, described in previous chapter, to 4 MSBs of the DAC. It is assumed that LSB works usually faster than MSB.

The major limitation of such ADC-DAC configuration is its being useless to measure SFDR of the DAC because it will be dominated by the less accurate ADC but not the DAC.

Nevertheless high-speed performance of the DAC can be well estimated with an envelope test [58]. Both converters are clocked with the same clock f_s frequency.

The input frequency of the ADC is selected to be:

$$f_{in} = \frac{1}{2} f_s + \Delta f \tag{4.8}$$

where Δf is the frequency of the envelope. To observe all output transitions the Δf should satisfy:

$$\Delta f < \frac{2\pi f_{in}}{2^n} \tag{4.9}$$

The measured output of the ADC-DAC is shown on Fig. 4.10, where envelopes at two input frequencies are depicted. On Fig. 4.10a the envelope of 5 GHz input signal is shown. Output is changing from ±1 LSB to ±0.5 $V_{p\text{-}p}$ and contains all quantization steps. It means that both ADC and DAC are fully functional. Output starts to degenerate at frequency 5.5 GHz, Fig. 4.10b, where the amplitude of output signal is decreased.

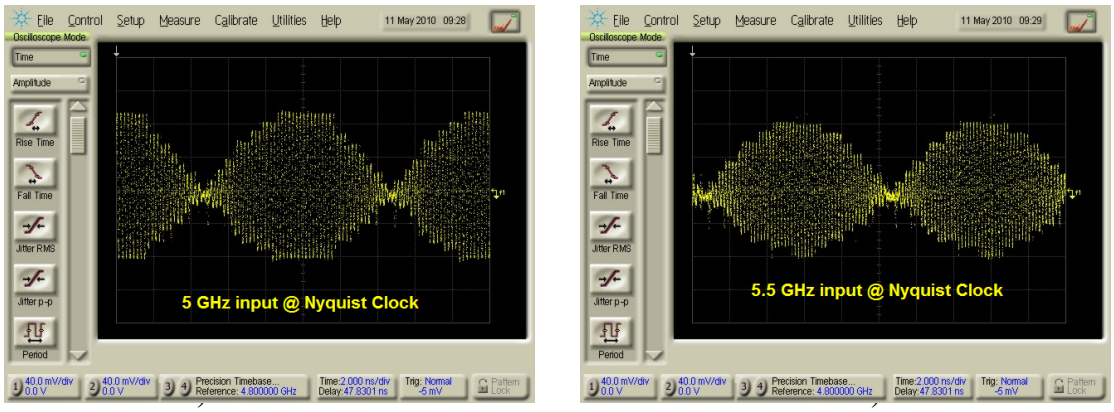


Fig. 4.10 Envelope test of ADC-DAC at a) 5 GHz and b) 5.5 GHz.

4.4 Conclusion

The design and test results of 5-bit DAC with external off-line calibration were presented in this chapter. Measurement results of the DAC presented satisfactory results for the integration into M-Sequence radar system. Intrinsic errors of 2.4% of the DAC were reduced to values lower than 0.15% with calibration. Measurements together with A/D converter have proved high-speed functionality of D/A converter up to target frequency 5 GHz. The main parameters of the DAC are summarized in Table XI.

Table XI. Summary of the DAC characteristics.

Parameter	Value
Sample rate	10 GS/s
Input frequency	5 GHz
Resolution	5 bit
Dynamic range	1 Vp-p
DNL	-0.03..+0.04 LSB
INL	± 0.05 LSB < 0.15%
Accuracy	<0.15%

Conclusion

The new concept of the Maximum Length Binary Sequence (M-sequence) Radar was developed within the framework of DFG UKoLoS program. The M-sequence radar is a result of cooperation of four institutions: RWTH Aachen University, Technical University Ilmenau, Friedrich-Alexander University of Erlangen and Brandenburg University of Technology Cottbus (BTU).

Within the frame of BTU's responsibility, the main components of data capturing device, such as track-and-hold amplifier (THA), analog-to-digital converter (ADC) and digital-to-analog converter (DAC) were designed, manufactured and tested. The last block of capturing device, the low noise subtraction amplifier, is decided to be integrated in the receiver front-end and implemented by another partner.

Two designs of the track-and-hold amplifier were presented in this work. Both amplifiers are very effective in terms of power/accuracy.

The significance of the first THA [34] is its low power dissipation in GS/s range. It dissipates less than 10% of power of nearest competitor (Table V, page 37). The low power dissipation was achieved by using low tail currents in the input buffer and switched emitter followers together with small hold capacitances to achieve high speed. The small hold capacitance makes THA core very sensitive to the load due to output buffers. The leakage current, which is caused by base current of the output buffer, changes the stored value. To prevent this, a leakage current compensation technique was implemented in output buffers. With this technique both low power and good accuracy could have been achieved. Because of the low power and low supply voltage, the amplifier very well suits the purpose of integration in low-resolution A/D converters.

In the second THA several parameters were improved. First, the bandwidth was increased to 3 GHz. Second, together with the higher bandwidth the resolution was increased to 8 bit. To achieve the better resolution direct feedthrough suppression using an additional input buffer was implemented. The switched emitter follower (SEF) was also modified for better speed performance. A current path in SEF was isolated from the

input buffer. The input buffer and SEF do not share the same load as in [34] which prevented the input buffer from saturating. This THA is suitable to be integrated in high-speed medium-resolution A/D converters.

Two A/D converters were designed and measured during this work. The first ADC [53] could not achieve the desired high-speed performance because the reference network did not have enough bandwidth at target frequency of 5 GHz. To overcome this limitation the new segmented reference network was proposed and successfully implemented in the second ADC [54]. The proposed network has a segmented, free configurable structure and can be configured according to power/speed requirements. The possible configurations are described more detail in patent application [46]. For the implementation in the ADC the full parallel configuration was selected because of speed concerns. With the new network the effective resolution bandwidth of the ADC was increased by 3 times compared to that of [53] while keeping the power dissipation 20% higher than in [53]. To summarize the advantages of proposed reference network, it can be said to have:

- The higher bandwidth for the same power dissipation.
- The free configurable segmented structure.
- Possibility to equalize bandwidth of the different segments.
- The optimal power distribution scheme for the each segment, therefore minimum power dissipation at given speed.
- Possibility for electronic calibration.

The ADC with proposed reference network fully meets the target specifications and is ready to be integrated into the M-sequence radar system.

The 10 GS/s 5-bit DAC with external off-line calibration, which works as predictor, was also realized as part of this work.

Intrinsic errors 2.4% of the DAC, that is 10 times higher than required, were reduced to values lover than 0.15% with calibration. Measurements together with A/D converter have proven high-speed functionality of D/A converter up to target frequency 5 GHz. The DAC is also ready to be integrated into whole M-Sequence radar system.

Future work

The implementation of the whole M-sequence radar is not finished within timeframe of this work. All components from all partners are nearly ready for implementation, but the system concept is continuously being developed, therefore components may also need to be changed.

The future work is going in two directions: the first direction is namely implementation of components into single chip, second is improving characteristics of the existing components to achieve better overall performance of the radar.

ADC: A/D converter could be optimized for achieving a higher bandwidth by elimination of the bottleneck in components. For instance the ROM look-up table limits the speed of the converter. The possible modification is dividing ROM table into several sub-tables.

Together with the bandwidth there is a potential to increase the accuracy of the converter. Higher DNL/INL values inherent in the new reference network could be easily lowered by electronic calibration. The calibration method was already tested with DAC and can also be implemented for the ADC.

DAC: The further work on DAC will go in the direction of integrating the calibration system with converter in single chip. Also a new converter with higher resolution could be desirable. Higher resolution of the DAC would result in increased SNR of the whole system. On the other hand, the higher resolution would require more precise calibration.

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List of Abbreviations

ADC, A/D	analog-to-digital converter
BW	bandwidth
CHEF	Cherry-Hooper amplifier with emitter follower feedback
DAC, D/A	digital-to-analog converter
DEMUX	demultiplexer
DLL	delay locked loop
DNL	differential nonlinearity
DUT	device under test
ENOB	effective number of bits
ERBW	effective resolution bandwidth
FA	folding amplifier
FM	frequency modulated
FoM	figure of merit
FPGA	field programmable gate array
INL	integral nonlinearity
IRF	impulse response function
LSB	less significant bit
MSB	most significant bit
M-sequence	maximum length binary sequence
MUX	multiplexer
NOB	number of bits
PN	pseudorandom

List of Abbreviations

ROM	read-only memory
SAR	successive approximation register
SEF	switched emitter follower
SINAD	signal-to-noise and distortion ratio
SNR	signal-to-noise ration
SPI	serial peripheral interface
THA	track-and-hold amplifier
THD	total harmonic distortion
UWB	ultra-wideband
VHDL	very high speed integrated circuit hardware description language

Appendix A. Calibration state machine.