A Novel Approach for Generating Active Inductors for Microwave Oscillators –

Mathematical Treatment and Experimental Verification of Active Inductors for Microwave Applications

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Preface and Appreciation

This work is the result of my research in the area of microwave oscillators and my desire to replace the costly microwave tuning diodes with an active circuit that allows the replacement of the inductor in an oscillator with such a circuit and yet optimized both in output power and phase noise. The related research work was only possible based on many measurements and tests performed at Synergy Microwave Corporation. I am very grateful for the support of the Engineering team, specifically, Dr.-Ing Ajay Kumar Poddar and Rucha Lakhe, who supported the improving of the manuscript, many of the time-consuming measurements, literature acquisitions and test and measurement. This work is a continuation of my PhD dissertation

A New and Efficient Method of Designing Low Noise Microwave Oscillators

submitted 2004 to the Technische Universitaet Berlin

The possibility to use this favorite topic of mine in a habilitation was only made available by Professor Dr.-Ing. Dirk Killat, who also made himself available for many discussions on the approach. Professor Dr.-Ing Ignatz Eisele and Professor Dr.-Ing. Thomas Eibert as well as Professor Dr.-Ing Hans Hartnagel were always available for final discussions and useful recommendations.

Summary

While the invention of the spark generator made the first transmitter possible, the resonator acted as both antenna and resonator. Figure 1 shows the mechanically huge inductor and capacitors. The circuit voltages were up to ten thousand volts.

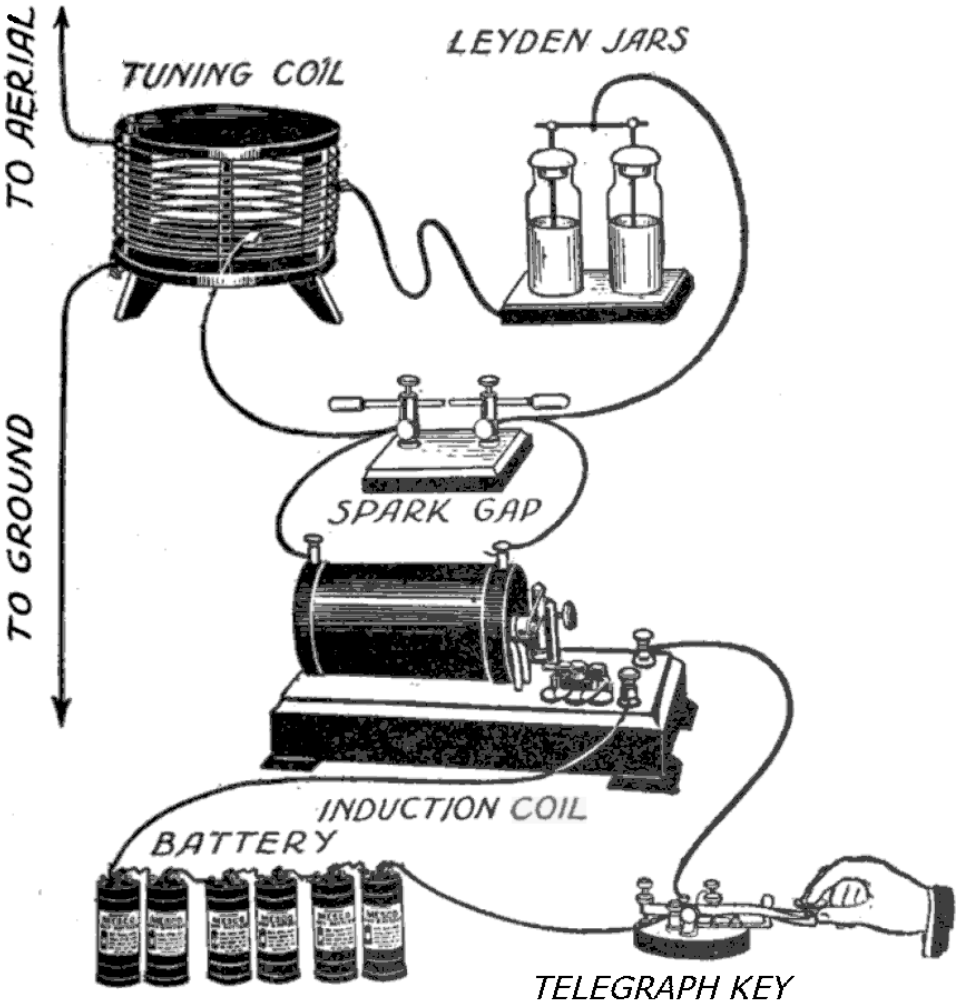

Figure 1. A typical Spark-gap transmitter [1]

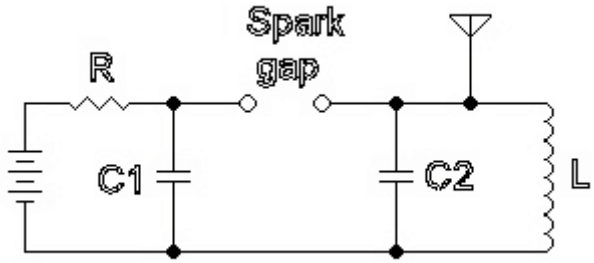

Figure 2. A typical Spark-gap receiver [1]

The spark-gap frequently was housed in a little glass tube and the spark observed under microscope. The initial invention by Heinrich Hertz [2] operated at microwave frequencies, while Marconi [3] operated at frequencies of 30 kHz and above. The objective of this research work is to explore cost-effective electronic versions of the mechanical inductor at RF and microwave frequencies. Shortly after the invention of the radio tube, specifically the

microwave lighthouse type triode (shown in Figure 3), the first experiments were made with quarter wavelength transmission line resonators.

Figure 3- The light-house tube EC 55 [4]-[6]

As shown in Figure 3, the name "lighthouse tube" [4]-[6] is due to its physically resemblance to a lighthouse.

For the first microwave oscillators the transmission line resonators were connected at the point of peak currents so that the RF voltages can be kept out of phase. As the tube has a negative polarity transconductance, relative from grid to plate, the two voltages needed to be out of phase. One side was connected to the plate or anode and the other to the grid. Figure 4 shows an oscillator based on mechanically tuned transmission lines based oscillator and its electrical equivalent. The tubes had direct or indirect filaments for heating so RF chokes were needed.

L_a *and* L_g are the quarter wavelength transmission lines connected to the anode (a) and grid (g) while B is the mechanical sliding bar used for frequency adjustment. C_{ga} is the intrinsic capacitance built between the grid and anode. C_{gk} is the intrinsic capacitance built between the grid and cathode (k). C_{ak} is the intrinsic capacitance built between the anode and cathode. D_r is the RF choke used and C_{DR} is its intrinsic capacitance.

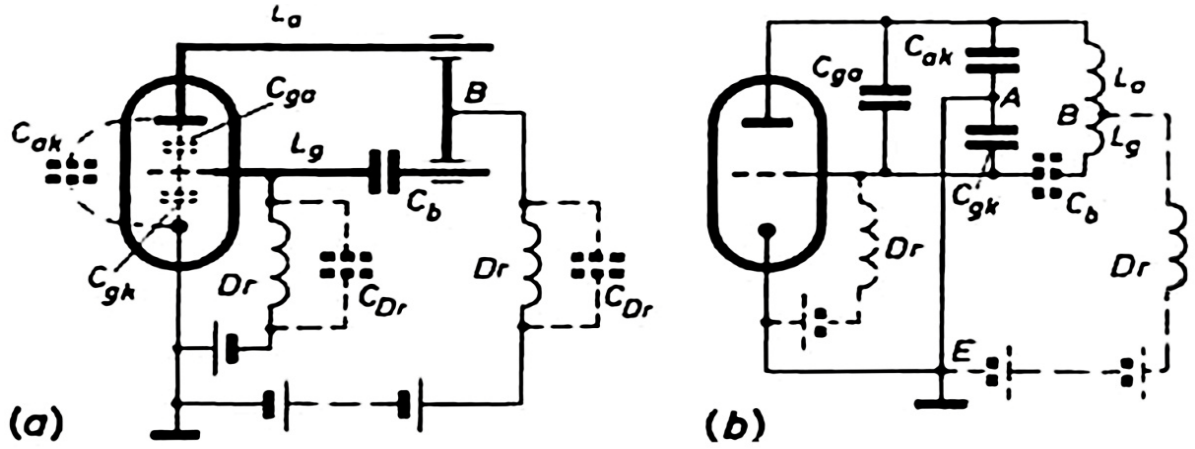

Figure 4. (a) the mechanically tuned quarter wavelength transmission lines based oscillator (b) shows its electrical equivalent [7]

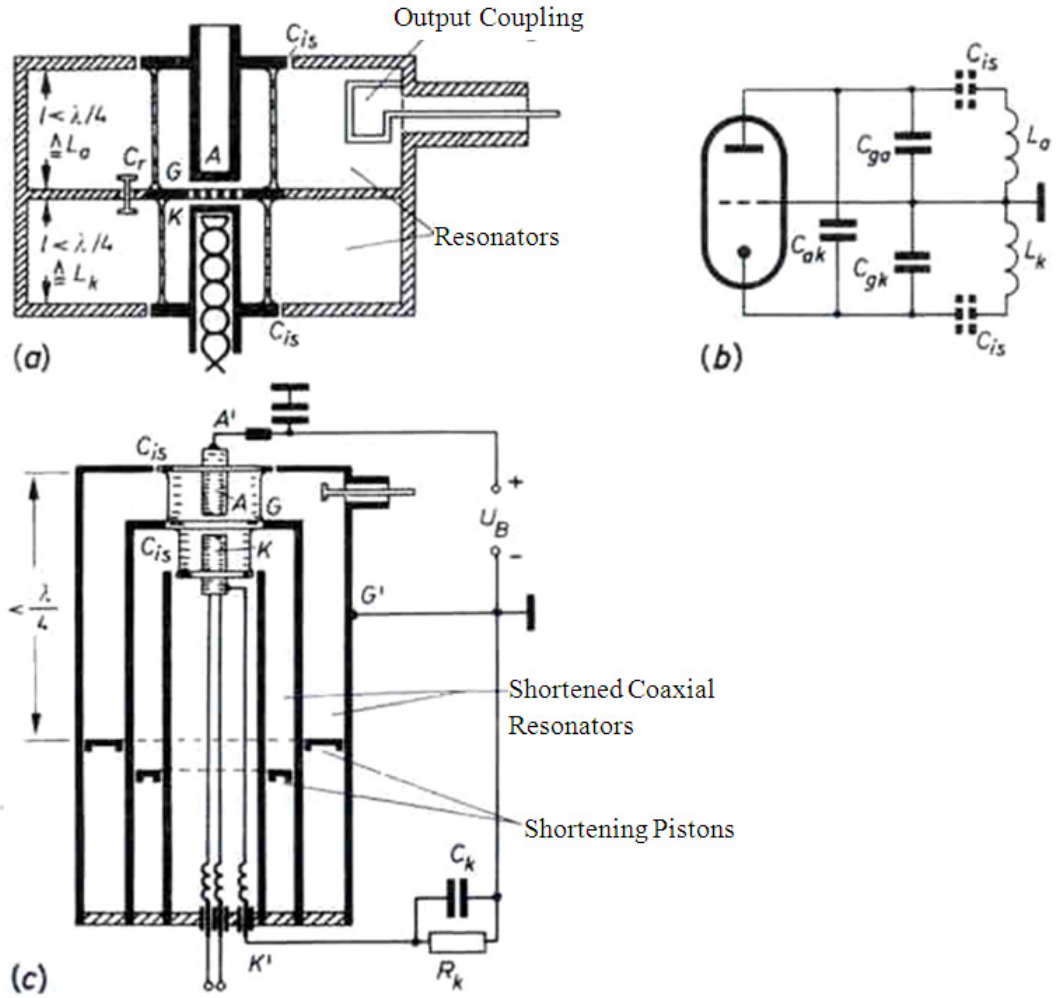

Figure 5. A typical schematic of a coaxial resonator based oscillator symmetrically built. The plate or anode (A) and cathode (K) are tuned. The grid is denoted by (G) [7].

There were two methods to change the frequency.

- One method was to reduce the length of the transmission line called as the "Lecher line" at that time, to increase the frequency.
- The other method incorporates an air variable capacitor between the grid and anode. The principle working of the capacitor was based on the glass bottles of Leyden. The aluminum foil placed inside and outside of the bottle with glass as the insulator forms the two plates of the capacitor.

This work will show that an active tunable inductor offers advantages compared to capacitors. It was found that certain L/C ratios gave the best frequency stability. If an external capacitor was much higher than the intrinsic tube capacitor, the stability was higher, as changes of the tube parameters did not matter much. Oscillators of these types were built up to 6 GHz. At higher frequencies, there were no discrete inductors but a coaxial resonator, as shown in Figure 5.

After RF tube based oscillator designs were replaced by transistor-based designs, similar tuning circuits were used at about 100MHz. Based on the Armstrong [8] patent, around 1922, the super regenerative receiver [9] was invented. While this is not a paper on receiver, it is interesting to show the need for high-Q inductors not only at microwave frequencies but also at low frequencies.

For lower frequencies as the amplitude modulated (AM) broadcast band, ranging from a few 100 KHz to a few MHz this situation was more complicated. The Armstrong patent based frequency modulated (FM) receiver was an oscillator, which was switched on and off at a quenching frequency above 25 KHz, which the ear could not hear. The gain of such an oscillator was in the vicinity of one million and the switching type feedback system made the LC circuit more narrow then its unloaded Q.

At the AM application (use of only amplitude modulation), before 1950, this regenerative principle was not known.

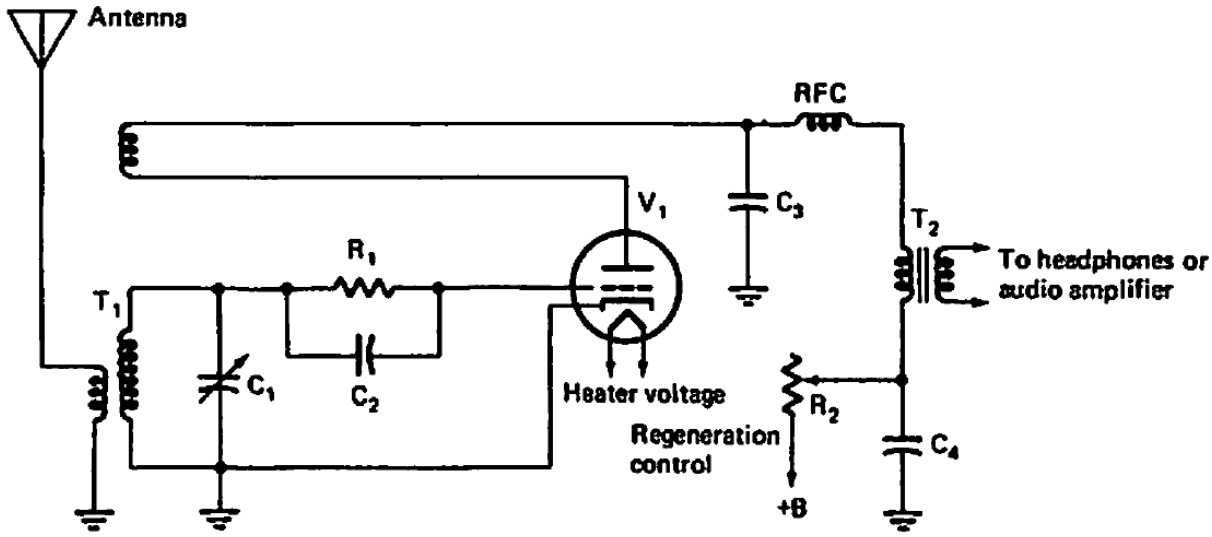

Figure 6 A typical schematic of regenerative AM- receiver

Simple receivers required several amplifiers tuned to the frequency of reception. These amplifiers were cascaded which can cause stability problems. The trick was to apply enough feedback to increase the operating Q (figure of merit) calculated typically as $\omega L/R_s$ (R_s= loss resistance) to above 50. Around this time, honeycomb coils were invented and Q values up to 100 were not uncommon. The electronic feedback allowed building these Q multipliers but tuning was very tricky. As the loss resistor R_s is responsible for the Q reduction, the feedback mechanism would apply a negative resistance to partially compensate the loss. This results in a higher Q-factor.

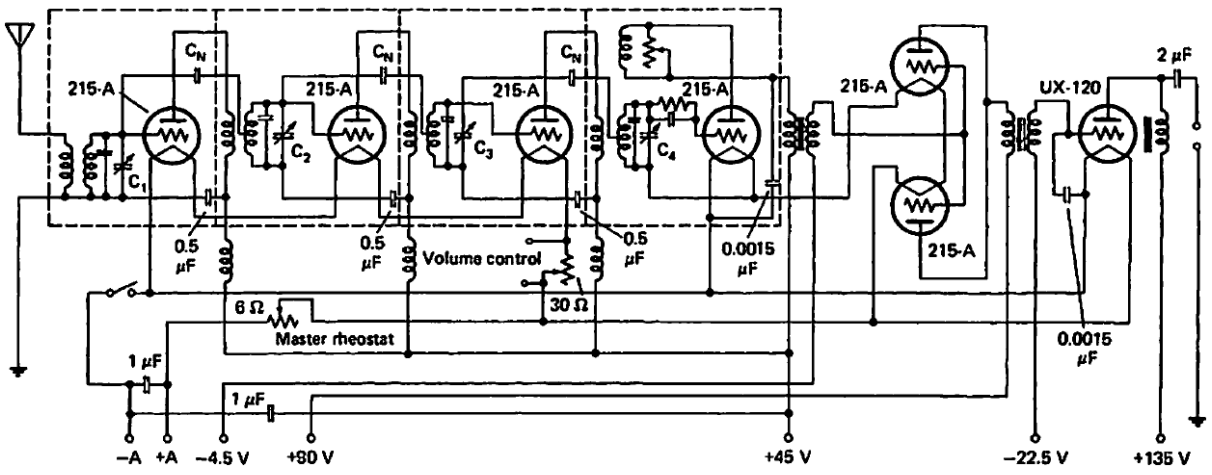

Figure 7 A typical schematic of three stage amplifier based receiver and detector/output amplifier

The capacitors C1 through C4 set the frequency of the receiver. This receiver has four discrete high-Q inductors, but these may take a large volume and were very costly. An active inductor because of the impedance transformation would not have worked here.

As the frequency of reception went up to around 10 MHz, the demand for high Q increased. The tuning became increasingly complicated and the receiver was usually unstable.

These complications were ultimately overcome by the invention of the dual conversion receiver, where the high gain stages operated at 200 kHz to 500 kHz and the input frequency was converted down to an IF (intermediate frequency). These types of receivers were also called superheterodyne receivers. The block diagram of a commonly used superheterodyne receiver is shown in the Figure 8.

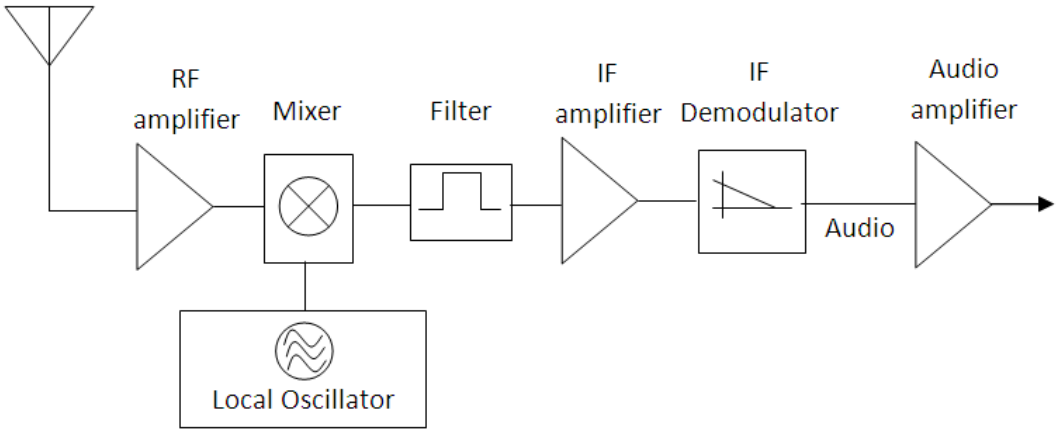

Figure 8 A typical block diagram of dual conversion receiver

The term heterodyne refers to a beat or difference frequency produced when two or more radio frequency carrier signals are mixed in a detector. A superheterodyne receiver or colloquially, superhet, uses frequency mixing or heterodyning to convert a received signal to a fixed intermediate frequency. This intermediate frequency can be more conveniently processed than the original radio carrier frequency. Virtually all modern radio and television receivers use the super heterodyne principle.

After this selectivity adventure, let us continue with the development of tube-based radios that need capacitors and inductors at various places. During the time tubes were in use, the tuning elements were strictly air variable capacitors. Oscillator-tuned circuits were gang tuned or synchronously tuned with the necessary frequency-offset (IF) [10]. Figure 9(a) shows a picture of a air-variable capacitor for VHF applications and Figure 9-(b) shows a high-Q inductor. The inductor consists of silver plated copper etched on a ceramic tube.

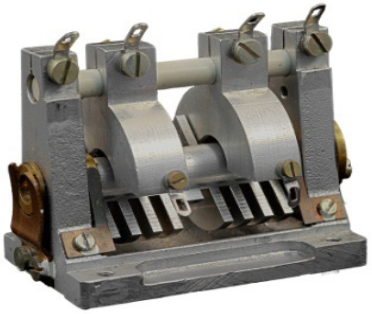

Figure 9 (a) An air- variable capacitor for VHF applications

Figure 9-(b) High-Q inductor

The inductor has one-tab for each turn and is used for a two hundred MHz oscillator. The object of this work is to replace this expensive mechanical inductor by high performance electronic circuits. The air-variable capacitor is already being replaced by tuning diodes. The two can form a resonator as shown in Figure 10. The left resonator is tuned by the capacitor and the right is tuned by a variable inductor.

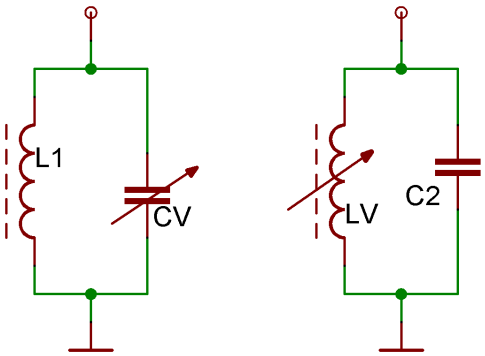

Figure 10. A typical schematic of tank circuit with either a tunable capacitor or tunable inductor.

After the semiconductors replaced radio tubes (valves), reverse biased diodes were used as voltage variable capacitors or varicaps, now called varactors or tuning diodes. At this point, it is necessary to mention that the air variable capacitors had a much higher Q then the coil inductors. Air coils, printed coils and coils with ferrites have large physical dimensions and as the IC based designs take over they do not match the design goal. This changed with the introduction of the tuning diode. Due to leakage currents and loss resistance, varactor Q-values of the order of 300 is considered reasonably high.

Figure 11 shows a varactor diode tuned circuit. The tunable capacitor from Figure 10 is replaced by the tuning diodes. The inductor L2 acts as the RF choke while providing bias. R1 is used to avoid any resonances due to L2. L1 is the resonator inductor. Tuning diodes now used in radios, cell phones and test equipment have acceptably small sizes. Silicon (Si) based tuning diodes are too lossy and have too high capacitance for microwave designs. Gallium arsenide (GaAs) tuning diodes [10] however, are expensive and do not integrate with Si based design. They have to be externally bonded, which is a costly process. The diodes D1 and D2 used at millimeter wave frequencies are fairly expensive, in the vicinity of $20 per device.

A promising and cost-effective solution is to use a fixed capacitor in conjunction with a tunable electronic inductor but this approach has yielded poor noise and dynamic range performance in the past. Based on the circuitry it is more correct to call it an, “active tunable inductor”.

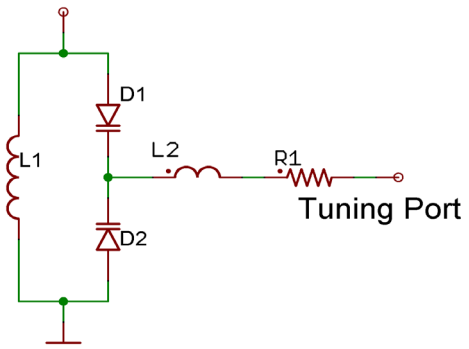

Figure 11 A typical; schematic of the tunable capacitor being replaced by the varactor diodes.

At microwave frequencies, YIG resonator based oscillators are used but are often too big and expensive for practical use. Therefore, it is a logical step to find a solution for a tunable semiconductor inductor that operates well above 5 GHz is inexpensive and not too noisy.

A passive inductor stores energy in the magnetic field while the electronic version constantly supplies energy. For Q multipliers, FET and bipolar transistors were used; the FET fails totally in oscillators because of the flicker corner frequency and only bipolar transistors can be used. If it becomes feasible to design JFEFTs with f_T above 10 GHz then the picture may change.

The purpose of this work is to take the reader through all the associated problems with the active inductor approach, including noise. At the end, a new and workable approach is shown that can solve most of the problems. The new and proven approach [11] uses proper negative feedback to generate a noisy but high-Q inductor and by adding a patented noise feedback technique, very good performance is obtained. Both measurements and CAD simulation results agreed, even with the analytic models and their correlation. The instrument used to measure the result is Rohde and Schwarz phase noise measurement system shown in Figure 14.

The Colpitts oscillator circuit shown in Figure 12 generates an approximate negative resistance of $R = -\frac{Y_{21}^{+}}{\omega^2 C_1 C_2}$, where $Y_{21}{}^{+}$ is the large signal transconductance of the transistor and requires an inductor to function as an oscillator. In this research work, it is shown that this resistance can be generated electronically and with much less noise contribution than achieved in the past. The active inductor by itself will have a negative resistance (-R1), but the one from the capacitive network will dominate.

The promising part about this arrangement is that this inductor value can be electronically tuned over a range of 4:1, resulting in a 2:1 frequency change.

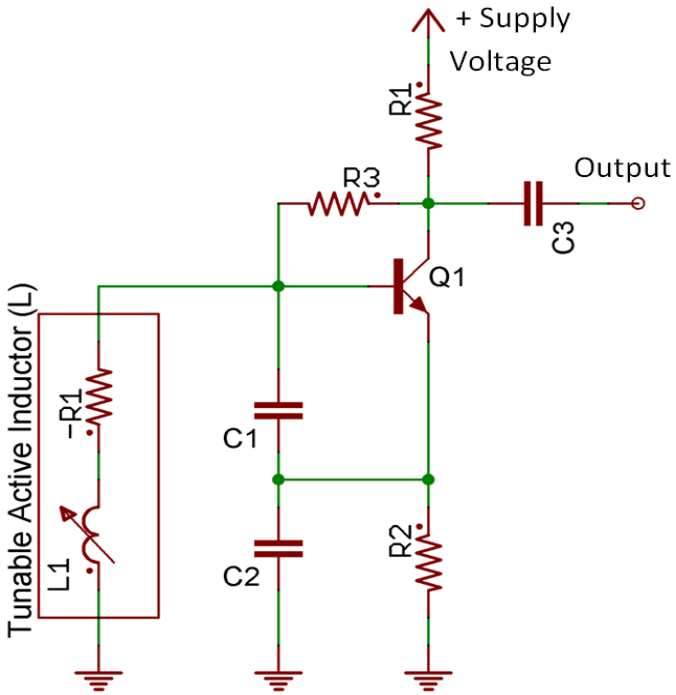

Figure 12. A typical schematic of a tunable active inductor in Colpitts oscillator circuit.

The design of tunable inductor oscillators has been and is the subject of continuous research work in many publications. To a certain degree, tunable inductor oscillators have been designed based on experimental data and experience, and the resulting performance has been measured and published. The notion of an active inductor originated as an active circuit that exhibits the mathematical 90-degree phase shift of voltage leading current as a passive inductor, but is also constrained by power consumption, added noise, and dynamic range. The designer, however, considers it important and useful to start from a set of specifications and then applies a synthesis procedure, which should lead to a successful circuit. Within the scope of this work, the existing literature has been researched to find which successful and optimum active inductor configurations were published. The relevant literature is referenced and commented upon.

This work takes a close look at this circuit, starting with the small-signal performance and then the large-signal performance is discussed in detail (Chapter 1). Since the large-signal parameters deviate further from the small-signal parameters, microwave bipolar transistors are being used rather than field-effect transistors. The oscillators considered in this work are based on commercially available silicon bipolar transistors and silicon germanium transistors. As most designers and companies do not have elaborate and expensive equipment for parameter extraction (to obtain accurate nonlinear models), this concept of synthesis is based on using available data from the manufacturer as well as measurements of large-signal S-parameters using a network analyzer. Modern microwave transistors are very well characterized by the manufacturer up to approximately 6 GHz. Noise data, as well as a SPICE-type Gummel-Poon model data are available. Next is a discussion of tunable inductor oscillator that can be integrated on a monolithic circuit (Chapter 2-3), including noise dynamics and parameter sensitivity characteristics (Chapter 4-5) followed with state-of-the-art and characterization of practical tunable active inductor oscillator circuits for RF& microwave applications (Chapter 6-8).

The core of the work studies different topologies for the realization of tunable active inductor networks. Tunable active inductors have applications in tunable oscillator circuits with additional benefits of integrating onto an IC. Modern microwave circuits are implemented in IC form, where possible. The following is the schematic and layout of a 2 GHz Colpitts GaAs oscillator using spiral inductors (L_1 and L_2) in the circuit layout. These inductors determine most of the die area, (shown in Figure 13), which increases the cost of the device. Planar inductors are also low Q, limiting their usefulness. This thesis explores the possibility of replacing the large spiral inductor with an active device (Bipolar/FET) requiring only fraction of the size. Mode-injection locking is used to improve noise and dynamic range at microwave frequencies. Besides generating an active inductor of the same value and a higher Q factor, the mathematical and experimental noise performance and large signal capabilities will be shown. The low-phase-noise *LC* oscillator design was then investigated. To reach the minimum phase noise design, the integrated inductor design, which is the key for *LC* oscillators, was described. The existing phase noise models were presented and reviewed in Chapter 5. The flicker noise up-conversion mechanisms in *LC* oscillators were analyzed and several phase noise suppression techniques were introduced in Chapter 6. A novel optimization procedure in *LC* oscillator design centered on a new inductance selection criterion was proposed in Chapter 7, which was constrained by power dissipation and chip area. According to a simple physical phase noise model, several closed-form expressions were derived to describe the phase noise generated in the *LC* oscillators.

Various topologies are discussed in chapter-4. The measurement of large-signal parameters of the transistor are shown in Chapter 1. Following the mathematical solution of the problem,

tunable inductor oscillators have been built using discrete components for validation of the approach and were measured (Chapters 6-8). In this research work, an injection-locked active inductor topology that can partially or fully overcome these effects, especially for oscillator applications is proposed. There is a good agreement between measurement, analysis and synthesis. Excellent agreement is also found using harmonic-balance-based commercial simulators (Ansoft and Agilent ADS).

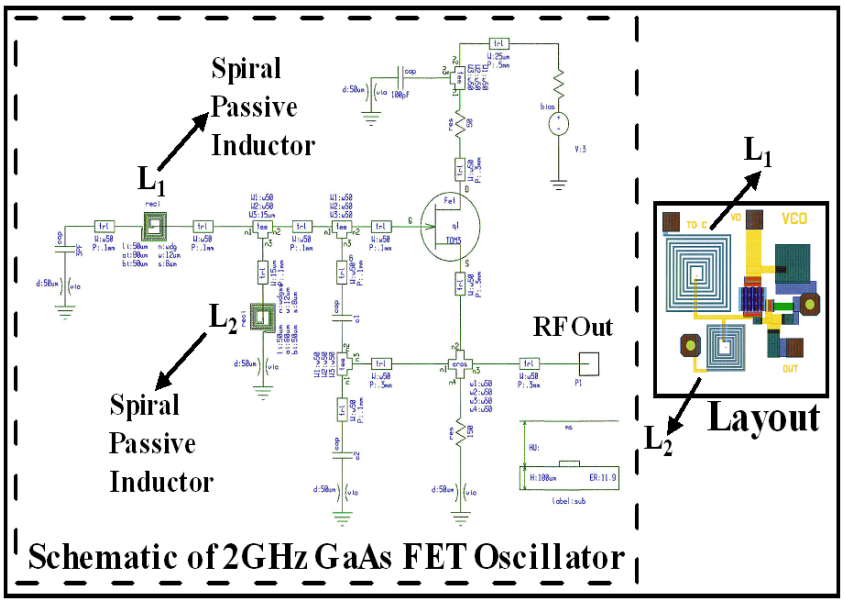

Fig.13. A typical schematic and layout of a 2 GHz Colpitts GaAs oscillator using spiral inductors (L_1 and L_2)

First results were shown in papers [12]-[21], and Synergy Microwave Corp. has submitted a US patent application, which is in the final stage of processing.

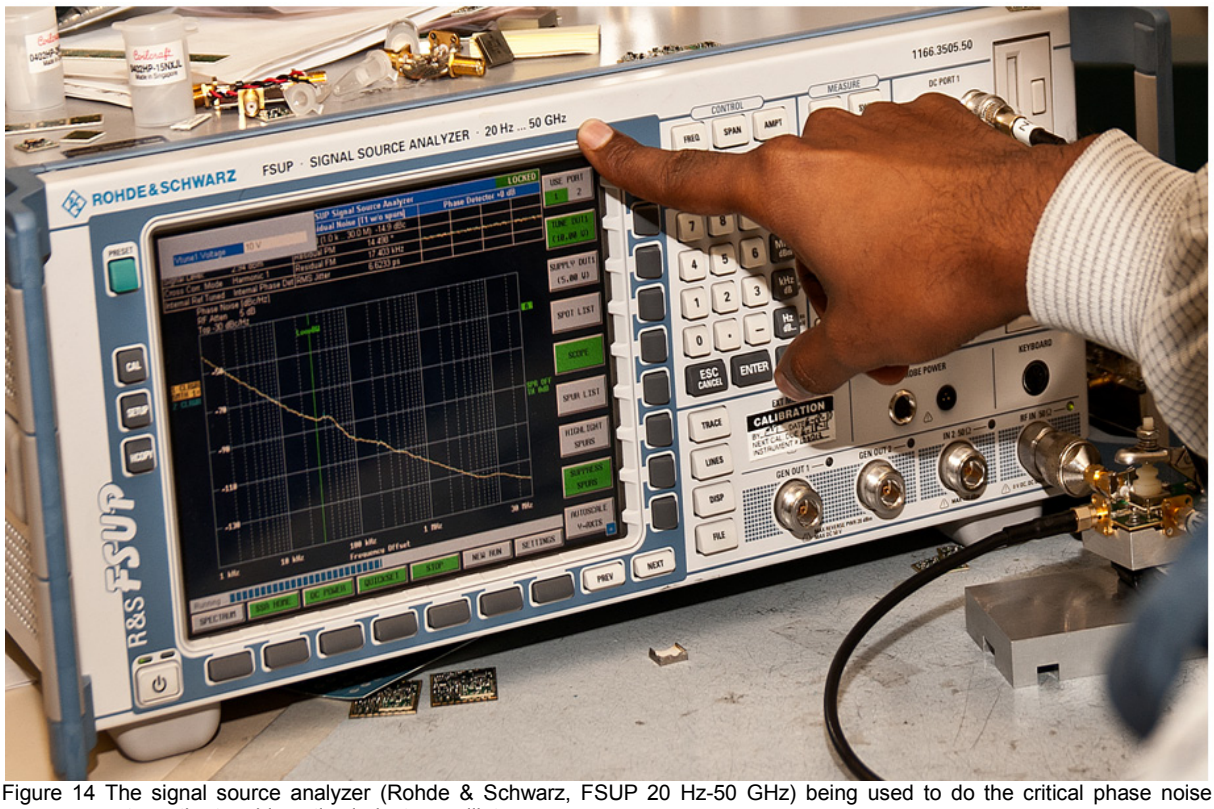

Figure 14 The signal source analyzer (Rohde & Schwarz, FSUP 20 Hz-50 GHz) being used to do the critical phase noise measurements on the tunable active inductor oscillators.

Figure 14 shows the signal source analyzer (Rohde & Schwarz, FSUP 20 Hz-50 GHz) being used to do the critical phase noise measurements on the tunable active inductor oscillators.

This work finishes by stating future possibilities and the application of synthseized active inductor in impedance matching networks, tunable filters, phase shifters, amplifiers, and mixer circuits. The active inductor has its limitations but shows a roadmap towards integrated and cost-effective solutions for current and later generation wireless communication systems.

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Chapter 1

1. 1 Introduction

The need for oscillators has existed for a long time [1]-[43]. The first time it became an important issue was when Maxwell's equations were to be experimentally proven. Heinrich Hertz made the first known oscillator. He used a dipole as the resonator and a spark gap generator as the oscillator circuit as shown in Figure 1-1.

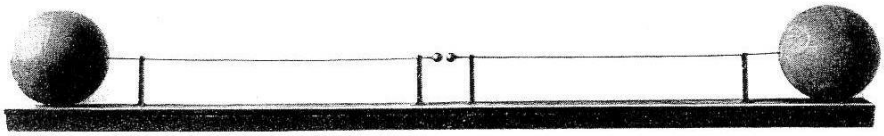


Figure 1-1 Original dipole made by Heinrich Hertz in 1887 using balls at the end to form a capacitive load (Deutsches Museum, Munich).

The spark gap oscillator changes AC or DC power into a spark, which is energy rich and wide band. The dipole then takes the energy at the resonant frequency and radiates it. Other discharges such as lightning with short pulse duration generate RF power from a few tens of KHz to hundreds of MHz.

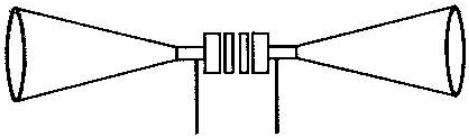


Figure 1-2 Dipole formed by two conical resonators with spark gap (1914)

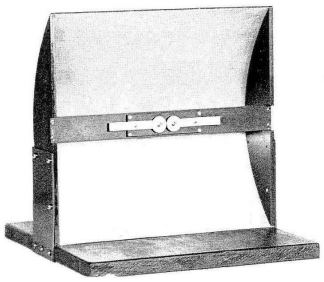


Figure 1-3 Dipole oscillator after Ludenia placed in a parabolic mirror to increase efficiency (1929).

Figures 1-2 and 1-3 show additional examples of early oscillators. The pictures in this chapter are taken from [6, pp. 1-4]. Today, oscillators are used in test and measurement equipment and communication equipment. The largest group of users is for the use of two-way radios and "handies" (cell phones). In this monograph, high performance and high volume applications are considered, but not the mass-market applications. External resonators rather than monolithic resonators are considered as high-quality phase noise requirements have only been met using external resonators so far.

For these applications, oscillators have to meet a variety of specifications, which affect the quality of the operational system. An important feature is the stability of the oscillator (low phase noise) and its freedom from spurious signals and noise. While the oscillator is almost always used as a voltage-controlled oscillator (VCO) in a frequency synthesizer system, its free-running noise performance outside the loop is still extremely important and solely determined by the oscillator.

An oscillator is a circuit that consists of an amplifier and a resonator. The feedback circuit takes a portion of the energy from the output of the amplifier and feeds it into the resonator to compensate its losses. The amplitude of the oscillator depends on the DC input power and the active device in the amplifier. A small portion of the energy is used to sustain oscillation and most of the RF power is available to be withdrawn at the output to be further amplified and used. The resonator mostly determines the frequency of the oscillator.

The use of negative resistance devices Such as Gunn diodes, tunnel diodes and IMPATT diodes have become attractive at millimeter wave frequencies but unattractive at RF and microwave frequencies as they are single terminal devices and require complicated biasing, heat sinking and decoupling. A key factor for oscillators is the phase noise, which describes the noise of an oscillator at frequency offset from the carrier for a given tuning range and power.

Unfortunately, oscillators do not generate perfect signals. The various noise sources in and outside of the active device (transistor) modulate the VCO, resulting in energy or spectral distribution on both sides of the carrier due to modulation and frequency conversion. AM and FM noise is expressed as the ratio of noise power in a 1 Hz bandwidth divided by the output power. It is measured at frequency offset of the carrier. Figure 1-4 shows a typical measured phase noise plot of a high Q oscillator using a ceramic resonator. The x-axis is the frequency offset from the carrier on a logarithmic scale. The y-axis is the phase noise in dBc/Hz

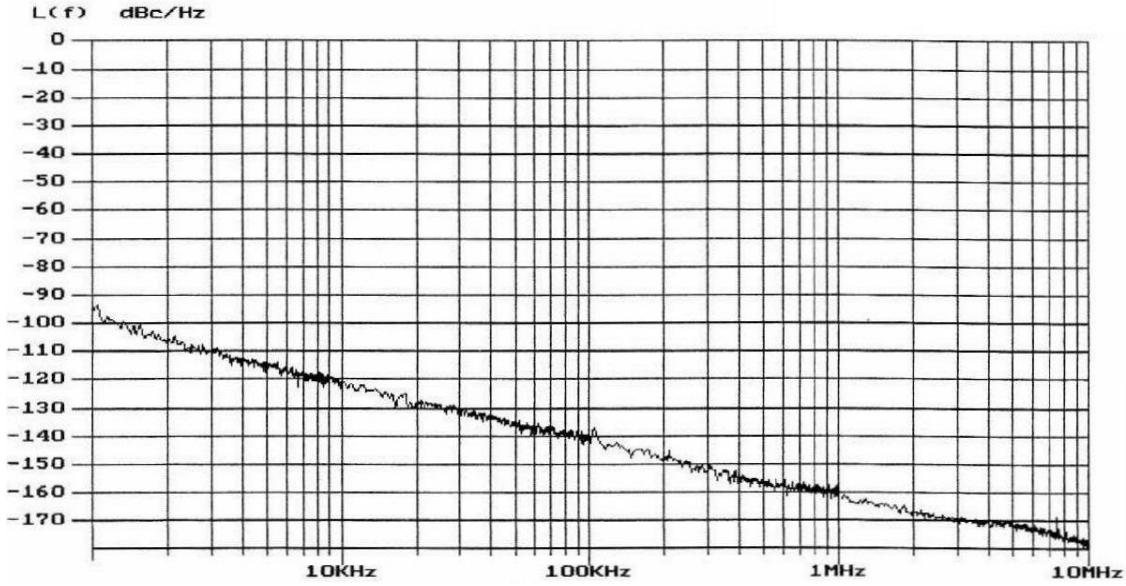


Figure 1-4 A typical measured phase noise plot of a 2488 MHz ceramic resonator-based oscillator with a small tuning range

The stability or phase noise of an oscillator can be determined in the time or frequency domain. Phase noise is a short-term phenomenon and has various components. Figure 1-5 shows the typical illustration of the stability and phase noise in the time and frequency domain. The major noise contributors are thermal noise, Schottky noise and the flicker noise from the active device. Flicker noise depends on the transistor type and its biasing. The noise contribution from the resonator is mainly thermal noise. The minimum phase noise is at far offsets from the carrier, the best number being $P_{out}(dBm) - kT_o\ (-174dBm) + NF$ (large-signal noise figure of the oscillator transistor in dB); all per 1Hz bandwidth.

In the case of a lossy (noisy) resonator (LC resonator), the operating Q is much less than 200 and therefore the far off noise does not get very much attenuated. At very high frequencies, above 150 MHz the inductor (L) dimension gets very small and violates the length/diameter > 3 rule for optimum realization. The following list provides the equations for the various standard inductors based on wound coils and printed inductors [Table1-1].

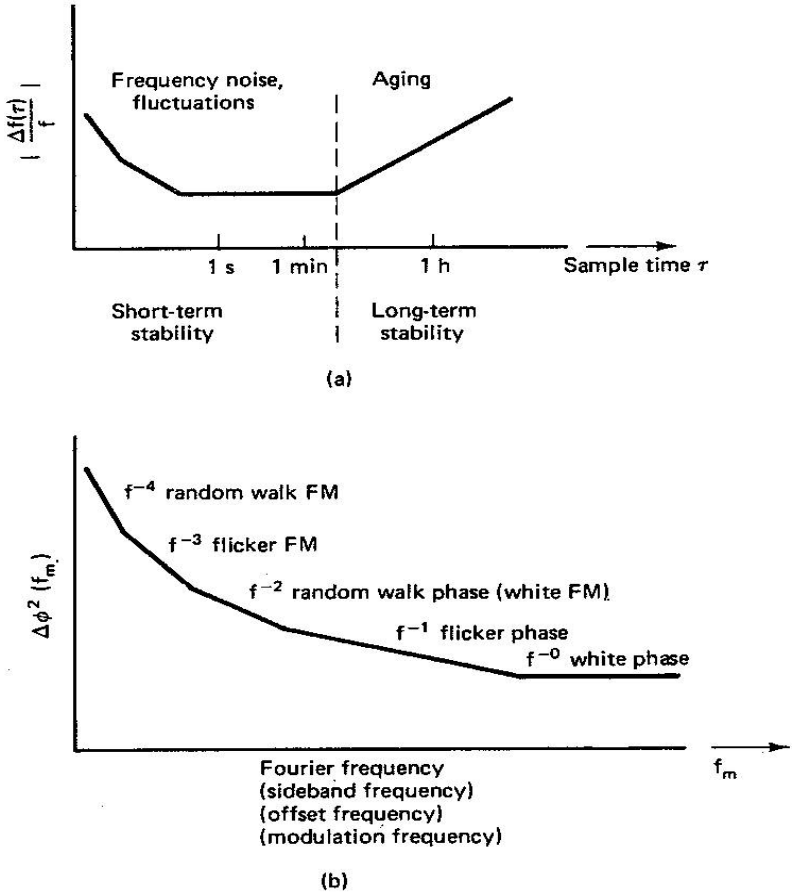


Figure 1-5 A typical characterization of the noise sideband in the time and frequency domain and its contributions: (a) time domain and (b) frequency domain. Note that two different effects are considered, such as aging in (a) and phase noise in (b).

For Frequencies above 400 MHz resonators are built around helical resonators, ceramic resonators (CR), dielectric resonators (DR), or resonant transmission lines (microstrip or coplanar waveguides) to name a few. Constraints on high-Q resonators used in high performance VCO circuits are particularly demanding, and a MMIC integrable solution has been the dream for decades [14]-[19]. In general, a high Q resonator element is required in order to achieve low phase noise characteristics in a VCO, but the realization of planar high-Q resonators is difficult due to the higher loss characteristics of the resonator at high frequency.

The DR (Dielectric resonator) offers high Q factor, and is also well known for high spectral purity signal sources at radio and microwave frequencies. However, a VCO employing a DR has a narrow tuning range, is sensitive to vibration, costly, and not suited for current fabrication process in MMIC technology.

Table 1-1: Common formulae for calculating the theoretical inductance of several inductor constructions

Construction	Formula	Dimensions
Cylindrical coil	$L = \frac{\mu_0 K N^2 A}{l}$	• L = inductance in Henries (H) • μ_0 = permeability of free space = $4\pi \times 10^{-7}$ H/m • K = Nagaoka coefficient • N = number of turns • A = area of cross-section of the coil in square metres (m^2) • l = length of coil in metres (m)
Straight wire conductor	$L = l\left(\ln\frac{4l}{d} - 1\right) \cdot 200 \times 10^{-9}$	• L = inductance (H) • l = length of conductor (m) • d = diameter of conductor (m)
	$L = 5.08 \cdot l\left(\ln\frac{4l}{d} - 1\right)$	• L = inductance (nH) • l = length of conductor (in) • d = diameter of conductor (in)
Short air-core cylindrical coil	$L = \frac{r^2 N^2}{9r + 10l}$	• L = inductance (μH) • r = outer radius of coil (in) • l = length of coil (in) • N = number of turns
Multilayer air-core coil	$L = \frac{0.8 r^2 N^2}{6r + 9l + 10d}$	• L = inductance (μH) • r = mean radius of coil (in) • l = physical length of coil winding (in) • N = number of turns • d = depth of coil (outer radius minus inner radius) (in)
Flat spiral air-core coil	$L = \frac{r^2 N^2}{(2r + 2.8d) \times 10^5}$	• L = inductance (H) • r = mean radius of coil (m) • N = number of turns • d = depth of coil (outer radius minus inner radius) (m)
	$L = \frac{r^2 N^2}{8r + 11d}$	• L = inductance (μH) • r = mean radius of coil (in) • N = number of turns • d = depth of coil (outer radius minus inner radius) (in)
Toroidal core (circular cross-section)	$L = \mu_0 \mu_r \frac{N^2 r^2}{D}$	• L = inductance (H) • μ_0 = permeability of free space = $4\pi \times 10^{-7}$ H/m • μ_r = relative permeability of core material • N = number of turns • r = radius of coil winding (m) • D = overall diameter of toroid (m)

One cost-effective and alternative way to eliminate the DR is to use a printed resonator, which is appropriate for current semiconductor manufacturing processes. However, phase noise characteristics of a VCO using a printed resonator is inferior to that of the VCO using a DR (DR Q factor is much higher than the printed resonator) [12]-[35]. Planar resonators, such as ring, hairpin, spiral, and coupled resonators, are implemented easily in practical MMIC fabrication process at the cost of large size and low *Q* in comparison to the commercially available DR [35]-[40]. Figure 1-6 shows the typical DR for giving brief insights about the possible resonant condition for given parameters (L, a, ε_r), where L is the length of DR, a, is the radius, and ε_r is the relative permittivity. Figure 1-7a shows the typical high performance DRO circuit using the DR in Push-Push configuration. It offers low phase noise but limited in tuning and poor sub-harmonic rejection [16]-[18]. As depicted in Figure 1-7b, the exact placement of the DR disc between the two parallel microstripline is critical, and slight variation may lead to higher harmonics and poor phase noise performance.

In addition to this, DR resonant frequencies may differ from the measured result due to the slight variation in temperature that causes problems in integration and mass production. The above problems limit the utility of DRs and moreover, the frequency drift is not a straightforward function of the temperature changes (due to different thermal expansion coefficients for the cavity and the dielectric puck. To overcome the above problems and reduce the thermal sensitivity of the DRO, temperature compensation and frequency locking using a PLL (phase locked loop) circuit are needed. However, is still not a cost-effective solution or suitable for integration.

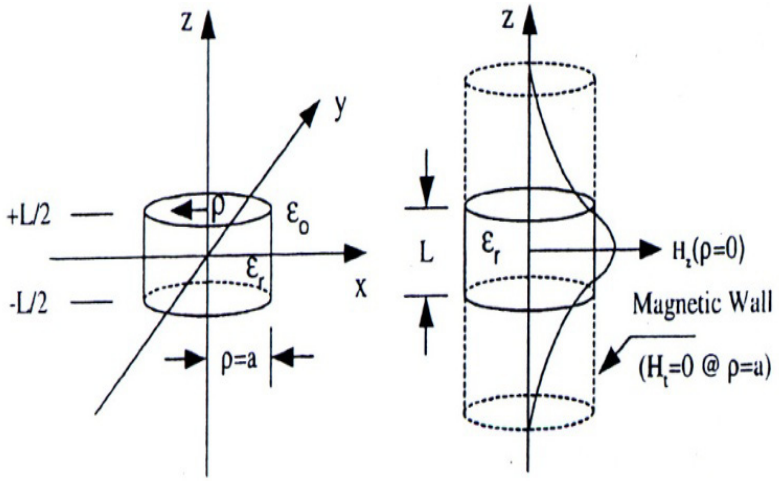


Figure.1-6. A typical DR $TE_{01\delta}$ mode and H_z field distribution

Standard integrated circuits are planar circuits, so only those resonators having a planar structure are suitable in a MMIC/RFIC environment. But integrable planar resonators lack sufficient Q (quality factor) and therefore are a limiting factor of the VCO's phase noise performance. The reason for the poor phase noise performance is due to the slow rate of phase change, and associated group delay characteristics of the resonator over the desired tuning range.

Recent publications explore the possibility of replacing the DR and techniques to improve the Q factor of the planar resonators for VCO applications, which have advantages for low cost, low phase hits, wide tuning range, and suited for on-chip realization [12]-[40].

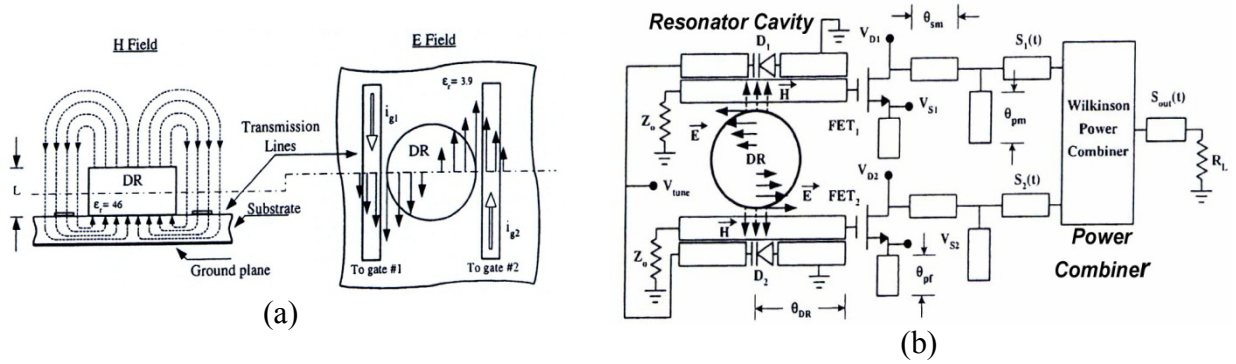


Figure 1-7. (a) DR microstrip coupling electromagnetic field distribution, (b) Tunable 12 GHz Push-Push DRO circuit

The low temperature co-fired ceramic (LTCC) resonator (Figure 1-8) is a possible alternative. It exhibits high-Q factor, and is amenable for integration in MMIC process, but is very difficult to integrate in a compact system configuration [14]. Printed helical resonators at microwave frequencies exhibit high Q factor for a given size, and are a strong contender for low phase noise VCO applications. Figure 1-9 depicts a typical 3-D layout of the inductively coupled helical resonator with two ¾ turn loops connected together using a via hole.

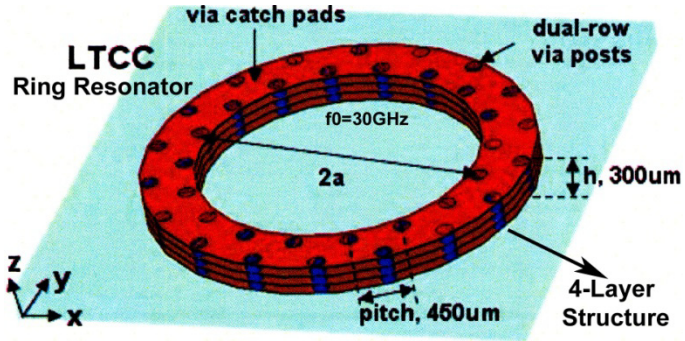


Figure 1-8. Layout of LTCC resonators (resonators are embedded in multilayer LTCC blocks for implementing integrated system in package)

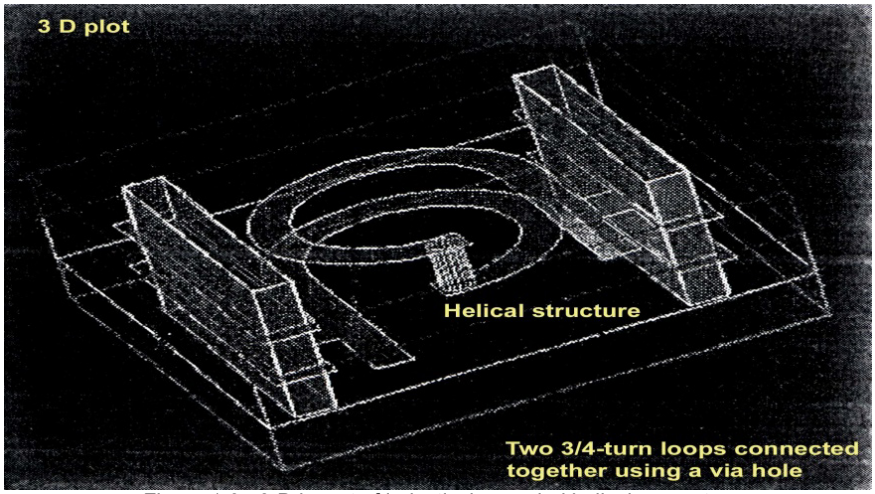


Figure 1-9. 3-D layout of inductively coupled helical resonator

Edward [37], proposed a novel high-Q compact multilayer integrable printed helical resonator that offers optimum Q_L/Q_0 ratio (loaded quality factor/unloaded quality factor) for minimum phase noise for a given VCO topology. Figure 1-10 illustrates the integrable planar helical resonator coupled to coplanar waveguide (CPW) line for high performance VCO applications [6]. The drawbacks of the reported [37]-[38] high-Q helical resonators are limited tuning capability for a given phase noise, size, and cost requirement.

For low cost, broadband tunability, and integrable solutions, a new approach is discussed, which is based on the tunable active inductor where total dimensions of the resonator are unaltered while exhibiting wider tuning and improved Q factor. The solution is reconfigurable and reduction in the number of manufacturing process steps.

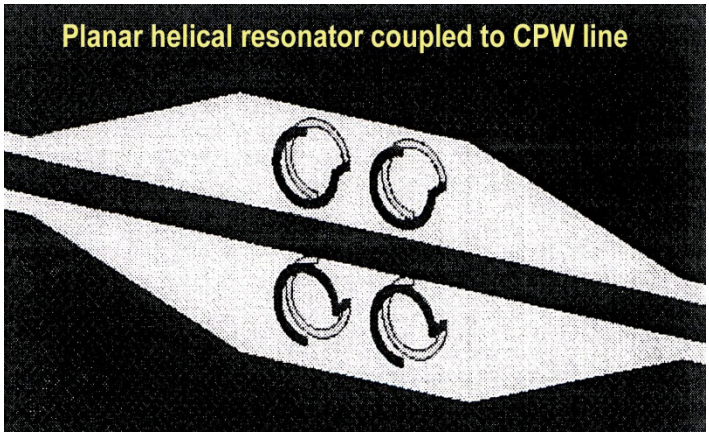


Figure 1-10 Typical planar helical resonator coupled to CPW line

1. 2 Resonator Choice

1.2.1 LC Resonator

Extensive research work is being done in the area of resonator networks such as passive and active resonator for the applications as the frequency selective element in voltage controlled oscillator applications.

Figure 1-11 shows the circuit diagram of a simple resonator. The coupling to the port is accomplished by a very small capacitor. The lumped resonator consists of a lossy 2pF capacitor and a lossy 1.76nH inductor with a 0.2pF parasitic capacitor. The capacitor has a lead inductor of 0.2nH and 0.2 Ω losses. Likewise, the inductor has the same value loss resistor. To measure the operating Q, this combination is attached to a network analyzer, which determines S_{11}. The operating Q is calculated by dividing the center frequency by the 3 dB bandwidth of S_{11}. The quality factor Q is defined as the ratio of stored energy to the dissipated energy. If there is no energy loss, the Q is infinite.

To determine the operating Q of the circuit, let us calculate the Q of the individual branches representing the resonator. The total Q of the circuit can be calculated by combining the two individual Q values using the equation.

$$Q = \frac{Q_1 \times Q_2}{Q_1 + Q_2} \tag{1.1}$$

$Q_1 = 2 \times \pi \times 2.4\ \text{GHz} \times 1.76nH/0.2\Omega = 133$, $Q_2 = 165$, $Q = 73$

The reason for the low Q is due to the 0.2Ω loss resistor. It should be possible to reduce this by more than a factor of two.

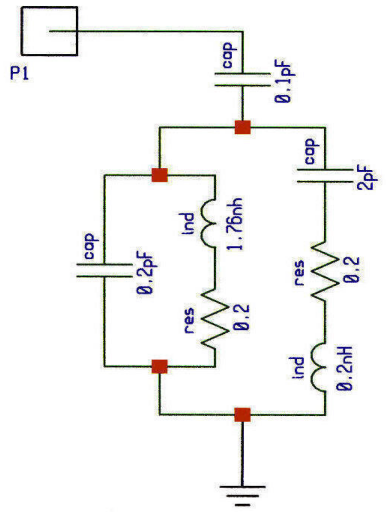


Figure 1-11 A typical circuit diagram of a parallel tuned circuit with lossy components and parasitics loosely coupled to the input

1.2.2 Transmission Line Resonator

The same parallel-tuned circuit shown in Figure 1-11 can be generated by using a printed transmission line instead of the lumped inductor and maintain the same capacitance. This is shown in Figure 1-12. Since the transmission line has losses due to the material, they need to be considered. It is not practical to calculate these by hand, but rather use a CAD program (Nexxim, ADS 2009, AWR, CST) which does this accurately. These references describe how to get the Q factor from S_{11} measurements. The Q can be determined from the 3dB bandwidth $\left(\frac{\Delta f}{f_0}\right)$ shown in Figure 1-13 and was determined to be 240.

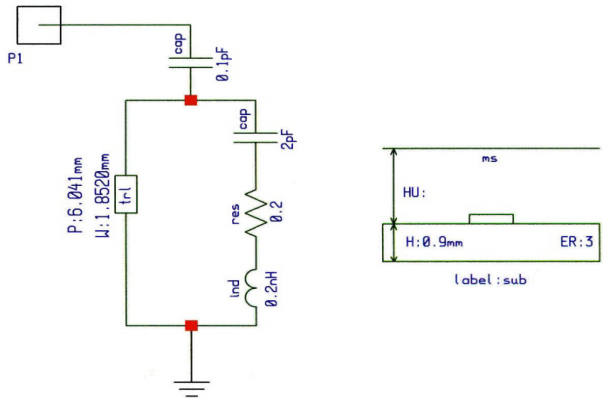


Figure 1-12 A typical 2.4 GHz resonator using both lumped and distributed components (physical dimensions are given).

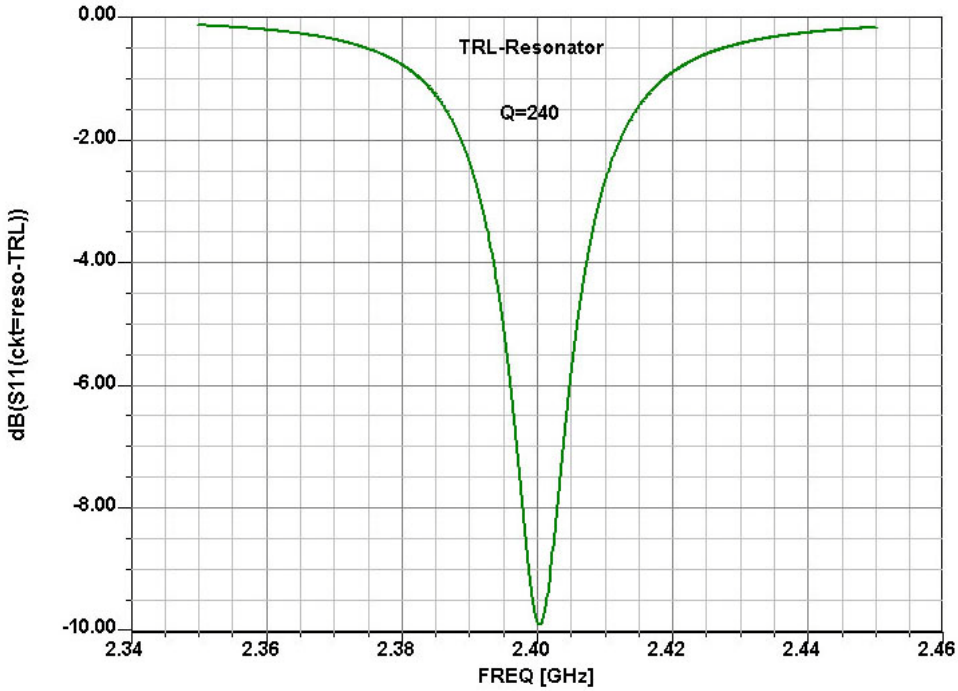


Figure 1-13 A typical CAD simulated reflection coefficient S_{11} to determine the operating Q. Since this material has fairly high losses, an operating Q of only 240 was achieved.

This is also valid if the Y or Z parameters are used. This is a typical value for a microstrip resonator. Values up to 300 are possible if the appropriate layout and material is used.

1.2.3 Integrated Resonator

The circuit of Figure 1-12 can be generated not only using printed circuit board material, but also in GaAs or silicon. Figure 1-14 shows the schematic of a parallel tuned circuit using a rectangular inductor and an inter-digital capacitor.

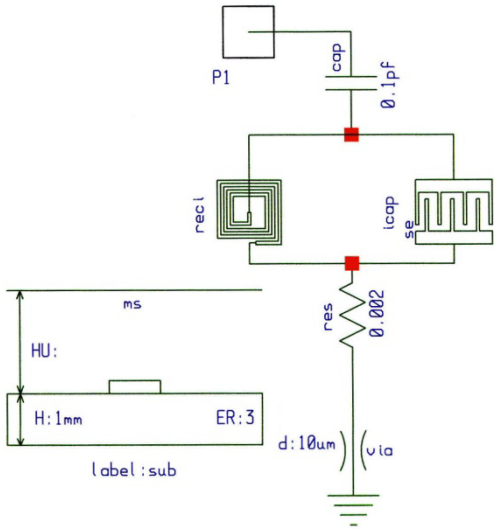


Figure. 1-14 Parallel tuned circuit using a rectangular inductor (spiral could also be used) and an interdigital capacitor. If implemented on GaAs or silicon, it exhibits low Q.

The ground connection is achieved through a via. At 2.4 GHz, the number of turns and size of the inductor would be significant. The same applies to the capacitor. This arrangement should be reserved for much higher frequencies, above 5 GHz. The inductor losses, both in GaAs and silicon, are substantial and this case is only shown for completeness. For optimum performance, wherever possible an external resonator should be used.

Referring to integrated resonators, a high Q resonator consisting of two coupled inductors has been developed. Figure 1-15 shows a three dimensional array where the two coupled resonators are easily identifiable. One side of the resonator is connected to ground through a via.

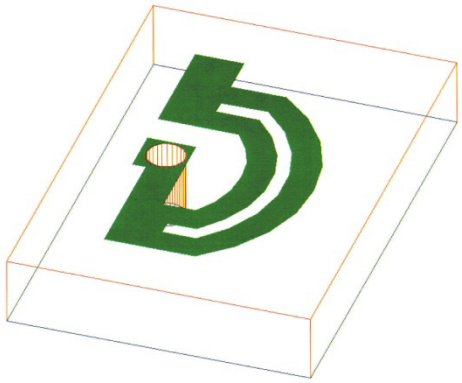


Figure 1-15 A typical 3-D view of the coupled resonator (patented).

The 3-D layout can be reduced to a two-dimensional layout as shown in Figure 1-16, which gives further details about the resonator. The resonator analysis was done using Ansoft Designer (now known as Ansys Nexxim), specifically the 2.5-D simulator.

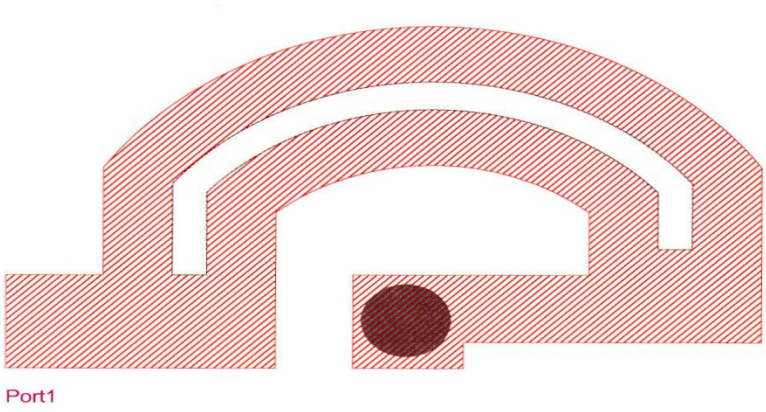


Figure. 1-16 2-D view of the coupled microstrip resonator (patented)

A more conventional resonator analysis can be performed, using the S-parameters obtained from the structure. Figure 1-17 shows the electrical equivalent circuit of the coupled microstrip line resonator. Finally, the S_{11} resonant curve is analyzed. The curve seen in Figure 1-18 shows a coupled micro-stripline resonator response, and the resulting Q is determined to be 560. This structure and application is covered by U.S. patents 7,088,189 B2 and 7,292,113 B2. This type of resonator, as shown in Figure 1-16, plays a major role in the design of ultra wide-band oscillators.

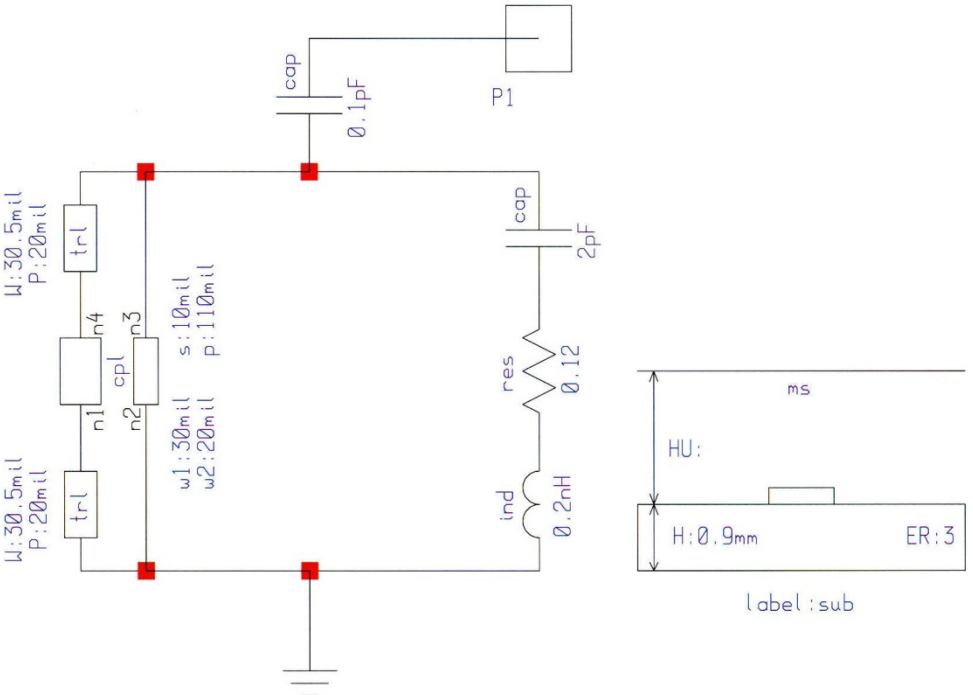


Figure. 1-17 Electrical equivalent of the coupled microstrip line resonator

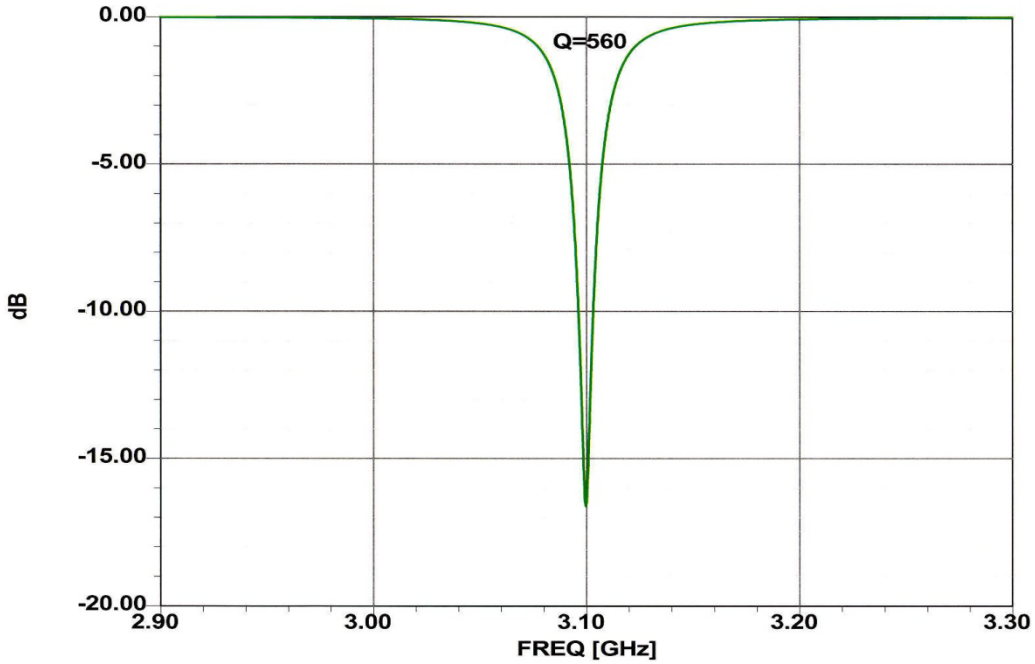


Figure. 1-18 Frequency response of the coupled microstrip line resonator.

Figure 1-19 shows the typical circuit layout of a coupled resonator oscillator as it is built on a multi-layer printed circuit board. It is a 1.5-4.5GHz multi-octave, low-noise oscillator, and this was achieved in our patented approach, US copyright registration No.VAU 603984 [6]. Besides the coupled resonator, which determines the resonant frequency, there is an additional resonator used for noise filtering. Figure 1-20 shows the achievable phase noise for this oscillator.

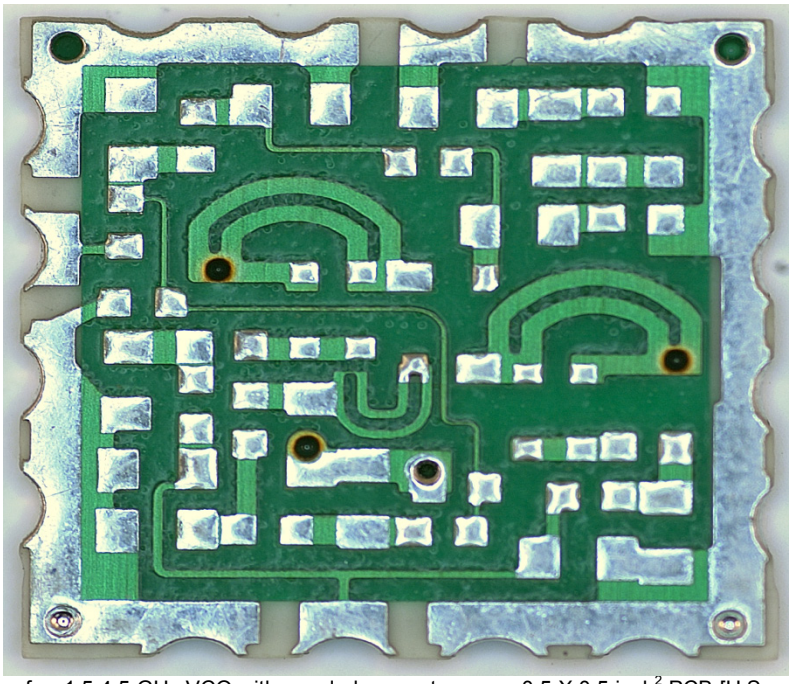


Figure 1-19 An example of a 1.5-4.5 GHz VCO with coupled resonators on a 0.5 X 0.5 inch^2 PCB [U.S. patent Nos. 7,088,189 B2 and 7,292,113 B2]

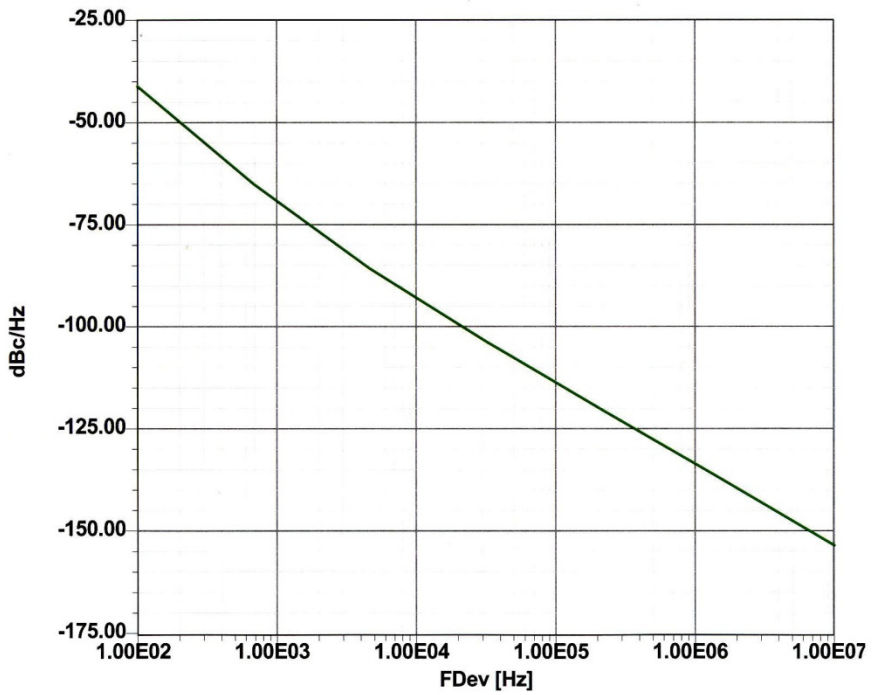


Figure 1-20 Predicated (simulated) phase noise of the oscillator layout shown in Figure. 1-19

However, these resonators use a large area and the purpose of this research work is to develop an *Active Inductor*, not a Q multiplier. Oscillators operate under large-signal conditions. Under large-signal conditions, the RF currents and voltages are of the same magnitude as the DC values. The most accurate result will be obtained by switching from linear to nonlinear analysis.

1.3 Large Signal S-Parameter Analysis

The description of linear, active or passive 2-ports can be explained in various forms. In the early days *Z*-parameters were commonly used which then were replaced by the *Y*-parameters. *Z*-parameters are open-ended measurements and *Y*-parameters are short circuit measurements relative to the output or input depending on the parameter. In reality, however, the open circuit condition does not work at high frequencies because it becomes capacitive and results in erroneous measurements. The short-circuit measurements also suffer from non-ideal conditions as most "shorts" become inductive. Most RF and microwave circuits, because of the availability of 50Ω coaxial cables, are now using 50Ω impedances. Component manufacturers are able to produce 50Ω termination resistors which maintain their 50Ω real impedance up to tens of GHz (40 GHz). The 50Ω system has become a defacto standard. While the *Z*- and *Y*-parameter measurements were based on voltage and currents at the input and output, the *S*-parameters refer to forward and reflected power.

1.3.1 Definition

For low frequency applications, one can safely assume that the connecting cable from the source to the device under test or the device under test to the load plays no significant role. The wavelength of the signal at the input and output is very large compared to the physical length of the cable. At higher frequencies, such as microwave frequencies, this is no longer true. Therefore, a measuring principle was founded that would look at the incoming and the outgoing power waves at the input and the output port. The following is a mathematical explanation of the *S*-parameters. This follows the definitions of [6] as outlined by Hewlett-Packard.

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{1-2}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{1-3}$$

or, in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1-4}$$

where, referring to Figure 1-21:

a_1 = (incoming signal wave at Port 1)
b_1 = (outgoing signal wave at Port 1)
a_2 = (incoming signal wave at Port 2)
b_2 = (outgoing signal wave at Port 2)
E_1, E_2 = electrical stimuli at Port 1, Port 2

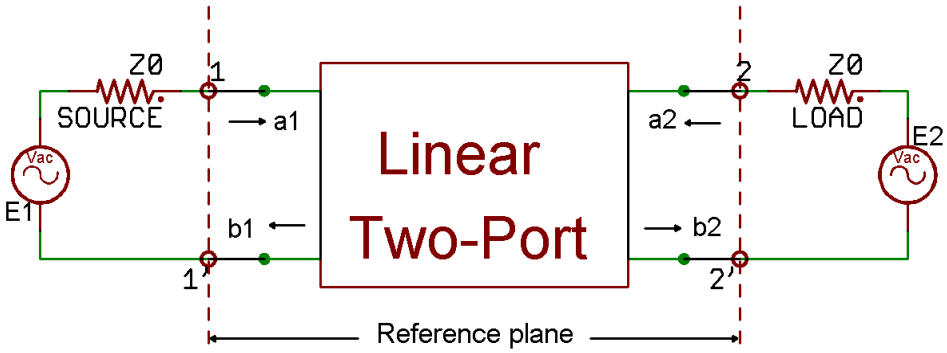


Figure 1-21 Two-port *S*-parameter definition.

From Figure 1-21 and defining linear equations, for $E_2 = 0$, then $a_2 = 0$, and (skipping through numerous rigorous steps):

$$\begin{aligned} |S_{11}| &= \frac{b_1}{a_1} \\ &= \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}}\right]^{1/2} \\ &= \frac{\text{Reflected Voltage}}{\text{Incident Voltage}} \\ &= \text{Input Reflection Coefficient} \end{aligned} \tag{1-5}$$

$$\begin{aligned} |S_{21}| &= \frac{b_2}{a_1} \\ &= \left[\frac{\text{Outgoing Output Power}}{\text{Incoming Input Power}}\right]^{1/2} \\ &= \left[\frac{\text{Output Power}}{\text{Available Input Power}}\right]^{1/2} \\ &= \left[\text{Foward Transducer Gain}\right]^{1/2} \end{aligned} \tag{1-6}$$

or, more precisely in the case of S_{21}:

$$\text{Forward Transducer Gain} = G_{TF} = |S_{21}|^2 \tag{1-7}$$

$$Z_i = Z_o \tag{1-8}$$

similarly at Port 2 for E_1=0, then a_1=0, and

$$S_{22} = \frac{b_2}{a_2} = \text{Output Reflection Coefficient} \tag{1-9}$$

$$S_{12} = \frac{b_1}{a_2} = \left[\text{Reverse Transducer Gain}\right]^{1/2} \tag{1-10}$$

$$G_{TR} = |S_{12}|^2 \tag{1-11}$$

Since many measurement systems display *S*-parameter magnitudes in decibels, the following relationships are particularly useful:

$$|S_{11}|_{\text{dB}} = 10\log|S_{11}|^2 = 20\log|S_{11}| \tag{1-12}$$

$$|S_{22}|_{\text{dB}} = 20\log|S_{22}| \tag{1-13}$$

$$|S_{21}|_{\text{dB}} = 10\log|S_{21}|^2 = 20\log|S_{21}| = 10\log|G_{\text{TF}}| = |G_{\text{TF}}|_{\text{dB}} \tag{1-14}$$

$$|S_{12}|_{\text{dB}} = 10\log|S_{12}|^2 = 20\log|S_{12}| = 10\log|G_{\text{TR}}| = |G_{\text{TR}}|_{\text{dB}} \tag{1-15}$$

1.3.2 Large Signal S-Parameter Measurements

Assume S_{11} and S_{21} are functions only of incident power at port 1 and S_{22} and S_{12} are functions only of incident power at port 2. Note: the plus (+) sign indicates the forward voltage wave and the minus (-) sign would be the reflected voltage wave.

$$S_{11} = S_{11}\left(\left|V_1^+\right|\right) \qquad S_{12} = S_{12}\left(\left|V_2^+\right|\right) \tag{1-16}$$

$$S_{21} = S_{21}\left(\left|V_1^+\right|\right) \qquad S_{22} = S_{22}\left(\left|V_2^+\right|\right) \tag{1-17}$$

The relationship between the traveling waves now becomes

$$V_1^- = S_{11}(V_1^+)V_1^+ + S_{12}(V_2^+)V_2^+ \tag{1-18}$$

$$V_2^- = S_{21}(V_1^+)V_1^+ + S_{22}(V_2^+)V_2^+ \tag{1-19}$$

Measurement is possible if V_1^+ is set to zero,

$$S_{12}(V_2^+) = \frac{V_1^-(V_2^+)}{V_2^+} \tag{1-20}$$

Check the assumption by simultaneous application of V_1^+ and V_2^+

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} F_1(V_1^+, V_2^+) \\ F_2(V_1^+, V_2^+) \end{bmatrix} \tag{1-21}$$

If harmonics are neglected, a general decomposition is

$$\begin{bmatrix} V_1^-(V_1^+, V_2^+) \\ V_2^-(V_1^+, V_2^+) \end{bmatrix} = \begin{bmatrix} S_{11}(V_1^+, V_2^+) & S_{12}(V_1^+, V_2^+) \\ S_{21}(V_1^+, V_2^+) & S_{22}(V_1^+, V_2^+) \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2 + \end{bmatrix} \tag{1-22}$$

If the signal from the signal generator is increased in power, it essentially has no impact on passive devices until a level of several hundred watts is reached where intermodulation distortion products can be created due to dissimilar alloys. However, active devices, depending on the DC bias point, can only tolerate relatively low RF levels to remain in the linear region.

In the case of the oscillator, there is a large RF signal, that is, a large voltage and current, imposed on the DC voltage/current. Assuming an RF output power from 0dBm to 10dBm, and

assuming 10-15 dB gain in the transistor, the RF power level driving the emitter/source or base/gate terminal is somewhere in the vicinity of –15dBm.

An RF drive of –15dBm will change the input and output impedance of the transistor, even if the transistor operates at fairly large DC currents. It is important to note that the input and output impedances of field-effect transistors are much less RF voltage-dependent or power-dependent than the bipolar transistor. The generation of "large-signal *S*-parameters" for bipolar transistors is, therefore, much more important than for FETs.

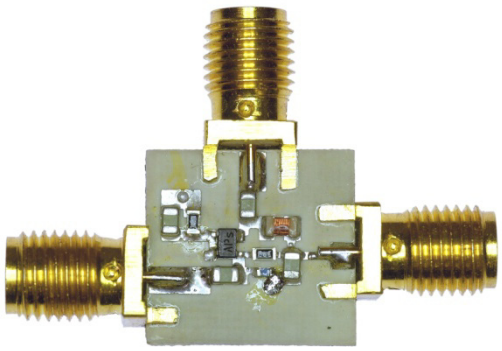


Figure 1-22 Test fixture to measure large signal *S*-parameters. A proper de-embedding has been done [6].

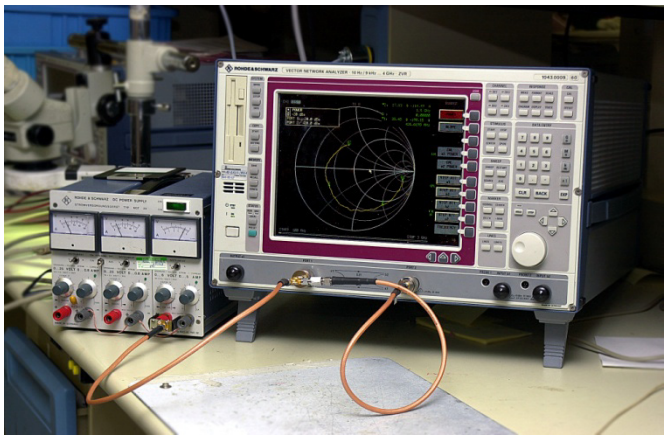


Figure 1-23 Rohde & Schwarz 3 GHz network analyzer to measure the large-signal *S*-parameters at different drive levels [6].

Figure 1-22 shows the test fixture, which was used to measure, the large-signal *S*-parameters for the device under test (DUT). The test fixture was calibrated to provide 50Ω to the transistor leads. The test set-up shown in Figure 1-23 consists of a DC power supply and a network analyzer for combined *S*-parameter measurements. The R&S ZVR network analyzer, as shown in Figure 1-23, was chosen because its output power can be varied between +10dBm to –60dBm. This feature is necessary to perform these measurements. The picture shows that the actual test system is very simple, but unfortunately, very expensive.

Currents and voltages follow Kirchhoff's law in a linear system. A linear system implies that there is a linear relationship between currents and voltages. All transistors, when driven at larger levels show nonlinear characteristics. The FET shows a square law characteristic, while the bipolar transistor has an exponential transfer characteristic. The definition of *S*-parameters in large-signal environment is ambiguous compared to small-signal *S*-parameters. When driving an active device with an increasingly higher level, the output current consists of a DC current and RF currents: the fundamental frequency and its harmonics. When increasing the drive level, the harmonic content rapidly increases. S_{12}, mostly defined by the feedback capacitance, now reflects harmonics back to the input. If these measurements are done in a 50Ω system, which has no reactive components, then we have an ideal system for termination. In practical applications, however, the output is a tuned circuit or matching network, which is frequency selective. Depending on the type of circuit, it typically presents either a short circuit or an open circuit for the harmonic. For example, say the matching network has a resonant condition at the fundamental and second harmonic frequency or at the fundamental and third harmonic frequency

(quarter wave resonator). Then a high voltage occurs at the third harmonic, which affects the input impedance, and therefore, S_{11} (Miller effect).

This indicates that *S*-parameters measured under large-signal conditions in an ideal 50Ω system may not correctly predict device behavior when used in a non-50Ω environment.
A method called "load pull", which includes fundamental harmonics, has been developed to deal with this issue [6].

In the case of an oscillator, however, there is only one high-Q resonator which suppresses the harmonics of the fundamental frequency (short circuit). In this limited case, the *S*-parameters, measured in a 50Ω system are useful. The following tables show two sets of measurements generated from the Infineon transistor BFP520 under different drive levels.

Since the oscillator will be in quasi-large-signal operation, we will need the large-signal *S*-parameters as a starting condition for the large-signal design (output power, harmonics, and others). The *S*-parameters generated from this will be converted into *Y*-parameters, defined under large-signal conditions and then used for calculating the large-signal behavior. We will use the symbol Y^+ to designate large-signal *Y*-parameters. In general, the Y parameters are computed from the S-parameters with the following equations:

$$Y_{11} = \frac{\left((1 - S_{11}) * (1 + S_{22}) + S_{12} * S_{21}\right)}{\Delta}$$

$$Y_{22} = \frac{\left((1 + S_{11}) * (1 - S_{22}) + S_{12} * S_{21}\right)}{\Delta}$$

$$Y_{12} = -2 * \frac{S_{12}}{\Delta}$$

$$Y_{21} = -2 * \frac{S_{21}}{\Delta}$$

Where, $\Delta = \left((1 + S_{11}) * (1 + S_{22})\right) + (S_{12} * S_{21})$
Tables 1-2 and 1-3 show the large-signal *S*-parameters for –20dBm and –10dBm. However, in some cases the analysis starts at small-signal conditions. All derivations have been verified with MATHCAD and the original text input has been used. Therefore, in some cases the Y^+ marker has <u>not</u> been used. The use of the MATHCAD equation set allows for error free reuse of the equations. The following four plots, Figures 1-24, 1-25, 1-26, 1-27, show S_{11}, S_{12}, S_{21}, and S_{22} measured from 50 MHz to 3000 MHz with driving levels from –20dBm to 5dBm. The DC operating conditions were 2V and 20mA as shown in Figure 1-22.

Table 1-2: Frequency Dependent S-Parameters

(*S*-Parameters at -20 dBm)

Frequency	S_{11}(Mag)	S_{11}(Ang)	S_{12}(Mag)	S_{12}(Ang)	S_{21}(Mag)	S_{21}(Ang)	S_{22}(Mag)	S_{22}(Ang)
1.0E+08	0.78	-17.15	29.57	-160.6	0.01	69.66	0.96	-7.63
1.5E+08	0.74	-19.95	30.87	-175.17	0.01	73.05	0.94	10.27
2.0E+08	0.71	-23.01	30.87	174.87	0.01	73.61	0.92	12.8
2.5E+08	0.69	-26.34	30.43	167.17	0.01	73.11	0.9	-15.25
3.0E+08	0.66	-29.8	29.8	160.76	0.01	72.13	0.87	-17.61
3.5E+08	0.64	-33.28	29.08	155.2	0.01	70.91	0.85	-19.92
4.0E+08	0.61	-36.73	28.3	150.22	0.01	69.59	0.83	-22.16
4.5E+08	0.59	-40.1	27.5	145.68	0.02	68.24	0.81	-24.33
5.0E+08	0.56	-43.36	26.68	141.5	0.02	66.91	0.78	-26.44
5.5E+08	0.53	-46.47	25.85	137.62	0.02	65.66	0.76	-28.44
6.0E+08	0.51	-49.42	25.02	134	0.02	64.51	0.73	-30.33
6.5E+08	0.48	-52.19	24.18	130.62	0.02	63.5	0.7	-32.07
7.0E+08	0.46	-54.78	23.35	127.46	0.02	62.63	0.68	-33.64
7.5E+08	0.44	-57.2	22.54	124.52	0.02	61.9	0.65	-35.04
8.0E+08	0.42	-59.44	21.74	121.76	0.02	61.3	0.63	-36.26
8.5E+08	0.39	-61.53	20.98	119.19	0.02	60.82	0.6	-37.31
9.0E+08	0.38	-63.48	20.24	116.77	0.03	60.43	0.58	-38.2
9.5E+08	0.36	-65.29	19.53	114.51	0.03	60.13	0.56	-38.95
1.0E+09	0.34	-66.99	18.85	112.38	0.03	59.88	0.54	-39.57
1.5E+09	0.22	-80.06	13.7	96.21	0.04	58.66	0.41	-41.5
2.0E+09	0.14	-91.02	10.61	85.03	0.04	57.04	0.33	-40.51
2.5E+09	0.09	-105.04	8.64	76	0.05	54.51	0.29	-39.1
3.0E+09	0.06	-129.69	7.27	68.07	0.06	51.33	0.25	-37.7

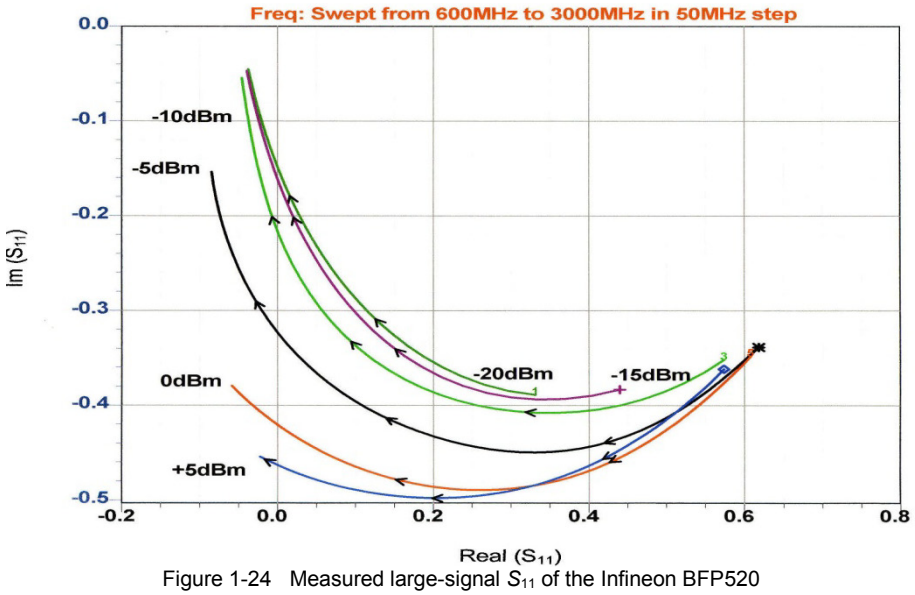


Figure 1-24 Measured large-signal S_{11} of the Infineon BFP520

Table 1-3 Frequency Dependent S-Parameters

(*S*-Parameters at -10 dBm)

Frequency	S_{11}(Mag)	S_{11}(Ang)	S_{12}(Mag)	S_{12}(Ang)	S_{21}(Mag)	S_{21}(Ang)	S_{22}(Mag)	S_{22}(Ang
1.00E+08	0.81	-12.8	14.53	179.18	0.02	39.17	0.55	-20.62
1.50E+08	0.79	-14.26	14.51	170.01	0.02	51.38	0.6	-24.42
2.00E+08	0.77	-16.05	14.46	163.78	0.02	57.11	0.65	-27.11
2.50E+08	0.76	-17.94	14.4	158.86	0.03	60.47	0.67	-28.33
3.00E+08	0.74	-19.85	14.31	154.78	0.03	62.9	0.69	-28.28
3.50E+08	0.73	-21.74	14.21	151.32	0.03	64.83	0.7	-27.33
4.00E+08	0.72	-23.62	14.1	148.32	0.03	66.46	0.71	-25.99
4.50E+08	0.71	-25.51	13.99	145.65	0.03	67.72	0.73	-24.6
5.00E+08	0.7	-27.42	13.88	143.19	0.03	68.57	0.74	-23.39
5.50E+08	0.68	-29.37	13.76	140.87	0.03	68.99	0.76	-22.5
6.00E+08	0.67	-31.38	13.65	138.62	0.04	68.98	0.77	-21.93
6.50E+08	0.66	-33.45	13.54	136.4	0.04	68.59	0.77	-21.68
7.00E+08	0.64	-35.56	13.42	134.2	0.04	67.95	0.78	-21.68
7.50E+08	0.63	-37.71	13.31	132	0.04	67.2	0.78	-21.89
8.00E+08	0.61	-39.88	13.19	129.83	0.04	66.31	0.77	-22.25
8.50E+08	0.59	-42.06	13.07	127.7	0.04	65.37	0.77	-22.62
9.00E+08	0.58	-44.23	12.95	125.6	0.04	64.48	0.76	-23.26
9.50E+08	0.56	-46.4	12.82	123.57	0.04	63.69	0.76	-24.04
1.00E+09	0.54	-48.55	12.69	121.6	0.04	62.82	0.75	-24.71
1.50E+09	0.37	-70.76	11.35	104.37	0.05	52.76	0.67	-33.77
2.00E+09	0.21	-91.19	9.99	88.64	0.05	46.68	0.48	-43.79
2.50E+09	0.12	-107.22	8.43	77.36	0.06	49.37	0.33	-43.13
3.00E+09	0.07	-130.38	7.18	68.7	0.06	48.69	0.27	-40.46

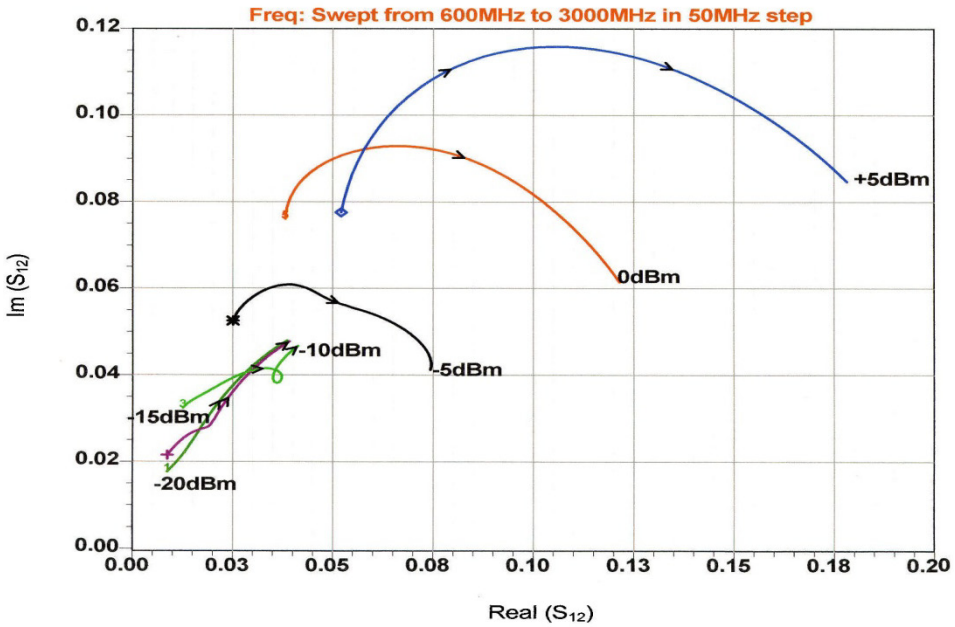


Figure 1-25 Measured large-signal S_{12} of the Infineon BFP520.

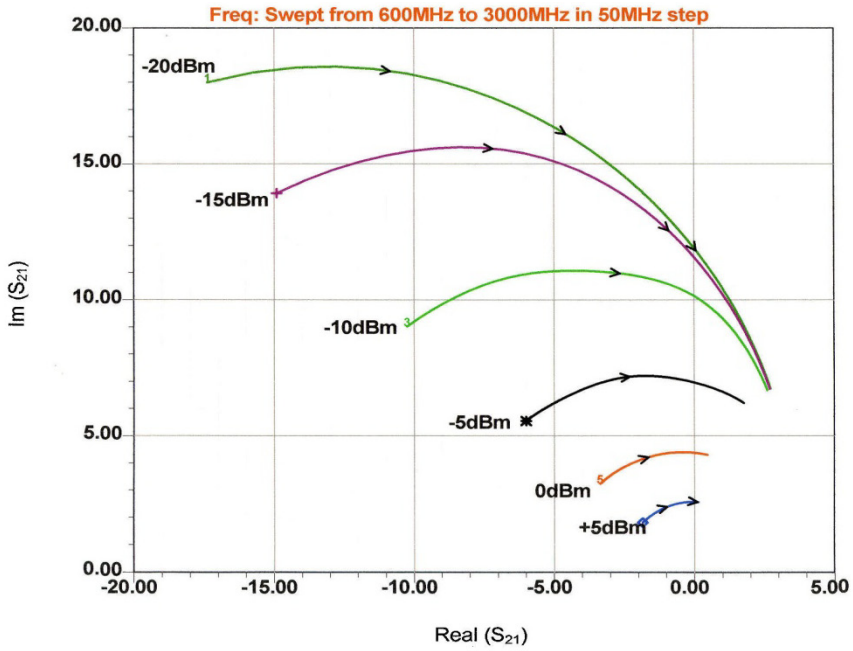


Figure 1-26 Measured large-signal S_{21} of the Infineon BFP520.

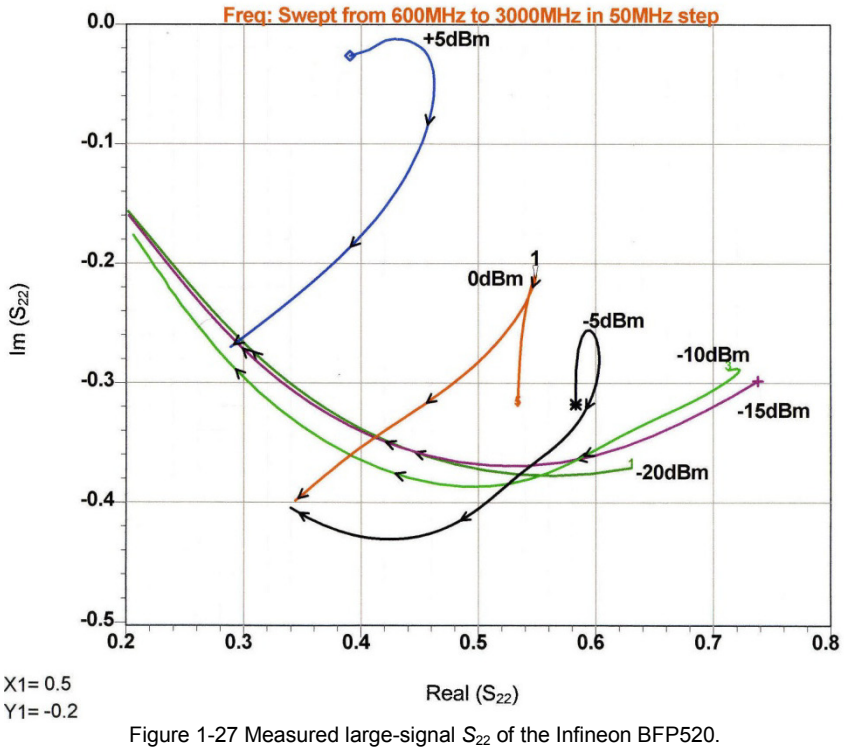


Figure 1-27 Measured large-signal S_{22} of the Infineon BFP520.

When using a SPICE type simulator, or a harmonic balance simulator, then one must use the non-linear model parameters as shown in Figure 1-29. Modern foundries supply relevant data for GaAs and for BiCMOS devices. The choices of what model to use are not always simple: for bipolar transistors, here the advanced Gummel Poon model [44, 45] is preferred similar to Figure 1-28. A modification to the base-emitter diffusion capacitance is preferred. Recent publications address this issue in greater detail. For GaAs devices the modified Materka model gives very

good results. Modeling a JFET using the Materka model also yields very accurate RF results. For oscillator circuits a well-documented MOS level-3 models and the EKV3 model can provide accurate simulation. For RF applications, the final optimum model is still undefined!

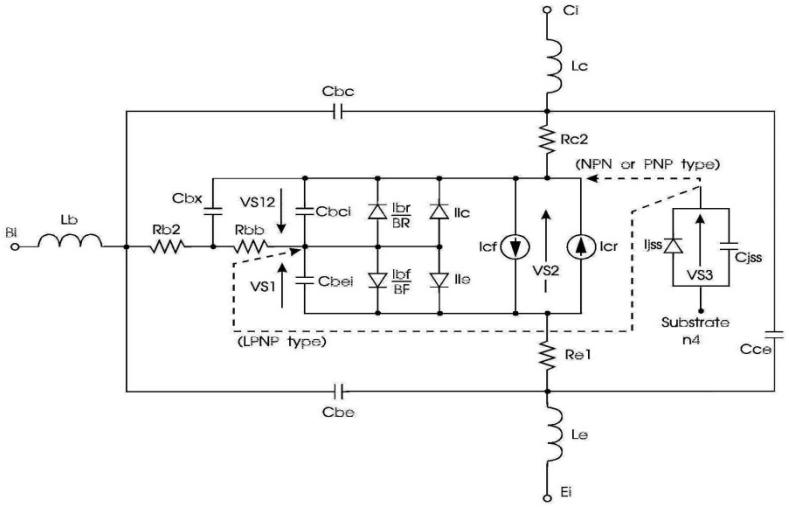


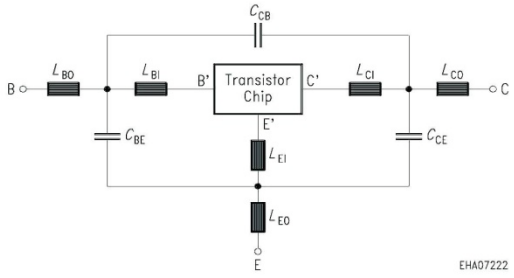
Figure 1-28 A modern equivalent circuit of a bipolar transistor

SPICE Parameters (Gummel-Poon Model, Berkley-SPICE 2G.6 Syntax) :

Transistor Chip Data

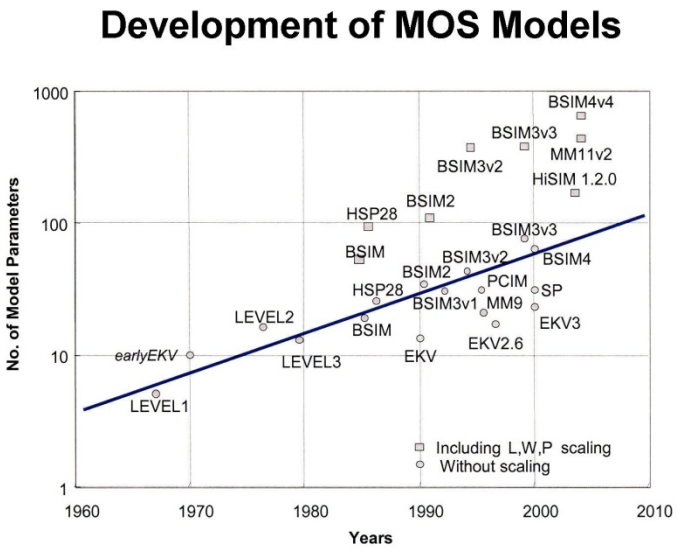
IS =	15	aA	BF =	235	-	NF =	1	-
VAF =	25	V	IKF =	0.4	A	ISE =	25	fA
NE =	2	-	BR =	1.5	-	NR =	1	-
VAR =	2	V	IKR =	0.01	A	ISC =	20	fA
NC =	2	-	RB =	11	Ω	IRB =	-	A
RBM =	7.5	Ω	RE =	0.6		RC =	7.6	Ω
CJE =	235	fF	VJE =	0.958	V	MJE =	0.335	-
TF =	1.7	ps	XTF =	10	-	VTF =	5	V
ITF =	0.7	A	PTF =	50	deg	CJC =	93	fF
VJC =	0.661	V	MJC =	0.236	-	XCJC =	1	-
TR =	50	ns	CJS =	0	fF	VJS =	0.75	V
MJS =	0.333	-	XTB =	-0.25	-	EG =	1.11	eV
XTI =	0.035	-	FC =	0.5	-	TNOM	298	K

Package Equivalent Circuit:



L_{BI} =	0.47	nH
L_{BO} =	0.53	nH
L_{EI} =	0.23	nH
L_{EO} =	0.05	nH
L_{CI} =	0.56	nH
L_{CO} =	0.58	nH
C_{BE} =	136	fF
C_{CB} =	6.9	fF
C_{CE} =	134	fF
Valid up to 6GHz		

Figure 1-29 SPICE parameters and package equivalent circuit of the Infineon transistor BFP520.



- Number of DC model parameters vs. the year of the introduction of the model
  Most recent versions of the EKV, HiSIM, MM11and SP models are included
- Significant growth of the parameter number that includes geometry (W/L) scaling

Figure 1-30 A survey of MOS model development

Figure 1-30 shows the developments in MOS models and the large number of model parameters used in modern models. The accompanied parameter extraction to measure the model parameters is similarly complex. Figure 1-31 shows the test fixture for the measurement of the large-signal *S*-parameters for the device under test (DUT). The test fixture was calibrated to provide 50Ω to the transistor leads. The test set-up consists of a DC power supply and a network analyzer for combined *S*-parameter measurements. The picture shows that the actual test system is very simple, but unfortunately, very expensive. Recently JFETs find many applications in the higher microwave frequencies and hence their large-signal measurement seems important and useful. The large-signal measurement has been done for the first time and tabulated in Table 1-4 below for Vishay-Siliconix U310 device.

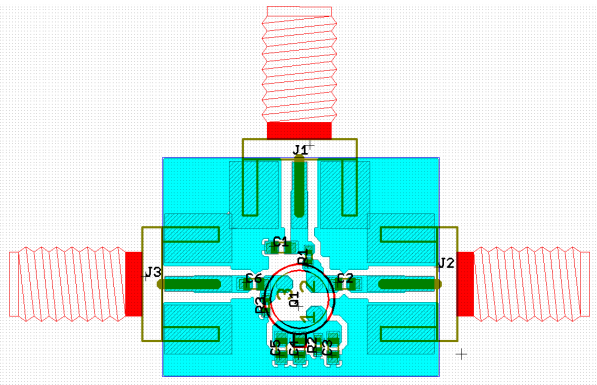


Figure 1-31 Test Fixture to measure large signal S-parameters (A proper de-embedding has been done)

The following four plots, Figures 1-32, 1-33, 1-34, 1-35, show S_{11}, S_{12}, S_{21}, and S_{22} measured from 1 MHz to 250 MHz with driving levels from –20dBm to 14dBm. The DC operating conditions were V_d = 11.08V and I_{dss} = 29.9mA. Using bipolar and JFET models, the basic topology of frequency selective RF components such as active inductor for the application of oscillator circuits has been developed. The flicker corner frequency for JFET is very small and

lends itself for the oscillator application. Large-signal parameter extraction for the U310 [13, pp. 237-321] JFET is shown in this work.

Table 1-4 Frequency Dependent S-Parameters
(*S*-Parameters at "+14 dBm)

Freq (Hz)	S11(MAG)	S11(ANG)	S12(MAG)	S12(ANG)	S21(MAG)	S21(ANG)	S22(MAG)	S22(ANG)
1.00E+06	0.9834591	-0.60739	0.740174	89.38105	0.001079	44.77566	0.626962	-0.06491
2.25E+06	0.95209	-0.76451	0.862556	88.87844	0.002328	45.1113	0.628065	0.106047
3.49E+06	0.9647607	-1.19221	0.843784	88.67394	0.003671	45.01349	0.626026	0.320344
4.74E+06	0.9530751	-1.93989	0.816117	88.27949	0.004997	44.9723	0.627554	0.696274
5.98E+06	0.9346731	-2.66621	0.802254	87.97664	0.006329	45.14298	0.646426	1.748353
7.23E+06	0.9276288	-3.04825	0.79989	85.53991	0.00791	43.01877	0.705886	-3.34346
8.47E+06	0.8988169	-3.81193	0.759218	85.28429	0.008821	43.52291	0.629004	-1.84411
9.72E+06	0.8992334	-3.82511	0.735759	85.48802	0.010085	43.80672	0.624356	-1.00415
1.10E+07	0.871265	-4.38601	0.740618	84.93882	0.011377	43.95555	0.626192	-0.4083
1.22E+07	0.8841737	-3.97852	0.725338	85.42127	0.012759	43.98933	0.634002	0.294813
1.47E+07	0.8809284	-4.1217	0.776742	85.05985	0.016568	43.60244	0.747623	0.070639
1.59E+07	0.8827215	-4.27524	0.775387	82.78854	0.017696	41.33582	0.724719	-4.31619
1.97E+07	0.8864995	-5.18443	0.749907	81.90788	0.020644	40.82397	0.644849	-4.28655
2.09E+07	0.8933217	-5.45192	0.750559	81.69948	0.021849	40.75882	0.640014	-4.17497
3.09E+07	0.8822452	-9.4792	0.758642	78.55151	0.031337	39.62138	0.628722	-4.45186
4.08E+07	0.7945661	-14.0581	0.778943	74.83038	0.041161	38.47967	0.625956	-5.4101
5.08E+07	0.8083689	-15.1562	0.775627	72.90865	0.051399	37.11436	0.623925	-6.4615
6.08E+07	0.7782173	-17.8718	0.788903	70.46195	0.061289	35.60201	0.620981	-7.62976
7.07E+07	0.7623562	-20.3858	0.792445	68.25586	0.071023	34.09352	0.61712	-8.81252
8.07E+07	0.7284944	-23.2199	0.735044	65.60994	0.080188	32.67454	0.613357	-9.91178
9.06E+07	0.7037216	-26.3696	0.742155	63.20748	0.089348	31.0434	0.612012	-11.293
1.09E+08	0.6525962	-30.9812	0.717226	59.21583	0.104921	28.49311	0.602189	-13.4376
1.21E+08	0.6500913	-32.4877	0.71241	57.38567	0.114396	26.97773	0.597791	-14.7239
1.30E+08	0.6404952	-34.9039	0.709601	55.85575	0.122751	25.67391	0.593966	-15.8937
1.40E+08	0.6356057	-37.3849	0.700585	54.28991	0.131083	24.34623	0.59106	-17.0329
1.50E+08	0.620072	-40.8496	0.697156	52.58038	0.139168	22.9388	0.586227	-18.2595
1.60E+08	0.6417533	-41.4992	0.696456	51.234	0.147369	21.52741	0.581754	-19.3461
1.70E+08	0.6316214	-44.4512	0.695538	49.58931	0.154902	20.15608	0.574913	-20.5718
1.80E+08	0.6270206	-46.2375	0.700985	47.97454	0.162491	18.73555	0.567691	-21.8026
1.90E+08	0.6165829	-48.2795	0.702078	46.38768	0.169299	17.27967	0.559321	-23.0908
2.00E+08	0.6058026	-50.1081	0.694571	44.68843	0.175688	15.88691	0.551985	-24.3263
2.10E+08	0.5994081	-52.0703	0.687501	43.0633	0.181734	14.52594	0.545476	-25.5089
2.20E+08	0.5890521	-54.7806	0.672689	41.28725	0.18759	13.26174	0.539928	-26.6053
2.30E+08	0.5865263	-56.7681	0.664567	39.56736	0.193005	11.98317	0.534875	-27.5698
2.40E+08	0.5971292	-57.4034	0.688218	38.03636	0.19764	10.57221	0.528051	-28.4852
2.50E+08	0.5797494	-61.1322	0.663015	36.33946	0.20239	9.370157	0.52125	-29.407

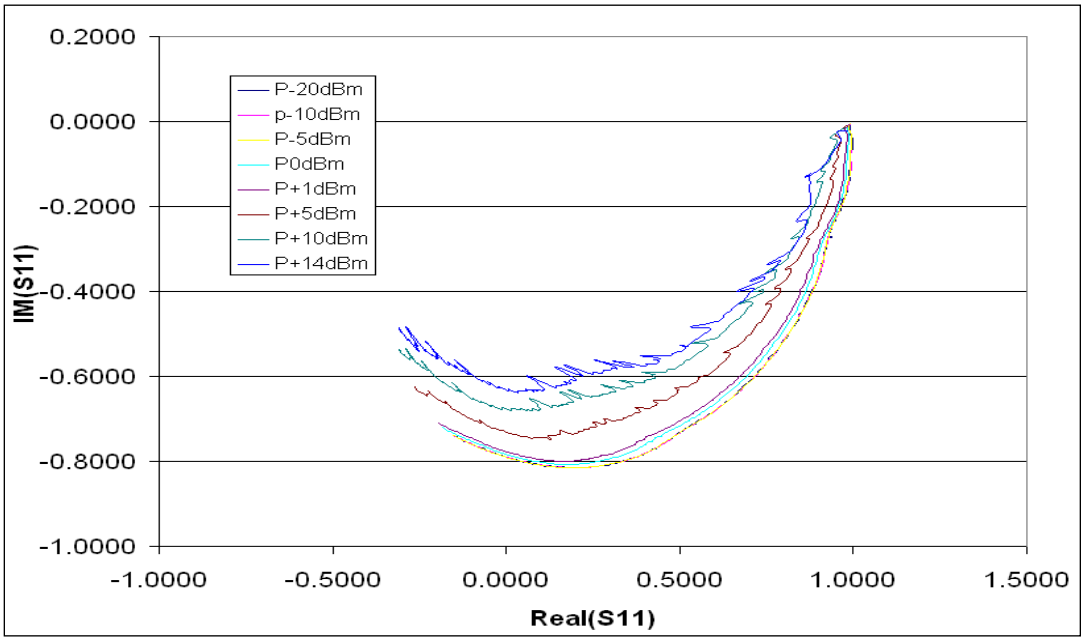


Figure 1-32: Measured large-signal S_{11} of the Vishay-Siliconix U310. Frequency swept from 1MHz to 250MHz.

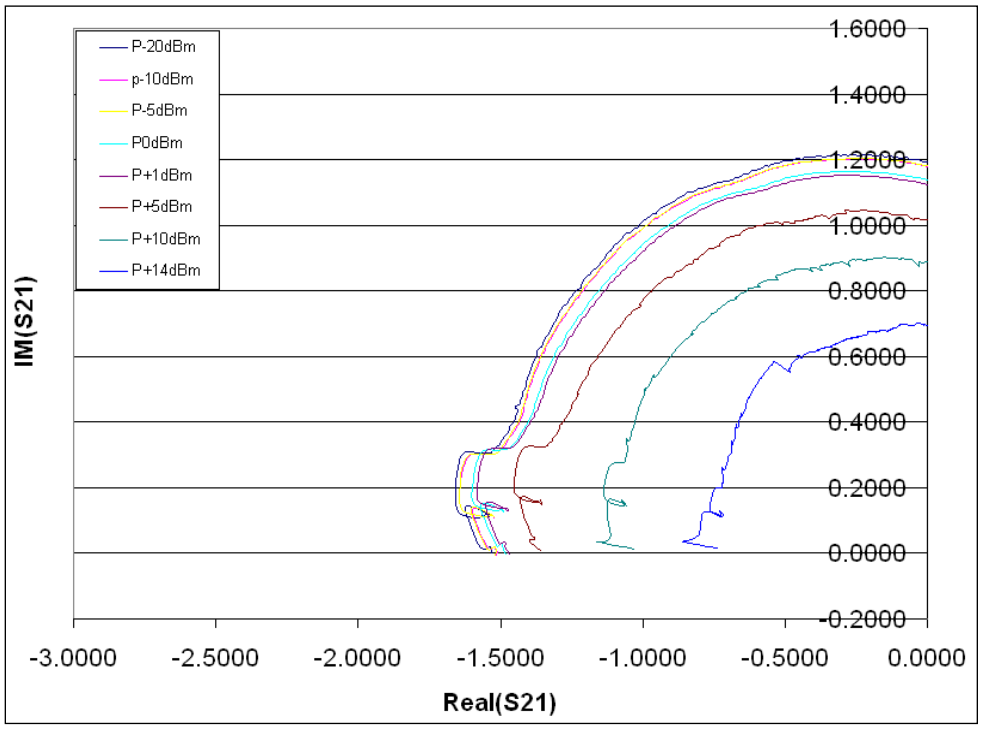


Figure 1-33 Measured large-signal S_{21} of the Vishay-Siliconix U310. Frequency swept from 1MHz to 250MHz.

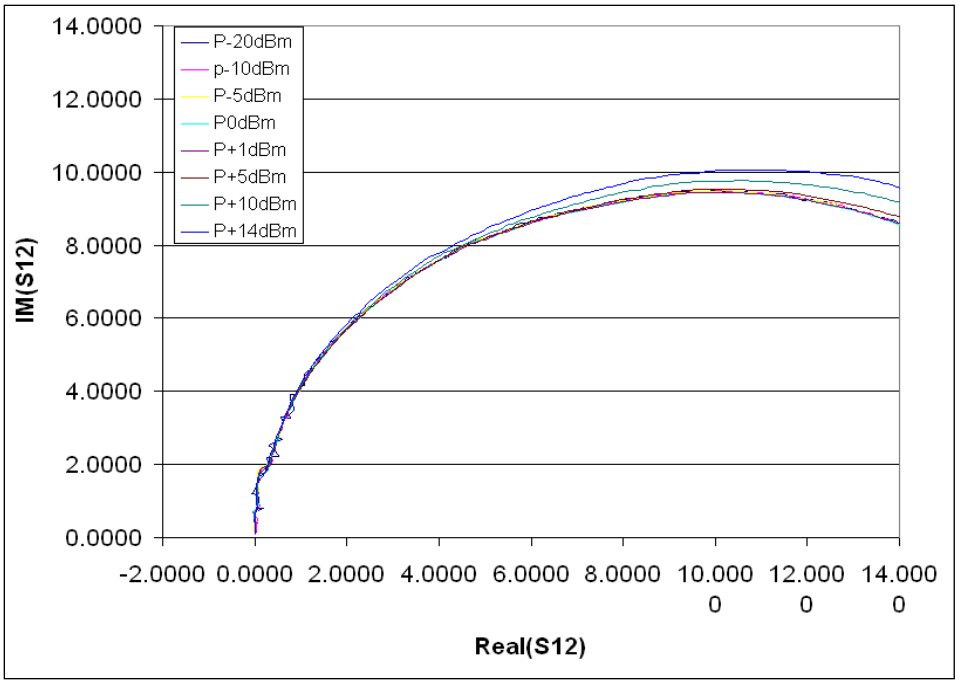


Figure 1-34 Measured large-signal S_{12} of the Vishay-Siliconix U310. Frequency swept from 1MHz to 250MHz.

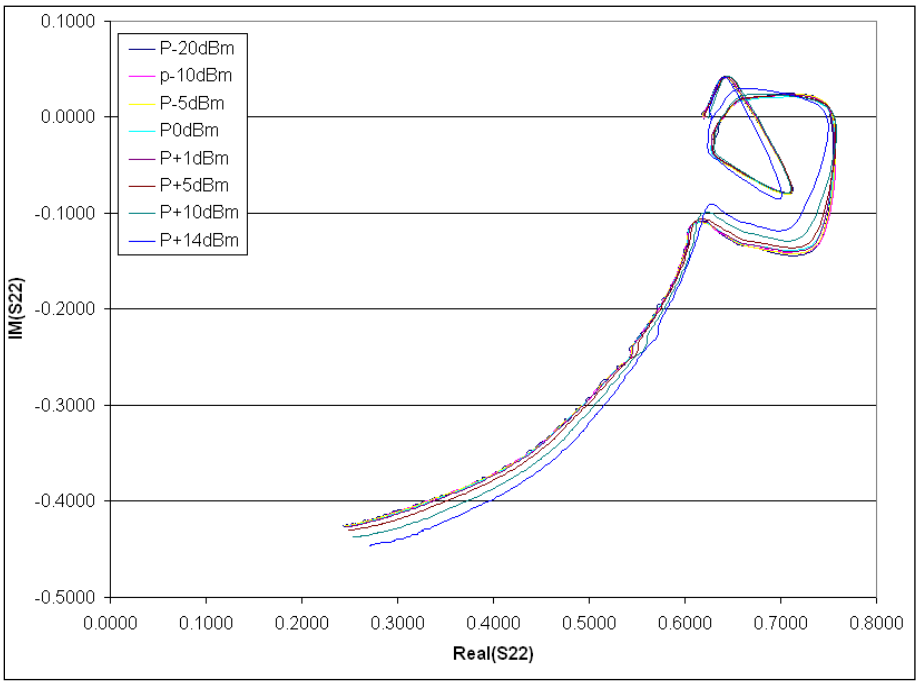


Figure 1-35: Measured large-signal S_{22} of the Vishay-Siliconix U310. Frequency swept from 1MHz to 250MHz.

1. 4 Passive and Active Inductor

Extensive work is being done in the area of passive RF components such as inductors for applications as the frequency selective element in voltage-controlled oscillators. Inductors are essential elements for resonators, filtering and impedance matching purposes within a multitude

of circuit solutions for RFICs/MMICs applications. Largely, inductor dictates their cost and performance. Passive integrated spiral inductors occupy large die area and increase costs. The magnetic coupling among inductors on a device initiates cross talk and deteriorates the overall circuit performance. It is also difficult to realize a broadband spiral inductor, especially with high inductance, because of stray capacitances. This motivates the need for alternative solutions such as the active inductor topology, which offers smaller die-area, high Q factor and easier floor planning.

The current trend moves towards multi-standard terminals and the application of active inductors paves the way for inductor-less reconfigurable radio-frequency circuit solutions. Voltage dependent variable capacitors (varactors) show high Q-factor but are limited in tuning range due to the influence of package parasitics, especially at higher operating frequencies. Tunable inductors offer the advantage of a wide tuning range in a small chip area and enable this technology as a cost-effective alternative for applications in filters, phase shifters, couplers, power dividers, and tunable oscillators.

1.4.1 Passive Inductor

Generally, passive inductors occupy large expensive die area. When fabricated on low-resistivity substrates, much of the electromagnetic energy leaks into the substrate resulting in low Q-factors. On the other hand, since the only noise generation mechanism is the loss due to the series resistance and leakage, passive inductors perform better than active inductors in terms of noise and linearity. Figure 1-36 shows a typical die photograph, inductance and quality factor of a 2.5 turn passive spiral inductor using a standard CMOS process [4]. Even though the maximum Q-factors are between 4 and 7 at 4-7 GHz, the Q-factor at 2GHz are as low as 3 because of the thin aluminum metallization and the conductive substrate. Figure 1-37 shows the schematic and layout of a 2GHz GaAs FET oscillator using passive spiral inductors [6, pp. 243]. Figures 1-38 and 1-39 show the load line and phase noise plots for the passive spiral inductor oscillator (shown in Figure 1-37). As shown in Figure 1-37, the two inductors (L_1 and L_2) in the circuit layout determine most of the surface die area, and are therefore not a cost-effective solution.

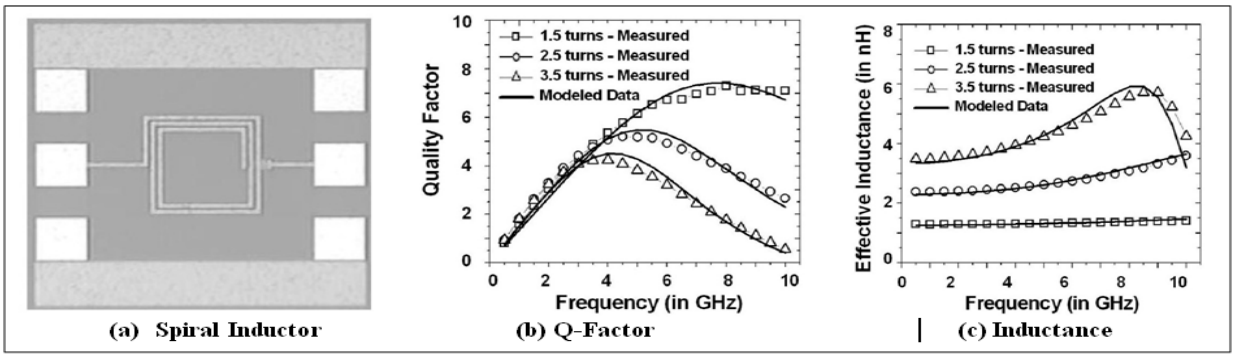


Figure 1-36 A typical 2.5 turn spiral inductor: (a) Die photograph, (b) Plot of Q-factor and (c) Plot of inductance value with frequency [4]

The idea is to explore the possibility to replace the large spiral inductor with an active device requiring only a fraction of its size. It is also necessary to find a solution that gives equal if not better noise and dynamic range at microwave frequencies, as compared with spiral inductor.

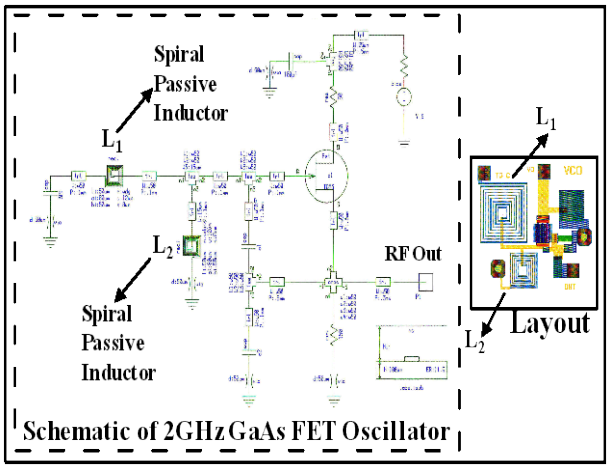


Figure 1-37 Schematic and layout of a 2 GHz GaAs FET Oscillator

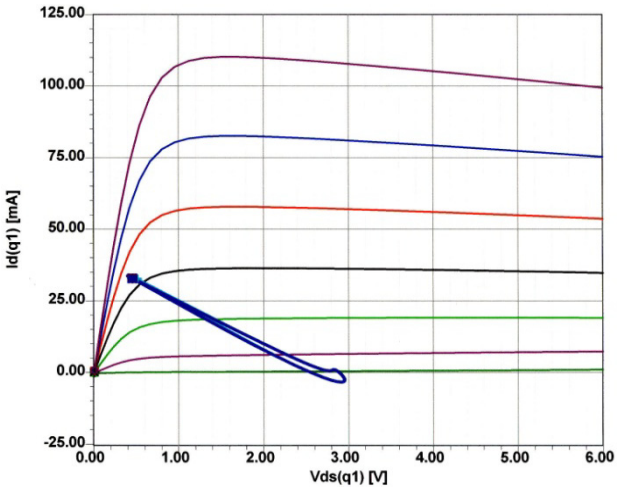


Figure 1-38 DC-IV and load line of the GaAs FET in the oscillator

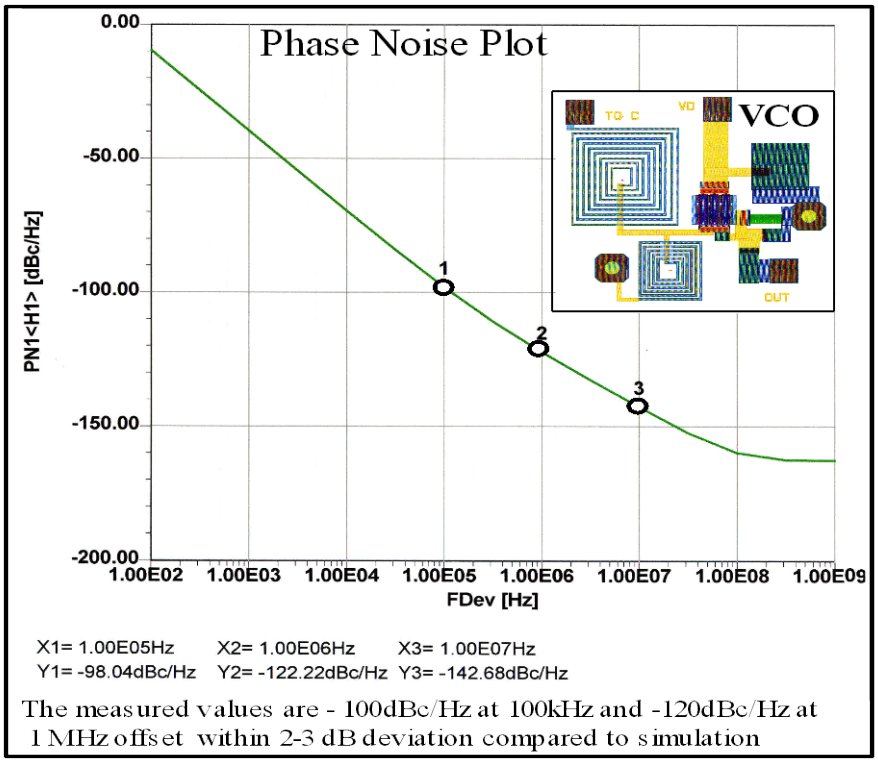


Figure 1-39 CAD simulated phase noise plot of oscillator shown in Figure 1-37

1.4.2. Active Inductor

Active inductors are implemented based on the well-known gyrator-C architecture consisting of two transistors in feedback generating inductive impedance. In general, the grounded active inductor topology is commonly used to implement high Q tunable active inductors (TAIs). To enhance the inductance and Q of this active inductor, the introduction of a tunable feedback resistance R_f is incorporated as shown in Figure 1-40.

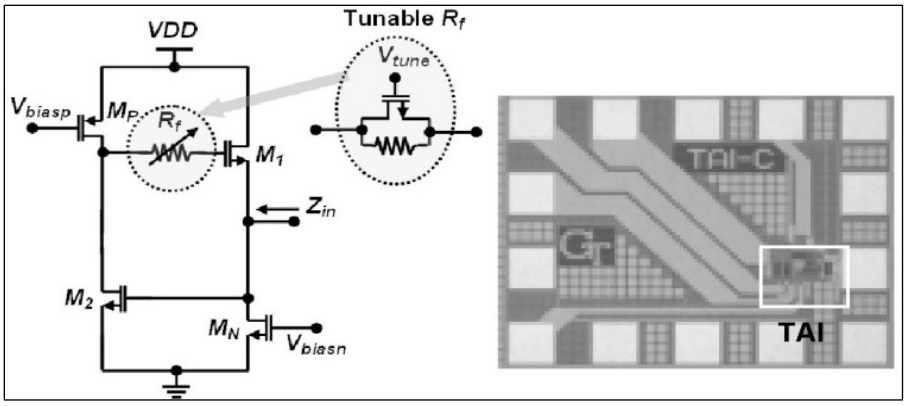


Figure 1-40 Active inductor circuit and its die photograph [4]

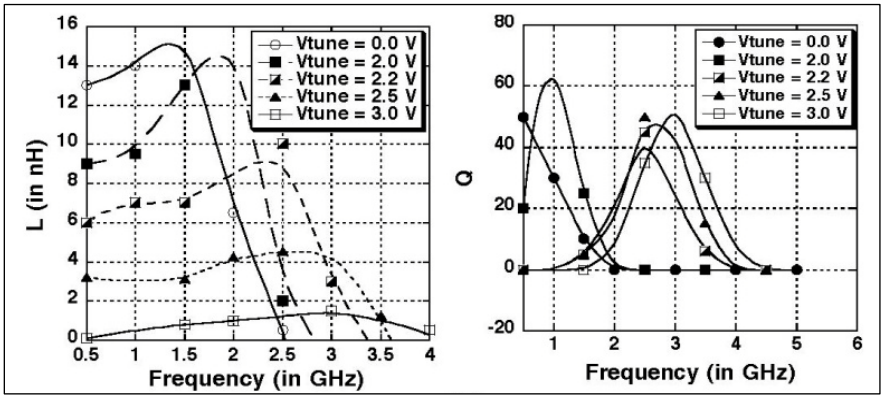


Figure 1-41 Plot of inductance and Q-factor [4]

The tunable feedback resistance increases the effective inductance, L_{eff}, and decreases the equivalent series resistance simultaneously, which enhances its quality factor [4]. The tunability has also been improved as all the three parameters namely L_{eff}, Q and the frequency, f_Q, associated with the maximum Q can be tuned independently.

Detailed analysis of the grounded TAI suggests a direct trade-off between the achievable range of tunable inductance, quality-factor and the output noise that calls for an optimization guideline. From the gyrator-C architecture and the noise analysis, the dependence of L_{eff}, Q, and the output noise on the design parameters is given as [4]

$$L_{eff} \propto \frac{R_f}{g_{m1} g_{m2}} \tag{1-23}$$

$$f_Q \propto \frac{1}{\sqrt{R_f}} \tag{1-24}$$

$$v_n \propto R_f \times g_{m1} \times g_{m2} \tag{1-25}$$

where g_{m1} and g_{m2} are the small-signal transconductance of the transistors M1 and M2 shown in Figure 1-40. Since g_{m1} and g_{m2} are related to each other from the expression for the effective inductance, the dependence on g_{m1} can be eliminated. To analyze the effects of the remaining two design variables on the performance, the simulated effective inductance and the, output noise voltage are plotted vs. the two variables for a fixed frequency of 2 GHz and a fixed g_{m1} = 20mS, as illustrated in Figure 1-42.

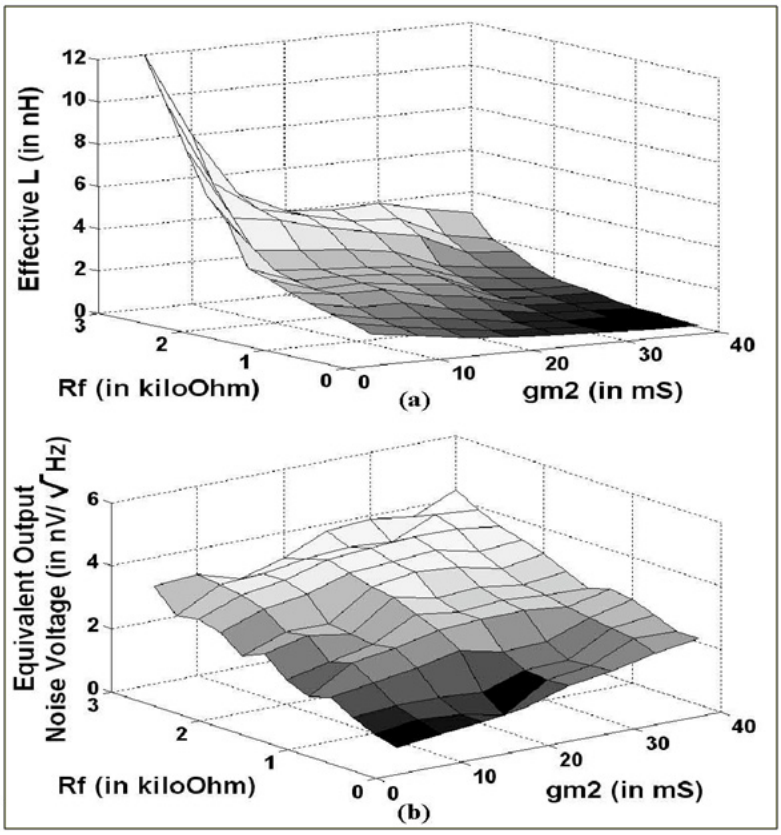


Figure 1-42 CAD simulated plot: (a) effective inductance and (b) output noise voltage versus g_{m2} and fixed g_{m1} =20mS [4]

It is observed that the effective inductance and the output noise voltage shown in Figure 1-42 follow similar trends as in Equation (1-23) and Equation (1-25). The degradation of noise with increasing feedback resistance is prominent from Figure 1-42(b). Higher feedback resistance also decreases the frequency of maximum Q, i.e., the frequency of operation. On the other hand, the range of tunable inductance increases with the range of the tunable feedback resistance. This leads to a direct trade-off between tunable inductance and the frequency of operation on one hand, and low-noise performance on the other. Thus, to achieve wide tunability and high frequency operation for a low output noise, the design parameters need to be optimized based on the 3D-plots of all the performance criteria under consideration.

The optimized active inductor has been fabricated using 0.18µm CMOS technology. The TAI achieved an inductance tuning range of 0.1-15nH with Q > 50 for frequencies between 0.5-4GHz, as shown in Figure 1-41. The active inductor consumes around 7.2mW from a 1.8V supply and occupies a very small area of 100 x 50 μm^2.

Noise is a major drawback of active inductors. An approximate equivalent output noise voltage due to the thermal and flicker noise sources as shown in Figure 1-43 can be evaluated. It can be observed that the total noise increases with an increase in the feedback resistance and with decrease in the device size. However, both the resistance and the sizing of devices have a significant effect on the inductance and the frequency of operation that leads to the trade-off between the inductance and the operating frequency on one side and the output noise on the other.

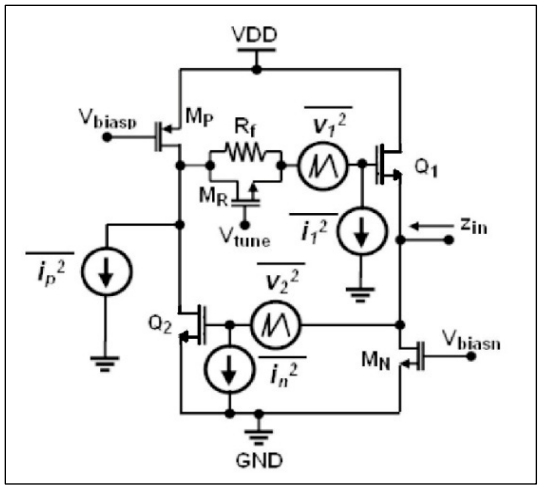


Figure 1-43 Active inductor circuit with its equivalent noise sources

1.5. Selection Criteria and Performance Comparison

The performance comparison criterion (Q-factor, Die-Area, Power Consumption, Linearity, Noise, EMI and Floor Planning) establishes important design guidelines for selection of inductors per particular applications. Table 1-5 describes the comparative analysis of the passive and active inductor for RF and microwave applications. Thus, in spite of the drawbacks such as noise and linearity, active inductors have a significant advantage over passive inductors in terms of die area, quality factor, and issues regarding EMI and floor planning. Additionally, the potential of extensive tunability of active inductors could be harnessed for multi-standard and wideband applications.

1.6. Tunable Active Inductor Oscillator

The conventional VCO circuit uses a negative-resistance generating network to compensate the loss associated with the passive resonators. This work uses the active inductor to replace the negative resistance generating active circuit of the conventional VCO and the active inductor features broadband tuning characteristics without tuning diodes.

Figure 1-44 shows the differential PMOS and NMOS cross-coupled VCO with a 400 MHz tuning range (around 3-3.4GHz) using a 1.5nH passive spiral inductor that occupies an area of $900\mu m \times 800\mu m$. The VCO core consumes 10mA current from a 2.7V supply and the measured phase noise is -104.3dBc/Hz at 1MHz offset frequency. For comparison, Figure 1-45 shows the single-ended 500MHz tunable inductor Colpitts oscillator with 80% tuning range implemented in 0.18µm Si CMOS technology. The output power varies from -29 to -20.8dBm with the power consumption of 13.8mW from a 1.8V supply and occupies an area of 300x300µm^2. The measured phase noise is typically -80dBc/Hz at 1MHz offset, which is inferior in comparison to commercially available passive inductor oscillator for similar power consumption.

Thus, in spite of the higher phase-noise, the active inductor VCO achieves a much higher tuning range consumes considerably lower power and occupies 1/8th of the die area. The phase-noise performance could be improved by the use of a differential active inductor in the resonator or a differential VCO topology using injection and mode locking techniques.

Table1-5: Comparative analysis of the passive and active inductor for RF & MW applications

Performance parameter	Passive Inductor	Active Inductor
Q-factor	Low Q-factor (Q-factor can be relatively improved by incorporating shielding or differential inductors topology but at added cost and large die- area)	High Q-factor (Active inductor offers higher Q than the passive spiral inductor, including the Q and the frequency of maximum Q are independently tunable.
Tunability	Fixed/Limited	Large tuning range
Die-Area	Large die-area	Small die-area
Power Consumption	Zero	Significant (Active inductor consumes power for generating inductance with negative loss resistance, resulting in high Q factor that offsets the power consumption due to reduction in losses)
Linearity	Good Linearity	Poor Linearity (Active inductor circuit is driven under large-signal condition, causing a shift in operating point, distortion, and impedance fluctuations)
Noise	Superior Noise Performance	Poor Noise Performance (The operating frequency and inductance values of the active inductor depend on device size and feedback resistance R_f but at the cost of the noise and dynamic range, therefore, they trade each other)
EMI	Significant EMI problems (Electromagnetic fields associated with the large metallic structure of the spiral inductors causing EMI)	EMI insensitive
Floor-Planning	Poor (The large unused area in the neighborhood of the inductors due to large die- area makes difficult floor-planning)	Not required

1.7. Tunable Inductor Using RF MEMS Technology

Cost-effective, power-efficient and compact RF modules such as tunable VCOs, filters, and mixers are critical components in reconfigurable receiver architectures. RF MEMS are expected to address reconfigurable and concurrent solutions by exploiting RF MEMS technology.

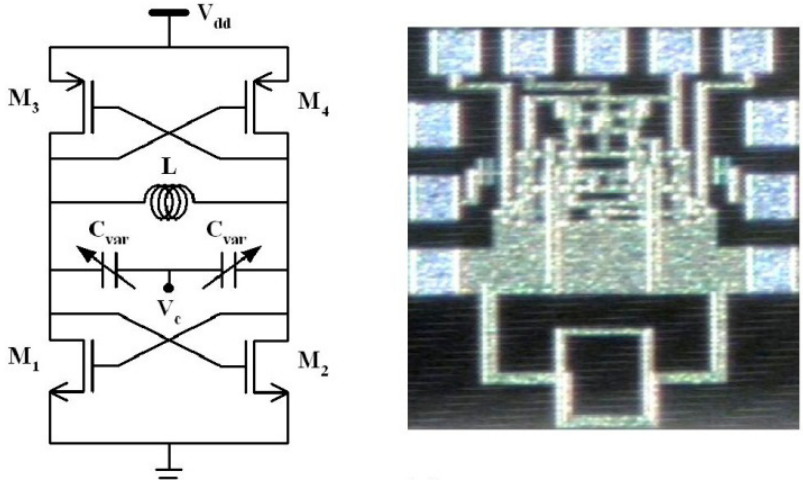


Figure 1-44 Schematic and die of differential spiral inductor VCO [4]

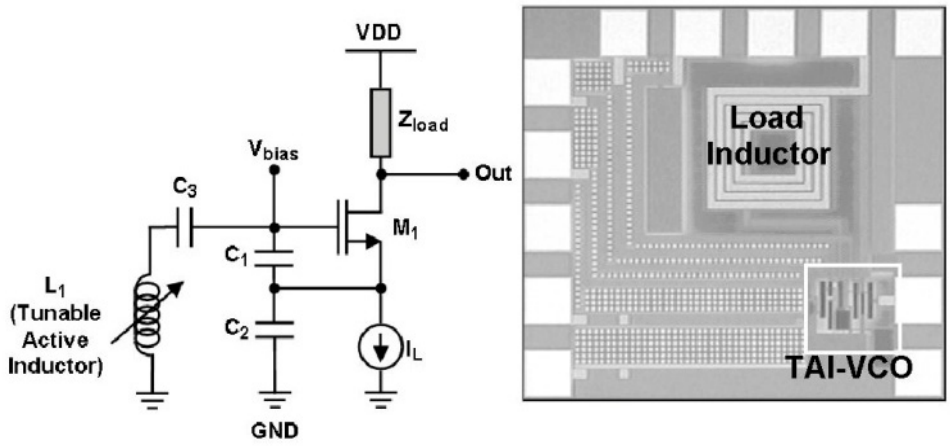


Figure 1-45 Schematic and die of the active inductor VCO [4]

1.7.1 RF MEMS Components

Figure 1-46 shows a typical RF MEMS enhanced dual-loop wideband receiver, which dynamically reconfigures the desired operating frequency from 100MHz to 10GHz [41]. As shown in Figure 1-46, an array of MEMS mixer-filters down convert the received signal from the GHz frequency band to a unique intermediate frequency (IF) in MHz range, set by the resonant conditions of the MEMS device.

Figure 1-47 shows a typical die photograph of an RF MEMS filter that comprises a 0.09mm^2 6nH symmetrical spiral inductor surrounded by four 0.13mm^2 MEMS capacitors in Jazz Semiconductor's SiGe60 four-metal BiCMOS process. Figure 1-48 shows the plot of the measured insertion loss of the RF MEMS filter, which is typically 7dB for a reconfiguration of 490MHz between 1.87GHz (f_{low}) to 2.36GHz (f_{high}).

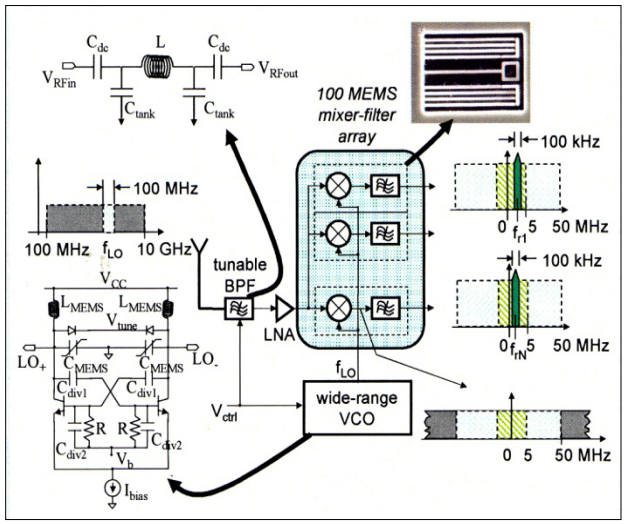


Figure 1-46 RF MEMS enhanced dual-hop wideband receiver [41]

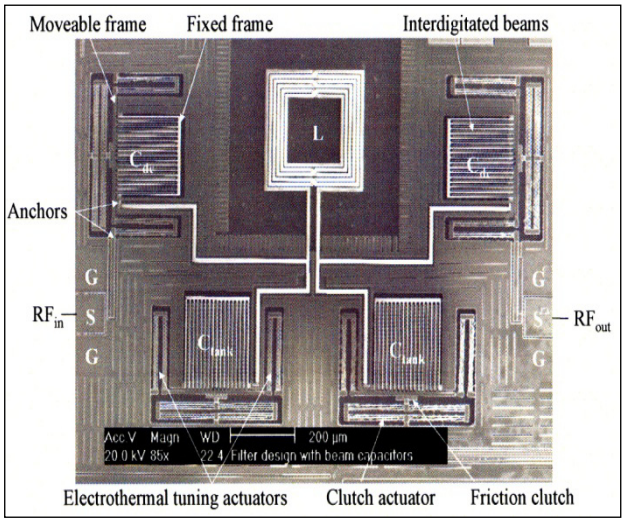


Figure 1-47 RF MEMS filter in the Jazz Semiconductor SiGe60 4-metal BiCMOS process (C_{dc} and C_{tank} switch from 550ff to 250ff and 800ff to 300ff, respectively [41]

Figure 1-49 shows a typical differential cross-coupled oscillator using SiGe BJTs to compensate the losses in a LC tank consisting of a 6.2nH symmetrical MEMS inductor and MEMS capacitors. The capacitors switch between 0.18pF and 1pF. Implementation is in the Jazz Semiconductor SiGe60 4-metal BiCMOS process with total die area 0.87 mm^2 [42].

Figure 1-50 shows the measured phase noise plot, which is typically lower than -122dBc/Hz at 1MHz offset from the carrier frequency of 2.8GHz. The DC operating point is 2.5V with a core current 1.1mA. The resulting figure of merit is 187dB.

Figure 1-51 shows a CAD simulated and measured plot of Q-factor of a RF MEMS mixer filter in the Jazz Semiconductor SiGe60 4-metal BiCMOS process.

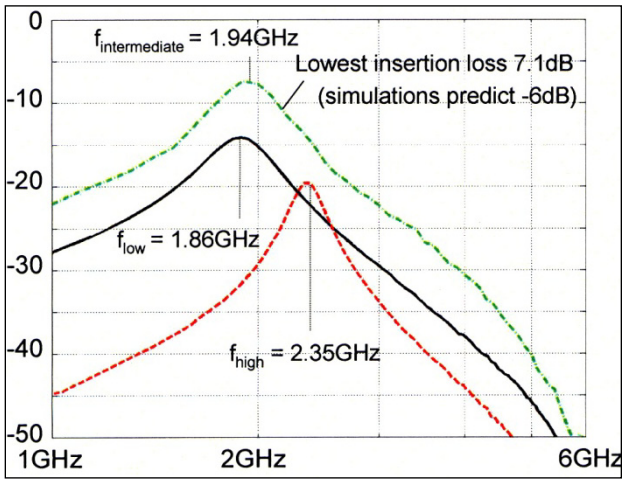


Figure 1-48 The Measured plot of insertion loss of RF MEMS filter [41]

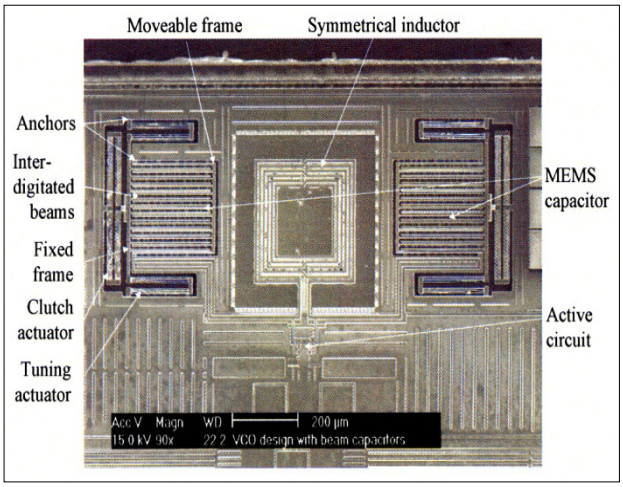


Figure 1-49 RF MEMS VCO in the Jazz Semiconductor SiGe60 4-metal BiCMOS process [41]

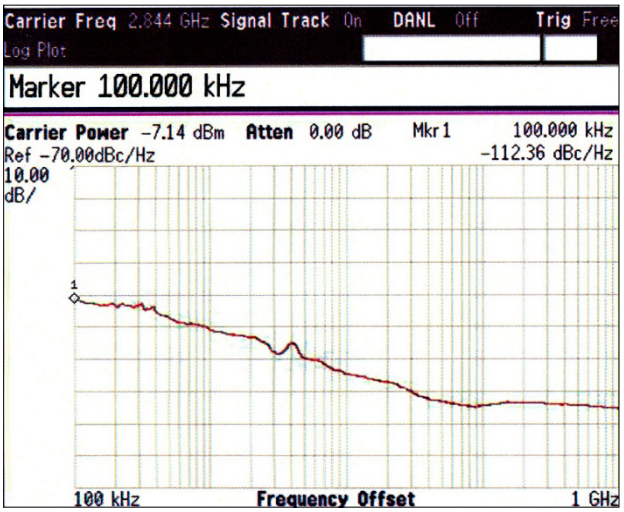


Figure 1-50 Measured phase noise of an RF MEMS VCO in the Jazz Semiconductor SiGe60 4-metal BiCMOS process [41]

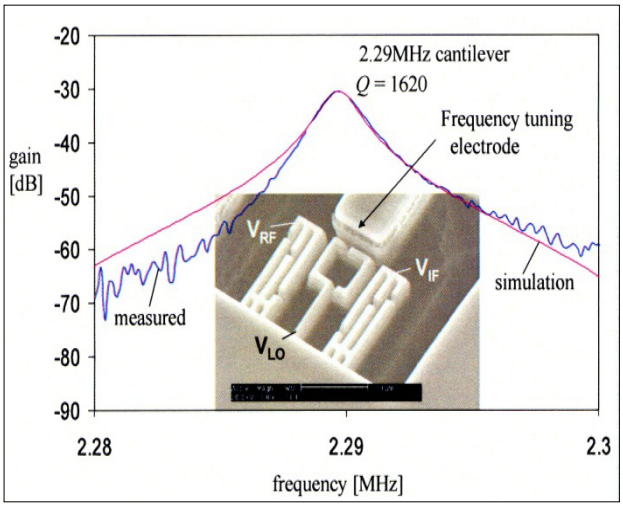
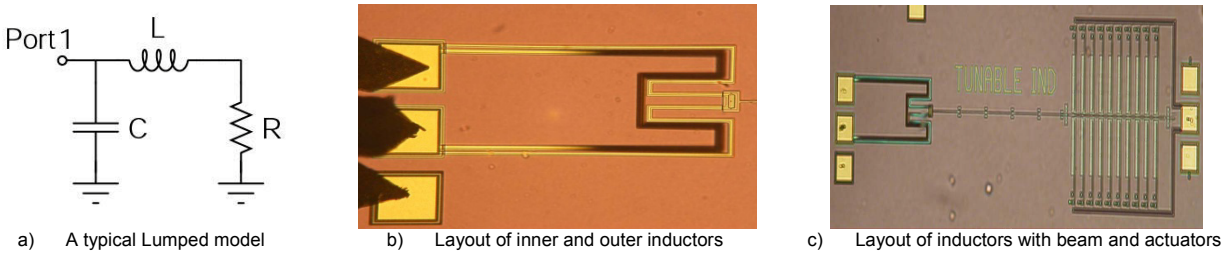


Figure 1-51 CAD simulated and measured Q of an RF MEMS mixer filter in the Jazz Semiconductor SiGe60 4-metal BiCMOS process [41]

1.7.2 Tunable Inductor Using RF MEMS Technology

Figure 1-52 shows the tunable inductor using RF MEMS technology in which tunability is achieved by incorporating thermal actuators that control the spacing between the main and secondary inductor. For planar inductors parasitic capacitance and low resistivity are the main sources of losses. By lifting the inductor off the substrate the losses can be minimized for improved quality factor. Figure 1-52 shows two inductors (inner inductor and outer inductor) that are connected in parallel. The inner inductor is raised off the substrate due to residual stress between the metal and the poly silicon layer. The outer inductor is attached to a beam, which is connected to an array of thermal actuators. When the array is actuated, the beam buckle lifts up the outer inductor. The control of the angle separating the two inductors allows tuning the mutual component of the total inductance. The OFF and ON states of the actuator correspond respectively to the maximum and the minimum inductance value. The resulting typical values for the off state are L_{off} = 1.185nH, R_{off} = 11.5Ω, C_{off} = 0.238pF and for the ON state are L_{on} = 1.045nH, R_{on} = 14.9Ω, C_{on} = 0.224pF. Notice that the resistance value is too high and the yield and realization is warranted. Low-cost packaging still remains a challenge.



a) A typical Lumped model b) Layout of inner and outer inductors c) Layout of inductors with beam and actuators

Figure 1-52 (a) Lumped equivalent model of the MEMS tunable inductor, (b) A photograph showing the two inductors with the beam and the actuator, and (c) A photograph showing the inner and the outer inductors [3].

The MEMS tunable inductor offers a cost-effective integrable solution for applications in tunable oscillators but at the cost of large series resistance and limited tuning range. In addition to this, negative mutual inductance associated with the MEMS structure can further restrict the operating frequency and tuning range, therefore they are not suitable for high frequency, low phase-noise signal-source applications.

1.7.3 Active Capacitor

Figure 1-53 shows the active capacitance circuit using BJT in common-emitter configuration where the frequency response can be controlled by adjusting feedback element (R, L, and C) [46].

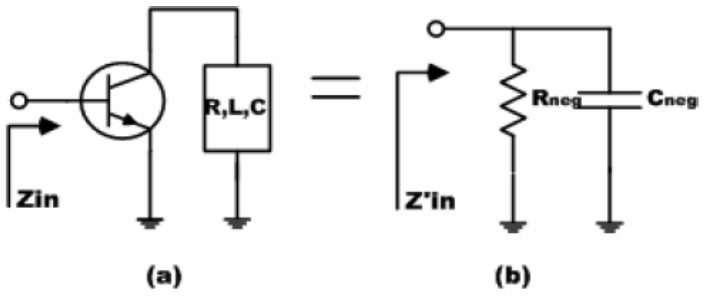


Figure 1-53 Block diagram of the proposed circuit (a) and its equivalent circuit (b) [46].

As shown in Figure 1-54, the input impedance of the circuit can be described by

$$Z_{in} = r_{bb} + r_{be} \parallel Z_{in1} \tag{1.26}$$

Where,

$$Z_{in1} = \frac{Z_1(Z_2 + Z_3)}{Z_1 + Z_2 Z_d + g_m(Z_1 \times Z_3)}$$

$$Z_1 = \frac{1}{j\omega C_{be}},\ Z_2 = \frac{1}{j\omega C_{bc}},\ Z_3 = \frac{1}{(j\omega C_{ce}) + \frac{1}{Z_d} + \frac{1}{r_0}} \text{ and } Z_d = R_d + j\left(\omega L_d - \left(\frac{1}{\omega C_d}\right)\right) \tag{1.27}$$

Since $r_{bb}, C_{ce}\ and\ r_0$ do not dominant the negative resistance and equivalent capacitance, the input admittance can be approximated as

$$Y_{in} = \frac{1}{Z_{in}} = \frac{1}{Z_{in}} = \frac{1}{R_{neg}} + j\omega C_{neg} \tag{1.28}$$

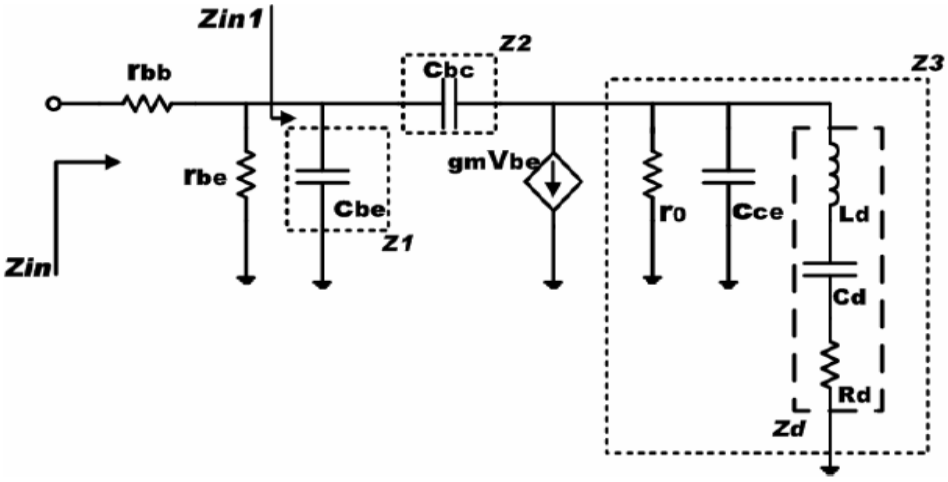


Figure 1-54 For high frequency, small signal equivalent circuit [46]

From Equation (1.28), the equivalent value of the negative resistance and capacitance can be given by

$$\frac{1}{R_{neg}} = Re[Y_{in}] = g_m + \frac{1}{r_{be}} + \frac{C_d\left(-(C_{bc}+C_d)g_m + C_{bc}C_d(g_m L_d + C_{bc}R_d)\omega^2\right)}{k} \tag{1.29}$$

$$C_{neg} = Im[Y_{in}] = \omega\left[C_{bc} + \frac{C_{bc}C_d(C_{bc}+C_d)}{k} + \frac{C_{bc}C_d\left(C_d g_m R_d - C_{bc}C_d L_d \omega^2\right)}{k}\right] \tag{1.30}$$

Where,

$$k = (C_{bc} + C_d)^2 + C_{bc}C_d(-2(C_{bc} + C_d)L_d + C_{bc}C_d R_d^2)\omega^2 + C_{bc}^2 C_d^2 L_d^2 \omega^4 \tag{1.31}$$

From Equation (1.29), the frequency range in which the circuit exhibits the negative loss resistance can be evaluated as

$$f_{\substack{high \\ low}} = \frac{1}{2\pi}\left(\frac{2C_{bc}L_d + 2C_d L_d - C_{bc}C_d R_d^2}{2C_{bc}C_d L_d^2} \pm \frac{R_d\sqrt{C_{bc}C_d}\sqrt{C_{bc}C_d R_d^2 - 4(C_{bc}+C_d)L_d}}{2C_{bc}C_d L_d^2}\right)^{1/2} \tag{1.32}$$

The frequency, which shows the maximum and minimum negative resistance, can be given by

$$f_{\substack{max \\ min}} = \frac{1}{2\pi}\left(\frac{g_m}{g_m L_d + C_{bc} R_d}\left(\frac{1}{C_{bc}} + \frac{1}{C_d}\right) \pm \frac{\sqrt{R_d^2\left(C_{bc}^2 + C_d^2\right)\left[C_{bc}^2 + C_d g_m^2 L_d + C_{bc}\left(C_d + C_d g_m R_d\right)\right]}}{C_{bc} C_d L_d \left(g_m L_d + C_{bc} R_d\right)}\right)^{1/2} \quad (1.33)$$

The dynamics of the negative resistance network can be stabilized by properly optimizing the behavior estimated by Equation (1.29) – Equation (1.33). Figure 1-55 shows the comparative plots of CAD simulated and measured impedance data of an active capacitance network for the given feedback parameters: L=23nH, C=10pF and R=46 Ω [46].

As shown in Figure 1-55, the measured active capacitance circuit behaves as a parallel network, consisting of frequency dependent equivalent capacitance and negative resistance, thereby, typically suitable for narrow band applications.

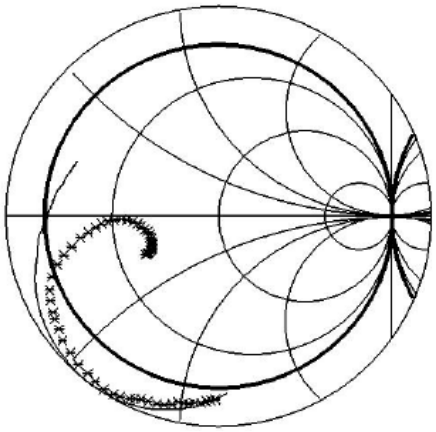


Figure 1-55 Simulated and measured input impedance of an active capacitance circuit using BJT [46].

1.7.3.1 Diplexer using Active Capacitor Circuit

Figure 1-56 shows the typical example of active duplexer using the active capacitance network of Figure 1-53 (implemented by Infineon SiGe HBTs, BFP 620F).

As illustrated in Figure 1-56, an active diplexer consists of two active BPFs at the cellular Rx/Tx bands. The active duplexer is designed at the Rx band (824~849 MHz) and the Tx band (869~894 MHz), and fabricated using lumped components with the design parameters given in Table 1-6 [46]. Figure 1-57 shows the typical layout of the active duplexer circuit. The DC bias condition is 1V at 5mA.

Figure 1-58 shows the CAD simulated results for the Rx and Tx active BPFs. The duplexer insertion loss is typically less than 1dB and a return loss of 13dB [46].

Table 1-6 Design Parameters [46]

	Feedback element	Matching network
Rx BPF	$R'_d = 5\Omega$ $L'_d = 15nH$ $C'_d = 6pF$	$C \parallel L = 2.4pF \parallel 13nH$ (optimized)
Tx BPF	$R_d = 5\Omega$ $L_d = 13.5nH$ $C_d = 6pF$	$C \parallel L = 3pF \parallel 13nH$ (optimized)

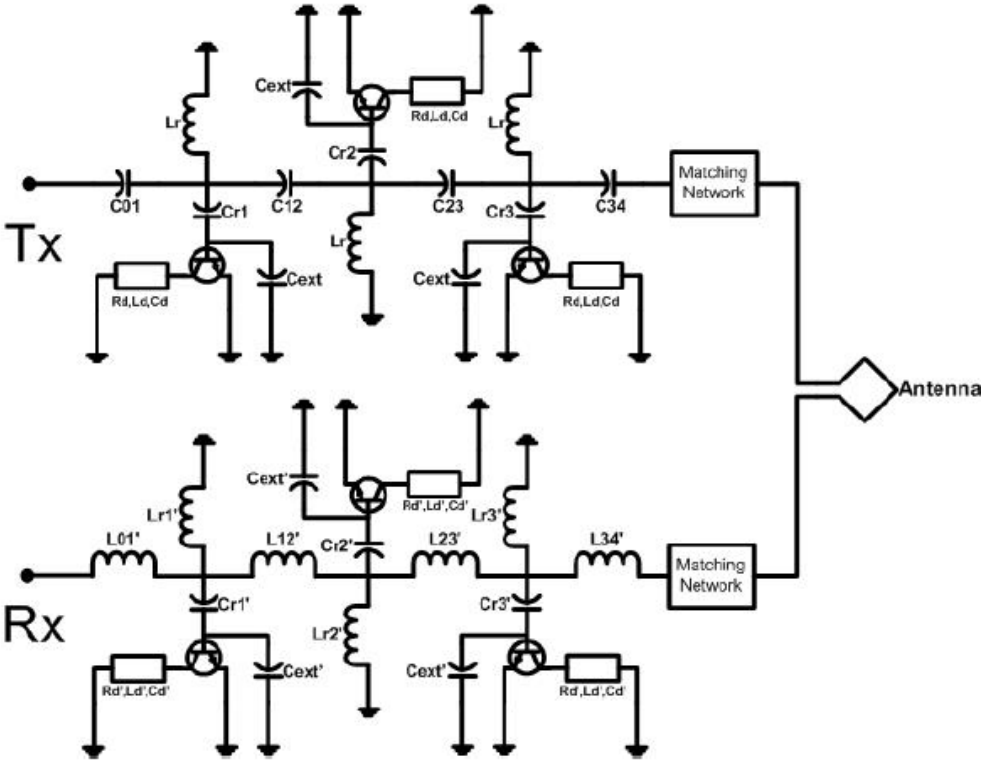


Figure 1-56 Schematic diagram of an active duplexer [46].

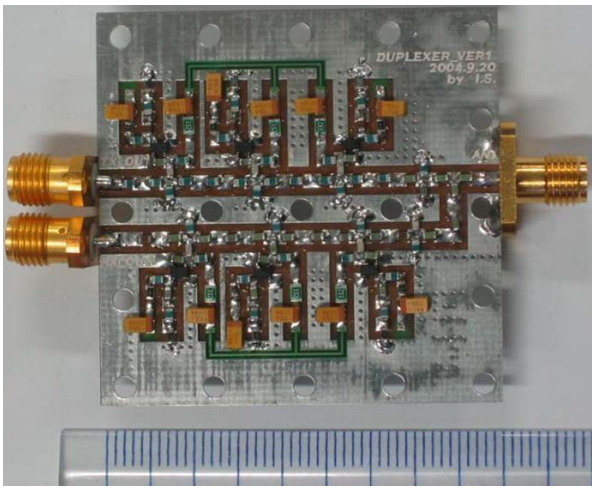


Figure 1-57 Photograph of the fabricated active duplexer [46].

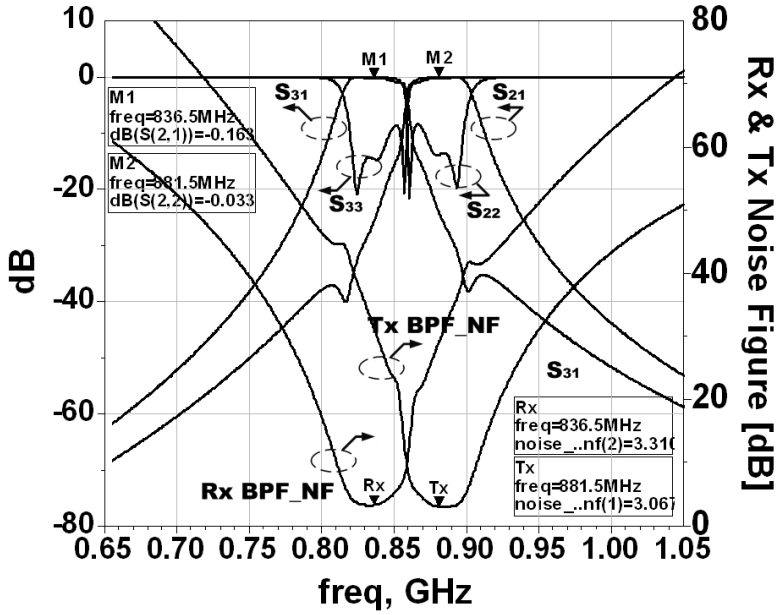


Figure 1-58 Simulated S-parameters and NF of the active duplexer (1: Antenna port, 2: Tx port, 3: Rx port) [46].

1.7.3.2 Oscillator using Active Capacitor Circuit

Figure 1-59 shows the typical Clapp-Gouriet oscillator using the active capacitance in a high-performance oscillator circuit [48]. Transistors Q1 exhibits a negative resistance at its base terminal for a given frequency range and Q2 acts as a current source. The negative impedance at the input terminal is generated by capacitive feedback. The circuit can be loaded for stable RF output at the collector terminal of Q1 (Figure 1-62). From Figure 1-69, the input impedance can be approximately given by

$$Z_{in} \approx -\frac{g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega\left(\frac{C_1 C_2}{C_1+C_2}\right)} \tag{1.34}$$

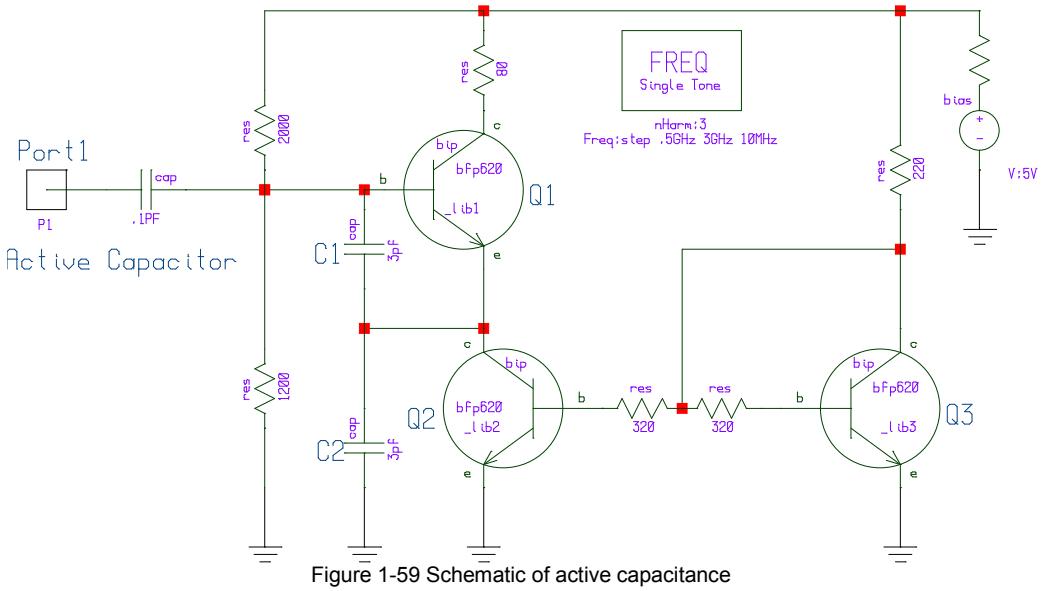


Figure 1-59 Schematic of active capacitance

Figures 1-60 and 1-61 show simulated plots of the negative loss resistance and capacitive impedance at Port 1 for a given operating frequency of 500 MHz to 3GHz. Care must be taken while optimizing the feedback capacitor C1. The base to emitter capacitance of transistor Q1 may dominate C1 and must be taken into account.

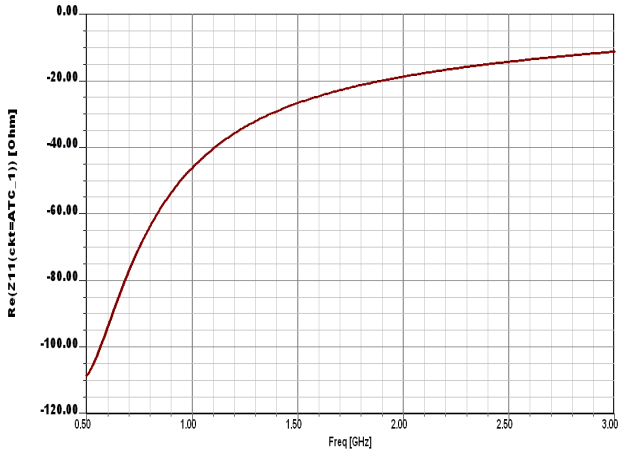


Figure 1-60 Simulated plot of Re [Z_{11}], shows the negative input resistance at Port 1

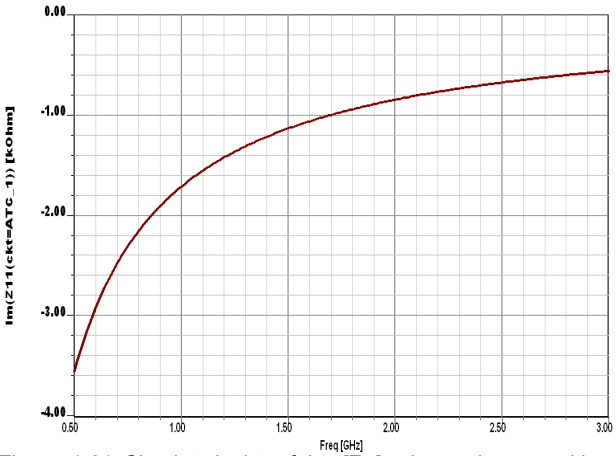


Figure 1-61 Simulated plot of Im [Z_{11}], shows the capacitive characteristics at Port 1

Figure 1-62 shows a 2000 MHz oscillator schematic using the active capacitance network of Figure 1-59 for the validation of the active capacitance in a high performance oscillator. As shown in Figure 1-63, the CAD simulated phase noise performance @ 10 kHz offset is better than -122dBc/Hz, indicating a cost-effective and promising topology for application in modern wireless communication systems.

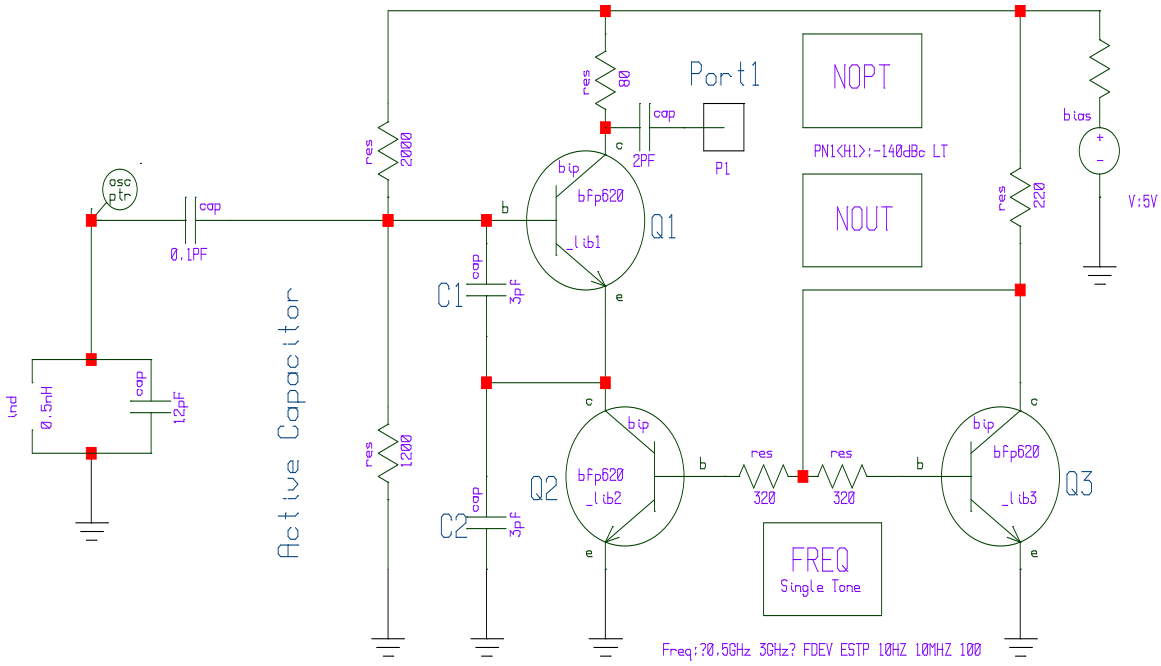


Figure 1-62. 2000 MHz oscillator schematic using an active capacitance network

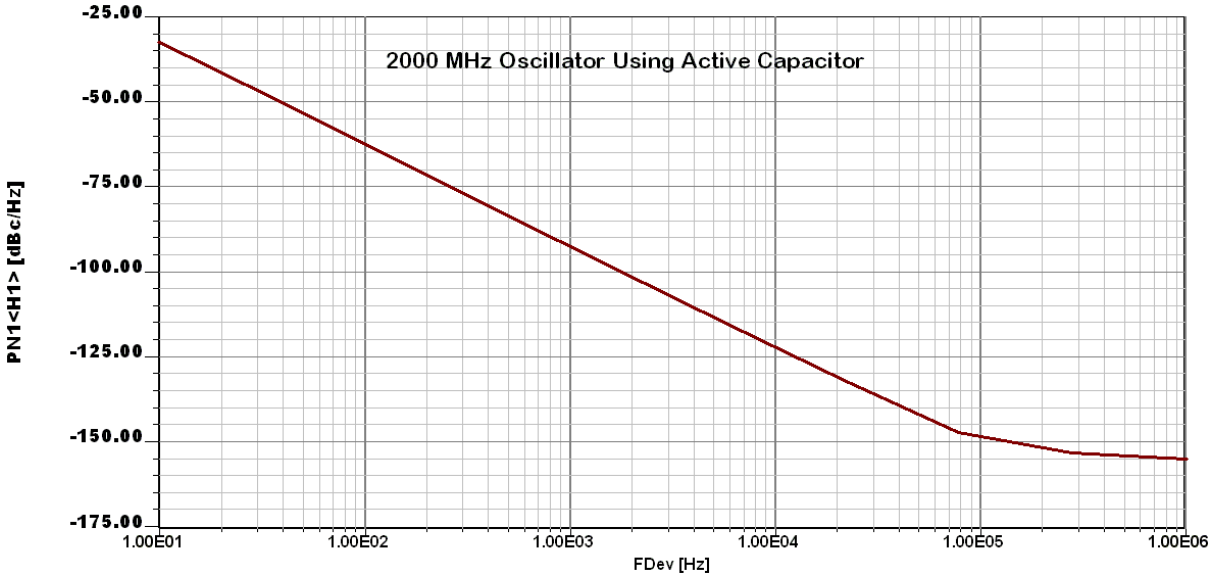


Figure 1-63 The CAD simulated phase noise performance of the 2000 MHz oscillator (Figure.1-62)

Although, the oscillator circuit shown in Figure 1-62 is a cost-effective alternative of SAW and ceramic resonator frequency references, the lack of tunability is restrictive. Frequency lock to a reference using PLL is still needed to counteract the effect of frequency drift caused by component tolerances, extreme operating temperature, package parasitics, and aging.

1.7.3.3 Tunable Oscillator using Active Capacitor Circuit

Figure 1-64 shows the typical tunable active capacitance network using a varactor diode for the realization of tunable oscillator circuits [47, 49].

Figure 1-65 shows a broadband oscillator circuit using an active tunable capacitor network. The main drawback of this topology is the limited tuning and stability over the desired operating frequency and temperature, which stems from the active capacitor that comprises the resonator network.

To overcome the limited tunability characteristics, the concept of the tunable active inductor oscillator has been reported throughout the short history of electronics [1]-[5]. The next chapter provides an in-depth treatment of the principles, topologies, characteristics, and implementation of active tunable inductor circuits for applications in broadband oscillator circuits.

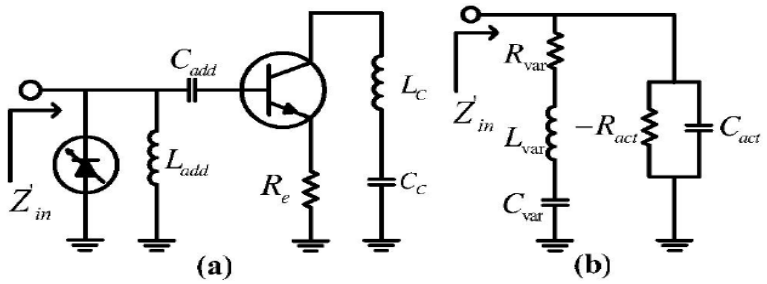


Figure 1-64 (a) A tunable capacitance circuit using a varactor and (b) its equivalent circuit

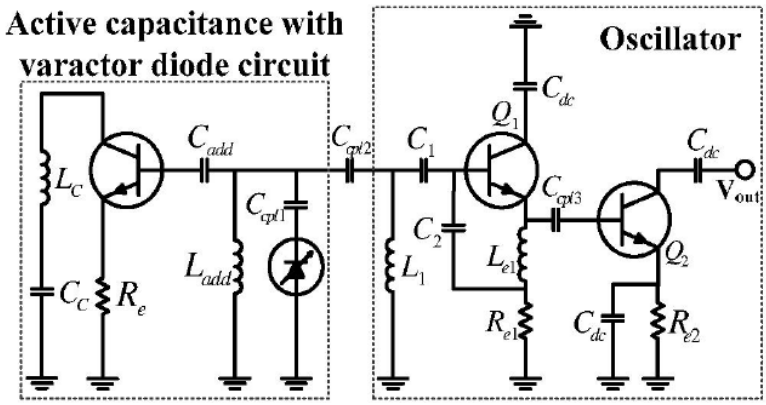


Figure 1-65 A narrow band oscillator with the an active capacitance circuit and varactor diode circuit (excluding the bias circuit).

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2. Oscillator Theory

2.1 Microwave Oscillator

Microwave oscillators typically consist of an active device, bipolar transistor or FET. The oscillator is a device that transfers DC power into RF power at the frequency of the resonator using the active device in a feedback amplifier, with positive feedback that generates a negative (time average noisy) resistance [1]. The use of negative resistance devices like a tunnel diode, Gunn diode or IMPATT diode have become unattractive as they are one terminal devices and require complicated biasing and decoupling. A key factor for oscillators is the single-sideband (SSB) phase noise and the tuning range, which describes the noise of an oscillator at different offsets from the carrier.

The major noise contributors are the noise sources in the active device, namely the thermal noise, the Schottky noise and the flicker noise. The flicker noise depends on the transistor type and its biasing. The noise contribution from the resonator is mainly thermal noise. The best phase noise is at wide offsets of the carrier; the best number being $Pout\ (dBm) - kTo\ (-174dBm) + NF$ (large signal NF of the oscillator transistor in dB) all per 1Hz bandwidth. In the case of a lossy (noisy) resonator, the operating Q is much less than 100 and therefore the far off noise is not very much attenuated.

Research has also shown that injection-locked symmetrical circuits offer lowest SSB phase noise for a given figure-of-merit (FOM). For example, push-push and push-pull circuits are more difficult to optimize in discrete topology for best phase noise performance and tuning characteristics due to the limitation of locking range; this work will focus on the asymmetrical Colpitts topology for giving detailed insights about the passive lumped inductor and active inductor based oscillator design. Why is the Colpitts oscillator so popular? To begin with, it is an emitter follower, which has a voltage gain of slightly less than one but provides very low output impedance and high power gain. The internal phase shift is very little, $f_{\max} >> f_{3\text{dB}}$, and therefore stable operation over a wide frequency range is possible.

Active inductor circuits can provide negative resistance and an inductive reactance. Past attempts to develop an oscillator based on an active inductor have failed because the combination of an active inductor with a negative resistance as replacement of a passive inductor failed to provide stable operation due to multi-mode resonance and resulted in excessive noise and power dissipation.

The circuit providing the active inductor must also be able to handle the same level of RF current we find in a passive inductor in the resonator. The question of the dynamic performance must therefore be considered for the application in tunable filter, phase shifter, matching network, and oscillator circuits.

The next difficulty is the fact that while a noise equation for the single transistor was found, it is not obvious how to solve the noise correlation of a multi-transistor circuit where the solution has to be found in the time rather than in the frequency domain [2, pp. 159-183]. Such a solution has

to integrate all the noise sources. This includes thermal noise (resonator, base spreading resistance), Schottky noise and current dependent flicker noise.

The resulting expression for the "active" inductor is a function of frequency, voltage, and current and can be designed monotonically increasing or decreasing with respect to tuning voltage depending upon the circuit topology. A key component for the motivation of an active inductor is significant size reduction as compared to spiral inductor, shown in Figure 2-1, where more than 50% of the active area is the spiral-tapped inductor. Oscillators using active inductors will compete well with standard integrated solutions at much lower cost.

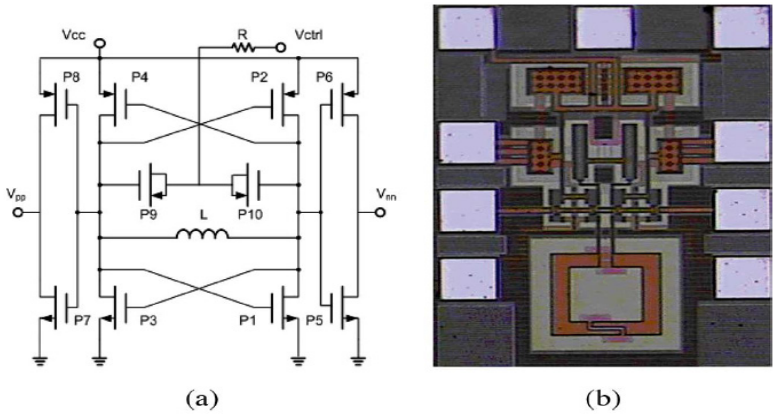


Figure 2-1. A typical cross-coupled differential VCO (1.69-2.1375 GHz) in standard CMOS 0.18 μm technology: (a) circuit model and (b) top view of the sample (die area: 365x504 μm^2), more than 50% of the active area is the spiral tapped-inductor [10].

Varactors at frequencies above 10 GHz are typically GaAs. These are expensive and have a medium Q factor. If a tunable inductor can be used together with a fixed high Q capacitor, varactors can be avoided with their associated high cost and dependence on a single manufacturer.

Even at this stage, the resulting SSB phase noise will not be sufficient. Rigorous analysis using analytical methods followed with optimization using frequency-domain (Harmonic Balance) simulators for obtaining canonical form, improved phase noise, and better dynamic range, are needed.

2.1.1 Some comments on frequency-domain (harmonic balance) simulators

The first analysis often performed by most engineers is a brief assessment using linear mathematics. The real noise analysis considering all effect must be done either with large-signal analysis using analytic equations (an attempt will be demonstrated here by developing a non-linear approach) or a harmonic-balance simulator. There are problems with these, which will be pointed out.

In the harmonic-balance analysis method, the linear calculations are done in the frequency domain, the non-linear calculation in the time domain. This method is several hundred times faster than the conventional time-domain SPICE method.

There are two techniques in use to transform between the time-domain nonlinear model and the frequency-domain evaluation of the harmonic currents of the linear network. One technique is

the Almost Periodic Discrete Fourier Transform technique (APDFT) and the other is the Multi-dimensional Fast Fourier Transform technique (MFFT) using quasi-analytic or analytic derivatives to evaluate the Jacobian matrix. The first one, which has a somewhat random sampling approach, has a typical dynamic range of 75 to 80dB, while the second one offers greater than 180dB dynamic range. Harmonic-balance analysis in recent years has greatly improved the speed and size of the problem that can be handled, but matrix solution remains the key problem.

It is important to be able to accurately predict a small signal in the presence of a large signal for mixer and intermodulation analysis, which also includes the calculation of noise in oscillator circuits. To reliably predict this, the dynamic range (the ratio of a large signal to a minimally detectable small signal) needs to be more than 175dB. The APDFT technique has a dynamic range of 75dB while the MFFT has a dynamic range of 190dB. Calculations for oscillators require a noise floor of –174dBc/Hz as the lower reference and the carrier level, which can be as high as +20dBm, indicates up to 190dB dynamic range is required. Therefore, a numerically stable approach is the need of the hour.

2.2 Passive LC Resonator Oscillator

It is well-known that the Colpitts oscillator topology is essentially an emitter follower stage with feedback that provides negative resistance for compensating the resonator loss (positive loss resistance associated with passive lumped inductor) and exhibits a nearly constant voltage gain A_v.

2.2.1 The Three-Reactance Oscillators Using *Y*-Parameters, Colpitts circuit

Although the current formulation of the stability (oscillation) condition (Y_1) is the easiest to express graphically, it is frequently difficult to apply, since it is often difficult to identify the actual required values of the components. A direct analysis of the circuit equations is frequently mathematically simple.

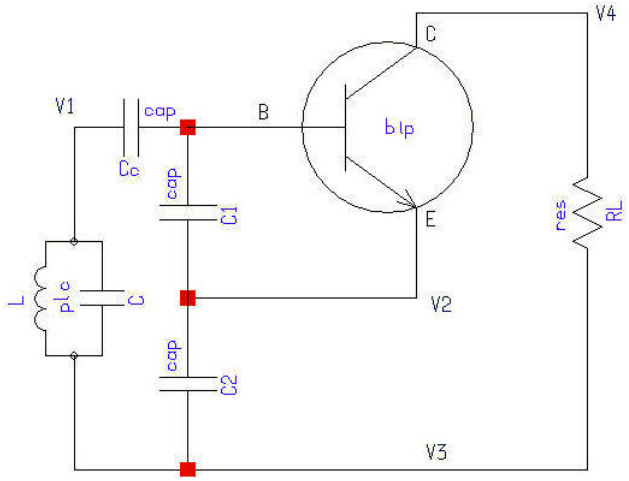


Figure 2-2 General topology of the Colpitts oscillator.

Figure 2-2 shows a simplified Colpitts oscillator circuit for the formulation of stable oscillation condition. It has a capacitive feedback network, C_1 and C_2, and a tuned circuit, which is built

from the inductor L and the capacitor C then coupled to the transistor circuit via a coupling capacitor C_C. Figure 2-2 can be redrawn by putting the tuned circuit with its coupling capacitor between base and collector. The feedback capacitor C_1 now is in parallel to the base-emitter junction, and the feedback capacitor C_2 is in parallel to the collector-emitter connection. A load resistor marked R_L in parallel with C_2 is also assumed as shown in Figure 2-3. C_1, C_2 and the tuned circuit are now shown in Y parameter form. For this early introduction, the transistor is also assumed ideal, meaning that $Y_{12} = 0$, and $Im[Y11] = Im[Y22] = 0$. Later we will reformulate without these assumptions. Figure 2-3 shows the feedback circuit with three parallel admittances. Y_2 can be either a susceptance or a more complex circuit such as a resonance circuit with a capacitance in series. In the case of a crystal oscillator, Y_2 is a series resonant circuit with a parallel capacitor, which comes from the crystal holder. The voltages V_1, V_2, and V_3 are measured relative to ground. The circuit is assumed floating.
It can be shown that:

$$\begin{bmatrix} (Y_1 + Y_2 + Y_i) & -Y_2 \\ -(Y_2 - Y_{21}) & (Y_2 + Y_3) \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = 0 \qquad (2\text{-}1)$$

In this equation Yi = Y11 and Y21 are the Y-parameters of the transistor.

In order for this circuit to oscillate, it must satisfy the matrix condition [Y][V] = 0 for a non-zero value of [V] (output power). Assuming the feedback circuit has lossless components, then

$$\begin{aligned} &(Y_2 + Y_3)(Y_1 + Y_2 + Y_i) - Y_2(Y_2 - Y_{21}) = 0 \\ &Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + Y_iY_2 + Y_iY_3 + Y_2Y_{21} = 0 \end{aligned} \qquad (2\text{-}2)$$

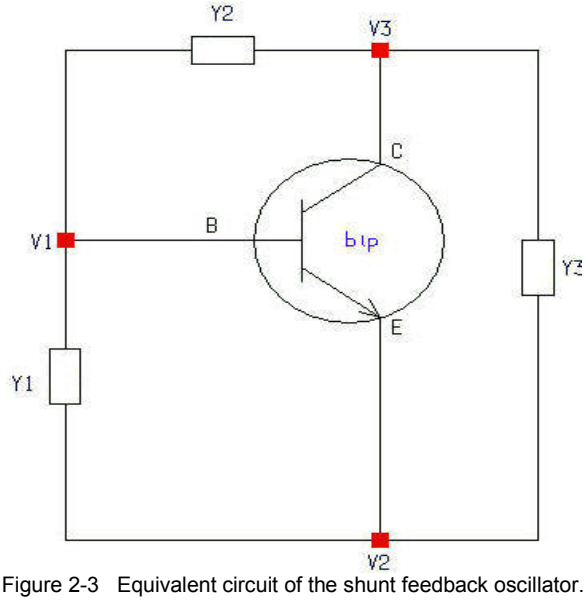


Figure 2-3 Equivalent circuit of the shunt feedback oscillator.

If the feedback network has ideal reactive components and Y11 = real, then

$$Y_i = G_i, Y_1 = jB_1, Y_2 = jB_2, Y_3 = jB_3 \qquad (2\text{-}3)$$

and the equation above is further simplified to:

$$\begin{aligned} &-B_1B_2 - B_1B_3 - B_2B_3 + jB_2G_i + jB_3G_i + jB_3Y_{21} = 0 \\ &-(B_1B_2 + B_2B_3 + B_1B_3) + j(B_2G_i + B_3G_i + B_3Y_{21}) = 0 \end{aligned} \tag{2-4}$$

From the equation above, the real and imaginary part will need to be zero separately to satisfy det [Y]=0.

$$\begin{aligned} &B_1B_2 + B_2B_3 + B_1B_3 = 0 \Rightarrow \frac{1}{B_1} + \frac{1}{B_2} + \frac{1}{B_3} = 0 \\ &Y_{21}B_3 + G_iB_3 + G_iB_2 = 0 \Rightarrow \frac{1}{B_3} + \left(1 + \frac{Y_{21}}{G_i}\right)\frac{1}{B_2} = 0 \end{aligned} \tag{2-5}$$

If we convert susceptance to reactance, and let

$$X_1 = \frac{1}{B_1}, X_2 = \frac{1}{B_2}; X_3 = \frac{1}{B_3} \quad \text{and} \tag{2-6}$$

$$X_1 + X_2 + X_3 = 0 \Rightarrow X_3 + \left(1 + \frac{Y_{21}}{G_i}\right)X_2 = 0 \tag{2-7}$$

$$\text{then} \qquad \frac{Y_{21}}{G_i} = \frac{X_1}{X_2} \Rightarrow \frac{Y_{21}}{Y_{11}} \tag{2-8}$$

Feedback conditions:

$$\frac{C_2}{C_1} = \frac{Y_{21}}{Y_{11}} \tag{2-9}$$

If Y_{21} and G_i are positive (simplified transistor model), it is implied that X_1 and X_2 have the same sign, and therefore, either capacitors or inductors. $X_1+ X_2+ X_3=0$, implies that X_3 must be opposite in sign from X_1 and X_2, and therefore, the opposite type of component.

$$\begin{aligned} &X_1 + X_2 + X_3 \Rightarrow \frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L_3 = 0 \rightarrow \text{Colpitts oscillator} \\ &\omega = \sqrt{\frac{1}{L_3}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} \text{ angular frequency, resonant condition} \end{aligned} \tag{2-10}$$

For complex value of Y_3 (Lossy Inductor):

$$\begin{aligned} &Y_3 = G_3 + jB_3 \Rightarrow Y_3 = \frac{1}{Z_3} \\ &Z_3 = R + j\omega L_3 \\ &\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + \frac{G_iR}{j\omega C_1} + j\omega L_3 = 0 \\ &\omega = \sqrt{\frac{1}{L_3}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{G_iR}{C_1}\right)} \Rightarrow \omega = \sqrt{\frac{1}{L_3}\left(\frac{1}{C_1'} + \frac{1}{C_2}\right)} \end{aligned} \tag{2-11}$$

where

$$C_1' = \frac{C_1}{1 + G_iR} \qquad \text{and} \tag{2-12}$$

$$\frac{R}{G_i} = \left(\frac{(1+\frac{Y_{21}}{G_i})}{\omega^2 C_1 C_2} \right) - \frac{L_3}{C_1} \tag{2-13}$$

For steady oscillation, the following condition has to be satisfied:

$$R_{Loss} < G_i \left[\frac{(1+\frac{Y_{21}}{G_i})}{\omega^2 C_1 C_2} - \frac{L_3}{C_1} \right] \tag{2-14}$$

Since $\frac{Y_{21}}{G_i}$ is the frequency dependent current gain β:

$$R_{Loss} < \left| \text{real}\left(Y_{11} \left[\frac{(1+\beta)}{\omega^2 C_1 C_2} - \frac{L_3}{C_1} \right] \right) \right| \tag{2-15}$$

A similar approach is found in [2].

2.2.2 Large-signal oscillator analysis

Figure 2-4 shows the typical Colpitts oscillator with base lead inductance and package capacitance.

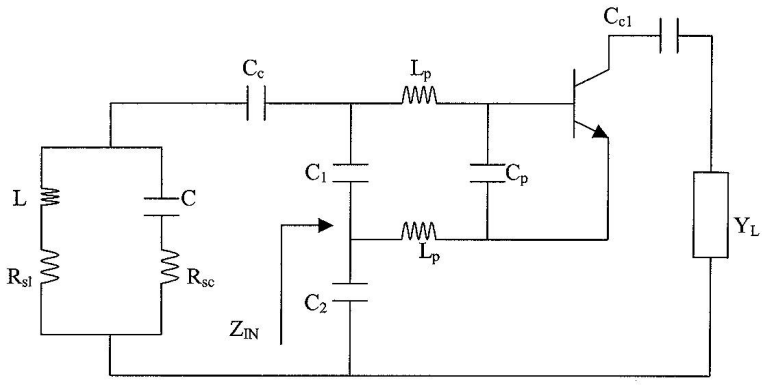


Figure 2-4 Typical Colpitts oscillator with base lead inductance and package capacitance

From figure 2-4, the expression of input impedance is given as [2, pp. 89]

$$Z_{IN}|_{pacakage} = -\left[\frac{Y_{21}}{\omega^2 (C_1 + C_p) C_2} \frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)} \right] - j\left[\frac{(C_1 + C_P + C_2)}{\omega (C_1 + C_P) C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)} \frac{Y_{21}}{\omega (C_1 + C_P) C_2} \right] \tag{2.16}$$

$$Z_{IN}|_{without-pacakage} = -\left[\frac{Y_{21}}{\omega^2 C_1 C_2} \right] - j\left[\frac{(C_1 + C_2)}{\omega C_1 C_2} \right] \tag{2.17}$$

Time mathematical expression of the time-domain analytical solution [2, pp.113]

$$Y_{21}|_{large-signal} = G_m(x) = \frac{qI_{dc}}{kTx} \left[\frac{2I_1(x)}{I_0(x)} \right]_{n=1} = \frac{g_m}{x} \left[\frac{2I_1(x)}{I_0(x)} \right]_{n=1} \tag{2.18}$$

Where

$$G_m(x) = \frac{1}{R_P}\frac{[C_1 + C_2]^2}{C_1 C_2} \tag{2.19}$$

From (2.18) and (2.19)

$$\frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} = \frac{1}{R_P}\frac{[C_1 + C_2]^2}{C_1 C_2} = \frac{1}{R_P}\frac{C_1}{C_2}\left[1 + \frac{C_2}{C_1}\right]^2 \tag{2.20}$$

$$\frac{C_1}{C_2}\left[1 + \frac{C_2}{C_1}\right]^2 = \frac{R_P g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \tag{2.21}$$

From (2.21)

$$\frac{R_P g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \leq \frac{C_1}{C_2}\left[1 + \frac{C_2}{C_1}\right]^2 \leq R_P g_m \tag{2.22}$$

$$x = \frac{g_m\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1}}{\left(\frac{1}{R_P}\frac{C_1}{C_2}\right)\left(1 + \frac{C_2}{C_1}\right)^2} \tag{2.23}$$

The value of $\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1}$ increases monotonically as the drive level x increases, and for large values of *x* and C2 <C1, n>1, the dependence of x can be expressed as

$$x = \frac{R_P G_m C_2}{C_1} \tag{2.24}$$

For large drive level, $x \propto C_2$, and the corresponding conduction angle of output current is given as

$$\varphi = \cos^{-1}\left[1 + \frac{\ln(0.05)}{x}\right] \Rightarrow \varphi \approx \cos^{-1}\left[1 - \frac{3}{x}\right] \tag{2.25}$$

$$\varphi = \cos^{-1}\left[1 - \frac{C_1}{3R_P G_m C_2}\right] \tag{2.26}$$

$$\varphi \propto \frac{1}{C_2} \tag{2.27}$$

$$x \propto C_2 \tag{2.28}$$

Normally, the value of C_1 is kept fixed to avoid loading by the transistor. By increasing the value of C_2, the conduction angle can be reduced, thereby, shortening the output current pulse. Any change in designed frequency, due to the variation of C_2, can be compensated by changing the value of the resonator inductance without much change of the value of the drive level x.

The following shows an example for a 100 MHz and a 1 GHz oscillator circuit for different normalized drive levels x. This is provided to give some insight into the relationship between the drive level, the current pulse, and the phase noise.

Figure 2-5 shows the circuit diagram of a 100MHz Colpitts oscillator with a load of 500Ω. To simplify the explanation, a 100MHz frequency has been selected; the transistor parasitics do not play a major role at such a low frequency. For this example, a NEC85630 transistor was chosen. The emitter to ground capacitor determines the normalized drive level x. As the drive level x produces narrow pulses, the phase noise improves. This can be seen in Figure 2-6.

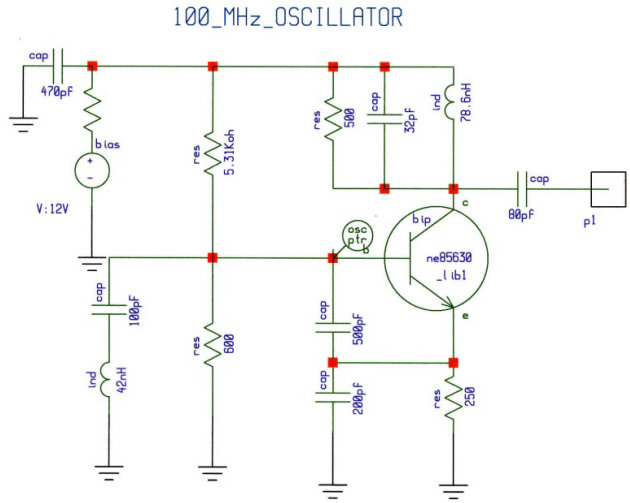
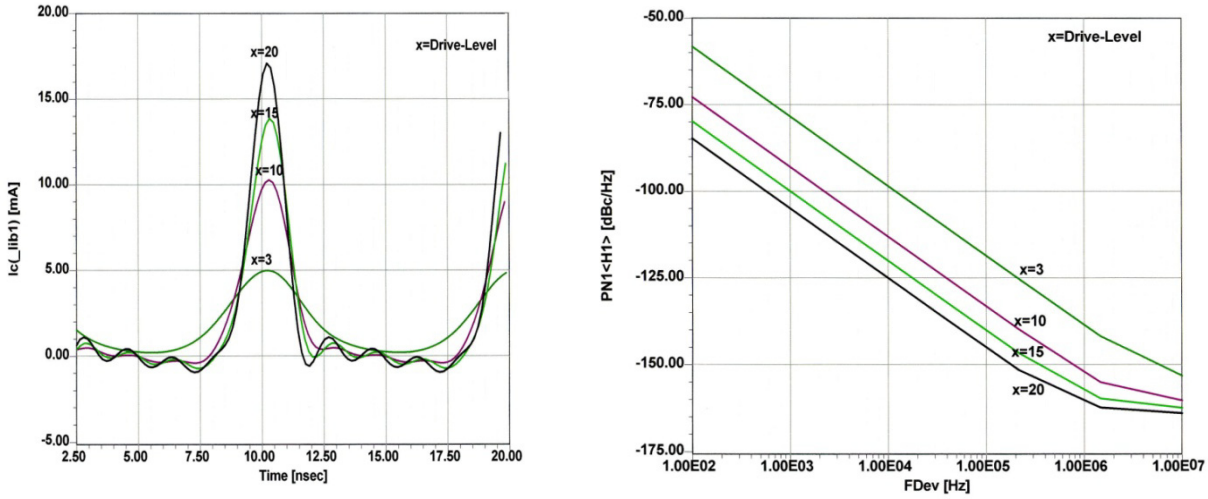


Figure 2-5 The circuit diagram of a 100 MHz Colpitts oscillator with a load of 500Ω.



(a) (b)

Figure 2-6 The RF current (a) and single sideband phase noise (b) as a function of the normalized drive level x.

2.2.3 Phase Noise

The mathematical solution for phase noise dynamics of the Colpitts oscillator have been found and published in [2, pp.176-184]. Other circuit configurations are noisier; also SiGe transistors

are preferred over Si-BiCMOS. The Phase noise, expressed in £ (f) is measured in dBc/Hz off the carrier and can be given by [2, pp. 181]

$$£(\omega) = 10 \times \log\left[\left[k_0 + \left(\frac{\omega^2 k^3 k_1 \left[\frac{Y_{21}^+}{Y_{11}^+}\right]^4 [y]^{4p}}{\left[Y_{21}^+\right]^6 [y]^{6q}} \right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\left[\frac{Q_{un}}{Q_l}\right]^2\right] \quad (2.29)$$

Where

$$k_0 = \frac{kTR}{\omega^2\, \omega_0^2 L^2 V_{cc}^2 C_2^2} \qquad k_1 = \frac{qI_c g_m^2 + \frac{K_f I_b^{AF}}{4\omega} g_m^2}{\omega^2\, \omega_0^4 L^2 V_{cc}^2} \qquad k_2 = \omega_0^4 (\beta^+)^2 \qquad k = \frac{k_3}{k_2 C_2^2} \qquad y = \frac{C_1}{C_2}$$

Figure 2-7 shows the simulated phase noise and its minimum for two values of C_1, 2pF and 5pF. 5pF provides a better phase noise and a flatter response. For larger C_1, the oscillator will cease to oscillate.

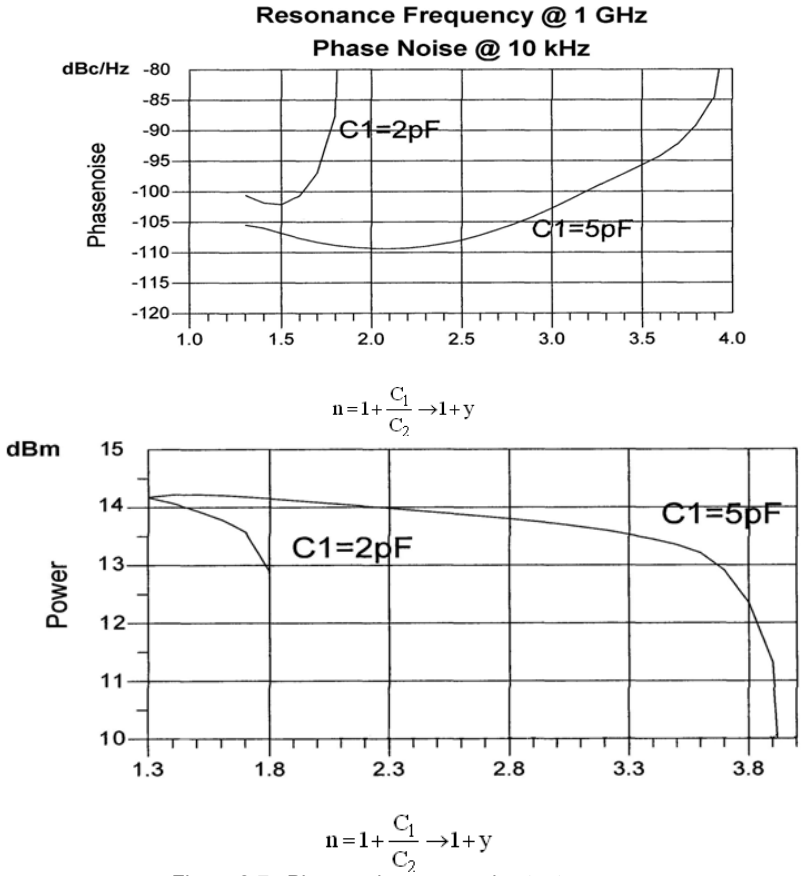


Figure 2-7 Phase noise vs. *n* and output power.

For the minimum phase noise condition,

$$\frac{\partial\left|\phi^2(\omega,y,k)\right|}{\partial y}\Rightarrow 0 \tag{2.30}$$

$$\frac{\partial}{\partial y}\left[\left[k_0+\left(\frac{\omega^2 k^3 k_1\left[\frac{Y_{21}^+}{Y_{11}^+}\right]^4[y]^{4p}}{\left[Y_{21}^+\right]^6[y]^{6q}}\right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\left[\frac{Q_{un}}{Q_l}\right]^2\right]_{y=m}\Rightarrow 0 \tag{2.31}$$

From curve-fitting attempts, the following values for q and p in Equation (2.31) were determined:

$$q=1 \text{ to } 1.1;\ p=1.3 \text{ to } 1.6.$$

q and p are a function of the normalized drive level x and need to be determined experimentally. The transformation factor n is defined as,

$$n=1+\frac{C_1}{C_2}\rightarrow 1+y \tag{2.32}$$

The following plot in Figure 2-8 shows the predicted phase noise resulting from Equation (2.31). Although, Equation (2.29) is approximate formulation of the noise dynamics the key contributors are still the resonator noise and the flicker noise. The Schottky noise dominates at larger offset frequencies. The break point for the flicker noise can be clearly seen in the Figure 2-8. From Equation (2.29) - Equation (2.31), the feedback capacitor C_2 has more influence compared to C_1. The drive level and conduction angle of the Colpitts oscillator circuit is a strong function of C_2. This approach has provided us with a design guide for the key components of the oscillator; however, it did not include all the noise sources of the transistor.

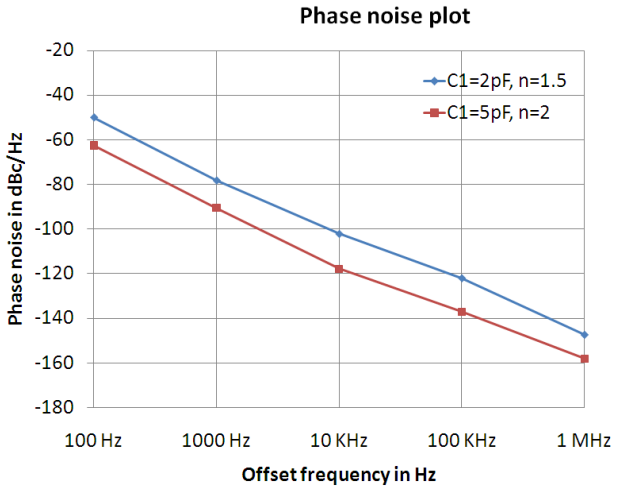


Figure 2-8- Using Equation (2.31), the phase noise for different values of *n* for constant C_2 can be calculated.

2.3. Tunable Voltage-Controlled Oscillators

Tunable voltage-controlled oscillator (VCO) with wide tuning range and low phase noise is the essential building block for next-generation wireless communication systems. The VCO is one of the most important blocks of the phase-locked-loop (PLL)-based frequency synthesizer because its performance is determined inside the loop bandwidth by the loop and outside the loop bandwidth by the phase noise of VCO. It is, therefore, of major importance to build a low-phase-noise integrated wideband oscillator also operating with low power consumption.

Conventional tunable oscillator design for wideband voltage controlled oscillator use a grounded base or grounded collector circuit for generating a negative resistance at one port, which is usually terminated with a parallel or series LC-resonant circuit. The main problems in this design are to generate negative resistance over the wide tuning range, which cannot be easily extended to an octave-tuning band. For octave band tunability, the required negative resistance over the band is generated by the feedback base-inductance (in the grounded base topology). However, the polarity of the reactance may change over the frequency band and can lead to the disappearance of the negative resistance as the operating frequency exceeds its self-resonant frequency (SRF). Furthermore, the low Q of commercially available SMD inductors and tuning diodes degrade the phase noise performance over the band.

The quality factor is important to understand the characteristics of the resonant circuit used in the oscillator. It is a measure of the ideality of a reactive component or circuit from the standpoint of internal energy loss. The larger the value of Q factor, the more ideal is the behavior of the resonator component.
Q has several definitions:

(1) It is 2π times the ratio of the peak energy stored and the average power dissipated per cycle or ω times the ratio of the peak energy stored and the average power dissipated for components or circuits that store magnetic, electric or both, energy.
(2) It is the ratio of the resonance frequency to the -3dB bandwidth of that resonance in RLC resonant circuits, and is used as a measure of the ideality of series or parallel resonant circuits from the standpoint of frequency selectivity.
(3) It is defined as a

$$\mathrm{Q} = -\frac{\omega_0}{2}\left[\frac{\mathrm{d}\theta}{\mathrm{d}\omega}\right]_{\omega=\omega_0} \tag{2.33}$$

where ω_0 is the resonance frequency and $\frac{\mathrm{d}\theta}{\mathrm{d}\omega}$ denotes the slope of the phase of the transfer function with respect to frequency. Figure 2-9 shows the series and parallel configuration of the oscillator.

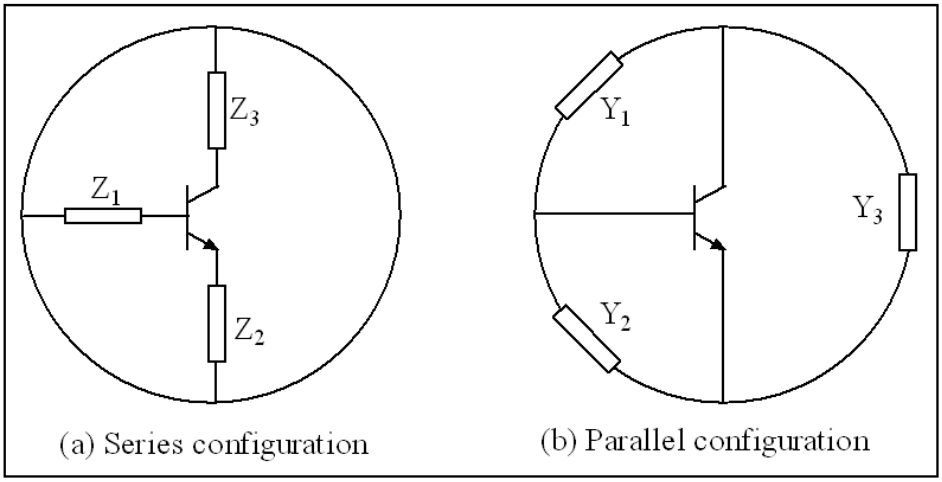


Figure 2-9 (a) Series and (b) Parallel configuration of the oscillator

Figure 2-10 shows the series feedback grounded base topology for the analysis of wideband VCOs. The negative resistance is created by an inductor in the base of the transistor instead of the capacitive feedback network used in the classical Colpitts oscillator, which is an example of parallel feedback topology. The series feedback grounded base topology is best suited for wide tuning range applications because the loaded Q of the resonator is approximately the same over the band and not affected much by the large-signal nonlinear negative resistance.

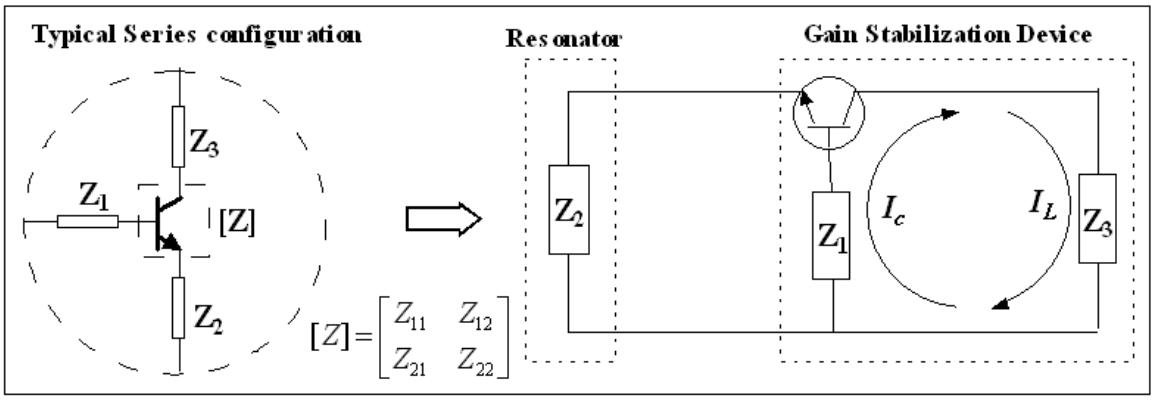


Figure 2-10 Series feedback grounded base topology

Figure 2-11 shows the general topology of the series feedback oscillator. The steady-state oscillation condition for the series feedback configuration shown in Figure 2-11 is [2]

$$Z_{osc}(I_L,\omega) + Z_L(\omega) = 0 \tag{2.34}$$

Where I_L is the load current amplitude and ω is the resonance frequency. Z_{osc} is the current and frequency dependent output impedance and Z_L is only function of frequency.

$$Z_{osc}(I_L,\omega) = R_{osc}(I_L,\omega) + jX_{osc}(I_L,\omega) \tag{2.35}$$

$R_{osc}(I_L,\omega)$ is the negative resistance generated by the device.

$$Z_L(\omega) = R_L(\omega) + jX_L(\omega) \tag{2.36}$$

$$Z_{osc} = [Z_{22} + Z_2] - \frac{[Z_{12} + Z_2][Z_{21} + Z_2]}{[Z_{11} + Z_1 + Z_2]} \tag{2.37}$$

$$[Z]_{Transistor} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (j\omega C_{b'e})^{-1} & 0 \\ g_m(\omega^2 C_{b'e} C_{ce})^{-1} & (j\omega C_{ce})^{-1} \end{bmatrix} \tag{2.38}$$

Where Z_{11}, Z_{22}, Z_{12} and Z_{21} are [Z] parameters of the transistor.
The [Z] parameters of the transistor can be calculated in terms of the [Y] parameter as [2]

$$Z_{11} = \frac{Y_{22}}{Y_{11}Y_{22} - Y_{12}Y_{21}}; \quad Z_{12} = \frac{-Y_{12}}{Y_{11}Y_{22} - Y_{12}Y_{21}};$$
$$Z_{21} = \frac{-Y_{21}}{Y_{11}Y_{22} - Y_{12}Y_{21}}; \quad Z_{22} = \frac{Y_{11}}{Y_{11}Y_{22} - Y_{12}Y_{21}} \tag{2.39}$$

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{2.40}$$

$$[Y] = \begin{bmatrix} (g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e}) & -(g_{b'c} + j\omega C_{b'c}) \\ g_m - (g_{b'c} + j\omega C_{b'c}) & (g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce}) \end{bmatrix} \tag{2.41}$$

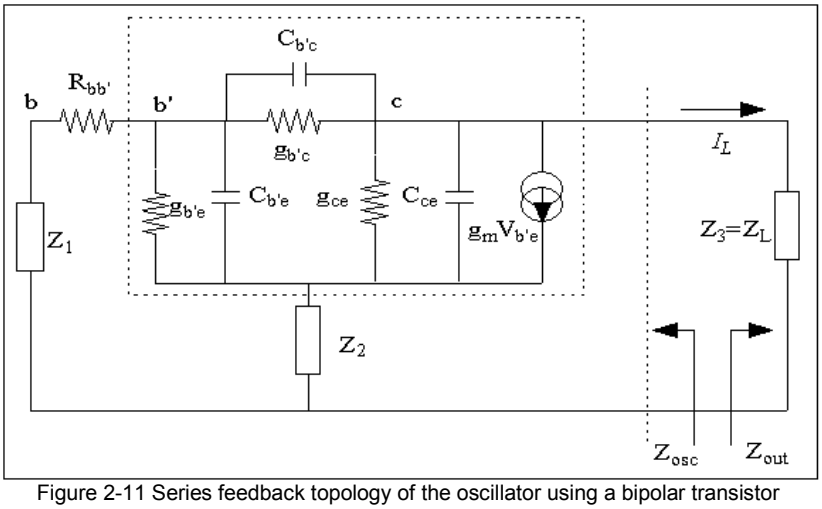


Figure 2-11 Series feedback topology of the oscillator using a bipolar transistor

From (2.39) Z_{11}, Z_{22}, Z_{12} and Z_{21} can be described by

$$[Z_{11}] = \frac{[(g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce})]}{[(g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e})][(g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce})] + [(g_{b'c} + j\omega C_{b'c})][g_m - (g_{b'c} + j\omega C_{b'c})]} \tag{2.42}$$

$$[Z_{12}] = \frac{[(g_{b'c} + j\omega C_{b'c})]}{[(g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e})][(g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce})] + [(g_{b'c} + j\omega C_{b'c})][g_m - (g_{b'c} + j\omega C_{b'c})]} \tag{2.43}$$

$$[Z_{21}] = \frac{-[g_m - (g_{b'c} + j\omega C_{b'c})]}{[(g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e})][(g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce})] + [(g_{b'c} + j\omega C_{b'c})][g_m - (g_{b'c} + j\omega C_{b'c})]} \tag{2.44}$$

$$[Z_{22}] = \frac{[(g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e})]}{[(g_{b'c} + g_{b'e}) + j\omega(C_{b'c} + C_{b'e})][(g_{b'c} + g_{ce}) + j\omega(C_{b'c} + C_{ce})] + [(g_{b'c} + j\omega C_{b'c})][g_m - (g_{b'c} + j\omega C_{b'c})]} \tag{2.45}$$

2.3.1 Grounded Base Parallel Lossless Passive LC Resonator Oscillator

Figure 2-12 shows the general topology of the series feedback lumped LC Resonator oscillator.

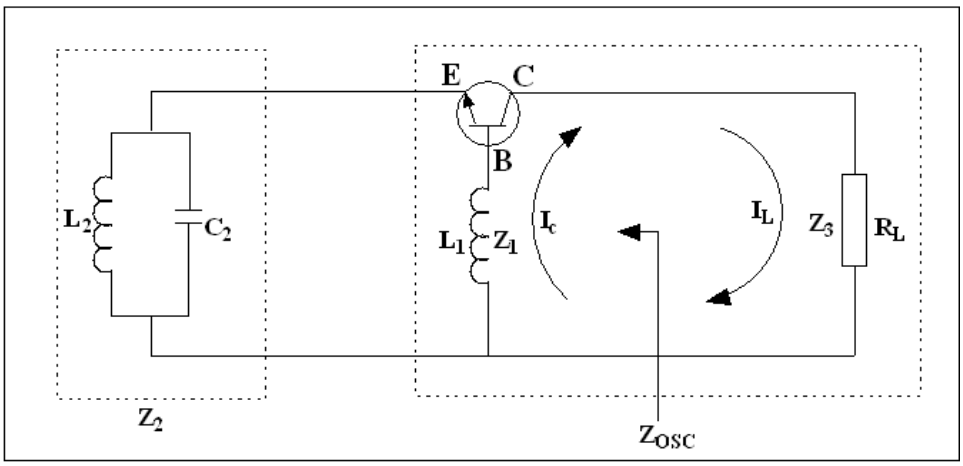


Figure 2-12 A typical series feedback grounded base topology

Assuming $g_{b'c}, g_{b'e}, g_{ce}$ and $C_{b'c}$ are having very little effect, then the [Z] parameters of the transistor as shown in Figure (2-11) can be described as in Equation (2.38) as

$$[Z] = \begin{bmatrix} \frac{1}{j\omega C_{b'e}} & 0 \\ \frac{g_m}{\omega^2 C_{b'e} C_{ce}} & \frac{1}{j\omega C_{ce}} \end{bmatrix} \tag{2.46}$$

where

$$Z_{11} = \frac{1}{j\omega C_{b'e}}, \quad Z_{12} = 0, \quad Z_{21} = \frac{g_m}{\omega^2 C_{b'e} C_{ce}}, \quad Z_{22} = \frac{1}{j\omega C_{ce}} \tag{2.47}$$

From (2.37),

$$Z_{osc} = (Z_{22} + Z_2) - \left[\frac{(Z_{12} + Z_2)(Z_{21} + Z_2)}{(Z_{11} + Z_2 + Z_1)} \right] \tag{2.48}$$

$$Z_{osc} = \left(\frac{1}{j\omega C_{ce}} + \frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \right) - \left[\frac{\left(\frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \right) \left(\frac{g_m}{\omega^2 C_{b'e} C_{ce}} + \frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \right)}{\left(\frac{1}{j\omega C_{b'e}} + \frac{j\omega L_2}{1 - \omega^2 L_2 C_2} + j\omega L_1 \right)} \right] \tag{2.49}$$

Where

$$Z_1 = j\omega L_1, \qquad Z_2 = \left[\frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \right] \tag{2.50}$$

From (2.49), expression of Z_{osc} can be simplified as

$$Z_{osc} = \left(\frac{1-\omega^2 L_2 C_2 - \omega^2 L_2 C_{ce}}{j\omega C_{ce}(1-\omega^2 L_2 C_2)} \right) - \left[\frac{\left(\frac{j\omega L_2}{1-\omega^2 L_2 C_2} \right)\left(\frac{g_m}{\omega^2 C_{b'e} C_{ce}} + \frac{j\omega L_2}{1-\omega^2 L_2 C_2} \right)}{\left(\frac{(1-\omega^2 L_2 C_2) - \omega^2 L_1 C_{b'e}(1-\omega^2 L_2 C_2) - \omega^2 L_2 C_{b'e}}{j\omega C_{b'e}(1-\omega^2 L_2 C_2)} \right)} \right] \tag{2.51}$$

$$Z_{osc} = -j\left[\frac{1-\omega^2 L_2(C_2 + C_{ce})}{\omega C_{ce}(1-\omega^2 L_2 C_2)} - \frac{\omega^3 L_2^2 C_{b'e}}{(1-\omega^2 L_2 C_2)^2(1-\omega^2 L_1 C_{b'e}) - \omega^2 L_2 C_{b'e}(1-\omega^2 L_2 C_2)} \right]_{Imag}$$
$$+ \frac{1}{C_{ce}} \left[\frac{g_m L_2}{(1-\omega^2 L_2 C_2) - \omega^2 L_1 C_{b'e}(1-\omega^2 L_2 C_2) - \omega^2 L_2 C_{b'e})} \right]_{Real} \tag{2.52}$$

$$Z_{osc} = [R_{osc}]_{Real} + j[X_{osc}]_{Imag} \tag{2.53}$$

Where

$$R_{osc} = \frac{1}{C_{ce}} \left[\frac{g_m L_2}{(1-\omega^2 L_2 C_2)(1-\omega^2 L_1 C_{b'e}) - \omega^2 L_2 C_{b'e})} \right] = \frac{g_m}{\omega C_{ce} \left[\left(\frac{1}{\omega L_2} - \omega C_2 \right)(1-\omega^2 L_1 C_{b'e}) - \omega C_{b'e} \right]} \tag{2.54}$$

$$R_{osc} = -\left[\frac{g_m}{\omega^2 C_2 C_{ce} \left(\left(1-\omega^2 L_1 C_{b'e}\right) + \frac{C_{b'e}}{C_2} \right)} \right]_{L_2 \to \infty, C_2 > C_{b'e}} = -\left[\frac{g_m}{\omega^2 C_2 C_{ce}(1-\omega^2 L_1 C_{b'e})} \right] \tag{2.55}$$

$$R_{osc} = R_{NR} = -\left[\frac{g_m}{\omega^2 C_2 C_{ce}(1-\omega^2 L_1 C_{b'e})} \right] = -\left[\frac{g_m}{\omega^2 C_2 C_{ce}} \right]_{\omega^2 L_1 C_{b'e} << 1} \tag{2.56}$$

From (2.52)

$$X_{osc} = -\left[\frac{1-\omega^2 L_2(C_2 + C_{ce})}{\omega C_{ce}(1-\omega^2 L_2 C_2)} - \frac{\omega^3 L_2^2 C_{b'e}}{(1-\omega^2 L_2 C_2)^2(1-\omega^2 L_1 C_{b'e}) - \omega^2 L_2 C_{b'e}(1-\omega^2 L_2 C_2)} \right] \tag{2.57}$$

$$X_{osc} = -\left[\frac{\omega^2 C_{b'e} C_{ce} - \left(\frac{1}{\omega L_2} - \omega(C_2 + C_{ce}) \right)\left[\left(\frac{1}{\omega L_2} - \omega C_2 \right)\left(1-\omega^2 L_1 C_{b'e}\right) - \omega C_{b'e} \right]}{\omega C_{ce} \left(\frac{1}{\omega L_2} - \omega C_2 \right)\left[\left(\frac{1}{\omega L_2} - \omega C_2 \right)\left(1-\omega^2 L_1 C_{b'e}\right) - \omega C_{b'e} \right]} \right] \tag{2.58}$$

$$X_{osc} = -\left[\frac{\omega C_{b'e} C_{ce} + (C_2 + C_{ce})[\omega C_2(1-\omega^2 L_1 C_{b'e}) + \omega C_{b'e}]}{[\omega^2 C_{ce} C_2^2(1-\omega^2 L_1 C_{b'e}) + \omega^2 C_{ce} C_2 C_{b'e}]} \right]_{L_2 \to \infty} \tag{2.59}$$

$$X_{osc} = -\left[\frac{C_2 + C_{ce}}{\omega C_{ce} C_2} + \frac{1}{\omega\left(\frac{C_2^2}{C_{b'e}}\right) + \omega C_2 - L_1 C_2^2 \omega^3}\right] = -\frac{1}{\omega C_2}\left[\frac{C_2 + C_{ce}}{C_{ce}} + \frac{C_{b'e}}{C_2 + C_{b'e} - \omega^2 L_1 C_2 C_{b'e}}\right] \tag{2.60}$$

For sustained oscillation, $X_{osc} = 0$,

$$X_{osc} = 0 \Rightarrow \frac{C_2 + C_{ce}}{C_{ce}} = \frac{C_{b'e}}{C_2 + C_{b'e} - \omega^2 L_1 C_2 C_{b'e}} \Rightarrow \omega^2 L_1 C_2 C_{b'e} = \left[C_2 + C_{b'e} - \frac{C_{b'e} C_{ce}}{C_2 + C_{ce}}\right] \tag{2.61}$$

$$\omega^2 = \frac{(C_2 + C_{b'e})(C_2 + C_{ce}) - C_{b'e} C_{ce}}{L_1 C_2 C_{b'e}(C_2 + C_{ce})} \Rightarrow f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L_1}\left[\frac{(C_{b'e} + C_2 + C_{ce})}{C_{b'e}(C_{ce} + C_2)}\right]} \tag{2.62}$$

2.3.2 Phase Noise

The total noise voltage power within 1Hz bandwidth can be described as [2, pp.176],

$$\left|\overline{e_n^2(\omega)}\right|_{\omega=\omega_0} = \overline{[e_R^2(\omega_0)]_{+R}} + \overline{[e_{NR}^2(\omega_0)]_{-R}} \tag{2.63}$$

The first term in the expression (2.63) is related to the thermal noise due to the equivalent series loss resistance (+R) associated with the resonator tank and the load resistor (R_L), and the second term is related to the negative resistance (-R) generated by the active device (Bipolar) to compensate the losses of the resonator tank.

The noise voltage associated with the positive loss resistance (+R) is given by

$$\left|\overline{e_n^2(\omega)}\right|_{\omega=\omega_0} = 4kTRB \Rightarrow \left|\overline{e_n^2(\omega)}\right|_{\omega=\omega_0} = [4kTR]_{B=1Hz} \tag{2.64}$$

From (2.57), the expression of negative resistance can be given by

$$R_{NR} \cong -\left[\frac{g_m}{\omega^2 C_2 C_{ce}(1 - \omega^2 L_1 C_{b'e})}\right] \tag{2.65}$$

The noise voltage power within 1Hz bandwidth associated with the negative loss resistance (R_{NR}) generated by the active circuit can be described by

$$\overline{[e_{NR}^2(\omega_0)]_{-R}} \approx \left[\frac{4qI_c g_m^2}{\omega_0^4 \beta^2 C_{ce}^2 (C_2 + C_{b'e} - L_1 C_2 C_{be} \omega_0^2)^2 + \left|g_m^2(t)\right| \omega_0^2 (C_2 + C_{b'e} - L_1 C_2 C_{b'e} \omega_0^2)^2}\right] \tag{2.66}$$

If we now change from the small-signal transconductance g_m, to a large-signal time-varying transconductance $g_m(t)$ then Equation (2.65) can be expressed as

$$R_n(t) = -\left[\frac{g_m(t)}{\omega^2 C_{ce} C_2 (1 - L_1 C_{b'e} \omega^2)}\right] \tag{2.67}$$

where $g_m(t)$ can be expressed as a Fourier series

$$g_m(t) = \sum_{n=-\infty}^{n=\infty} g_m^{(n)} \exp(jn\omega t) \tag{2.68}$$

where n truncates as the number of the harmonics considered.

After some lengthy calculations and approximations, adding shot noise, flicker noise and the loss resistor, the equivalent expression of the phase noise can be given from Equation (2.63)-(2.68) as [2, pp., 320]

$$\pounds(\omega) = \left[4kTR + \frac{\left|g_m^2(t)\right|(4qI_c) + \left|g_m^2(t)\right|\left(\frac{K_f I_b^{AF}}{\omega}\right)}{\omega_0^4 \beta^2 C_{ce}^2 (C_2 + C_{b'e} - L_1 C_2 C_{be} \omega_0^2)^2 + \left|g_m^2(t)\right| \omega_0^2 (C_2 + C_{b'e} - L_1 C_2 C_{b'e} \omega_0^2)^2}\right] \times$$

$$\frac{\omega_0^2}{4\omega^2 V_{ce}^2}\left[\frac{Q_0^2}{Q_L^2} + \left(1 - \frac{1}{\omega_0^2 L_1}\left(\frac{[(C_2 + C_{b'e} - L_1 C_2 C_{b'e} \omega_0^2) + C_{ce}]}{C_{ce}[(C_2 + C_{b'e} - L_1 C_2 C_{b'e} \omega_0^2)]}\right)\right)^2\right] \tag{2.69}$$

The flicker noise contribution in Equation (2.69) is introduced by adding term $\frac{K_f I_b^{AF}}{\omega}$ in the RF collector current I_c. K_f is the flicker noise coefficient and AF is the flicker noise exponent. This is valid only for the bipolar transistor. For an FET, the equivalent current transformations have to be used.

2.4 Grounded Base Lossy Passive LCR Resonator Oscillator

Figure 2-13 shows the general topology of the series feedback lumped LCR resonator oscillator.

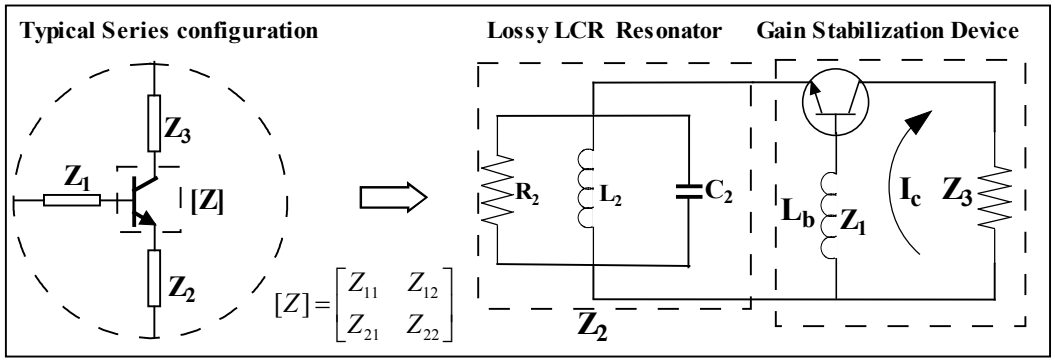


Figure 2-13 Series feedback grounded base LCR resonator oscillator topology

Assuming $g_{b'c}, g_{b'e}, g_{ce}$ and $C_{b'c}$ have very little effect, then the [Z] parameters of the transistor shown in Figure 2-13, described by the Equation (2.38) are

$$[Z]_{\text{Transistor}} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (j\omega C_{b'e})^{-1} & 0 \\ g_m(\omega^2 C_{b'e} C_{ce})^{-1} & (j\omega C_{ce})^{-1} \end{bmatrix} \tag{2.70}$$

Where Z_{11}, Z_{22}, Z_{12} and Z_{21} are the [Z] parameters of the transistor.
From Equation (2.37),

$$Z_{\text{osc}} = [Z_{22} + Z_2] - \frac{[Z_{12} + Z_2][Z_{21} + Z_2]}{[Z_{11} + Z_1 + Z_2]} \tag{2.71}$$

$$Z_{\text{osc}} = \left(\frac{1}{j\omega C_{ce}} + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 + j\omega L_2} \right) - \left[\frac{\left(\frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 + j\omega L_2} \right) \left(\frac{gm}{\omega^2 C_{b'e} C_{ce}} + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 + j\omega L_2} \right)}{\left(\frac{1}{j\omega C_{b'e}} + j\omega L_1 + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 + j\omega L_2} \right)} \right] \tag{2.72}$$

Where

$$Z_1 = j\omega L_1, \quad Z_2 = \left(j\omega L_2)^{-1} + \left(\frac{1}{j\omega C_2} \right)^{-1} + (R_2)^{-1} \right)^{-1} = \left(\frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 + j\omega L_2} \right) \tag{2.73}$$

From Equation (2.53), expression of Z_{osc} can be rewritten as

$$Z_{\text{osc}} = R_{\text{osc}} + jX_{\text{osc}} \tag{2.74}$$

$$R_{\text{osc}} = \left[\frac{\frac{1}{R_2}}{\left(\left(\frac{1}{\omega L_2} - \omega C_2 \right)^2 + \left(\frac{1}{R_2} \right)^2 \right)} \right] - \left[\frac{-gm \left((1 - \omega^2 C_{b'e} L_1) \left(\frac{1}{\omega L_2} - \omega C_2 \right) - \omega C_{b'e} \right) \left(\left(\frac{1}{\omega L_2} - \omega C_2 \right)^2 + \left(\frac{1}{R_2} \right)^2 \right) - \frac{\omega^2 C_{b'e} C_{ce}}{R_2} \left(2(1 - \omega^2 C_{b'e} L_1) \left(\frac{1}{\omega L_2} - \omega C_2 \right) - \omega C_{b'e} \right)}{\omega C_{ce} \left(\left(\frac{1}{\omega L_2} - \omega C_2 \right)^2 + \left(\frac{1}{R_2} \right)^2 \right) \left(\left((1 - \omega^2 C_{b'e} L_1) \left(\frac{1}{\omega L_2} - \omega C_2 \right) - \omega C_{b'e} \right)^2 + \left(\frac{1 - \omega^2 C_{b'e} L_1}{R_2} \right)^2 \right)} \right] \tag{2.75}$$

From Equation (2.75),

$$[R_{\text{osc}}]_{R_2 \to \infty} = \left[\frac{g_m}{\omega C_{ce} \left(\left(\frac{1}{\omega L_2} - \omega C_2 \right) (1 - \omega^2 C_{b'e} L_1) - \omega C_{b'e} \right)} \right] \tag{2.76}$$

$$[R_{osc}]_{L_2\to\infty} = \frac{R_2^{-1}}{(\omega^2 C_2^2 + R_2^2)} - \frac{g_m\{\omega C_2(1-\omega^2 C_{b'e}L_1)+\omega C_{b'e}\}\{\omega^2 C_2^2+R_2^2\}+\omega^2 C_{b'e}C_{ce}R_2^{-1}\{2\omega C_2(1-\omega^2 C_{b'e}L_1)+\omega C_{b'e})+\omega C_{b'e}\}}{\omega C_{ce}\{\omega^2 C_2^2+R_2^2\}\{(\omega C_2(1-\omega^2 C_{b'e}L_1)+\omega C_{b'e})^2+(1-\omega^2 C_{b'e}L_1)^2 R_2^{-2}\}} \quad (2.77)$$

$$[R_{osc}]_{L_2\to\infty,R_2\to\infty} = -\left[\frac{g_m}{\omega^2 C_2 C_{ce}\left(\left(1-\omega^2 L_1 C_{b'e}\right)+\frac{C_{b'e}}{C_2}\right)}\right] \Rightarrow \quad (2.78)$$

$$[R_{osc}]_{L_2\to\infty,R_2\to\infty,C_2>C_{b'e}} = -\left[\frac{g_m}{\omega^2 C_2 C_{ce}(1-\omega^2 L_1 C_{b'e})}\right]$$

From Equation (2.71) and Equation (2.74),

$$X_{osc} = \left(\frac{\left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{\omega L_2}-\omega C_2\right)-\frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2 C_{b'e}L_1}{R_2}\right)^2\right]}{\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2 C_{b'e}L_1}{R_2}\right)^2\right]}\right) +$$

$$\left(\frac{\omega C_{b'e}\left(\frac{1}{\omega L_2}-\omega C_2\right)\left[(1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right]-\frac{(1-\omega^2 C_{b'e}L_1)}{\omega R_2 C_{ce}}gm\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2-\left(\frac{1}{R_2}\right)^2\right]-\frac{(1-\omega^2 C_{b'e}L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}}{\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e}L)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{(1-\omega^2 C_{b'e}L_1)}{R_2}\right)^2\right]}\right) \quad (2.79)$$

For sustained oscillation $X_{osc}=0$,

$$X_{osc} = \left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{\omega L_2}-\omega C_2\right)-\frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2 C_{b'e}L_1}{R_2}\right)^2\right]+$$

$$\omega C_{b'e}\left(\frac{1}{\omega L_2}-\omega C_2\right)\left[(1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right]-\frac{(1-\omega^2 C_{b'e}L_1)}{\omega R_2 C_{ce}}gm\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2-\left(\frac{1}{R_2}\right)^2\right]-\left[\frac{(1-\omega^2 C_{b'e}L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}\right]=0 \quad (2.80)$$

From Equation (2.78), oscillation frequency ω_{osc} can be given by

$$[\omega_{osc}]_{R_2\to\infty,\,L_2\to\infty} = \sqrt{\frac{(C_{ce}+C_2+C_{b'e})}{C_{b'e}L_1(C_{ce}+C_2)}} \quad (2.81)$$

2.5 Grounded Base Active LC Resonator (-R) Oscillator

Figure 2-14 shows the general topology of the series feedback active LC resonator (-R) oscillator.

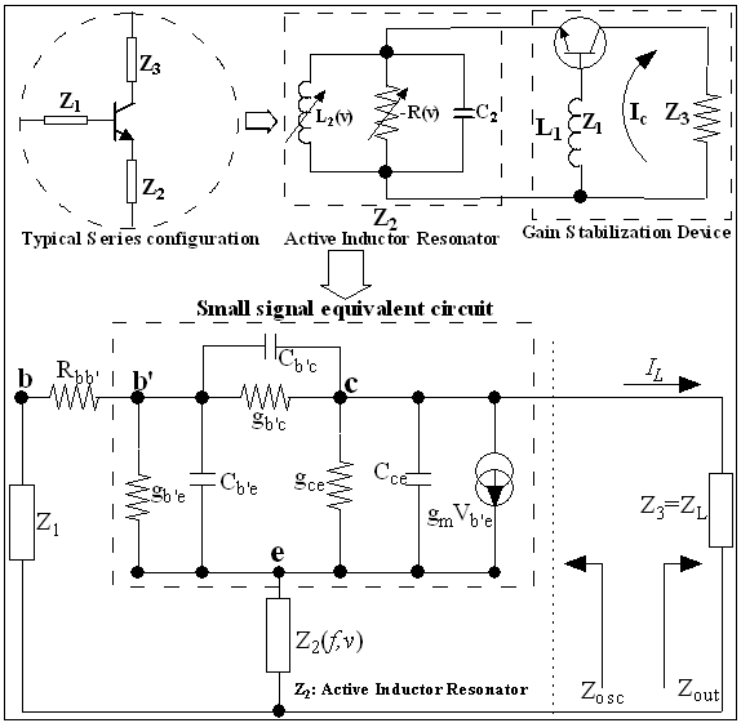


Figure 2-14 A typical series feedback grounded base active LC resonator oscillator topology

Assuming $g_{b'c}, g_{b'e}, g_{ce}$ and $C_{b'c}$ have very little effect, then the [Z] parameters of the transistor are described by Equation (2.38) as

$$[Z]_{\text{Transistor}} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (j\omega C_{b'e})^{-1} & 0 \\ g_m(\omega^2 C_{b'e} C_{ce})^{-1} & (j\omega C_{ce})^{-1} \end{bmatrix} \tag{2.82}$$

Where Z_{11}, Z_{22}, Z_{12} and Z_{21} are [Z] parameter of the transistor.

From Equation (2.37),

$$Z_{osc} = [Z_{22} + Z_2] - \frac{[Z_{12} + Z_2][Z_{21} + Z_2]}{[Z_{11} + Z_1 + Z_2]} \tag{2.83}$$

$$Z_{OSC} = \left(\frac{1}{j\omega C_{ce}} + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 - j\omega L_2} \right) - \left[\frac{\left(\frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 - j\omega L_2} \right) \left(\frac{gm}{\omega^2 C_{b'e} C_{ce}} + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 - j\omega L_2} \right)}{\left(\frac{1}{j\omega C_{b'e}} + \frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 - j\omega L_2} + j\omega L_1 \right)} \right] \tag{2.84}$$

Where

$$Z_1 = j\omega L_1, \quad Z_2 = \left[(j\omega L_2)^{-1} + \left(\frac{1}{j\omega C_2} \right)^{-1} - (R_2)^{-1} \right]^{-1} = \left[\frac{j\omega R_2 L_2}{R_2 - \omega^2 L_2 R_2 C_2 - j\omega L_2} \right] \tag{2.85}$$

The expression of Z_{osc} can be rewritten as

$$Z_{osc} = R_{osc} + jX_{osc} \tag{2.86}$$

$$R_{osc}=\left[\frac{\frac{1}{R_2}}{\left(\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right)}\right]-$$
$$\left[\frac{-gm\left((1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)\left(\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right)-\frac{\omega^2C_{b'e}C_{ce}}{R_2}\left(2(1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)}{\omega C_{ce}\left(\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right)\left(\left((1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2C_{b'e}L_1}{R_2}\right)^2\right)}\right] \quad (2.87)$$

From Equation (2.87),

$$[R_{osc}]_{R_2\to\infty}=\left[\frac{g_m}{\omega C_{ce}\left(\left(\frac{1}{\omega L_2}-\omega C_2\right)(1-\omega^2C_{b'e}L_1)-\omega C_{b'e}\right)}\right] \quad (2.88)$$

$$[R_{osc}]_{L_2\to\infty}=\frac{R_2^{-1}}{(\omega^2C_2^2+R_2^{-2})}-\frac{g_m\{\omega C_2(1-\omega^2C_{b'e}L_1)+\omega C_{b'e}\}\{\omega^2C_2^2+R_2^{-2}\}+\omega^2C_{b'e}C_{ce}R_2^{-1}\{2\omega C_2(1-\omega^2C_{b'e}L_1)+\omega C_{b'e}\}}{\omega C_{ce}\{\omega^2C_2^2+R_2^{-2}\}\{(\omega C_2(1-\omega^2C_{b'e}L_1)+\omega C_{b'e})^2+(1-\omega^2C_{b'e}L_1)^2R_2^{-2}\}} \quad (2.89)$$

$$[R_{osc}]_{L_2\to\infty,R_2\to\infty}=-\left[\frac{g_m}{\omega^2C_2C_{ce}\left(\left(1-\omega^2L_1C_{b'e}\right)+\frac{C_{b'e}}{C_2}\right)}\right]\Rightarrow[R_{osc}]_{L_2\to\infty,R_2\to\infty,C_2>C_{b'e}}=-\left[\frac{g_m}{\omega^2C_2C_{ce}(1-\omega^2L_1C_{b'e})}\right] \quad (2.90)$$

From Equation (2.84) and Equation (2.86),

$$X_{osc}=\left(\frac{\left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{\omega L_2}-\omega C_2\right)-\frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2C_{b'e}L_1}{R_2}\right)^2\right]}{\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right]\left[\left(\left(1-\omega^2C_{b'e}L_1\right)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2C_{b'e}L_1}{R_2}\right)^2\right]}\right)+ \quad (2.91)$$

$$\left(\frac{\omega C_{b'e}\left(\frac{1}{\omega L_2}-\omega C_2\right)\left[(1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right]+\frac{(1-\omega^2C_{b'e}L_1)}{\omega R_2C_{ce}}g_m\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2-\left(\frac{1}{R_2}\right)^2\right]-\frac{(1-\omega^2C_{b'e}L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}}{\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2C_{b'e}L)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{(1-\omega^2C_{b'e}L_1)}{R_2}\right)^2\right]}\right)$$

For sustained oscillation $X_{osc}=0$,

$$X_{osc}=\left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{\omega L_2}-\omega C_2\right)-\frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2C_{b'e}L_1}{R_2}\right)^2\right]+$$
$$\omega C_{b'e}\left(\frac{1}{\omega L_2}-\omega C_2\right)\left[(1-\omega^2C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right]+\frac{(1-\omega^2C_{b'e}L_1)}{\omega R_2C_{ce}}g_m\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2-\left(\frac{1}{R_2}\right)^2\right]-\left[\frac{(1-\omega^2C_{b'e}L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}\right]=0 \quad (2.92)$$

From Equation (2.92),

$$
\begin{aligned}
&-\left((\omega^{-1}L_2^{-1}-\omega C_2)^2+R_2^{-2}\right)\left(\left((\omega^{-1}L_2^{-1}-\omega C_2)(1-\omega^2L_1C_{b'e})-\omega C_{b'e}\right)^2+(1-\omega^2L_1C_{b'e})^2R_2^{-2}\right)\\
&+\omega C_{ce}(\omega^{-1}L_2^{-1}-\omega C_2)\left((\omega^{-1}L_2^{-1}-\omega C_2)(1-\omega^2L_1C_{b'e})-\omega C_{b'e}\right)^2+\omega^2C_{b'e}C_{ce}(\omega^{-1}L_2^{-1}-\omega C_2)\left((\omega^{-1}L_2^{-1}-\omega C_2)(1-\omega^2L_1C_{b'e})-\omega C_{b'e}\right)\\
&+\omega C_{ce}(\omega^{-1}L_2^{-1}-\omega C_2)(1-\omega^2L_1C_{b'e})^2R_2^{-2}-(1-\omega^2L_1C_{b'e})R_2^{-2}\omega^2C_{b'e}C_{ce}+(1-\omega^2L_1C_{b'e})R_2^{-1}g_m\left((\omega^{-1}L_2^{-1}-\omega C_2)^2+R_2^{-2}\right)=0
\end{aligned}
\tag{2.93}
$$

Rearranging Equation (2.93),

$$
(1-\omega^2L_1C_{b'e})^2\left(\omega C_{ce}(\omega^{-1}L_2^{-1}-\omega C_2)-(\omega^{-1}L_2^{-1}-\omega C_2)^2-R_2^{-2}\right)+(1-\omega^2L_1C_{b'e})\left(2\omega C_{b'e}(\omega^{-1}L_2^{-1}-\omega C_2)-\omega C_{b'e}\omega C_{ce}+R_2^{-1}g_m\right)-(\omega C_{b'e})^2=0
\tag{2.94}
$$

$$
\begin{aligned}
&1-\omega^2L_1C_{b'e}=\\
&\left(\omega^4C_{ce}^2C_{b'e}^2+g_m^2R_2^{-2}-2\omega^2g_mR_2^{-1}C_{b'e}C_{ce}+4\omega^2g_mR_2^{-1}C_{b'e}(\omega^{-2}L_2^{-1}-C_2)+8\omega^4C_{b'e}^2(\omega^{-2}L_2^{-1}-C_2)^2-8\omega^4C_{ce}C_{b'e}^2(\omega^{-2}L_2^{-1}-C_2)+8\omega^2R_2^{-2}C_{b'e}^2\right)^{1/2}
\end{aligned}
\tag{2.95}
$$

$$
\left(1-\omega^2L_1C_{b'e}\right)=
\tag{2.96}
$$

$$
\left(\omega^4C_{ce}^2C_{b'e}^2+\left(\frac{g_m}{R_2}\right)^2-2\omega^2C_{b'e}C_{ce}\left(\frac{g_m}{R_2}\right)+4\omega^2C_{b'e}\left(\frac{g_m}{R_2}\right)\left(\frac{1}{\omega^2L_2}-C_2\right)+8\omega^4C_{b'e}^2\left(\frac{1}{\omega^2L_2}-C_2\right)^2-8\omega^4C_{ce}C_{b'e}^2\left(\frac{1}{\omega^2L_2}-C_2\right)+8\omega^2C_{b'e}^2\left(\frac{1}{R_2}\right)^2\right)^{1/2}
$$

Equation (2.96) yields multimode oscillation conditions. For $\omega=[L_2C_2]^{\frac{1}{2}}$ and $\omega=[L_1C_{b'e}]^{\frac{1}{2}}$ Equation (2.96) reduces to

$$
\omega^2C_{ce}^2C_{b'e}^2+\left(\frac{g_m}{R_2}\right)^2-2C_{b'e}C_{ce}\left(\frac{g_m}{R_2}\right)+8C_{b'e}^2\left(\frac{1}{R_2}\right)^2=0
\tag{2.97}
$$

$$
\omega=\frac{1}{C_{b'e}C_{ce}}\sqrt{\left[2C_{b'e}C_{ce}\left(\frac{g_m}{R_2}\right)-\left(\frac{g_m}{R_2}\right)^2-8C_{b'e}^2\left(\frac{1}{R_2}\right)^2\right]}
\tag{2.98}
$$

From Equation (2.96), the possible modes of oscillations are:

$$
\omega_1=\left[\frac{1}{L_2C_2}\right]^{1/2},\quad \omega_2=\left[\frac{1}{L_1C_{b'e}}\right]^{1/2},\quad \omega_3=\frac{1}{C_{b'e}C_{ce}}\left[2C_{b'e}C_{ce}\left(\frac{g_m}{R_2}\right)-\left(\frac{g_m}{R_2}\right)^2-8C_{b'e}^2\left(\frac{1}{R_2}\right)^2\right]^{1/2}
\tag{2.99}
$$

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3. Inductive Dynamics

Inductors are found in a broad range of applications. Some of the applications include tunable signal sources, high-speed analog signal processing including impedance matching and gain-boosting in wireless transceivers, bandwidth improvement in broadband data communications over wire and optical channels, modulators, RF bandpass filters, RF phase shifters, RF power dividers, and coupling of high-frequency signals. The usefulness of these inductors is limited due to its inherited properties. Some of these limiting factors are listed here.

- A low quality factor,
- A low self-resonant frequency,
- A small and non-tunable inductance,
- Moreover, the need for a prohibitively large silicon area in integrated circuits.

Generally, the inductors are off-chip discrete components. Designs with these passive components severely limits bandwidth, reduces reliability, and increases the cost of system. Since the early 1990s, significant intensive research on the synthesis of inductors using active devices has been made to fabricate inductors on a silicon substrate. This aims at minimizing the silicon area, thus the fabrication cost resulting in improved performance. It will also enable fabrication of the entire wireless transceiver on a single substrate integrated monolithically.

The most comparative advantage of using active inductors synthesized with active devices over their spiral counterparts are as follows:

- Virtually no chip area requirement,
- Large and tunable inductance with large inductance tuning range,
- Large and tunable quality factor,
- High self-resonant frequencies,
- Full compatibility with digital oriented CMOS, BiCMOS and SiGe technologies.

Active inductors are found in many applications including high-speed analog signal processing and data communications, where spiral inductors were employed. Some of the disadvantages of using the active inductor can be:

- Small dynamic range,
- Poor noise performance,
- Higher power consumption,
- High sensitivity to supply voltage fluctuation and process variation.

This research work provides a comprehensive treatment of the principle topologies, and characteristics of active inductors. It also highlights in-depth examination of their emerging applications in high-speed analog signal processing and data communications.

3.1 Inductive Characteristics in High-Speed Applications

Inductive characteristics are critically needed in high-speed applications to improve the performance of systems. Inductors are employed for improving bandwidth and boosting the gain of the system. They can be used to perform specific tasks, such as impedance matching and frequency selection [1]. Some of the applications are discussed in the contents below.

3.1.1 LC Oscillators

One of the key applications of inductors in wireless communication is the construction of LC oscillators. As compared to ring oscillators, LC oscillators with spiral inductors or transformers have lower phase-noise. This forms the basic advantage of an LC oscillator over the ring oscillator. The LC oscillators are preferred in wireless communication systems where a stringent constraint on the phase noise of oscillators exists. Frequency tuning of LC oscillators with spiral inductors is typically performed by varying the capacitance of the LC tank. Variable capacitor circuits often realized using MOS varactors are used as the tuning element. The inductance tuning of spiral inductors or transformers in monolithic integrated circuits is difficult. Moreover, the variable capacitors offer a relatively small tuning range, hence a smaller frequency tuning range for the oscillators. This method can be adequate for narrow-band wireless applications. For applications such as clock and data recovery in broadband data communications over wire lines or optical channels, a larger frequency tuning range is required. Table 3.1 summarizes the state-of-the-art of LC oscillators with either spiral inductors or spiral transformers using CMOS technology.

Table 3.1 The state-of-the-art of LC oscillators using CMOS technology.

[Ref]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
CMOS Process	0.18µm	0.25µm	0.18µm	0.18µm	90nm	350nm	180nm	65nm
F_O (GHz)	2.4	2.4	2.42	2.4	5	0.9	4.5	21
L{Δf} (dBc/Hz)	-138	-105	-134	-123.8	-103	-101	-109	-110
Δf (HZ)	3M	600k	1M	1M	1M	600k	1M	10M
P_{Diss} (mW)	5.4	17.5	4.6	15.1	2.8	9.8	0.16	1.92
FOM (dBc/Hz)	188.7	164	195	179.6	199	182	195	206

3.1.2 Bandwidth Improvement

Bandwidth is a critical concern in broadband communications, such as optical front-ends and data communications over wire links. The bandwidth of a circuit is set by the time constant of the critical node, i.e. the node that has the largest time constant, of the circuit. Three approaches, namely *inductive peaking*, *current-mode signaling*, and *distributed amplification*, are widely used to improve the bandwidth of circuits.

- *Inductive peaking* – Inductive peaking utilizes the idea to place an inductor at the node where a large nodal capacitance exists. This will replace the first-order RC network of the node with a second-order RLC network. This is useful as the RLC network will have three different modes of operation, namely over damped, critically damped, and under damped. The bandwidth in these three cases differs. The largest bandwidth is obtained with under-damped RLC systems. Both shunt peaking [10, 11] and series peaking [12], have been used, as shown in Figure 3-1. It was demonstrated in [10, 11] that inductive shunt peaking can improve the bandwidth of a common-source amplifier by as much as 70%.

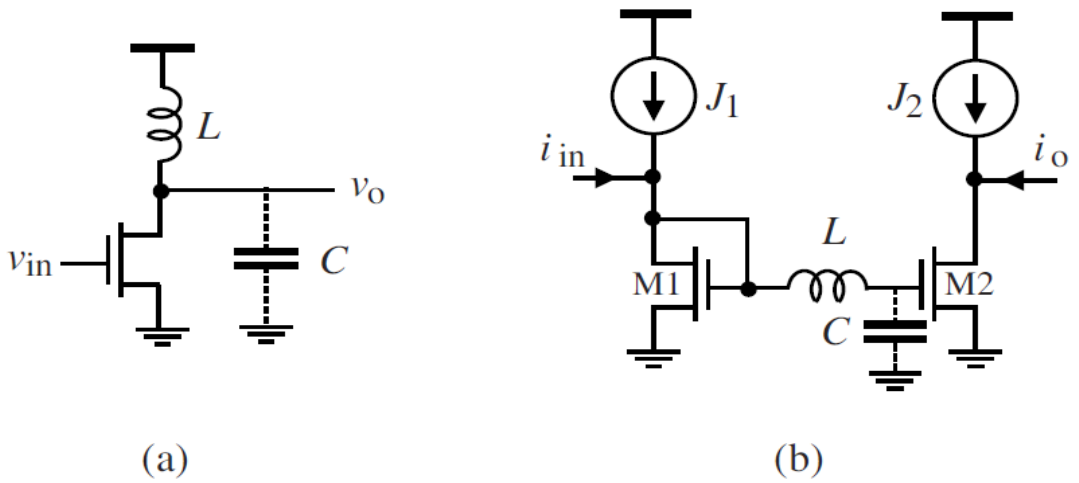


Figure 3-1 Inductive peaking used in two configurations to improve the bandwidth of a common source amplifier. (a) Shunt peaking - The peaking inductor *L* is in parallel with the dominant capacitor *C*. (b) Series peaking - The peaking inductor *L* is in series with the dominant capacitor *C*.

- *Current-mode signaling* – In the current-mode configuration the information carriers are the branch currents of the circuit. A key distinction between current-mode and voltage-mode circuits is the nodal impedance. For a current-mode circuit the nodal impedance is low whereas that of voltage mode circuit is high. This distinct characteristic forms the foundation on which current-mode circuits are designed. As the information processed by a current-mode circuit is represented by the branch currents, the swing of the nodal voltages in the circuit can be made small without sacrificing the fidelity of the signal. Current mode circuits offer an improved bandwidth due to the following reasons:
  - *i.* Low nodal impedances - the low nodal impedances of current-mode circuits lower the nodal time constants of the circuits.
  - *ii.* Low voltage swings - the small swing of the nodal voltages of current-mode circuits reduces the amount of the time required to charge and discharge the nodes of the circuits [13].

In the current mode configuration the speed of signaling is moderate mainly due to low nodal impedance. As each node is essentially a first-order RC network represented by the time constant $\tau_n = R_n C_n$, where R_n and C_n denote the resistance and capacitance of the node respectively, the net reduction in the nodal time constant depends mainly on them. The moderation in speed is the result of lower impedance level needing increased capacitance.

- *Distributed Amplification* - The bandwidth or speed of a circuit is set by the time constant of the critical node in the circuit. The most common method to minimize the effect of the large shunt capacitance of the critical node is to break the large shunt capacitor into several smaller shunt capacitors and separate them with inductors. Then we can replace the large shunt capacitor with a distributed LC network or a transmission line [14, 15]. Shown in Figure 3-2 is a common-source amplifier. A shunt peaking inductor employed at the drain of the transistor offsets the effect of the large output capacitance *C* coming from the large width of the transistor. Inductive shunt-peaking, though effective, may still not deliver the needed bandwidth. Notice that the typical layout of a transistor is in multi-finger fashion. This is equivalent to connecting *N* smaller transistors whose width is only $(1/N)^{th}$ that of the original transistor in parallel, as shown in the figure, where *N* is the number of the fingers of the transistor. Inductors can then be employed to separate these small transistors and form two transmission lines, one at the drain and the other at the source. Resistors $R1-4$ shown in Figure 3-2 are for the purpose of impedance matching.

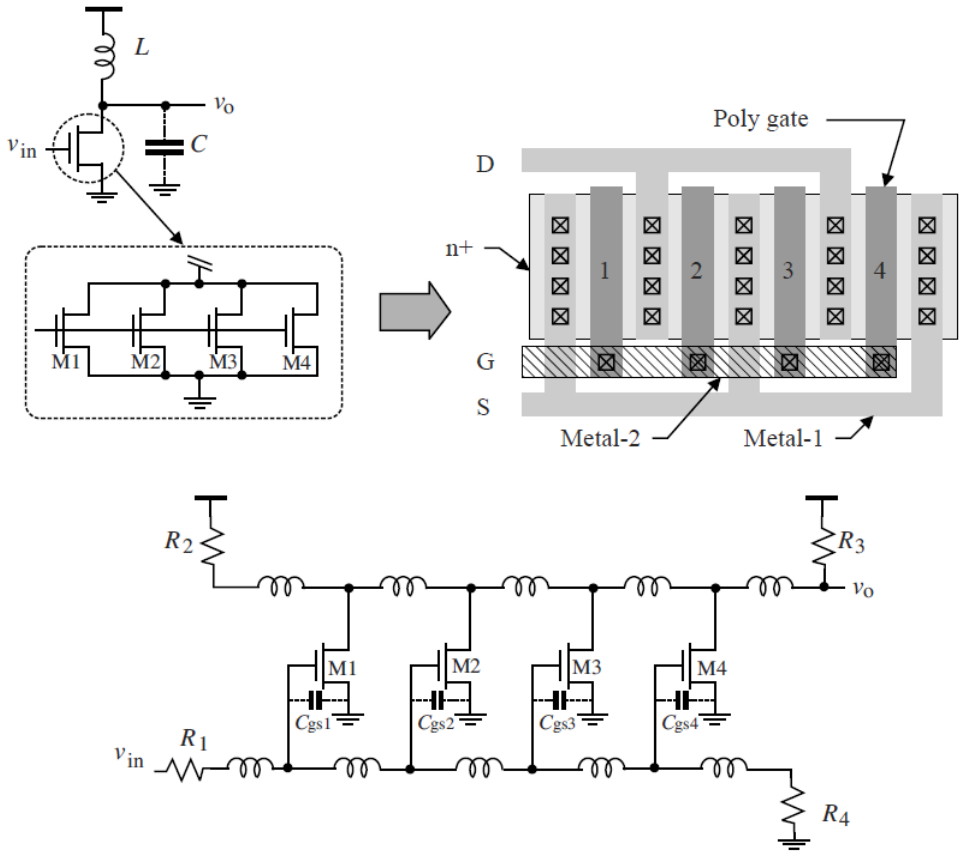


Figure 3-2 Distributed amplifiers.

3.1.3 Impedance Matching

Impedance matching is required between channels and high-speed circuits to minimize signal reflection at their interfaces. Resistors are used to provide a matching impedance in broadband communication systems as it provides impedance matching over a broader frequency spectrum. A shunt resistor termination at the far end of the channel being employed is shown in Figure 3-3. Active terminations, such as some of the recent applications in [13] using transistors as terminating devices, can be implemented to take advantage of tunability for the termination resistance. Frequency-dependent elements, such as capacitors and inductors, cannot be used for impedance matching in broadband communication systems. Their frequency-dependent characteristics itself inhibits the operation over a broad band of frequencies.

Most wireless communication systems operate in a narrow-band mode enabling the impedance matching operation only for small frequency range. Resistors can be used for these applications, but noiseless elements such as spiral inductors and capacitors are preferred. The high level of thermal noise in resistors disqualifies them from being used in wireless communications where a stringent constraint on the noise performance exists. The frequency-dependent noiseless elements can provide the desired impedance in a narrow frequency band and at the same time keep the noise at the minimum [16, 17]. Shown in Figure 3-4 is a widely used termination scheme for narrowband low-noise amplifiers. Neglecting C_{gd} and other parasitic capacitances, it is elementary to show that the input impedance of the LNA is given by

$$Z_{in} = \left[j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs1}} \right] + \frac{g_{m1} L_2}{C_{gs1}} \tag{3.1}$$

where C_{gs1} and g_{m1} are the gate-source capacitance and transconductance of $M1$, respectively. It is seen from Equation (3.1) that the first term on the right hand side of Equation (3.1) is reactive while the second term is resistive. The reactive term can be made zero by imposing

$$\omega(L_1 + L_2) - \frac{1}{\omega C_{gs1}} = 0 \tag{3.2}$$

The input impedance of the LNA in this case becomes purely resistive and is given by

$$Z_{in} = \frac{g_{m1} L_2}{C_{gs1}} \tag{3.3}$$

The need for two inductors $L1$ and $L2$ with $L1$ at the gate and $L2$ at the source is justified as in the following text. Once the dimension of $M1$ is chosen, g_{m1} and C_{gs1} are determined. The desired input impedance of the LNA in this case can be obtained by adjusting $L2$. Once $L2$ is chosen, the value of $L1$ can be tuned to ensure the total cancellation of the reactive part of the input impedance.

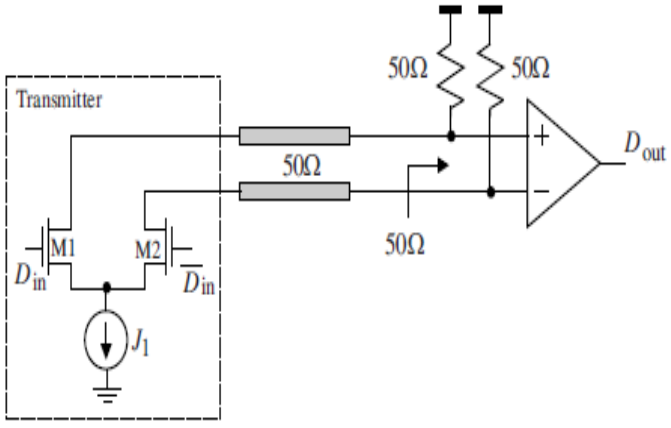


Figure 3-3 Impedance matching in high-speed current-mode serial links

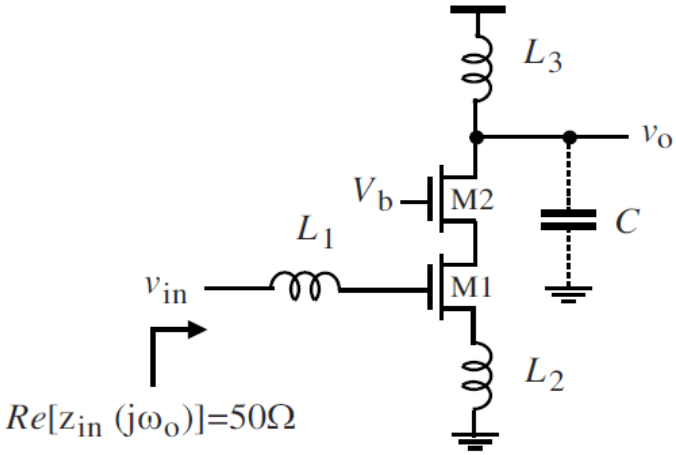


Figure 3-4 Impedance matching in narrow-band low-noise amplifiers

3.1.4 Phase Shifting

A phase shifter is a unidirectional serial network inserted in a signal path so that the phase of the signal at the output of the signal path can be adjusted in a controlled manner [18, 19]. A well-designed phase shifter has the following characteristics:

- A low insertion loss,
- A high return loss,
- A large phase shift range.

The common configuration of an RF phase shifter is shown in Figure 3-5. The floating inductors are imprinted using high-impedance metal lines and the phase shift tuning is achieved by the shunt varactors.

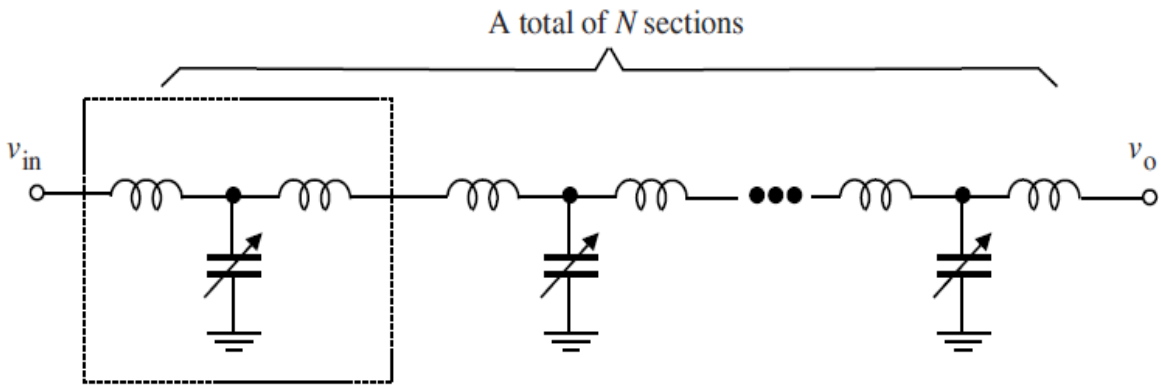


Figure 3-5 RF phase shifters with floating inductors and shunt varactors.

3.1.5 Frequency Selection

Bandpass filters for high frequencies are used extensively in narrow-band wireless communications for RF band selection. These filters are traditionally implemented using lumped inductors and capacitors. Sometimes the most widely used surface acoustic wave (SAW) resonators are used to build highly selective filters. SAW filters are not compatible with CMOS technology. Recent efforts to integrate RF bandpass filters on a silicon substrate are accelerated with the emergence of CMOS spiral inductors. A single-chip realization of RF transceivers with on-chip RF bandpass filters offers a number of critical advantages including reduced assembly cost, increased system reliability, and improved performance. To compensate for the high insertion loss of spiral inductors at high frequencies, active negative resistance has been used to boost the quality factor of the spiral inductors [20]-[26].

3.1.6 Gain Boosting

Traditional gain-boosting techniques such as cascode and regulated cascode lose their potency at high frequencies. The increased gate-source and gate-drain couplings via the gate-source and gate-drain capacitors of MOSFETs are mainly responsible for this. Other techniques include using a LC tank circuit to boost the voltage gain for a narrowband LNAs. The method involves utilizing the infinite impedance of ideal LC tanks at their self-resonant frequency. When a LC tank is used as the load of a common-source amplifier the large impedance of the LC tank at its self-resonant frequency $\omega_0 = 1/\sqrt{L_P C}$ will significantly boost the gain of the amplifier at, ω_0. The voltage gain of the common-source amplifier is approximated by $A_V \approx -g_m Z_L$, where g_m is the transconductance of the MOSFET and Z_L is the load impedance, as shown in Figure 3-6. The resonant frequency of the tank is set to be the same as the frequency of the input of the LNA. Note that the voltage gain of the amplifier at frequencies other than ω_0 is low.

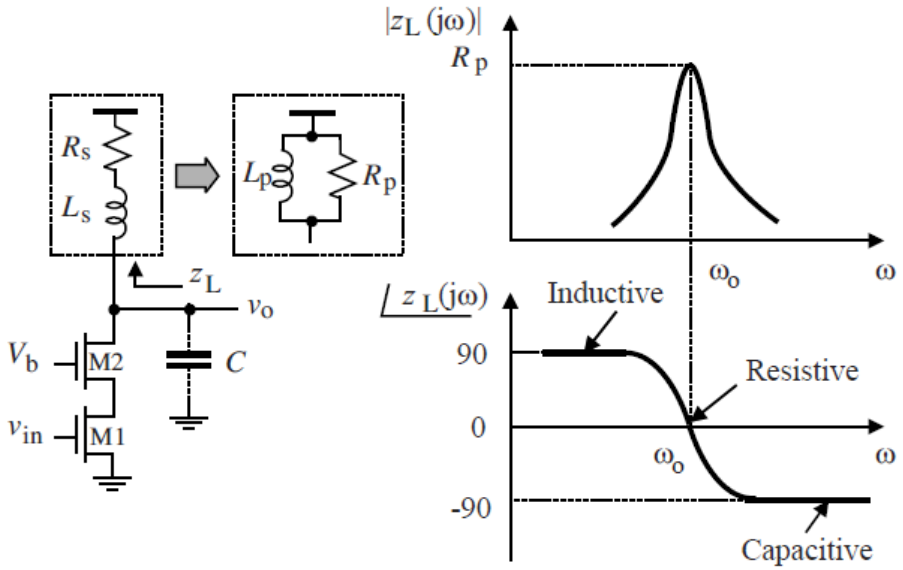


Figure 3-6 Gain boosting of low noise amplifiers using LC tank.

3.1.7 Improving Q factor

Quality factor of inductors: The performance of the inductor is limited by the losses through undesired currents in the substrate and in the series resistance of the inductor windings. It is commonly known that the quality factor increases when the losses decrease.

The general definition of quality factor is

$$Q = \frac{(Inductively)Stored\ energy\ per\ cycle}{(Resistively)Dissipated\ energy\ per\ cycle} \tag{3.4}$$

The most common and most widely used definition of quality factor Q [57]

$$Q = \frac{Im(Y11)}{Re(Y11)} \tag{3.5}$$

Q in terms of effective inductance L_{eff} and effective resistance R_{eff} is

$$Q = \frac{2\pi f L_{eff}(f)}{R_{eff}(f)} \tag{3.6}$$

where f is the frequency.

Figure 3-7 shows a typical quality factor plot. Due to its definition, this quality factor is zero at the self-resonance frequency of the inductor, which is a physically unreasonable result [57].

There are different definitions of quality factor based on the consideration that parameters of interest to designers are loss, bandwidths of resonant circuits and frequency stability factors of oscillators.

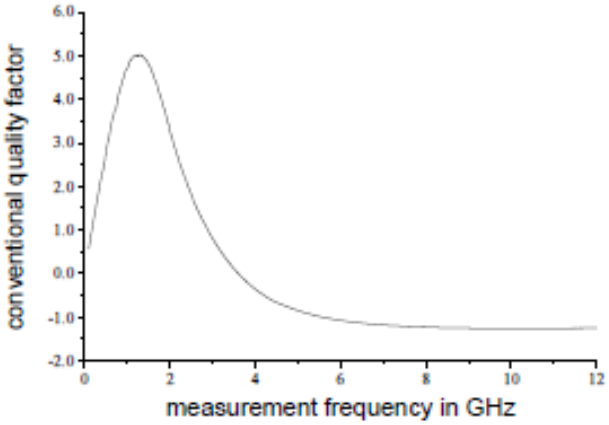


Figure 3-7 Typical measured plot of conventional quality factor according to Equation 3.6.

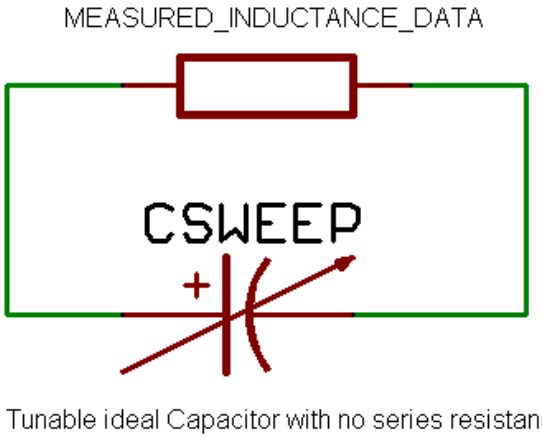


Figure 3-8 Test circuit to extract quality factors according to bandwidth definition.

The 3dB-bandwidth, Δf_{3dB}, at the resonance frequency, f_{res}, of the test circuit shown in Figure 3-8 is then converted to an effective quality factor Q_{BW} via

$$Q_{BW} = f_{res}/\Delta f_{3dB} \tag{3.7}$$

This figure serves as quality factor as it describes the frequency selectivity of the virtual LC-tank. In plots Q_{BW} is typically shown as a function of the resonance frequency of the virtual tank.

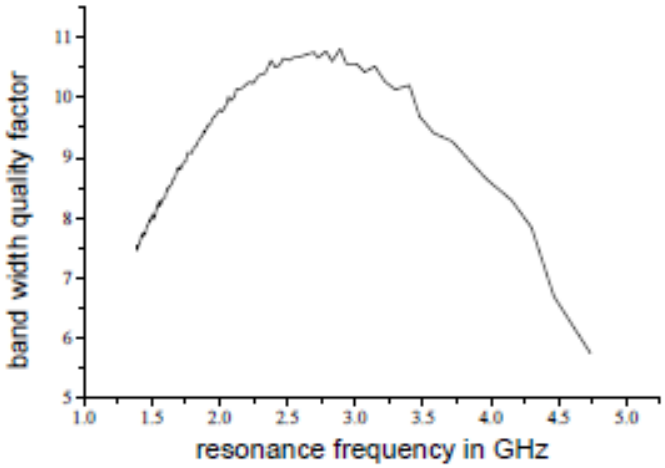


Figure 3-9 Typical plot of quality factor according to the bandwidth definition based on measured inductor data.

The quality factor according to the bandwidth definition offers two considerable advantages over the conventional definition. First, it remains useful up to the self-resonance frequency of the inductor. Second, it allows the designer to identify an oscillator's frequency range at which the quality factor is highest and simultaneously gives the necessary parallel capacitance.

Methods to improve Q of inductors: For low phase noise and lower power consumption of a VCO, it is essential that the passive elements of the tank have large quality factors. However, at the frequencies for mobile communications the quality factors of integrated inductors are usually much lower than the quality factors of conventional diodes or MOS varactors. Mostly, low cost CMOS technology is preferred in IC design. The CMOS technology has some disadvantages as compared to its competing technologies, bipolar and BiCMOS. The main disadvantages are:

- The smaller thickness of metal layer causes higher series resistance.

- The distance between the inductor and the substrate are low and substrates are highly doped. This results in strong coupling to the substrate.

Hence, to improve the performance of inductors it is required to minimize the losses through parasitic component reduction.

One method used to reduce the series resistance is to make parallel connections of the metal layers. Certain substrate structures and ground shields can further minimize it. Nevertheless, most of these techniques reduce the eddy currents while the capacitive coupling remains untouched or increases. The reduction in the eddy currents due to ground shield patterning lowers the self-resonant frequency of the inductor.

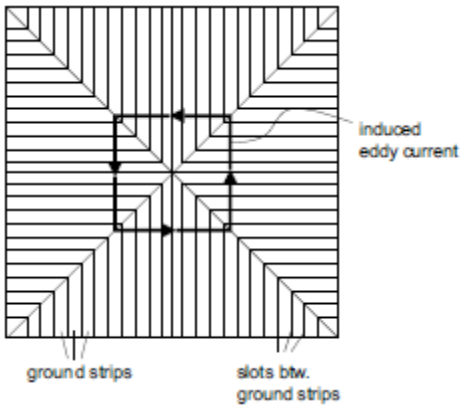


Figure 3-10 Principle of patterned ground shields.

To reduce the parasitic capacitance in standard CMOS technology the only solution is to have the depletion region below the inductor. This depletion causes a well structure called the n- well, that will decrease the parasitic capacitance. However, with this n- well structure any patterning cannot reduce eddy currents.

3.1.8 Power Dividers

RF power dividers are traditionally realized using transmission lines. Lumped passive implementation of power dividers has also been used to reduce the size of the power dividers. This, however, will increase the insertion loss and limit the bandwidth. Figure 3-11 shows the equivalent circuit of the lumped Wilkinson power divider. The use of CMOS active inductors to replace passive spiral inductors in RF power dividers is proposed by Lu and Wu in [27] to take advantage of high quality factor, low silicon area, and high self-resonant frequency of CMOS active inductors.

3.2 Spiral Inductors

The layout of monolithic on-chip inductors and transformers gives them the name of spiral inductors and transformers. Both planar and stacked spiral inductors have been developed and the detailed characterization and modeling of these inductors and transformers are available. Modern CAD tools for IC design are equipped with spiral inductors as standard elements in their component libraries.

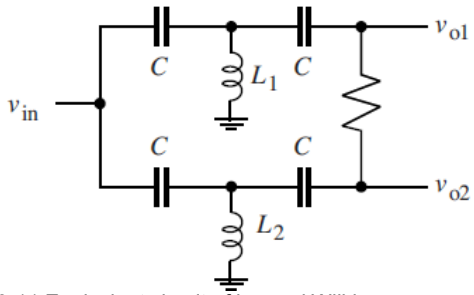


Figure 3-11 Equivalent circuit of lumped Wilkinson power divider.

3.2.1 Planar Spiral Inductors

Figure 3-12 is a sketch of square-shaped planar spiral inductors. The lumped equivalent circuit of spiral inductors is given in Figure 3-13, where

- *L* is the inductance of the spiral inductor,
- *Rs* represents the series resistance of the spiral caused by the skin-effect and the resistance induced by the eddy current in the substrate [28],
- *Cs* accounts for the capacitance due to the overlap of the spiral and the center-tap underpasses,
- *Cox* denotes the capacitance between the spiral and the substrate,
- *Cb* and *Rb* quantify the capacitance and resistance of the substrate, respectively.

Although modern CMOS technologies are equipped with multiple metal layers, typically only the top metal layer is used to construct planar spiral inductors and transformers. This is done in order to minimize the unwanted parasitic capacitance between the spiral pattern and the substrate. As pointed out in [28], the substrate loss accounts for 10-30% of the quality factor reduction of the spiral inductors in low GHz ranges, mainly due to the penetration of the electric field generated by the spiral into the substrate. A main drawback of planar spiral inductors is their low inductance.

3.2.2 Stacked Spiral Inductors

The inductance of spiral inductors can be increased significantly using stacked configurations, as shown in Figure 3-14. As mentioned before, it increases the spiral-substrate capacitance because the lower metal layers are also used in the construction of the inductors [29]. The total inductance of a stacked inductor with two spiral layers is given by

$$L_{total} = L_1 + L_2 + 2M$$

where *L*1 and *L*2 are the self-inductances of spirals 1 and 2, respectively, and *M* is the mutual inductance between the two spirals.

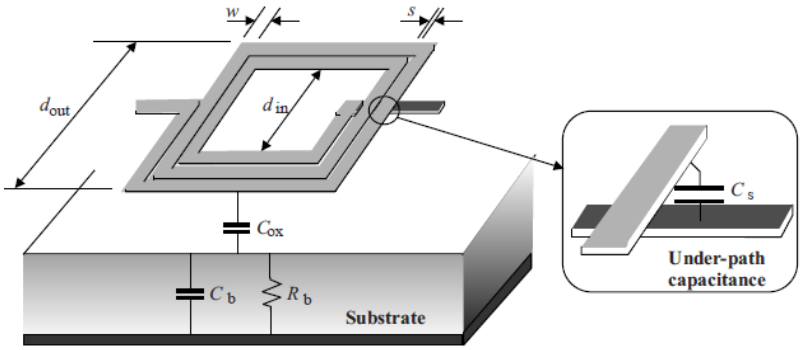


Figure 3-12 Square-shaped planar spiral inductors. w is the width of the spiral trace and s is the spacing between the turns of the spiral.

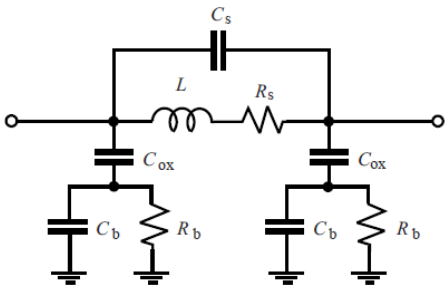


Figure 3-13 Lumped circuit model of planar spiral inductors

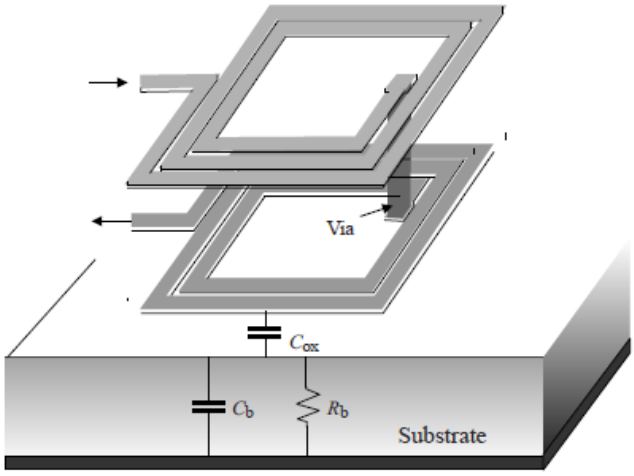


Figure 3-14 Square-shaped stacked spiral inductors.

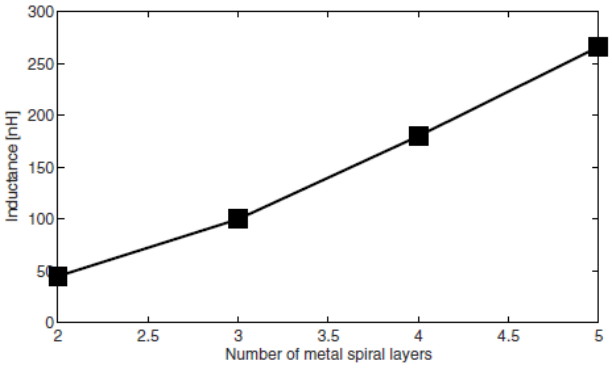


Figure 3-15 Dependence of the inductance of stacked spiral inductors on the number of spiral layers.

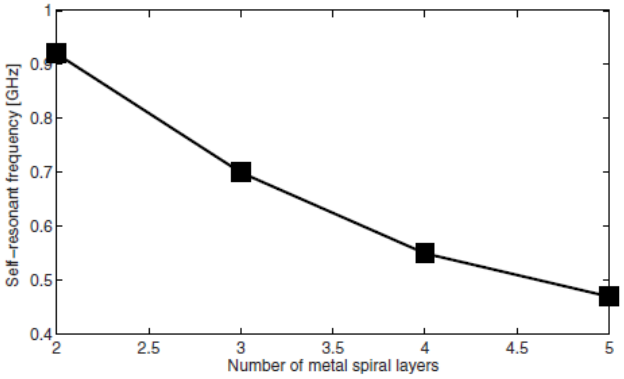


Figure 3-16 Dependence of the self-resonant frequency of stacked spiral inductors on the number of spiral layers.

Note the direction of the routing of the spirals in differential metal layers must be carefully chosen such that the total inductance increases. Figure 3-15 and Figure 3-16 show the dependence of the measured inductance and self-resonant frequency of stacked inductors on the number of spiral layers [29]. It is seen that the inductance of stacked spiral inductors increases approximately linearly with the increase in the number of the spiral layers. The self-resonant frequency of stacked inductors decreases with the increase in the number of spiral layers in a nonlinear fashion.

3.2.3 Characteristics of Spiral Inductors

Spiral inductors offer the key advantages of superior linearity and a low level of noise. There are a number of drawbacks that are intrinsic to the physical geometry of these passive devices and integrated

circuit technologies in which spiral inductors are implemented that affect their performance and applications. These drawbacks include:

- *Low quality factor* - The quality factor of spiral inductor is limited by the ohmic loss of the spiral at high frequencies. Two sources that contribute to the ohmic loss of the spiral inductors include resistance due to skin-effect and the resistance induced by eddy currents in the substrate. The skin effect resistance is proportional to the square root of the signal frequency whereas resistance due to eddy currents is proportional to the square of the signal frequency. Because the resistance of the substrate in the lateral direction is much larger as compared with that in the vertical direction [30], the eddy currents in the lateral direction in the substrate are small. The substrate eddy current induced resistance of the spiral is often negligible compared to the resistance caused by the skin-effect [29]. The quality factor value for a spiral inductor in standard CMOS is typically below 20.
- *Low self-resonant frequency* - The self-resonance of a spiral inductor is the resonance of the LC tank formed by the series inductance of the spiral inductor and the parasitic shunt capacitance. The shunt capacitance is formed between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low self-resonant frequency of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral [31]-[34].
- *Low and fixed inductance* - As pointed out earlier the inductance of a planar spiral inductor is low and fixed once the number of the turns of the spiral is set. The only way to increase the inductance of the spiral inductor is to either increase the number of turns of the spiral or use a stacked configuration where spirals on multiple metal layers are connected using vias. The former is at the expense of a large silicon area while the latter increases the spiral-substrate capacitance.
- *Large silicon area* - The planar spiral inductors have low inductance, and since the inductance is directly proportional to the number of the spiral turns, the silicon area required for routing is large. As an example, as shown in [18], a square-shaped spiral inductor of 8nH requires 6 turns with $d_{out} = 400\mu m$. The actual silicon consumption of the inductor is larger than $400 \times 400 \mu m^2$ when design rules on the minimum spacing are followed. Moreover, the design rules of most IC foundries prohibit the placement of either active or passive devices in the region between the spiral of the inductors and the substrate, making spiral inductors the components that consume the most silicon.

3.3 Integrated Inductors

Integrated inductors offer many advantages over bond-wires the most prominent being:

- Easy and exact manufacturability
- Very little inductance variations

However, they have a relatively larger die area.

3.3.1 Common inductor designs

The most common integrated inductors are hollow spiral inductors (connected metal traces arranged in a spiral configuration). Mostly the spiral inductors have several windings, and hollow in this context means that none of the windings extend into or near to the center of the device. (Further on, when the term inductor is used, it stands for integrated, spiral, hollow inductor.) Figure 3-17 depicts some important inductor designs, a quadrilateral, an octagonal and a symmetrical octagonal inductor.

Figure 3-17 Quadrilaterals, octagonal and symmetrical octagonal inductor designs.

Symmetrical inductors appear identical from either port, an essential property for differential VCO applications. The homogeneity of the magnetic field can be increased through increasing the circularity. However, in many cases the extent to which the number of corners can be increased is limited by mask data preparation often only allowing 45° and 90° angles between metal lines (i.e. quadrilateral and octagonal inductors).

The advanced features of using submicron multilayer substrates enable the reduction of some disadvantages of the integrated inductors. Each layer can use the identical pattern and the individual layers connected in two different methods. In the first method, each layer is connected in series thereby increasing the inductance of the integrated inductor. The overall construction looks like a solenoid. This construction however, increases the series resistance of the inductor as the overall length of the metal has increased. In addition, as the adjacent metal layers are not at the same potential the capacitance between them becomes active. The second method on the other hand connects the two layers in parallel thereby reducing the series resistance. If the series resistance of a one-layer inductor is R_s and n similar layers are used then the series resistance of n-layer inductor would be R_s/n. The low-ohmic connections between the adjacent layers can keep the capacitance low too.

3.3.2 Electrical properties of inductors

The differential output signals of the VCO appear at the inductor nodes. The swing of this signal is large and the inductor is subject to large-signal AC currents. To model the resulting electrical properties (and problems) of an inductor a simple π-model is sufficient (although it might not be enough to simulate the inductor accurately). Figure 3-18 shows the cross section of a simple integrated inductor and the lumped elements forming the π-model (grey bar indicates the simplified one metal layer inductor). The inductor is described by the inductance L and the series resistance of the metal windings R_l. There is a parasitic capacitance C_f from input to output (including the capacitances between adjacent windings) and a capacitance C_{ox} from the inductor to the grounded substrate. R_{sub} describes an effective substrate resistance.

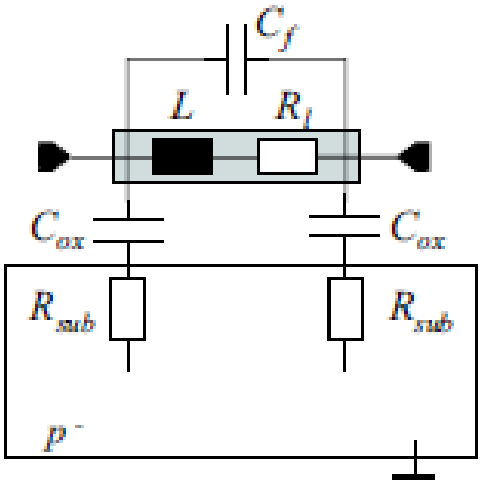


Figure 3-18 Cross section of a simple one-layer inductor (grey bar) and its lumped-elements model (in low-ohmic substrate).

- Inductance

The inductance L of a rectangular inductor can be calculated by the Greenhouse method [58, 59]. There exist handier simplifications, e.g. the inductance of a hollow, square inductor is approximated by [50, 53]

$$L \approx \frac{45\mu_0 n^2 a^2}{22r-14a} \tag{3.8}$$

with μ_0 the permeability of vacuum (the relative permeability μ_r is assumed to be 1), n is the number of windings, r is the outer radius and a is the mean radius of the inductor (Figure 3-19). This formula generally yields accurate results with less than 5% error.

The above formula is simplified for quick, crude calculations to

$$L \approx \mu_0 n^2 r \tag{3.9}$$

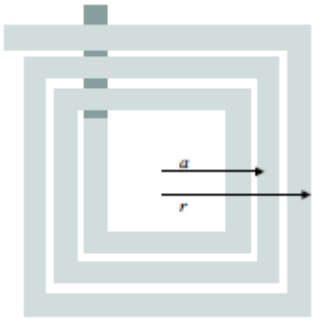


Figure 3-19 Top view of a square inductor and dimensions necessary for inductance calculation.

3.3.3Losses in the metal windings

The series resistance of the metal windings at low frequencies can be calculated as the product of the resistance per square and the total number of metal squares. At high frequencies magnetic field effects result in non-uniform current flow in the conductor. This further increases the series resistance of the windings. The most prominent of these effects is the skin effect resulting from the inner self-inductance of the conductor [60]. It causes current crowding at the surface of the conductor. The thickness of the sheet in which current flows depends on permeability and resistivity of the conductor and frequency.

In digital CMOS, metal layers are thin and hence current crowding in the vertical direction does not play a role. However, the winding width often exceeds the skin depth and the skin effect leads to a noticeable increase in series resistance. The skin effect is enhanced due to the magnetic field originating from a nearby conductor called the proximity effect. The magnetic field generated by the inductor passes not only through the center of the inductor but is also strong in a certain area around the center.

If windings extend near to or into the center of the inductor the magnetic field will lead to circular eddy currents in the inner windings. These eddy currents will disturb the original current flow in the inductor and generate a magnetic field in the opposite direction of the inductor's field. Therefore, at high frequencies, the total resistance increases and the inductance decreases (as the total magnetic field decreases). The innermost windings do not contribute significantly to the inductance (as they enclose only a small area) but have a detrimental effect on resistance.

3.3.4 Losses in the substrate

The large-signal AC currents in the inductor result in undesired capacitively and inductively induced substrate currents. They are described by the resistances R_{sub}. The capacitively induced substrate currents stem from the capacitive coupling between the inductor and the substrate C_{ox}. The first order approximation is given as $C_{ox}/A_{metal} = d_{ox}$, where, A_{metal} is the total metal area of the inductor and d_{ox} is the thickness of the oxide between the metal layer and the substrate. The constantly changing magnetic field around the inductor results in inductively induced eddy currents in the substrate (according to Lenz's Law). Both type of currents increase the losses of the inductor and deteriorate its performance.

In order to minimize the influence of these currents the inductors are realized on the topmost layer. This reduces the coupling capacitance C_{ox} (as the oxide thickness is increased) and reduces the magnetic field of the inductor (and therefore the induced eddy currents) in the substrate. A lower doped substrate also helps. The lower doping means highly resistive substrates, and hence the current flow in the substrate is suppressed.

3.3.5 Model for extraction of inductor parameters

To extract parameters the complex inductor is generally viewed as simple series connection of an effective inductance and an effective series resistance (Figure 3-20), both with frequency dependent values $L_{eff}(f)$ and $R_{eff}(f)$.

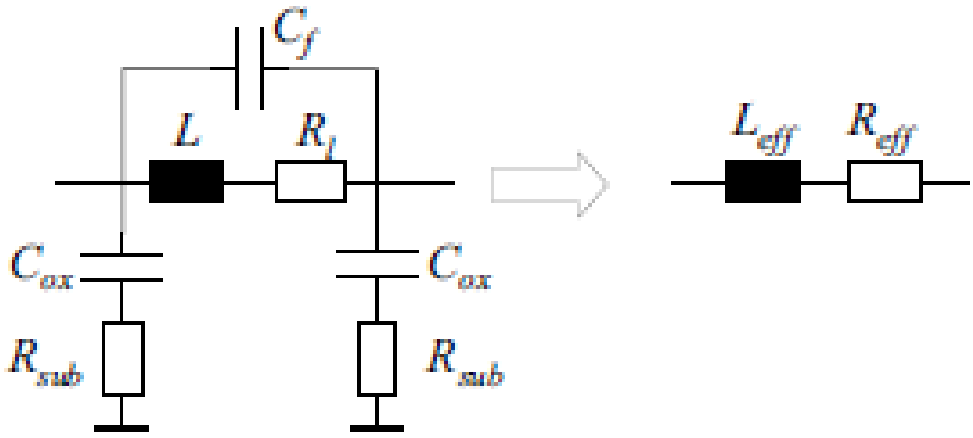


Figure 3-20 Further simplification of simple π-model of the inductor for parameter extraction.

Due to this simplification the typical inductance and resistance plots (Figure 3-21) of an inductor show a strong frequency dependence introduced mainly through the parasitic capacitances.

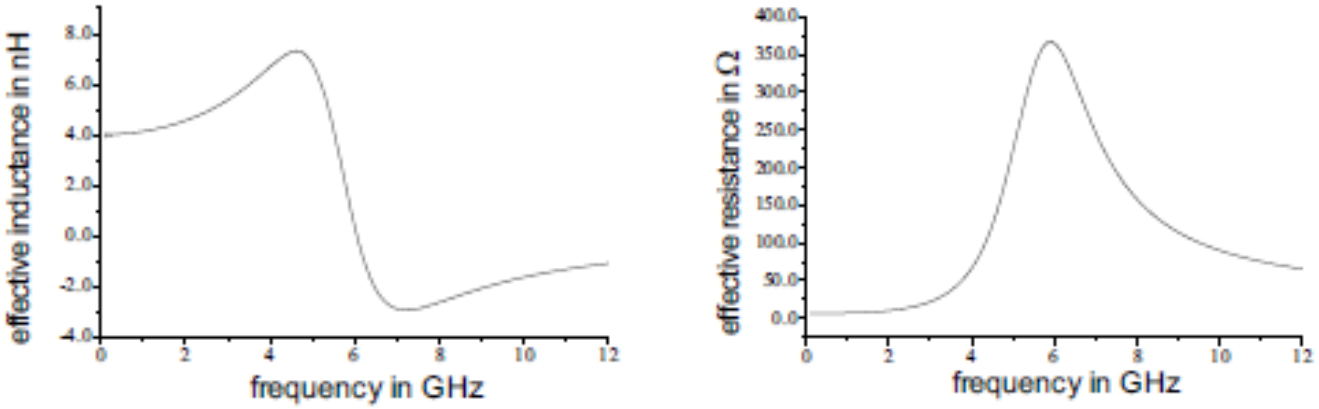


Figure 3-21 Typical measured effective inductance and resistance plots of an inductor.

At a certain frequency, the self-resonance frequency, the effective inductance even becomes zero, as L resonates with the parasitic capacitances.

3.3.6 Inductor design

Two examples of integrated inductor designs are discussed in section 3.3.7. They are realized either in 0.25µm technology with four aluminum layers or in 0.12µm technology with six copper layers.

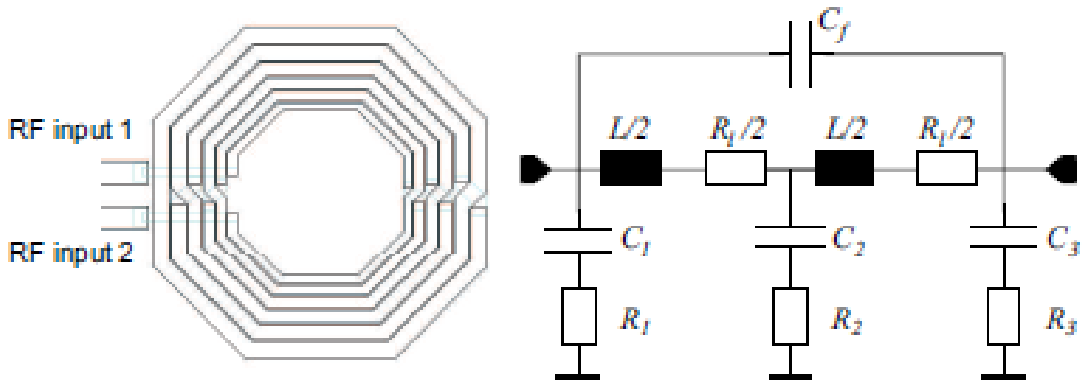


Figure 3-22 Symmetrical, octagonal inductor and equivalent double-π model.

The symmetrical inductor with octagonal windings as shown in Figure 3-22, features two RF inputs at the inner windings; the outer winding is at common mode. A lesser capacitive penalty is applied if the winding width is increased from inner to outer winding. The series resistance is lower due to the wider winding being the longest.

As discussed earlier, to reduce series resistance several metal layers are shunted, resulting in a thicker effective metal layer. A connection between the layers is made with interleaved copper vias, to provide a low-ohmic connection between the windings and further lower the series resistance. The inductor is represented with the double-π model of Figure 3-22.

L denotes the inductance and R_l the series resistance. The parasitic capacitances between the metal layers of the inductor and the substrate are denoted by C_1, C_2 *and* C_3 where C_1 and C_3 are equal due to

symmetry. Similarly, $R_1 = R_3 = R_2$. C_f describes the parasitic capacitance resulting from the coupling between the windings and the two terminals.

3.3.7 Parameter extraction

The de-embedding on the wafer S-parameter measurements [61] are used to extract the effective inductance L_{eff} and resistance R_{eff} parameters. The S-Parameter obtained are converted to Y-parameters and used in the equation below.

$$L_{eff}(f) = Im(Y_{11}^{-1})/2\pi f\ ;$$
$$R_{eff}(f) = Re(Y_{11}^{-1}) \tag{3.10}$$

Where f is the swept frequency. Quality factor is determined based on Equation (3.6).

3.3.8 The two designed examples.

Two inductors 3.7nH and 4.4nH are fabricated and the measured results are presented. The design data is shown in the tabulated form below.

The 3.7nH inductor is designed as a differential, symmetrical inductor comprised of six octagonal windings. To reduce series resistance the winding width is staggered (larger width at outer winding). The metal (aluminum) in layers 2, 3, and 4 of the four-metal layer process are connected in parallel (0.25µm technology). The layout of this inductor is shown in Figure 3-23 and its measured plots are shown in Figure 3-24.

Table 3-2 Design data of the 3.7nH inductor

Windings	winding width min/max	radius inner/outer	spacing min/max	metal
6	2.9µm/5.8µm	30µm/58µm	0.6µm	2, 3, 4 aluminum

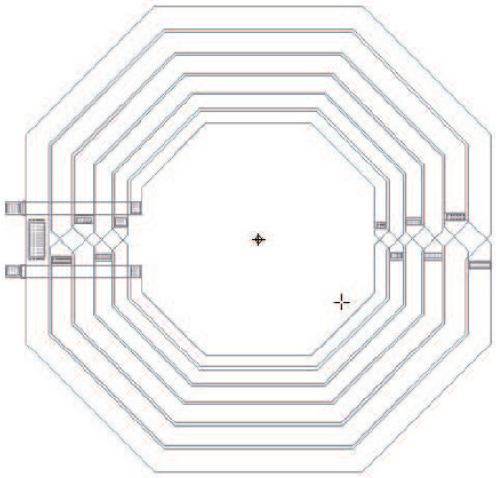


Figure 3-23 Layout of the 3.7nH inductor

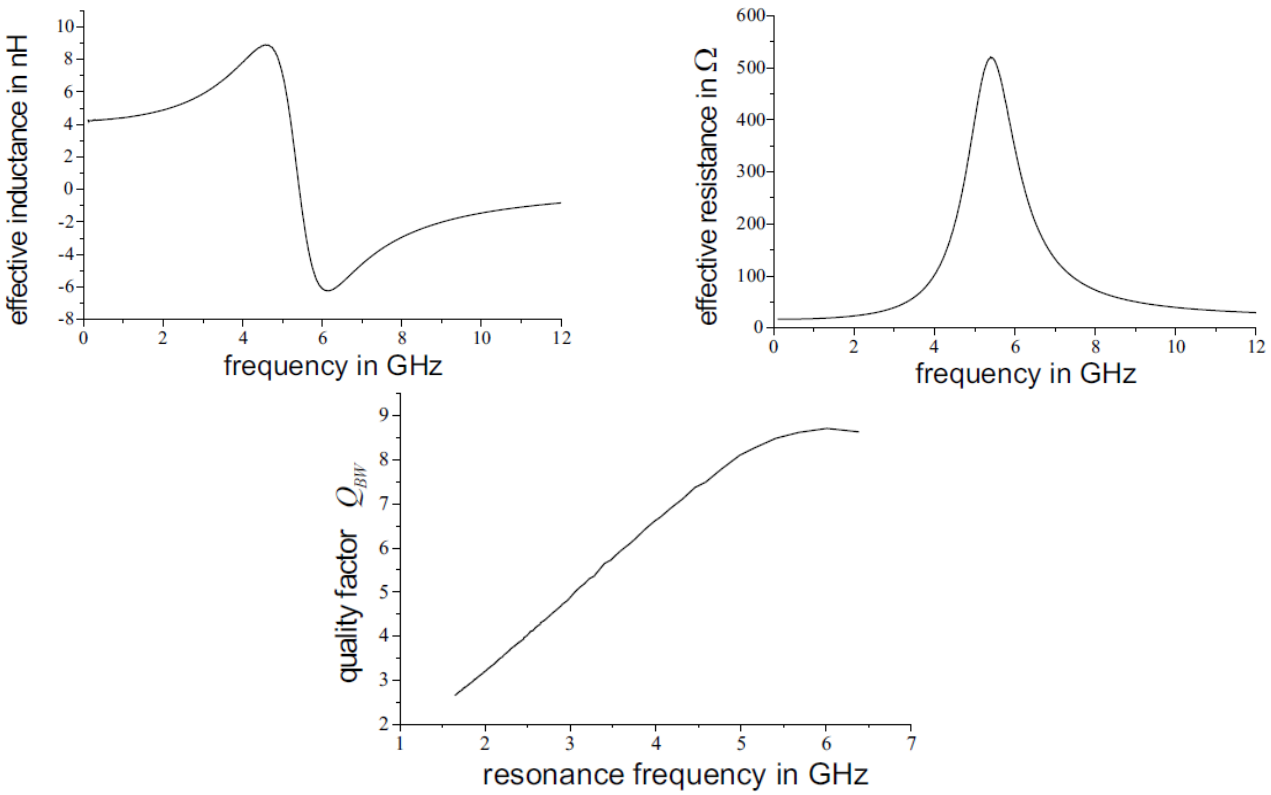


Figure 3-24 Measurement results of the original 4.2nH inductor (3.7nH by scaling) showing the effective inductance, effective resistance and the quality factor of the inductor.

The low-frequency inductance is 4.2nH (scaled 3.7nH) and the resistance is 16.7Ω. The quality factor reaches a maximum value above 9 (scaled 7.5).

A 4.4nH inductor is designed as a differential, symmetric inductor with six octagonal windings. To reduce series resistance the winding width is staggered (larger width at outer winding). The metal (Copper) in layers 4, 5, and 6 of the 0.12µm digital CMOS process are connected in parallel with copper via bars. The layout of this inductor is shown in Figure 3-25 and its measured plots are shown in Figure 3-26.

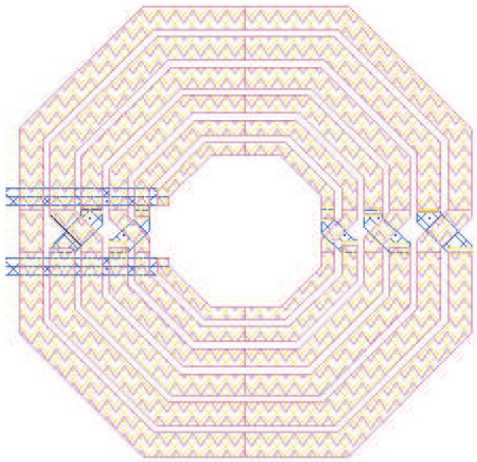


Figure 3-25 Layout of the inductor (4.4nH)

Table 3-3 Design data of the inductor.

Windings	winding width min/max	radius inner/outer	spacing min/max	Via bars Width/spacing	metal
6	5µm/10µm	32µm/95µm	2.8µm/3.2µm	0.4µm/0.8µm	4,5,6 copper

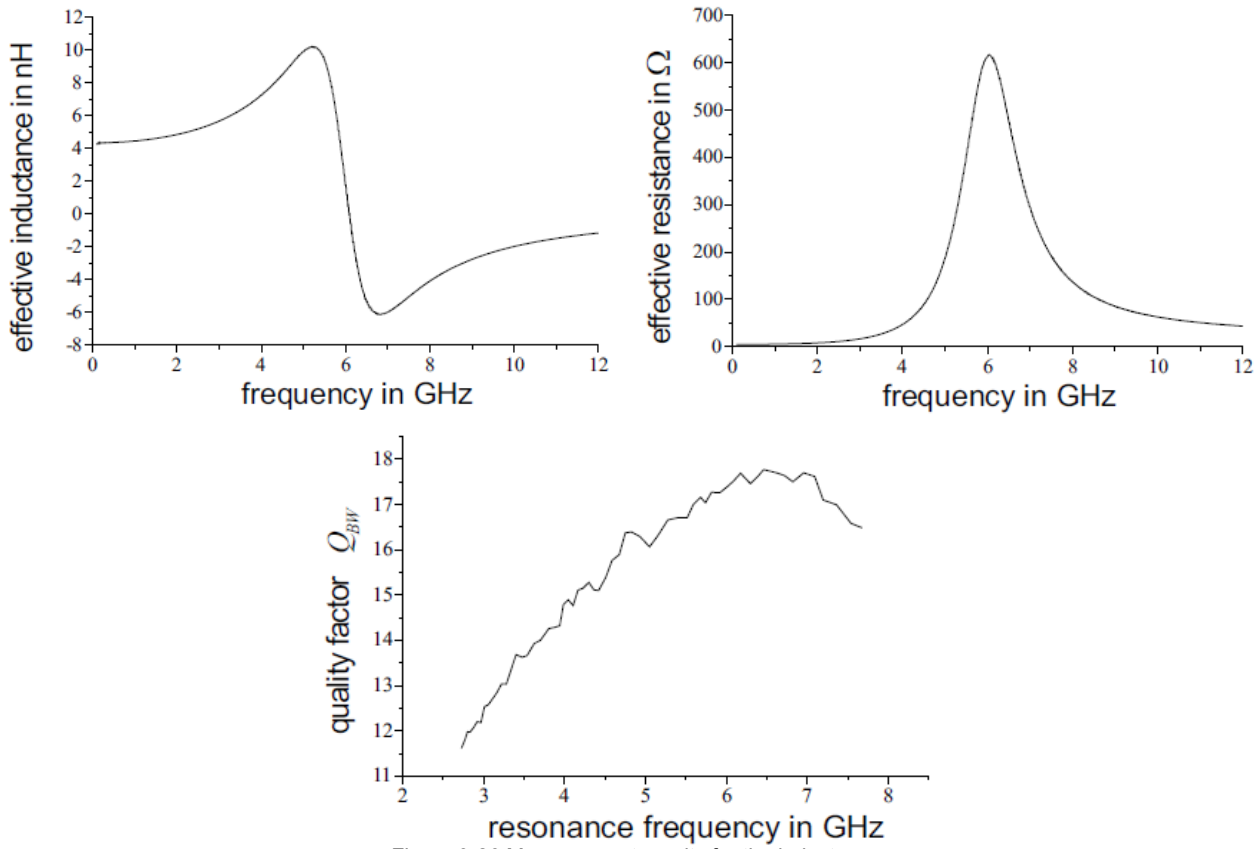


Figure 3-26 Measurement results for the inductor.

Figure 3-26 summarizes measurement results for the inductor. The inductor features an inductance of 4.4nH and a DC series resistance of 4.7Ω. The maximum quality factor is 18.

3.3.9 Substrate structure for integrated inductors

The proposed structure is fully compatible with standard digital CMOS process flow and low resistivity substrates. It is comprised of alternating n depleted (denoted as n-) well and p depleted (denoted as p-) substrate regions. By applying a voltage to the structure, the semiconductor region below the inductor is depleted from mobile charge carriers up to a certain depth.

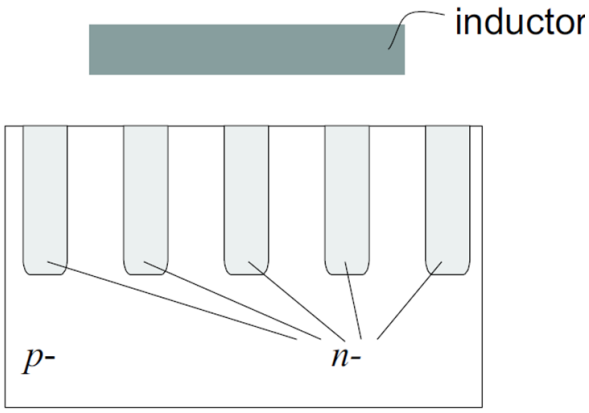


Figure 3-27 Substrate structure: thin, parallel n- wells in p- substrate and a simple one-layer inductor (grey bar).

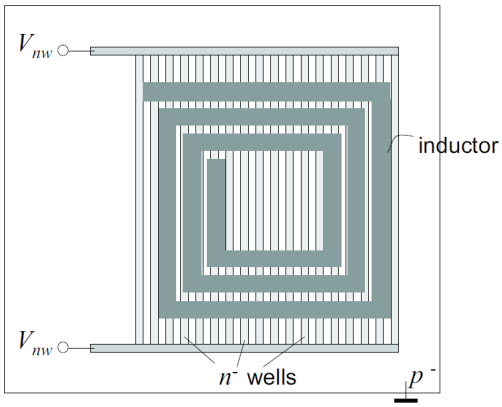


Figure 3-28 Substrate structure: thin, parallel n- wells in p- substrate and a simple one-layer inductor.

Substrate losses due to parasitic capacitances and eddy currents are thereby reduced. Four test structures with the identical inductor, three with and one without the substrate structure, are compared in a standard 0.12µm digital CMOS process. The cross-section of the substrate structure and (for simplicity) a one-metal layer inductor is shown in Figure 3-27; a top view is shown in Figure 3-28.

In the simplest case the substrate structure is implemented as parallel stripes of equidistant n- well and p- substrate regions. At both ends, the n- wells are connected by highly doped n+ regions and a voltage can be applied. Increasing the voltage applied to the n- wells increases the depletion region laterally between them, and vertically beneath them. At some n- well voltage the depletion regions of two adjacent n- wells touch and deplete the p- substrate totally to at least the depth of the n- wells (Figure 3-29). The n- wells themselves will be partially depleted, too. The depleted semiconductor layer leads to a reduced effective small-signal capacitance between inductor and substrate. Assuming that the non-depleted width of the n- wells is negligible, this capacitance can be approximated by

$$C_{eff} = \left(C_{ox}^{-1} + C_{jd}^{-1}\right)^{-1} \tag{3.11}$$

where C_{jd} is the depletion region capacitance.

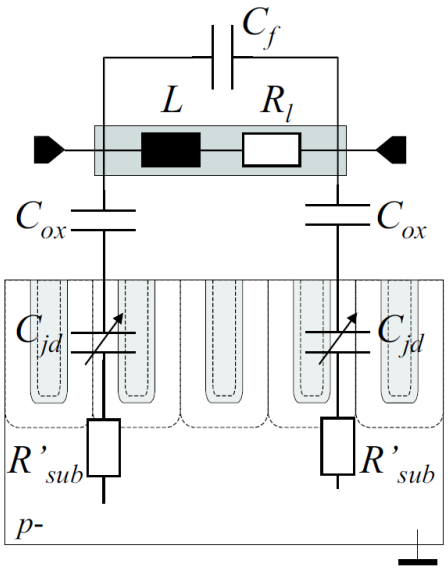


Figure 3-29 Simple inductor (grey bar) and substrate structure with totally depleted p- substrate regions between the n- wells. Dashed lines indicate the borders of the depletion regions.

The n- wells should be as thin as possible. The n- wells in the substrate can only be partially depleted due to their higher doping level as compared to the p- substrate.

Table 3-4 summarizes the design data for the reference inductor to evaluate the substrate structure.

Table 3-4 Design data of the inductor used to evaluate the substrate structure.

Windings	winding width min/max	radius inner/outer	spacing min/max	Via bars Width/spacing	metal
5	4.8µm/10µm	45µm/90µm	1.8µm/2.9µm	0.2µm/0.8µm	2,3,4 copper

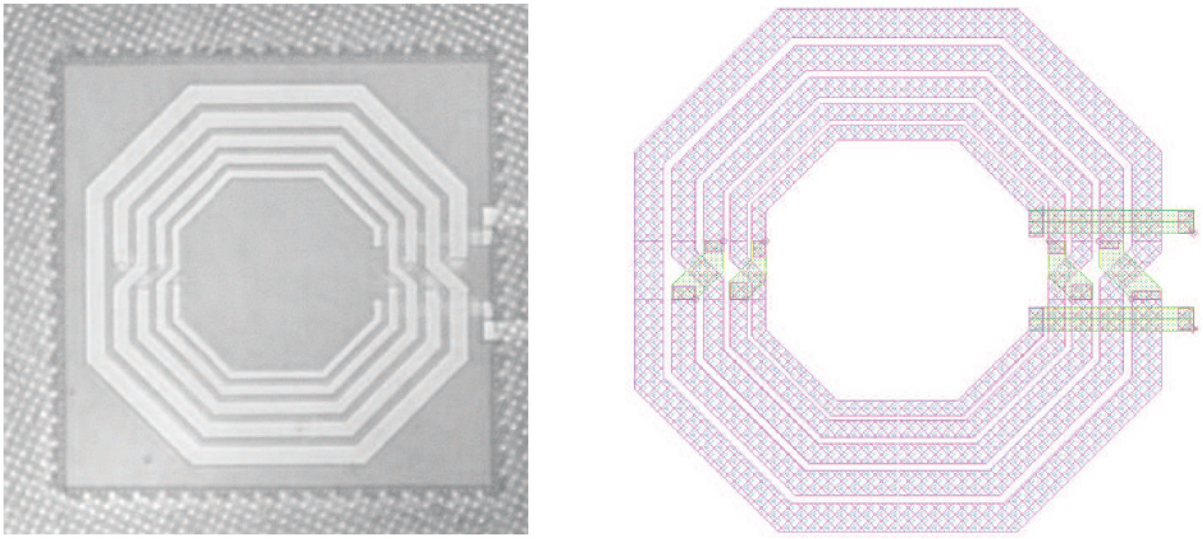


Figure 3-30 Die photograph and layout of the inductor used for evaluation of the substrate structure.

Figure 3-30 shows the die photograph and layout of the reference inductor constructed. The reference inductor is fabricated without the substrate structure. Clearly visible is the suppression of metal fill structures in the area of the inductor. Inductor size is 200µm x 200µm. The substrate structures for the other three inductors feature equidistant n- well stripes with minimum allowed width. Spacing of the n-wells is 0.7µm, 1.0µm and 1.3µm respectively.]

Figure 3-31 summarizes measurement results for the reference inductor. The measured inductance is 4.0nH at a DC series resistance of 6.2Ω. These values are not influenced by the substrate and are identical for the other three inductors. The 3dB quality factor of the reference inductor reaches a maximum value of 8.6.

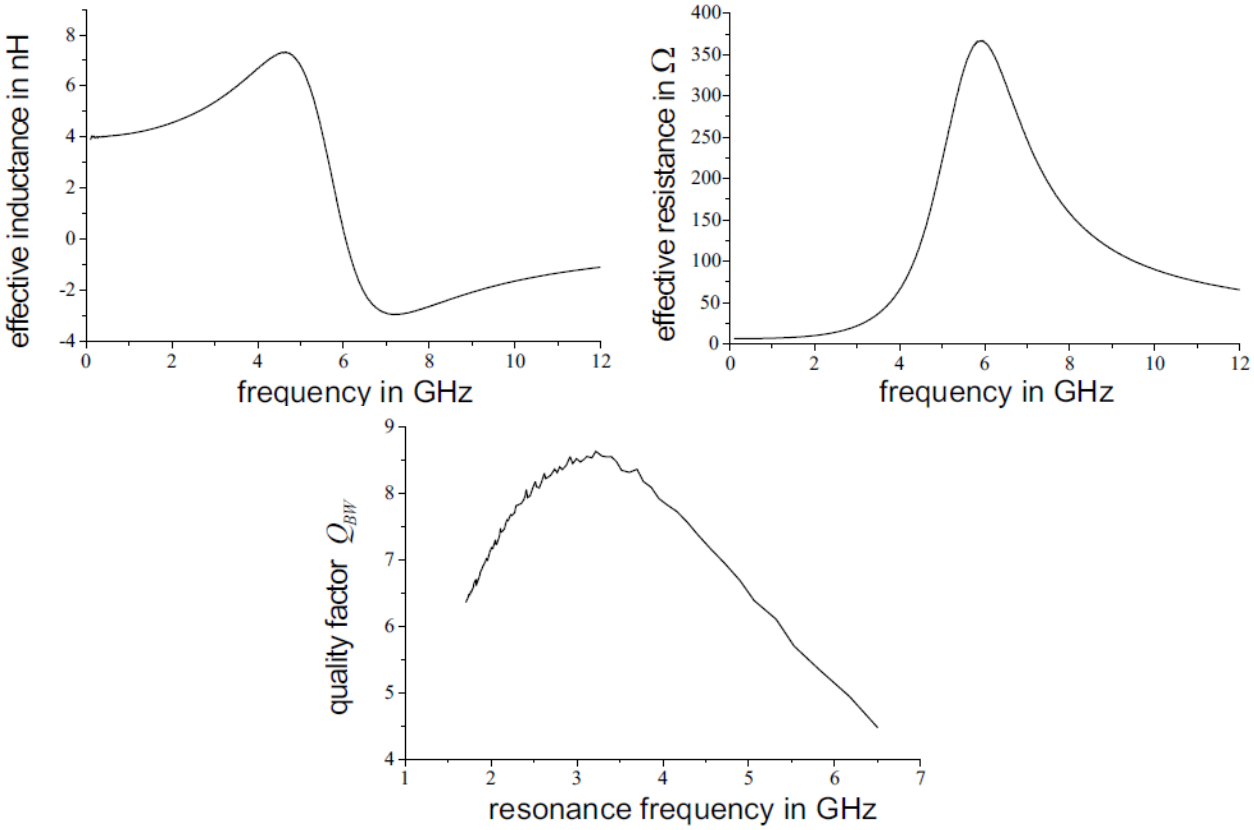


Figure 3-31 Measurement results of the reference inductor (3 plots).

The measured quality factor of the inductors with substrate structures is plotted in Figure 3-32 – Figure 3-34. Table 3-5 lists the maximum quality factor and the corresponding resonance frequency. Figure 3-32 depicts the quality factor of the inductor with 0.7µm distance of the n- wells at four different n- well voltages V_{nw} in comparison to the reference inductor.

Due to the built-in voltage of the n- well/p- substrate junction, depletion regions are already present at zero n- well voltage. They reduce C_{eff} and the eddy current. Thus, even at zero V_{nw} the substrate structure increases the maximum quality factor as well as the corresponding resonance frequency by 34% compared to the reference inductor. Increasing V_{nw} from 0V to 1.5V increases the maximum quality factor by further 5%. The corresponding resonance frequency is 16% higher. At n- well voltages of 3V and 4.5V no further influence is observed. The p- substrate regions are totally depleted at 1.5V already.

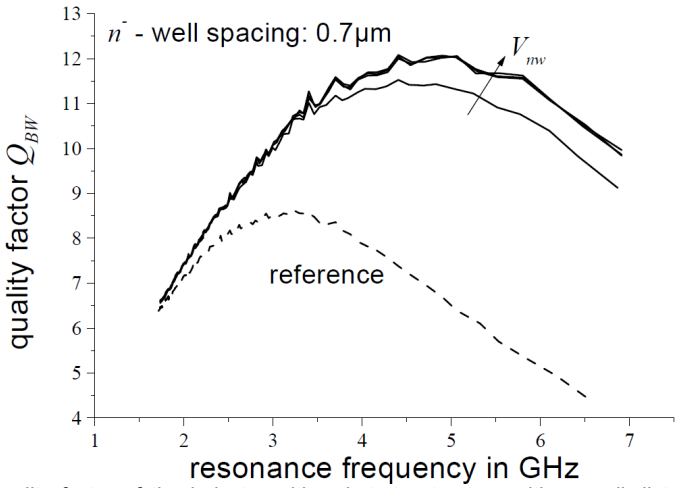


Figure 3-32 Measured bandwidth quality factor of the inductor with substrate structure with n- well distance 0.7µm and at n- well voltages (V_{nw} = 0V to 4.5V in 1.5V steps).

The quality factor results for the inductor with n- well distance of 1.0µm in comparison to the reference inductor are shown in Figure 3-33. At zero n- well voltage a 27% higher quality factor and a 25% shift in resonance frequency is obtained. With a V_{nw} increase from 0V to 1.5V the maximum quality factor of the inductor increases by further 12% and the resonance frequency shifts by 25%. Similarly, to the substrate structure with 0.7µm distance of the n- wells, the p- substrate regions seem to be totally depleted at 1.5V already and a further increase of applied voltage has no effect. Figure 3-34 depicts the quality factor of the inductor with 1.3µm n- well separation in comparison to the reference inductor.

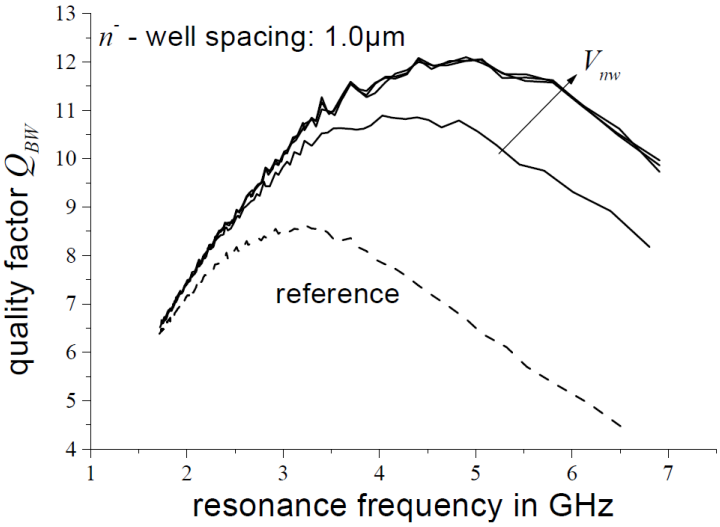


Figure 3-33 Measured bandwidth quality factors of the inductor with substrate structure with n- well distance 1.0µm and at n- well voltages (V_{nw} = 0V to 4.5V in 1.5V steps).

At zero V_{nw} a 16% higher maximum quality factor and a 22% higher resonance frequency as compared to the reference inductor are observed. The maximum quality factor is further increased by 14% through applying a voltage. The resonance frequency at maximum quality factor shifts to higher frequencies by another 28%. Contrary to the two inductors with closer n- well spacing different maxima are observed at all values of V_{nw}, indicating that only above 4.5V a total depletion of the p- substrate regions between the n- wells can be obtained.

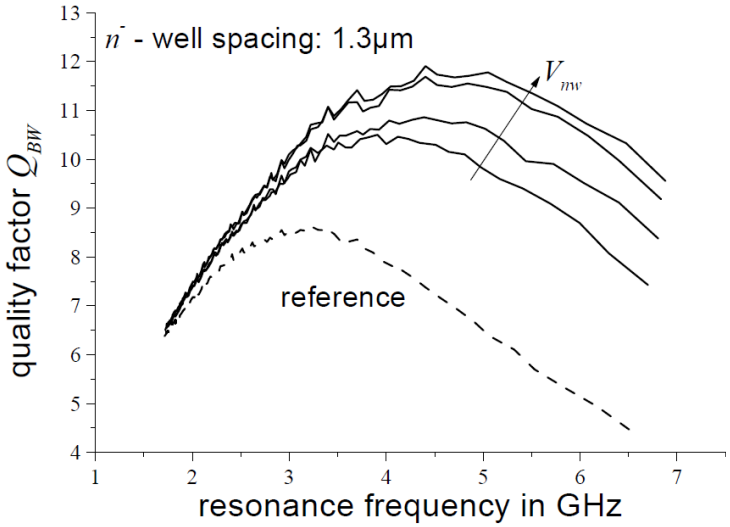


Figure 3-34 Measured bandwidth, quality factor of the inductor with substrate structure with n- well distance 1.3µm and at n- well voltages (V_{nw} = 0V to 4.5V in 1.5V steps).

The maximum quality factors at zero V_{nw} are lower with larger n- well distance (compare Figure 3-32, Figure 3-33, and Figure 3-34). With closely spaced n- wells the depletion region due to the built-in voltage of n- well/p- substrate junction lead to a larger depleted area and smaller capacitance. At larger n- well spacing and this situation the decreased capacitance is only reached at some non-zero V_{nw}. Additionally more freely flowing eddy currents in wider p- substrate regions might be of importance.

Table 3-5 Measured maximum quality factors and corresponding resonant frequencies at different n- well voltages.

	$Q_{BW,max}$ @ $f_{resonance}$		
Vnw	0.7µm	1.0µm	1.3µm
0V	11.5 @ 4.3GHz	10.9 @ 4.0GHz	10.5 @ 3.9GHz
1.5V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	10.9 @ 4.4GHz
3.0V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	11.6 @ 4.9GHz
4.5V	12.0 @ 5.0GHz	12.1 @ 5.0GHz	11.9 @ 5.0GHz
Reference inductor: 8.6 @ 3.2GHz			

Despite the fact that the total number of n- wells underneath the inductor is different in each case, all inductors reach the same Q value at total depletion. The depletion of the n- wells into p- substrate is considerably larger than into p- wells. Therefore the average doping of the n- wells in the substrate structure is much lower and depletion regions within much wider than in conventionally used n- wells. The non-depleted regions within the n- wells do not play a significant role and thus the different number of n- wells does not show in the maximum results.

3.4 Active Inductors

A novel circuit network is described here using active devices, known as active inductors. Under certain DC bias conditions and signal level constraints, these networks exhibit an inductive characteristic in a specific frequency range. As compared with their spiral counterparts, active inductors offer the following attractive advantages:

- *Low silicon area* - The inductance values of active inductors is inversely proportional to the transconductance of the transistors; the silicon area is negligible as compared with that of their spiral counterparts.

- *Large and tunable self-resonant frequency* - A typical active inductors with a large self-resonant frequency are highly desirable. A large self-resonant frequency of active inductors ensures that the active inductors will have an inductive characteristic over a large frequency range.
- *Large and tunable inductance* – In general, the inductance of active inductors is inversely proportional to the transconductance of the transistors synthesizing the inductor. Large inductance value implies a smaller finger width of the transistors. The inductance value can be tuned conveniently by varying the DC bias condition for the transistors comprising the active inductor providing a large inductance tuning range.
- *Large and tunable quality factor* - The quality factor of active inductors is set by the ohmic loss from the finite output resistance of the transistor transconductance. The quality factor of CMOS active inductors can be maximized by increasing this output resistance. A number of methods are available to boost the output resistance, such as the cascode, regulated cascode, and negative resistor compensation. In each of these approaches, the degree of compensation can be varied.
- *Compatibility with digital CMOS technologies* - Spiral inductors are not available in low-cost digital-oriented CMOS processes. CMOS active inductors can be realized using standard digital CMOS processes. CMOS active inductors have found increasing applications in areas where an inductive characteristic is required. Table 3-6 summarizes some of the recently published work where CMOS active inductors were employed.

The application of active inductors inherits the disadvantages of intrinsic characteristics of active devices (transistors) such as:

- limited dynamic range,
- a high level of noise,
- High sensitivity to process spread, supply voltage fluctuation, and ground bounce.

However, these drawbacks can be overcome by novel and innovative designs. For example, the limited dynamic range of active inductors can be expanded using class-AB configuration where the voltage swing of active inductors can be made nearly rail-to-rail [45]. The effect of the high sensitivity to process spread can be minimized by making use of the tunability of both the inductance and quality factor of active inductors. The effect of supply voltage fluctuation and ground bouncing can be greatly reduced by using replica biasing techniques and proper circuit configuration [46]. The raised level of noise from active inductors on the phase noise of LC oscillators using active inductors can be minimized by improving the quality factor of the active inductors [47]. New design techniques are yet critically needed to further improve the performance of active inductors.

Table 3-6. Applications of CMOS active inductors and transformers

Ref.	CMOS Technology	Operating Frequency (GHz)	Characteristics and Applications	Publication Year
[35]	0.13μm	2.4	Oscillator	2010
[36]	0.18μm	23-26	VCO	2009
[37]	0.18μm	3.8-7.4	VCO	2008
[38]	0.18μm	1.6	Modulator	2008
[39]	0.18μm	3.34-5.72	BPF (bandpass filter)	2007
[40]	0.18μm	1.6	VCO	2007
[41]	0.18μm	0.5-3.0	VCO	2006
[42]	0.18μm	1.9-2.19	VCO	2005
[43]	0.35μm	2.3	Limiting Amplifier	2005
[44]	0.18μm	3.5-5.7	BPF (bandpass filter)	2004

3.4.1 Active Inductor Based Resonator

Major research in the field of integrable tunable oscillators, is for the implementation of high Q-factor resonator networks using active inductor technology [48]-[56]. The active inductor based resonator possesses the same state equation as the passive inductance-capacitance (LCR+) resonator. It also has some gain and scaling terms to compensate the loss resistance R associated with the passive LC resonator. An active inductor based (LCR-) resonator of a specific Q-factor is always more dissipative than its passive equivalent with the same LC values. This is mainly due to the fact that the active devices consume a certain power for realization of the inductor with negative resistance (-R). Therefore, it is reasonable to expect larger power dissipation for the active inductor, including an increase in rms noise.

Noise in an ideal passive resonator (LCR+) arises from the dissipation represented by the loss resistance R_{Loss} = R+. The mean square voltage of kT/C appears across the passive resonator (LCR+) regardless of the magnitude of R.

The selectivity (ω_0/Q) of the passive resonator is set by the dissipation per the relationship $1/Q = (\omega_0 L/R+)$. Since noise sets the lower limit on a detectable signal in the resonator network, the upper limit may be arbitrarily large if the resonator network is assumed free from inductor saturation or other possible linearity.

The concept of tunable active inductors is not new. However, a limitation of active inductors as a tuning element is due to various factors, mainly dynamic range and noise performances. As a part of this research work, the pros and cons will also be discussed. With respect to different ATI topologies and also a possible alternative of varactor-tuned resonator networks for oscillator circuits (where enhanced Q-factor plays important role) and for tunable filter circuits (where the dynamic range is a critical factor), the dynamic noise cancellation and filtering techniques are applied to overcome the limitation of lower dynamic range. Broadband tuning at millimeter wave frequencies becomes very difficult if not impossible with varactor tuned resonators due to package parasitics. Therefore even with a slightly degraded dynamic range, an active inductor for MMIC VCOs at high frequencies may be a better choice.

3.4.2 State-of-the-Art

Modern microwave circuits are implemented in planar configuration, and frequently as a RFIC/MMIC. Figure 3-35 shows the schematic and layout of 2GHz GaAs FET oscillator using passive spiral inductors [49, pp 241-243]. The two inductors (L_1 and L_2) in the circuit layout determine most of the surface die area and therefore are not a cost-effective solution. The opportunity is to replace the large spiral inductor with an active device (transistor) requiring only a fraction of the size and with equal if not better performance at microwave frequencies. Besides generating an active inductor of the same value and a higher Q-factor as passive spiral inductor, the phase noise performance in oscillators and its large signal capabilities will also be addressed. Such an “active inductor” generates additional noise, which results in a higher noise factor and thereby degraded phase noise performance.

In comparison to the conventional oscillator using passive spiral inductor, active inductors do not show the advantages in phase noise performance but offer compact, cost-effective and integrable solutions.

Additional, poor dynamic range, large signal instabilities and additional DC power consumption can limit the application of the active inductor in the high performance signal source, tunable filter, and wideband

matching network. Figure 3-36a and Figure 3-36b show the schematic and performance of an active inductor using SiGe HBT devices. As shown in Figure 3-36b, the slope of the inductance with control voltage and frequencies can be negative (decreasing L: plot I) or positive (increasing L: plot II) depending upon the TAI topologies. The strong nonlinearities associated under large-signal drive condition (shown in plot I and plot II) makes it intrinsically noisy, thus not suitable for very low-power signals.

Figure 3-37 shows a schematic of a VCO using TAI and active capacitor to improve the noise factor and dynamic range. A sufficiently high dynamic range is obtained only if the inductor is capable to handling relatively high power signals with reduced distortion.

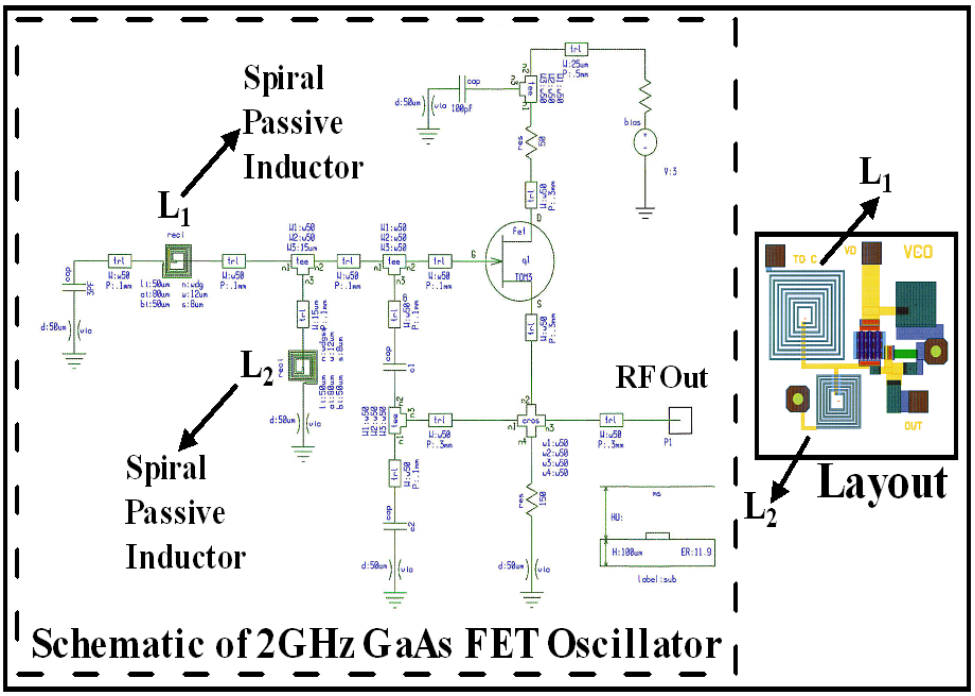
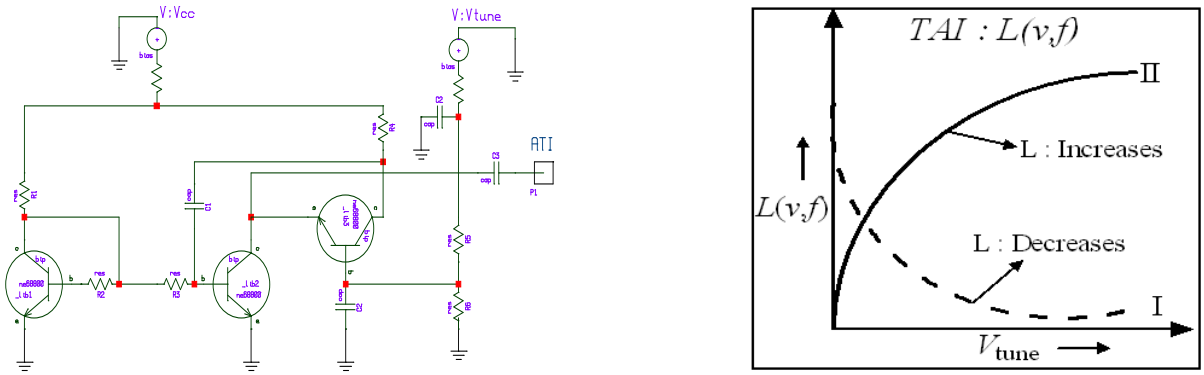


Figure 3-35 Schematic and layout of 2 GHz GaAs FET Oscillator



(a) Schematic of TAI

(b) Plot of L Versus V_{tune}

Figure 3-36 (a) Schematic of TAI and (b) plot of inductor (L) versus tuning voltage (V_{tune})

Most of the tunable inductors described in the literature use the bias point of some active device in the gyrator as the tuning parameter, with the device transconductance (g_m) as the tuned value. Since the variation of transconductance with respect to bias point is nonlinear under large-signal conditions, achieving good linearity in the oscillator is a next-to-impossible task.

For this work, a dynamic phase injection technique is proposed so that effective inductance value as well as the series resistance, changes with the applied control voltage without affecting the linearity, and can thus achieve high dynamic range.

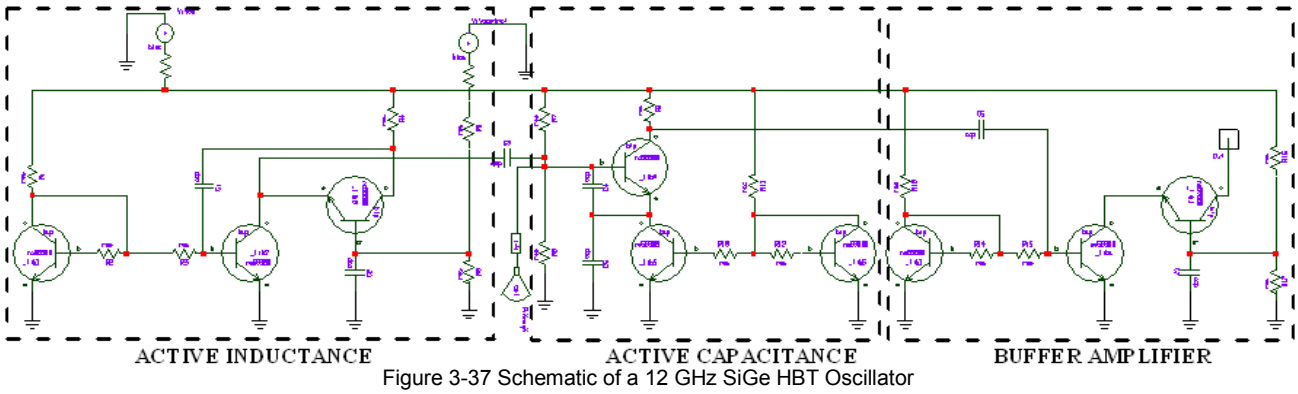


Figure 3-37 Schematic of a 12 GHz SiGe HBT Oscillator

3.4.3 Active Inductor Topology

The Dutch theorist B.D.H. Tellegen of Philips first explored the concept of TAIs and built it using gyrators. Figure 3-38 shows one such active inductor design based on a gyrator, realized by connecting inverting and non-inverting amplifier back-to-back in parallel.

Figure 3-40 shows the typical configuration of tunable active inductor; (a) grounded active inductor, (b) cascode grounded active inductor and (c) resistive feedback active inductor [48]-[55]. Such an "active inductor" can be useful in power dividers (Figure 3-39), quadrature couplers (Figure 3-41), and oscillators (Figure 3-42), provided the inductor can handle voltages similar to the passive inductor. The drawback of the conventional TAI topology in Figure 3-40 is low dynamic range and limited tunability. Therefore, the circuits in Figure 3-39, Figure 3-41, and Figure 3-42 have narrow band operation.

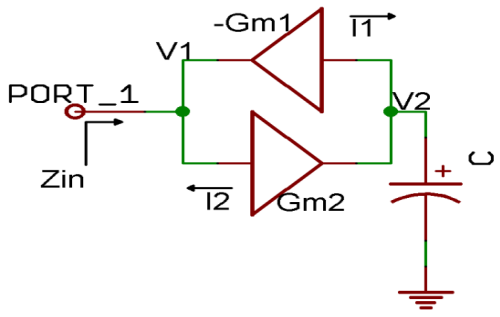


Figure 3-38 A typical gyrator based tunable active inductor

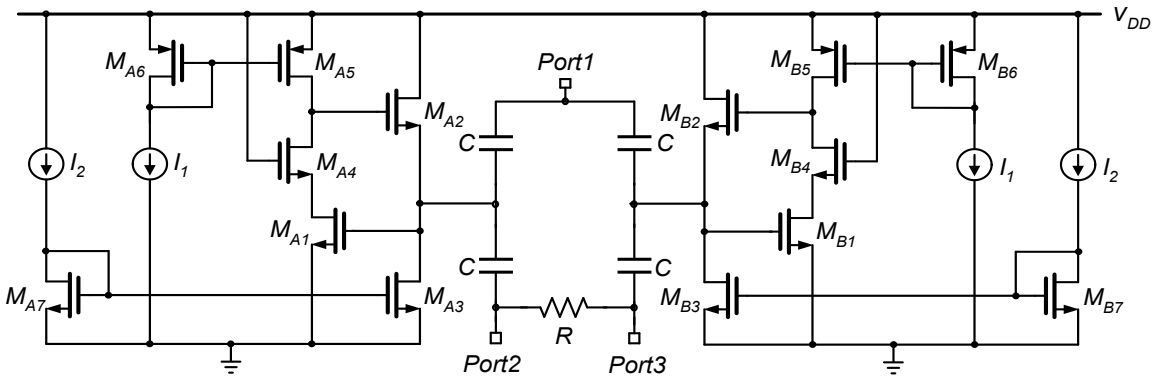


Figure 3-39 Typical Wilkinson power divider using TAI

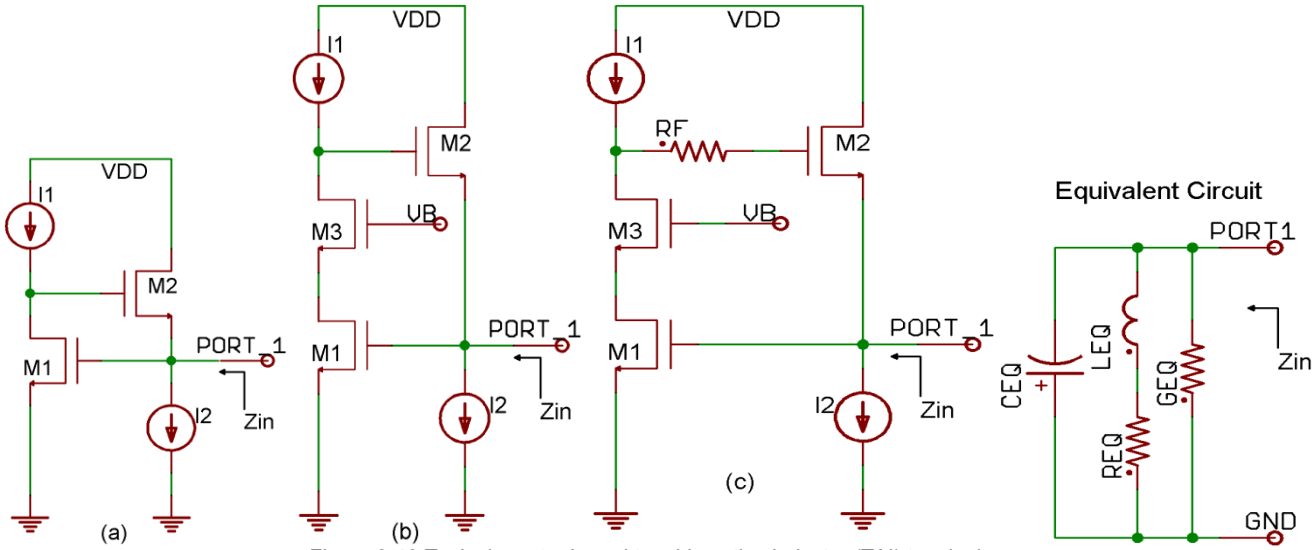


Figure 3-40 Typical gyrator based tunable active inductor (TAI) topologies

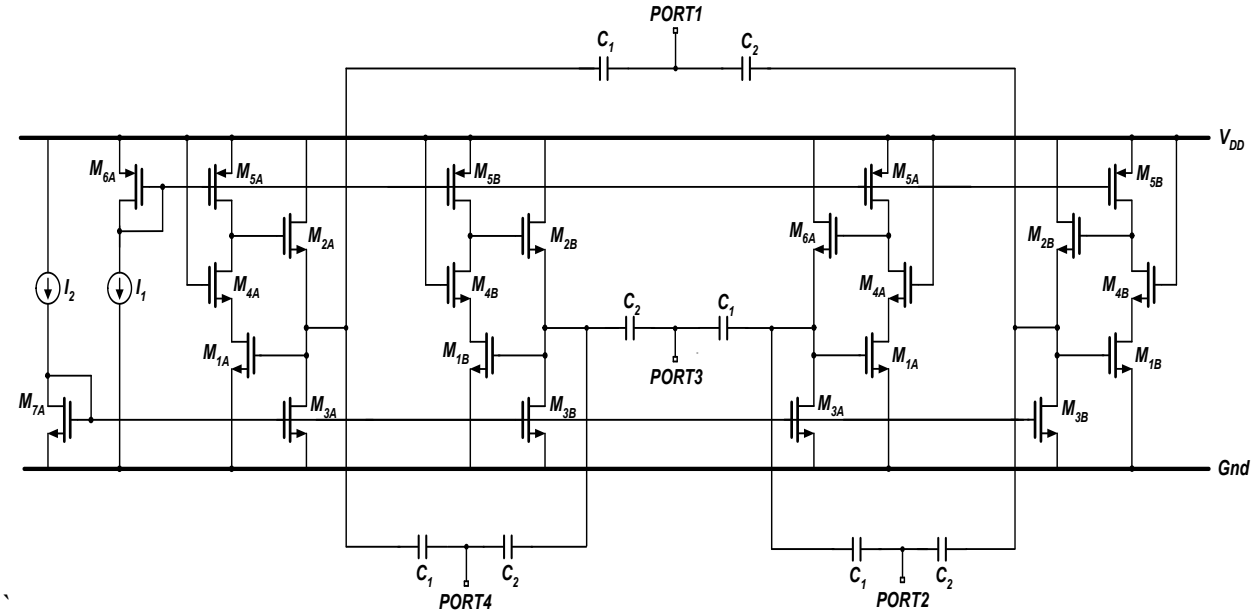


Figure 3-41 Typical schematic of quadrature coupler using TAI

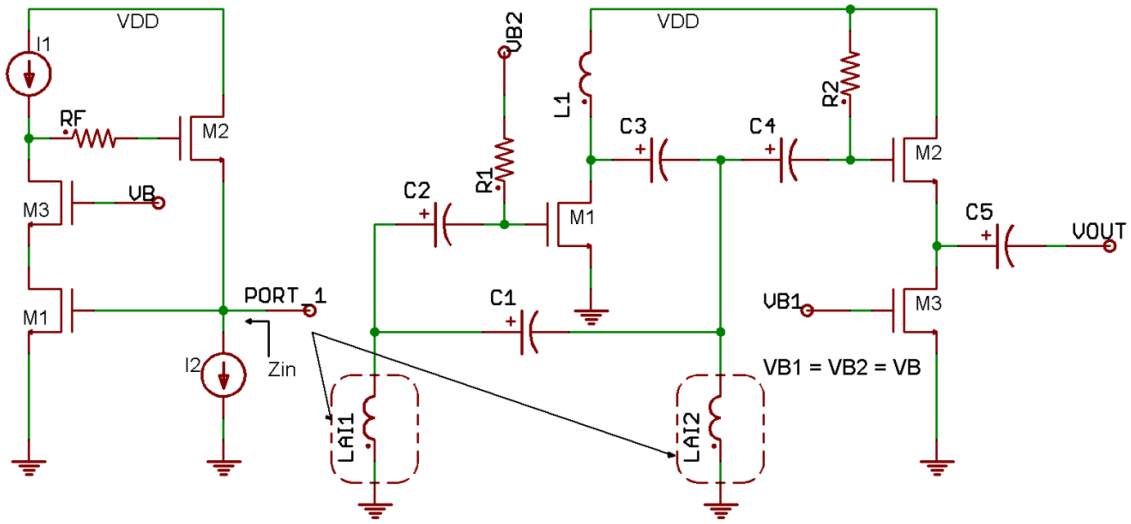


Figure 3-42 Schematic of CMOS oscillator using TAI

For oscillator applications, the tuning range is very critical. A typical gyrator (from Figure 3-38) with a phase compensating network converts capacitor C (v), into an inductance L (v), as a function of delay (φ) and control voltage (v) [48]. This modified TAI using a dynamic phase compensating network for broadband applications is shown in Figure 3-43.

$$L(v) \approx \frac{C(v)}{g_{m1} \times g_{m2}} \tag{3.12}$$

Figure 3-44a shows the TAI schematic using a phase compensating network (φ) and Figure 3-44b plots the complex impedance on the Smith-chart. Figure 3-44b reveals the inductive behavior of the circuit from 600MHz (#2) to 30GHz (#5). The real part of the input impedance is positive everywhere, therefore lossy and not a promising alternative. Encircling and crossing at 4.3GHz (#3) can be carefully avoided, which limits the applications.

3.4.4 Tunable Active Inductor Oscillator

Figure 3-45 shows the schematic and Figure 3-46 shows the phase noise plot of the 12GHz TAI VCO circuit.

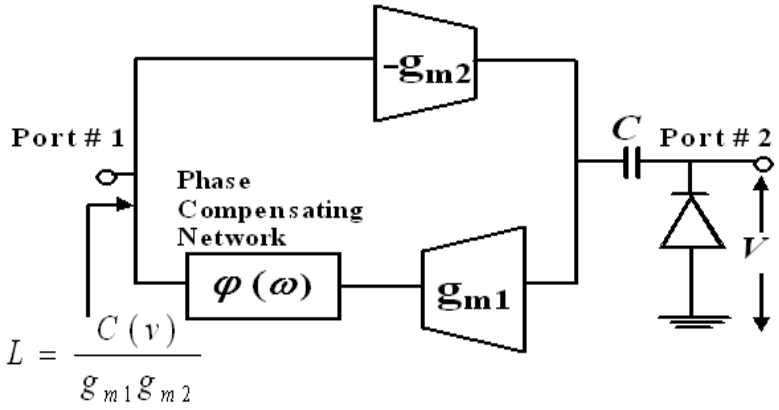


Figure 3-43 A typical TAI using phase compensating network

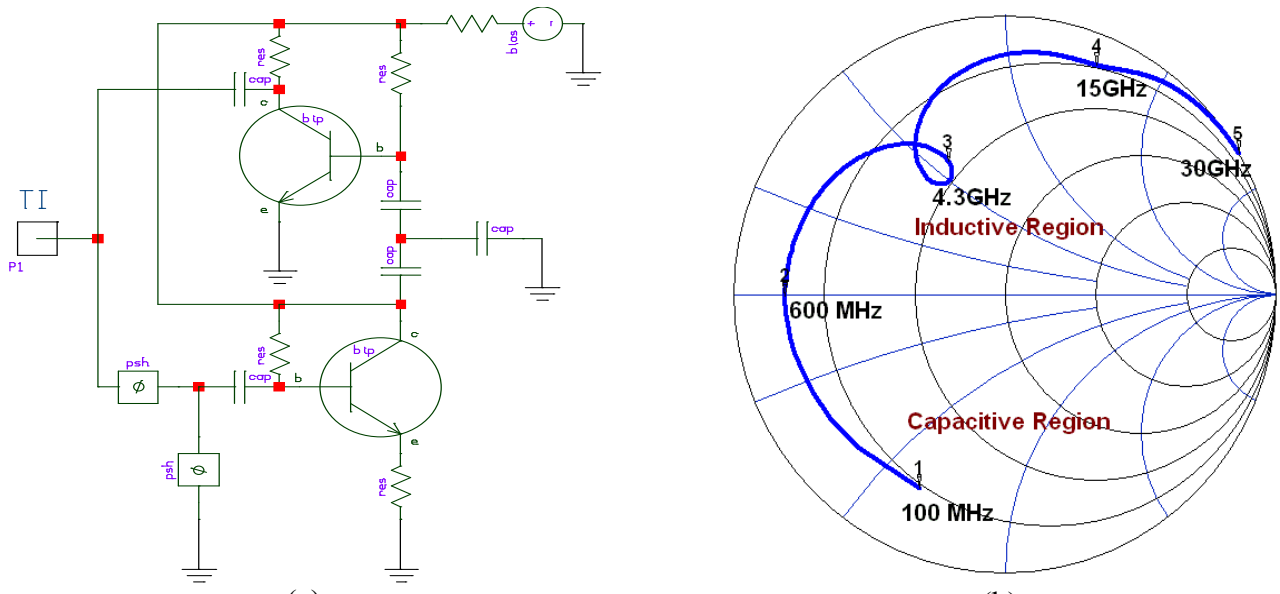


Figure 3-44 (a) Schematic of TAI and (b) impedance plot

As shown in Figure 3-46, phase noise at 1MHz offset from the carrier frequency 12GHz for the simple oscillator is -100dBc/Hz, which is inferior compared to commercially available varactor-tuned VCOs [56]. Several approaches considered to overcome the phase noise problem, including the minimization of the active device noise [48]-[56], result in power hungry and limited band characteristics. The negative resistance generated in series with the inductance is not constant across the operating frequencies. To verify the improvement in phase noise performance without affecting the dynamic range, a schematic was designed (Figure 3-45) with the dynamic phase injection technique, as discussed in Figure 3-43.

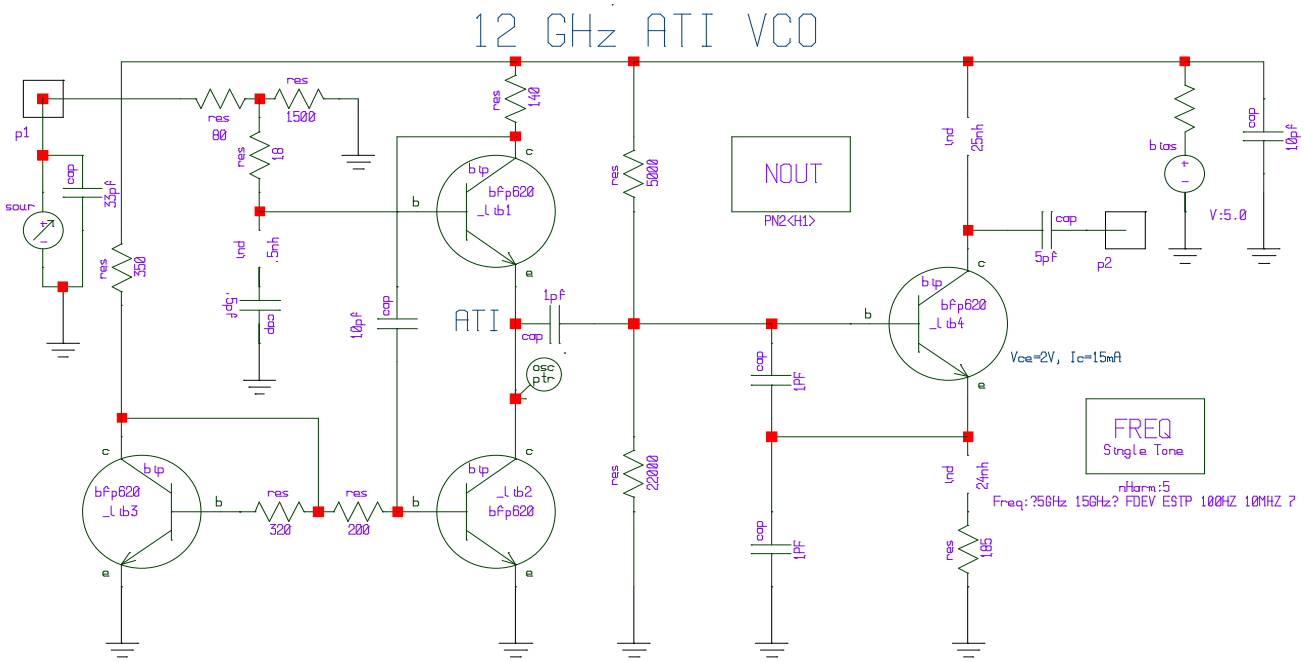


Figure 3-45 Schematic of 12GHz TAI VCO circuit

A novel 12GHz TAI VCO reported in this work replaces the varactor-tuned VCO, and the technology is compatible with existing IC processes. The state-of-the-art approach incorporates dynamic-phase-injection which minimizes the noise figure and current consumption resulting in low phase noise. The user has an option of trading phase noise with tuning range for a given power consumption. For further improvement in phase noise, of the schematic in Figure 3-45, an injection-locking technique was applied. The validation circuit of a injection locked 12GHz TAI using the dynamic phase injection technique in a VCO is fabricated on a Rogers substrate with a dielectric constant of 3.38 and a thickness of 30mils (microstrip line). Figure 3-47 shows the schematic and Figure 3-48 is the measured phase noise plot showing the predicted 10-15dB improvement as compared to the reported TAI VCO of Figure 3-45 [48]. The measured phase noise plot agrees with the simulated result within 3dB. A tuning range of 200MHz and bias of 3V, 12mA were achieved.

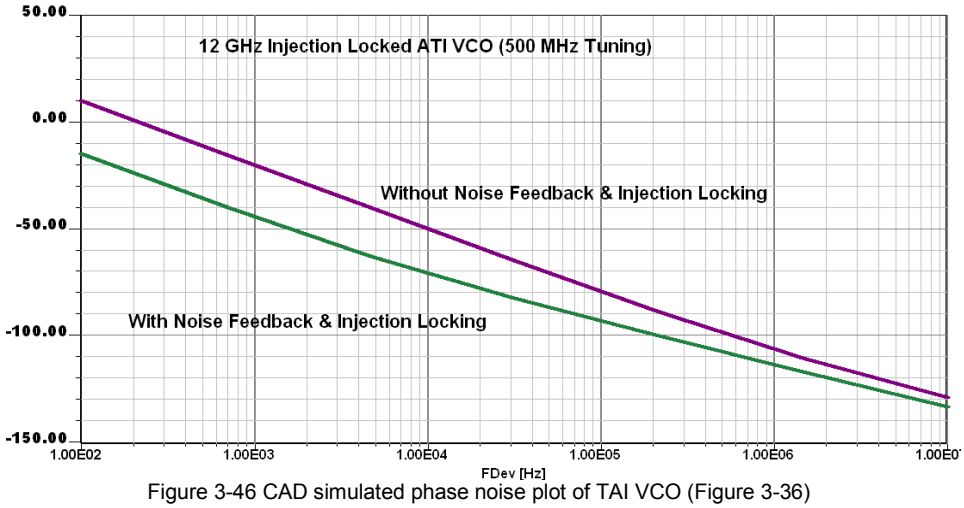


Figure 3-46 CAD simulated phase noise plot of TAI VCO (Figure 3-36)

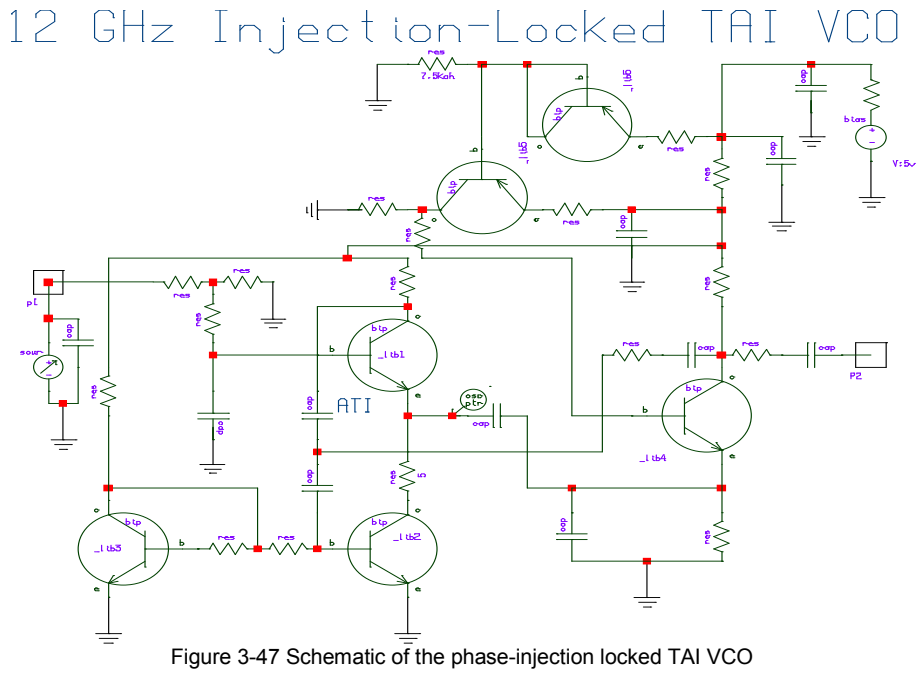


Figure 3-47 Schematic of the phase-injection locked TAI VCO

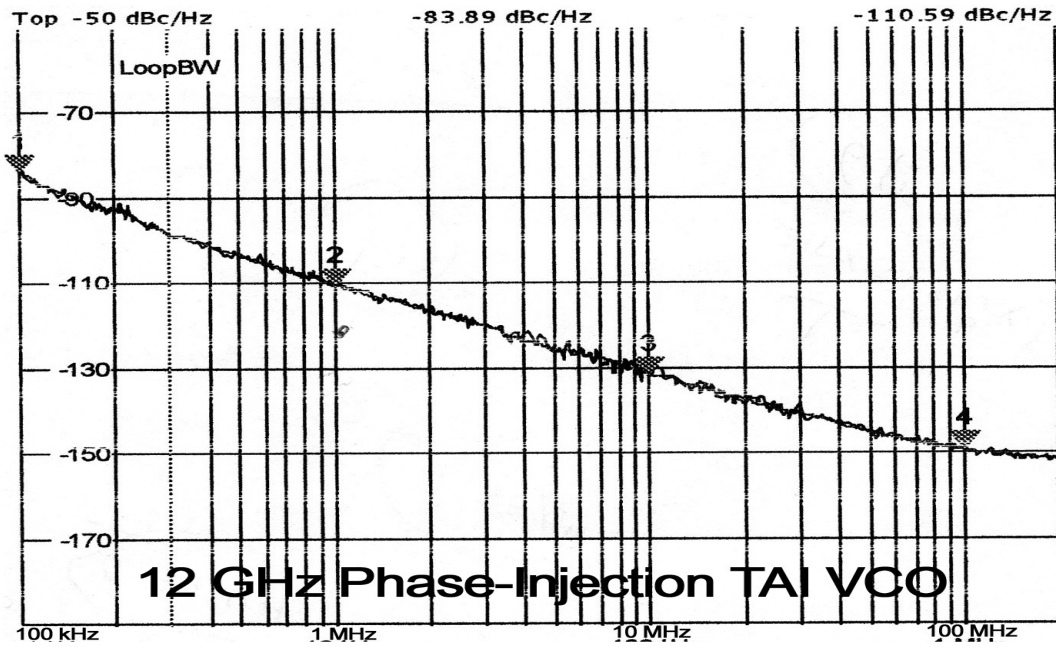


Figure 3-48 Measured phase noise plot of TAI VCO (Figure 3-47)

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4 Active Inductor Circuits

Cost and size minimization are key issues in modern portable radio systems. The integration of electronic parts has constantly grown to the point where the only discrete parts can be found in the RF front end. The most expensive discrete parts, in terms of both price and manufacturing costs, are spiral inductors. Much effort has been made to overcome this problem in the past few years by realizing the active inductor.

The total monolithic approach is the strength of active inductor technology. They can be embedded into fully integrated systems without any need to bring the RF signal out of the chip to a noisy and interfering environment. No on-chip passive inductors are necessary, which extends the range of applicable process technology. Potential future systems, to which these properties are a prerequisite and where noise and dynamic range specifications are relieved, will be prominent applications for active inductors. By incorporating noise-filtering and injection-mode coupling (Chapters-8 & 9), noise characteristics of the active inductor can be improved for applications in integrated RFIC/MMIC oscillators. This chapter provides typical topologies and performance characteristics of active inductors for applications in microwave oscillators and filter circuits.

4.1 Historical Perspective

B. D. H. Tellegen of Philips Research Laboratory proposed a new two-port network element in 1948, shown in Figure 4-1 [1]-[2]. Tellegen realized that all two-ports containing only resistors, capacitors, inductors and transformers are linear, constant, passive and reciprocal. In order to find a new fundamental element, he had to rule out one of these properties. He considered the last one, reciprocity, to be of least importance in the network theory, and suggested that a new non-reciprocal element, the gyrator, can be regarded as the fifth fundamental circuit element.
The ideal passive gyrator is described by [2]

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.1}$$

Where, the quantity g is called 'gyration conductance'.

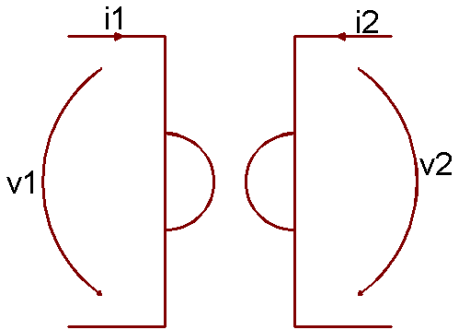


Figure 4-1 Symbol for the ideal gyrator as proposed by Tellegen [1]

Tellegen noticed that a capacitance connected to the secondary terminals would look like an inductor at the primary terminals $L = C/g^2$ or vice versa $C = g^2L$. This is the most important property of the gyrator, as it enables the synthesis of inductors. More generally, any admittance Y

connected to the secondary terminals is converted to its dual g^2/Y. This phenomenon is called immittance conversion [2]. The name gyrator originates from the gyroscopic terms that occur in the state equations of coupled rotating masses.

4.1.1 Passive Magnetic Gyrators

Figure 4-2 shows a typical construction of a passive magnetic gyrator where the medium between the electrodes of the primary terminal must consist of particles carrying both permanent electric and permanent magnetic dipoles [1]-[2]. Magnetic gyrators have also been realized by using the Hall Effect in a semiconductor, Faraday Effect in a ferrite, non-reciprocal properties of coupled-electric and magnetic transducers (the piezoelectric-piezomagnetic gyrator) [3]-[5]. It is clear that these kind of passive gyrators have little practical importance in oscillator design, and they should be regarded only as demonstrations of the gyrator effect [2]. However, ferromagnetic circulators are widely used as gyrators in microwave circuits.

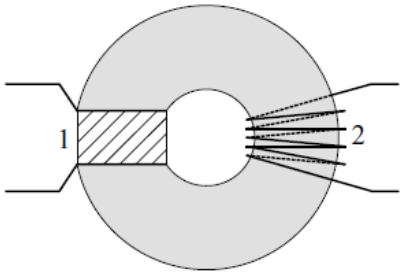


Figure 4-2 Construction of a passive gyrator [2]

4.1.2 Electronic Gyrators

When the two gyrator conductances, g, are equal, the gyrator is passive and non-dissipative. In general, this need not be the case, and the gyrator conductances can be unequal but still opposite in sign. Depending on their ratios, the gyrator is either active or dissipative. The conductance matrix can be split into two parts as [2]:

$$y = \begin{bmatrix} 0 & g_1 \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -g_2 & 0 \end{bmatrix} \tag{4.2}$$

The matrices in Equation (4.2) correspond to ideal voltage-controlled current sources, i.e. transconductors, with opposite signs, resulting in an ideal electronic gyrator [2]:

$$y = \begin{bmatrix} 0 & g_{m1} \\ -g_{m2} & 0 \end{bmatrix} \tag{4.3}$$

However, in practice, ideal electronic gyrators do not exist; therefore, it is imperative to consider the mechanisms causing imperfections and their effects. The matrix for practical gyrators can be described in Equation (4.4).

$$y = \begin{bmatrix} y_{p1} & g_{m1}e^{-j\emptyset_1} \\ -g_{m2}e^{-j\emptyset_2} & y_{p2} \end{bmatrix} \tag{4.4}$$

Figure 4-3 shows the schematic representation of ideal and non-ideal electronic gyrators. The complex gyration admittances $g_{m1}e^{-j\emptyset_1}$ and $g_{m2}e^{-j\emptyset_2}$ describe the phase shift in the transconductors. The non-zero diagonal elements y_{p1} and y_{p2} represent the parasitic admittances at the corresponding ports. They occur because of the finite output conductances in the transconductors. Imperfections due to an external biasing network will alter the port impedances and the affect on the gyrator performance, too.

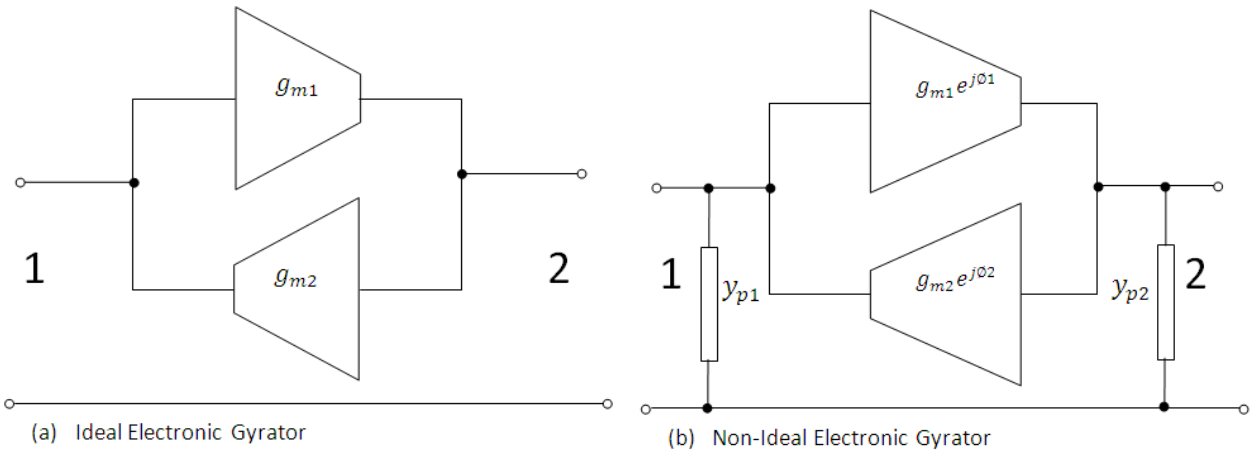


Figure 4-3 Representation of the Electronic Gyrator: (a) Ideal Electronic gyrator, (b) Non-Ideal Electronic Gyrator

For the realization of an active inductor, a capacitor is incorporated to either of the port in Figure 4-4, and the impedance seen from the other port can be transformed to an inductance according to the immittance conversion theorem. As shown in Figure 4-4, the active inductor is designed by using the gyrator-C topology to provide the inductance, where two amplifiers are connected back-to-back. This topology is capable of transforming the intrinsic capacitance from the amplifier to an inductive behavior. In this configuration, there are four main components, which are total transconductance of amplifier1, g_{m1}, transconductance of amplifier2, g_{m2}, parasitic capacitance of amplifier1, C_1 and parasitic capacitance of amplifier2, C_2. The inductance and the resonant frequency, f_r of the active inductor can be described by

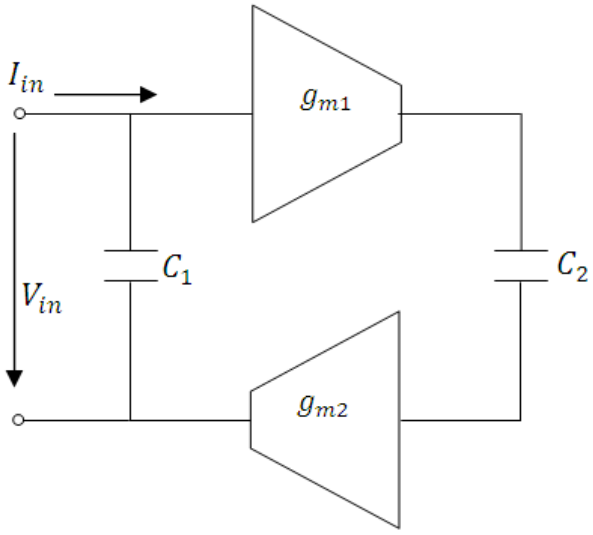


Figure 4-4 A typical Gyrator-C Topology

$$L = \frac{C_2}{g_{m1} g_{m2}} \tag{4.5}$$

$$f_r = \frac{g_{m1} g_{m2}}{C_2} \tag{4.6}$$

where $C2$ is the port capacitance, known as the gyrator capacitance.

From Equation (4.5) and Equation (4.6), we can tune the frequency and inductance value by tuning g_{m1} and g_{m2} rather than tuning $C2$ as its value is fixed by the length and width of the transistors. To increase the inductance value, we need to decrease the current as this will decrease g_{m1} and g_{m2}. Therefore, to have a smaller inductance value, a higher current is used to increase g_{m1} and g_{m2}. This will increase power consumption of the design if a small inductance value and higher resonant frequency are required.

Several electronic gyrators based on anti-parallel transconductors were presented but the concept really made advances during the following years, when transistors became readily available in the 1960's [6]-[10]. Figure 4-5 shows the typical gyrator from 1965 and the main objective at that time, as well as nowadays, was to replace the tuning diode and form tunable inductor-less resonators and filters [7]. As transistors were becoming inexpensive, it was predicted that they would replace the costly wound inductors in some sense or another in the future [2].

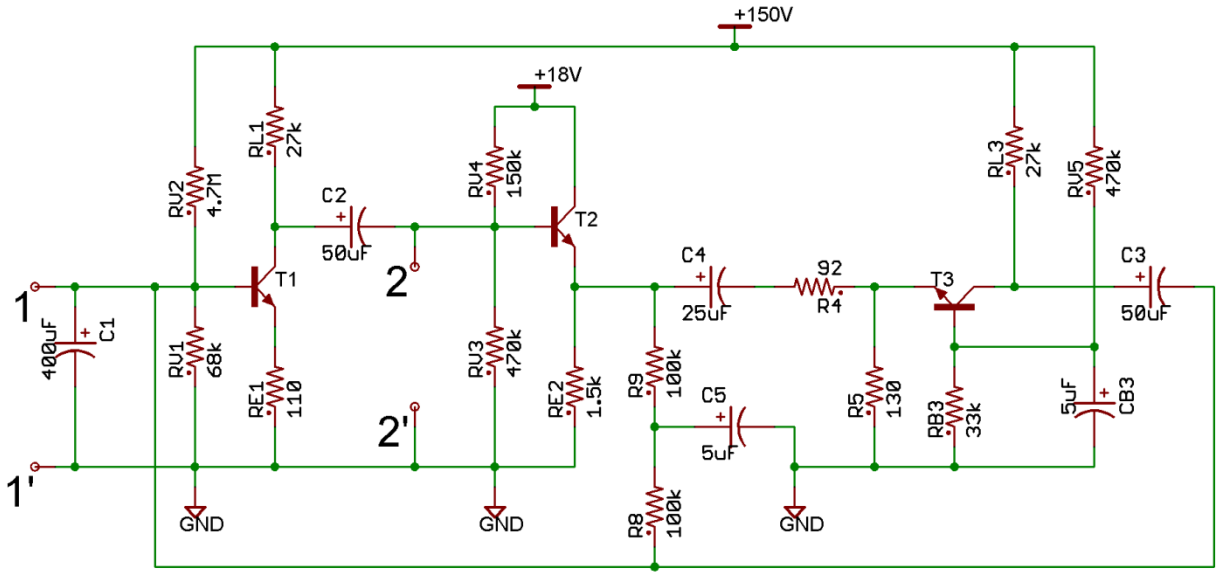


Figure 4-5 Typical gyrator topology from 1965 [7]

The first partially integrated gyrators began to show in the early 1970's along with the development of integrated operational amplifiers [11], [12]. In terms of integration the gyrator filter was soon made obsolete due to the rapid evolution in other active continuous-time and discrete-time filtering techniques. Only after high frequency integrated circuits and MMICs became a focus of research in the late 1980's, integrated microwave gyrators became potential circuit elements for active filtering [2].

4.1.3 Design Philosophy of Active Inductors

To understand the design philosophy, a simplified active inductor model can be used for brief insights about its implementation in the main circuit [13]-[14]. Figure 4-6 shows the equivalent representation of active inductor that can be modeled by using four passive components, *C, R, L* and *RL*. The synthesized inductor L is a function of loss resistance RL and package parasitic C and R, and can be described by

$$C = \frac{1}{2C_1} \tag{4.7}$$

$$R_L = \frac{2g_2}{g_{m1}g_{m2}} \tag{4.8}$$

$$R = \frac{g_1}{2} \tag{4.9}$$

where g_1 and g_2 are the output transconductances of g_{m1} and g_{m2} respectively.

From Equation (4.8), by lowering the g_2, Q-factor can be improved without increasing the current. This could be achieved by having a larger length of g_{m2}.

In general, there are four different active inductor topologies suitable for high Q resonator and filter applications [14].

(a) Basic active inductor
(b) Cascode active inductor
(c) Regulated cascode active inductor
(d) Differential active inductor

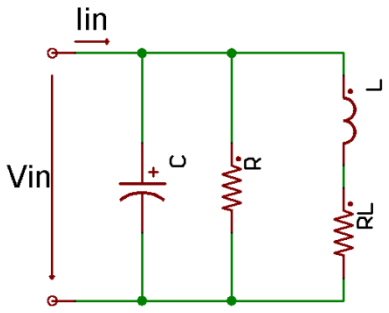


Figure 4-6 Active inductor Model [13]

4.1.3.1 Basic Active Inductor

By incorporating two back-to-back amplifiers, a simplified architecture of a basic active inductor can be realized. The simplest configuration of an amplifier can be characterized the transistor itself. Figure 4-7 shows the typical schematic of basic active inductor topology [15].

As shown in Figure 4-7, $M1$ and $M2$ are amplifier1 and amplifier2 respectively. The parasitic capacitance of both transistors will provide C_1 and C_2 to this circuit. However, this architecture has limited Q-factor values as the output transconductance at $V1$ is quite large.

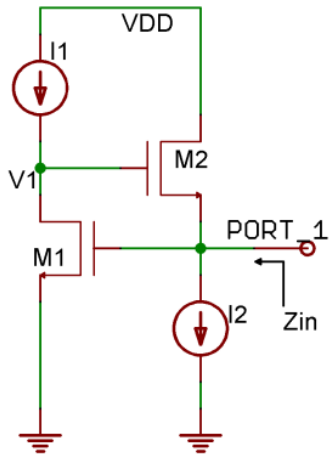


Figure 4-7 A typical schematic of basic active inductor [15]

4.1.3.2 Cascode Active Inductor

To improve the basic active inductor architecture, a cascode technique (transistor $M3$ is incorporated and biased by external V_{bias}) is employed to reduce the output transconductance at $V1$, including an increase in Q-factor [16]. Figure 4-8 shows the typical schematic of a cascode topology where we have reduced output transconductance at $V1$, but at the cost of reduction in operating frequency (introduction of $M3$ will limit the resonant frequency).

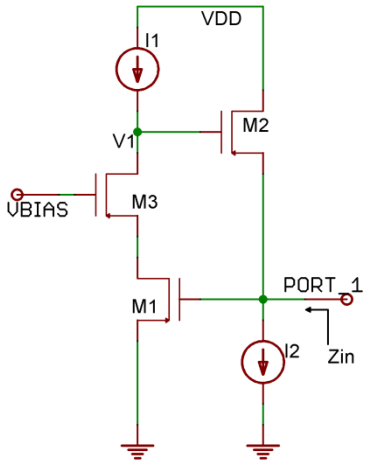


Figure 4-8 A typical schematic of cascode active inductor [16]

4.1.3.3 Regulated Cascode Active Inductor

To overcome the problems associated with the cascode active inductor topology shown in Figure 4-8, a regulated cascode architecture (transistor $M4$ and current source $I3$ are incorporated) was introduced in [13, 17]. As shown in Figure 4-9, inclusion of $M4$ increases the resonant frequency and the Q-factor (even though $M3$ is needed to control the output conductance, but the inclusion of $M4$ improves the Q-factor). In addition to this, the configuration does not need an external V_{bias} for $M3$ as it is provided by $V3$. The main drawback of this configuration is the

large power consumption due to the additional current source $I3$, resulting in degraded noise performance.

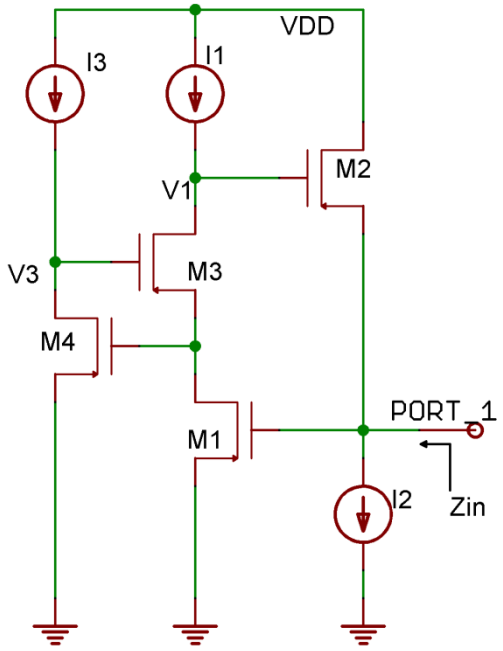


Figure 4-8 A typical schematic of regulated cascode active inductor topology [13], [17]

4.1.3.4 Differential Active Inductor

The active device (transistor) is a known noise generator. Therefore, the additional current source should be eliminated to strive for a noise-free circuit. This can improve the noise performance of the active inductor. To improve the performance of the cascode topology shown in Figure 4-8, a differential active inductor architecture (a differential architecture can improve noise performance by rejecting the common-mode noise) is introduced. Figure 4-9 shows the differential configuration that can offer large values of transconductance, resulting in smaller synthesized inductance values. As shown in Figure 4-9, two current sources, $I_{Q1} and\ I_{Q2}$ are incorporated to improve the Q-factor value by using $M3, M4, M7\ and\ M8$ to generate a negative resistance [15], [18]. Moreover, these current sources (I_{Q1} and I_{Q2}) can be used to tune the Q-factor value and enable user-defined inductance and Q-factor tuning and thereby broadband tunability. However, this configuration requires more DC power since the active inductor is tuned by current.

Figure 4-10 shows the modified differential active inductor topology by removing current sources I_{Q1} and I_{Q2}. This leads to current saving without compromising the Q-factor tunability. Care must be taken towards maximizing Q-factor by reducing the *Rout* value. To achieve this, the length of $M11, M12, M13\ and\ M14$ must be reduced to smaller values.

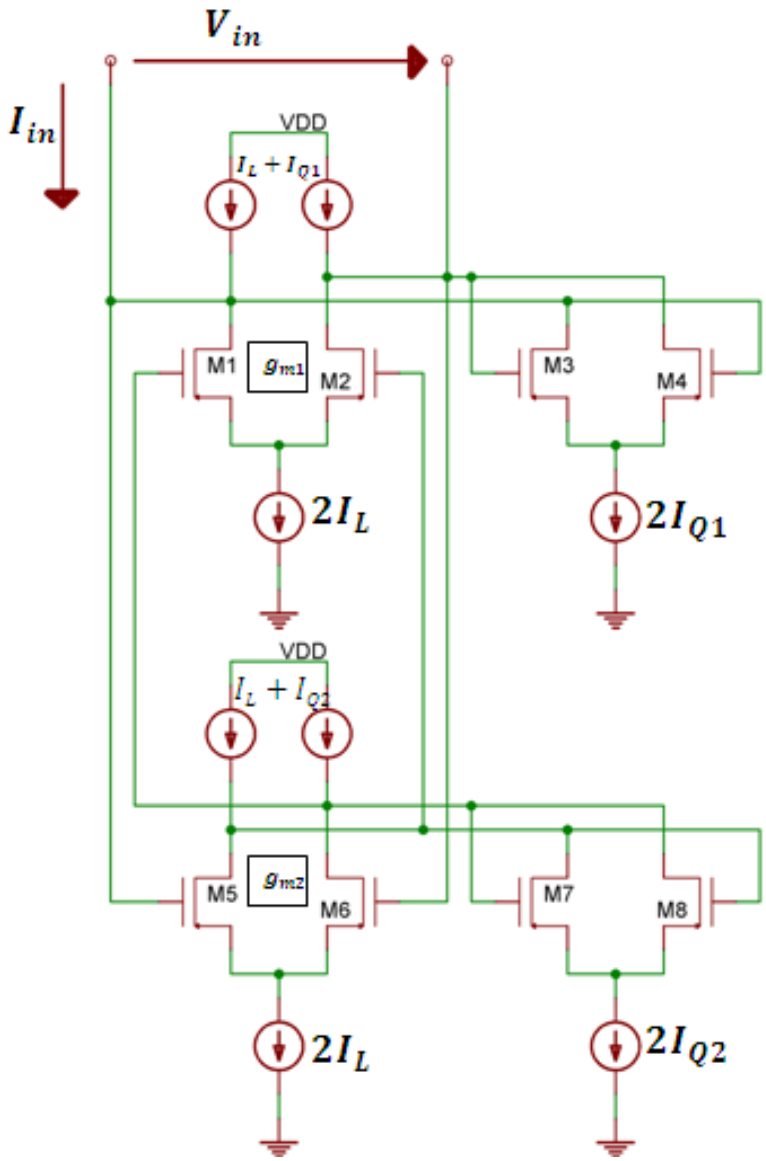


Figure 4-9 A typical circuit schematic of differential active inductor [15], [18]

In Figure 4-10, $M5, M6, M7, M8\ and\ M9$ represent the current source I_L of Figure 4-9. The inductance value can be tuned by providing current through Ix. Vx also needs a DC voltage for biasing $M9$. After removing I_{Q1} and I_{Q2}, $M11, M12, M13\ and\ M14$ also need to be biased. This is the reason why $M10$ is introduced by sharing the same current source with Ix. As a result, the inductance and Q-factor values are controlled only by *IX*. Even though the free-tuning capability on Q-factor is lost by removing I_{Q1} and I_{Q2}, Ix can be used to control Q-factor value. However, as Ix plays a major role to tune the inductance value Ix only has a small effect on Q-factor value.

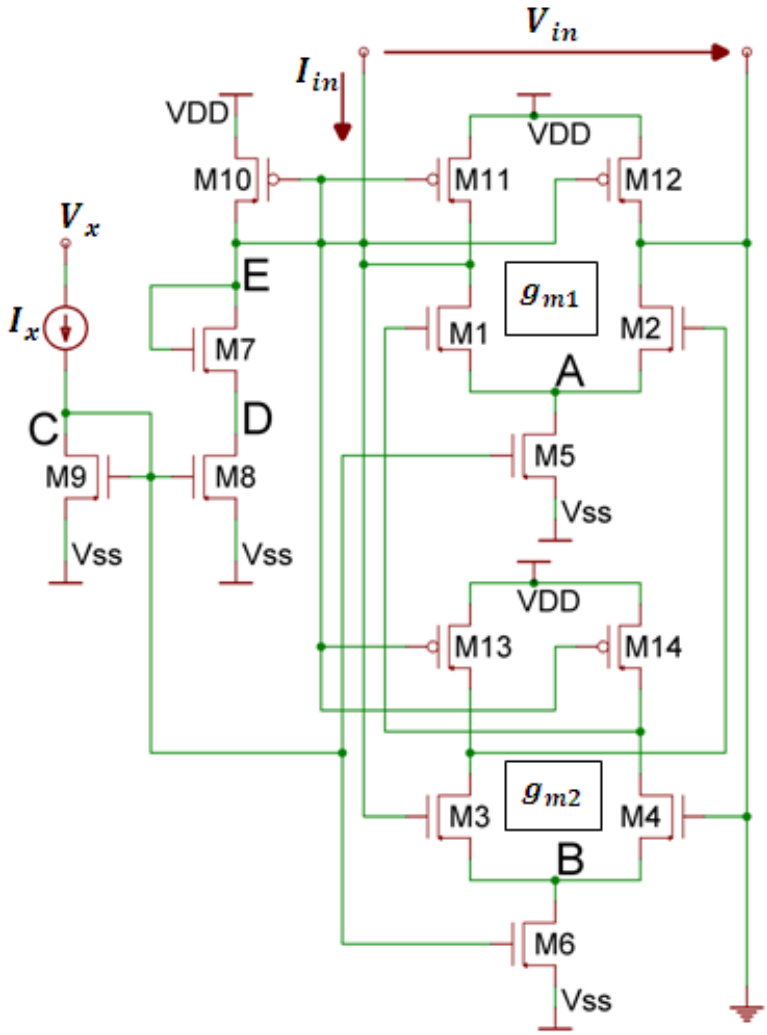


Figure 4-10 A typical circuit schematic of the modified differential active inductor [15]

4.2 Active Inductor Noise

Noise is a very critical issue in synthesized active inductor circuits based on gyrator configurations. Intrinsically, the gyration conductances responsible for synthesized inductors generate minimum noise independent of the electronic circuitry associated with tunable oscillators [10]-[11]. For the realization of active resonators using synthesized inductor networks, capacitors are needed at each port of a gyrator that forms an active inductor network. Therefore, intrinsic noise sources associated with the capacitor loaded gyrator network remain the same, and the equivalent circuit can be represented in Figure 4-11 [2]. To simplify the analysis, the noise voltage sources at the inputs of the transconductors could be transferred into current sources at the outputs (Figure 4-12).

As shown in Figure 4-11 and Figure 4-12, the noise voltage source $\hat{v}_{n,1}^2$ from transconductances $g_{m1,2}$ can be expressed as a series voltage source in conjunction with the simulated inductance L, whereas, $\hat{\imath}_{n,2}^2$ forms a parallel current source for the resonating capacitor C. Therefore, the synthesized active resonator susceptance is noisier than the equivalent passive LC resonator

where the equivalent loss resistance generates noise with identical parameters [20]. It can be concluded that the total noise of an active inductor resonator must be higher than that of a passive resonator with identical parameters unless the effective noise of the synthesized inductor is compensated by noise filtering and mode-injection. This will be discussed in chapter 7.

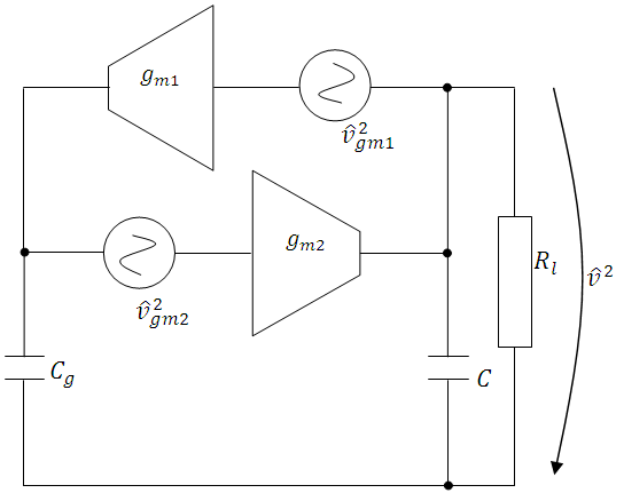


Figure 4-11 Capacitor loaded gyrator based active inductor resonator with noise sources [2]

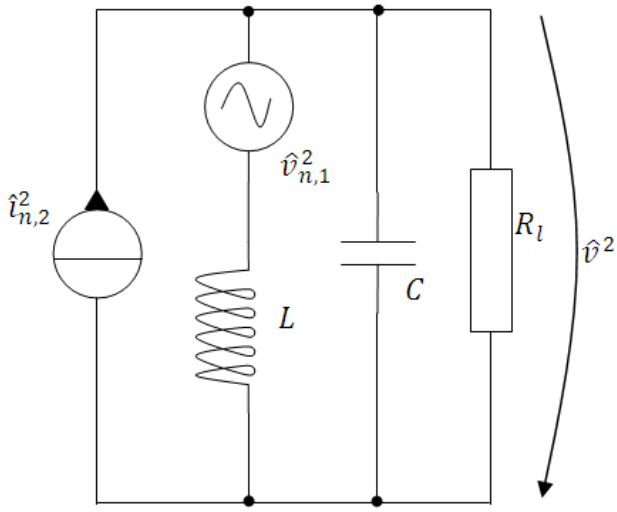


Figure 4-12 A simplified circuit of active inductor resonator with noise sources [2]

From Figure 4-12, the equivalent noise sources can be described by

$$\hat{v}^2_{n,1} = \hat{v}^2_{g_{m1}} \cong \frac{4kT\lambda}{g_m}, \quad \hat{\imath}^2_{n,2} = \hat{g}^2_{g_{m2}}\hat{v}^2_{g_{m2}} = 4kT\lambda g_m \tag{4.10}$$

where $v_{g_{m1}}$ and $v_{g_{m2}}$ are equivalent input noise voltages associated with the transconductances of the gyrator that forms the active inductor circuit, and $\lambda = 0.5\ (Bipolar),\ \lambda = 0.67\ (JFET)\ and\ \lambda = 0.12\ (MESFET)$.

4.2.1 Relative Noise Resistance and Conductance

The noise dynamics of active negative resistors can be formulated as passive resistors (positive resistor) where the equivalent noise voltage and noise current spectral densities are given by [2]

$$\hat{v}^2_n \cong 4kTr_n|R|, \quad \hat{\imath}^2_n \cong 4kTg_n|G| \tag{4.11}$$

where R and G are the negative resistance and conductance values, and the coefficients $r_n\ and\ g_n$ are frequency dependent relative noise resistance and conductance (these give a comparative value of how much noise the active negative resistor produces compared to a passive resistor of the same value).

The total noise voltage spectral density of the synthesized active resonator can be given by [2]

$$\hat{v}^2 = \frac{\hat{v}^2_{g_{m1}} + \hat{v}^2_{g_{m2}} g^2_{m2}\omega^2L^2}{\omega^2L^2G_l^2 + (\omega^2LC-1)^2} \Longrightarrow \hat{v}^2|_{\omega\to\omega_0} = Q_l^2\left(\hat{v}^2_{g_{m1}} + g^2_{m2}\hat{v}^2_{g_{m2}}\omega^2L^2\right) = 4kT\lambda Q_l^2\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{\omega_0^2C^2}\right) \approx \frac{4kT\lambda Q_l^2}{g_{m1}}\left(1 + \frac{C_g}{C}\right) \tag{4.12}$$

Where $Q_l = \frac{\omega L}{R_l} = \omega L G_l$ and $\omega_o = \frac{1}{\sqrt{LC}}$

From Equation (4.11) and Equation (4.12), the active inductor resonator noise can be compared to that of negative resistor resonators.

From Equation (4.12), the effective noise resistance *R* can be associated with that of the passive inductor $R = R_s(1 + r_n, g_n)$ in a negative resistance resonator. Therefore, it is possible to define 'the effective unloaded noise quality factor' for an active inductor. This shows what would be the magnitude of Q_0 in the passive inductor inducing the same amount of noise as an active inductor [2]:

$$Q_{0,noise} = \frac{\omega_0(1+r_n,g_n)}{\lambda g_{m2}\left(\frac{1}{C}+\frac{1}{C_g}\right)} \tag{4.13}$$

Equation (4.13), with realistic parameters shows that $Q_{0,noise}$ is very low. The noise calculations are idealized and do not account for additional critical parameters but give a suitable basis for comparisons. It is reasonable to draw the conclusion that active inductor resonators are inferior to negative resistor resonators in terms of noise performance.

From Equation (4.12), the effective noise can be lowered by minimizing g_{m2} and maximizing g_{m1}. But due to practical limitations, these parameters cannot be optimized unconditionally. The total RMS noise of an active inductor resonator can be determined by [19]-[21], as below.

$$\overline{v^2} = \int_0^\infty \hat{v}^2 df = \frac{\hat{v}_{gm1}^2}{2\pi}\omega_o \int_0^\infty \frac{d\omega}{[(\omega^2 LC-1)^2 + \omega^2 L^2 G_l^2]} + \frac{\hat{g}_{gm2}^2 \hat{v}_{gm2}^2}{2\pi}\int_0^\infty \frac{\omega^2 L^2 d\omega}{[(\omega^2 LC-1)^2 + \omega^2 L^2 G_l^2]} \tag{4.14}$$

$$\overline{v^2} \approx \frac{kT\lambda}{C} Q_l \left(\frac{g_{m2}}{g_{m1}}\right)^{1/2}\left[\left(\frac{C_g}{C}\right)^{1/2} + \left(\frac{C}{C_g}\right)^{1/2}\right] = \frac{kT\lambda}{C} Q_l \frac{\omega_O}{g_{m1}}(C + C_g) \tag{4.15}$$

$$\overline{v^2}\Big|_{g_{m1}=g_{m2}, C_g=C} \approx \frac{2kT\lambda}{C} Q_l \tag{4.16}$$

4.3 Classification of Gyrator based Active Inductors

Active inductors are commonly implemented based on gyrator architecture consisting of two transistors connected in a feedback configuration to generate an inductive impedance. A typical gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, the network is called the gyrator-C network, and can be categorized as one of the following [22]:

- Lossless Single-Ended Gyrator-C Active Inductors
- Lossy Single-Ended Gyrator-C Active Inductors
- Lossless Floating Gyrator-C Active Inductors
- Lossy Floating Gyrator-C Active Inductors

Figure 4-13, Figure 4-14, Figure 4-15, and Figure 4-16 show the common Gyrator-C active inductor topologies. The performance characteristics of these topologies trade each other depending upon the operating frequency, dynamic range, tuning range, noise and power consumptions.

Consider the lossless gyrator-C network shown in Figure 4-13. The admittance at port 2 of the gyrator-C network, given by its Laplace transform is,

$$Y(s) = \frac{I_{in}(S)}{V_2(s)} = \frac{1}{s\left(\frac{C}{g_{m1}g_{m2}}\right)} \tag{4.17}$$

Equation (4.17) indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with its inductance given by

$$L = \frac{C}{g_{m1}g_{m2}} \tag{4.18}$$

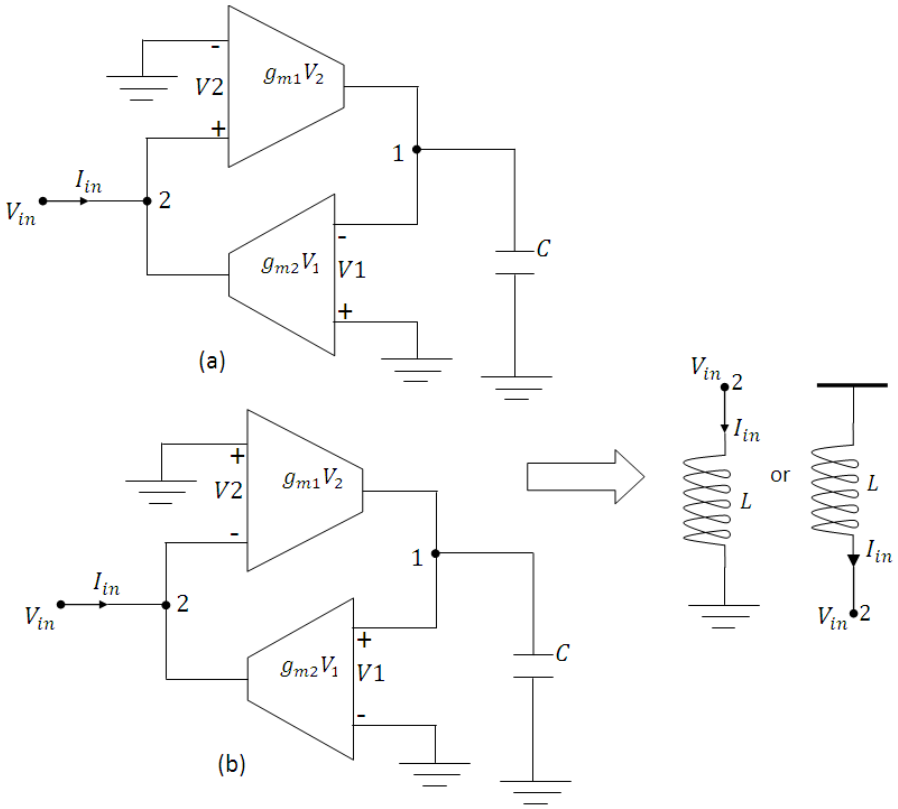


Figure 4-13 A Lossless single-ended gyrator-C active inductor topologies. g_{m1} and g_{m2} are the transconductances of transconductors 1 and 2, respectively, and C is the load capacitance at node 1. (a) Transconductor in the forward path has a positive transconductance while the transconductor in the feedback path has a negative transconductance; (b) Transconductor in the forward path has a negative transconductance while the transconductor in the feedback path has a positive transconductance.

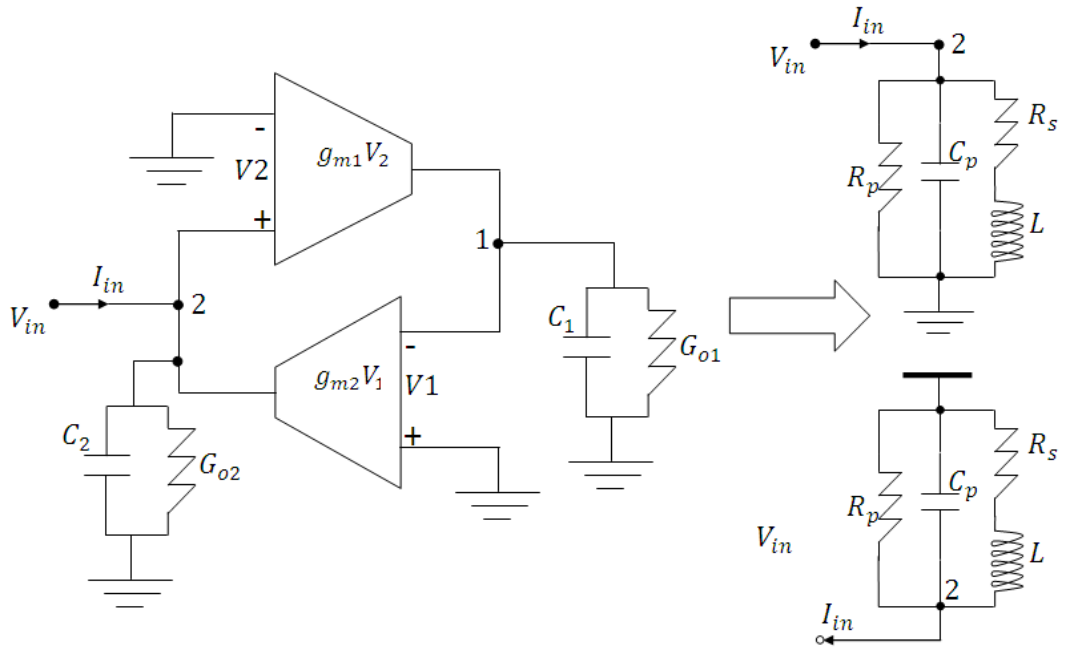


Figure 4-14 A lossy single-ended gyrator-C active inductor (C_1 *and* G_{o1}, C_2 *and* G_{o2} denote the total capacitance and conductance at nodes 1 and 2, respectively).

The admittance at port 2 of the lossy gyrator-C network shown in Figure 4-14 obtained from its Laplace transform is

$$Y(s) = \frac{I_{in}(s)}{V_2(s)} = (sC_2 + G_{o2}) + \left[\frac{1}{s\left(\frac{C_1}{g_{m2}g_{m1}}\right)+\left(\frac{G_{o1}}{g_{m2}g_{m1}}\right)}\right] \tag{4.19}$$

Equation (4.19) can be represented by the RLC network shown in Figure 4-14 with its parameters given as

$$R_p = \frac{1}{G_{o2}} \tag{4.20}$$

$$C_p = C_2 \tag{4.21}$$

$$R_s = \frac{G_{o1}}{g_{m1}g_{m2}} \tag{4.22}$$

$$L = \frac{C_1}{g_{m1}g_{m2}} \tag{4.23}$$

The self-resonant frequency (ω_0) of the RLC networks of the active inductor is given by

$$\omega_0 = \frac{1}{\sqrt{LC_p}} = \sqrt{\frac{g_{m2}g_{m1}}{C_2C_1}} = \sqrt{\omega_1\omega_2} \tag{4.24}$$

Where

$$\omega_{1,2} = \frac{g_{m1,2}}{C_{1,2}} \tag{4.25}$$

$\omega_{1,2}$ is the cut-off frequency of the transconductor 1 and 2 respectively while ω_0 is the self-resonant frequency of the lossy gyrator-C active inductor. This self-resonant frequency is typically the maximum frequency at which the active inductor operates.

Lossless floating gyrator-C active inductors offer the following attractive advantages over their single-ended counterparts:

(i) The differential configuration of the transconductors effectively rejects the common-mode disturbances of the network, making them particularly attractive for

applications where both analog and digital circuits are fabricated on the same substrate.

(ii) The level of the voltage swing of floating active inductors is twice that of the corresponding single-ended active inductors.

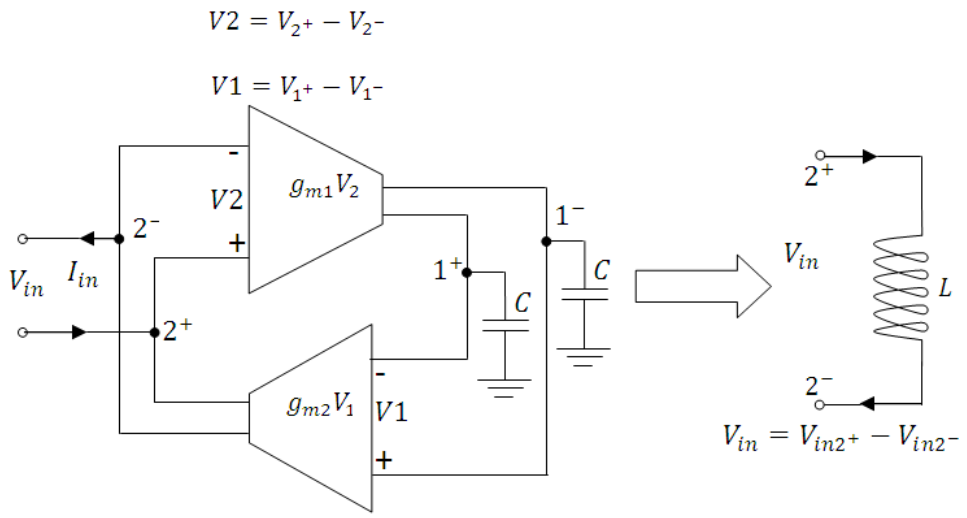


Figure 4-15 A lossless floating Gyrator-C active inductor topology (C_1 and G_{o1}, C_2 and G_{o2} denote the total capacitances and conductance at nodes 1 and 2, respectively).

The admittance at port 2 of the lossless floating gyrator-C network shown in Figure 4-15 from its Laplace transform is given by

$$Y(s) = \frac{I_{in}(s)}{V_{in2^+}(s) - V_{in2^-}(s)} = \frac{1/2sC}{g_{m1}g_{m2}} \tag{4.26}$$

Equation (4.26) reveals port 2 of the gyrator-C network behaves as a floating inductor with its inductance given by

$$L = \frac{2C}{g_{m1}g_{m2}} \tag{4.27}$$

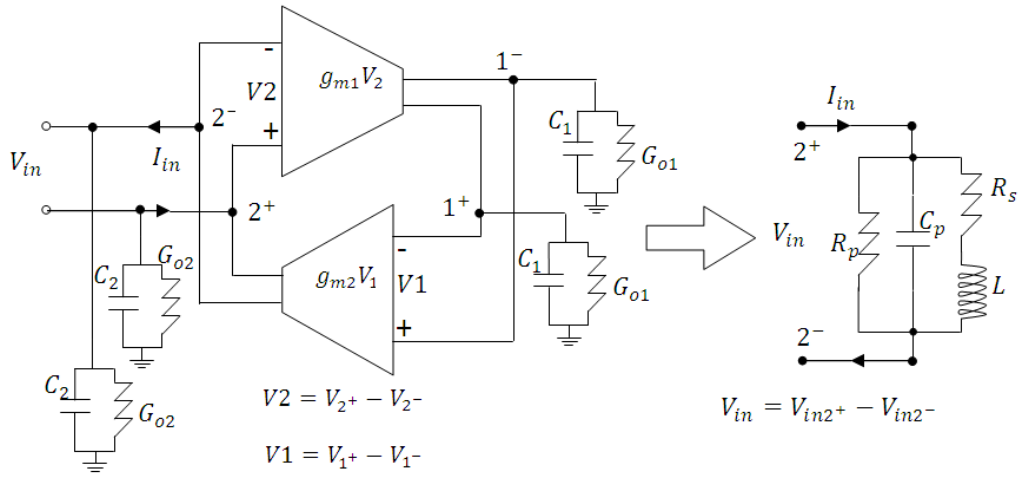


Figure 4-16 A lossy floating Gyrator-C active inductor topology (C_1 and G_{o1}, C_2 and G_{o2} denote the total capacitance and conductance at nodes 1 and 2, respectively).

The admittance at port 2 of the lossy floating gyrator-C network shown in Figure 4-16 is obtained using the Laplace transform as

$$Y(s) = \frac{I_{in}(s)}{V_{2+}(s) - V_{2-}(s)} = \left(\frac{sC_2 + G_{o2}}{2}\right) + \left[\frac{1}{s\left(\frac{C_1}{2g_{m2}g_{m1}}\right) + \left(\frac{G_{o1}}{2g_{m2}g_{m1}}\right)}\right] \tag{4.28}$$

Equation (4.28) can be represented by the RLC network shown in Figure 4-16 with its parameters given as below:

$$R_p = \frac{2}{G_{o2}} \tag{4.29}$$

$$C_p = \frac{C_2}{2} \tag{4.30}$$

$$R_s = \frac{G_{o1}}{2g_{m1}g_{m2}} \tag{4.31}$$

$$L = \frac{C_1}{2g_{m1}g_{m2}} \tag{4.32}$$

4.3.1 Characterization of Active Inductors

The performance of the active inductor typically depends on following [22]:

- Frequency range
- Inductance tunability
- Quality factor
- Noise
- Linearity
- Stability
- Supply voltage sensitivity
- Parameter sensitivity
- Signal sensitivity
- Power consumption

4.3.1.1 Frequency Range

A lossy active inductor shows an inductive characteristic only over a limited frequency range. Figure 4-17 exhibits the Matlab generated Bode plot that describes the frequency range of the lossy active inductor topology. This frequency range is obtained, from the impedance of the RLC equivalent circuit of the lossy active inductor, given as

$$Z(s) = \left(\frac{R_s}{C_p L}\right)\left[\frac{\left(\frac{sL}{R_s} + 1\right)}{s^2 + s\left(\left(\frac{1}{R_p C_p}\right) + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}}\right] \tag{4.33}$$

When a complex conjugate pole occurs, the pole resonant frequency of the impedance in Equation (4.33) is given by

$$\omega_p = \sqrt{\frac{(R_p + R_s)}{R_p C_p L}} \tag{4.34}$$

Typically, $R_p \gg R_s$, and Equation (4.34) simplifies to

$$\omega_p \approx \sqrt{\frac{1}{C_p L}} = \omega_0 \tag{4.35}$$

Where ω_0 is the self-resonant frequency of the active inductor. The impedance in Equation (4.33) also shows a zero frequency, hence the zero resonant frequency will be termed as

$$\omega_Z = \frac{R_S}{L} = \frac{G_{o1}}{C_1} \tag{4.36}$$

It is evident from Figure 4-17 that the gyrator-C network is resistive when $\omega < \omega_Z$, inductive when $\omega_Z < \omega < \omega_0$, and capacitive when $\omega > \omega_0$. The frequency range in which the gyrator-C network is inductive is lower-bounded by ω_Z and upper-bounded by ω_0. R_p has no effect on the frequency range of the active inductor.

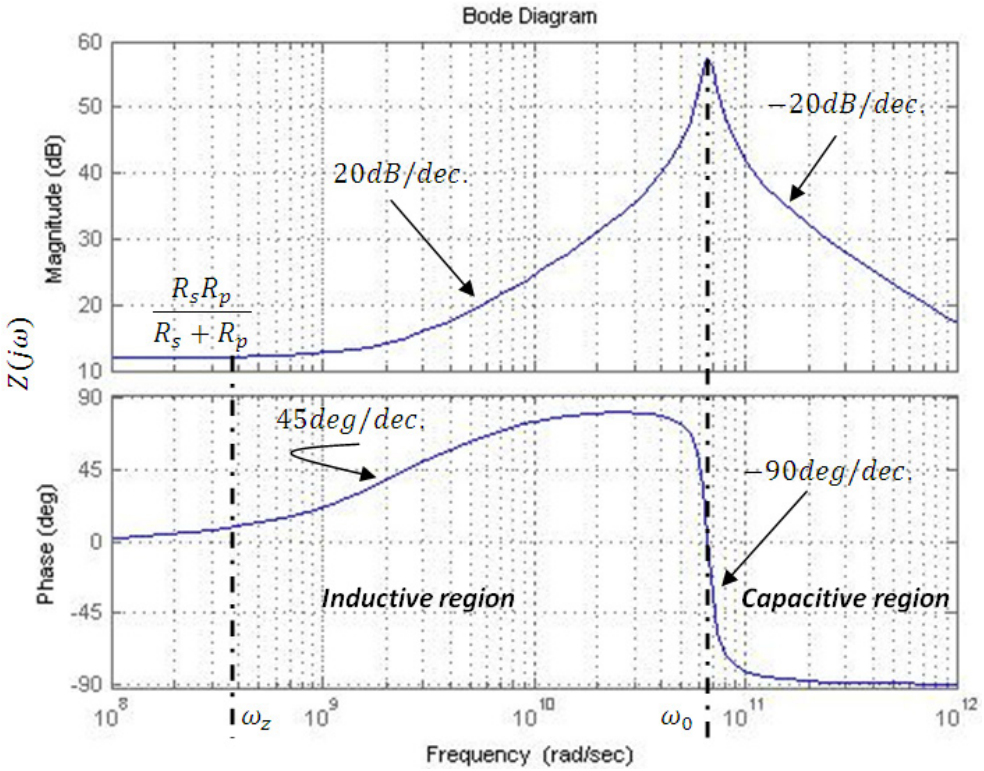


Figure 4-17 Matlab generated Bode plot describing the frequency range of the lossy active inductor topology.

4.3.1.2 Inductance Tunability

Motivated by the growing market of low cost tunable resonator solutions, much effort has been devoted characterize of the tunable inductor topologies for successful implementation as a tuning element in VCOs and filter circuits. Many applications, such as filters, voltage or current controlled oscillators, and phase-locked loops, require the inductance of active inductors to be tunable with a large inductance tuning range. Figure 4-18 shows the typical tuning mechanism of active inductor circuits.

Capacitance tuning in standard CMOS technologies is usually done by using varactors. Two types of varactors exist, namely pn-junction varactors and MOS varactors. A common drawback of junction varactors and MOS varactors is their small capacitance tuning range.

Conductance tuning can be done by varying the dc operating point of the transconductors. This approach offers a large conductance tuning range and subsequently a large inductance tuning range. The constraint of the conductance tuning range is set by the transconductance of the transconductor transistor that has to remain in saturation. Conductance tuning can be used for the

coarse tuning of the inductance while capacitance tuning can be used for the fine tuning of the inductance, as shown in Figure 4-18.

Changing the transconductance does not affect the R_p and C_p of gyrator-C active inductors but alters the parasitic series resistance R_s of the active inductor thereby causing a change in quality factor. This variation of Q due to tuning of L must be compensated such that L and Q are tuned in a truly independent fashion. It is also noted that fine-tuning the inductance using capacitance tuning does not affect R_s.

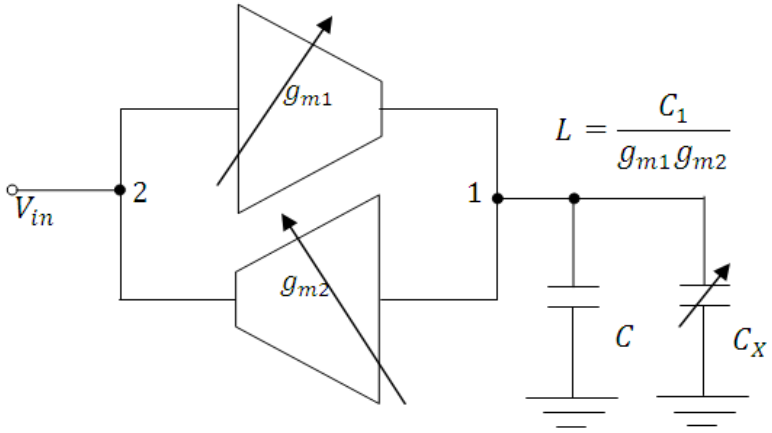


Figure 4-18 Shows the tunability features of active inductor

4.3.1.3 Quality Factor

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle [22]-[24]. For spiral inductors, the quality factor of these inductors is independent of the voltage or current of the inductors. These properties, however, do not hold for active inductors as the inductance depends upon the transconductances and the load capacitance. When active inductors are used in applications such as LC oscillators, the inductance is a strong function of the swing of the voltage and current of the oscillators. To quantify the ratio of the net magnetic energy stored in the inductor to its ohmic loss and relate it to the performance of LC oscillators, in particular, the phase noise of the oscillators, an alternative definition of the quality factor that accounts for the swing of the voltage and current is needed.

For passive spiral inductors, the Q-factor is independent of the voltage and current of the inductors, described by Equation (4.37) and Equation (4.38),

$$Q(\omega) = \frac{\omega_0}{2}\frac{\partial \emptyset(\omega)}{\partial \omega} \tag{4.37}$$

$$Q = 2\pi \times \frac{Net\ magnetic\ energy\ stored}{energy\ dissipated\ in\ one\ oscilation\ cycle} \approx \frac{Re[z]}{Im[Z]} \approx \frac{\omega L}{R_s} \tag{4.38}$$

For active inductor, Q-factor is strong function of the swing of the voltage and current, including the transconductances and the load capacitances. An alternative definition of the Q-factor that accounts for the swing of the voltage and current is defined as

$$\overline{Q(\omega)} = \frac{\omega}{2(I_{max}-I_{min})}\int_{I_{min}}^{I_{max}} Q(\omega, i)di \tag{4.39}$$

Where $I_{min}\ and\ I_{max}$ are the minimum and the maximum currents of the transconductors, and $Q(\omega, i)$ is the instantaneous quality factor at frequency ω and channel current i, in a large-signal mode.

The quality factor of a typical lossy gyrator-C active inductor can be described by [22]

$$Q = [Q_1 \times Q_2 \times Q_3] = \left(\frac{\omega L}{R_s}\right) \times \left[\frac{R_p}{R_p + R_s\left(1+\left(\frac{\omega L}{R_s}\right)^2\right)}\right] \times \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 C_p L\right] \tag{4.40}$$

From Equation (4.40), Q_1 quantifies the quality factor of the active inductor at low frequencies, whereas Q_2 and Q_3 manifest themselves at high frequencies. Figure 4-12 shows the typical plots of frequency dependence of the quality factor (Q) of a lossy active inductor ($R_s = 4\Omega, R_p = 1K\Omega, C_p = 140fF, and\ L = 1.6nH$) [22].

General, $Q1$ is widely used to quantify the quality factor of active inductors as it dominates in the active inductor and is similar to the Q-factor of a passive inductor. However, Q_2 accounts for the effect of the finite output impedance of deep sub-micron MOSFETs, and Q_3 vanishes when frequency approaches the cut-off frequency of the transconductors of the active inductor.

Figure 4-13 and Figure 4-14 show the sensitivity of quality factor with respect to R_s and R_p. It can be seen that when frequency increases the quality factor Q1 increases to infinity and is limited by Q2 and Q3 as the frequency approaches the cutoff frequency of the transistor transconductance.

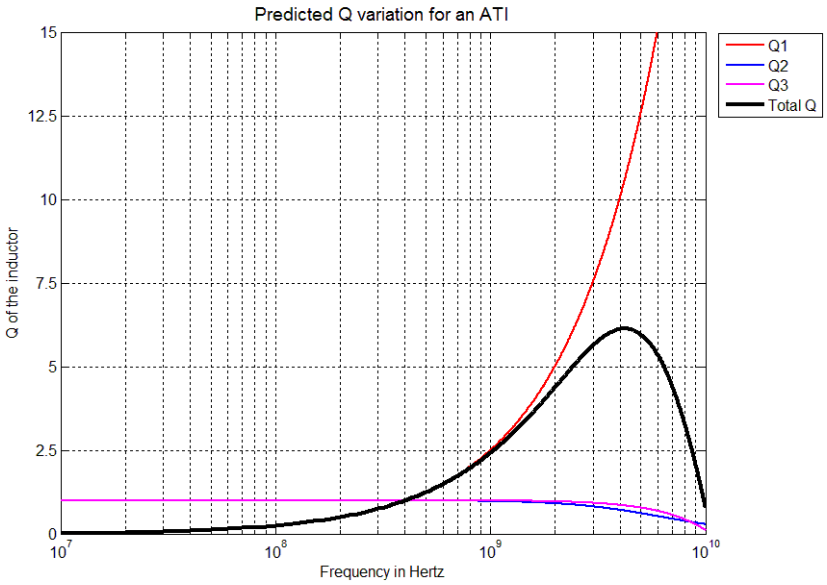


Figure 4-12 Frequency dependence of the quality factor of active inductors.

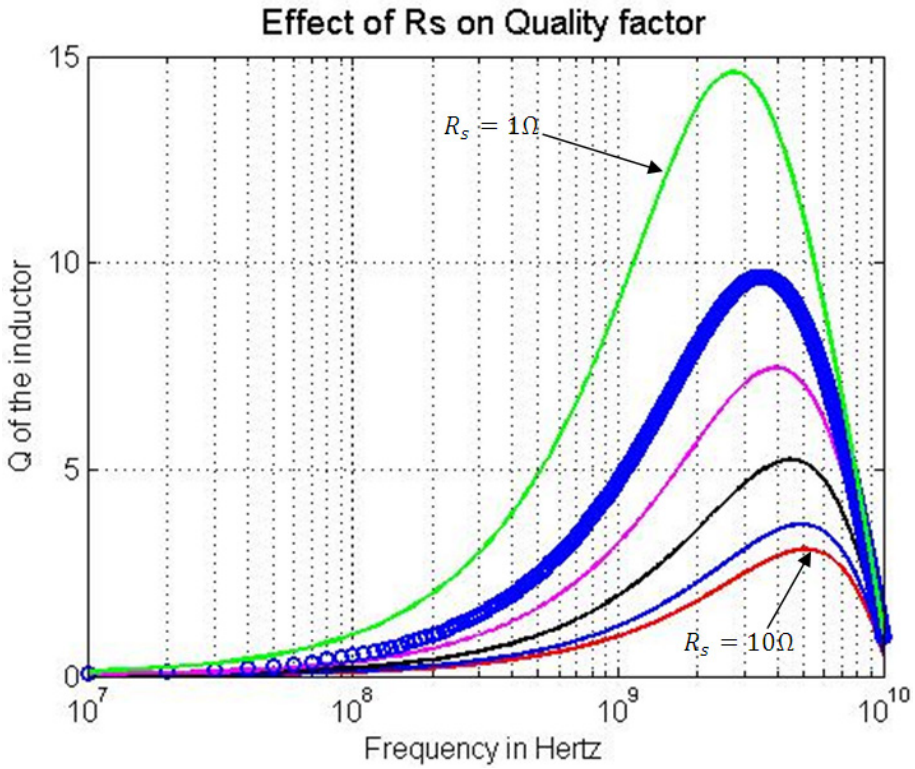


Figure 4-13 Shows the effect of R_s on the quality factor of active inductors. R_s is varied from 1Ω to 10Ω.

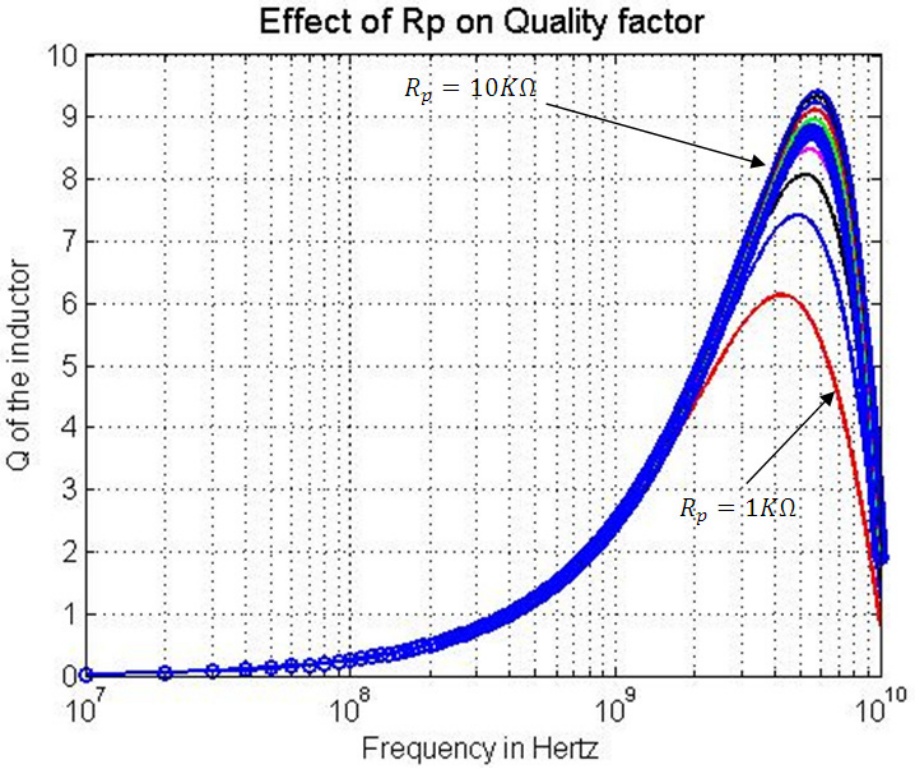


Figure 4-14 The effect of R_p on the quality factor of active inductors. R_p is varied from 1kΩ to 10kΩ.

To improve the Q factor of and active inductor R_s must be minimized. In general, four approaches can be implemented for the minimization of loss resistance R_s [22]:

Approach # 1

Figure 4-15 shows the typical schematics of transconductors with a positive transconductance, since $R_s = G_{o1} \times [g_{m1}g_{m2}]^{-1}$. One possible approach to reduce R_s is to increase the output impedance of the transconductor (lower the value of G_{o1}). G_{o1} is typically the output impedance of the transconductor with a positive transconductance, the use of transconductors with a large output impedance is critical. For a common-drain positive transconductor topology (Figure 4-15a), v_{GS} increases with v_{in}, which in turn increases i_D, resulting in an increased output current i_o ($i_o = i_D - J$). For a differential-pair positive transconductor topology as shown in Figure 4-15(b, c), an increased v_{in} will decrease i_{D1}, as a result, $i_{D2} = J_1 - i_{D1}$ will increase. Since $i_o = i_{D2} - J_2$, i_o will increase as well. Although both transconductors have a positive transconductance and both have an infinite input impedance, the output impedance of the transconductor in Figure 4-15(a) is given by approximately $1/g_m$ whereas that of the transconductor in Figure 4-15(b) or (c) is given by r_{o2}. However, the active inductors topology using the transconductor in Figure 4-15(b) or (c) will exhibit a lower value of R_s, and thereby, a higher Q.

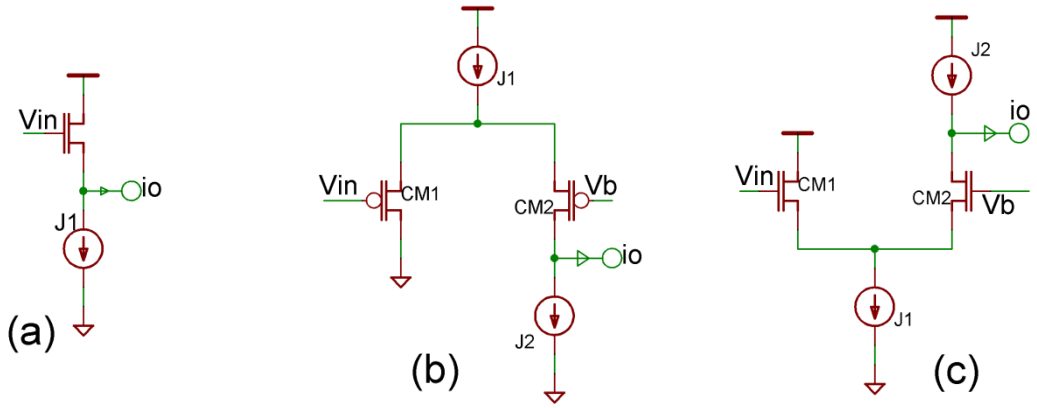


Figure 4-15 Typical schematics of transconductors with a positive transconductor: (a) Common-drain transconductor; (b), (c) Differential-pair transconductors [22]

Approach #2

Since $R_s = G_{o1} \times [g_{m1}g_{m2}]^{-1}$, R_s can be reduced by increasing g_{m1} and g_{m2} directly. Generally, the transconductances are directly proportional to the DC bias currents and the width of the transistors but this comes at the cost of power consumption at a given operating frequency. Increasing the DC bias currents increases the power consumption, whereas increasing the transistor width lowers the self-resonant frequency of the active inductor. Increasing transistor width also affects the inductance of the inductors.

Approach # 3

Using circuit techniques like cascode configuration can be effective to reduceG_{o1}. The cascode of Figure 4-16 can lower the output conductance. Table 4.1 compares the minimum supply voltage and output conductance for basic, cascode, regulated cascode, and multi-regulated cascode transconductors.

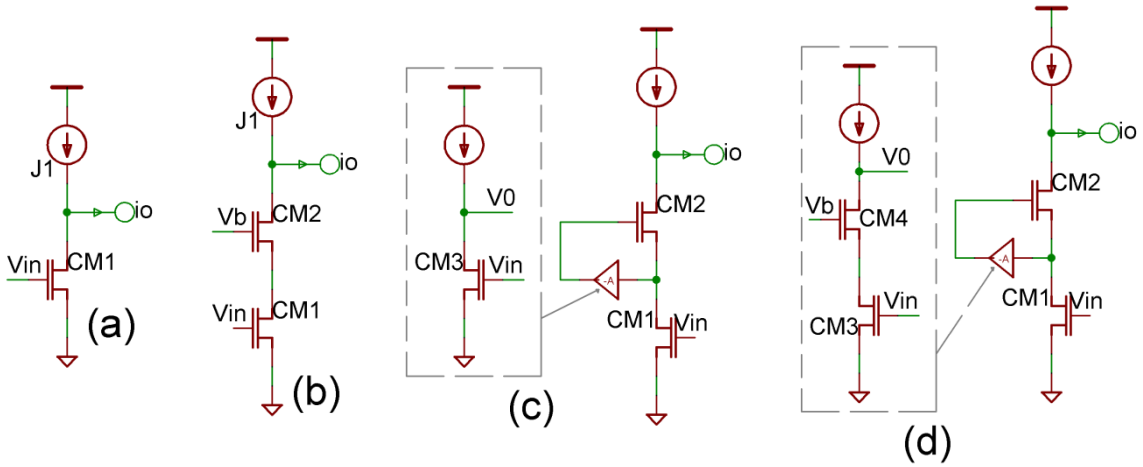


Figure 4-16 Schematics of cascode transconductors: (a) basic transconductor; (b) cascode transconductor; (c) regulated cascode transconductor; (d) multi-regulated cascode transconductor.

Approach # 4

Another approach is to use a shunt negative resistor at the output of the positive transconductor to cancel out the parasitic resistances, both in series and parallel, of active inductors.

The series RL network of the RLC network shown in Figure 4-17 can be replaced with the parallel RL network [22, 25].

$$R_p = R_s(1 + Q^2) \tag{4.41}$$

$$L_p = L_s(1 + Q^{-2}) \tag{4.42}$$

where $Q = \omega L_s/R_s$

In order for the two network to be equivalent they have to exhibit the same terminal impedance: $Z_s(j\omega) = Z_p(j\omega)$, resulting:

$$R_s + j\omega L_s = \frac{j\omega L_p R_p}{R_p + j\omega L_p} \tag{4.43}$$

$$R_s R_p - \omega^2 L_s L_p = 0 \tag{4.44}$$

$$R_s L_p + R_p L_s = R_p L_p \tag{4.45}$$

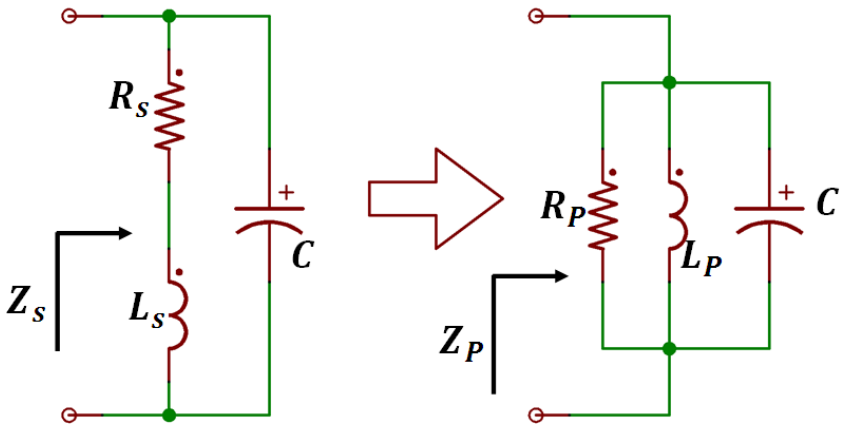


Figure 4-17 Transformation of a series RL branch to a parallel RL branch

Figure 4-18 shows the equivalent RLC network of a typical active inductor. The series $L \sim R_s$ branch of the RLC circuit of the active inductor can be characterized with the parallel $\hat{L} \sim \hat{R}_p$ as

$$\hat{R}_p = R_s(1 + Q^2) \tag{4.46}$$

$$\hat{L}_p = L_s(1 + Q^{-2}) \tag{4.47}$$

$$R_{total} = \hat{R}_p \parallel R_p \tag{4.48}$$

In this case, a negative resistor of resistance $R_{comp} = -R_{total}$ can be connected in parallel with C_p to eliminate the effect of both R_p *and* R_s of the active inductor simultaneously. Note that the resistance of the negative resistor should be made tunable such that a total cancellation can be achieved.

Table 4.1. The minimum supply voltage and output conductance for various transconductors [22]

Transconductor	Min. V_{DD}	Output Impedance
Basic	$2V_{sat}$	$G_o = \frac{1}{r_o}$
Cascode	$3V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})}$
Regulated Cascode	$2V_t + V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})}$
Multi-regulated Cascode	$2V_t + V_{sat}$	$G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})(r_{o4}g_{m4})}$

From Equation (4.41), if R_s is negligible, then R_p mainly influences the Q factor of the active inductor as

$$Q|_{R_s=0} = \left[\frac{\omega L}{R_s} \times \frac{R_p}{R_p + R_s\left(1+\left(\frac{\omega L}{R_s}\right)^2\right)} \times \left(1 - \frac{R_s^2 C_p}{L} - \omega^2 C_p L\right)\right]_{R_s \to 0} = \frac{R_p}{\omega L}\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right) \tag{4.49}$$

$$For\ \omega \ll \omega_0, \left(\frac{\omega}{\omega_0}\right)^2 \to 0\ Q = \frac{R_p}{\omega L_s} \tag{4.50}$$

From Equation (4.41), if R_p is large, the Q factor is mainly determined by R_s, and can be described by

$$Q = \frac{\omega L}{R_s}\left[1 - \left(\frac{\omega_Z}{\omega_0}\right)^2 - \left(\frac{\omega}{\omega_0}\right)^2\right] \tag{4.51}$$

$$For\ \omega_Z < \omega < \omega_0, \left(\frac{\omega_Z}{\omega_0}\right)^2 \to 0\ and\ \left(\frac{\omega}{\omega_0}\right)^2 \approx 0 \to Q = \frac{\omega L}{R_s} \tag{4.52}$$

The quality factor of the compensated active inductor at ω_0 is given by

$$Q(\omega_0) = R_{total} \parallel R_{comp}\sqrt{\frac{C_p + C_{comp}}{L}} \tag{4.53}$$

Where C_{comp} is the input capacitance of the compensating negative resistor.

In general, R_p *and* R_s are frequency-dependent. R_{comp} should be designed in such a way that a total resistance cancellation is obtained across the frequency range of the active inductor.

The negative resistor compensation technique can be used to improve the quality factor of spiral inductors, however, a total compensation is difficult to achieve because the active negative

resistor network is used to cancel out the large skin effect induced by the parasitic series resistance of spirals.

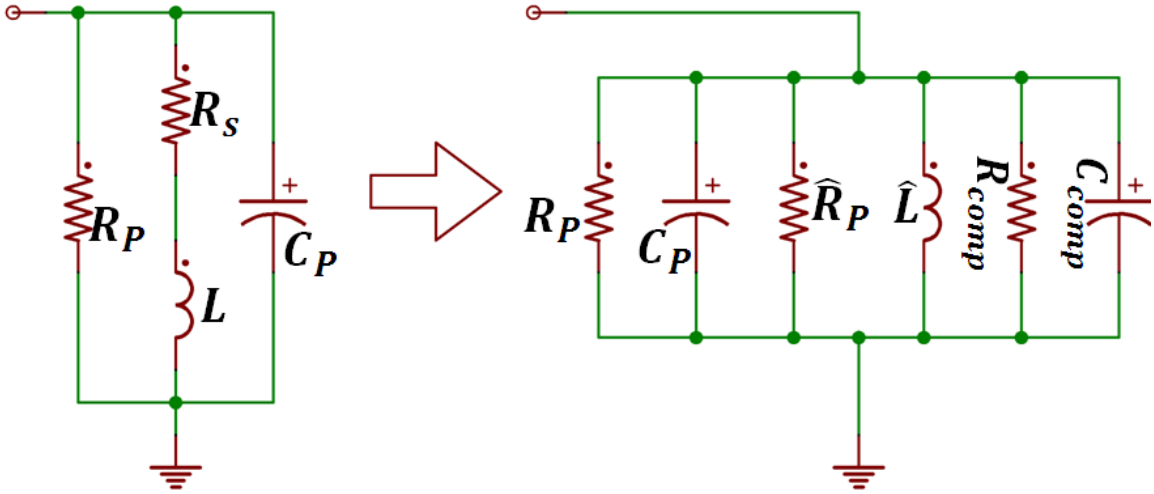


Figure 4-18 Q improvement technique using an active resistor (shunt negative resistor).

4.3.1.4 Noise

Intrinsically, active inductors show higher noise characteristics as compared with their spiral counterparts. Figure 4-19 shows the partial schematic of basic transconductors used in active inductor topologies with the relevant input-referred noise sources (voltage and current generator) for comparative analysis. Table 4.2 describes the noise characteristics of the basic transconductors widely used in active inductor topologies at low frequencies with the power of the input-referred noise voltage $\overline{v_n^2}$ and noise current $\overline{i_n^2}$ generators, where $\overline{i_{nD}^2}$ can be described as [22, 26].

$$\overline{i_{nD}^2} = 4kT(\gamma + R_g g_m) g_m \Delta f \tag{4.54}$$

Equation (4.54) represents the sum of the power of the thermal noise generated in the MOSFET channel and the thermal noise of the MOSFET gate series resistance.

R_g is the gate series resistance,
$\gamma = 2.5$ for deep sub-micron devices,

T is the temperature in degrees Kelvin, and k is the Boltzmann constant (neglecting the effect of the flicker noise, thermal noise of the bulk resistance of the source and drain diffusions) [27].

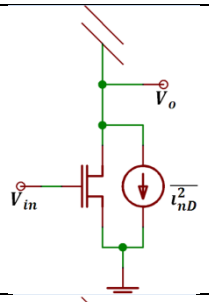
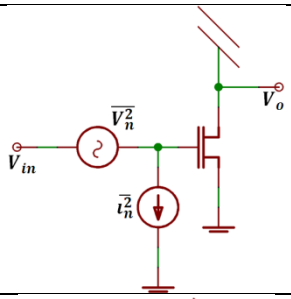
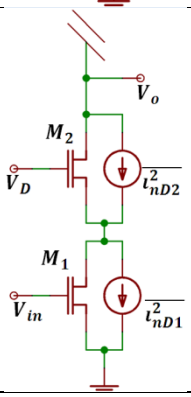
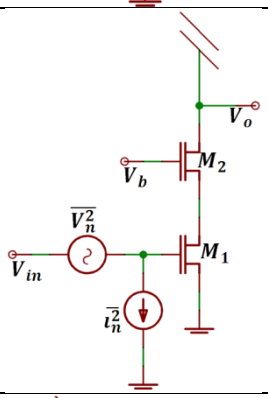
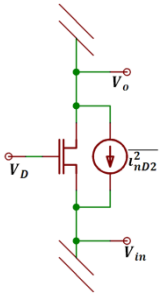
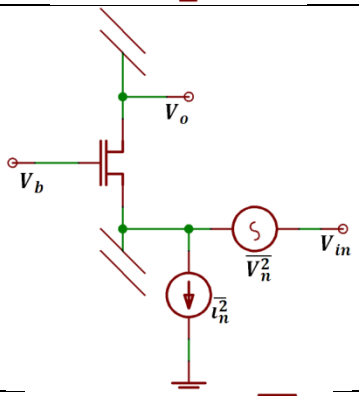
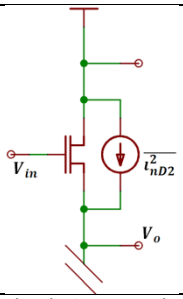
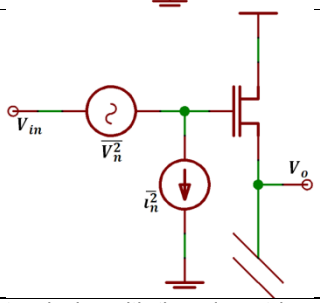
	Transconductors with noise sources	Transconductors with noise generators
Common source		
Cascode		
Common gate		
Source follower		

Figure 4-19 Partial schematics of the basic transconductors used in active inductor topologies with the relevant input-referred noise sources (voltage and current noise generators) for comparative analysis [22].

To illustrate the results of Table 4.2, Figure 4-20 shows the equivalent representation by short-circuiting the input for the derivation of the input-referred noise-voltage generator $\overline{v_n^2}$ of the transconductor. The output noise power of the transconductor due to i_{nD} is given by

$$\overline{v_{no}^2} = \overline{i_{nD}^2} r_o^2 \tag{4.55}$$

where r_o is the output resistance of the transistor.

The output noise power of the transconductor can be obtained by removing $\overline{i_{nD}^2}$ and applying v_n at the input of the transconductor (Figure 4-21) [22]

$$\overline{v_{no}^2} = \overline{v_n^2}(1 + r_o g_m)^2 \tag{4.56}$$

From Equation (4.55) and Equation (4.56)

$$\overline{v_n^2} = \overline{i_{nD}^2}\left[\frac{r_o^2}{(1+r_o g_m)^2}\right] \approx \frac{1}{g_m^2}\overline{i_{nD}^2} \quad (for\ r_o g_m \gg 1) \tag{4.57}$$

To derive the noise-current generator of the common-gate transconductor, consider Figure 4-22 where the input port of the transconductor is open-circuited and the output noise power of the circuit is calculated. To avoid the difficulty caused by the floating node 1, we assume that there exists a resistor of resistance R_x between node 1 and the ground.

Note that this approach is used in most IC CAD systems to avoid floating nodes. Writing KCL at nodes 1 and 2 yields [22]

$$(g_x + g_m + g_o)v_1 - g_o v_2 = i_{nD} \quad (node\ \#1) \tag{4.58}$$

$$-(g_m + g_o)v_1 + g_o v_2 + i_{nD} = 0 \quad (node\ \#2) \tag{4.59}$$

From Equation (4.58) and Equation (4.59)

$$\overline{v_n^2} = \overline{i_n^2}\frac{1}{g_x^2}\left[1 + \frac{g_m}{g_o}\right]^2 \tag{4.60}$$

From Equation (4.57) and Equation (4.60)

$$\overline{i_n^2} = \frac{\overline{i_{nD}^2}}{\left[\left(1+\frac{g_m}{g_o}\right)\right]^2} \times \left(\frac{g_x}{g_o}\right)^2 \quad for\ g_x \to 0, \overline{i_n^2} = 0 \tag{4.61}$$

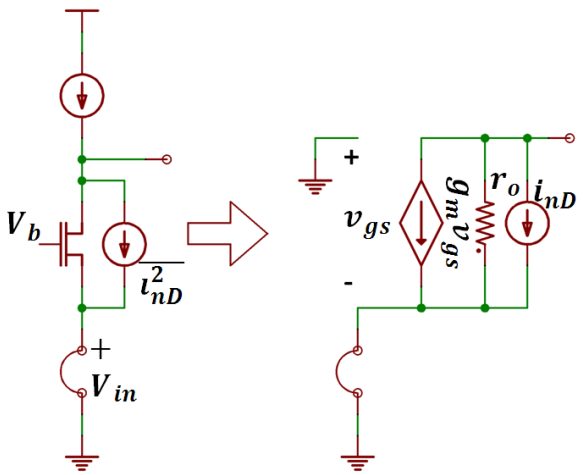


Figure 4-20 Schematic of the input-referred noise-voltage generator of a common-gate transconductor at low frequencies.

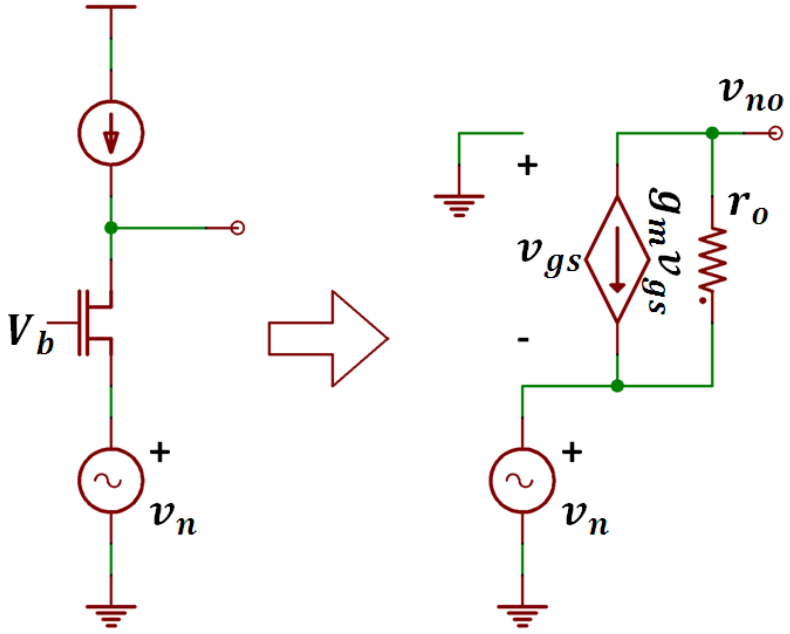


Figure 4-21 Schematic of the input-referred noise-voltage generator of a common-gate transconductor at low frequencies.

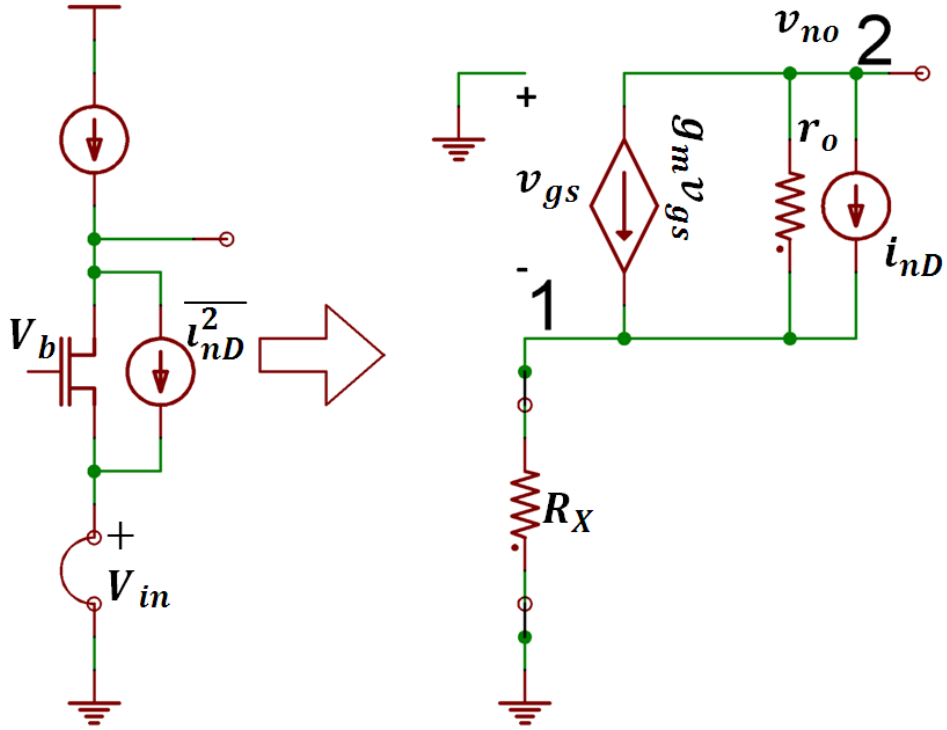


Figure 4-22 Schematic of the input-referred noise-current generator of a common-gate transconductor at low frequencies.

From Equation (4.57) and Equation (4.61), $\overline{v_n^2}$ *and* $\overline{i_n^2}$ of the transconductors are available. The power of the input referred noise-voltage and noise-current generators of active inductors can be derived. Figure 4-23 shows the typical representation of the active inductor topology where $\overline{v_{n1}^2}$ *and* $\overline{v_{n2}^2}$ denote the power of the noise-voltage generators of the transconductors 1 and 2, respectively, and Y_1 *and* Y_2 are the admittance at ports 1 and 2, respectively. As shown in Figure 4-23(a), $\overline{V_1^2}$ can be described by

$$\overline{V_1^2} = \overline{\left(V_{n1} + Y_1 \frac{G_{m2}V_{n2} + Y_2 V_{n1}}{Y_1 Y_2 + G_{m1}G_{m2}} \right)^2} \tag{4.62}$$

For the equivalent network of Figure 4-19(b), $\overline{V_1^2}$ can be given by

$$\overline{V_1^2} = \overline{\left(V_n + \frac{Y_1}{Y_1 Y_2 + G_{m1}G_{m2}} I_n^2 \right)^2} \tag{4.63}$$

Since the equivalent network shown in Figure 4-23(a) and Figure 4-23(b) are identical, this leads to following:

$$V_n = V_{n1} \tag{4.64}$$

$$I_n = V_{n1}Y_2 + V_{n2}G_{m2} \tag{4.65}$$

$$Z_{in}(s) = \frac{Y_1}{Y_1 Y_2 + G_{m1}G_{m2}} \tag{4.66}$$

$$V_n = V_{n1} + Z_{in}\, I_{in} \tag{4.67}$$

For lossy active inductors

$$Y_1 = G_{o1} + sC_1 \tag{4.68}$$

$$Y_2 = G_{o2} + sC_2 \tag{4.69}$$

From Equation (4.65) and Equation (4.69),

$$I_n = (G_{o2} + sC_2)V_{n1} + G_{m2}V_{n2} \tag{4.70}$$

Assuming V_{n1} and V_{n2} are uncorrelated, from Equation (4.64) and Equation (4.70) yield:

$$\overline{V_n^2} = \overline{V_{n1}^2} \tag{4.71}$$

$$\overline{I_n^2} = \left(|G_{o2} + sC_2|\right)^2 \overline{V_{n1}^2} + G_{m2}^2 \overline{V_{n2}^2} \tag{4.72}$$

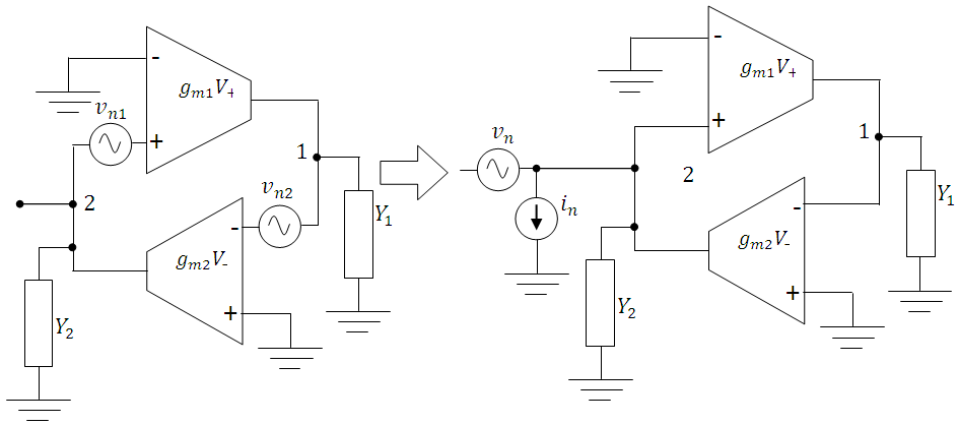


Figure 4-23 Equivalent representation of the active inductor topology where $\overline{v_{n1}^2}$ *and* $\overline{v_{n2}^2}$ denote the power of the noise-voltage generators of the transconductors 1 and 2, respectively, and Y_1 *and* Y_2 are the admittance at ports 1 and 2, respectively.

Table 4.2 describes the noise characteristics of the basic transconductors widely used in the active inductor topologies at low frequencies, with power of the input-referred noise-voltage and noise current generators [22].

Table 4.2 The noise characteristics of the basic transconductors used in the AI topology at low frequencies

Transconductor	$\overline{\upsilon_n^2}$	$\overline{i_n^2}$
Basic	$\overline{\upsilon_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Cascode	$\overline{\upsilon_n^2} = \frac{\overline{i_{nD1}^2}}{g_{m1}^2} + \frac{\overline{i_{nD2}^2}}{(g_{m1}r_{o1}g_{m2})^2}$	$\overline{i_n^2} = 0$
Common gate	$\overline{\upsilon_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$
Source follower	$\overline{\upsilon_n^2} = \frac{\overline{i_{nD}^2}}{g_m^2}$	$\overline{i_n^2} = 0$

4.3.1.5 Linearity

Transconductors of the active inductor are linear only if the swing of the input voltage for the transconductors is small. When the voltage swing is large, the transconductors will exhibit a nonlinear characteristic and the synthesized active inductors are no longer linear. Thus, the linearity constraint of active inductor sets the maximum operating voltage swing. When the transistors enter the triode region, the transconductances decrease from g_m (saturation) to g_{ds} (triode) in a nonlinear fashion, as depicted graphically in Figure 4-24.

The inductance of the gyrator-C active inductors increases from $L = \frac{C}{g_{m1}g_{m2}}$ to $L = \frac{C}{g_{ds1}g_{ds2}}$.

Note that we have assumed that the load capacitance C remains unchanged. The inductance thus varies with the swing of the voltage of the active inductor in a nonlinear fashion. It should also be noted that the parasitic resistances also vary with the voltage swing.

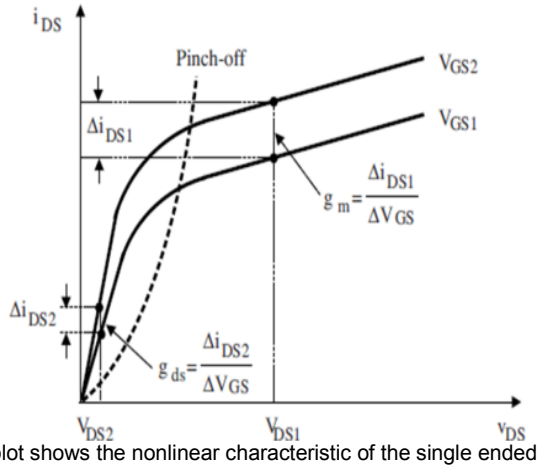


Figure 4-24 A typical plot shows the nonlinear characteristic of the single ended lossy active inductors

4.3.1.6 Stability

Typical active inductors use negative feedback system topologies. The stability of active inductor is critical to the overall stability of system employing them. The impedance at port 2 of the gyrator-C active inductor shown in Figure 4-25 is given by [22]

$$Z = \frac{G_{01} + sC_1}{s^2 C_1 C_2 + s(C_1 + C_2) + g_{m2} g_{m1}} \tag{4.73}$$

where we have utilized $g_m >> G_o$ to simplify the results.

The poles of the system are given by [22]

$$p_{1,2} = \frac{(C_1 + C_2)}{2C_1 C_2}\left[-1 \pm \sqrt{1 - \frac{4C_1 C_2 g_{m2} g_{m1}}{(C_1 + C_2)^2}}\right] \tag{4.74}$$

The poles of the gyrator-C active inductor are located in the left half of the *s*-plane and the gyrator-C active inductor is a stable system. The degree of stability can be assessed by evaluating its damping factor, which is obtained by comparing the denominator of Equation (4.73) with the standard form of the characteristic equation of second-order systems:

$$s^2 + 2\omega_0 \xi s + \omega_0^2 = 0 \tag{4.75}$$

where ξ denotes the damping factor and ω_o is the pole frequency. It should be noted that the preceding analysis is based on the assumption that active inductors are 2nd-order systems. When the parasitic of MOSFETs are accounted for, active inductors are no longer 2nd-order systems and their stability will deteriorate, which can be described by [22]

$$\xi = \frac{1}{2\sqrt{g_{m2} g_{m1}}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right) \tag{4.76}$$

From Equation (4.74), an increase in $g_{m1} and\ g_{m2}$ will lead to a decrease in ξ. This is replicated with an increase in the level of oscillation in the response of the active inductor. In addition to this, the ratios $\frac{C_1}{C_2}$ and $\frac{C_2}{C_1}$ have a marginal impact on the damping factor simply because these two quantities vary in opposite directions when $C_1 and\ C_2$ change, and the values of $C_1\ and\ C_2$ are often close. For a given $C_1 = C_2 = C$ and $g_{m1} = g_{m2} = g_m$,

$$p_{1,2} = \frac{1}{C}\left[-1 \pm \sqrt{1 - g_m^2}\right] \tag{4.77}$$

$$\xi = \frac{1}{g_m} \tag{4.78}$$

From Equation (4.77) and Equation (4.78), increasing g_m will lead to a decrease of ξ. This is echoed with a reduced level of damping. Since $p_{1,2} = -\frac{1}{C}$, the absolute stability margin is set by the capacitance C and is independent of g_m[22].

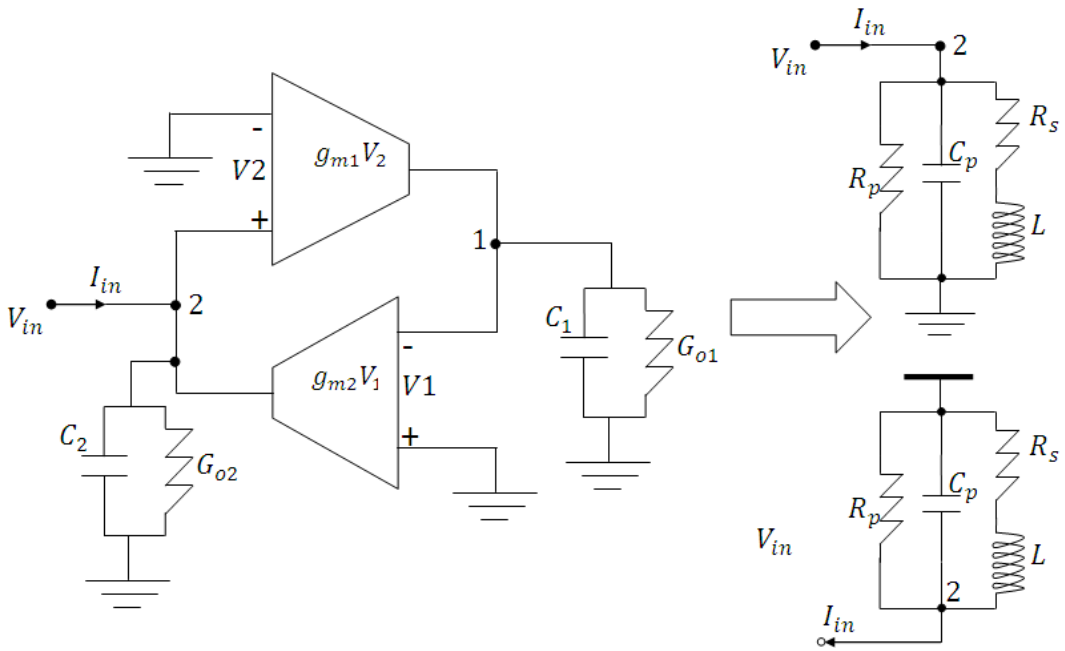


Figure 4-25 Schematic used for the stability characteristics of the active inductor and the dependence of damping factor on stability

4.3.1.7 Supply Voltage Sensitivity

The supply voltage sensitivity of an active inductor is a figure-of-merit (FOM) quantifying the effect of the variation in supply voltage on the inductance of the active inductor. The fluctuations in the supply voltage for a mixed analog-digital system occur mainly due to the switching noise of the system [22].

Assume that the supply voltage of a mixed-mode system containing an active inductor varies from V_{DD} to $V_{DD}+\Delta V_{DD}$, where ΔV_{DD} is a random variable with mean zero denoted as $E[\Delta V_{DD}] = 0$ and $\Delta V_{DD} << V_{DD}$ holds true. The small-signal analysis approach can therefore be employed to analyze the effect of ΔV_{DD} on the inductance of the active inductor. Following the definition given in [6], the normalized sensitivity of the inductance of an active inductor to the supply voltage is defined as

$$S_{V_{DD}}^{L} = \left(\frac{V_{DD}}{L}\right)\frac{\partial L}{\partial V_{DD}} \tag{4.79}$$

The fluctuation of the supply voltage V_{DD} affects the inductance of the active inductor mainly by altering the DC operating point and subsequently the transconductances of the transconductors constituting the active inductor. By assuming that the load capacitance C of the gyrator-C active inductor does not vary with V_{DD} and because $L = \frac{C}{g_{m1}g_{m2}}$ then $\frac{\partial L}{\partial V_{DD}}$ can be described by

$$\frac{\partial L}{\partial V_{DD}} = -L\left(\frac{1}{g_{m1}}\frac{\partial L}{\partial g_{m1}} + \frac{1}{g_{m2}}\frac{\partial L}{\partial g_{m2}}\right) \tag{4.80}$$

The normalized supply voltage sensitivity of the active inductor is given by

$$S_{V_{DD}}^{L} = -\left(S_{V_{DD}}^{g_{m1}} + S_{V_{DD}}^{g_{m2}}\right) \tag{4.81}$$

where $S_{V_{DD}}^{g_{m1}}$ and $S_{V_{DD}}^{g_{m2}}$ are the normalized supply voltage sensitivities of $g_{m1} and\ g_{m2}$, respectively. Equation (4.80) reveals that both $S_{V_{DD}}^{g_{m1}}$ and $S_{V_{DD}}^{g_{m2}}$ contribute equally to $S_{V_{DD}}^{L}$. To minimize the supply voltage sensitivity of active inductors, transconductors with a constant g_m should be used.

4.3.1.8 Parameter Sensitivity

A typical active inductor consists of number of active devices and the performance is influenced by the parameter spread of these components. The normalized sensitivity of the inductance of an active inductor to a parameter x_j of the inductor defined as [22]

$$S_{x_j}^{L} = \frac{x_j}{L}\frac{\partial L}{\partial x_j} \tag{4.82}$$

Considering the parameters of the active inductor are Gaussian distributed and uncorrelated, the overall effect of the variation of the parameters of the active inductor on the inductance of the inductor can be described by [22]

$$\sigma_L^2 = \sum_{k=1}^{N}\left(\frac{\partial L}{\partial x_j}\right)^2 \sigma_{x_j}^2 \tag{4.83}$$

where σ_{L} and $\sigma_{\mathrm{x_j}}$ denote the standard deviations of L and $\mathrm{x_j}$, respectively, and N is the number of parameters in the active inductor.

For a typical gyrator-C active inductor,

$$\frac{\partial L}{C} = \frac{1}{g_{m1}g_{m2}} \tag{4.84}$$

$$\frac{\partial L}{g_{m1}} = -\frac{C}{g_{m1}^2 g_{m2}} \tag{4.85}$$

$$\frac{\partial L}{g_{m2}} = -\frac{C}{g_{m2}^2 g_{m1}} \tag{4.86}$$

Assuming that the parameters of the active inductors are Gaussian distributed and uncorrelated, the normalized spread of the inductance of the active inductor can be described by

$$\frac{\sigma_L^2}{L^2} = \frac{\sigma_C^2}{C^2} + \frac{\sigma_{g_{m1}}^2}{g_{m1}^2} + \frac{\sigma_{g_{m2}}^2}{g_{m2}^2} \tag{4.87}$$

The effect of parameter spreads on the inductance can be analyzed by 'corner' and 'Monte Carlo' analysis. The corner analysis determines the inductance at process corners. The Monte Carlo analysis quantifies the degree of the spread around the nominal value of inductance for the active inductor. The accuracy of Monte Carlo analysis increases with an increase in the number

of simulation runs and is therefore extremely time consuming. Corner analysis, on the other hand, is time-efficient and hence most widely used, but the results obtained are typically over conservative [22].

4.3.1.9 Signal Sensitivity

Unlike spiral inductors whose inductance is independent of the voltage and current of the inductor, the inductance of gyrator-C active inductors varies with the voltage and current of the transconductors constituting the active inductors [22]. This is because the transconductances $g_{m1} and\ g_{m2}$, when signal swing is large, are signal-dependent. When an active inductor is used in applications where the voltage of the active inductor experiences a large degree of variation, such as active inductor LC oscillator, the transconductances vary with the signal swing. As a result, the inductance, parasitic resistance, and quality factor of the active inductor all vary with the signal swing.

4.3.1.10 Power Consumption

Spiral inductors do not consume static power. Active inductors consume DC power, mainly due to the DC bias currents of their transconductors. The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance is inversely proportional to the transconductances. To have a large inductance, $g_{m1} and\ g_{m2}$ are made small which is achieved by lowering the DC bias currents of the transconductors. When replica biasing is used to minimize the effect of supply voltage fluctuation on the inductance of active inductors, the power consumed by the replica-biasing network must be accounted for. Sometimes negative resistance is employed for boosting the quality factor of active inductors and their power consumption must be included. Often the power consumption of an active inductor is set by that of its replica-biasing and negative resistor networks.

4.4 Implementation of Active Inductors

For the realization of a higher SRF (self-resonant frequency), synthesized active inductor topologies that are comprised of transconductors should be configured with minimum possible components and as simple as possible. This effectively reduces the power consumption, including the silicon area required to fabricate the synthesized inductor. In general, the gyrator based active inductor topology employs a common-source configuration as negative transconductors, common-gate, source follower, and differential pair configurations as positive transconductors. These basic transconductors have the simplest configuration, yield the highest cutoff frequency and uses the lowest silicon area. In addition to this, the load capacitor of the transconductors is realized using the intrinsic capacitance C_{gs} of the transistors. This will directly maximize the upper bound of the active inductor frequency range and avoid the use of expensive floating capacitors, which are available only in mixed-mode CMOS processes. MOS varactors are often added in parallel with C_{gs} to tune the inductance of active inductor.

4.4.1 Single-Ended Active Inductors

The following sections present a comprehensive treatment of both the circuit implementation and characteristics of single-ended CMOS active inductors [22]. It is based on the following assumptions made in the analysis of the active inductor and in determination of their signal swing and the minimum supply voltage. To help simplify the mathematical treatment the following in assumed: (i) nMOS and pMOS transistors have the same threshold voltage V_T. (ii)

nMOS and pMOS transistors have the same pinch-off voltage V_{sat}. (iii) Only C_{gs} is considered. C_{gd} and parasitic diffusion capacitances are neglected unless otherwise noted explicitly. (iv) The minimum voltage drop across bias current source and current-source loads is V_{sat}.

4.4.1.1 Basic Gyrator-C Active Inductors

Figure 4-26 shows the typical schematics of two basic gyrator-C active inductors, where all transistors form the active inductor topology are biased in saturation. In Figure 4-26(a), the transconductor with the positive transconductance is common gate configured and the transconductor with the negative transconductance is common-source configured. In Figure 4-26(b), the transconductor with the positive transconductance is common-drain configured and the transconductor with the negative transconductance is common-source configured. It can be seen that the active inductor topology shown in Figure 4-26(b) is comprised of nMOS transistors, making it attractive for high frequency applications [22].

The parameters of the equivalent RLC network of the lossy single-ended active inductor with $C_1 = C_{gs2}, G_{o1} \approx g_{o1}, G_{m1} = g_{m1}, C_2 = C_{gs1}, G_{o2} \approx g_{m1}$, $and\ G_{m2} = g_{m2}$, $where\ g_{oj}\ and\ g_{mj}$, $j = 1, 2$, are the output conductance and transconductance of transistor j, can be described by

$$R_p = \left[\frac{1}{g_{m1}}\right] \tag{4.88}$$

$$R_S = \left(\frac{g_{o1}}{g_{m1}g_{m2}}\right) \tag{4.89}$$

$$C_p = C_{gs1} \tag{4.90}$$

$$L = \left(\frac{C_{gs2}}{g_{m1}g_{m2}}\right) \tag{4.91}$$

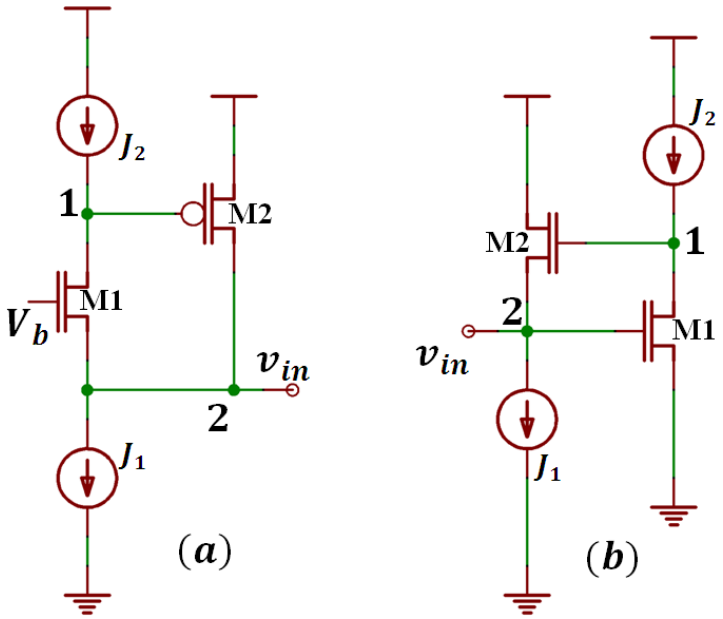


Figure 4-26 A typical simplified schematic of basic gyrator-C active inductors

From Equation (4.88) and Equation (4.89), for large values of transconductance, the parasitic parallel resistance R_p exhibits a rather small value, whereas the parasitic series resistance R_s is often large. These limit the quality factor of the active inductor. Moreover, the effect of the parasitic series resistance R_s is often neglected as R_p is small, and in this case, the quality factor (Q), self resonant frequency (f_0), and the cut-off frequencies (f_{t1} and f_{t2}) of the active inductor can be described by

$$Q \approx \frac{R_p}{2\pi f L} = \frac{f_{t2}}{f} \Rightarrow Q(f_o) = \frac{f_{t2}}{f_o} = \sqrt{\frac{f_{t2}}{f_{t1}}} \tag{4.92}$$

$$\text{Where, } f_0 \approx \frac{1}{2\pi}\left[\frac{1}{\sqrt{C_p L}}\right] = \sqrt{f_{t1} f_{t2}} \tag{4.93}$$

$$f_{t1} = \frac{g_{m1}}{C_{gs1}}, \quad f_{t2} = \frac{g_{m2}}{C_{gs2}} \tag{4.94}$$

From Equation (4.89), the parasitic series resistance R_s can be lowered by incorporating cascode and regulated cascode topologies to reduce g_{o1} [27]-[31]. The zero frequency of the active inductor, which is the lower bound of the useful frequency range, is described by

$$f_z = \frac{g_{o1}}{C_{gs2}} \tag{4.95}$$

From Equation (4.92) - Equation (4.95), f_0 can be increased by reducing f_z. This can be achieved by reducing g_{o1} or increasing C_{gs2} but, the former is usually preferred as the latter lowers f_o. In addition to this, the output impedance of deep sub-micron MOSFETs is small, thus the detrimental effect of $R_p = 1/g_{m1}$ on the quality factor cannot be neglected. However, the effect of R_p can be compensated by incorporating an active resistor (negative loss resistance) of $\widehat{R}_p = -R_p$ in parallel with R_p. Figure 4-27 and Figure 4.28 show the typical configuration of single-ended and differential active resistor networks using transconductors with positive feedback.

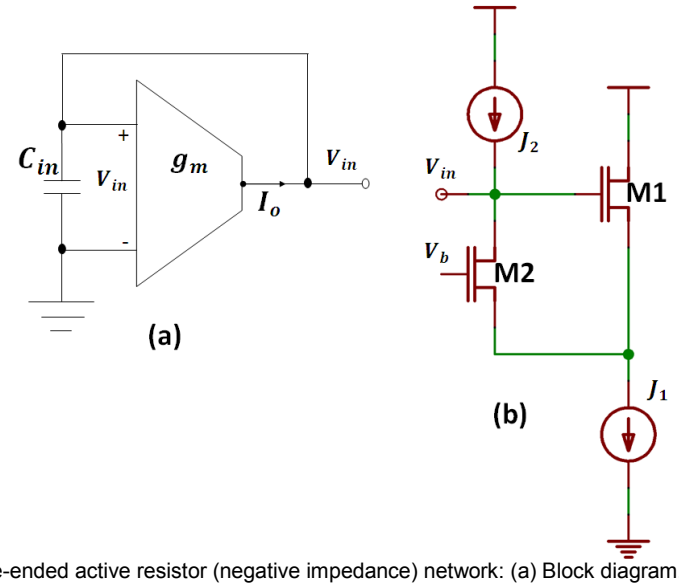


Figure 4-27 A typical single-ended active resistor (negative impedance) network: (a) Block diagram. (b) Circuit implementation.

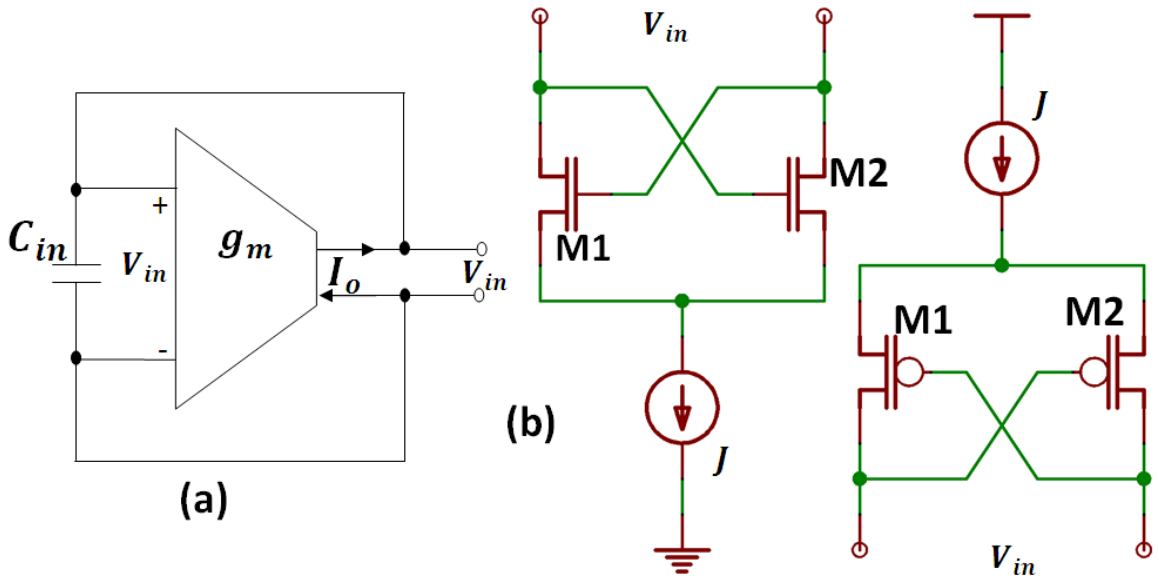


Figure 4-28 A typical differential active resistor (negative impedance) network: (a) Block diagram. (b) Circuit implementation. The tail current source in the differential configuration can be removed, provided that biasing currents are provided by the circuit connected to the negative resistor but at the cost of tunability [22].

Table 4.3 describes the range of the voltage swing and the minimum supply voltage of the two basic active inductors shown in Figure 4-26. It is noticed that active inductor topology depicted in Figure 4-26(a) offers a large input voltage swing with comparatively lower minimum supply voltage.

Table 4.3 Performance characteristics of single-ended basic gyrator-C active inductor topologies

Single-ended Active Inductor	Figure 4-26(a)	Figure 4-26(b)
Maximum Input Voltage	$V_{DD} - V_T - V_{sat}$	$V_{DD} - V_T - V_{sat}$
Minimum Input Voltage	V_{sat}	V_T
Minimum V_{DD}	$V_T + 2V_{sat}$	$2V_T + V_{sat}$

4.4.1.2 Wu Current-Reuse Active Inductors

Figure 4-29 show the typical schematic of Wu current-reuse active inductors proposed in [32]-[34]. As shown in Figure 4-29 (a), the positive transconductor in nMOS version can be realized in common-gate configuration, whereas the negative transconductor is common-source configured. The parameters of the equivalent RLC network of the Wu current-reuse active inductor with $C_1 = C_{gs2}, G_{o1} \approx g_{o1} + g_{o2}, G_{m1} = g_{m1}, C_2 = C_{gs1}, G_{o2} = 1/g_{m1}$, $and\ G_{m2} = g_{m2}$ can be described by [22]

$$R_p = \left[\frac{1}{g_{m1}}\right] \tag{4.96}$$

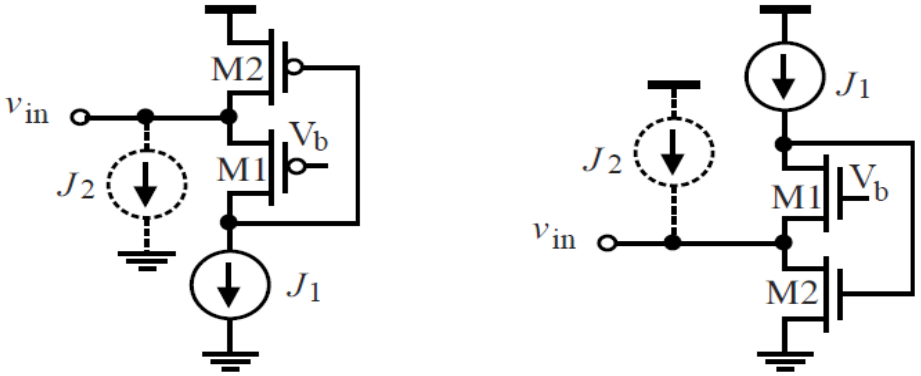
$$C_p = C_{gs1} \tag{4.97}$$

$$R_S = \left(\frac{g_{01} + g_{02}}{g_{m2} g_{m1}}\right) \tag{4.98}$$

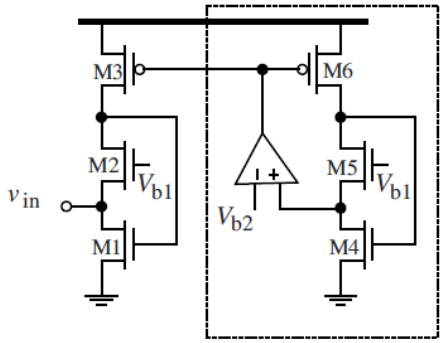
$$L = \left(\frac{C_{gs2}}{g_{m2} g_{m1}}\right) \tag{4.99}$$

$$Q \approx \frac{R_p}{2\pi f L} = \frac{f_{t2}}{f} \Rightarrow Q(f_o) = \frac{f_{t2}}{f_o} = \sqrt{\frac{f_{t2}}{f_{t1}}}, \quad f_0 = \sqrt{f_{t1} f_{t2}} \tag{4.100}$$

To increase f_o, both f_{t1} and f_{t2} need to be increased, but increasing the value of f_{t1} lowers $Q(\omega_o)$. Therefore, for higher f_o, it is advisable to increase f_{t2} without increasing f_{t1}. This can be achieved by keeping constant the DC bias current of M_1 constant while that of M_2 is increased by injecting an additional current J_2 into M_2. The additional current source J_2 is used to improve the transconductance of M_2 in such a way that the upper frequency bound can be increased without lowering the $Q(\omega_o)$. In practical design, J_2 is provided by the stage proceeding to the inductors and the active inductors are known as Wu current-reuse active inductors [22].



(a) Simplified schematic of Wu current reuse active inductors



(b)Simplified schematic of Wu current reuse active inductor (nMOS) with replica biasing.

Figure 4-29 A typical schematic of Wu active inductors: (a) Wu current reuse active inductors, and (b) Wu current reuse active inductor (nMOS) with replica biasing

It is evident that the parameters of synthesized active inductors, such as the inductance and parasitic resistance, are sensitive to the fluctuation of the supply voltage because a fluctuation not only alters the DC operating point of the transconductors, but also changes the junction capacitance of the active inductor. Figure 4-29 (b) shows the configuration of Wu current-reuse active inductors with replica biasing that reduces the effect of supply voltage fluctuation [71]. As shown in Figure 4-29 (b), the replica-biasing section is comprised of a sensing circuit using $M_{4,5,6}$ and an auxiliary voltage amplifier, where an increase in V_{DD} will lead to an increase in $v_{SG3,6}$, and subsequently the channel current of $M_{3,6}$. [22]. Therefore, the voltage of the non-inverting terminal of the amplifier increases, and the output of the amplifier boosts the gate voltage of $M_{3,6}$. This ensures that $v_{SG3,6}$ is kept nearly unchanged, minimizing the effect of the V_{DD}

fluctuation. Care must be taken to maintain the width of the transistors in the replica-biasing section as that of the active inductor section so that both sections will sense the same voltage change caused by the variation of V_{DD}.

4.4.1.3 Lin-Payne Active Inductors

Figure 4-30 and Figure 4-31 show the typical Lin-Payne active inductor circuits, which require the minimum supply voltage of only $V_T + 2V_{sat}$ [35]. They can be analyzed in a similar way as the Wu current re-use active inductors shown in Figure 4-29.

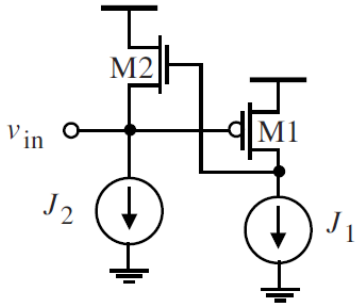


Figure 4-30 A typical simplified schematic of Lin-Payne active inductor.

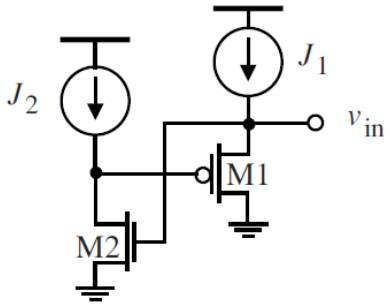


Figure 4-31 A typical simplified schematic of a variation of Lin-Payne active inductor of Figure 4-30.

4.4.1.4 Hara Active Inductors

Figure 4-32 and Figure 4-33 show the simplified schematic and small-signal equivalent circuits for the Hara active inductor circuits, which employ only a MOSFET and a resistor [37]-[44]. As shown in Figure 4-32, feedback operation of active inductor is realized as follows: increase of the input current will result in an increase in the voltage at the input node, since the gate voltage is kept at V_{DD}, v_{GS} is reduced, resulting in lower current out of the active inductor [22]. The major drawback of the Hara active inductor topology is loss of the voltage headroom by at least V_T.

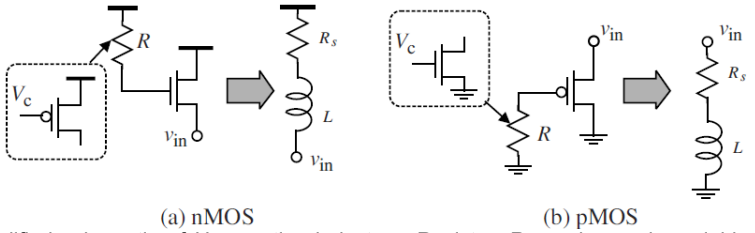


Figure 4-32 A typical simplified schematic of Hara active inductors: Resistor, R can be made variable by implementing it using MOSFETs biased in the triode.

From Figure 4-33, the input impedance can be described by

$$Z \approx \left(\frac{1}{RC_{gs}C_{gd}}\right)\left(\frac{1+sRC_{gd}}{s^2+s\frac{g_m}{C_{gs}}+s\frac{g_m}{RC_{gs}C_{gd}}}\right), \quad g_m >> g_o, \quad C_{gs} >> C_{gd} \tag{4.101}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{RC_{gs}C_{gd}}} = \sqrt{f_t f_z} \tag{4.102}$$

$$f_z = \frac{1}{2\pi}\frac{1}{RC_{gd}} \tag{4.103}$$

$$f_t = \frac{g_m}{C_{gs}} \tag{4.104}$$

For $f_z < f < f_0$, Hara's topology exhibits inductive characteristics, the inductance L and parasitic series resistance R_s of nMOS Hara active inductors can be described by (neglecting C_{gd}, C_{ds}, and high-order effects) [22]

$$R_S = \left(\frac{g_m+\omega^2 RC_{gs}^2}{g_m^2+\omega^2 C_{gs}^2}\right) \tag{4.105}$$

$$L = \left(\frac{C_{gs}\left(R_{g_m}-1\right)}{g_m^2+\omega^2 C_{gs}^2}\right), \quad for\ L>0\ \left(g_m R >> 1\right) \tag{4.106}$$

From Equation (4.105) and Equation (4.106),

$$R_S = \left(\frac{\frac{1}{g_m}+\left(\frac{f}{f_t}\right)^2 R}{1+\left(\frac{f}{f_t}\right)^2}\right) \approx \frac{1}{g_m}, \quad L = \frac{R}{f_t\left[1+\left(\frac{f}{f_t}\right)^2\right]} \approx \frac{R}{f_t} \quad \left(for\ f << f_t\right) \tag{4.107}$$

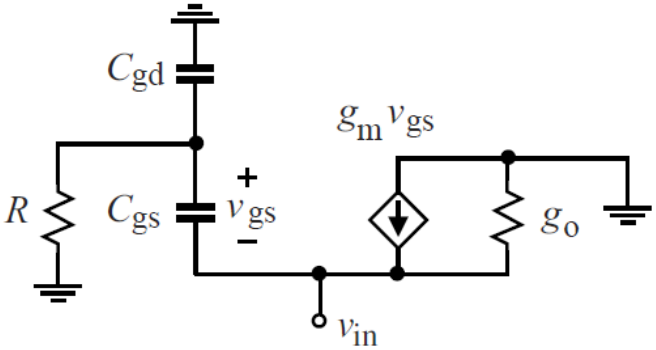


Figure 4-33 A simplified small-signal equivalent circuit of nMOS Hara active inductors shown in Figure 4-32.

From Equation (4.107), the inductance L is directly proportional to R and can be tuned by varying R, whereas series resistance R_s is dominated by g_m at frequencies below the cut-off frequency of the transistor ($f << f_t$).

4.4.1.5 Wu Folded Active Inductors

The drawback of Hara active inductors can be overcome by employing the Wu folded active inductor topology. Figure 4-34 and Figure 4-35 show the simplified schematic and small-signal equivalent nMOS version of Wu folded active inductors [45]-[46].

To simplify the analysis, the effect of C_{gd}, g_o and other parasitic capacitances of the transistor can be neglected for the calculation of input impedance, as given by [22]

$$Z(s)=\left[\frac{1+sRC_{gs}}{g_m+sC_{gs}}\right]_{s=j\omega} \tag{4.108}$$

$$Z(j2\pi f)=\left[\frac{1+j2\pi fRC_{gs}}{g_m+j2\pi fC_{gs}}\right]_{f<f_z}\approx\frac{1}{g_m} \tag{4.109}$$

From Equation (4.108), Z(s) has a zero at frequency $f_z=1/2\pi RC_{gs}$ and a pole at frequency $f_p=g_m/2\pi C_{gs}$. Figure 4-36 shows the network is resistive at low frequencies $f<f_z$ with resistance $R\approx 1/g_m$ and inductive when $f_z<f<f_p$. From Equation (4.108), the input admittance can be given by

$$Y_{in}(s)=\left[\frac{g_m+sC_{gs}}{1+sRC_{gs}}\right]_{s=j\omega}=\frac{1}{R}+\frac{1}{1\Big/\left(g_m-\frac{1}{R}\right)+sRC_{gs}\Big/\left(g_m-\frac{1}{R}\right)} \tag{4.110}$$

From Equation (4.108) and Equation (4.110), RLC equivalent circuit can be represented by a series RL network in parallel with a resistor R_p with

$$R_p=R \tag{4.111}$$

$$R_s=\frac{1}{\left(g_m-\frac{1}{R}\right)}\quad\left(R_s>0\quad for\ g_m>\frac{1}{R};\ R_s=\frac{1}{g_m}\quad for\ g_m>>\frac{1}{R}\right) \tag{4.112}$$

$$L=\frac{RC_{gs}}{\left(g_m-\frac{1}{R}\right)}\quad\left(L_s>0\quad for\ g_m>\frac{1}{R};\ L=\frac{RC_{gs}}{g_m}=\frac{R}{\omega_t}\quad for\ g_m>>\frac{1}{R}\right) \tag{4.113}$$

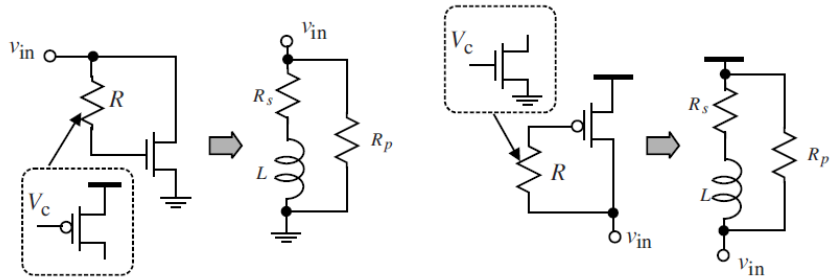


Figure 4-34 Typical simplified schematic of Wu folded active inductors.

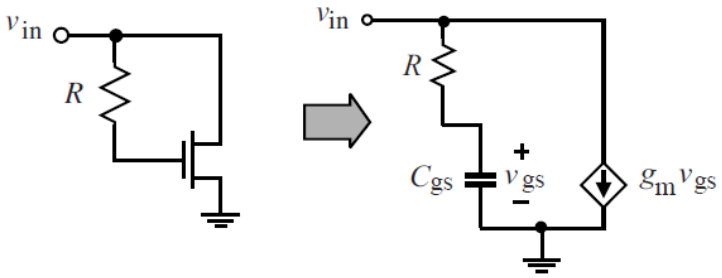


Figure 4-35 A typical small-signal equivalent circuit of the nMOS version of Wu folded active inductors.

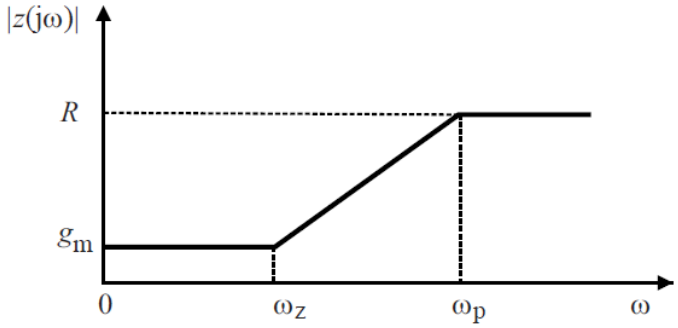


Figure 4-36 A typical input impedance characteristics of the nMOS version of Wu folded active inductors shown in Figure 4-35.

4.4.1.6 Karsilayan-Schaumann Active Inductors

Figure 4-37 and Figure 4-38 show the simplified schematic and small-signal equivalent circuit of the lossless Karsilayan-Schaumann active inductor. This consists of a differentially configured transconductor with a positive transconductance and a common-source transconductor with a negative transconductance [47]-[52]. Figure 4-38 shows the inductance of the synthesized inductor can be derived from the admittance of the active inductor assuming $gds = 0$ as [22]

$$Y = sC_{gs1}\frac{sC_{gs2}+g_{m2}}{s(C_{gs1}+C_{gs2})+(g_{m1}+g_{m2})}+\frac{g_{m2}g_{m3}}{sC_{gs3}}\frac{sC_{gs1}+g_{m1}}{s(C_{gs1}+C_{gs2})+(g_{m1}+g_{m2})} \quad (4.114)$$

$$Y = s\left(\frac{C_{gs}}{2}\right)+\frac{1}{s\left(\frac{2C_{gs3}}{g_m g_{m3}}\right)} \quad \left(for\ g_{m1}=g_{m2}=g_m\ and\ C_{gs1}=C_{gs2}=C_{gs}\right) \quad (4.115)$$

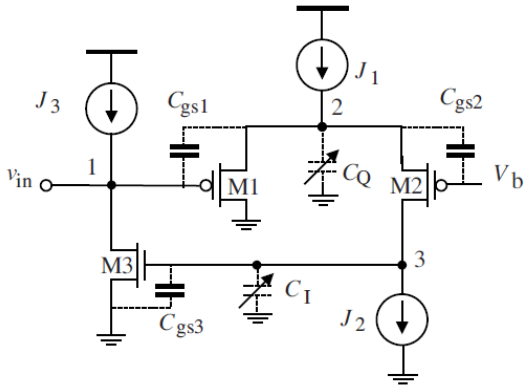


Figure 4-37 Simplified schematic of the Karsilayan-Schaumann active inductor.

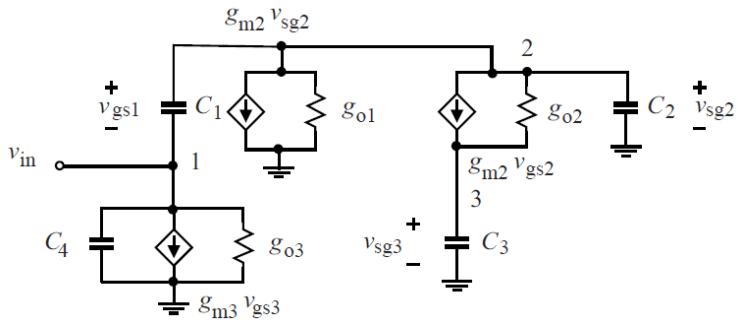


Figure 4-38 Small-signal equivalent circuit of Karsilayan-Schaumann active inductor.

From Equation (4-115), the active inductor can be represented by a capacitor in parallel with an inductor, and is described by

$$C_p = \frac{C_{gs}}{2} \tag{4.116}$$

$$L = \frac{2C_{gs3}}{g_m g_{m3}} \tag{4.117}$$

From Equation (4.115) to Equation (4.117), the differentially-configured transconductor with only one of its two input terminals connected has a transconductance $g_m/2$, whereas the capacitance encountered at the input node of the active inductor is given by $C_{gs}/2$ (as capacitors of C_{gs1} and C_{gs2} are connected in series). From Equation (4.117), the inductance of the active inductor can be increased by increasing the capacitance between the gate and source of M_3 by adding an auxiliary capacitor C_I in parallel with C_{gs3}, as shown in Figure 4-37. The auxiliary capacitor C_I can be implemented using MOS varactors for tuning the synthesized inductance and can be given by

$$L = \frac{2\left(C_{gs3} + C_I\right)}{g_m g_{m3}} \tag{4.118}$$

The preceding analysis excludes the effect of g_{ds} and other parasitic capacitances of the transistors. Without lossy conductance g_{ds}, the quality factor of the active inductor cannot be evaluated. From Figure 4-38, where C_1, C_2, C_3, and C_4 represent the total capacitances including both intrinsic and parasitic capacitances encountered at or between respective nodes, the admittance of the active inductor is given by [47]

$$Y \approx \frac{1}{j\omega\left(\frac{2C_3}{g_m g_{m3}}\right) + \frac{G(\omega)}{g_m g_{m3}}} \tag{4.119}$$

Where

$$G(\omega) = g_{o2} + 2g_{o4} - \omega^2 C_3\left(\frac{C_1 + C_2}{g_m}\right) \tag{4.120}$$

$$G(\omega) = 0 \rightarrow C_2 = \frac{\left(g_{o2} + 2g_{o4}\right)g_m}{\omega^2 C_3} - C_1 \tag{4.121}$$

From Equation (4.119), the active inductor can be represented by an inductor L with series resistance R_s

$$L = \left(\frac{2C_3}{g_m g_{m3}} \right) \tag{4.122}$$

$$R_s = \frac{G(\omega)}{g_m g_{m3}} \tag{4.123}$$

From Equation (4.122) and Equation (4.123), yield the quality factor of the active inductor and can be described by

$$Q \approx \frac{\omega L}{R_s} = \frac{2\omega C_3}{G(\omega)} \Rightarrow Q\big|_{G(\omega)=0} = \infty \tag{4.124}$$

High Q-factor, $(G(\omega) \to 0)$, this can be achieved by tuning an auxiliary capacitor C_Q at the source of M_1 and M_2, while the synthesized inductance is tuned by varying C_I the capacitance of the auxiliary capacitor added between the gate and source of M_3 as shown in Figure 4-37. This can lead to independent tuning features of Q and L of the synthesized active inductor as shown in Figure 4-37. Recent publications reported that the quality factor of the active inductor is close to 400 and the typical synthesized inductor value exceeded 600nH in a 0.5μm CMOS implementation [22], [47].

To reduce the silicon area and increase the speed, the synthesized inductor topology is implemented in TSMC-0.18μm CMOS technology using all nMOS transistors (excluding bias current sources), which offers self-resonant frequency of 6.68 GHz and a quality factor of 106 (Figure 4-39) [51]. To boost the transconductance from g_{m3} to g_{m3} + g_{m4}, the common-source configured transconductor of the preceding Karsilayan-Schaumann active inductor was replaced with a static inverter as shown in Figure 4-40 [53, 54]. The synthesized inductance is tuned by varying C_Q while the quality factor is independently tuned by changing C_I. Care must be taken for ensuring M_3 and M_4 are in the saturation while setting the input voltage of the static inverter so that $V_{IL} \leq v2 \leq V_{IH}$ where V_{IL} and V_{IH} are the lower and upper voltage bounds of the transition region of the static inverter, respectively. However, the disadvantage of this approach is the constraint imposed on the voltage swing of node 2 of the synthesized active inductor.

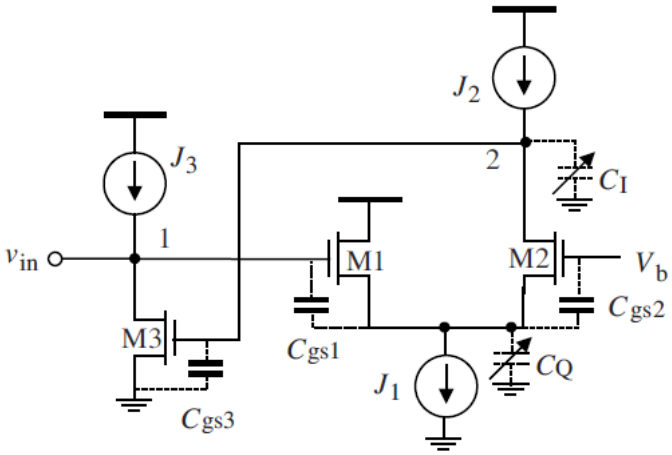


Figure 4-39 A typical schematic of the Karsilayan-Schaumann active inductor using nMOS transistors only.

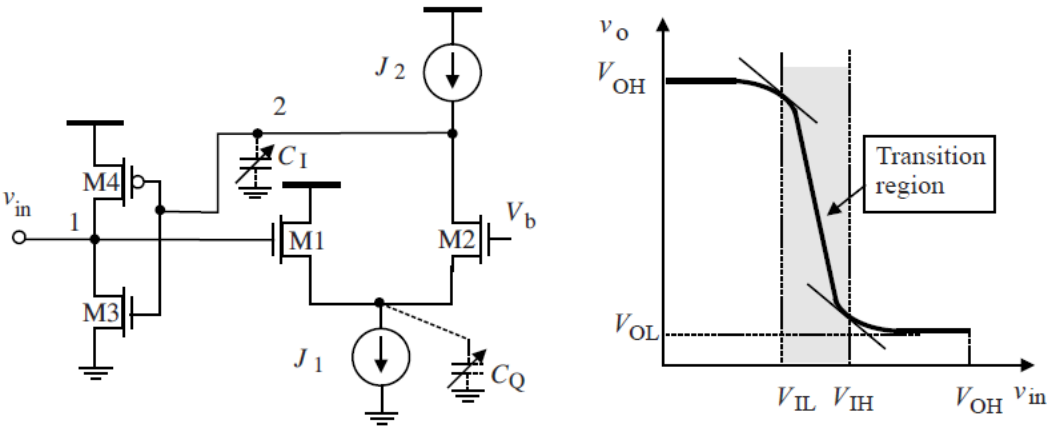


Figure 4-40 A simplified schematic of the Karsilayan-Schaumann active inductor using a static inverter negative transconductor.

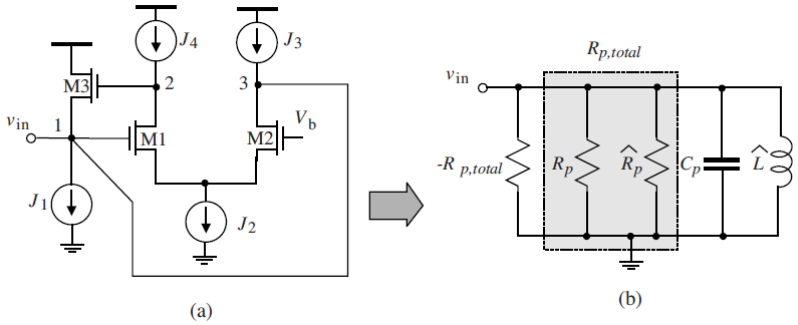
4.4.1.7 Yodprasit-Ngarmnil Active Inductors

Figure 4-41 shows the simplified schematic and equivalent RLC representation of the Yodprasit-Ngarmnil synthesized active inductor topology. From Equation (4.125) to Equation (4.127) describe the equivalent circuit. To improve the quality factor, the effect of both R_s and R_p should be compensated by incorporating negative resistor $-R_{p,total}$ in parallel so that net loss resistance either vanishes or become negative (Figure 4-41b). The L and R_s series branch of the RLC equivalent circuit (Figure 4-17) can be equivalently transformed into $\hat{L}$ and $\hat{R}_p$ parallel branch shown in Figure 4-41 (b) as

$$\hat{R}_p = R_p\left(1+Q^2\right) \tag{4.125}$$

$$\hat{L} = L\left(1+Q^{-2}\right) \tag{4.126}$$

$$R_{p,total} = \hat{R} \,//\, R_p \tag{4.127}$$



Figures 4-41 (a) Simplified schematic of Yodprasit-Ngarmnil active inductor, and (b) equivalent RLC representation of synthesized active inductor topology.

In general, negative resistors are realized by a positive feedback approach as shown in Figure 4-41 (a) in which electrical connection between the input terminal of the active inductor and the drain of M_2 forms the required positive feedback condition. The impedance at the gate of M_1 at low frequencies can be described by [22]

$$Z_{in} \approx -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right) \tag{4.128}$$

Considering $g_{o,}$ the Q-factor of the Yodprasit-Ngarmnil active inductor is given by [55]

$$Q = \frac{\sqrt{g_{m1}g_{m3}C_{gs1}C_{gs3}}}{\frac{C_{gs1}}{r_{o1}} + 2\frac{C_{gs3}}{r_{o3}}} \tag{4.129}$$

From Equation (4.129), Q can be tuned by either varying $g_{m1,3}$ or $r_{o1,3}$. The former also changes inductance so the preferred choice is to vary the r_o of M_1 and M_2 . This can be realized by varying the gate voltage of M_4 and M_5 in cascode configuration of the differential-pair transconductor as shown in Figure 4-42, where $ro1$ and $ro2$ now become $(gm_4ro_4)r_{o1}$ and $(g_{m5}r_{o5})r_{o2}$, respectively. As shown in Figure 4-42, Q was tuned up to 12000 in a 0.6μm implementation where transconductances $g_{m4,5}$ can be tuned by varying the gate voltage of $M_{4,5}$ [55].

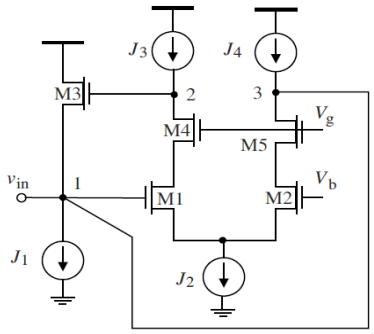


Figure 4-42 Schematic of the cascode Yodprasit-Ngarmnil active inductors.

4.4.1.8 Uyanik-Tarim Active Inductor

Figure 4-43 shows the schematic of the Uyanik-Tarim active inductor topology where M_1 and J form a transconductor with a negative transconductance g_{m1}, $M_{2,3,4}$ form a transconductor with a positive transconductance $\frac{g_{m2}\, g_{m4}}{g_{m3}} = g_{m2}$, provided that M_3 and M_4 are identical [56]. The reported topology is attractive for low-voltage applications. To facilitate inductance tuning without affecting the parasitic series resistance that controls the quality factor of the synthesized active inductor, a tuning diode (varactor C) is incorporated at the gate of M_2. The reported quality factor of the active inductor is typically over 100 in the frequency range 4.8-6.4 GHz with its phase error less than 1 degree in UMC-0.13μm 1.2V CMOS technology [56].

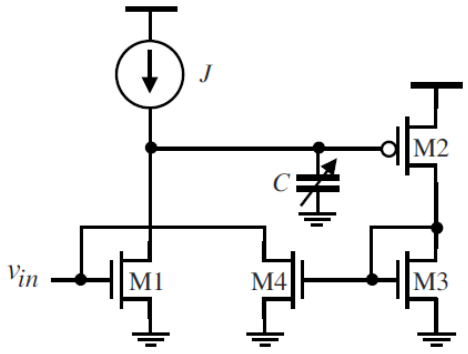


Figure 4-43 Schematic of the Uyanik-Tarim active inductor.

4.4.1.9 Thanachayanont-Payne Cascode Active Inductors

Figure 4-44 shows the schematic of the Thanachayanont-Payne cascode active inductor for improved Q factor and operating bandwidth [30, 31, and 58]. This occurs because cascode configured transistors are insensitive to the Miller effect and thus, has no effect on the bandwidth. Moreover, cascode configurations can effectively expand the frequency range of active inductors by lowering the lower bound of the frequency range of active inductors. The minimum supply voltage of the active inductor without the cascode is given by $V_T + 2V_{sat}$, whereas, for the cascode topology as shown in Figure 4-44(b) and Figure 4-44 (c) it is given by $2V_T + V_{sat}$ and $V_T + 2V_{sat}$ respectively.

From Figure 4-44, with $g_m \gg g_0$ (for simplification in analysis) the impedance of the synthesized cascode active inductor can be described by

$$[Z(s)]_{g_m \gg g_0} \approx \left[\left(\frac{g_{01}g_{03}}{C_{gs1}C_{gs2}g_{m3}}\right)\frac{\left[s\left(\frac{C_{gs2}g_{m3}}{g_{01}g_{03}}\right)+1\right]}{s^2+s\left(\frac{g_{01}g_{03}}{C_{gs2}g_{m3}}+\frac{g_{01}}{C_{gs1}}\right)+\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}\right], \quad (s=j\omega) \tag{4.130}$$

From Equation (4.130), the self resonant frequency (SRF) and frequency of the zero of Z can be given by

$$[f_z]_{without\ cascode} = \frac{1}{2\pi}\left[\frac{g_{01}}{C_{gs2}}\right] \tag{4.131}$$

$$[f_z]_{with\ cascode} = \frac{1}{2\pi}\left[\left(\frac{g_{01}}{C_{gs2}}\right)\left(\frac{1}{r_{03}g_{m3}}\right)\right] \tag{4.132}$$

$$f_0 = \frac{1}{2\pi}\left[\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}\right] = \sqrt{f_{t1}f_{t2}} \tag{4.133}$$

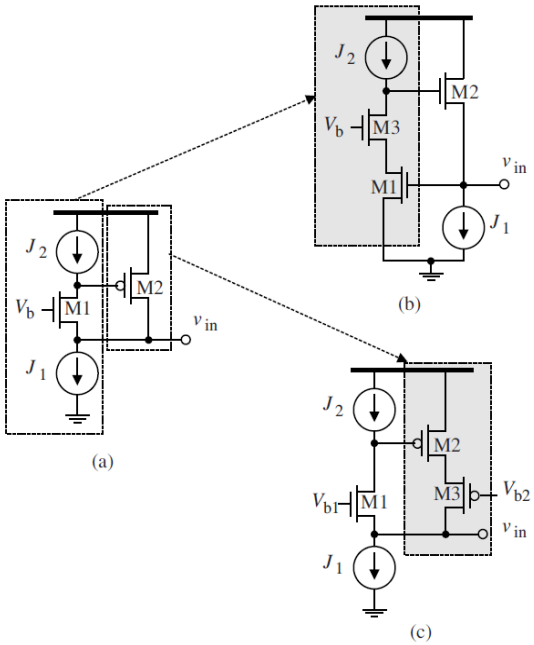


Figure 4-44 Schematic of Thanachayanont-Payne cascode active inductors: (a) Basic active inductor, (b) simplified schematic of Thanachayanont-Payne cascode active inductors, and (c) equivalent Thanachayanont-Payne cascode active inductors.

The RLC equivalent network of the Thanachayanont-Payne cascode topology can be determined by analyzing the admittance as

$$R_p = \frac{1}{g_{02}} \tag{4.134}$$

$$C_p = C_{gs1} \tag{4.135}$$

$$R_s = \left(\frac{g_{01}}{g_{m1}g_{m2}}\right)\left(\frac{1}{g_{m3}r_{03}}\right) = \left(\frac{g_{01}g_{03}}{g_{m1}g_{m2}g_{m3}}\right) \tag{4.136}$$

$$L = \left(\frac{C_{gs2}}{g_{m1}g_{m2}}\right) \tag{4.137}$$

From Equation (4.134) to Equation (4.137), the parasitic series resistance is reduced from $R_s = \left(\frac{g_{01}}{g_{m1}g_{m2}}\right)$ without cascode to $R_s = \left(\frac{g_{01}}{g_{m1}g_{m2}}\right)\left(\frac{1}{g_{m3}r_{03}}\right)$ with the cascode. The parallel resistance is increased from $R_p = \frac{1}{g_{m1}}$ without cascode to $R_p = \frac{1}{g_{02}}$ with the cascode while marinating identical value of synthesized inductance L. The quality factor can be described for cases as [22]

$$Q \approx \frac{2\pi fL}{R_s} = 2\pi f C_{gs2} r_{01} \quad (with\ cascode: R_s \rightarrow \text{dominates}) \tag{4.138}$$

$$Q \approx \frac{R_p}{2\pi fL} = \frac{g_{m2}}{2\pi f C_{gs2}} \quad (with\ cascode: R_p \rightarrow \text{dominates}) \tag{4.139}$$

$$Q \approx \frac{2\pi fL}{R_s} = 2\pi f C_{gs2} r_{01}(g_{m3}r_{03}) \quad (without\ \ cascode: R_s \rightarrow \text{dominates}) \tag{4.140}$$

$$Q \approx \frac{R_p}{2\pi fL} = \frac{g_{m2}}{2\pi f C_{gs2}}(g_{m1}r_{01}) \quad (without\ \ cascode: R_p \rightarrow \text{dominates}) \tag{4.141}$$

4.4.1.10 Weng-Kuo Cascode Active Inductors

Figure 4-45 shows schematic of the Weng and Kuo cascode active inductor topology using a current-reuse mechanism to eliminate the drawback of the Thanachayanont-Payne cascode, where the inductance and quality factor cannot be tuned independently [59]. As shown in Figure 4-45, g_{m1} is proportional to $J_1 + J_3$ while g_{m3} is only proportional to J_1.
From Equation (4.133) and Equation (4.137)

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} = \sqrt{f_{t1}f_{t2}} \tag{4.142}$$

$$Q \approx \frac{2\pi fL}{R_s} = \frac{g_{m3}}{g_{01}g_{03}}\sqrt{\frac{C_{gs2}g_{m1}g_{m2}}{C_{gs1}}} \tag{4.143}$$

From Equation (4.142), f_o can be tuned by varying g_{m1} and g_{m2} whereas the *Q-factor* can be independently tuned by varying g_{m3} only.

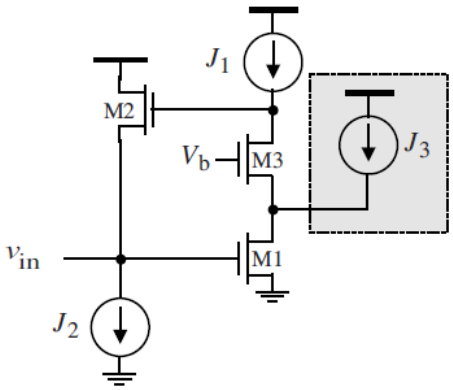


Figure 4-45 Schematic of the Weng-Kuo active inductor topology

4.4.1.11 Manetakis Regulated Cascode Active Inductors

Figure 4-46 shows the typical schematic of regulated cascode active inductor topology. The performance of the Weng and Kuo cascode active inductor can be improved by minimizing series resistance *Rs* by using regulated cascode and multi-regulated cascode techniques [60]. The RLC equivalent circuit of the regulated cascode active inductor can be given by [22]

$$C_1 = C_{gs2} \tag{4.144}$$

$$C_2 = C_{gs1} \tag{4.145}$$

$$G_{o1} = \frac{1}{g_{01}(g_{m3}r_{03})(g_{m4}r_{04})} \tag{4.146}$$

$$G_{o2} = g_{o2} \tag{4.147}$$

From Equation (4.144) to Equation (4.147),

$$R_p = \frac{1}{G_{02}} \tag{4.148}$$

$$C_p = C_2 \tag{4.149}$$

$$R_s = \left(\frac{G_{01}}{g_{m1}g_{m2}}\right) \tag{4.150}$$

$$L = \left(\frac{C_1}{g_{m1}g_{m2}}\right) \tag{4.151}$$

Since $f_z = \frac{1}{2\pi}\frac{G_{01}}{C_1}$ and $f_o = \frac{1}{2\pi}\frac{1}{\sqrt{LC_p}}$, the lower bound of the frequency is reduced while the upper bound of the frequency range remains unchanged. The RLC equivalent circuit of the multi-regulated cascode gyrator-C active inductor can be described by

$$C_1 = C_{gs2} \tag{4.152}$$

$$C_2 = C_{gs1} \tag{4.153}$$

$$G_{o1} = \frac{1}{g_{01}(g_{m3}r_{03})(g_{m4}r_{04})(g_{m5}r_{05})} \tag{4.154}$$

$$G_{o2} = g_{o2} \tag{4.155}$$

It can be noticed from Equation (4.152) to Equation (4.155) that the lower bound of the frequency is further reduced while the upper bound of the frequency range remains unchanged [22].

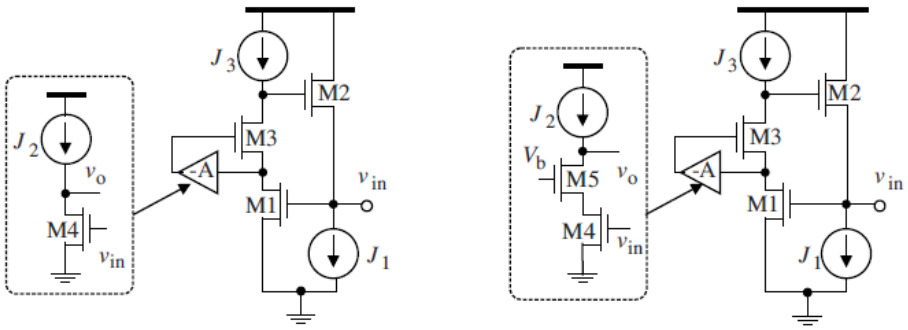


Figure 4-46 Schematic of the Manetakis regulated and multi-regulated cascode active inductors. (a) Regulated cascode active inductors, and (b) Multi-regulated cascode active inductors.

The CAD simulation results of cascode active inductors, regulated cascode active inductors and multi-regulated cascode active inductors given in [60] demonstrated that regulated cascode reduced the lower frequency bound of active inductors by one decade while multi-regulated cascode further reduced the lower frequency bond by more than one decade [22].

4.4.1.12 Hsiao Feedback Resistance Cascode Active Inductors

As discussed earlier cascode configured active inductors offer a high Q-factor and a wide frequency range. By incorporating feedback resistance, the Q-factor of the synthesized active inductor can be further improved [61]-[63]. Figure 4-47 shows the typical schematic of the feedback resistance configured synthesized active inductor circuits. Considering that the biasing current source transistors M_n and M_p are ideal, the equivalent RLC network can be characterized by

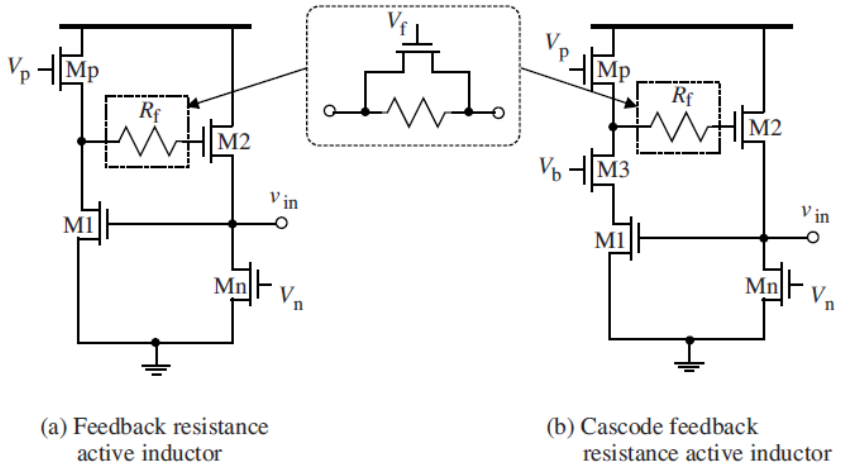
$$R_p = \frac{R_f g_{o2}+1}{2g_{o2}+R_f g_{o2}^2} \rightarrow R_p = \left[\frac{R_f g_{o2}+1}{2g_{o2}+R_f g_{o2}^2}\right]_{R_f=0} \approx \frac{1}{g_{o2}} \tag{4.156}$$

$$C_p = C_{gs3} \tag{4.157}$$

$$R_s = \left[\frac{g_{m1}g_{o2}g_{o3}+\omega^2[g_{m2}C_{gs1}^2-g_{m1}C_{gs1}C_{gs2}(R_f g_{o2}+1)]}{g_{m1}^2 g_{m2}g_{m3}+\omega^2 g_{m2}g_{m3}C_{gs1}^2}\right]_{R_f=0} \approx \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}} \tag{4.158}$$

$$L = \left[\frac{g_{m1}g_{m2}C_{gs1}+\omega^2 C_{gs1}C_{gs2}(R_f g_{o2}+1)]}{g_{m1}^2 g_{m2}g_{m3}+\omega^2 g_{m2}g_{m3}C_{gs1}^2}\right]_{R_f=0} \rightarrow L \approx \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{4.159}$$

From Equation (4.156) to Equation (4.159), added the feedback resistor R_f lowers R_s and increases L simultaneously, thus improving the quality factor but at the cost of SRF (self-resonant frequency). It should be noted that the SRF with the feedback resistors R_f is reduced due to the increase of L. However, varying the bias voltage V_p of the current-source transistor *Mp,* can compensate the SRF to some extent [64]-[66].



(a) Feedback resistance active inductor

(b) Cascode feedback resistance active inductor

Figure 4-47 Schematic of Hsiao feedback resistance active inductors: (a) Feedback resistance active inductor, and (b) Cascode feedback resistance active inductor.

The feedback resistor R_f does not consume any static power and can be tuned by connecting a nMOS transistor in parallel with a poly resistor. Liang et al improved the Hsiao considering of Figure 4-47 (b) by replacing the cascode portion of the active inductor with a regulated cascode branch, as shown in Figure 4-48 to incorporate the advantages of the regulated cascode active inductor investigated in Figure 4-46 [67].

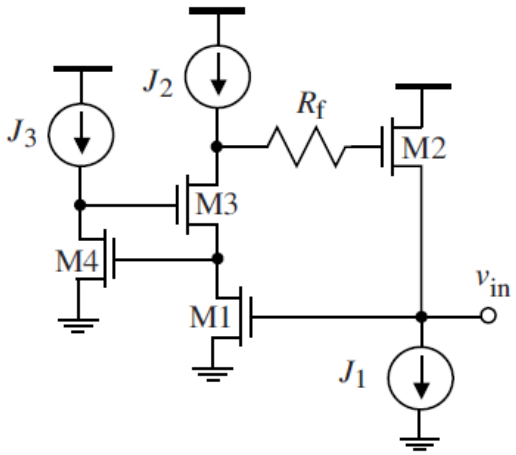


Figure 4-48 Simplified schematic of Liang feedback resistance regular cascode active inductors.

4.4.1.13 Abdalla Feedback Resistance Active Inductors

Karsilayan-Schaumann active inductor topologies discussed in Figure 4-37 offer independent tunability features of Q-factor and synthesized inductance values. Figure 4-48 shows the modified Karsilayan-Schaumann topology by incorporating a feedback resistor between the two transconductors of the active inductor to improve the quality factor of the synthesized inductor [68]. As shown in Figure 4-48, the added feedback resistor increases the inductance of the active inductor and at the same time minimizes the parasitic series resistance, thereby improving Q. It can be seen in Figure 4-49 that C_I and C_Q are MOS varactors to tune the inductance and quality factor, respectively.

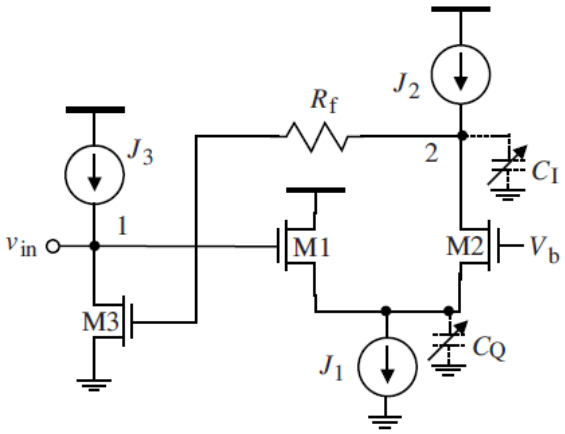


Figure 4-49 Schematic of the single-ended Abdalla feedback resistance active inductors.

4.4.1.14 Nair Active Inductors

Figure 4-50 shows the typical schematic of the Nair active inductor with a negative feedback network consisting of R_1, R_2, and C_2 in cascode configuration for low-power, low-noise and ultra wideband amplifier applications [69]-[70]. The RC network consists of R_1, R_2 $-C_2$ as shown in Figure 4-50 is a typical negative feedback network that reduces the parasitic resistances of the synthesized Nair active inductor. The parameters of this synthesized active inductor can be described by

$$L = \frac{(C_3+C_{gs3})}{g_{m1}g_{m3}} \tag{4.160}$$

$$\mathrm{f}_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m3}}{C_{gs1}(C_3+C_{gs3})}} \tag{4.161}$$

$$\mathrm{Q}(\mathrm{f}_0) = \sqrt{\frac{g_{m1}g_{m3}(C_3+C_{gs3})}{C_{gs1}g_{o1}^2}} \tag{4.162}$$

From Equation (4.161) and Equation (4.162), C_3 is incorporated to improve the Q factor but it increases the synthesized inductance at the cost of reduced SRF.

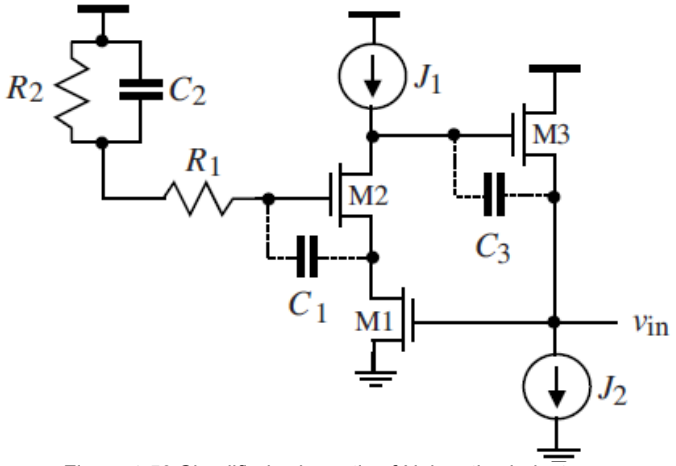


Figure 4-50 Simplified schematic of Nair active inductors.

4.5 Implementation of Differential Active Inductors

4.5.1 Lu Floating Active Inductors

Figure 4-51 shows the typical schematic of the differentially configured Lu floating active inductor circuit [72]. All the transistors are biased in saturation except M_5 and M_6, which are biased in the triode region and act as a voltage controlled resistors whose resistances are controlled by the gate voltage V_b[22]. The basis of negative feedback can be described as follows: an increase in v_{1+} and a decrease in v_{1-} results in an increase in v_{2+} and a decrease in v_{2-} due to the common-gate operation of $M_{1,2}$ The source followers of $M_{3,4}$ ensure that v_{1+} and v_{1-} will be reduced proportionately.

For simplification in analysis, M_5 and M_6 can be represented with channel conductances g_{ds5} and g_{ds6} in the small-signal equivalent circuit of the active inductor depicted in Figure 4-51.

The equivalent RLC parameters can be described in terms of the differential input impedance as given by [22]

$$Z(j\omega) = \frac{2[j\omega(C_{gs1}+C_{gs3})-g_{m1}+g_{ds5}]}{g_{ds5}[g_{m1}+g_{m3}+j\omega(C_{gs1}+C_{gs3})]} \tag{4.163}$$

$$R_p = \frac{2}{g_{ds5}} \tag{4.164}$$

$$R_s = \left[\frac{2(g_{ds5}-g_{m1})}{g_{ds5}(2g_{m1}+g_{m3}-g_{ds5})}\right] \Rightarrow R_s > 0 \; for \; [(2g_{m1} + g_{m3}) > g_{ds5} \text{ and } g_{ds5} > g_{m1}] \tag{4.165}$$

$$L = \frac{2(C_{gs1}+C_{gs3})}{g_{ds5}(2g_{m1}+g_{m3}-g_{ds5})} \Rightarrow L_s > 0 \; for \; [(2g_{m1} + g_{m3}) > g_{ds5} \text{ and } g_{ds5} > g_{m1}] \tag{4.166}$$

The inductance of the synthesized active inductor can be tuned by varying V_b, and subsequently g_{ds5}. Therefore, an increase in V_b will push M_5 and M_6 from the triode region towards the saturation region, lowering g_{ds5} and g_{ds6}, resulting in the increased inductance values.

4.5.2 Grozing Floating Active Inductors

Figure 4-52 shows the typical schematic of the differentially configured Grozing Floating Active Inductor circuit [73]-[74]. The floating synthesized active inductor topology incorporates two basic differential-pair transconductors, where two negative resistors are connected across the output nodes of the transconductors to cancel out the parasitic resistances of the active inductor.

By adjusting the tail currents of the differential pairs $J_{1,2,}$ transconductances can be varied, resulting in a change in the inductance values. By varying the tail current sources $J_{3,4}$, the magnitude of negative resistance changes, resulting in tuned Q-factor [22].

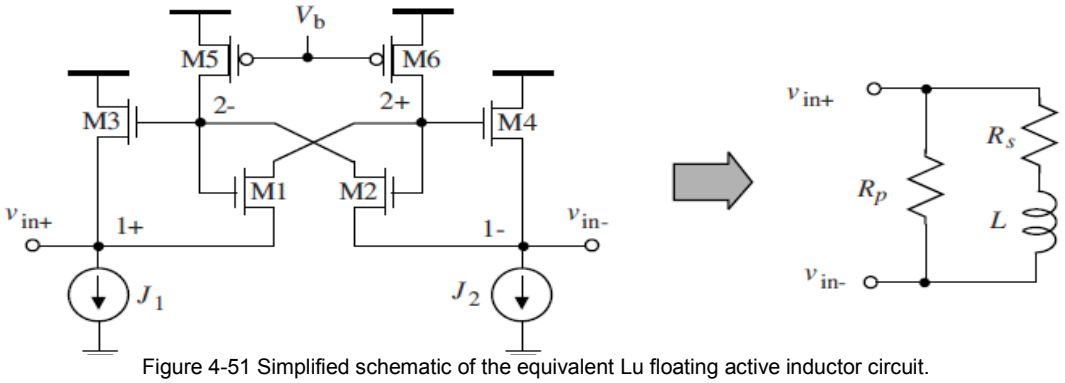


Figure 4-51 Simplified schematic of the equivalent Lu floating active inductor circuit.

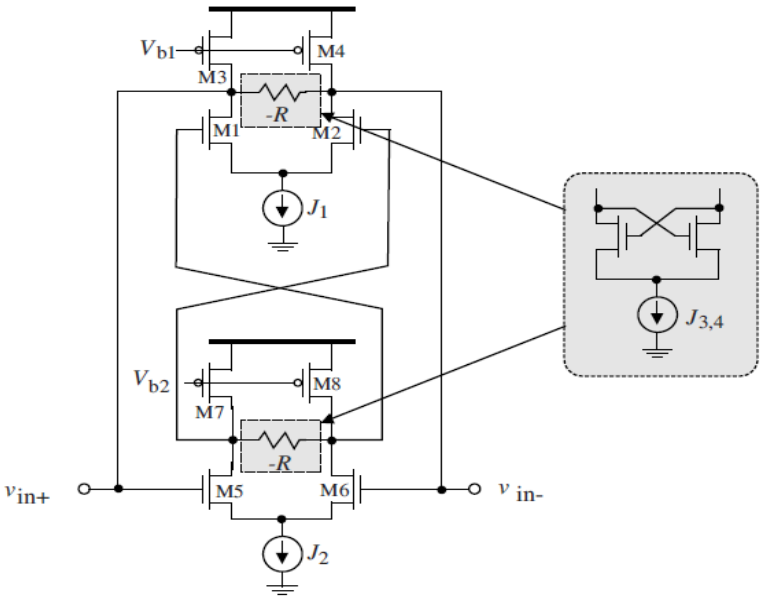


Figure 4-52 Schematic of Grozing floating active inductor circuit

4.5.3 Thanachayanont Floating Active Inductors

Figure 4-53 shows the typical schematic of the cascode-configured floating active inductor circuit [28]-[31]. $M_{4,5}$ form a negative resistance to cancel out the parasitic resistances of the active inductor to improve the Q-factor (the resistance of the negative resistor cannot be tuned in this implementation) [47]-[48] . By adjusting J_2 the inductance of the synthesized active inductor can be tuned.

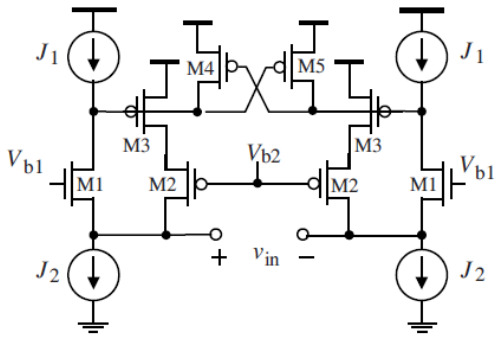


Figure 4-53 Schematic of Thanachayanont floating active inductor circuit.

4.5.4 Mahmoudi-Salama Floating Active Inductors

Figure 4-54 shows the typical schematic of the Mahmoudi-Salama Floating Active Inductors circuit that consists of a pair of differential transconductors and a pair of negative resistances at the output of the transconductors [76]-[77]. $M_{8,16}$ are biased in the triode region and behave as voltage-controlled resistors. These are incorporated to the conventional cross-coupled configuration of negative resistances to provide the tunability of the resistance without using a tail current source [22].

Figure 4-54(b) shows the small-signal equivalent circuit of the tunable negative resistance where a test voltage source V_x is added for the derivation of the equivalent resistance of the negative resistor, and R represents the resistance of M_8. From circuit theory, KCL (Kirchhoff current law) at nodes 1 and 2 yields:

$$g_{m1}V_2 + \frac{V_x}{R} - I_x = 0 \quad (node\ \#1) \tag{4.167}$$

$$g_{m1}(V_x + V_2) - \frac{V_x}{R} + I_x = 0 \quad (node\ \#2) \tag{4.168}$$

$$Z = \frac{V_x}{I_x} = -\frac{R\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)}{R-\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)} \rightarrow Z = R \parallel -\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right) \tag{4.169}$$

By assuming that nodes A and B are the virtual ground and neglecting C_{gd} and the diffusion junction capacitances, the inductance of the synthesized active inductor as shown in Figure 4-54 can be given by

$$L = \frac{C}{g_{m1}g_{m2}} \approx \frac{C_{gs2,3,10,11}}{g_{m1}g_{m2}}, \tag{4.170}$$

$$\text{where } C \approx \frac{C_{gs2,3,10,11}}{g_{m1}g_{m2}} \tag{4.171}$$

where $2C$ is the total capacitance encountered at each of the output nodes of the transconductor, $g_{m1}\ and\ g_{m2}$ are the transconductances of the differential transconductors 1 and 2, respectively.

4.5.5 Feedback Resistance Floating Active Inductors

Figure 4-55 shows the typical schematic of the feedback resistance floating active inductor circuit that consists of 2 basic differential-pair transconductors and two feedback resistors [78]-[79].

As shown in Figure 4-55 (a), the characteristics of the added feedback resistors is same as that of the single-ended active inductor, discussed earlier, i.e. they lower the parasitic series resistance and increase the inductance [22].

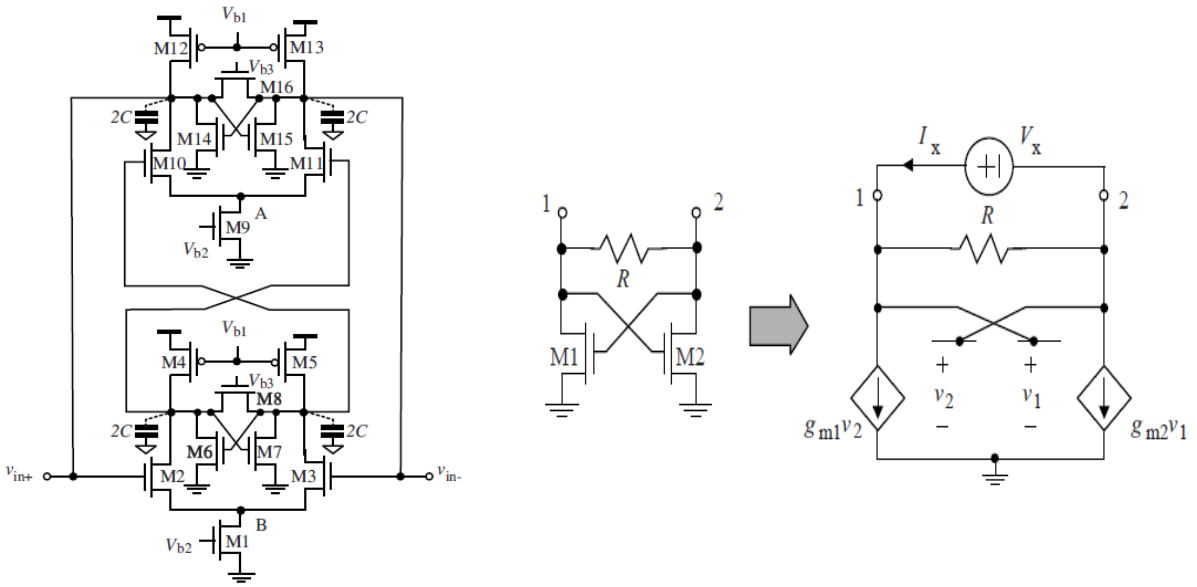
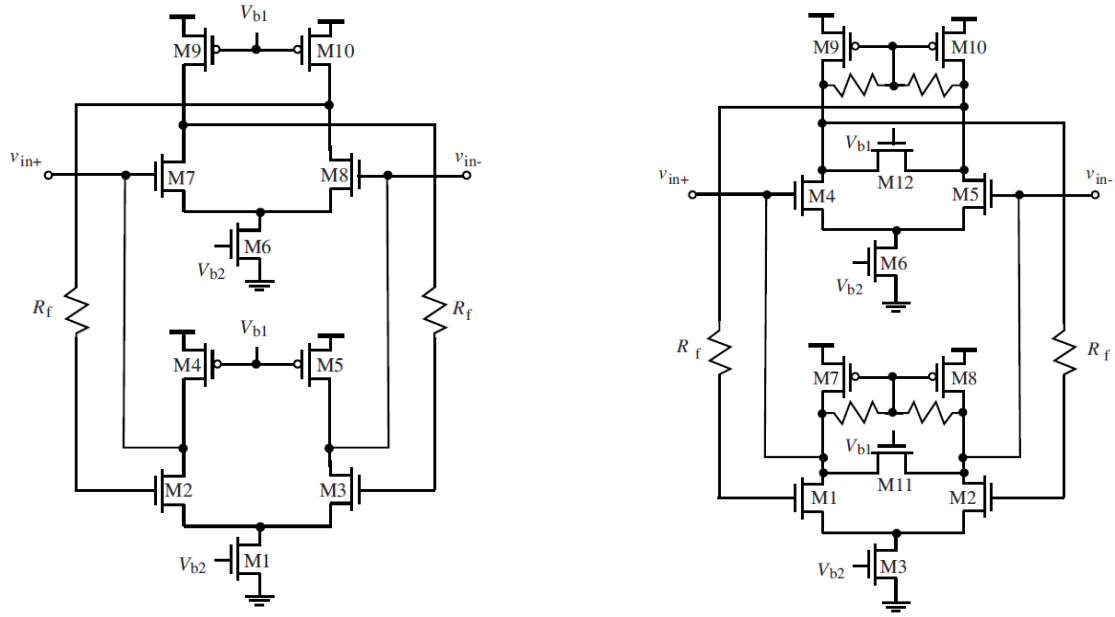


Figure 4-54 A typical Mahmoudi-Salama floating active inductor: (a) simplified schematic, and (b) small-signal equivalent representation of Mahmoudi-Salama floating active inductor circuit (g_o of the transistors is neglected for the simplification).



(a) Simplified schematic of feedback resistance floating active inductor circuit,

(b) Simplified schematic differential feedback resistance floating active inductor circuits

Figure 4-55 Akbari-Dilmaghani active inductor: (a) feedback resistance floating active inductor circuit, and (b) differential feedback resistance floating active inductor circuit

Figure 4-55 (b) shows the simplified schematic of the differential feedback resistance floating active inductor topology where $M_{11,12}$ are biased in the triode region and behave as voltage-controlled resistors. The equivalent inductance and the parasitic series resistance of the floating active inductor are given by

$$L = \frac{C+C_{gs4,5}\left(1+\frac{R_f}{R_T}\right)}{g_{m1,2},g_{m4,5}} \tag{4.172}$$

$$R_s = \frac{\frac{1}{R_T} - \omega^2 C_{gs4,5} C R_f}{g_{m1,2}, g_{m4,5}} \quad (4.173)$$

where

$$C = C_{gd7,8} + C_{db1,2} + C_{db7,8} + C_{gs1,2} \quad (4.174)$$

$$R_T = R_f \parallel R_{ds11,12} \parallel r_{o1,2} \parallel r_{o7,8} \quad (4.175)$$

From Equation (4.172) to Equation (4.175), $M_{11,12}$ controls the series resistance R_s(by adjusting V_{b1}, R_s can be minimized), R_f improves L and lowers R_s simultaneously, thus improving the performance of the floating synthesized active inductor [22].

4.5.6 Class AB Active Inductors

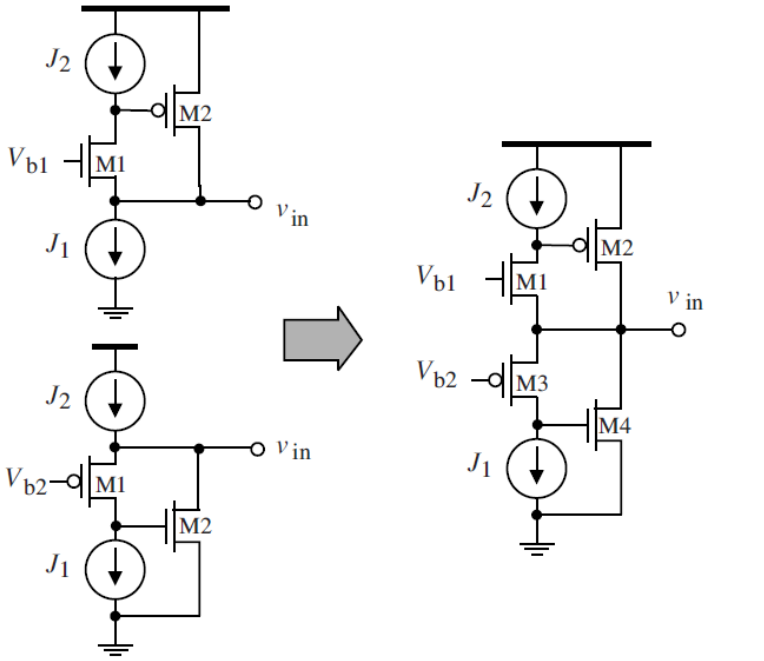
A typical class-A active inductor topology suffers from a drawback of a small voltage swing at the terminals of the active inductor circuits. To increase the voltage swing of the active inductor without sacrificing linearity, class-AB configuration can be employed. A typical class-AB active inductor can be constructed from a nMOS-configured class-A active inductor and a pMOS-configured class-A active inductor, as shown in Figure 4-56 [30].

In presence of high input voltage, nMOS class-A active inductor is activated, whereas, when input voltage is low, pMOS class-A active inductor is activated, therefore, both active inductor networks are operated in an interleave manner, thus exhibits an inductive characteristic over a large input voltage range. Table 4.4 describes the class-A and class-AB operation based on swing of the input voltage and the minimum supply voltage.

It can be noticed that the need for a large minimum supply voltage of class-AB active inductors makes them less attractive for low-voltage applications. As shown in Figure 4-56 (b), class-AB active inductor topology is limited in frequency range and loaded quality factor. Figure 4-57 shows the typical cascode topology for improving the Q-factor and increases the operating frequency range. Floating cascode class-AB active inductor can also be constructed in a similar manner as that of non-cascode floating active inductor, as shown in Figure 4-58. For improving the performance, negative resistance compensation techniques can be employed to class-AB active inductor for broadband high dynamic range operations.

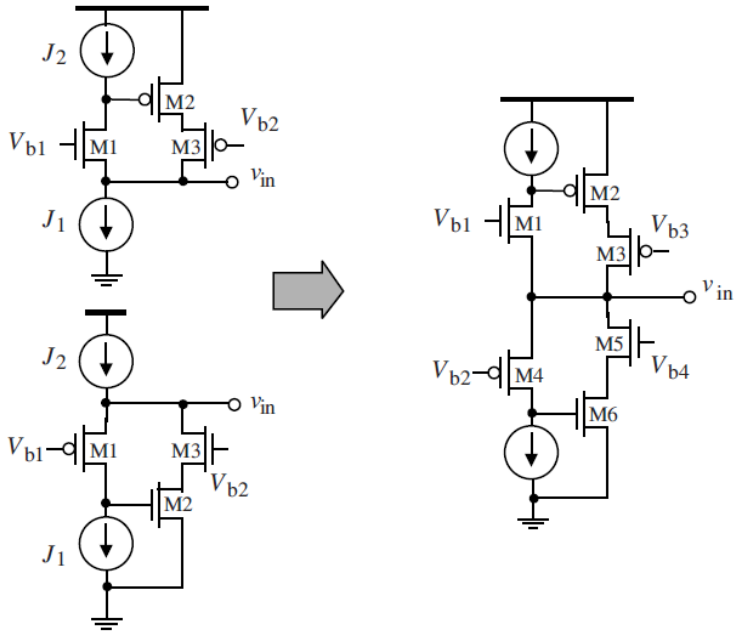
Table 4.4 A comparison of the input voltage swing and the minimum supply voltage of class-A and class-AB active inductors

	Class-A (nMOS)	Class-A (pMOS)	Class-AB
$V_{in,min}$	V_{sat}	$V_T + V_{sat}$	0
$V_{in,max}$	$V_{DD} - (V_T + V_{sat})$	$V_{DD} - V_{sat}$	V_{DD}
$V_{DD,min}$	$V_T + 2V_{sat}$	$V_T + 2V_{sat}$	$2V_T + 2V_{sat}$



(a) Class A active inductors (b) Class AB active inductor

Figure 4-56 Schematic of the Thanachayanont-Ngow class AB active inductor circuit



(a) Cascode class A active inductors (b) Cascode class AB active inductor

Figure 4-57 Schematic of the Thanachayanont-Ngow cascode class AB active inductor topology.

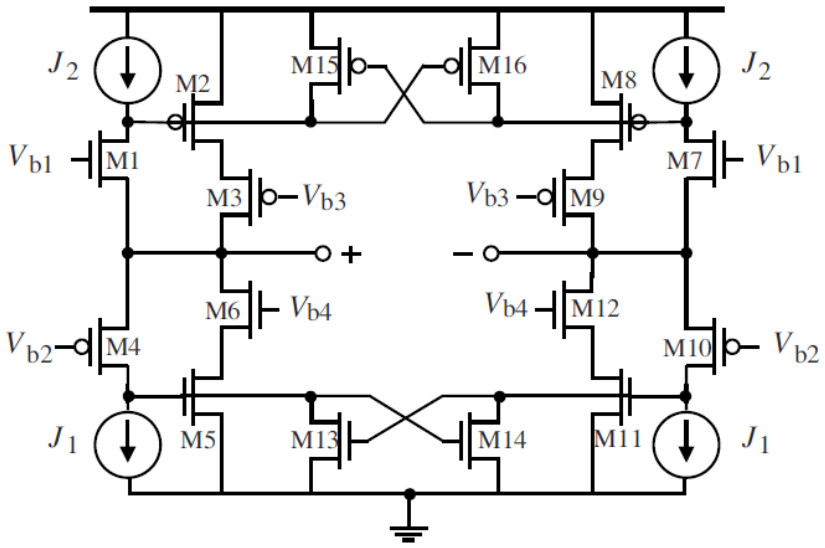


Figure 4-58 Schematic of the Thanachayanont-Ngow cascode floating class AB active inductors topology.

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5. Active Inductor Oscillators (AIOs)

The applications of tunable active inductor oscillators are confronted with two main difficulties: a high level of phase noise and a limited dynamic range. An in-depth research in these areas and novel circuit topologies are critically needed in order to lower the phase noise and improve the dynamic range prior to a large-scale deployment of AIOs in applications where passive inductors are currently dominating. In general, the applications of AIOs fall into two categories: (i) the active inductor circuit replaces the inductor in the LC oscillator, and (ii) the oscillator is implemented by the active inductor directly.

5.1 Embedded Active Inductor into LC Oscillator

Figure 5-1 shows the typical circuit of an LC oscillator where the synthesized floating active inductor replaces the passive inductor in the LC oscillator [1]. As shown in Figure 5-1, two single-ended active inductors consisting of Q_1, Q_2, Q_3 and Q_4, Q_5, Q_6 are combined together to form a floating active inductor and the oscillation frequency can be varied by controlling the bias voltage (V_{tune}).

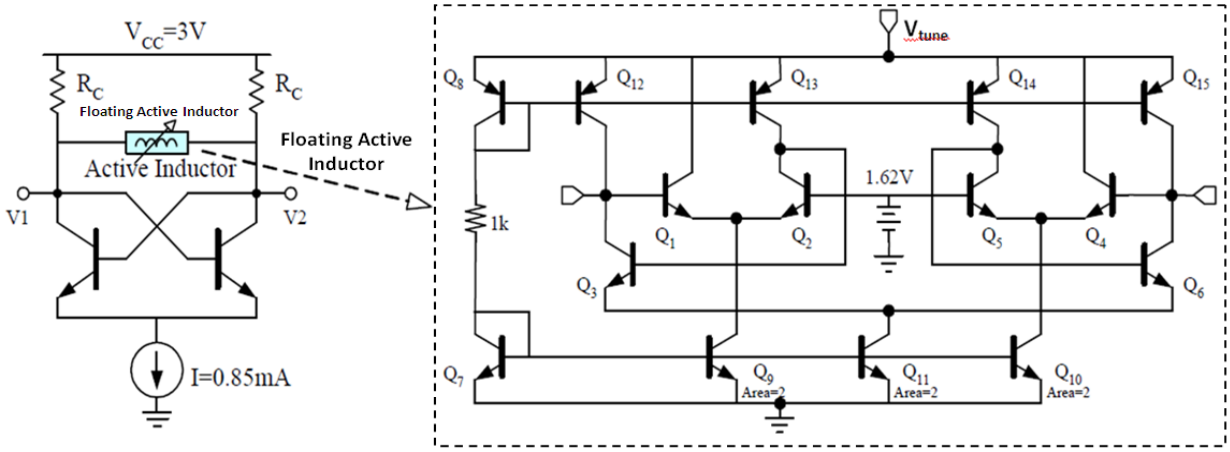

Figure 5-1 A typical schematic of an *LC* VCO using synthesized embedded active inductor in a LC oscillator topology

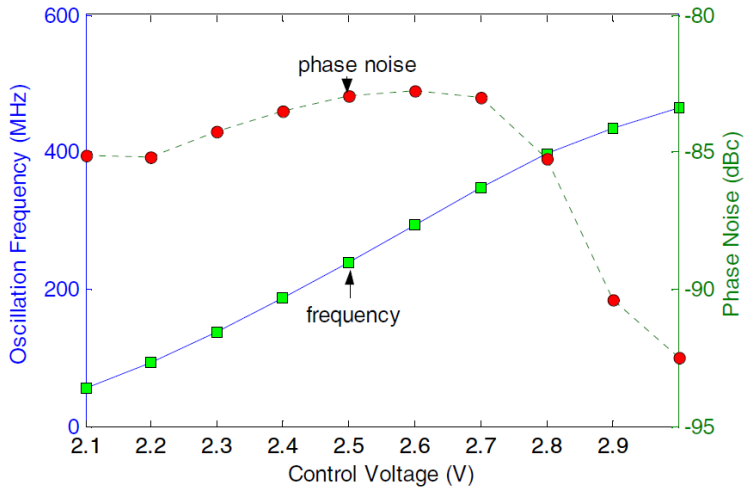

Figure 5-2 CAD simulated tuning and phase noise characteristics (at 1MHz offset) as a function of V_{tune} of the active inductor VCO circuit shown in Figure 5-1(*RC* = 3.3k).

Active inductor based oscillators usually have a very large tuning range but poor linearity. However, because the synthesized inductance is controlled by bias current, it makes a cost-effective alternative to the varactor tuned oscillator and is also well suited for MMIC VCOs. Figure 5-2 shows the simulated tuning and phase noise characteristics (at 1MHz offset) with a wide tuning range (typically more than 150%) for 2.1V to 3V bias tuning (V_{tune}). Note that, although the active inductors provide broadband tuning capability and compact chip area, the excessive power consumption and poor phase noise limits its application in oscillator design. Since the phase noise degradation is the most critical performance shortfall, ATI's do not find any application unless this is partially or fully compensated using new techniques at radio frequencies. The overall power dissipation is 36mW if the bias voltage (V_{tune}) is chosen as 3V. However, the active inductor consumes 28.2mW, which is approximately 80 % of the total power dissipation.

Figure 5-3 shows the simulated performance characteristics of a synthesized active inductor based *LC* oscillator. The oscillation frequency is 465MHz. The differential output voltage amplitude is about 180mVrms, and the phase noise is –92.49dBc/Hz at 1MHz offset from the carrier. As seen from the Figure 5-3(b), the phase noise performance of embedded synthesized active inductor oscillator is relatively poor in comparison with the *LC* oscillator using passive inductors [2]-[8]. By adjusting the bias voltage (V_{tune}) and load resistor (R_C) of the cross-coupled transistors, phase noise can be minimized (the dependence is shown in Figure 5-4).

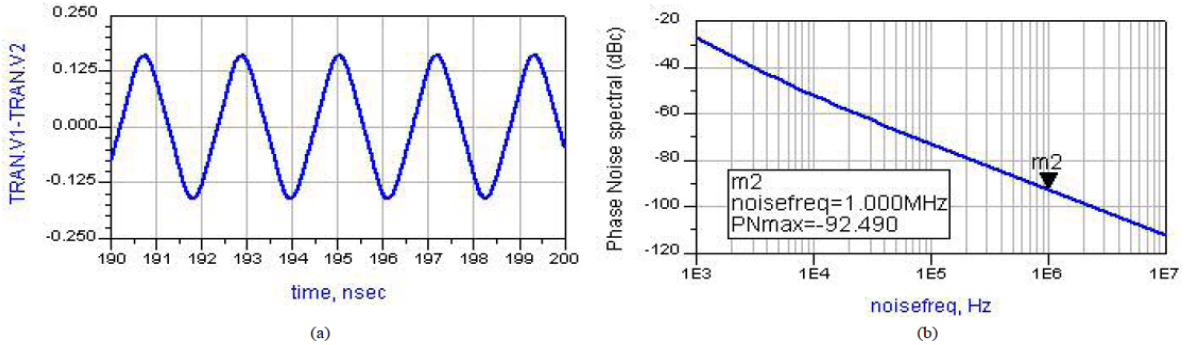

Figure 5-3 CAD simulated plots: (a) differential output voltage waveform, and (b) phase noise characteristics

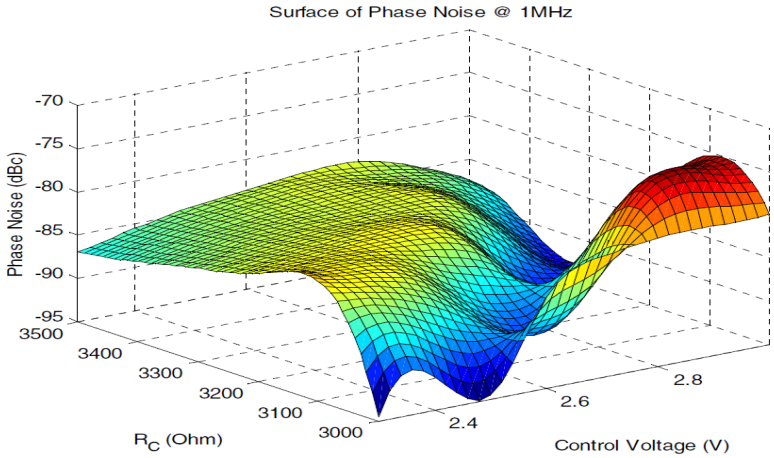

Figure 5-4 Phase noise characteristics as a function of tuning bias control voltage V_{tune} and the load of the cross-coupled transistors *RC* at 1MHz offset frequency.

5.2 Active Inductor Acts as an Oscillator

Figure 5-5 shows the typical single-ended active inductor that consists of Q_1, Q_2 and Q_3 bipolar transistor. Figure 5-6 shows simplified small signal equivalent circuit of the active inductor circuit (the bipolar transistor is modeled by C_π, r_π, g_m and r_b). The input impedance Z_{in} is given by

$$Z_{in} = \left[\frac{(1+j\omega Z_{\pi 1} r_{b1})(g_{m2}+j\omega Z_{\pi 2})+(1+j\omega Z_{\pi 2} r_{b2})(g_{m1}+j\omega Z_{\pi 1})}{j\omega Z_{\pi 1}(g_{m2}+j\omega Z_{\pi 2})+\frac{g_{m2}g_{m3}(g_{m1}+j\omega Z_{\pi 1})}{j\omega Z_{\pi 3}}}\right],\ where\ Z_{\pi i} = \left[\frac{r_{\pi i} C_{\pi i}}{r_{\pi i}+C_{\pi i}}\right]_{i=1,2,3} \quad (5.1)$$

$$Z_{in} = Re[Z_{in}] + jIm[Z_{in}] = \left[\frac{-2\omega^2 Z_\pi^2 r_b}{g_m^2-\omega^2 Z_\pi^2} + j\frac{2\omega Z_\pi}{g_m^2-\omega^2 Z_\pi^2}\right]_{(g_{mi}=g_m\ \&\ Z_{\pi i}=Z_\pi)} \quad (5.2)$$

$$Re[Z_{in}] = -\left(\frac{2\omega^2 Z_\pi^2 r_b}{g_m^2-\omega^2 Z_\pi^2}\right) \Rightarrow Re[Z_{in}]_{g_m \gg \omega^2 Z_\pi^2} \quad (5.3)$$

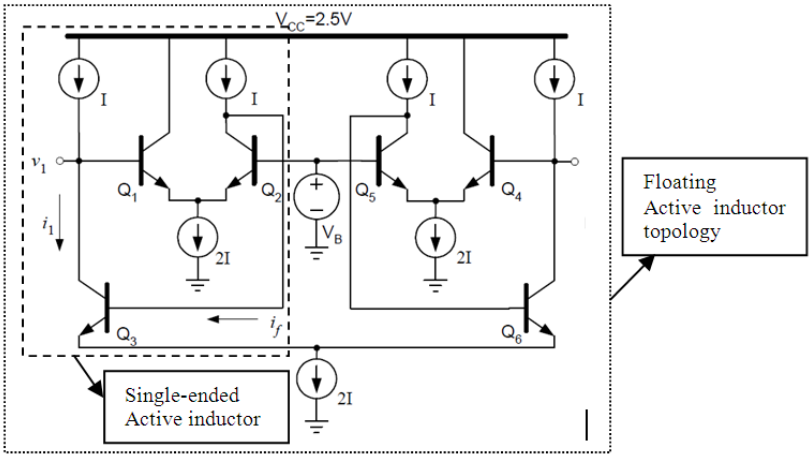

Figure 5-5 A typical schematic of a single-ended active inductor circuit (using bipolar transistors Q1, Q2 and Q3) part of the floating active inductor configuration.

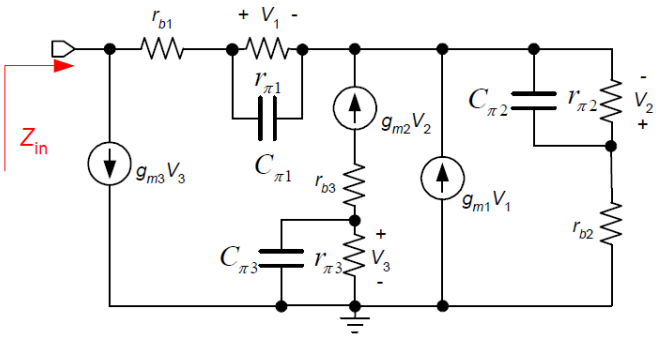

Figure 5-6 Small-signal model of the active inductor circuit of Figure 5-5

From Equation (5.3), the real part of the input impedance is negative for large value of g_m. Such a circuit is potentially unstable and may oscillate with the proper bias. Figure 5-7 shows a typical single-ended active inductor oscillator for a comparative analysis [1]. Figure 5-8 shows the simulated output signal and phase noise plots. The oscillation condition is successfully established (f_0 = 476 MHz) with less power (29 mW) compared to embedded active inductor in the LC oscillator of Figure 5-1 at the cost of poor phase noise performance.

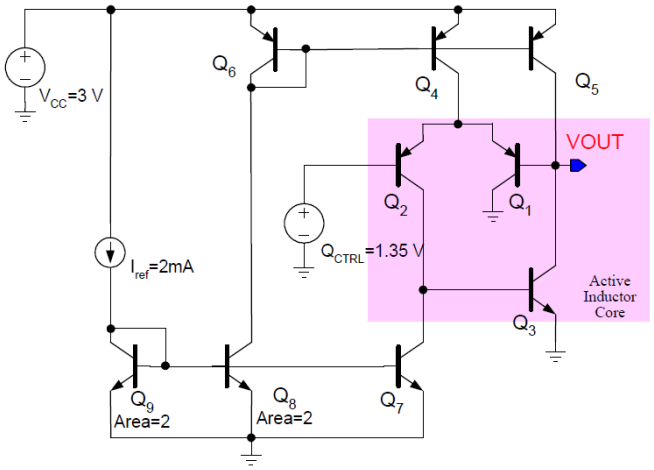

Figure 5-7 Schematic of a synthesized single-ended active inductor oscillator

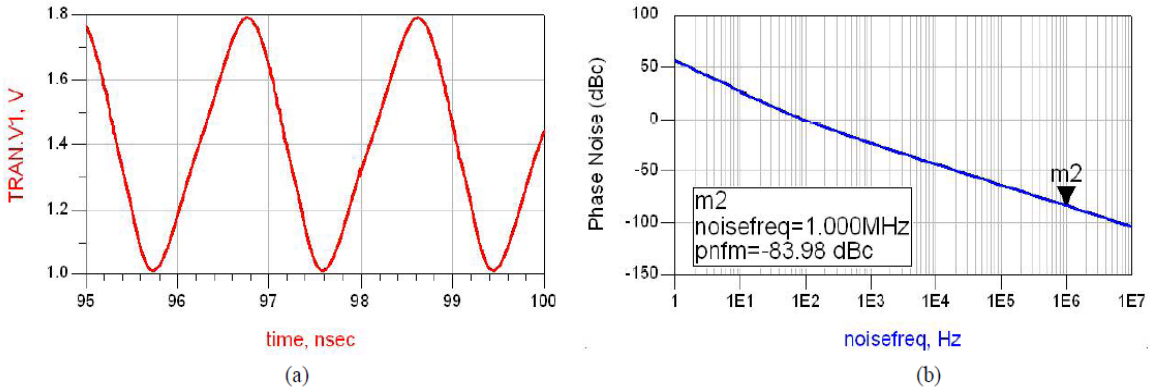

Figure 5-8 Simulated plots of synthesized single-ended active inductor oscillator: (a) output waveform, and (b) phase noise characteristics

It can be seen that only the transistors and capacitors (if necessary) realize active inductor-based oscillators. Thus, it is possible to achieve very compact designs in term of the chip area. However, the phase noise performance is relatively poor due to the lack of the narrow band resonant circuit. Note that noise generated by the active devices in the active inductors significantly deteriorates the phase noise even if the synthesized active inductor has a very high *Q* factor.

The quality factor of the active inductor-based resonator is tuned by varying the DC bias currents of the compensating negative resistance. Because the variation of the DC bias currents of the negative resistance usually affects the DC bias currents of the transconductors, the resonator tuning characteristics and the Q factor are coupled.

5.3 Resonator Noise Dynamics

Resonators are essential component of any signal-generating source to provide high spectral purity frequency references for modern wireless applications. RF resonators typically use a passive inductor and capacitor for storing electromagnetic energy. However, on-chip spiral inductors are notorious for their low quality factor (Q) and the large chip area they occupy. As a

result, RF resonators are usually implemented off-chip, a process that adds extra cost and manufacturing time to the design cycle.

Unlike on-chip spiral inductors, active inductors have smaller die area, larger inductance, higher-quality factor (Q), broadband tunability, and lower cost. Unfortunately, active inductor resonators have some disadvantages,

- poor phase noise performance
- poor linearity
- limited dynamic range
- power hungry, and
- sensitive to process, voltage supply, and temperature (PVT) variation compared to passive spiral inductors.

With proper design based on noise cancellation and filtering techniques, the noise contribution from the active inductor can be reduced to its minimum level for integrable low cost and low phase noise oscillator applications. The concept of active inductor resonators are not by any means a new approach for resonator tank circuits. They have been reported throughout the short history of electronics [9]-[15]. However, to the author's knowledge no publication gives a design guideline to minimize the shortcomings of to the active inductor to the application of tunable oscillators. Methods for understanding active inductor noise generation and its partial or eventual cancellation are presented with the goal of obtaining low phase noise.

Monolithic microwave integrated circuit (MMIC) technology realizes large inductances using spiral or stacked spiral inductors [8]. Unfortunately, these inductors can suffer from excess series resistance and undesirable high-frequency resonances. Thus, the spiral inductors can place a fundamental limit on the performance of an associated circuit. As a result a considerable amount of interest has been shown in the use of active inductors. Active inductors can be classified into two groups: (1) passive inductor with resistive loss compensating circuits, and (2) active inductor using phase shift and feedback techniques realized by transistors [11]-[36].

5.3.1 LC Resonator and Noise Dynamics

Figure 5-9 shows the typical passive unloaded LC resonator (series and parallel modes) including noise sources associated with the loss resistance.

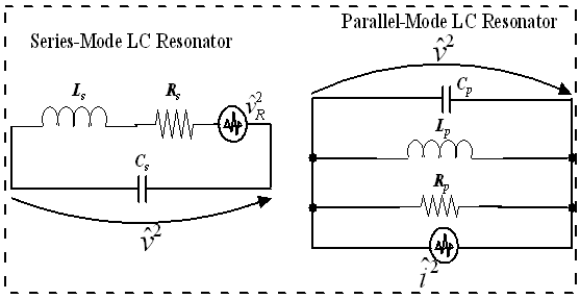

Figure 5-9. A representation of an unloaded LC resonator including noise sources associated with the loss resistance

The expression of the noise voltage at the output is given by the product of the noise source voltage and the noise transfer function as

$$\hat{v}^2 = \frac{\hat{v}_{Rs}^2}{[(1-\omega^2 LC)^2 + \omega^2 R_s^2 C^2]} = \frac{4kTR_s}{[(1-\omega^2 LC)^2 + \omega^2 R_s^2 C^2]} \tag{5.4}$$

$$\hat{v}^2\Big|_{\omega\to\omega_0} = \frac{4kTR_s}{[(1-\omega_0^2 LC)^2 + \omega_0^2 R_s^2 C^2]_{\omega_0 = 1/\sqrt{LC}}} = \frac{4kTR_s}{\omega_0^2 R_s^2 C^2} = 4kTR_s Q_0^2 \tag{5.5}$$

The net RMS output noise voltage of an unloaded passive LC resonator can be given by

$$\overline{v^2} = \int_0^\infty \hat{v}^2 df = \frac{2kTR_s}{\pi} \int_0^\infty \frac{d\omega}{[(1-\omega_0^2 LC)^2 + \omega_0^2 R_s^2 C^2]} \tag{5.6}$$

$$\overline{v^2} = \left(\frac{2kTR_s}{\pi}\right)\left(\frac{\pi}{2}\right)\left(\frac{1}{R_s C}\right) = \frac{kT}{C} \tag{5.7}$$

If the unloaded passive LC resonator is to be used as a resonator tank of an oscillator circuit, it is always loaded by the, tuning network, bias network, source and load impedances and other components (active and passive).

Figure 5-10 shows the equivalent representation of a loaded LC resonator including noise sources associated with the loss resistance. For simplification the parallel-mode LC resonator and injected output noise current sources are used instead of the output noise voltages, as the former are independent of loading.

The output noise current of a passive LC resonator is

$$\hat{i}^2 = \frac{4kT}{R_p} = \frac{4kTR_s}{R_s^2 + \omega^2 L^2}, \quad R_p = R_s + \frac{\omega^2 L^2}{R_s} \tag{5.8}$$

$$\hat{v}^2 = \hat{i}^2 |Z_n|^2 = \frac{4kTR_s}{\left(1 + \frac{R_s}{R_{Load}} - \omega^2 LC^2\right)^2 + \omega^2\left(R_s C + \frac{L}{R_{Load}}\right)^2} \tag{5.9}$$

Where $(L_P = L_S, C_P = C_S \quad \text{for} \quad Q >> 1)$

$$\hat{v}^2\Big|_{\omega_0} = \frac{4kTR_s}{\left(\frac{R_s}{R_{Load}}\right)^2 + \omega_0^2\left(R_s C + \frac{L}{R_{Load}}\right)^2} \tag{5.10}$$

$$\hat{v}^2\Big|_{\omega_0} = \frac{4kTR_s}{\left(\frac{1}{Q_0 Q_{ext}}\right)^2 + \left(\frac{1}{Q_0} + \frac{1}{Q_{ext}}\right)^2} = \frac{4kTR_s}{\left(\frac{1}{Q_0 Q_{ext}}\right)^2 + \left(\frac{1}{Q_l}\right)^2} \approx 4kTR_s Q_l^2 \tag{5.11}$$

$$\frac{1}{Q_l} = \left(\frac{1}{Q_0} + \frac{1}{Q_{ext}}\right), \quad Q_{ext} = \frac{R_{Load}}{\omega L}, Q_l = Q_0 \text{for} Q_{ext} \to \infty \tag{5.12}$$

The total RMS output voltage of loaded resonator is

$$\overline{v^2} = \int_0^\infty \hat{v}^2 df = \frac{2kTR_s}{\pi} \int_0^\infty \frac{d\omega}{\left(1 + \frac{R_s}{R_{Load}} - \omega^2 LC^2\right)^2 + \omega^2\left(R_s C + \frac{L}{R_{Load}}\right)^2} \tag{5.13}$$

$$\overline{v^2} = \frac{kT}{C}\frac{1}{\left(1+\frac{R_s}{R_{Load}}\right)\left(1+\frac{L}{R_{Load}R_sC}\right)} \Rightarrow \frac{kT}{C}(R_{Load}\to\infty) \tag{5.14}$$

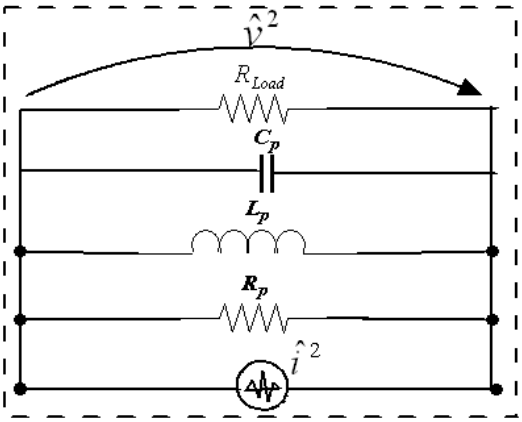

Figure 5-10 A passive LC resonator with loading including noise sources associated with the loss resistance R_P

From Equation (5.14), the noise associated due to the resonator loss can be compensated by adding negative resistance across the loaded resonator. By definition, a negative resistor is a circuit element where voltage applied across its terminal creates in-phase current of the opposite direction. Regardless of the resonator type, there are two approaches for compensating the resonator losses: series compensation and parallel compensation.
Figure 5-11 shows the typical arrangement of series and parallel compensation methods for passive LC resonators [9]. Figure 5-12 shows the typical configuration of a series-mode active resistor using a simple 3-port transistor, where negative resistance is seen at any of the three ports if the remaining two of the ports are terminated with suitable impedances.

In terms of noise, active negative resistors can be regarded as passive resistors whose noise voltage and current spectral densities are [10]

$$\hat{v}_n^2 = 4kTr_a|R_a|, \quad R_a = -R \tag{5.15}$$

$$\hat{i}_n^2 = 4kTg_a|G_a|, \quad G_a = -G \tag{5.16}$$

$$\hat{i}_n^2 = 4k\,T\lambda\,g_m \tag{5.17}$$

$\lambda = 0.5\ (Bipolar), \lambda = 0.67\ (JFET), \lambda = 0.12\ (MESFET)$ where R_a and G_a are the negative resistance and conductance values. The relative noise resistance r_a can be defined:

$$r_a = \lambda\frac{Z_3}{Z_1} \tag{5.18}$$

From Equation (5.17) and Equation (5.18), the noise can be minimized by minimizing the reactance Z_3 and maximizing Z_1, but keeping their product constant for unchanged negative resistance.

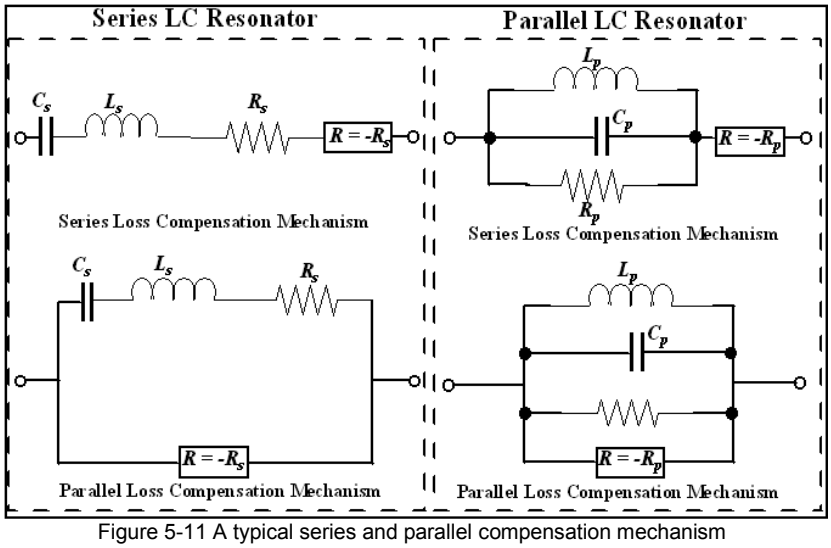

Figure 5-11 A typical series and parallel compensation mechanism

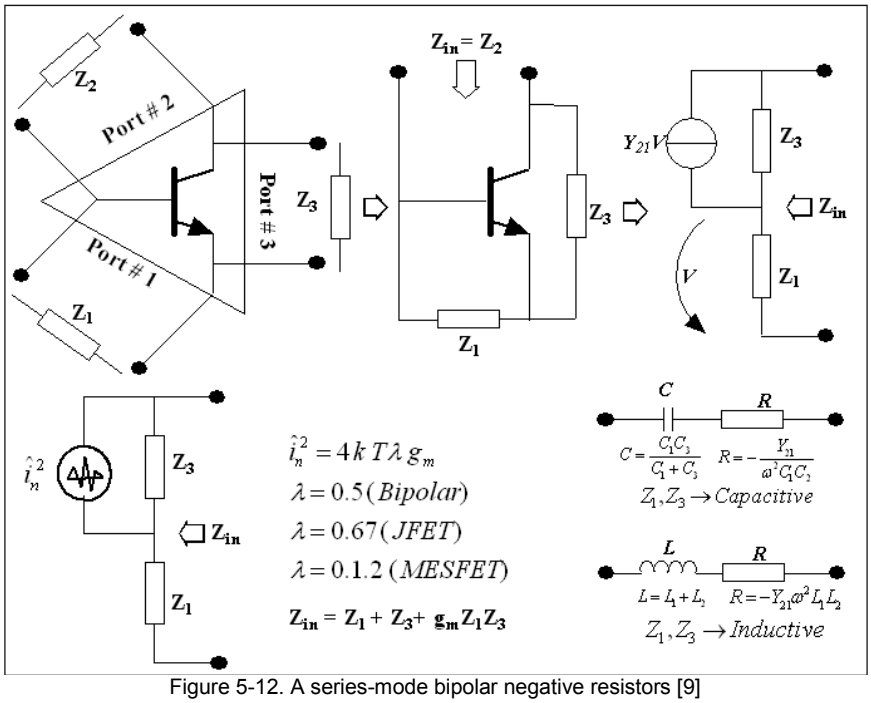

Figure 5-12. A series-mode bipolar negative resistors [9]

The coefficients r_a and g_a are relative noise resistance and conductance, respectively. They give a comparative estimate of how much more or less noise the active negative resistor produces relative to a passive positive resistor of the same value. It is worth noting from Equation (5.18), that an active negative resistor can be less noisy with proper selection of the reactance ratio than its passive counterpart ($r_a<1$).

This is one of the main reasons why negative resistance resonators are superior to other active resonator types in terms of noise. Nevertheless, noise characteristics, i.e. losses, of the actual passive LC resonator components may have a greater effect on the overall noise performance than the loss compensating active circuits. Figure 5-13 shows the small-signal representation of parallel mode single-transistor negative resistance circuit with transistor noise sources.

The expression of input admittance is given by

$$Y_{in} = [Z_1 + Z_2]^{-1} + \left[\frac{1}{g_m}\left(1 + \frac{Z_2}{Z_1}\right)\right]^{-1} \tag{5.19}$$

The relative noise conductance is used as a measure of noise performance.

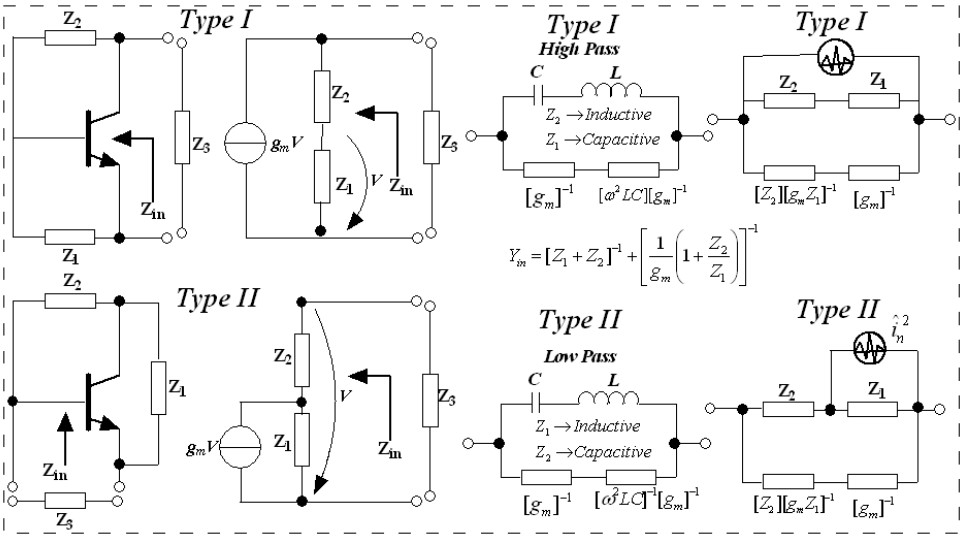

Figure 5-13 A typical small signal equivalent representation of parallel mode single-transistor negative resistance circuits

For the type-I case, the noise source links directly to the output noise current, and can be described by

$$g_n = \lambda\left|1 + \frac{Z_2}{Z_1}\right| = \lambda(m^2 - 1), \quad m = \frac{\omega}{\omega_{sr}} \tag{5.20}$$

for a high-pass negative resistor where Z_2 is inductive, Z_1 is capacitive and ω_{sr} is their mutual resonating frequency. The relative noise conductance rises with increasing frequency and the best results are obtained near the self-resonance of the LC pair. The type II of parallel-mode circuits is suited for low-noise applications, as its relative noise conductance deduces is

$$g_n = \lambda\left|1 + \frac{Z_2}{Z_1}\right|^{-1} = \lambda(m^2 - 1)^{-1} \tag{5.21}$$

From Equation (5.21), the noise reduces rapidly with increasing frequency, and is the right candidate for the synthesized low-noise parallel mode negative resistance for tunable active inductor oscillator applications.

5.4 Oscillator Phase Noise Dynamics

For phase noise analysis, the oscillator is considered as a feedback system and a noise source is present in the input as shown in the Figure 5-14.

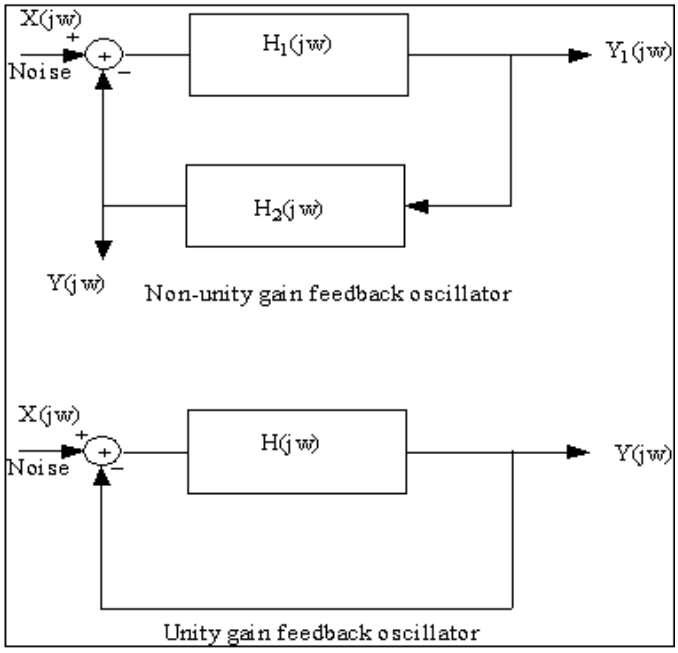

Figure 5-14 Feedback oscillator with noise source.

The oscillator output phase noise is a function of

- the amount of the source noise present at the input of the oscillator circuit, and
- the amount that the feedback system rejects or amplifies various noise components.

As shown in Figure 5-15, an error voltage at an oscillator's output at the nominal time of threshold crossings shifts the actual threshold crossing time by an amount proportional to the voltage error and inversely proportional to the slew rate, is given by [44-45].

$$\overline{\Delta\tau^2} = \frac{\overline{v_n^2}}{(dv/dt)^2} \tag{5.22}$$

where $\overline{\Delta\tau^2}$ is the timing jitter, $\overline{v_n^2}$ is the power of the noise injected at the threshold-crossing, and *dv/dt* is the slew rate of the output voltage of the oscillator at the threshold-crossing point.

The closed-loop transfer function at a frequency offset from the oscillation frequency, ω*o*, by Δω with Δω<<ω*o* is given by

$$|H_c(\omega_0 + \Delta\omega)|^2 \approx \frac{\overline{v_n^2}}{(dv/dt)^2} \tag{5.23}$$

The unity-gain system closed loop transfer function is

$$\left[\mathrm{TF}(\mathrm{j}\omega)\right]_{\mathrm{closed-loop}} = \frac{\mathrm{Y}(\mathrm{j}\omega)}{\mathrm{X}(\mathrm{j}\omega)} = \frac{\mathrm{H}(\mathrm{j}\omega)}{1+\mathrm{H}(\mathrm{j}\omega)} \tag{5.24}$$

$$\left[\mathrm{H}(\mathrm{j}\omega)\right]_{\omega=\omega_0} = -1 \tag{5.25}$$

Figure 5-16 shows the noise signal in response to the injected impulse current at two different times, peak and zero crossing.

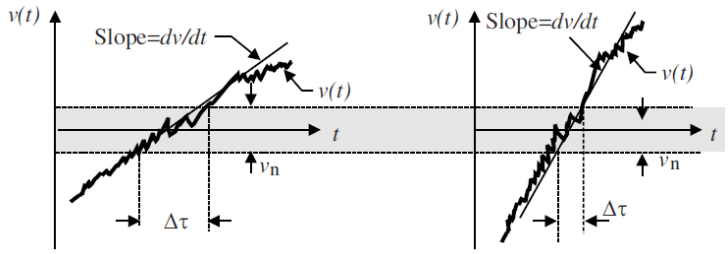

Figure 5-15. Typical RF output waveform of oscillators.

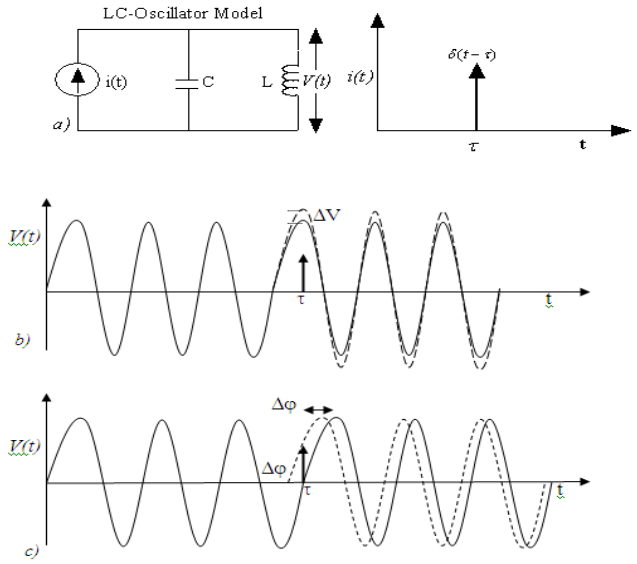

Figure 5-16 a) LC oscillator excited by a current pulse, b) impulse injected at peak of the oscillation signal, and c) impulse injected at zero crossing of the oscillation signal.

For frequencies close to $\omega = \Delta\omega + \omega_0$, the open loop transfer function is

$$\left[\mathrm{H(j\omega)}\right]_{\omega=\omega_0+\Delta\omega} \approx \left[\mathrm{H(j\omega_0)} + \Delta\omega\frac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}}\right] \tag{5.26}$$

The noise transfer function is

$$\left[\frac{\mathrm{Y(j\omega + j\Delta\omega)}}{\mathrm{X(j\omega + j\Delta\omega)}}\right] = \left[\frac{\mathrm{H(j\omega_0)} + \Delta\omega\dfrac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}}}{1 + \mathrm{H(j\omega_0)} + \Delta\omega\dfrac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}}}\right] \tag{5.27}$$

Since $\mathrm{H(j\omega_0)} = -1$ and for most practical cases, $\Delta\omega\dfrac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}} << 1$, we can write

$$\left[\frac{\mathrm{Y(j\omega + j\Delta\omega)}}{\mathrm{X(j\omega + j\Delta\omega)}}\right] \approx \left[\frac{-1}{\Delta\omega\dfrac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}}}\right] \tag{5.28}$$

From the noise transfer function it appears that the noise component at $\omega = \Delta\omega + \omega_0$ is multiplied by the term $\left[\dfrac{-1}{\Delta\omega\dfrac{\mathrm{dH(j\omega)}}{\mathrm{d\omega}}}\right]$, relative to the output.

The broadband white noise is shaped by the resonator as seen in Figure 5-17.

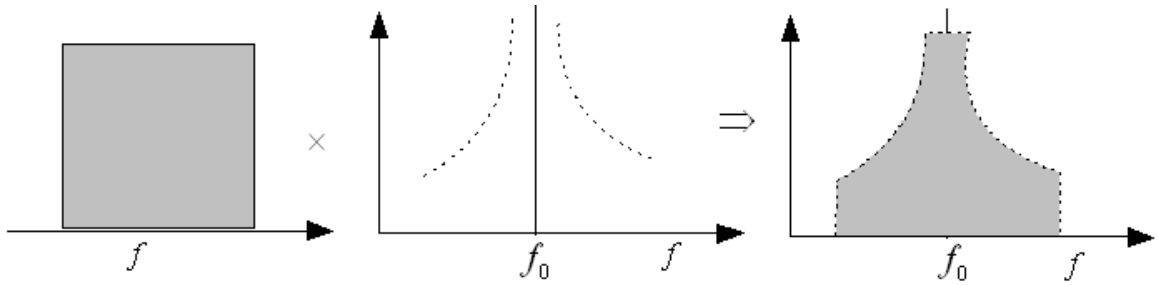

Figure 5-17 Noise shaping in the oscillator.

Therefore, the noise power spectral density can be explained as

$$\left|\frac{Y(j\omega+j\Delta\omega)}{X(j\omega+j\Delta\omega)}\right|^2=\left|\frac{-1}{\Delta\omega\frac{dH(j\omega)}{d\omega}}\right|^2 \tag{5.29}$$

$$H(j\omega)=A(j\omega)\exp[j\phi(j\omega)] \tag{5.30}$$

$$\frac{dH(j\omega)}{d\omega}=\left[\frac{dA(j\omega)}{d\omega}+jA(j\omega)\frac{d\phi(j\omega)}{d\omega}\right]\exp[j\phi(j\omega)] \tag{5.31}$$

Assume $\omega=\Delta\omega+\omega_0$, $\omega\to\omega_0$ and $|A(j\omega_0)|\to 1$ then the above equation is reduced to

$$\left|\frac{Y(j\omega+j\Delta\omega)}{X(j\omega+j\Delta\omega)}\right|^2=\left[\frac{1}{(\Delta\omega)^2\left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2+\left[\frac{d\phi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0} \tag{5.32}$$

The open loop Q_L becomes

$$Q_L=\frac{\omega_0}{2}\sqrt{\left[\frac{dA(j\omega)}{d\omega}\right]^2+\left[\frac{d\phi(j\omega)}{d\omega}\right]^2} \tag{5.33}$$

and

$$\left|\frac{Y(j\omega+j\Delta\omega)}{X(j\omega+j\Delta\omega)}\right|^2=\left[\frac{1}{(\Delta\omega)^2\left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2+\left[\frac{d\phi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0}=\frac{1}{4Q_L{}^2}\left[\frac{\omega_0}{\Delta\omega}\right]^2 \tag{5.34}$$

For the LC resonator $\left[\frac{dA(j\omega)}{d\omega}\right]$ at resonance ($\omega\to\omega_0$) becomes zero and $Q_L=\frac{\omega_0}{2}\frac{d\varphi}{d\omega}$ (5.35)

Equation (5.35) reveals that to minimize the phase noise of oscillators, the quality factor of the oscillators should be maximized by maximizing the sensitivity of the phase $\phi(\omega)$ with respect to frequency at ω_0. Lee and Hajimiri introduced an impulse sensitivity function (ISF) based on the injected impulse, which is different for each topology of the oscillator. It has its largest value when the most phase modulation occurs and it has the smallest value when only the amplitude modulation occurs. Based on this theory, the phase noise equation is expressed as [37-43]

$$\pounds(f_m) = \begin{cases} 10\log\left[\left(\frac{C_0{}^2}{q_{max}^2}\right)\left(\frac{i_n{}^2/\Delta f}{8f_m^2}\right)\left(\frac{\omega_{1/f}}{f_m}\right)\right]; & \frac{1}{f^3} \rightarrow \text{region} \\ 10\log\left[10\log\left[\left(\frac{\Gamma_{rms}{}^2}{q_{max}^2}\right)\left(\frac{i_n{}^2/\Delta f}{4f_m^2}\right)\right]\right]; & \frac{1}{f^2} \rightarrow \text{region} \end{cases} \quad (5.36)$$

$$\Gamma_{rms}^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = \sum_{n=0}^{\infty} C_n^2 \quad (5.37)$$

$$\Gamma(x) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n Cos(nx + \theta_n); \quad x = \omega_0 t \quad (5.38)$$

$$\omega_{1/f^3} = \omega_{1/f}\left[\frac{C_0^2}{\Gamma_{rms}^2}\right] \quad (5.39)$$

Where
$\left(i_n{}^2/\Delta f\right)$ is the noise power spectral density,
Δf is the noise bandwidth,
Γ^2_{rms} is the root mean square value of $\Gamma(x)$, the impulse sensitivity function (ISF),
C_n are the Fourier series coefficients, $x = \omega_0 t$,
C_0 is the 0^{th} order of the ISF (Fourier series coefficient),
θ_n is the phase of the n^{th} harmonic,
f_m is the offset frequency from the carrier,
$\omega_{1/f}$ is the flicker corner frequency of the device,
q_{max} is the maximum charge stored across the energy storing capacitor in the resonator network.

As illustrated in Figure 5-16, if an impulse is injected into the tuned circuit at the peak of the signal, it will cause maximum amplitude modulation and no phase modulation whereas if an impulse is injected at the zero crossing of the signal, there will be no amplitude modulation, only maximum phase modulation. If noise impulses are injected between the zero crossing and the peak, there will be components of both the phase and the amplitude modulation. Variations in amplitude are generally ignored because they are limited by the gain control mechanism of the oscillator. Therefore, according to this theory, to obtain the minimal phase noise, special techniques have to be adopted so that any noise impulse should coincide in time with the peaks of the output voltage signal rather than at the zero crossing or in between the zero crossing and peak.

From Equation (5.36), the minimum phase noise at far offset frequencies can be obtained by minimizing the noise factor *F*. Close-in phase noise is related to the 1/*f* noise up-conversion and can be suppressed by allowing symmetry property of the oscillator RF signal waveforms. From Equation (5.36), 1/*f* noise up-conversion can be reduced by minimizing the value of C_0, which is a function of the slope of the rise and fall time of the waveform across active inductor resonator. However, the calculation of the ISF in Equation (5.36) is tedious and therefore does not lead to exact design rules.

Traditional approaches (Leeson model, Lee and Hajimiri model) are not sufficient to describe the phase noise dynamics of active inductor oscillators due to regenerative behavior of the active inductor that influences oscillator noise dynamics significantly.

5.5 Active Inductor Oscillator Phase Noise

Figure 5-18 shows the series feedback tunable active inductor oscillator (TAIO) topology for the purpose of the phase noise analysis. The steady-state oscillation condition is given by [10]

$$Z_{osc}(I_L,\omega)+Z_L(\omega)=0 \tag{5.40}$$

$$Z_{osc}(I_L,\omega)=R_{osc}(I_L,\omega)+jX_{osc}(I_L,\omega) \tag{5.41}$$

$$Z_L(\omega)=R_L(\omega)+jX_L(\omega) \tag{5.42}$$

$$Z_{osc}=[Z_{22}+Z_2]-\frac{[Z_{12}+Z_2][Z_{21}+Z_2]}{[Z_{11}+Z_1+Z_2]} \tag{5.43}$$

where Z_{11}, Z_{12}, Z_{21}, Z_{22} are the [Z] parameters of the transistor.

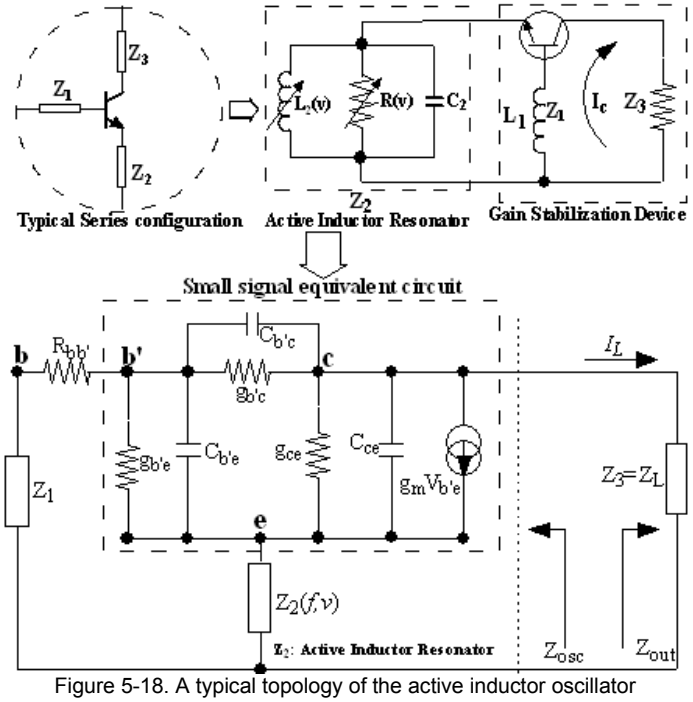

Figure 5-18. A typical topology of the active inductor oscillator

From [10], Z_{osc}, R_{osc}, X_{osc}, and R_n can be described by

$$Z_{osc}=-\frac{g_m^0}{\omega^2 C_{ce}[C_{b'e}+C_2-L_2C_2C_{be}\omega^2]}-j\left[\left(\frac{C_{ce}+C_2}{\omega C_{ce}C_2}\right)-\left(\frac{1}{\omega\left(\frac{C_2^2}{C_{b'e}}\right)+\omega C_2-L_2C_2^2\omega^3}\right)\right] \tag{5.44}$$

$$Z_{osc}=[R_{osc}+jX_{osc}]\Rightarrow R_{osc}=R_n=-\left[\frac{g_m^0}{\omega^2 C_{ce}[C_{b'e}+C_2-L_2C_2C_{b'e}\omega^2]}\right] \tag{5.45}$$

$$X_{osc}=-\left[\left(\frac{C_{ce}+C_2}{\omega C_{ce}C_2}\right)-\left(\frac{1}{\omega\left(\frac{C_2^2}{C_{b'e}}\right)+\omega C_2-L_2C_2^2\omega^3}\right)\right] \tag{5.46}$$

From Equation (5.44), we change the small-signal transconductance g_m^0, to a large-signal $g_m(t)$

$$R_{osc} = R_n(t) = -\left[\frac{g_m(t)}{\omega^2 C_{ce} C_2 [1 - L_2 C_{b'e} \omega^2]}\right] \tag{5.47}$$

where $g_m(t)$ can be describe by [10]

$$g_m(t) = \sum_{n=-\infty}^{n=\infty} g_m^{(n)} \, exp(jn\omega t); \text{ (n = number of harmonics)} \tag{5.48}$$

The phase noise can be given by [10]

$$\pounds(\omega) = \left[4kTR + \frac{\left|g_m^2(t)\right|\left[4qI_c + \frac{K_f I_b^{AF}}{\omega}\right]}{\omega_0^4 \beta^2 C_{ce}^2 (C_2 + C_{b'e} - L_2 C_2 C_{b'e} \omega_0^2)^2 + \left|g_m^2(t)\right| \omega_0^2 (C_2 + C_{b'e} - L_2 C_2 C_{b'e} \omega_0^2)^2}\right] \times$$

$$\left[\frac{\omega_0^2}{4(\omega)^2 V_{cc}^2}\right]\left[\frac{1}{Q_L^2} + \left(1 - \left(\frac{1}{\omega_0^2 L_2}\right)\left(\frac{[(C_2 + C_{b'e} - L_2 C_2 C_{b'e} \omega_0^2) + C_{ce}]}{C_{ce}[(C_2 + C_{b'e} - L_2 C_2 C_{b'e} \omega_0^2)]}\right)\right)^2\right] \tag{5.49}$$

Where
$\pounds(\omega)$ is the ratio of sideband power in a 1Hz bandwidth,
ω is the offset frequency from the carrier,
ω_0 is the resonance frequency,
Q_L is the loaded Q of the tuned circuit,
K_f is the flicker noise coefficient,
AF is the flicker noise exponent,
kT is 4.1×10^{-21} at 300K, (Boltzmann's constant multiplied by the room temperature in Kelvin)
R is the equivalent noise resistance of the active inductor resonator circuit (function of shot, thermal and flicker noise, which will be calculated in full length paper),
I_c is the RF collector current,
I_b is the RF base current, and
V_{cc} is the RF collector voltage.

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6. State-of-the-art and Characterization of Varactor-Tuned and Inductor-Tuned LC Oscillator Circuits

The concept of passive LC resonator based oscillators is well understood and validated in discrete and integrated solution, including the noise dynamics, which is critical for signal source applications. However, there is lack of understanding about the active inductor oscillator noise dynamic. It becomes more critical with reference to the technological scaling for high frequency integrable signal source applications.

In MMIC design, inductors form an essential element in frequency selection, matching and filtering. Unfortunately, the spiral inductors used in MMIC design occupy a large die area. Their magnetic coupling results in cross talk degrading their performance. The embedded stray capacitances are also a concern at high frequencies. Hence, active inductors have long been considered as an alternative for passive inductors. Since active inductors are formed using transistors, it is very easy to realize them in MMIC design. They occupy a very small fraction of area compared to passive spiral inductors. It is also possible to realize a wide range of inductance values and tunable inductors using active inductors [1]-[5].

In this research work, a basic active tunable inductor structure is analyzed. A 1.9-2.8 GHz Colpitts oscillator circuit is designed using a passive and active inductor topology with similar values of Q-factor and DC operating conditions. It was observed that both the passive and active oscillators were found to oscillate at almost the same frequency but the active inductor oscillator was noisier. It was also observed that the Leeson formula for phase noise prediction does not hold for active inductor based oscillators.

For RF signal source applications, stringent conditions are placed on ATI oscillators owing to its inherent high noise figure and low dynamic range caused by the uncontrolled nonlinearity at large-signal conditions. In addition, these problems become critical at high frequency when active devices (Bipolar/FET) are technologically scaled to obtain higher cut-off frequency.

6.1 Passive and Active Inductor Oscillators

It is well know that the inductor is the key element in the realization of an on-chip LC resonator network for the application in oscillator circuits. The fabrication of the capacitor is readily available in all standard IC technologies. Nevertheless, a standard technology that allows the realization of the inductor lacks high quality factor (Q-factor) and self-resonance frequency (SRF). For comparative analysis, three basic topologies are discussed using low Q-factor inductance: LC oscillator, varactor-tuned LC oscillator, and inductor-tuned oscillator. For fair comparison, both the oscillator circuits (lumped inductor and synthesized inductor) incorporate similar values of inductance and loss resistance for a given Q-factor and resonant conditions.

6.1.1 Passive Low Q-Factor Lumped Colpitts LC Oscillator Circuit

Figure 6-1 shows the schematic of a 1.9 GHz LC Colpitts oscillator using low Q-factor passive inductor (L= 0.8nH, R_S= 1.9Ω, Unloaded Q = 5.29). Figure 6-2 shows the CAD simulated phase noise plot. The reason for considering the low *Q*-factor lumped inductor is to show comparative analysis in standard IC technology (standard IC technology offers low *Q*-factor for spiral inductors) for varactor and inductor tuned oscillator circuits.

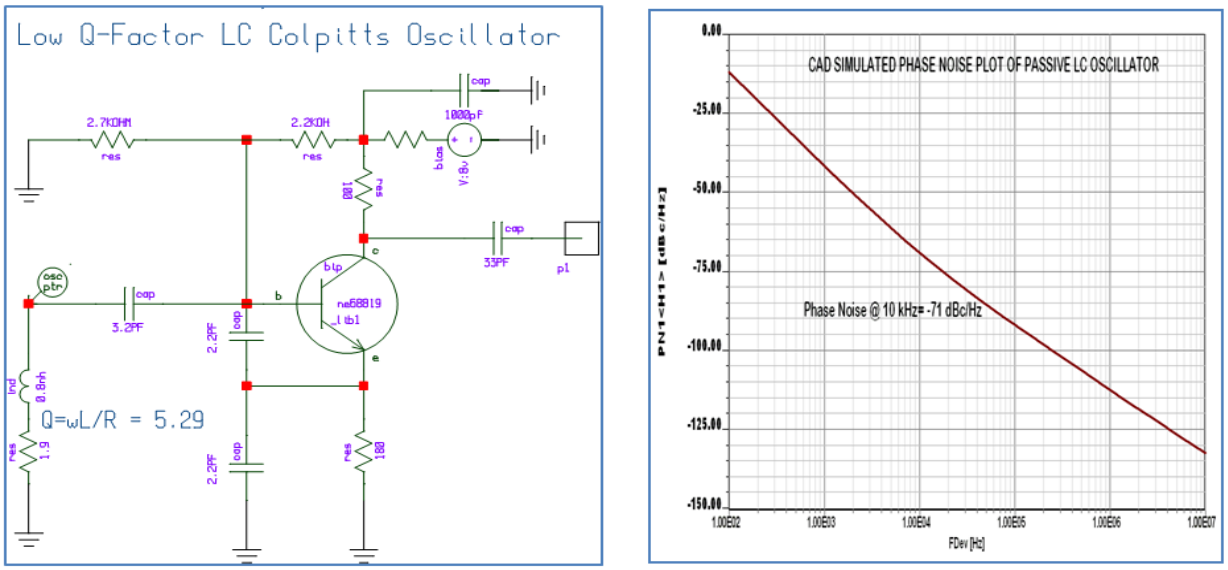


Figure 6-1 Schematic of the 1.9 GHz Colpitts oscillator (with unloaded Q =5.29, using 0.8nH lumped inductor with series loss resistance 1.9 Ohm)

6.1.2 Varactor-Tuned Passive Low Q-Factor Lumped Colpitts LC Oscillator Circuit

Figure 6-3 shows the schematic of a varactor-tuned LC Colpitts oscillator circuit using a passive lumped inductor (L= 0.8nH, R_S= 1.9Ω, unloaded Q = 5.29). Figure 6-4 shows the CAD simulated phase noise plots of fixed and varactor tuned LC oscillator circuit of Figure 6-1 and Figure 6-3.

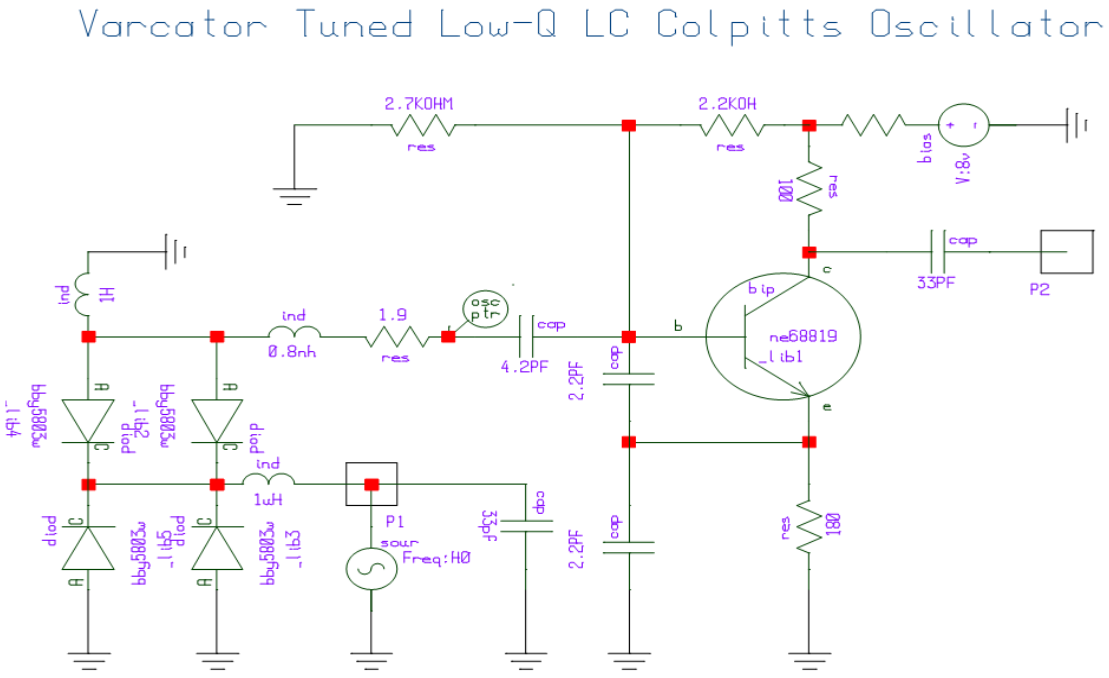


Figure 6-3 Schematic of a varactor-tuned LC Colpitts oscillator circuit using passive lumped inductor (L= 0.8nH, R_S= 1.9Ω, Unloaded Q = 5.29).

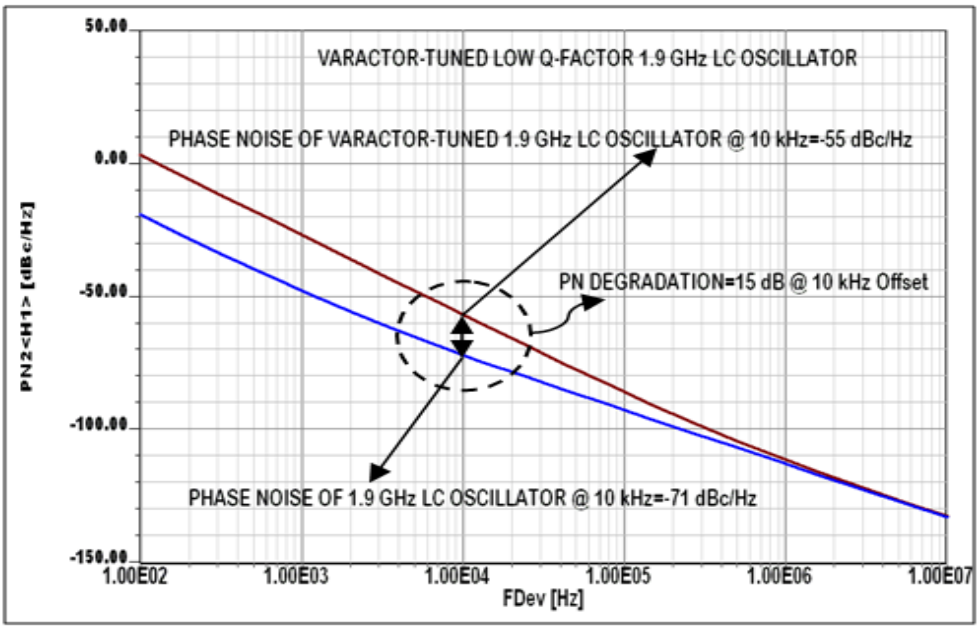


Figure 6-4a CAD simulated phase noise plot of fixed frequency LC (Figure 6-1) and varactor tuned LC oscillator circuit (Figure 6-3)

It can be seen from Figure 6-4, the varactor-tuned LC oscillator circuit degrades the phase noise as much by 15 dB as compared to the fixed frequency LC oscillator at 10 kHz offset from the 1.9 GHz carrier frequency.

The oscillator voltage gain associated with the tuning sensitivity of the varactor diode comprised tuning network is the reason for the noise degradation. From [6], the Leeson phase noise Equation can be given by

$$£(f_m) = 10\log\left[\left(1+\frac{{f_0}^2}{(2f_mQ_0)^2m^2(1-m)^2}\right)\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}\right] \tag{6.1}$$

The Leeson phase noise equation (6.1) is modified by Rohde [6]

$$£(f_m) = 10\log\left\{\left[1+\frac{{f_0}^2}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^2}{f_m^2}\right\} \tag{6.2}$$

where m, Q_0, f_0, f_c, f_m, F , K_0, R, k and T are defined as the ratio of the loaded and unloaded Q, unloaded Q_0, oscillation frequency, flicker corner frequency, offset frequency from the carrier, noise factor, oscillator voltage gain, noise resistance of the tuning diode, Boltzmann's constant and temperature in degrees Kelvin, respectively.

Equation (6.2) explains the phase noise degradation (as compared to the fixed frequency LC oscillator due to the oscillator voltage gain K_0 associated with the tuning diode network. The reason for noise degradation is due to the increased tuning sensitivity of the varactor diode tuning network.

The last term of Equation (6.2) accounts for a degradation of 15dB of phase noise and is due to modulation noise in varactor-tuned oscillator circuits.

The characterization of synthesized inductor with relevant intrinsic noise due to nonlinearity associated with active devices that comprises inductor network gives better flexibility during the design. It is possible to introduce an arbitrary noise parameter linked with synthesized inductor and equate with effective noise factor for the fitting parameters in modified Leeson phase noise equation. The model can be extended to reflect some basic imperfections: their modulation sensitivity and noise generation. The effects of these imperfections can be analyzed based on the extended model, and can be verified with equivalent varactor-tuned oscillator circuits for similar noise factor and other critical parameters.

Analytical Phase Noise Evaluation Using MatLab:
The mathematical model to simulate the phase noise model described in Equation (6.1) and Equation (6.2) for the Colpitts oscillator is plotted in Figure 6-4b. The parameters of the mathematical model are given below.

```
*** Defining the known parameters ****
F=10^3.81;                  %  38.1 db NF = 10 log10 (F)
KT=4.2*1e-21;               %  Boltzmann constant at room temperature T=300K
Psav=10^(0/20);             %  P = 0dBm ==> 0dBm = 20 log10 (Psav)
fc=1000;                    %  Flicker Corner Freq. Unit Hertz
B=1;                        %  1 Hz Bandwidth
f=1.9*1E9;                  %  Desired Frequency in Hertz
QL=2.6045;                  %  Loaded Q factor (Rohde's phase noise model)
Qunl=5.29;                  %  Unloaded Q factor for Leeson's Equation
m=QL/Qunl;                  %  m = Qun/Ql; gives optimum phase noise
fm=[100 300 500 700 900 10^3 3000 7000 8000 9000 10^4 10^5 10^6 10^7 10^8];

*** Computing the Phase noise as per Leeson's equation ***
for i=1:length(fm)
   denunl=((2*fm(i)*Qunl)^2)*((1-m)^2)*(m^2);
   L1(i)=10*log10((1+(f^2/denunl))* (1+(fc/fm(i)))* (F*KT/(2*Psav));
   if L1(i)<=-174
      L1(i)=-174;
   end
end

*** Computing the Phase noise for the active inductor oscillator ***
fcscale=fc*4.1^4;
m1=QL/(1*Qunl);
R=1.89;                     %  Resistance 1.9 ohm
K0=1500;                    %  K0 = 1.5KHz/V
for i=1:length(fm)
   den=(((1/0.45)*fm(i)*Qunl)^2)*((1-m1)^2)*(m1^2);
   t3=(1+(f^2/den))* (1+(fcscale/fm(i)))* F*KT/(2*Psav);
   L2(i)=10*log10(t3+ KT*R*B*(K0/fm(i))^2);
   if L2(i)<=-174
      L2(i)=-174;
   end
end

*** Plotting both the Phase noise on graph ***
semilogx(fm, L1)
hold on
semilogx(fm, L2)
```

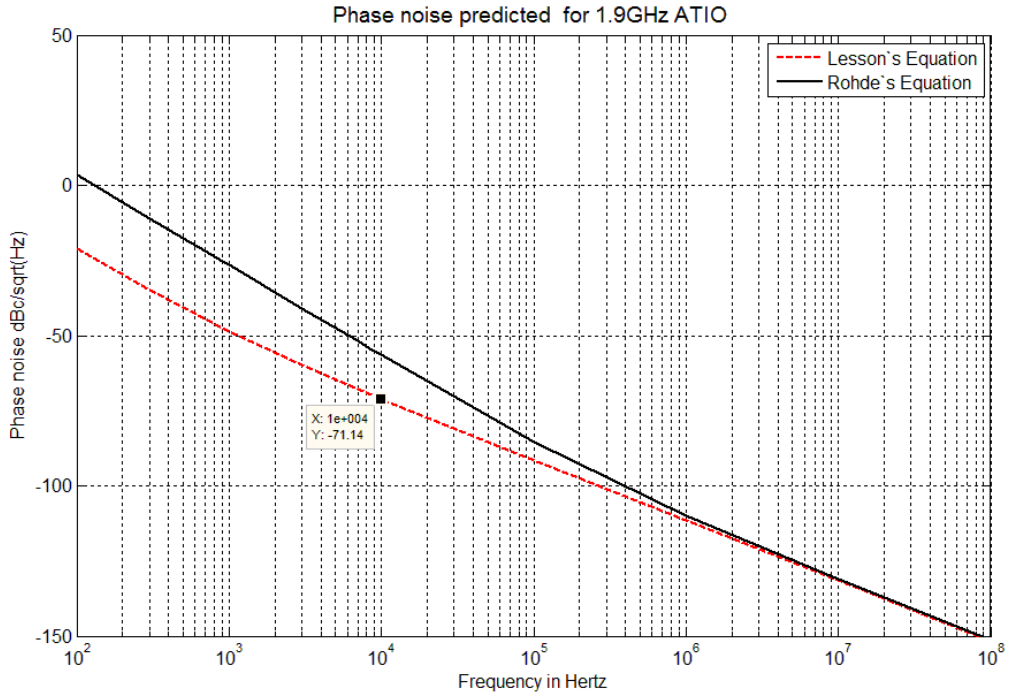


Figure 6-4b The analytical predicted phase noise plot for 1.9 GHz LC oscillator

The terms that are scaled are flicker corner frequency fc changed to fcscale=fc*4.1^4; and the denominator factor, den=(((1/0.45)*fm(i)*Qunl)^2)*((1-m1)^2)*(m1^2); the noise figure was found to be 38.1 db and the simulated noise figure was 38.21dB. The 4.1^4 is termed in this text as the scaling parameter-1 and it mainly affects the frequencies below 10^5. The scaling factor in the denominator is termed as scaling parameter-2, which affects the noise floor at the far offset.

6.1.3 Inductor-Tuned Low Q-Factor Colpitts LC Oscillator

Figure 6-5 shows a schematic of a transistorized inductor using SiGe HBT (BFP 620) from Infineon. Figure 6-6 shows the typical plot of reactance and equivalent loss resistance of the synthesized inductor using high cut-off frequency SiGe HBTs. The reason for using a high cut-off frequency SiGe HBT transistor is to minimize the package parasitic effects and allow comparative evaluations of the 1.9GHz varactor-tuned and synthesized inductor-tuned LC oscillator using discrete components for experimental validations.

As shown in Figure 6-6, the value of the realized inductance and associated equivalent loss resistance are 0.8nH and 1.9Ω at 1.9 GHz for the operating DC bias condition (3V, 1.8mA) and V_{tune} (2.5V). The operating DC bias and V_{tune} are adjusted in such a way that realized equivalent noise resistance must be positive to avoid the multi-mode oscillations caused by the regenerative effect (if the simulated loss resistance associated with realized inductor is negative in value).

Figure 6-7 shows the schematic of an inductor-tuned Colpitts oscillator circuit using the synthesized inductor (0.8nH, 1.9Ω) realized from the SiGe-HBT BFP620 (Infineon) of Figure 6-5 as a part of resonating network at 1.9GHz.

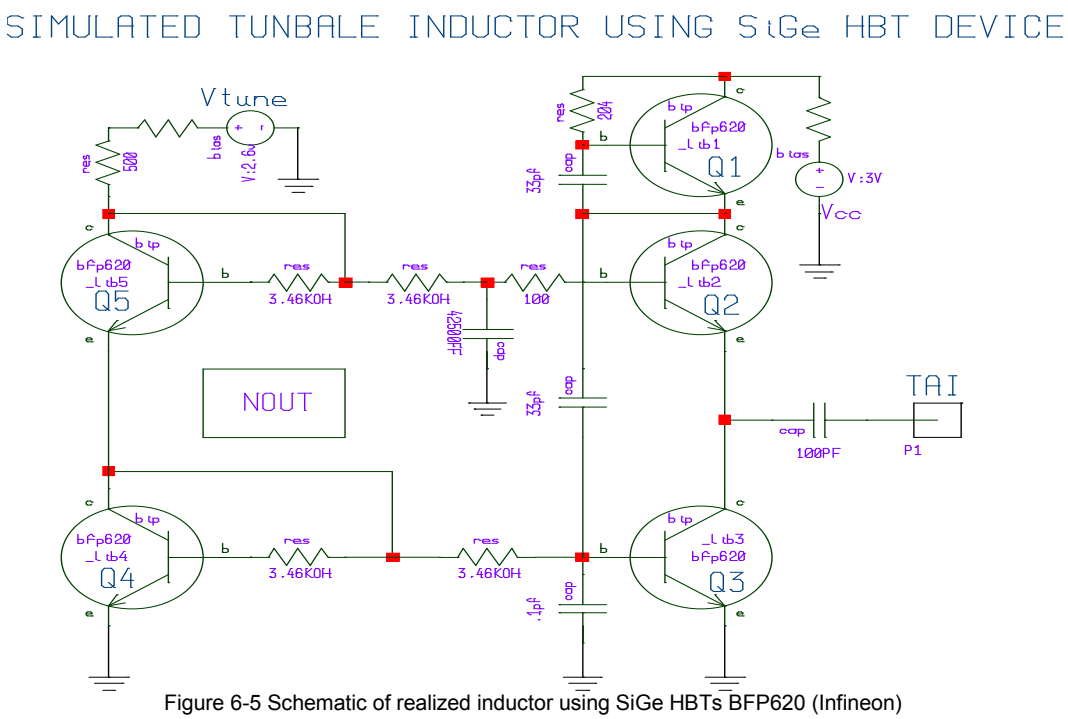


Figure 6-5 Schematic of realized inductor using SiGe HBTs BFP620 (Infineon)

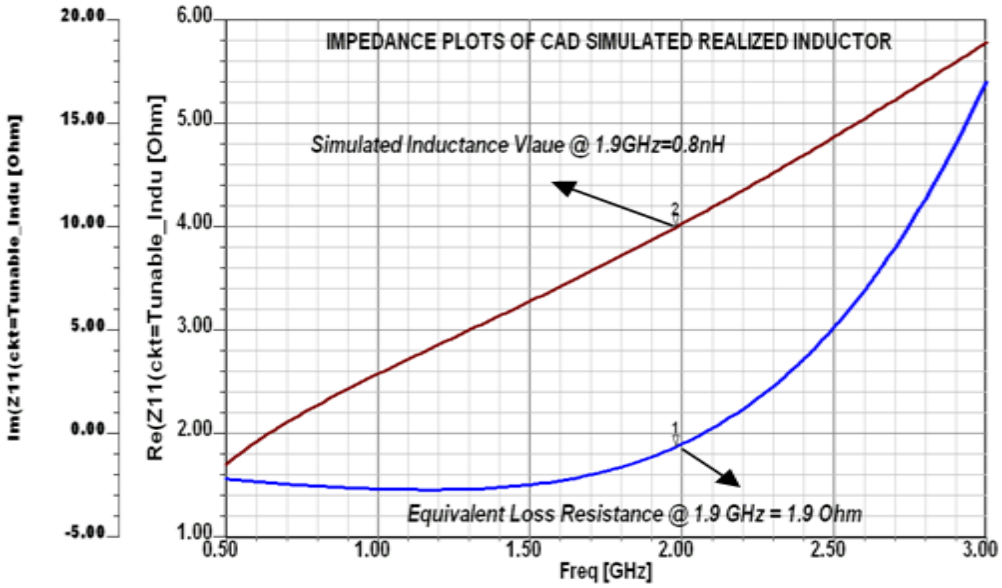


Figure 6-6 Reactance and equivalent loss resistance of realized inductor using SiGe HBT BFP620 (Infineon).

Figure 6-7 shows the phase noise using the synthesized inductor (0.8nH with series loss resistance 1.9Ω) with approximately similar oscillator voltage gain K_0 as given for the varactor-tuned oscillator circuit of Figure 6-3.

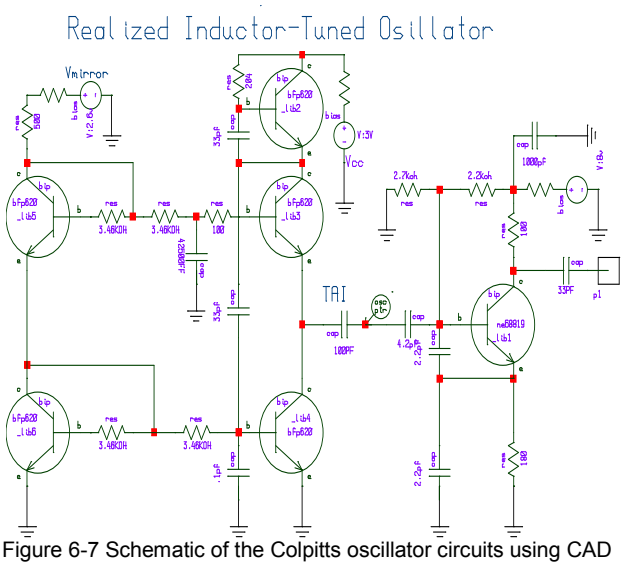


Figure 6-7 Schematic of the Colpitts oscillator circuits using CAD simulated inductor (0.8nH, 1.9Ω) of Figure 6-5.

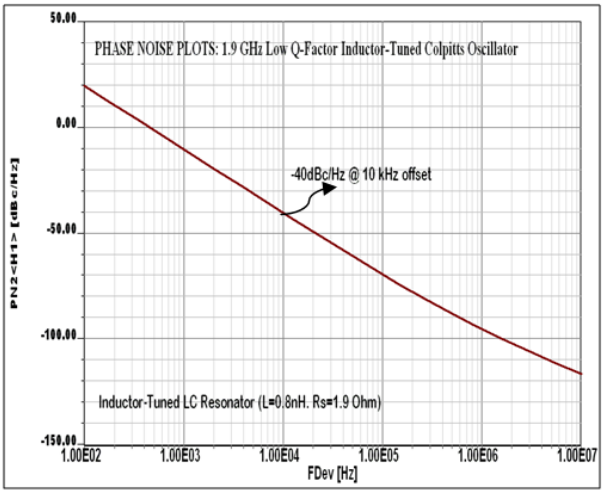


Figure 6-8 Simulated phase noise plot of circuit in Figure 6-7

Figure 6-9 shows the comparative phase noise plots based on the phase noise model described in Equation (6.1) and Equation (6.2) for the LC Colpitts oscillators using the passive lumped LC resonator, the varactor-tuned resonator and the synthesized inductor-tuned resonator network for identical inductance value and loss resistance (0.8nH with series loss resistance 1.9Ω).

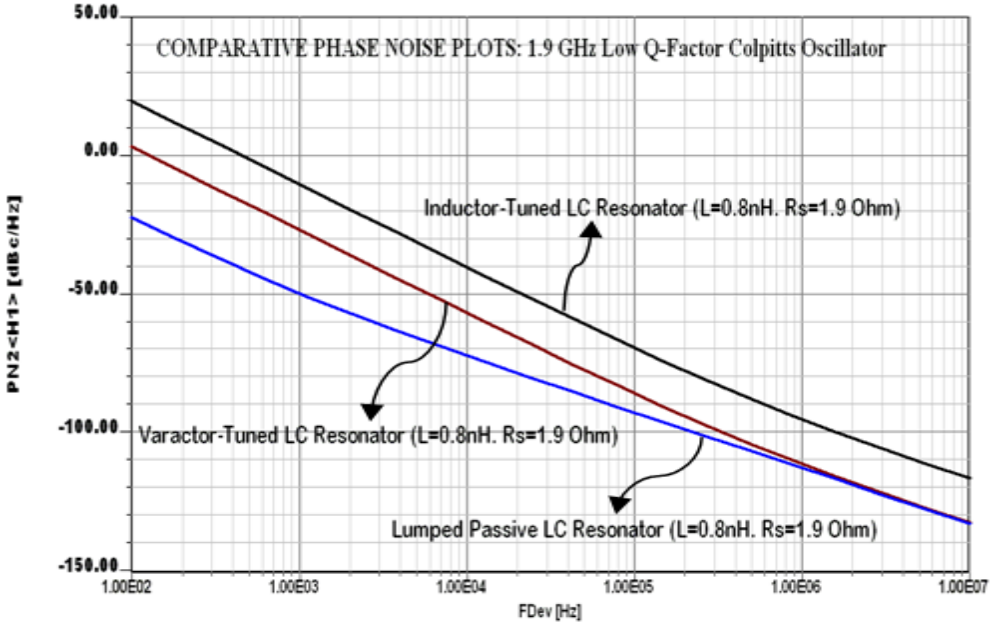


Figure 6-9 Comparative phase noise plots of LC oscillators using fixed lumped LC resonator (Figure 6-1), varactor-tuned resonator (Figure 6-3) and synthesized inductor-tuned resonator circuits (Figure 6-7).

It can be determined from Figure 6-9 that the inductor-tuned oscillator shows inferior phase noise performance as compared to lumped LC and varactor-tuned oscillator circuits.

All the three topologies (Figure 6-1, Figure 6-3 and Figure 6-7) use similar operating conditions, including the Q-factor. However, the oscillator gain and modulation sensitivity become the dominating factor for the overall phase-noise performance. It is important to note that even

though the oscillator gain and modulation sensitivity are kept identical for the varactor-tuned and inductor-tuned oscillators, the latter shows inferior phase noise performance. This is because the inductor-tuned resonator exhibits a high value of dynamic noise factor under large-signal conditions as compared to the varactor-tuned resonator circuit.

In addition to this, a *priori* knowledge of noise factor F is a challenging task for the regenerative active inductor if it is used as a part of resonator network in autonomous RF oscillator circuits. This leads to trial and error exercise for the optimization of phase noise using current CAD simulators (Agilent-ADS 2011, Ansoft-Nexxim, AWR and Microwave Office). Moreover, the optimization process seldom converges due to the higher order of noise cross-correlation dynamics involved in synthesized active tunable inductor oscillator circuits. This is major drawback of inductor-tuned oscillator circuits. The goal for improving the phase noise performance and dynamic range of inductor-tuned oscillator is paramount for a smooth transition from integrated varactor-tuned signal sources [2].

6.2 Practical Examples

The objective of this research work is to explore the topology and describe the methodology for minimizing the phase noise using a synthesized inductor-tuned network for a cost-effective alternative to varactor-tuned networks in tunable oscillator circuits.

6.2.1 Active Inductor-Tuned VCO (1.9-2.8 GHz)

As shown in Figure 6-10, the transistors Q_1 and Q_2 form the active portion of the inductor. The transistors Q_3 and Q_4 form a current mirror circuit. The current through Q_1 and Q_2 are set by this current mirror. It is assumed that Q_1 and Q_2 are similar devices and are biased at the same current. Hence, we can assume that both Q_1 and Q_2 have the same transconductance (G_m) and base-emitter capacitance (C_{be}). It was observed that the input impedance Z_{IN} varies with the current I_C through Q_2.

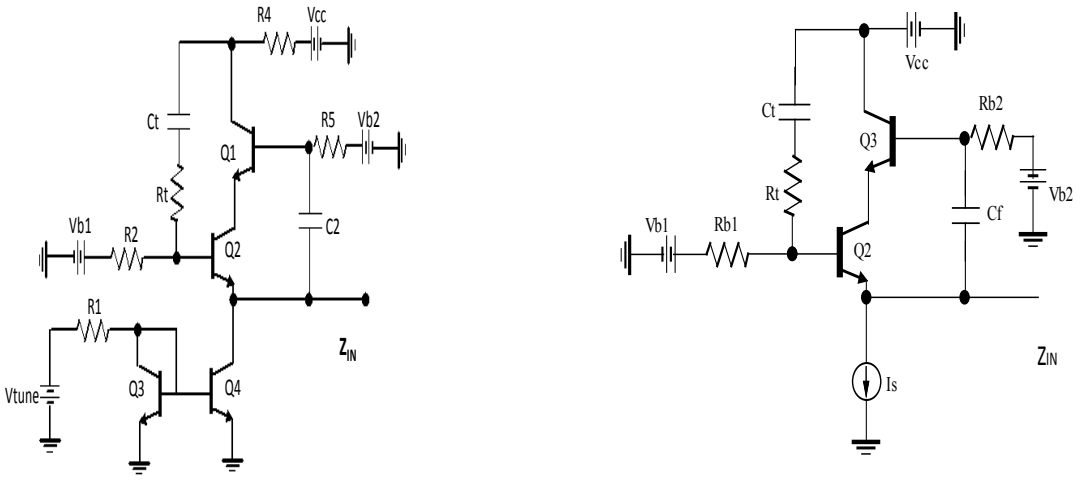
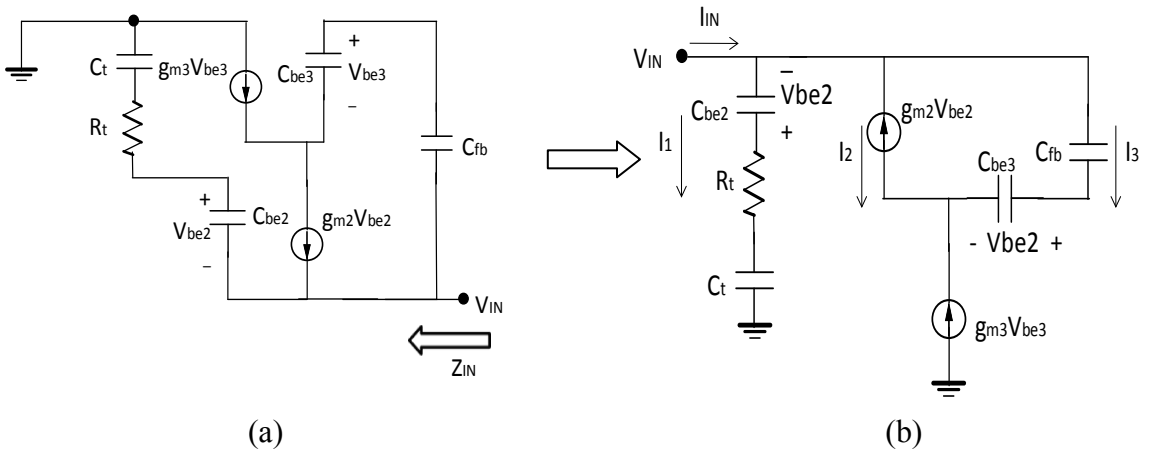


Figure 6-10. A simplified schematic of an ATI circuit topology



(a) (b)

Figure 6-11. Equivalent small signal model of the ATI shown in Figure 6-10

For small-signal analysis, all the DC voltage sources are shorted and the current sources are made open (Figure 6-11). The bias resistors R_{b1} and R_{b2} are of high values and can be considered to be open. The transistors Q_2 and Q_3 are replaced by their equivalent Pi-models and their characteristics can be characterized by

$$I_1 = -j\omega C_{be2}V_{be2} = \frac{V_{in}}{[R_t+\frac{1}{j\omega}\left(\frac{1}{C_{be2}}+\frac{1}{C_t}\right)]} \tag{6.3}$$

$$V_{be2} = \frac{-\mathrm{V_{in}}}{[\mathrm{j\omega C_{be2}R_t}+\left(\frac{\mathrm{C_{be2}+C_t}}{\mathrm{C_t}}\right)]} \tag{6.4}$$

$$V_{be3} = \frac{g_{m2}}{g_{m3}+j\omega C_{be3}}V_{be2} \tag{6.5}$$

For $g_m >> j\omega C_{be}$ $V_{be3} = \frac{g_{m2}}{g_{m3}}V_{be2}$ (6.6)

$$I_2 = -g_{m2}V_{be2} = \frac{g_{m2}V_{in}}{[j\omega C_{be2}R_t+\left(\frac{C_{be2}+C_t}{C_t}\right)]} \tag{6.7}$$

$$I_3 = I_{b3} = j\omega C_{be3}V_{be3} \rightarrow I_3 = j\omega C_{be3}\frac{g_{m2}}{g_{m3}}V_{be2} \tag{6.8}$$

For simplicity, assuming that the transistors Q_2 and Q_3 are biased under similar conditions, we have $g_{m2} = g_{m3}, C_{be2} = C_{be3}$ and

$$I_3 = j\omega C_{be3}V_{be2} \Rightarrow I_3 = \frac{j\omega C_{be3}V_{in}}{[j\omega C_{be2}R_t+\left(\frac{C_{be2}+C_t}{C_t}\right)]} \tag{6.10}$$

$$I_{IN} = I_1 + I_2 + I_3 \Rightarrow I_{IN} = \frac{g_{m2}V_{in}}{[j\omega C_{be2}R_t+\left(\frac{C_{be2}+C_t}{C_t}\right)]} \tag{6.11}$$

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{[j\omega C_{be2}R_t+\left(\frac{C_{be2}+C_t}{C_t}\right)]}{g_{m2}} \tag{6.12}$$

For $\mathrm{C_t >> C_{be2}}$, $Z_{IN} = \frac{[j\omega C_{be2}R_t+1]}{g_{m2}} \Rightarrow Z_{IN} = R_{IN} + j\omega L_{IN}$ (6.13)

$$L_{IN} = \frac{C_{be2}R_t}{g_{m2}},\ R_{IN} = \frac{1}{g_{m2}} \tag{6.14}$$

Using small signal analysis, the input impedance Z_{IN} into the emitter of Q_2 is given by

$$Z_{in} = R_{in} + j\omega L_{in} \tag{6.15}$$

Where, $R_{in} = \frac{1}{Gm} = \frac{n}{I_c}\frac{KT}{q}$ (6.16)

$$\mathrm{L_{in}} = \frac{\mathrm{C_{be}(I_c).R_t}}{\mathrm{G_m}} = \frac{\mathrm{C_{be}(I_c).Rt}}{\mathrm{I_c.q}}.\mathrm{nkT} \tag{6.17}$$

I_C is the current through Q_1 and Q_2, and C_{be} is the base-emitter capacitance of Q_1 and Q_2. It can be seen that as the current I_C through Q_2 increases, the inductance and resistance seen from port 1 decreases. Thus a tunable inductor is achieved by using a voltage source V_{tune} to control the current through Q_1, thereby changing the inductance L_{in}. For the validation of the phase-noise discrepancy as predicted by Leeson's phase noise model Equation (6.1), an active tunable inductor VCO was designed and fabricated in 20 mil Rogers TMM3 PCB substrate (Figure 6-12).

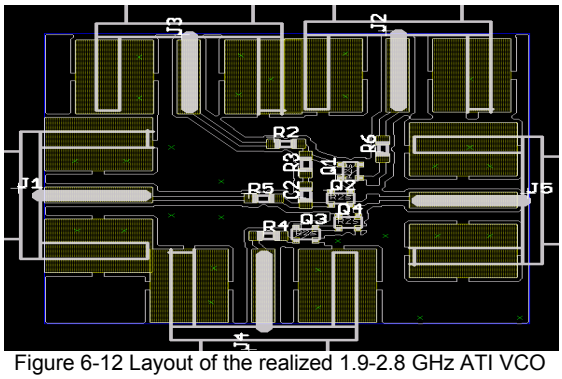


Figure 6-12 Layout of the realized 1.9-2.8 GHz ATI VCO

Figure 6-13 shows the measured output power and phase noise which was found to be 2.8dBm and $-95\ dBc/Hz$ at 100 kHz offset from the carrier at 2.4GHz. The measured phase noise performance is inferior in comparison to commercially available spiral inductor LC resonator based oscillators for a given DC power consumption. In addition to this 1/*f* noise associated with the active devices (SiGe HBT BFP 620F, Infineon) forming the active inductor under large-signal drive can become the principle degrading factor.

The goal for improving flicker noise (1/*f* noise) characteristics is paramount for enabling seamless transition from varactor-tuned LC resonator oscillator topologies to inductor-tuned oscillator applications. The noise contribution due to 1/*f* noise, which lies in the base current of the SiGe HBTs, can be described by

$$S_{I_b,1/f} = \left[\frac{\overline{i^2_{1/f}}}{\Delta f}\right] = \left[\frac{K}{A_e}\right]\left[\frac{I_B^a}{f^b}\right] \tag{6.18}$$

where Δf is a narrow frequency bandwidth at frequency f, I_B is a base current, K is a constant for a particular device and technology, A_e is the emitter area, a is flicker noise exponent (≅2 for SiGe HBTs), and b is the flicker noise frequency shaping factor with a value of about unity. The impact of 1/f noise can be described by [4]

$$\pounds(f_m) = \begin{cases} 10\log\left[\left(\frac{C_0{}^2}{q^2_{\max}}\right)\left(\frac{i_n{}^2/\Delta f}{8f_m^2}\right)\left(\frac{\omega_{1/f}}{f_m}\right)\right]; & \frac{1}{f^3} \rightarrow region \\ 10\log\left[10\log\left[\left(\frac{\Gamma_{rms}{}^2}{q^2_{\max}}\right)\left(\frac{i_n{}^2/\Delta f}{4f_m^2}\right)\right]\right]; & \frac{1}{f^2} \rightarrow region \end{cases} \tag{6.19}$$

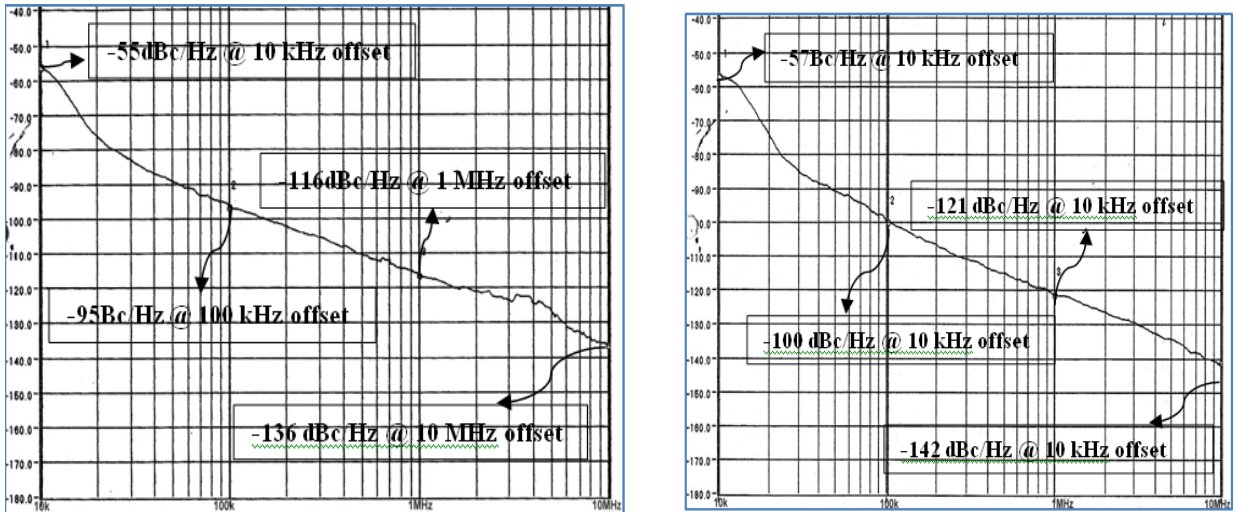
$$\Gamma^2_{rms} = \frac{1}{\pi}\int_0^{2\pi}|\Gamma(x)|^2 dx = \sum_{n=0}^{\infty} C_n^2 \tag{6.20}$$

$$\Gamma(x) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n Cos(nx + \theta_n); \quad x = \omega_0 t \tag{6.21}$$

$$\omega_{1/f^3} = \omega_{1/f}\left[\frac{C_0^2}{\Gamma_{rms}^2}\right] \tag{6.22}$$

Where
$\left(i_n^2 / \Delta f\right)$ is the noise power spectral density,
Δf is the noise bandwidth,
Γ^2_{rms} is the root mean square value of $\Gamma(x)$, the impulse sensitivity function (ISF),
C_n are the Fourier series coefficient, x is $(\omega_0 t)$,
C_0 is the 0^{th} order of the ISF (Fourier series coefficient),
θ_n is the phase of the n^{th} harmonic,
f_m is the offset frequency from the carrier,
$\omega_{1/f}$ is the flicker corner frequency of the device,
q_{max} is the maximum charge stored across the energy storing capacitor in the resonator network.

From Equation (6.19) to Equation (6.22), $1/f$ noise up-conversion can be reduced by minimizing the value of C_0, which is a function of the slope of the rise and fall time of the waveform across the active devices of the voltage tunable inductor circuits. The value of C_0 is minimized by enabling phase-injection and linearizing the tuning sensitivity of the inductor-tuned oscillator [3].



(a) (without optimization) (b) with optimization

Figure 6-13 Measured phase noise plots of the ATI VCO at 2.4 GHz: (a) with and (b) without optimization of C_0 (0^{th} order of the ISF)

Further improvement in phase noise performance over entire the frequency band can be achieved by using N-push inductor-tuned oscillator topology; this task is taken as a future research work, which is in progress in BiCMOS technology.

6.2.2 Self-Injection-Locked Inductor-Tuned Colpitts Oscillator Circuits

A typical transistorized inductor-tuned oscillator exhibits inherent high noise factor due to the uncontrolled nonlinearity associated with the simulated inductor under the large signal drive-level conditions. The emerging applications of tunable active inductor topology continue to be

unfolded along with the inception of new design techniques for improving phase noise and dynamic range. In spite of the drawbacks, active inductors have a significant advantage over passive inductors in terms of die-area, Q-factor, and issues regarding EMI and floor planning. This section develops method to understand the impact of the injection mechanism and minimization of noise factor associated with synthesized inductor topologies.

In this thesis, design techniques to enhance the tuning range and to improve the phase noise performance of tunable active-inductor (TAI)-based oscillators have been presented. Noise analysis of the TAI suggests a direct trade-off between the range of tunable inductance and the output noise that leads to an optimization. The novel and cost-effective approach is to incorporate self-injection-locking mechanism to improve the noise dynamics of inductor-tuned oscillator circuits for a given figure-of-merit (FOM). Measurements of the injection locked TAI-based VCOs in SiGe HBTs technology demonstrate a phase noise improvement of around 10dBc/Hz @ 10 kHz offset from the carrier. Figure 6-14 shows the typical schematic of self-injection-locked inductor-tuned Colpitts oscillator realized by incorporating phase shifter network in the feedback path, which improves the 1/*f* noise, including linearization of the large signal drive-level characteristics of the synthesized inductor circuits. Figure 6-15 shows the CAD simulated phase noise plots with and without injection-locking for giving brief insights about the improvement in phase noise performance. It can be seen from the phase noise plots (Figure 6-16) that the phase noise without injection locking is approximately -41dBc/Hz, whereas, with injection locking, the phase noise drops to -58dBc/Hz at 10 kHz offset from the 1.9 GHz carrier frequency.

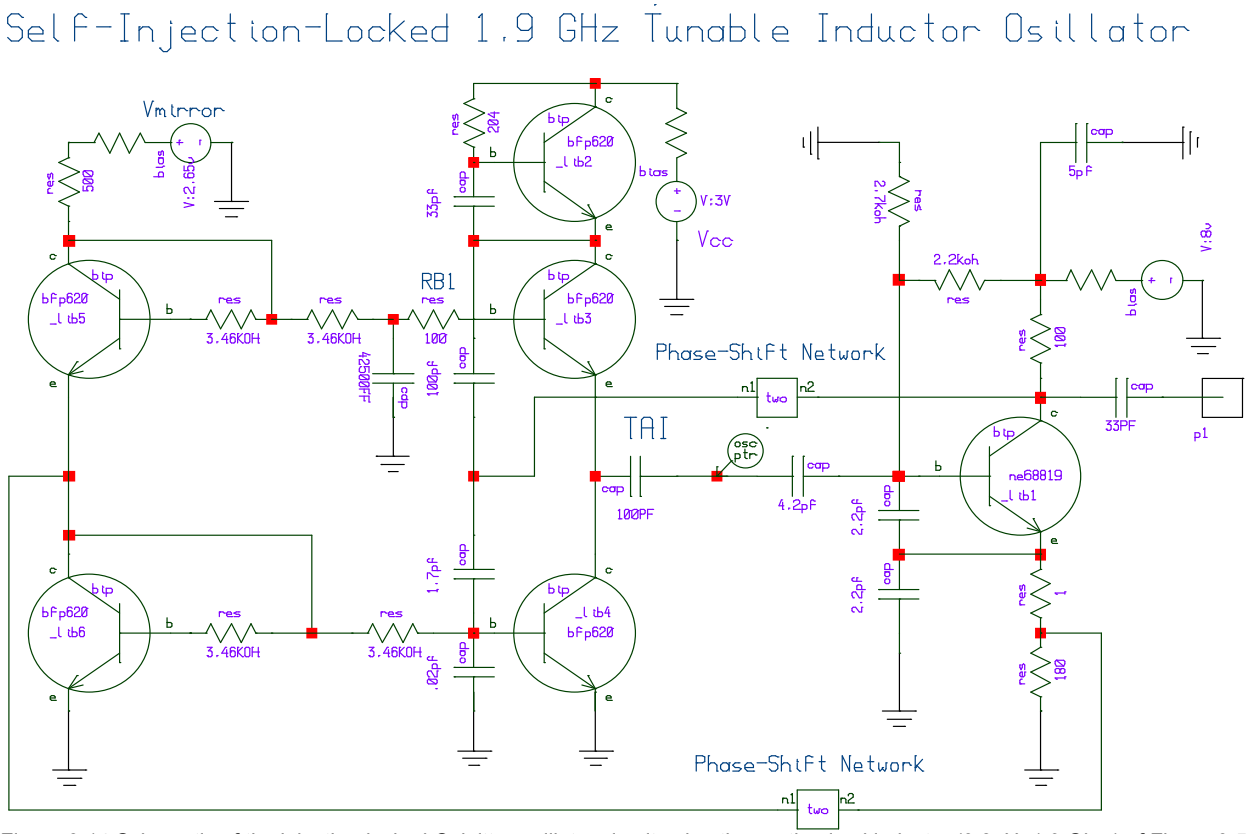


Figure 6-14 Schematic of the injection-locked Colpitts oscillator circuit using the synthesized inductor (0.8nH, 1.9 Ohm) of Figure 6-5

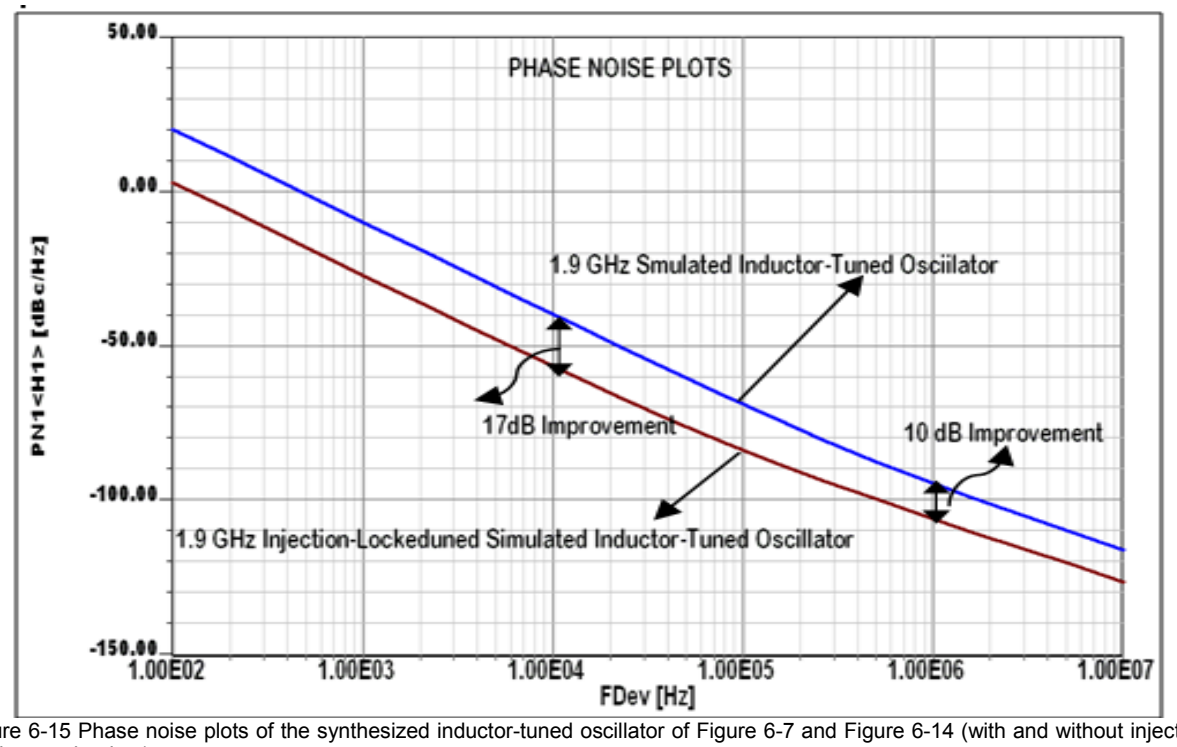


Figure 6-15 Phase noise plots of the synthesized inductor-tuned oscillator of Figure 6-7 and Figure 6-14 (with and without injection locking mechanism).

As shown in Figure 6-15, the self-injection locking mechanism improves phase noise by 17dB @ 100 kHz and 10dB @ 1MHz offset from the 1.9GHz carrier frequency. This observation is justified as injection-locking is more effective at lower offset (less than 100 kHz) and starts to degrade when the offset frequency exceeds 1MHz. This is due to a trade-off between phase shift and the broadband thermal noise with locking range for a given injection-level.

Figure 6-16 shows the measured phase noise plots of the injection-locked inductor-tuned oscillator circuit shown in Figure 6-14. It can be seen from Figure 6-16 that the measured phase noise plot shows superior performance at far offset frequencies and varies more than 10dB as compared to simulated phase noise plot (as shown in Figure 6-15). The reason for this discrepancy in phase noise characteristics is due to the package parasitic and convergence problem associated with CAD tools in the presence of the injection-locking signal, which is fed through delay line phase shifter network into the synthesized inductor circuit (Figure 6-14). The locking range of the injection-locked inductor-tuned oscillator can be described in terms of maximum change in frequency for a given operating condition. The oscillation frequency of the inductor-tuned oscillator can be tuned by varying the inductance of the synthesized inductor as

$$f_0 + \Delta f = \frac{1}{\sqrt{(L+\Delta L)C}} \approx f_0\left[1 - \frac{1}{2}\frac{|\Delta L|}{L}\right]_{\Delta L \ll L} \tag{6.23}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{6.24}$$

$$|\Delta f| \cong f_0\left[\frac{1}{2}\frac{\Delta L}{L}\right]_{\Delta L \ll L} \tag{6.25}$$

where ΔL and Δf, are the maximum change of the inductance of the synthesized inductor (shown in Figure 6-5) due to the injection-locking signal (realized using delay-line phase shifter as

shown in Figure 6-14), and the maximum frequency shifts that translates to locking range of the inductor-tuned oscillator [33].

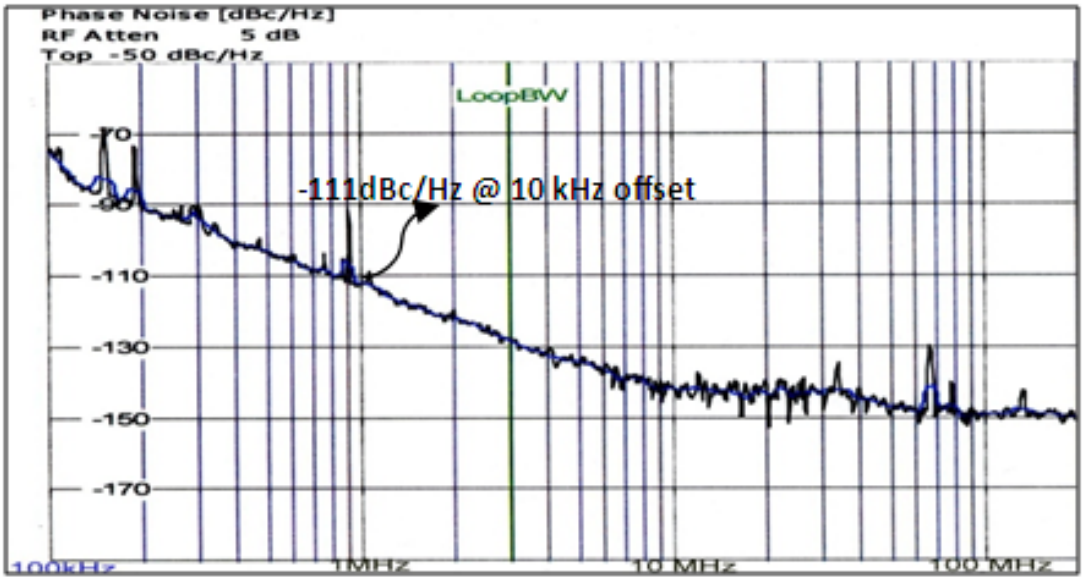


Figure 6-16 Measured phase noise plots of the injection-locked inductor-tuned oscillator circuit of Figure 6-14.

From Equation (6.25), the locking range of the injection-locked inductor-tuned oscillator is directly proportional to the maximum amount of the change of the inductance caused by the locking signal. Similarly, for a varactor-tuned injection-locked LC oscillator, the locking range can be described by

$$|\Delta f| \cong f_0 \left[\frac{1}{2}\frac{|\Delta C|}{C}\right]_{\Delta C \ll C} \tag{6.26}$$

where ΔC is the maximum amount of the change of the capacitance of the varactor caused by the locking signal.

For a given oscillator circuit topology, operating condition, and figure-of-merit, it is important to note that the maximum change of Δ*L* is higher than ΔC and can be given by [7]

$$\left[\frac{\Delta L}{L}\right]_{\Delta L \ll L} > \left[\frac{|\Delta C|}{C}\right]_{\Delta C \ll C} \tag{6.27}$$

From Equation (6.27), the synthesized injection-locked inductor-tuned oscillator has a superior ability to adjust and cause its frequency to follow the locking signal. It thus has a higher locking range as compared to varactor-tuned oscillator circuits. The higher locking range is exhibited in varactor-tuned oscillators, as there is minimum impact of the injected signal on output node voltages, giving an insignificant change in capacitance (ΔC) of the varactor devices. On the other hand, inductance of the synthesized inductor-tuned oscillator is more sensitive to the injected signal, and therefore, significantly varies the current of the active device that forms the synthesized inductor circuit (Figure 6-5). Another important consideration is the effects of large-signal voltage swings on the frequency tuning varactors in the LC-tank. It has been shown that the large signal output swing of the VCO modulates the varactor capacitance in time, resulting in a VCO tuning curve that deviates from the "DC" tuning curve of the particular varactor structure.

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7. Research Analysis and Validation

This research work develops a method to improve the Q-factor (quality factor) of synthesized inductor-tuned resonator circuits using SiGe HBTs for a high-frequency integrable low noise signal sources. This thesis also addresses the selection criteria, trade-offs, and possible solutions for enabling active inductor as the right candidate for tunable oscillators (where enhanced Q-factor plays important role) and for tunable filter circuits (where dynamic range is a dominating factor) [1]-[34].

7.1 Active Inductor Using SiGe HBTs Cascode Topology

Figure 7-1 shows the typical circuit schematic of an active inductor using the common-emitter cascode topology. The common-emitter cascode arrangement has been implemented with SiGe HBTs transistors (Q_1-Q_5) from Infineon (BFP620). The transistors Q_1 (common emitter) & Q_2 (common base) form the cascode to give high impedance. The output is fed back to the base of Q_1 through common base transistors Q_3 & Q_5. Transistor Q_5 is used as a voltage variable resistor. The base of Q_3 is grounded through resistor R_3, which controls the negative resistance of the active inductor. Transistor Q_4 is used as a current source.

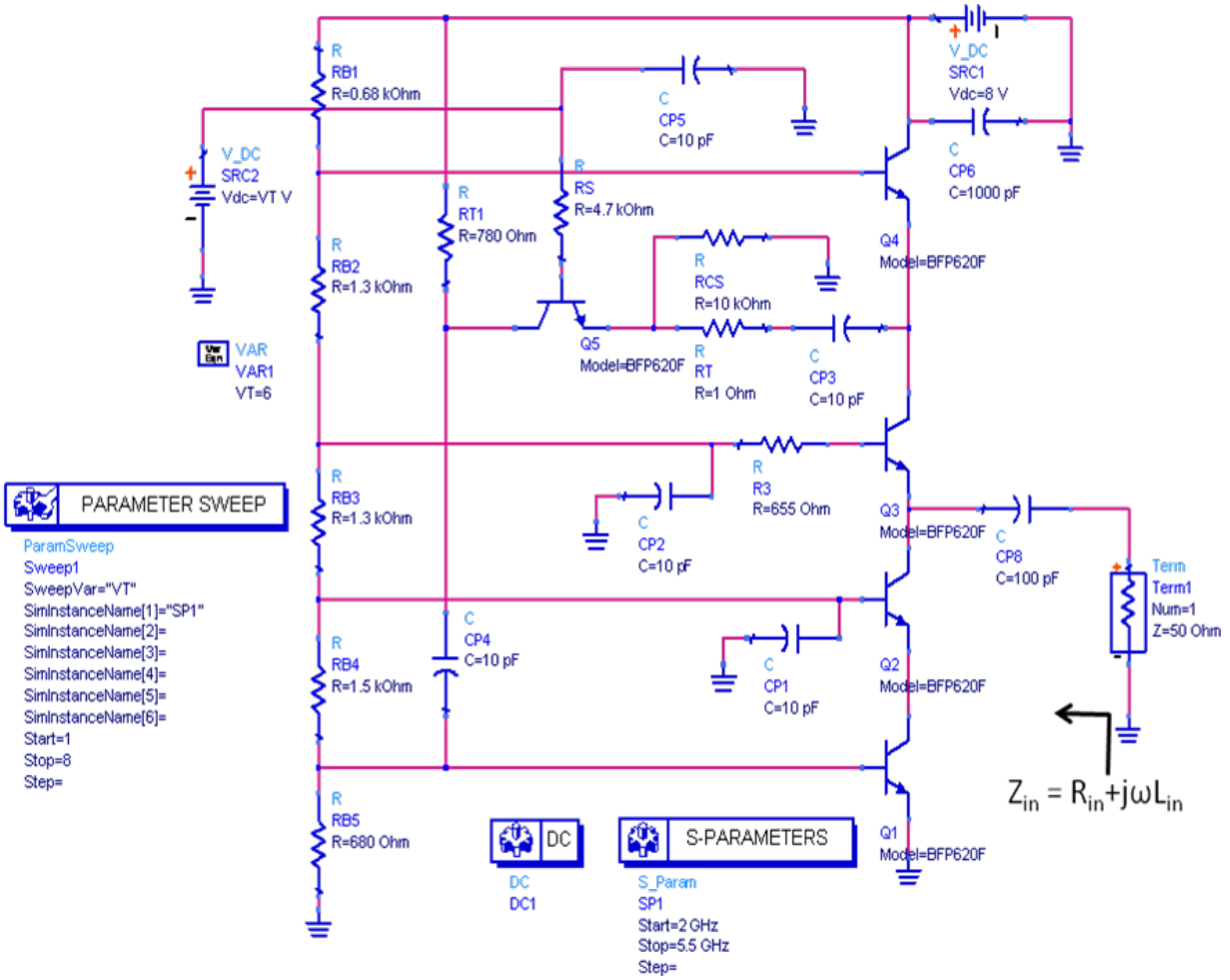

Figure 7-1 A typical schematic of an active inductor using cascode topology

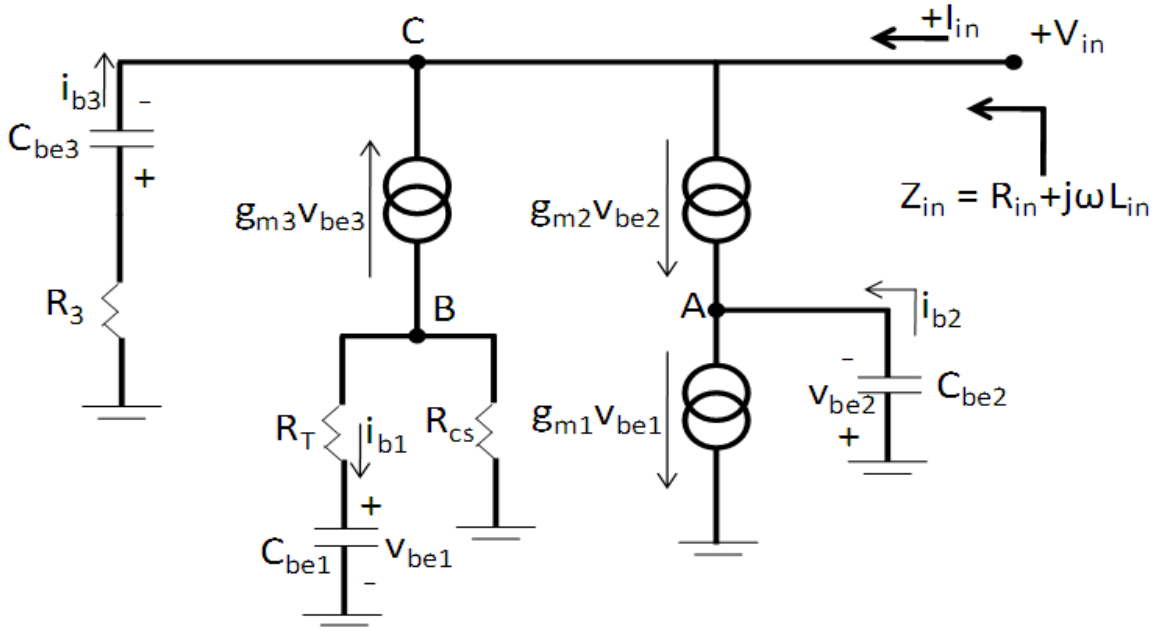

Figure 7-2 A simplified model of the tunable active inductor shown in Figure 7-1

Figure 7-2 shows the simplified equivalent circuit model of the active inductor shown in Figure 7-1. The transistors Q_1-Q_3 are represented only by their transconductance g_{mi} and base emitter capacitance C_{bei}. Transistors Q_4 and Q_5 are represented by resistances R_{CS} and R_T respectively.

Using nodal analysis the expression of inductance and equivalent series resistance can be described as follows:

Applying KCL at node 'C', we have

$$I_{in} = \frac{V_{in}}{R_3 + \frac{1}{j\omega C_{be3}}} + g_{m2}v_{be2} - g_{m3}v_{be3} \tag{7.1}$$

$$I_{in} = \frac{j\omega C_{be3}V_{in}}{1+j\omega C_{be3}R_3} + g_{m2}v_{be2} - g_{m3}v_{be3} \tag{7.2}$$

$$-v_{be3} = V_{in} - \frac{V_{in}R_3}{R_3 + \frac{1}{j\omega C_{be3}}} \tag{7.3}$$

$$-v_{be3} = V_{in} - \frac{j\omega C_{be3}V_{in}R_3}{1+ j\omega C_{be3}R_3} \tag{7.4}$$

$$v_{be3} = -\frac{V_{in}}{1+ j\omega C_{be3}R_3} \tag{7.5}$$

Applying KCL at node 'B', we have

$$i_{b1} = -\frac{g_{m3}v_{be3}R_{CS}}{R_{cs}+R_T+\frac{1}{j\omega C_{be1}}} = -\frac{j\omega C_{be1}g_{m3}v_{be3}R_{CS}}{1+ j\omega C_{be1}(R_{cs}+R_T)} \tag{7.6}$$

$$i_{b1} = \frac{j\omega C_{be1}g_{m3}R_{CS}V_{in}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][1+ j\omega C_{be3}R_3]} \tag{7.7}$$

Performing nodal analysis at node 'A', we have

$$v_{b1} = \frac{i_{b1}}{j\omega C_{be1}} = \frac{g_{m3}R_{CS}V_{in}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][1+ j\omega C_{be3}R_3]} \tag{7.8}$$

$$g_{m2}v_{be2} + i_{b2} = g_{m1}v_{be1} \tag{7.9}$$

$$g_{m2}v_{be2} + j\omega C_{be2}v_{be2} = g_{m1}v_{be1} \tag{7.10}$$

$$(g_{m2} + j\omega C_{be2})v_{be2} = g_{m1}v_{be1} \tag{7.11}$$

$$v_{be2} = \frac{g_{m1}v_{be1}}{g_{m2}+j\omega C_{be2}} = \frac{g_{m1}g_{m3}R_{CS}V_{in}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][1+ j\omega C_{be3}R_3][g_{m2}+j\omega C_{be2}]} \tag{7.12}$$

From Equation (7.3), we have

$$I_{in} = \frac{j\omega C_{be3}V_{in}}{1+j\omega C_{be3}R_3} + \frac{g_{m1}g_{m2}g_{m3}R_{CS}V_{in}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][1+ j\omega C_{be3}R_3][g_{m2}+j\omega C_{be2}]} + \frac{g_{m3}V_{in}}{1+ j\omega C_{be3}R_3} \tag{7.13}$$

$$I_{in} = \frac{(g_{m3}+j\omega C_{be3})V_{in}}{1+j\omega C_{be3}R_3} + \frac{g_{m1}g_{m2}g_{m3}R_{CS}V_{in}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][1+ j\omega C_{be3}R_3][g_{m2}+j\omega C_{be2}]} \tag{7.14}$$

$$I_{in} = \frac{V_{in}}{1+j\omega C_{be3}R_3}\left\{(g_{m3} + j\omega C_{be3}) + \frac{g_{m1}g_{m2}g_{m3}R_{CS}}{[1+ j\omega C_{be1}(R_{cs}+R_T)][g_{m2}+j\omega C_{be2}]}\right\} \tag{7.15}$$

$$I_{in} = \frac{V_{in}}{1+j\omega C_{be3}R_3}\left\{(g_{m3} + j\omega C_{be3}) + \frac{g_{m1}g_{m2}g_{m3}R_{CS}}{[g_{m2}- \omega^2 C_{be1}C_{be2}(R_{cs}+R_T)]+j\omega[g_{m2}C_{be1}(R_{cs}+R_T)+C_{be2}]}\right\} \tag{7.16}$$

Defining

$$\gamma = g_{m2} - \omega^2 C_{be1}C_{be2}(R_{cs} + R_T)$$

$$\delta = \omega[g_{m2}C_{be1}(R_{cs} + R_T) + C_{be2}]$$

$$\varphi = \frac{g_{m1}g_{m2}g_{m3}R_{CS}}{\gamma^2+\delta^2}$$

Substituting γ and δ from above in Equation (7.16), the expression of I_{in} can be described by

$$I_{in} = \frac{V_{in}}{1+j\omega C_{be3}R_3}\left\{(g_{m3} + j\omega C_{be3}) + \frac{g_{m1}g_{m2}g_{m3}R_{CS}}{\gamma+j\delta}\right\} \equiv \frac{V_{in}}{1+j\omega C_{be3}R_3}\left\{(g_{m3} + j\omega C_{be3}) + \frac{g_{m1}g_{m2}g_{m3}R_{CS}(\gamma-j\delta)}{\gamma^2+\delta^2}\right\} \tag{7.17}$$

Substituting for φ in Equation (7.17) the expression of I_{in}can be given by

$$I_{in} = \frac{V_{in}}{1+j\omega C_{be3}R_3}\{(g_{m3} + j\omega C_{be3}) + \varphi(\gamma - j\delta)\} \equiv \frac{V_{in}}{1+j\omega C_{be3}R_3}\{(g_{m3} + \varphi\gamma) + j(\omega C_{be3} - \varphi\delta)\} \tag{7.18}$$

The input impedance Z_{in} is given by

$$Z_{in} = R_{in} + jX_{in} = \frac{V_{in}}{I_{in}} = \frac{1+j\omega C_{be3}R_3}{(g_{m3}+\varphi\gamma)+j(\omega C_{be3}-\varphi\delta)} \equiv \frac{(1+j\omega C_{be3}R_3)\{(g_{m3}+\varphi\gamma)-j(\omega C_{be3}-\varphi\delta)\}}{(g_{m3}+\varphi\gamma)^2+(\omega C_{be3}-\varphi\delta)^2} \quad (7.19)$$

$$Z_{in} \equiv \frac{(g_{m3}+\varphi\gamma)+\omega C_{be3}R_3(\omega C_{be3}-\varphi\delta))+j\{\omega C_{be3}R_3(g_{m3}+\varphi\gamma)-(\omega C_{be3}-\varphi\delta)\}}{(g_{m3}+\varphi\gamma)^2+(\omega C_{be3}-\varphi\delta)^2} \quad (7.20)$$

$$R_{in} = \frac{(g_{m3}+\varphi\gamma)+\omega C_{be3}R_3(\omega C_{be3}-\varphi\delta))}{(g_{m3}+\varphi\gamma)^2+(\omega C_{be3}-\varphi\delta)^2} \quad (7.21)$$

$$X_{in} = \omega L_{in} = \frac{\omega C_{be3}R_3(g_{m3}+\varphi\gamma)-(\omega C_{be3}-\varphi\delta)}{(g_{m3}+\varphi\gamma)^2+(\omega C_{be3}-\varphi\delta)^2} \quad (7.22)$$

$$L_{in} = \frac{1}{\omega}\left\{\frac{\omega C_{be3}R_3(g_{m3}+\varphi\gamma)-(\omega C_{be3}-\varphi\delta)}{(g_{m3}+\varphi\gamma)^2+(\omega C_{be3}-\varphi\delta)^2}\right\} \quad (7.23)$$

Where

$\omega = 2\pi f$, $g_{mi} = \frac{\beta_i}{h_{iei}}$, where β_i is the current gain and h_{iei} is the input impedance of the ith transistor. The transistors Q_1 to Q_4 (Figure 7-1) are biased at (2V, 27mA). For simplification of the analysis, all the transistor parameters are identical ($C_{be1} \approx C_{be2} \approx C_{be3} = C_{be}$ and $g_{m1} \approx g_{m2} \approx g_{m3} = g_m$).

From Equation (7.21) and Equation (7.22),

$$R_{in} = \frac{(g_m+\varphi\gamma)+\omega C_{be}R_3(\omega C_{be}-\varphi\delta))}{(g_m+\varphi\gamma)^2+(\omega C_{be}-\varphi\delta)^2} \quad (7.24)$$

$$L_{in} = \frac{1}{\omega}\left\{\frac{\omega C_{be}R_3(g_m+\varphi\gamma)-(\omega C_{be}-\varphi\delta)}{(g_m+\varphi\gamma)^2+(\omega C_{be}-\varphi\delta)^2}\right\} \quad (7.25)$$

Where

$$\gamma = g_m - (\omega C_{be})^2(R_{cs} + R_T)$$

$$\delta = \omega[g_m C_{be}(R_{cs} + R_T) + C_{be}]$$

$$\varphi = \frac{g_m{}^3 R_{CS}}{\gamma^2+\delta^2}$$

From Equation (7.2) through Equation (7.25), it can be analytically shown that a wide range of inductance values can be synthesized, for a wide range of positive and negative series resistance values. Figure 7-3 shows the CAD simulated plot of $S(1,1)$ for the circuit shown in Figure 7-1 (with V_T = 2V and frequency swept from 500 MHz to 6 GHz). The required Gummel-Poon model and package parasitic for BFP620F were obtained from the datasheet of BFP620 provided by Infineon.

It can be seen from Figure 7-4 that a wideband inductance is realized and at frequencies above 4 GHz the series resistance of the realized inductance exhibits negative values. This topology is well suited at 10 GHz and above for the realization of active inductor oscillator. The impedance exhibits a negative series resistance to overcome the loss of the integrated resonator, which in this case is a bare minimum. Figure 7-4 shows the variation of inductance and series loss resistance with the applied tuning voltage V_T. The value of inductance varies from about 2.4nH to 1.0nH at 4GHz with negative series loss resistance. From the theoretical analysis and CAD

simulations (shown in Figure 7-4), it is obvious that an active inductor tunable oscillator has the advantages of wider tuning ranges and integrable solutions in smaller chip area. The typical circuit schematic as shown in Figure 7-1 can be realized using TSMC's 0.35 um SiGe RF process for integrated applications of low cost tunable oscillator signal sources for wireless applications.

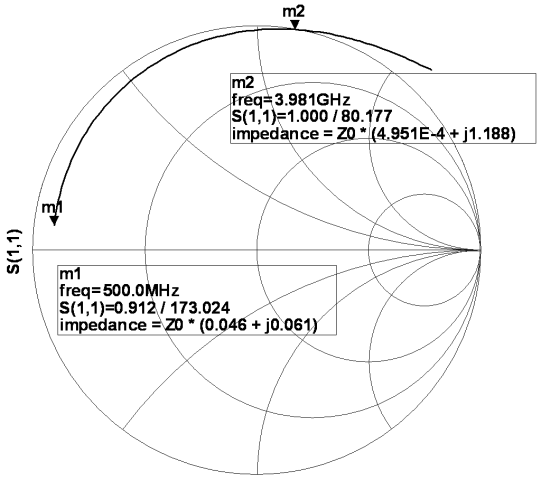

Figure 7-3 CAD simulated plot of S(1,1) for the circuit of Figure 7-1 (with V_T=2V)

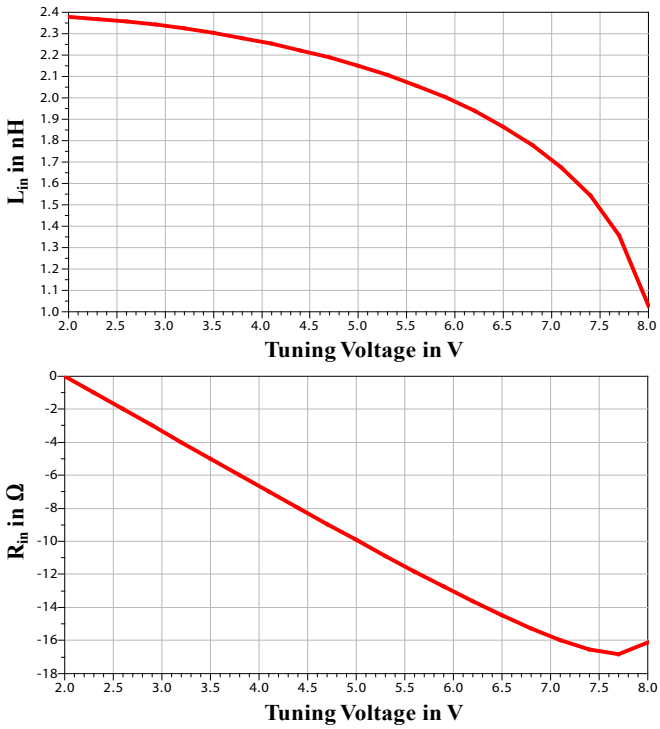

Figure 7-4 CAD simulated plots of the variation of inductance and series loss resistance at 4GHZ for the TAI circuit of Figure 7-1.

7.2 High Q-Factor Tunable Active Inductor Using SiGe HBTs

In general, a high-Q factor tunable inductor circuit can be implemented by two common methods: (1) passive lumped inductors, actively coupled and (2) active inductors, passively coupled. With both methods, negative resistances can be introduced at proper nodes/ports to compensate the dissipative loses in the inductors to realize high-Q tunable inductor circuits [14]. High Q-factor inductors can be classified into two groups: (1) passive inductor with resistive loss compensating circuits, and (2) active inductor (using phase shift and feedback techniques realized by transistors) [3]-[18].

With monolithic microwave integrated circuit (MMIC) technology, large inductances are traditionally realized using spiral or stacked spiral inductors [1]. Unfortunately, these inductors can suffer from excess series resistance and undesirable high-frequency resonances. Thus, the spiral inductors can place a fundamental limit on the performance of an associated circuit. As a result a considerable amount of interest has been shown in the use of active inductors including an alternative to varactor-tuned resonator networks.

A spiral inductor greater than 1nH, can occupy most of the die area of an IC. This can restrict the application due to cost, size, and limited Q at RF and microwave frequencies. To overcome this problem, high value spiral inductors (L_{spiral}) are replaced by feedback parallel ($L_f\ C_v$) resonant circuits using gyrator networks where the value of inductance L_f can be lowered to the realizable integrable value ($< L_{\text{spiral}}$) in standard ICs [13].

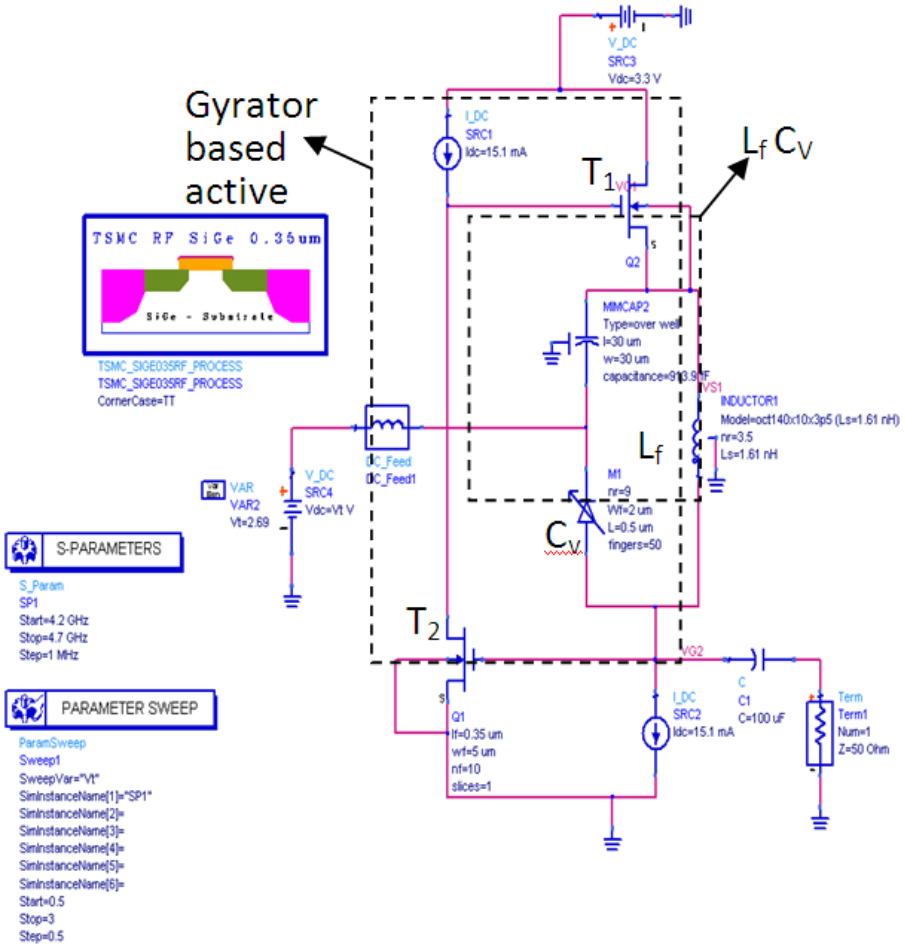

Figure 7-5 Schematic of the varactor tuned transistorized high-Q active inductor for broadband tunable oscillator, filter, and phase-shifter circuit applications.

Figure 7-5 shows the schematic of the high-Q inductor using a tunable LC resonant circuit (HITR) consisting of the conventional active grounded inductor and feedback parallel resonant circuit. The Q factor of the inductor can be improved by incorporating a grounded gyrator structure in conjunction with the parallel ($L_f\ C_v$) resonator network composed of a low-Q spiral inductor and MOS varactor.

As shown in Figure 7-5, the parallel ($L_f\ C_v$) resonator is connected between the gate of T_1 and the source of T_2. The effective inductance of the parallel ($L_f\ C_v$) resonance network is described by

$$Z_{reso} = j\omega L_{reso} = \frac{j\omega L_f}{1-\omega^2 L_f C_v} \tag{7.26}$$

From Equation (7.26), large inductance value L_{reso} can be realized using a minimum value of the spiral inductor under the constraints of cost and die size for a given integrated circuit technology. The typical inductance value in $(L_f\ C_v)$ resonator is 1.61nH and the MOS varactor operates in accumulation-mode. The resonance frequency is set by varying the varactor control voltage.

Figure 7-6 shows the CAD simulated (ADS 2010) plot that illustrate the Q-factor versus frequency for the active inductor network shown in Figure 7-5. Figure 7-7 shows the plot of inductance variation of the varactor-tuned high-Q active inductor, which depicts the large variation of inductance with improved unloaded Q-factor. The power consumption is a major concern for the realization of high Q integrable inductor, and current topology (Figure 7-5) consumes typically 100mW for a 3.3V supply voltage.

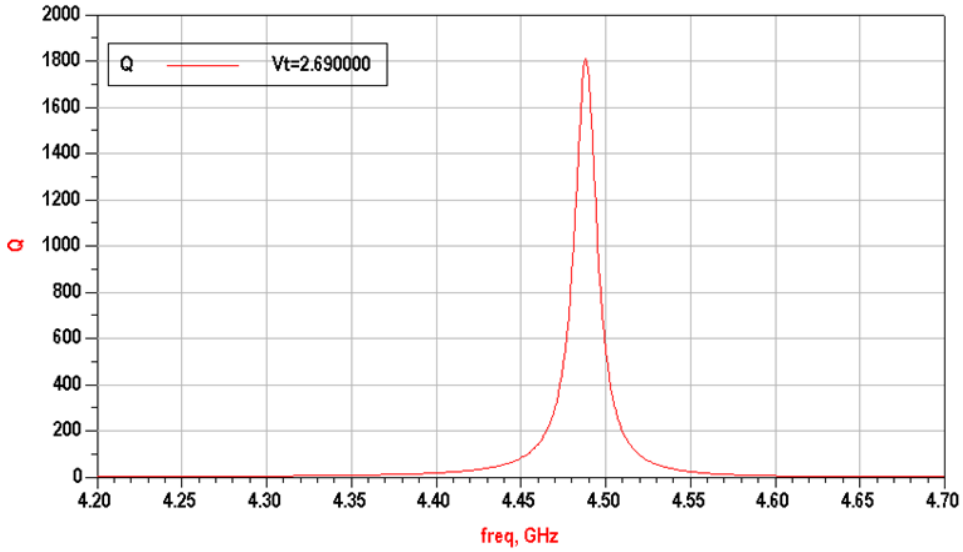

Figure 7-6 CAD simulated plot (ADS 2010) that shows the Q- factor versus frequency for the active inductor network of Figure 7-5.

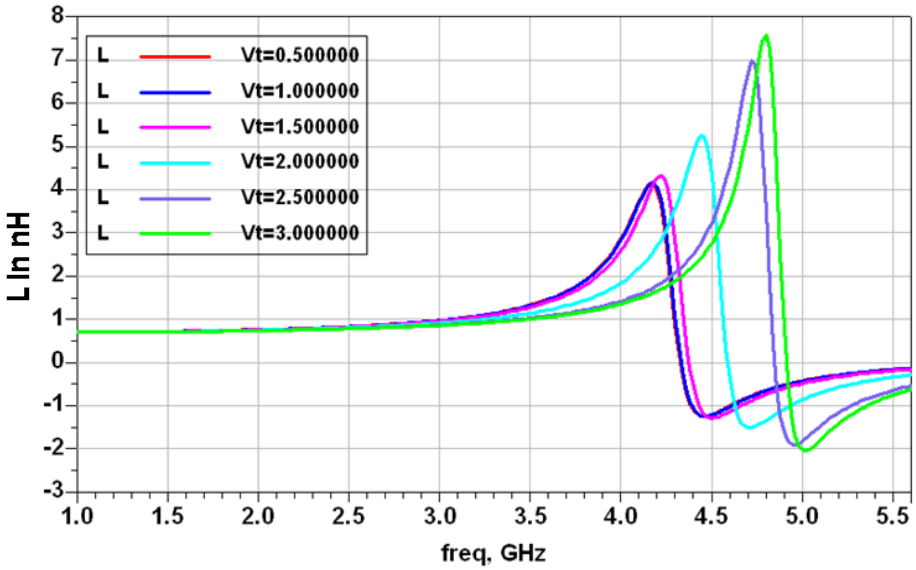

Figure 7-7 CAD simulated plot (ADS) of the varactor-tuned active inductor network as of Figure 7-5.

As shown in Figure 7-7, the maximum value of inductance is about 7.5nH at 4.8 GHz, which is a significantly higher value than the conventional topology for a given figure-of-merit and die-size in standard RFICs/MMICs [13]. Although the varactor-tuned active inductor of Figure 7-5 exhibits a broadband tuning range with improved Q-factor, the tuning diode in the parallel feedback network ($L_f\ C_v$) limits the applications. The current trend moves towards varactor-less reconfigurable radio-frequency circuit solutions using a differential active inductor topology.

7.3 Differential Active Inductor Topology

Figure 7-8 shows the basic circuit diagram of the typical 2-port differential active inductor topology [15]. The inductor is implemented using SiGe HBT transistors Q_1 to Q_4 (BFP620F from Infineon). The transistors Q_1 & Q_2 and are biased at (2V, 21mA) and Q_3 and Q_4 are biased at (2.5V, 21mA).

Figure 7-9 shows the simplified version of the equivalent representation of the circuit of Figure 7-8, where $G_1 = 1/R_1$ and $G_2 = 1/R_2$. Assuming DC bias conditions across the base of the transistors Q_1 & Q_3 and Q_2 & Q_4 are common, we have $v_{be1} = v_{be3}$ and $v_{be2} = v_{be4}$. C_1 & C_2 are large value capacitors used for DC decoupling. The transformer converts the single ended input to differential and is used for measurement and verification purposes only.

Applying conventional nodal analysis at node 'A' we have

$$I_{in} + g_{m1}v_{be1} + g_{m3}v_{be1} + i_{b1} + i_{b3} = 0 \tag{7.27}$$

$$I_{in} + g_{m1}v_{be1} + g_{m3}v_{be1} + j\omega C_{be1}v_{be1} + j\omega C_{be3}v_{be1} = 0 \tag{7.28}$$

$$I_{in} + v_{be1}(g_{m1} + g_{m3} + j\omega C_{be1} + j\omega C_{be3}) = 0 \tag{7.29}$$

$$v_{be1} = \frac{-I_{in}}{g_{m1}+g_{m3}+j\omega C_{be1}+j\omega C_{be3}} \tag{7.30}$$

Because of the differential nature of the circuit we have,

$$v_{be2} = -v_{be1} = \frac{I_{in}}{g_{m1}+g_{m3}+j\omega C_{be1}+j\omega C_{be3}} \tag{7.31}$$

where $$g_{m1} = g_{m2} \tag{7.32}$$

Applying conventional nodal analysis at node 'B' we have

$$i_{b1} + i_{b3} + v_{b1}G_1 + g_{m2}v_{be2} = 0 \tag{7.33}$$

From Equation (7.30) and Equation (7.31) we have

$$i_{b1} + i_{b3} + v_{b1}G_1 - g_{m1}v_{be1} = 0 \tag{7.34}$$

$$j\omega C_{be1}v_{be1} + j\omega C_{be3}v_{be1} + v_{b1}G_1 - g_{m1}v_{be1} = 0 \tag{7.35}$$

Since

$$v_{b1} = v_{be1} + v_{e1} \tag{7.36}$$

$$v_{b1} = v_{be1} + \frac{V_{in}}{2} \tag{7.37}$$

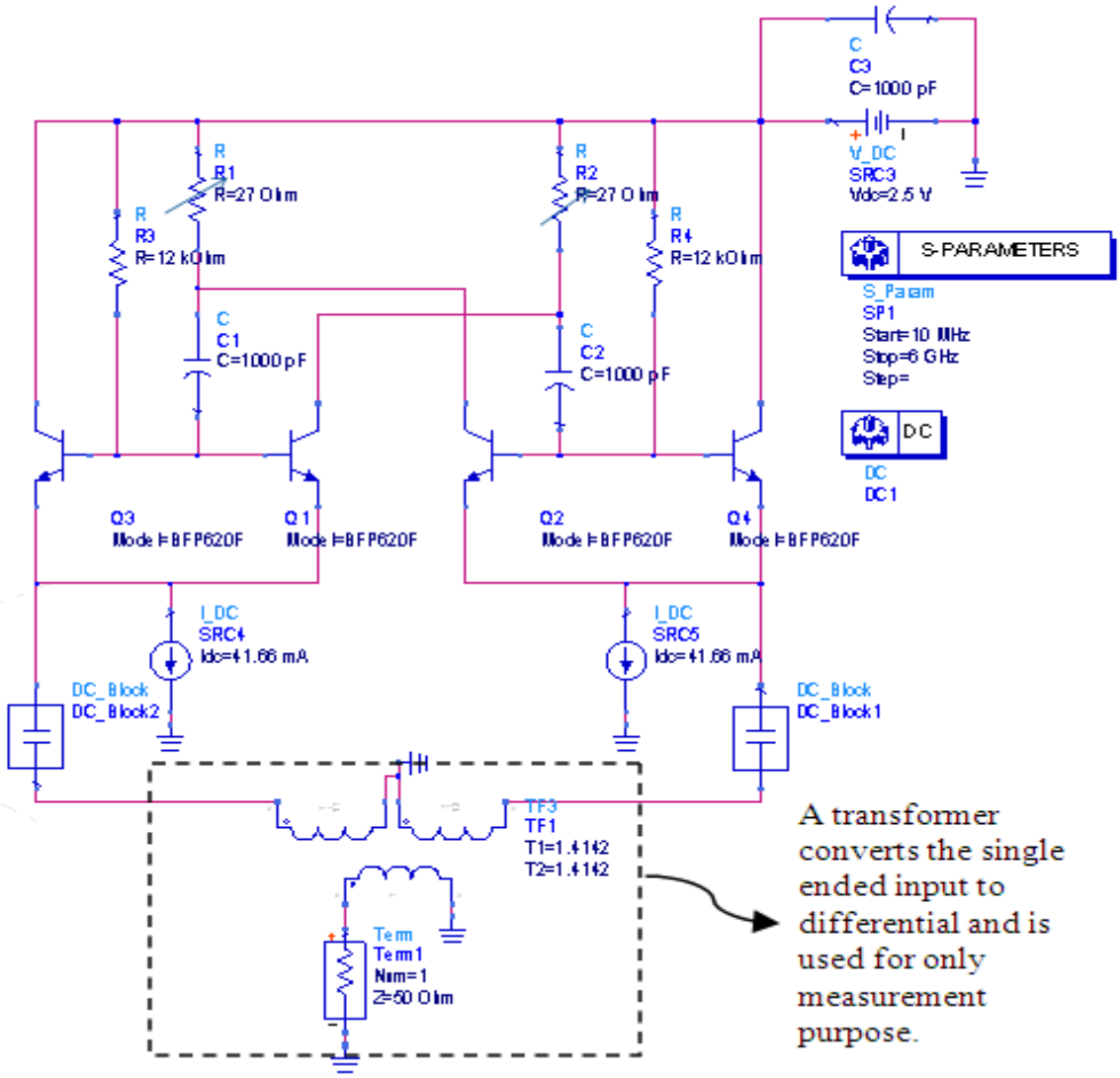

Figure 7-8 Schematic of the 2-port differential active inductor

By substituting Equation (7.36) in Equation (7.34) we have,

$$j\omega C_{be1} v_{be1} + j\omega C_{be3} v_{be1} + \left(v_{be1} + \frac{V_{in}}{2}\right) G_1 - g_{m1} v_{be1} \Longrightarrow$$

$$[j\omega C_{be1} + j\omega C_{be3} + G_1 - g_{m1}] v_{be1} = \frac{-G_1 V_{in}}{2} \tag{7.38}$$

$$v_{be1} = \frac{-G_1 V_{in}}{2[j\omega C_{be1} + j\omega C_{be3} + G_1 - g_{m1}]} \tag{7.39}$$

From Equation (7.30) we have,

$$v_{be1} = \frac{-G_1 V_{in}}{2[j\omega C_{be1} + j\omega C_{be3} + G_1 - g_{m1}]} = \frac{-I_{in}}{g_{m1} + g_{m3} + j\omega C_{be1} + j\omega C_{be3}} \tag{7.40}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2[j\omega(C_{be1}+C_{be3})+G_1-g_{m1}]}{G_1[g_{m1}+g_{m3}+j\omega(C_{be1}+C_{be3})]} \tag{7.41}$$

$$Z_{in} = \frac{2[j\omega(C_{be1}+C_{be3})+G_1-g_{m1}]\times[g_{m1}+g_{m3}-j\omega(C_{be1}+C_{be3})]}{G_1[(g_{m1}+g_{m3})^2+\omega^2(C_{be1}+C_{be3})^2]} \tag{7.42}$$

$$Z_{in} = \frac{2[j\omega(C_{be1}+C_{be3})(2g_{m1}+g_{m3}-G_1)+(G_1-g_{m1})(g_{m1}+g_{m3})+\omega^2(C_{be1}+C_{be3})^2]}{G_1[(g_{m1}+g_{m3})^2+\omega^2(C_{be1}+C_{be3})^2]} \tag{7.43}$$

$$Z_{in} = \frac{2[\{(G_1-g_{m1})(g_{m1}+g_{m3})+\omega^2(C_{be1}+C_{be3})^2\}+j\omega(C_{be1}+C_{be3})(2g_{m1}+g_{m3}-G_1)]}{G_1[(g_{m1}+g_{m3})^2+\omega^2(C_{be1}+C_{be3})^2]} \tag{7.44}$$

For $Z_{in} = (R_{in} + j\omega L_{in})$,

$$L_{in} = \frac{2(C_{be1}+C_{be3})(2g_{m1}+g_{m3}-G_1)}{G_1[(g_{m1}+g_{m3})^2+\omega^2(C_{be1}+C_{be3})^2]} \tag{7.45}$$

$$R_{in} = \frac{2[(G_1-g_{m1})(g_{m1}+g_{m3})+\omega^2(C_{be1}+C_{be3})^2]}{G_1[(g_{m1}+g_{m3})^2+\omega^2(C_{be1}+C_{be3})^2]} \tag{7.46}$$

From Equation (7.27) to Equation (7.46), we notice that by varying G_1 (R_1) and G_2 (R_2) the inductance can be varied. Figure 7-10 and Figure 7-11 show the CAD simulated plots of the variation of the inductance and the series resistance at 3GHz with R_1 and R_2 respectively. The CAD simulation was performed at 3GHz with R_1 (& R_2) varying from 15 Ω to 50 Ω.

Figure 7-12 and Figure 7-13 show the variation of inductance and series resistance with respect to frequency for R_1 (& R_2) = 27 Ω. It can be seen from the results that the realized inductance is relatively constant over a broad bandwidth.

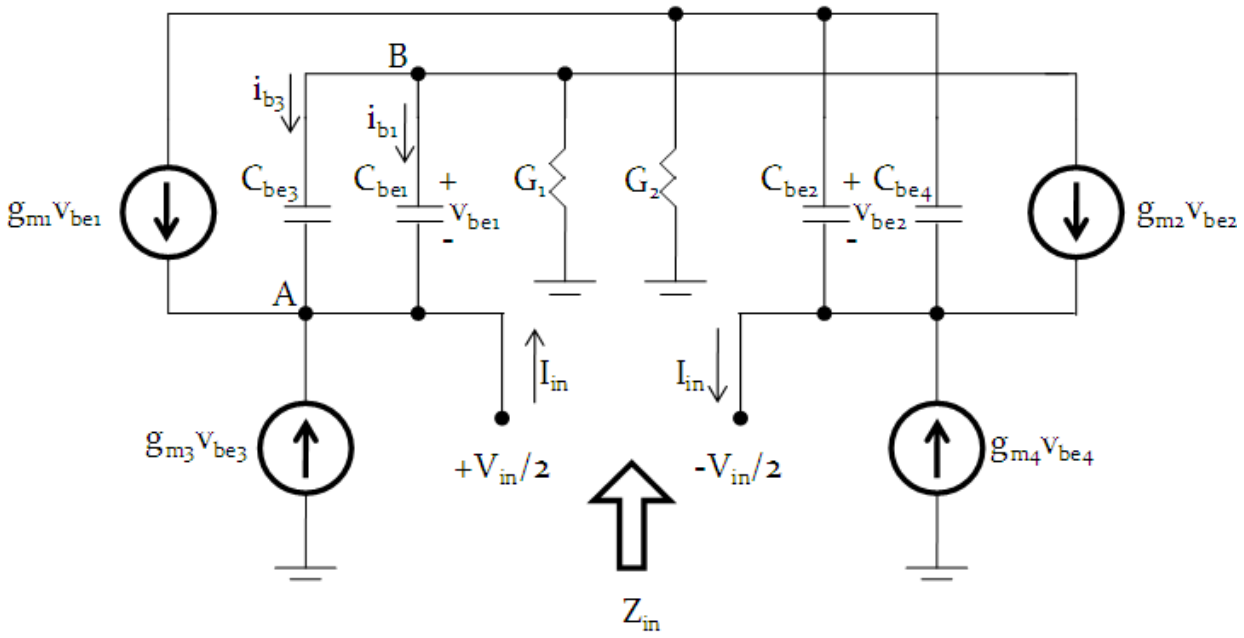

Figure 7-9 Equivalent circuit representation of the circuit shown in Figure 7-8

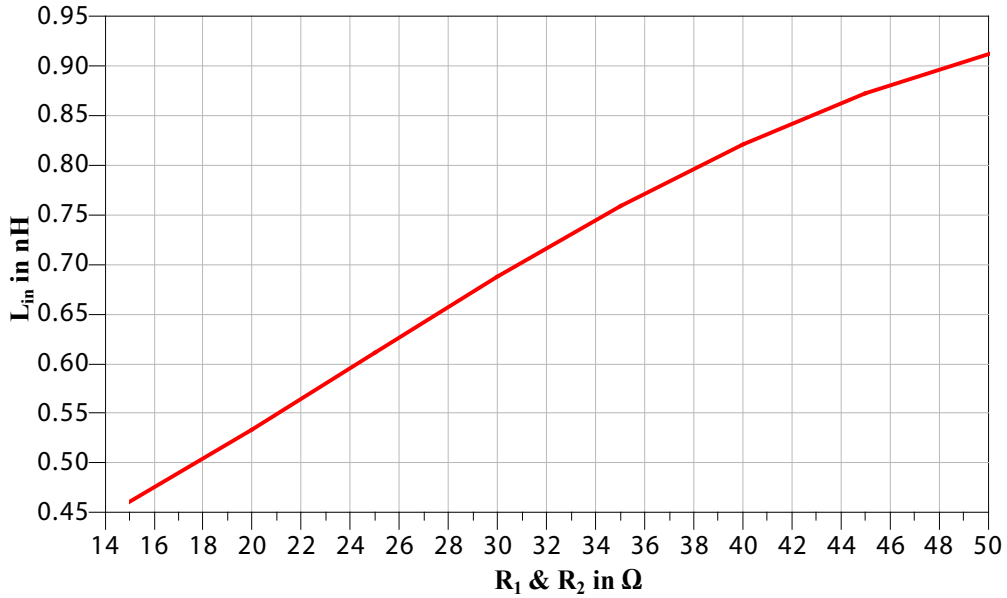

Figure 7-10 Simulated plot of the variation of L_{in} vs. R_1 (& R_2) at 3GHz

To tune the inductance of the circuit shown in Figure 7-8, we need variable resistors (R_1 and R_2). Figure 7-14 shows the circuit schematic of the active tunable inductor (ATI) where the voltage variable resistors are implemented using R_1 and Q_5 & R_2 and Q_6. As V_T increases the collector load of the transistors Q_1 and Q_2 reduces which reduces the realized inductance value.

Figure 7-15 and Figure 7-16 show the CAD simulated plot of the variation of L_{in} and R_{in}, respectively, at 3GHz with the applied tuning voltage (V_T) respectively. Figure 7-17 and Figure 7-18 show the simulated frequency variation of L_{in} and R_{in} respectively for V_T = 3V. It can be seen from the results that even though the R_{in} varies with frequency, a very broadband inductance can be realized.

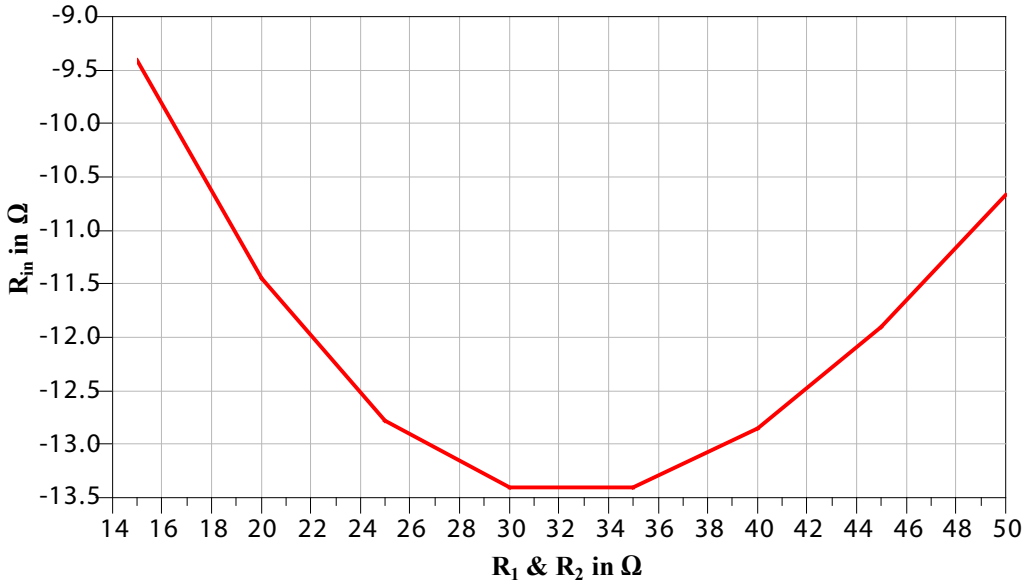

Figure 7-11 Simulated plot of the variation of R_{in} vs. R_1 (& R_2) at 3GHz

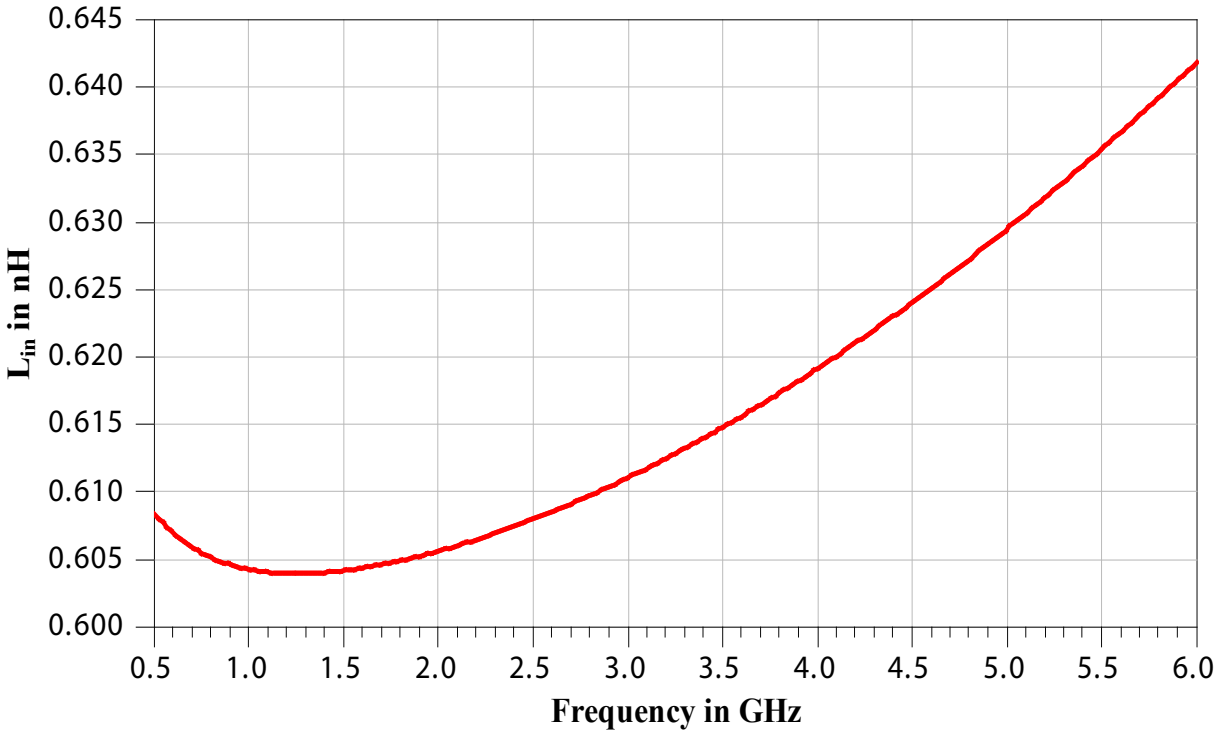

Figure 7-12 Simulated plot of the variation of L_{in} vs. frequency at $R_1 = R_2 = 27\Omega$

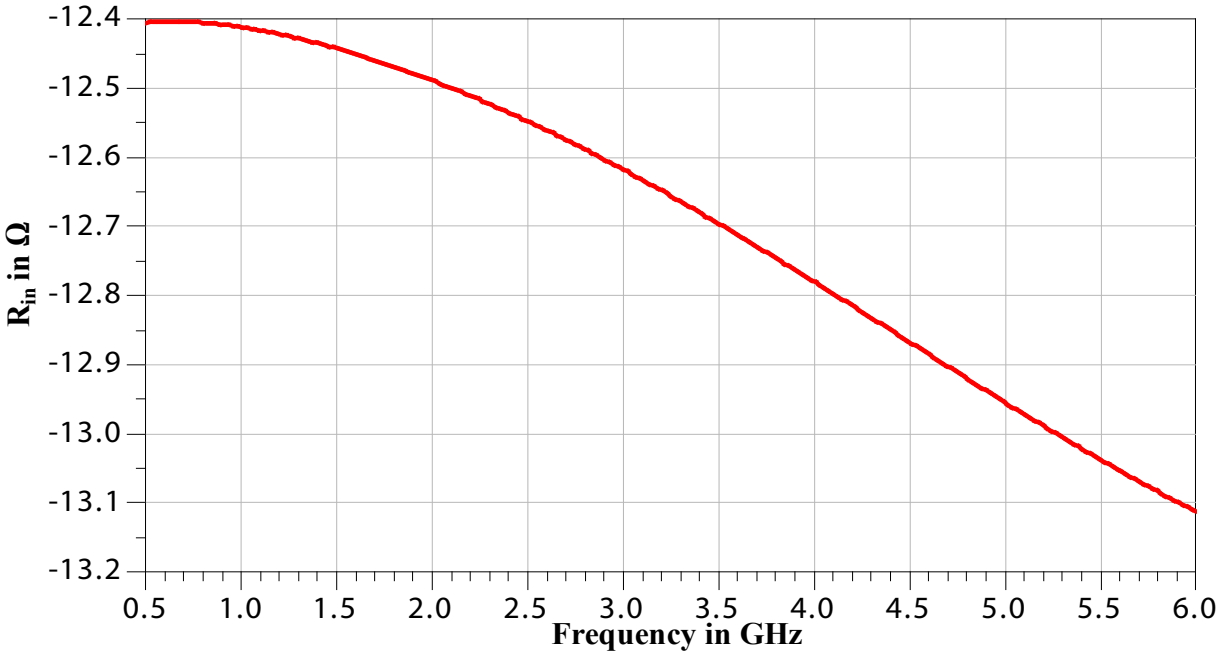

Figure 7-13 Simulated plot of the variation of R_{in} vs. frequency at $R_1 = R_2 = 27\Omega$

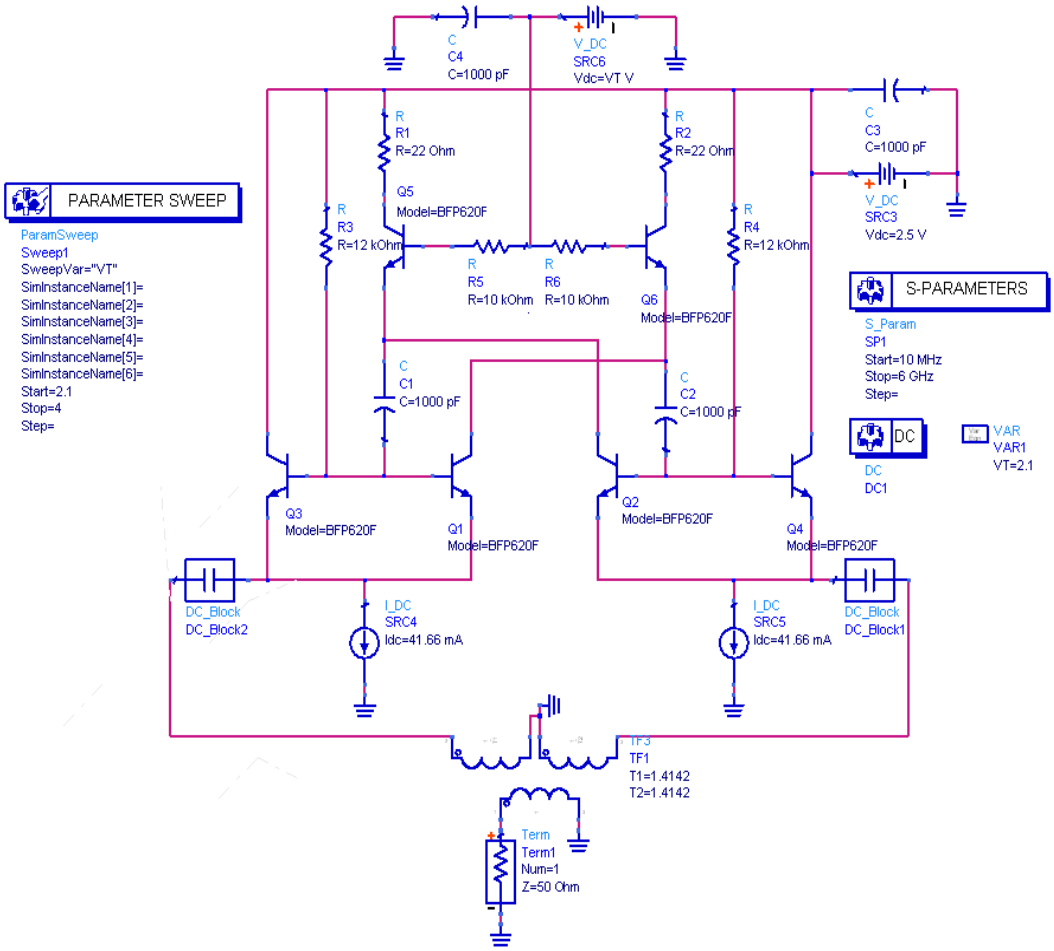

Figure 7-14 Circuit schematic of the transistorized tunable inductor circuit where the voltage variable resistor is implemented using R_1 & Q_5 (& R_2 and Q_6)

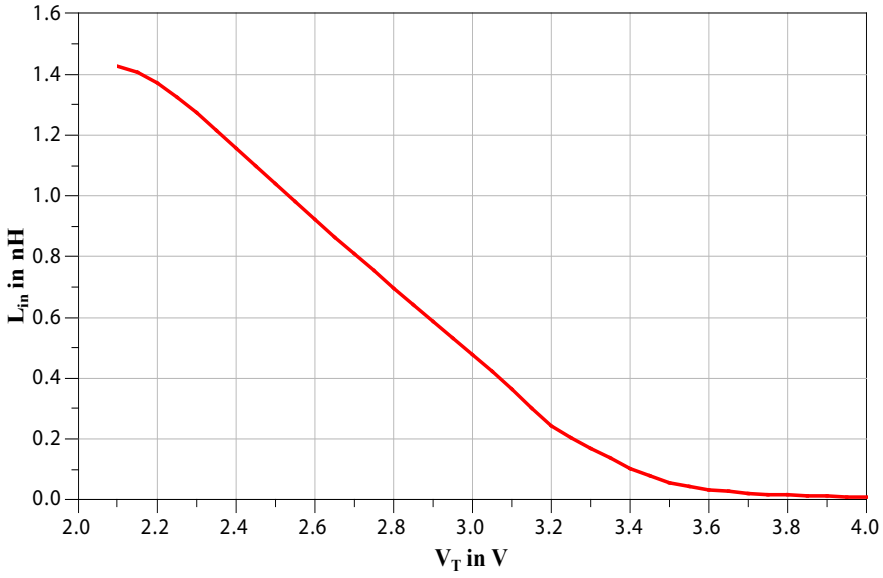

Figure 7-15 The variation of inductance vs. tuning voltage at 3GHz

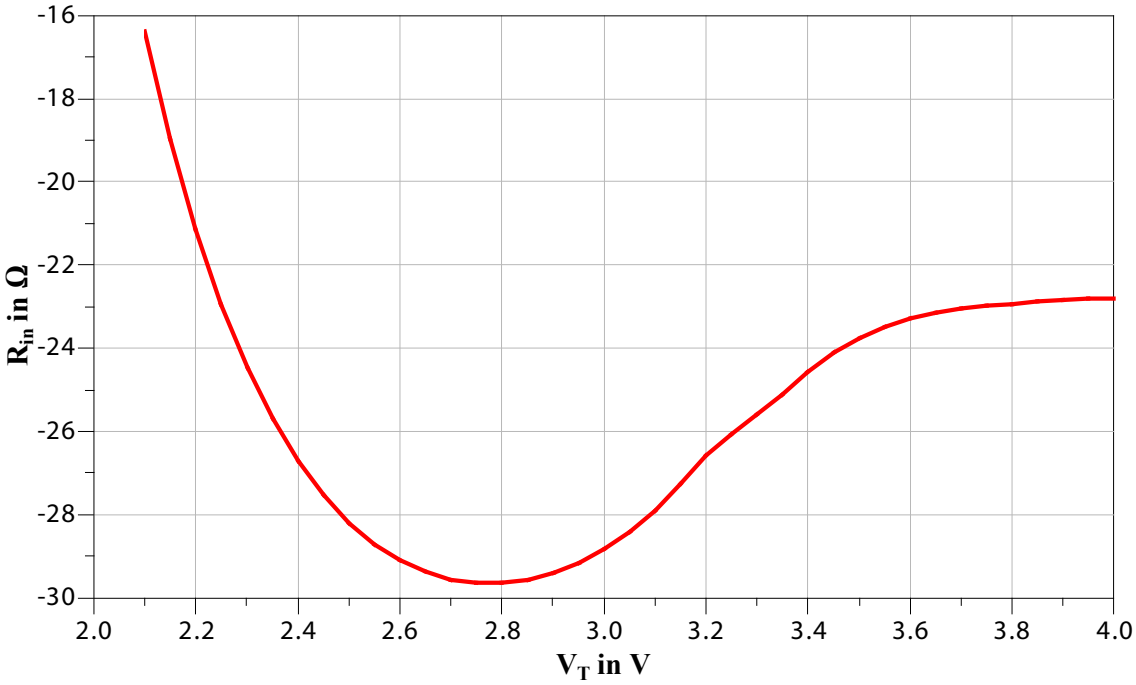

Figure 7-16 The variation of series resistance vs. tuning voltage at 3GHz

7.4 A 700MHz Tunable Active Inductor Oscillator

Figure 7-17shows a basic active tunable inductor [36] circuit realized using SiGe HBT's.

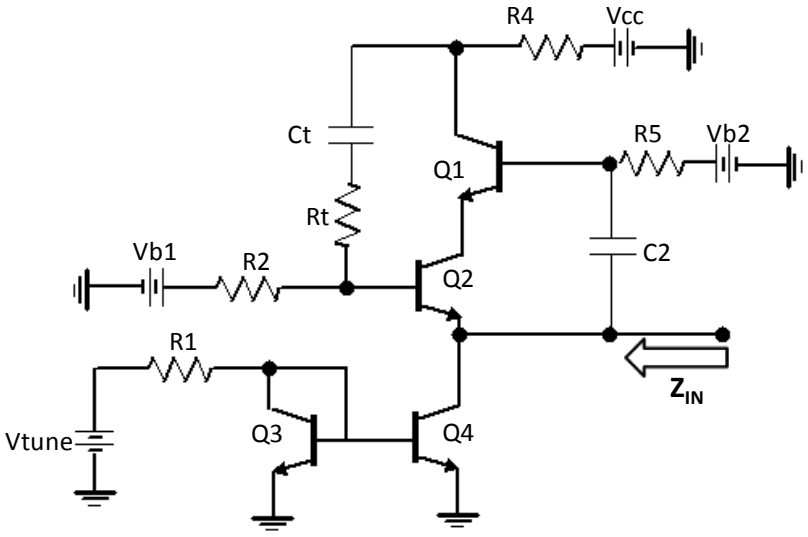

Figure 7-17 A typical Active Tunable Inductor (ATI) circuit

The transistors Q1 and Q2 form the active portion of the inductor. The transistors Q3 and Q4 form a current mirror circuit. The current through Q1 and Q2 are set by using this current mirror. It is assumed that Q1 and Q2 are similar devices and are biased at the same current. Hence we can assume that both Q1 and Q2 have the same transconductance (G_m) and base to emitter capacitance (C_{be}). It was observed that the input impedance Z_{IN} varies with the current I_C through Q2.

7.4.1 Small Signal Analysis of ATI

Figure 7-18 shows the simplified representation of the active tunable inductor circuit of Figure 7-17.

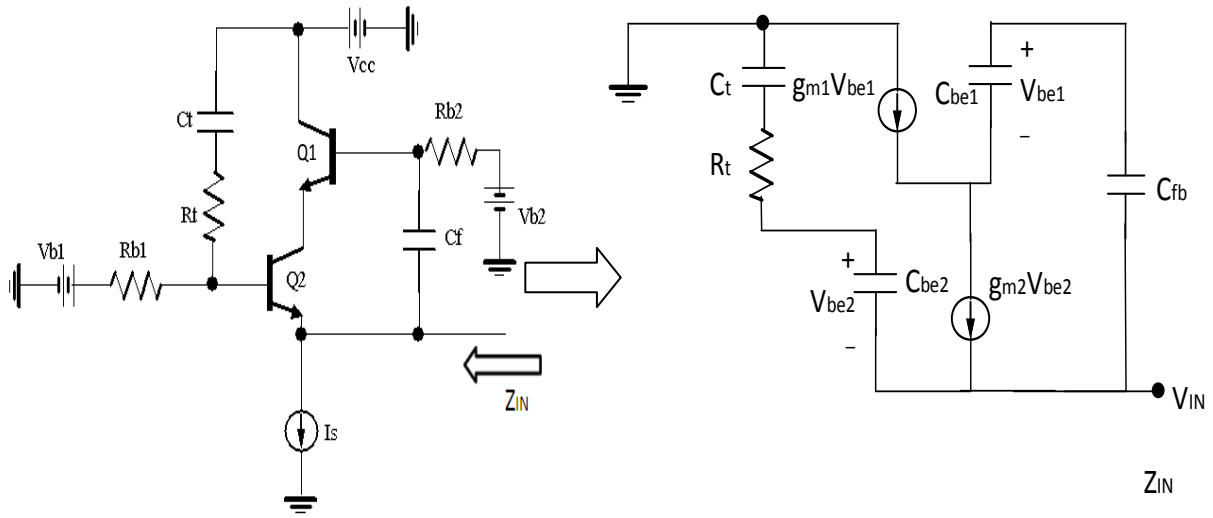

Figure 7-18 Simplified representation of an active tunable inductor circuit of Figure 7-17.

For small-signal analysis, all the DC voltage sources are short circuited and the current sources are open circuited. The bias resistors Rb1 and Rb2 are high resistance values and can be considered to be open. The transistors Q1 and Q2 are replaced by their equivalent Pi-models (Figure 7-19).

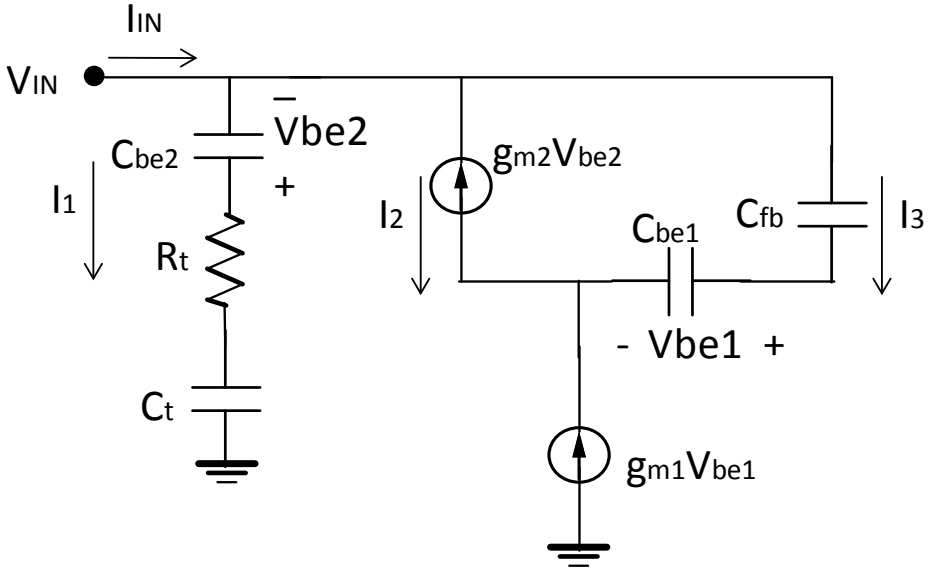

Figure 7-19 Small signal model of ATI (Figure. 7-17)

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{[j\omega C_{be2} R_t + \left(\frac{C_{be2}+C_t}{C_t}\right)]}{g_{m2}} \tag{7.47}$$

Assuming $C_t >> C_{be2}$, we get

$$Z_{IN} = \frac{[j\omega C_{be2} R_t + 1]}{g_{m2}} \quad (7.48)$$

$$\text{i.e.} \quad Z_{IN} = R_{IN} + j\omega L_{IN} \quad (7.49)$$

where inductance, $L_{IN} = \frac{C_{be2} R_t}{g_{m2}}$ and resistance, $R_{IN} = \frac{1}{g_{m2}}$

Using small-signal analysis, the input impedance Z_{IN} into the emitter of Q_2 is given by Equation (7.49), hence we have

$$R_{IN} = \frac{1}{Gm} = \frac{n}{I_c}\frac{KT}{q} \quad (7.50)$$

And

$$L_{IN} = \frac{C_{be}(I_c).R_t}{G_m} = \frac{C_{be}(I_c).R_t}{I_c.q}.nkT \quad (7.51)$$

Where I_c is the current through Q1 and Q2, and C_{be} is the base-emitter capacitance of Q1 and Q2 and n is the number of charge carriers in the semiconductor. It can be seen that as the current I_c through Q_2 increases, the inductance and resistance seen from port 1 decreases. Thus a tunable inductor was achieved by using a voltage source Vtune, to control the inductance L_{IN}.

The active tunable inductor is designed using the transistor BFP620 and simulated using Agilent ADS 2010. The BFP620 is a packaged SiGe HBT transistor from Infineon having a high f_T of 65GHz. For simulation purposes, the Gummel-Poon spice model (SPICE GP model) of the transistor [37] is used. The simulated values of resistances and inductances for different values of Vtune are plotted in Figure 7-20 and Figure 7-21, respectively.

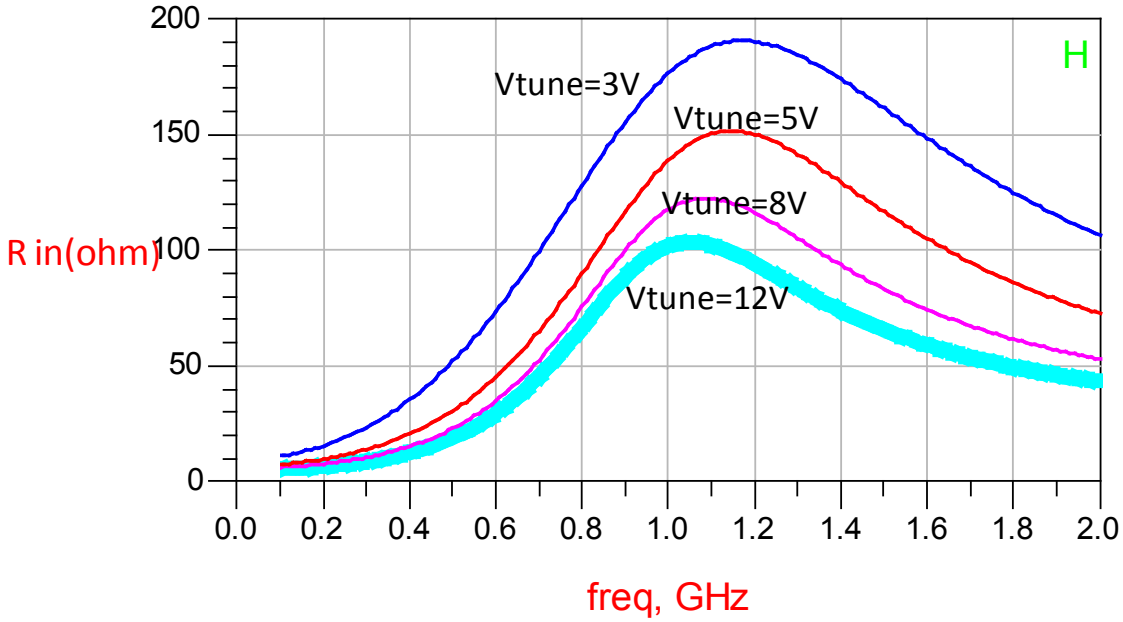

Figure 7-20 Simulated plot of resistance (R_{IN}) of the Active inductor for different values of Vtune

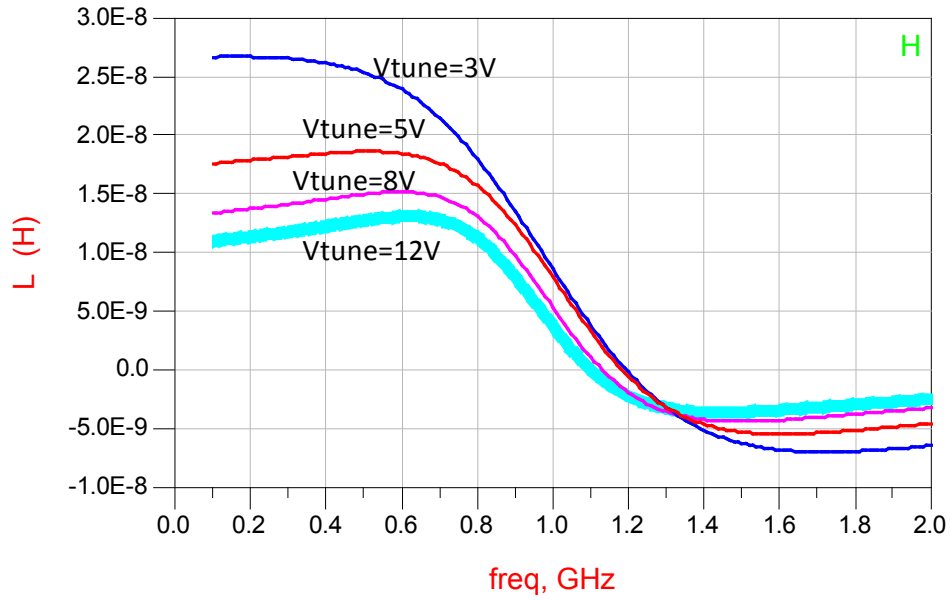

Figure 7-21 Simulated plot of inductance (L_{IN}) of the Active inductor for different values of Vtune

It can be seen from these plots that as Vtune increases, the current through the transistors (I_c) increases and the corresponding inductance L_{IN} and resistance R_{IN} of the active inductor decreases. It was observed that the resistance R_{IN} is a high positive value. Hence the inductor achieved is a lossy inductor with a bad Q. The advantage is that these inductors could be realized in a very small area in an integrated circuit compared to the space required for a passive inductor. For a tuning voltage, Vtune = 8V, CAD simulation (Ansoft) of the active inductor circuit had been performed and the equivalent admittance X_{IN} ($X_{IN} = \omega L_{IN}$) and resistance R_{IN} of the active inductor is plotted in Figure 7-22.

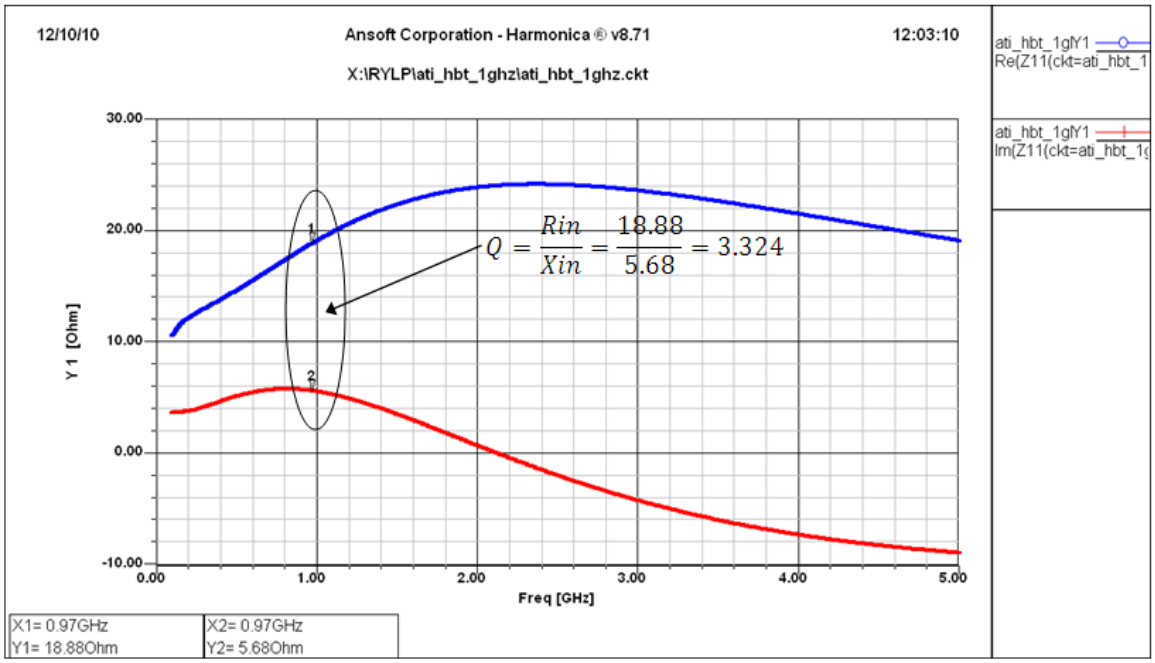

Figure 7-22 Simulated plot from Ansoft Serenade for R_{IN} and X_{IN} of the active inductor when Vtune=8V

The schematic of a Colpitts oscillator is shown in Figure 7-23. The frequency of oscillation is set by the LC resonator and is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{7.52}$$

The positive feedback required for oscillations is provided by the emitter inductor L_e, resistor R_e, along with the capacitive divider C_1 and C_2.

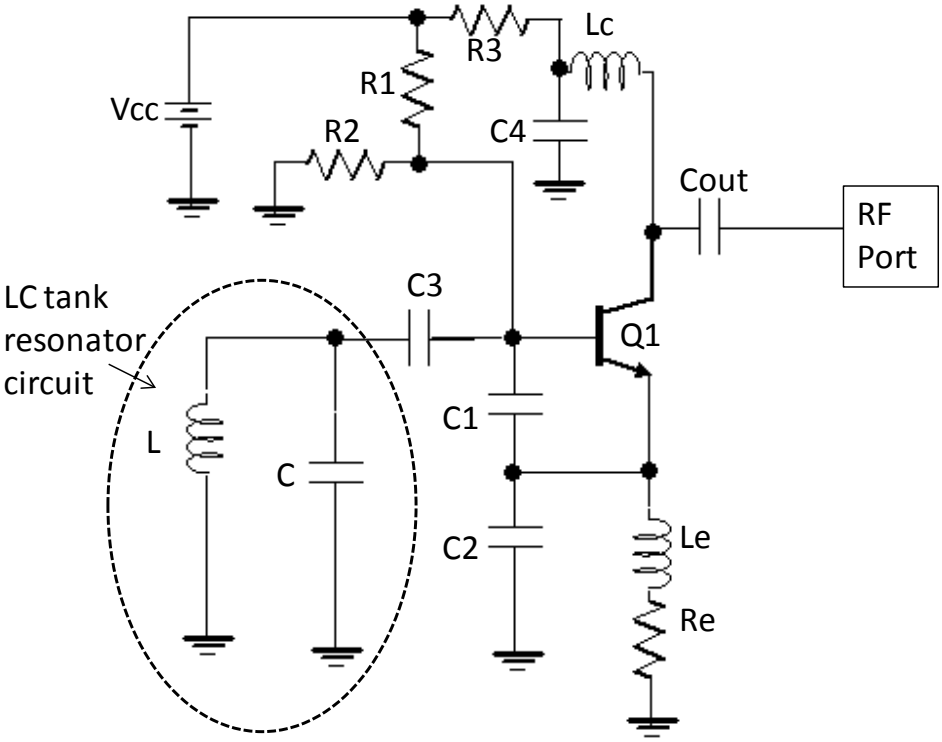

Figure 7-23 Schematic of a Colpitts Oscillator using a LC tank circuit

A Colpitts oscillator was designed and simulated using the ANSOFT CAD simulation tool. The Si-BJT transistor NE68819 from NEC is chosen for the design. The circuit is initially designed using a passive inductor. For simulation, the Q of the passive inductor is set as 3.3 at 800MHz. This is the same as the designed active inductor with Vtune =8V. For the resonator inductance value of L=12nH, the circuit was found to oscillate at 700MHz.

The transistor Q1 is biased under the conditions of Ic = 19.5mA, V_{be} = 0.8V and Vce = 3.4V using the bias resistors R_1, R_2, R_e and R_3. A harmonic balance analysis is performed and the phase noise of the oscillator circuit is simulated and plotted. From harmonic balance analysis, the output power of the fundamental frequency of oscillation was found to be 8dBm at 700MHz. The phase noise of the oscillator was simulated to be -72dBc/Hz at 10 kHz offset from the carrier.

For this example, the operational Q at 970 MHz is 3.324 and the simulated noise figure is 39.1dB. The simulated plots of noise figure and F_{min} are shown in Figure 7-24, output power is shown in Figure 7-25 and the phase noise plot is shown in Figure 7-26.

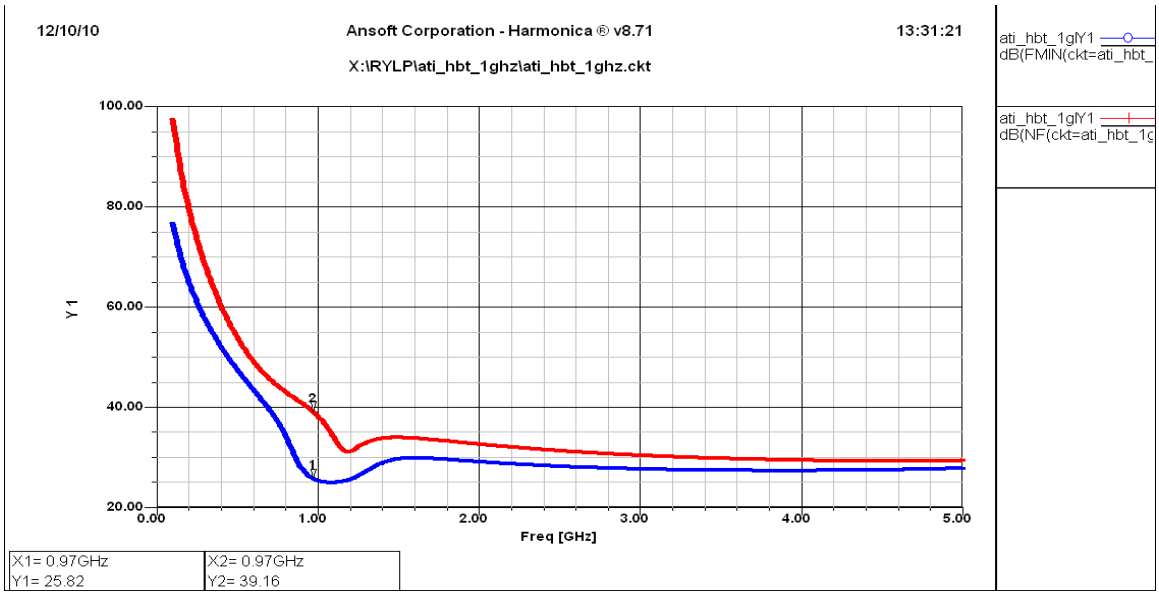

Figure 7-24 Simulated noise figure and F_{min} of oscillator with passive inductor.

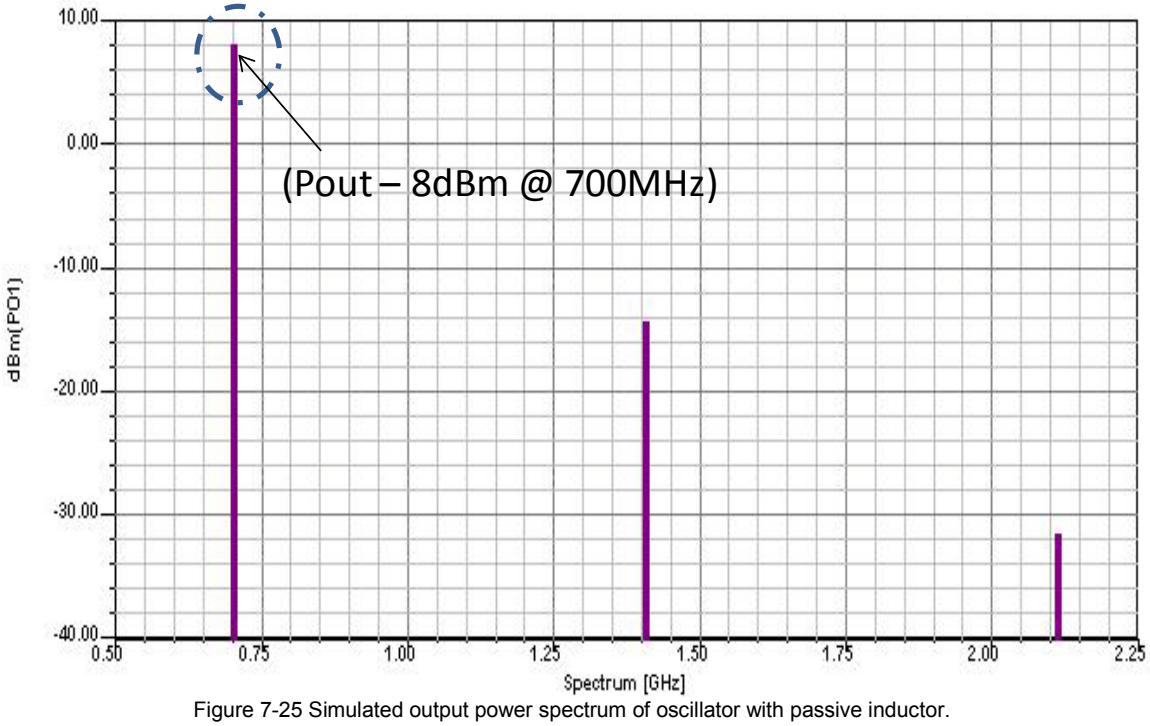

Figure 7-25 Simulated output power spectrum of oscillator with passive inductor.

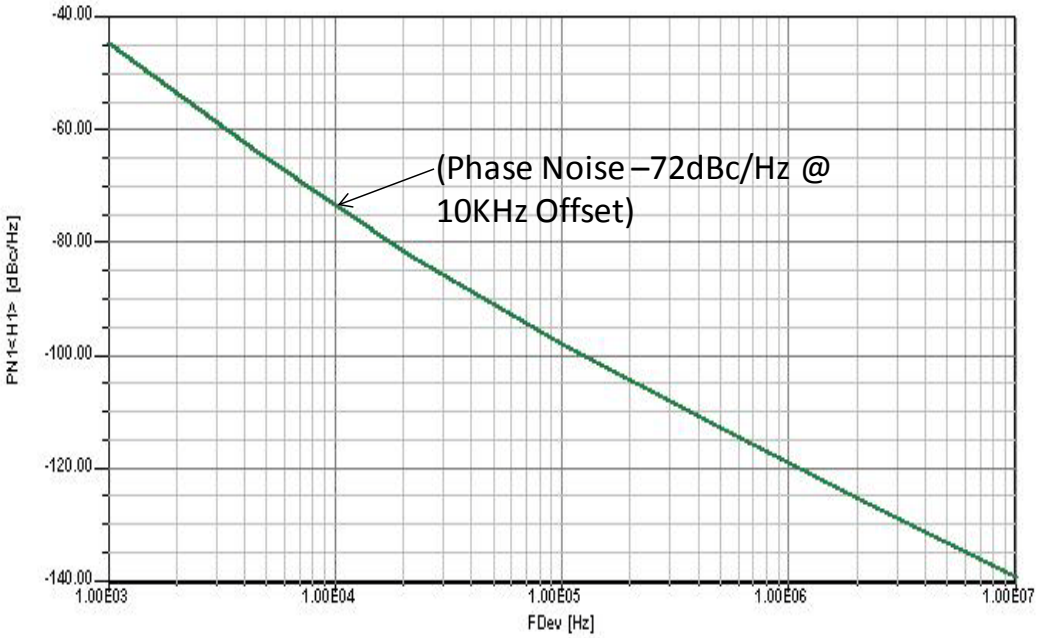

Figure 7-26 Simulated phase noise of the oscillator with passive inductor

The passive inductor in the LC tank circuit is replaced by the designed active inductor (under Vtune = 8V). The obtained circuit is drawn in the Figure 7-27. The Q and the inductance value of the active inductor are the same as that of the passive inductor at 700MHz. It was found that the active inductor-based oscillator also oscillates at 700MHz. The fundamental output power and the phase noise of the oscillator are measured using harmonic balance.

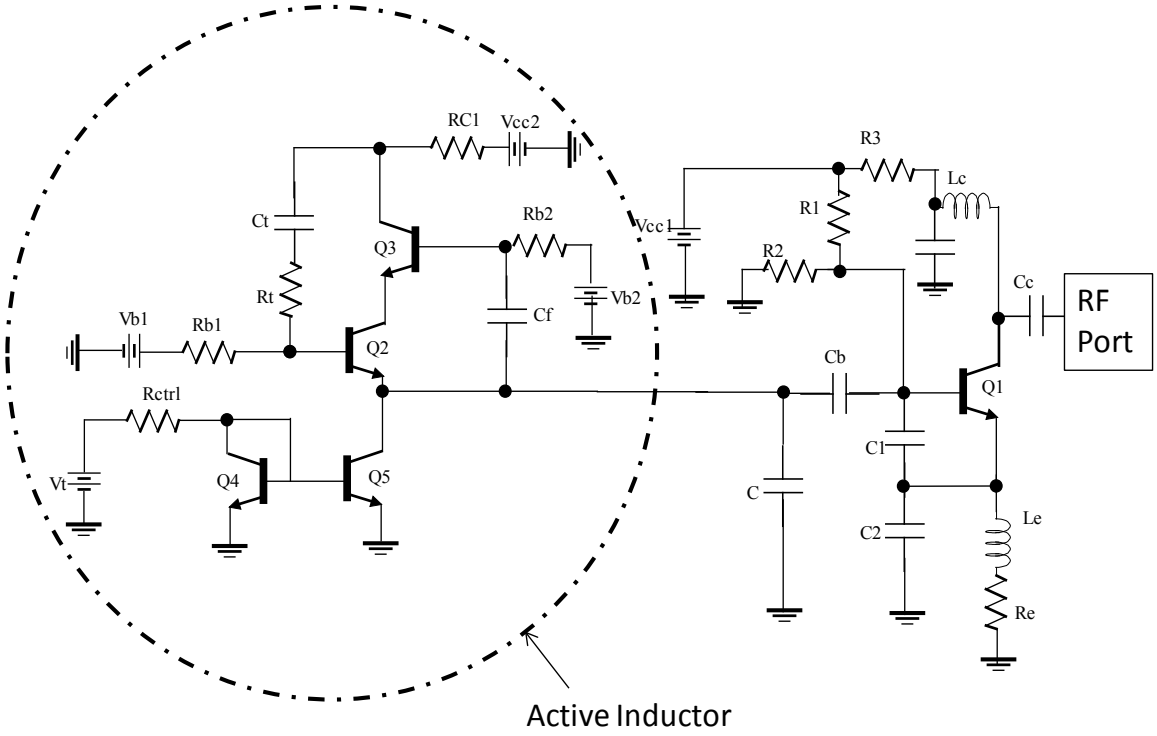

Figure 7-27 Colpitts oscillator with an active inductor (passive inductor of Figure 7-23 replaced by active inductor)

From simulation, the fundamental output power was 9dBm at 700 MHz, shown in Figure 7-28. This is in close agreement with the simulated output power of the passive inductor oscillator. The phase noise of the active inductor based oscillator was simulated to be -38dBc/Hz at 10 kHz offset from the carrier. The phase noise is plotted in Figure 7-29. The phase noise of the active inductor oscillator is about 34dBc worse compared to passive inductor oscillator. The inductors Lc and Le can be replaced by resistors in the final design to obtain an oscillator circuit without any passive inductors.

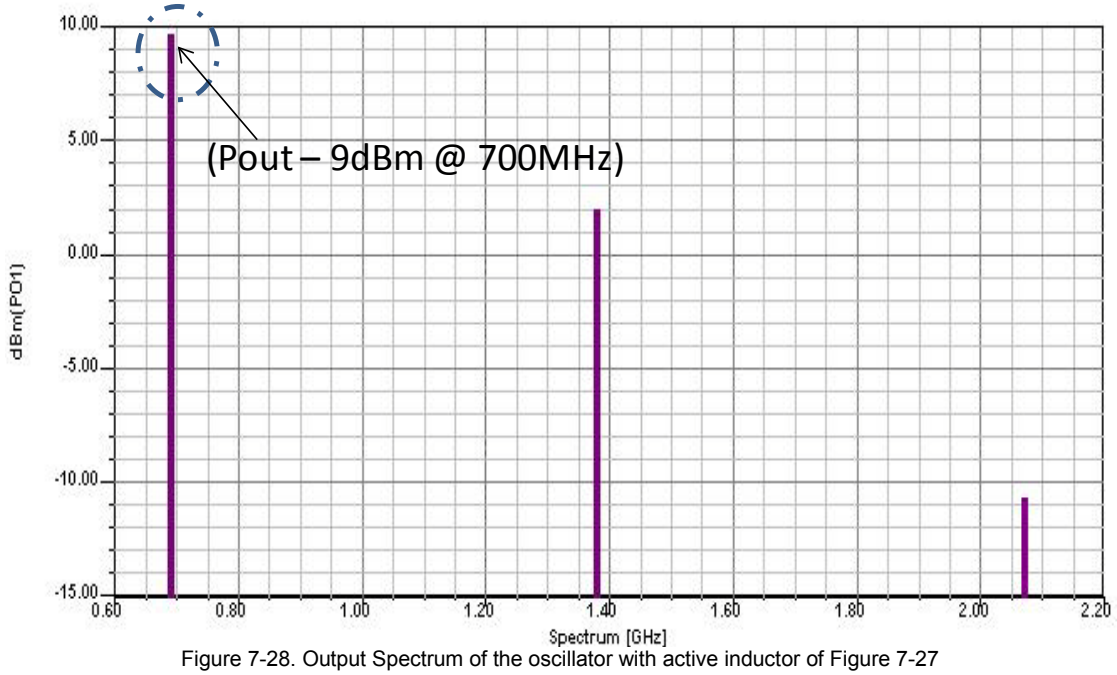

Figure 7-28. Output Spectrum of the oscillator with active inductor of Figure 7-27

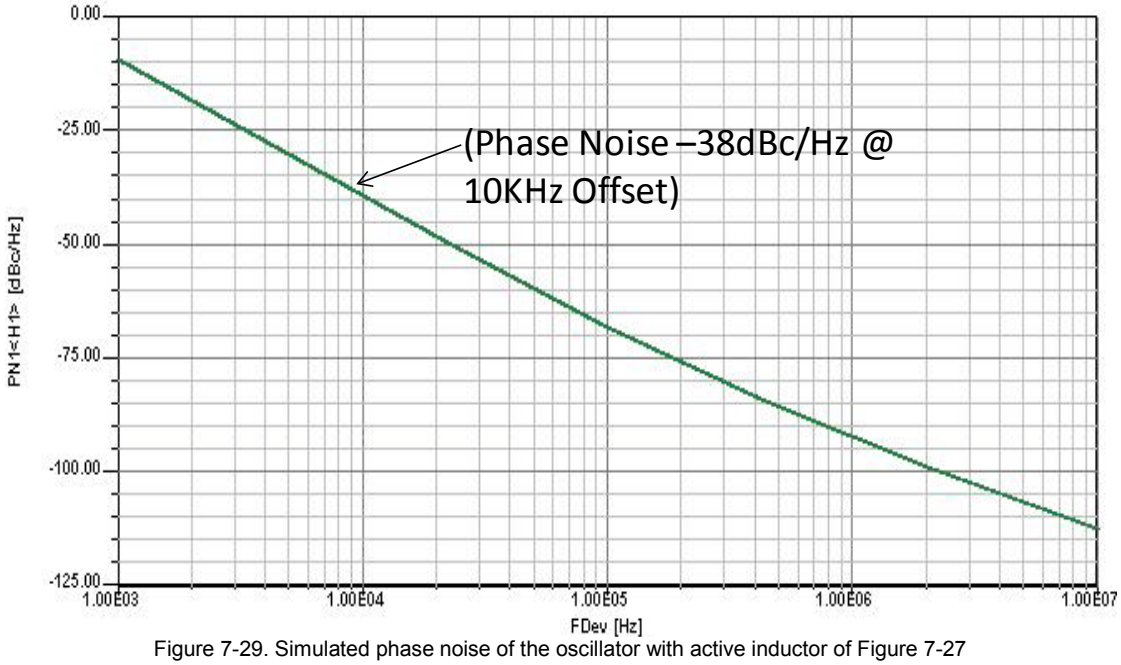

Figure 7-29. Simulated phase noise of the oscillator with active inductor of Figure 7-27

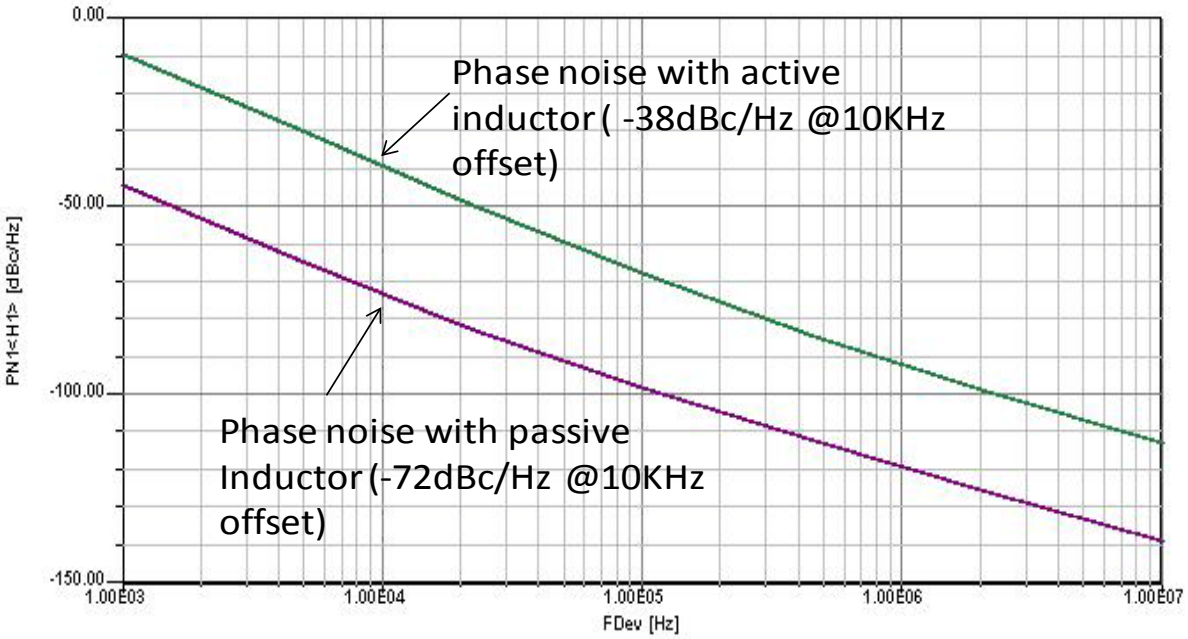

Figure 7-30 Comparison of the phase noise of oscillator with active inductor and passive inductor

Two identical Colpitts oscillator circuits have been designed, one with a passive inductor and another with an active inductor. Both the oscillators were found to oscillate at 700MHz and the output power of the oscillations was found to be in close agreement with each other. The passive and active inductors were made to be of same inductance value and same Q value at the output oscillating frequency. The phase noise of the active inductor oscillator was found to be about 34 dB worse compared to that of the passive inductor at 10 kHz offset from the carrier frequency. The simulated phase noise plots of these two oscillators are shown in Figure 7-30, and the 34dB difference between them can be seen.

Leeson had derived an empirical phase noise expression for a Colpitts oscillator given by [5]

$$L(f_m) = 10\log\left[\left[\left(\frac{f_o}{2*Q_L*f_m}\right)^2 + 1\right] * \left(\frac{FKT}{P}\right) * \left(\frac{f_c}{f_m} + 1\right)\right] \tag{7.53}$$

Where,
$L(f_m)$ is the phase noise at offset frequency f_m in dBc/Hz.
f_o is the center frequency (carrier frequency) in Hz.
Q_L is the loaded Q,
F is the noise factor,
T is absolute temperature,
P is carrier power in dBm, and
f_c is the corner frequency for flicker noise in Hz.

Leeson's formula is quite popular for predicting the phase noise of Colpitts oscillator and in most cases; it gives a fair approximation of the phase noise.

According to Leeson's formula, for two identical oscillator circuits having same output frequency and output power, the phase noise of the oscillator depends on the Q of the LC resonator. Therefore, if the resonators of the identical oscillators have the same Q, then the

oscillators should have same phase noise. However, with the same Q factor for passive and active inductor-based Colpitts oscillator circuit, the CAD simulated phase noise characteristics differed drastically as illustrated in Figure 7-30. Hence, it is inferred that the Leeson's phase noise formula does not hold for ATI based oscillators.

An active tunable inductor as shown in Figure 7-31 was designed and fabricated in 20 mil Rogers TMM3 PCB substrate. The designed layout is shown in Figure 7-32 and the fabricated unit under test is shown in Figure 7-33.

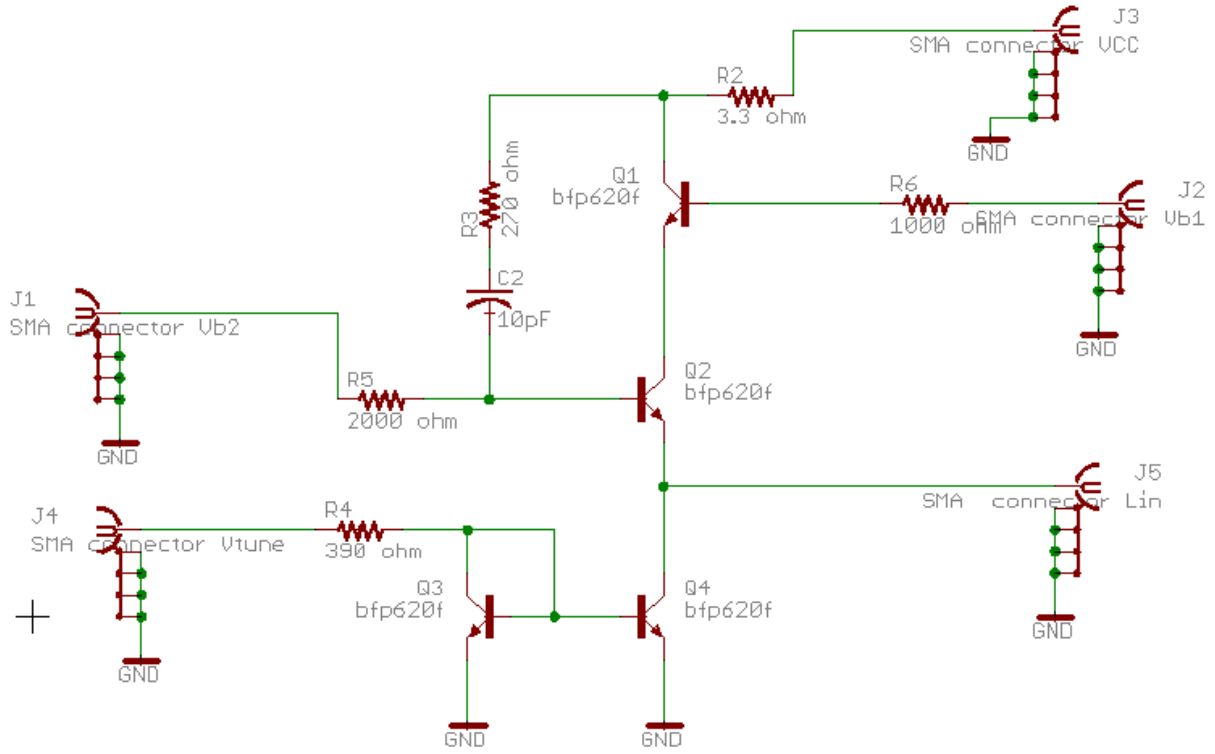

Figure 7-31 Schematic of the realized ATI

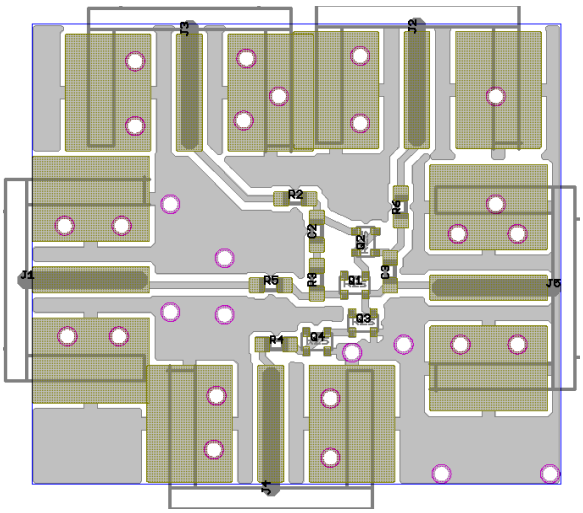

Figure 7-32 Layout of the Realized ATI

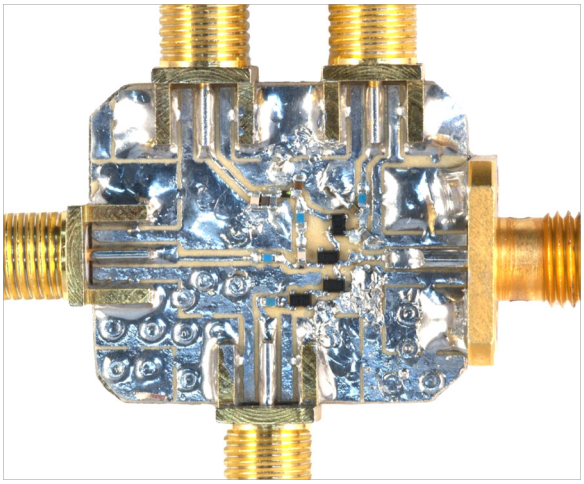

Figure 7-33 Photograph of the fabricated Active inductor

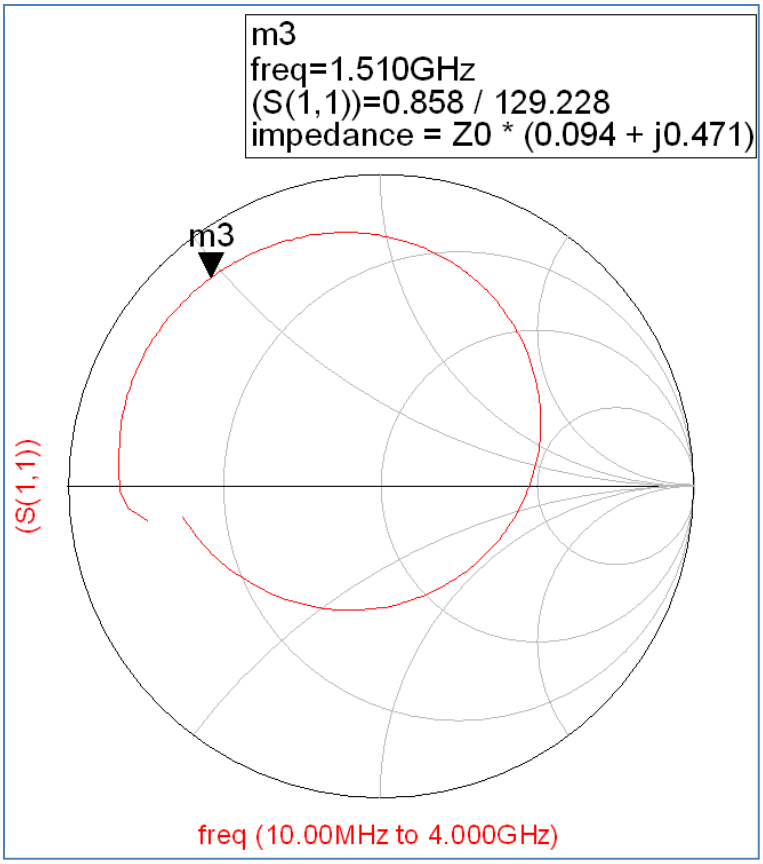

Figure 7-33 CAD Simulated S11 plot for Vtune = 5V

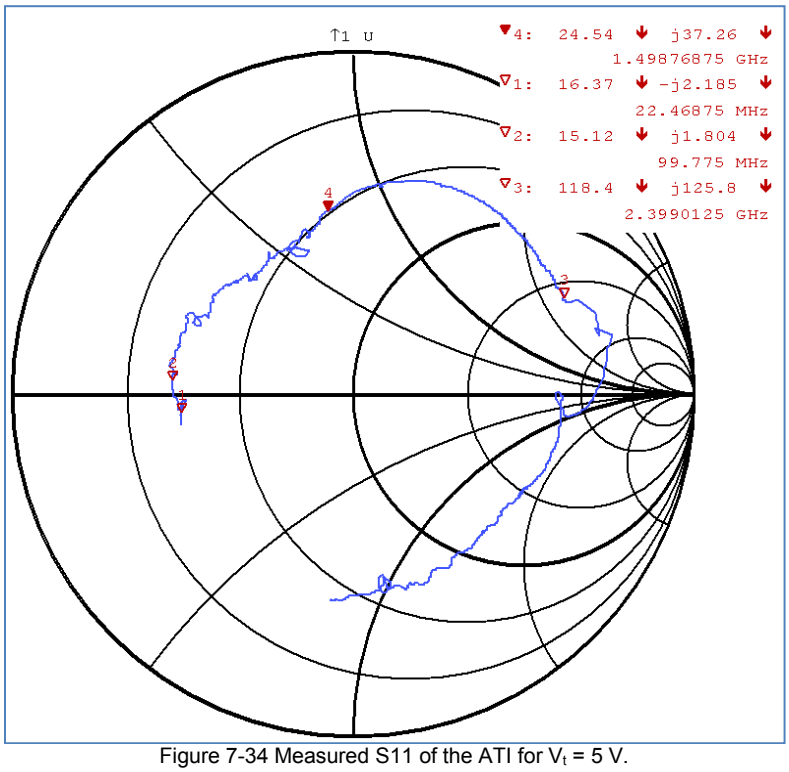

Figure 7-34 Measured S11 of the ATI for V_t = 5 V.

Figure 7-33 and Figure 7-34 show the CAD simulated and measured results, respectively, for tuning voltage V_{tune} = 5V. There is a small discrepancy between the measured and the simulated results, which needs to be analyzed. This could be due to the inaccuracy in modeling the layout parasitics or could be due to the discrepancy in the properties of the PCB used for fabricating the ATI.

Figure 7-35 shows the schematic and layout of the tunable active inductor implemented using Rogers-4003C substrate. Figure 7-36 and Figure 7-37 depict the CAD simulated and measured results. The discrepancies between simulated and measured results are due to the package parasitic associated with the devices.

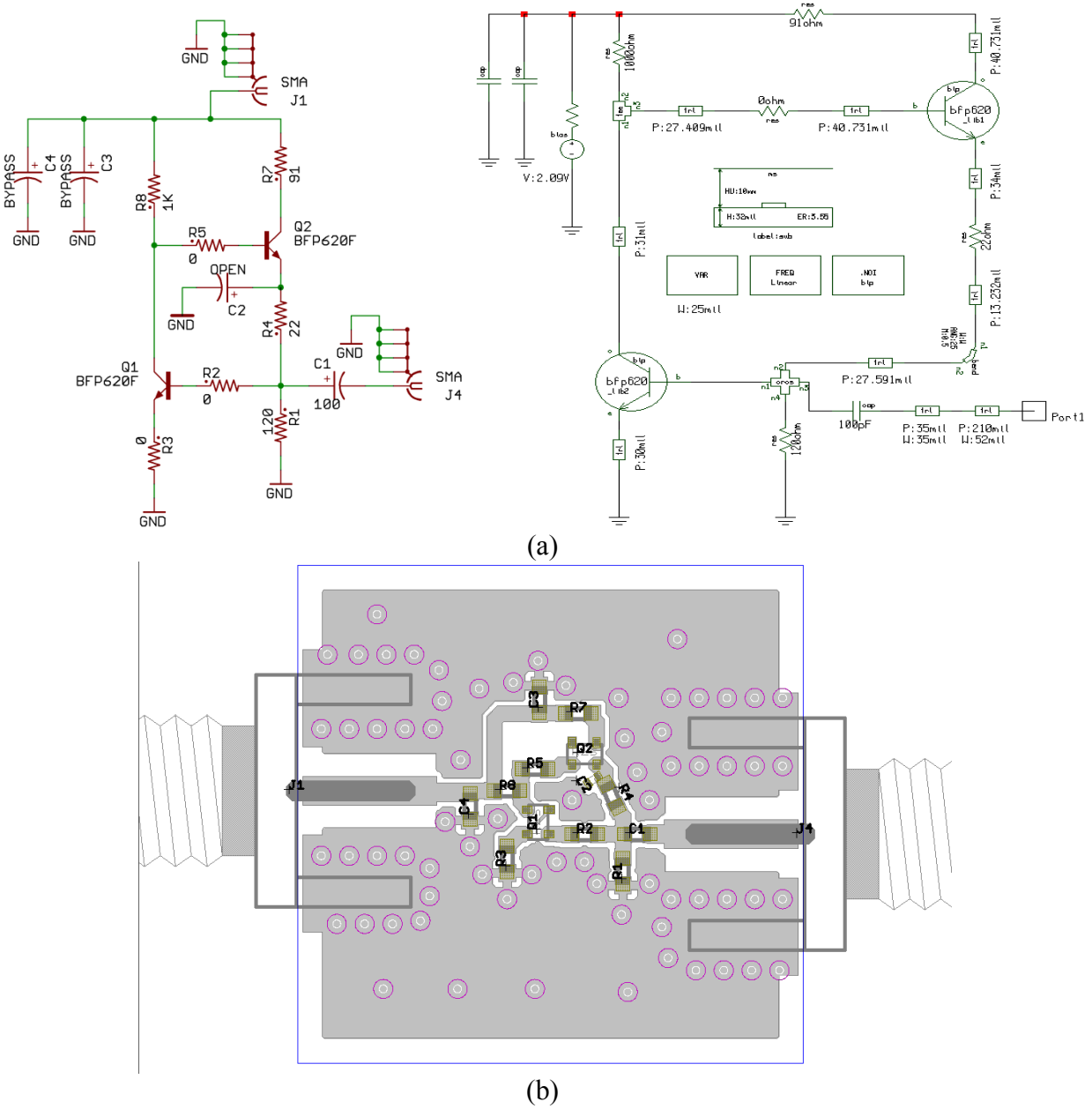

Figure 7-35 (a) Schematic of the built active inductor (left) and the schematic simulated (right) (b) Layout of the built active inductor

The measurement is done on the Rohde and Schwarz vector network analyzer and the inductance plot is shown in Figure 7-37.

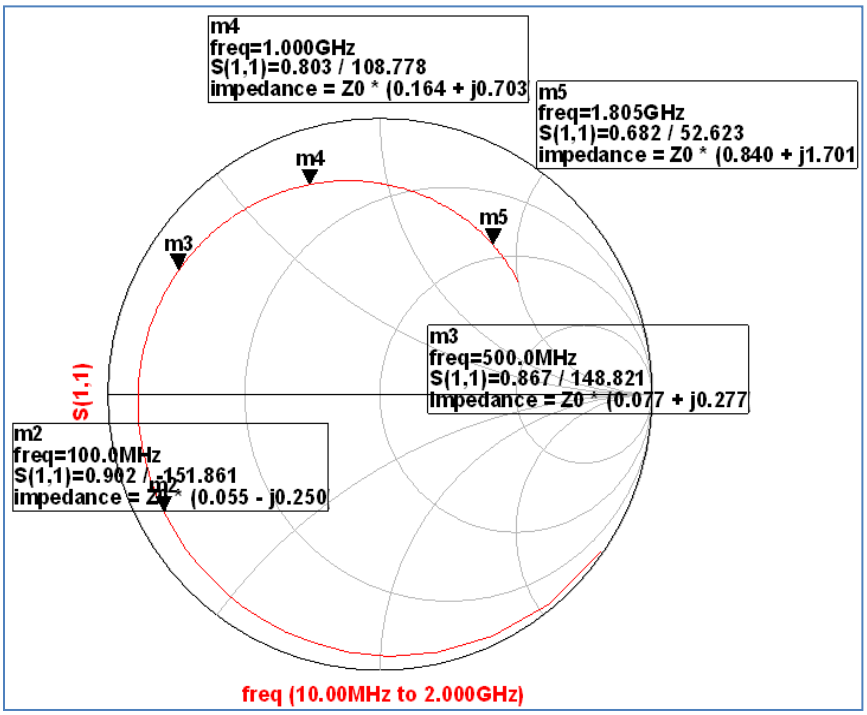

Figure 7-36 CAD simulated response of the active inductor of Figure. 7-35

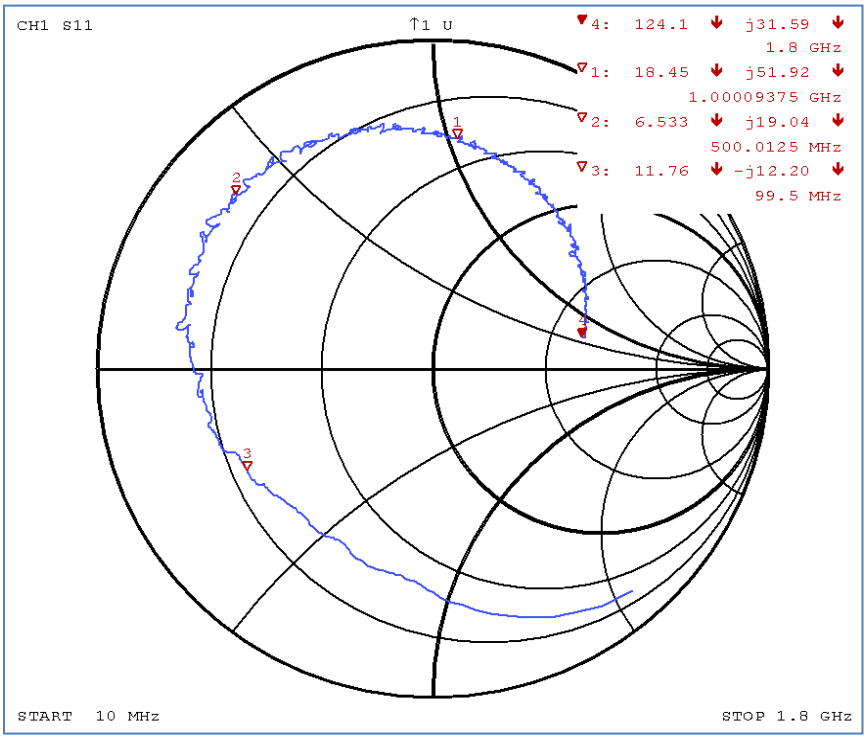

Figure 7-37 Measured response of the active inductor of Figure. 7-35

For validation of synthesized active inductor (L) network as shown in Figure 7-35, 900 MHz oscillator is designed and the phase noise performance is compared with the passive inductor (L_2) based oscillator using (7.53).

Figure 7-38 shows the analytical phase noise plots using MathCAD (described in Ch-6, section 6.1.2) for providing brief insights about the accuracy of the CAD tools (simulated phase noise plots shown in Figure 7-39), which agree within 2- 4 dB .

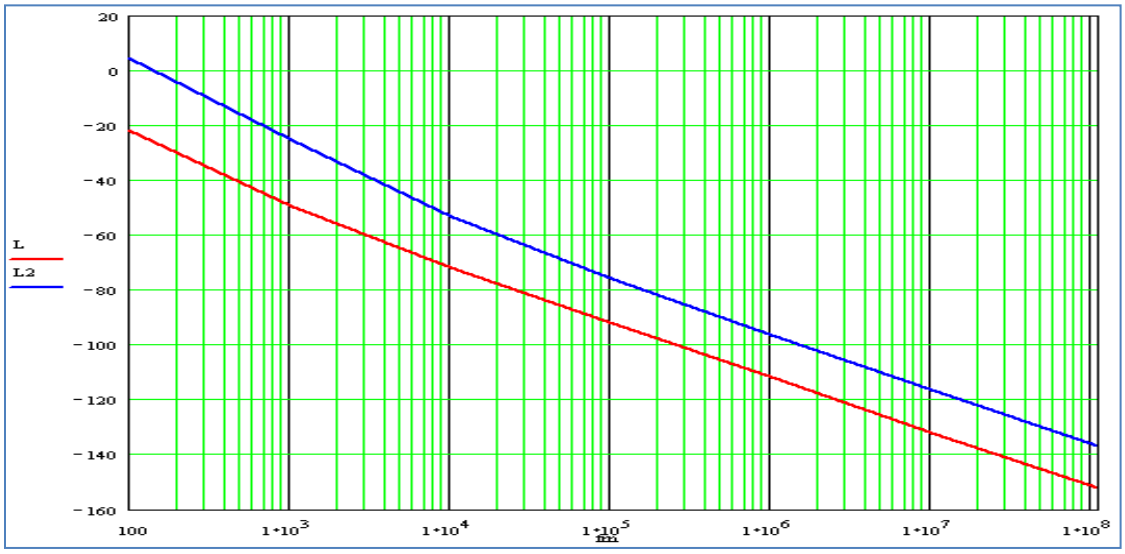

Figure 7-38 Comparison of the phase noise of oscillator with synthesized active inductor (L2) and passive inductor (L)

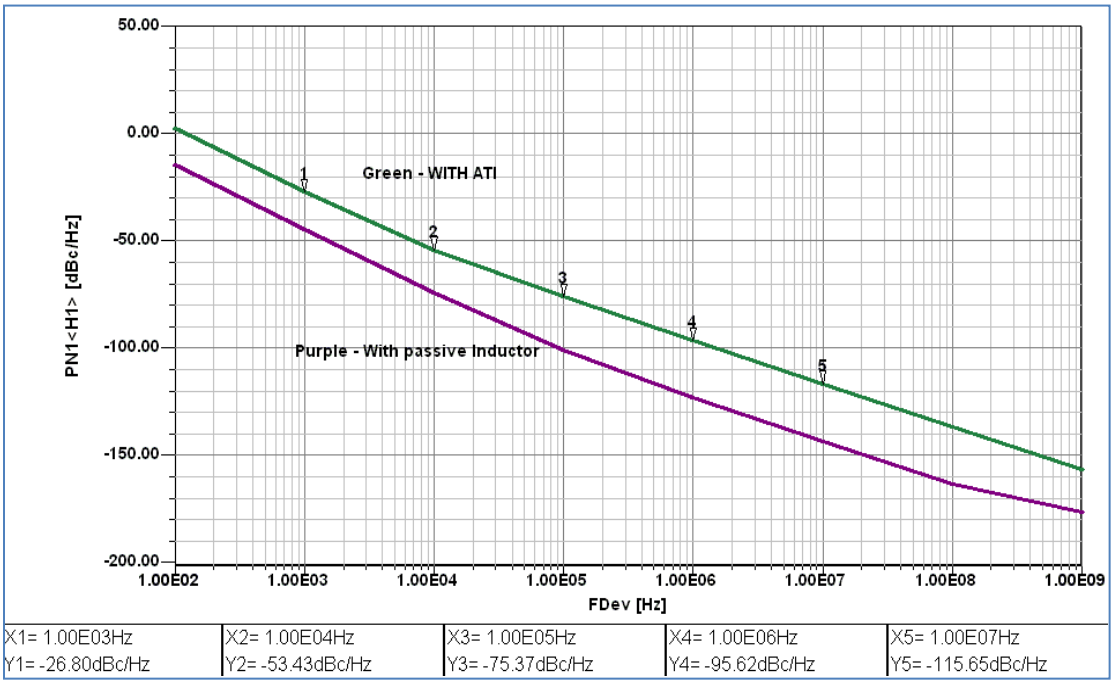

Figure 7-39 Comparison of the phase noise of oscillator with active inductor and passive inductor

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8. Device Scaling

Device scaling and architecture design advances have fueled the rapid growth in on-chip processing power for the past decades. This continuing growth in computing capacity demands that the off-chip bandwidth also scale in step. Unlike active devices, spiral inductors do not scale with technologies and in general, the real estate area consumed by spiral inductors will be prohibitively large. A much more compact alternative to realize on-chip inductors for tunable resonator application as well as improving the quality factor is to use active inductors. Both the area and speed of active inductors scale with technology and they are easy to implement in IC processes since they can be designed using only active devices. These favorable features make their usages compatible with the trend of very high level of integration, particularly in systems that are enabled by MMIC technology (e.g., System-on-Chip To evaluate the suitability of using active inductors in the tunable oscillator circuits, in this thesis we are motivated to design and implement prototype active inductor circuits using discrete higher f_t active device (SiGe HBTs) from Infineon that we have access to.

An oscillator designed with active inductor is presented. From the theoretical analysis and simulations, it is obvious that an active inductor tunable oscillator has the advantages of wider tuning range and smaller chip area. The main disadvantage of noise performance is mainly due to more component noise and smaller voltage swing.

The design techniques of TAIOs to obtain a larger voltage swing and better phase noise performance are discussed. With the trend of device scaling**,** the maximum obtainable oscillation frequency and phase noise performance can be improved.

The developed theory explains operation and gives the calculation of amplitude and frequency in the VCO with active inductors. The simulation results are in a reasonable agreement with theoretical calculations. The deflection of simulated results from theory is explained by the insufficiency of the noise model associated with synthesized inductors. Further characterization of oscillator noise dynamics should be linked with synthesized inductor on realization of a convenient and practical circuit for tunable oscillators.

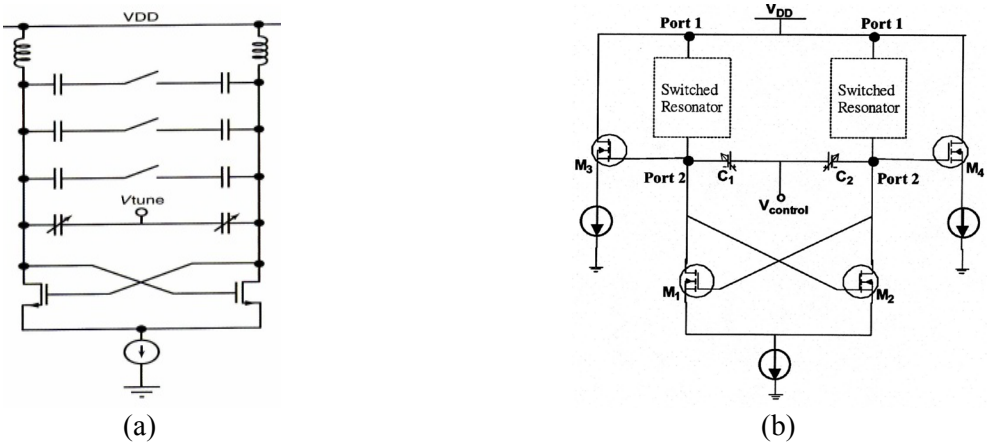
8.1 Introduction

For higher frequencies, the manufacturing of low cost, low phase noise oscillators is more challenging owing to the frequency limitations of the active devices. The operating frequency of the oscillator is limited by the cutoff frequency (f_T) of the active device (transistor). Most research effort is directed towards scaling down the device geometric profile to obtain a higher cutoff frequency (f_T).

The oscillator tuning range is a critical parameter for the multi-band and multi-mode wireless communication systems, including compensation of the frequency drift due to package parasitics and temperature. A general problem in the oscillator design is a trade-off between tuning range, phase noise and power consumption. A simplified approach for a tunable oscillator is a switched capacitor bank for coarse tuning and tuning diodes (varactors) for fine, as shown in Figure 8-1. However, the varactor tuned oscillator is limited in tuning range due to the influence of package

parasitics at higher operating frequencies, including a large die area and is therefore not a cost-effective RFICs/MMICs solution [1]-[7].

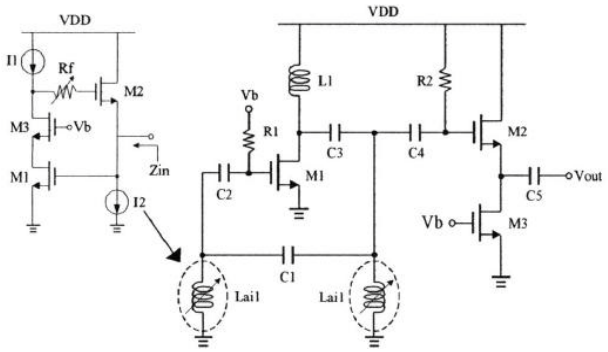
To overcome the above problems, we proposed a tunable active inductor oscillators (TAIOs) using scaled SiGe HBT device for applications in radio and microwave signal sources. Unfortunately, active inductor oscillators show poor phase noise performances and sensitivity to PVT (process, voltage supply, temperature) variation compared to varactor-tuned oscillators. Nevertheless, the advantages of the integration in small chip area make this technology promising and cost-effective integrable alternative for applications such as oscillators, phase shifters, couplers, and power dividers (Figure 8-2) [7].



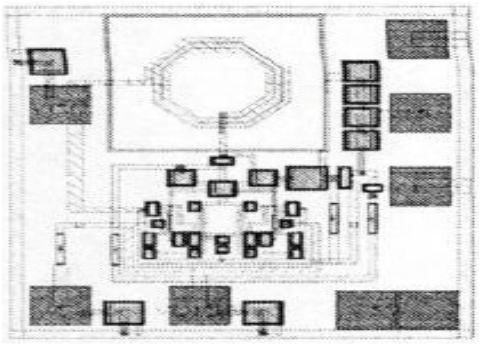
(a) (b)

Figure 8-1 Multi-band oscillator: (a) LC-oscillator with switched capacitor network for coarse tuning and (b) dual-band oscillator using switched resonator technology

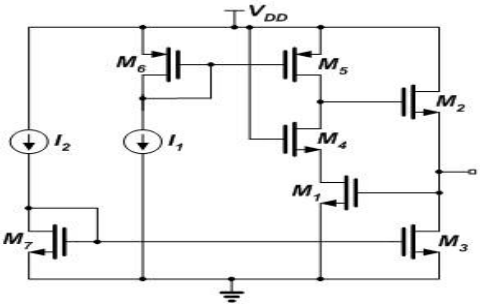
RF signal source applications, place stringent conditions on the noise dynamics of active inductor-tuned oscillator technologies because of the inherent high noise figure and low dynamic range due to the uncontrolled nonlinearity at large-signal conditions. These problems become critical at high frequency when the active device (Bipolar/FETs) is technologically scaled to obtain a higher cutoff frequency. In this research work, the impact of scaling on noise parameters in SiGe HBTs based active inductor oscillator circuits is described and its partial or eventual cancellation with an appropriate phase-injection is shown.



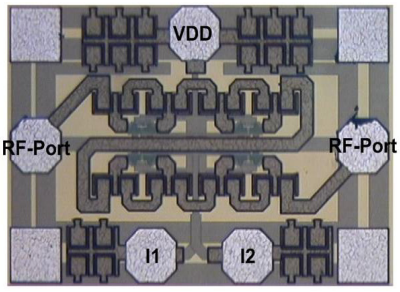
(i) Active inductor oscillator (3 -5 GHz)



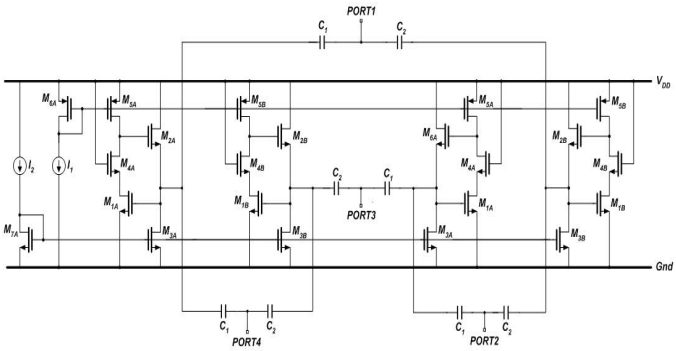
Chip layout (600×675 μm2)



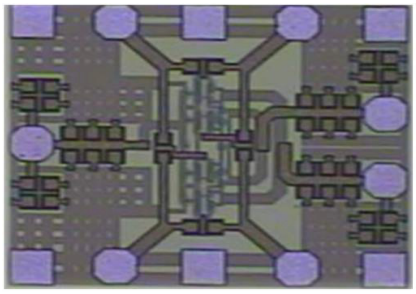
(ii) Active inductor phase shifter (3.5-4.5 GHz)



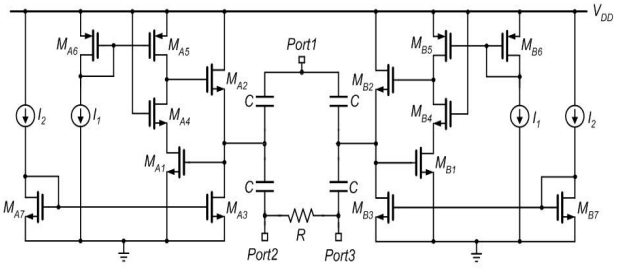
Chip layout (1.08 mm2)



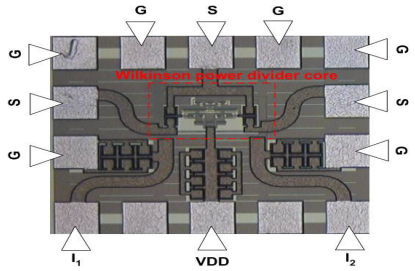
(ii) Active inductor quad coupler (3.2-5.2 GHz)



Chip layout (700×550 μm2)



(iii) Active inductor power divider (4.5 GHz)



Chip layout (640×720 μm2)

Figure 8-2. Typical lumped microwave integrated circuits implemented using active inductor technology in the standard TSMC 0.18-um CMOS process: (i) active inductor oscillator, (ii) analog phase shifter using active inductor, (iii) quadrature coupler using active inductor, and (iv) Wilkinson power divider using active inductor [7].

8.2 Device Scaling and Noise Dynamics

The performance of communication system depends on the speed of the device, and typically specified by two figures-of-merit (FOM). The first FOM is the transistor cutoff frequency f_T, and second FOM is the maximum oscillation frequency f_{max}, which are defined as the frequency point where the current gain and the power gain become unity, respectively. Device scaling improves these RF figures of merit. The f_T *and* f_{max} for SiGe HBT is given by [4]

$$f_T \cong \frac{1}{2}\left[\frac{1}{g_m}(C_{be}+C_{bc})+\tau_b+\tau_e+\tau_{bc}\right]^{-1} \tag{8.1}$$

$$f_{max} \cong \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \tag{8.2}$$

where C_{be} is the parasitic base-emitter junction capacitance, C_{bc} is the parasitic base-collector junction capacitance, R_b is the parasitic base resistance, g_m is the device transconductance, τ_b is the base transit time, τ_e is the emitter delay time, and τ_{bc} is the base-collector junction depletion layer time. These parameters are sensitive to technological scaling and greatly influences noise dynamics of the active inductor oscillators.

Noise is a major drawback of synthesized active inductors realized using active devices. Noise in the active inductor is characterized as broadband noise (base and collector current shot noise, and base resistance thermal noise), and low frequency noise (1/*f* noise), which are sensitive to the device scaling of the active device (Bipolar/FET). Figure 8-3 shows the simplified inductor-tuned oscillator with equivalent noise sources associated with inductor and transistors.

8.2.1 Broadband Noise (Thermal and Shot Noise)

The broadband noise in a bipolar transistor as shown in the Figure 8-3 is due to the base current shot noise $2qI_B$, the collector current shot noise $2qI_C$, base resistance thermal noise $4kTR_b$, and the emitter resistance thermal noise $4kTR_e$. The mean square values of the broadband noise generator (scaling sensitive parameters) for a frequency interval Δf can be described by [6]

$$\overline{i_{bn}^2} = 2qI_B\Delta f \Rightarrow S(i_{bn}) = \frac{\overline{i_{bn}^2}}{\Delta f} = 2qI_b = \frac{2kTg_m}{\beta} \tag{8.3}$$

$$\overline{i_{cn}^2} = 2qI_C\Delta f \Rightarrow S(i_{cn}) = \frac{\overline{i_{cn}^2}}{\Delta f} = 2qI_c = 2kTg_m \tag{8.4}$$

$$\overline{v_{bn}^2} = 4kTR_b\Delta f \Rightarrow S(v_{bn}) = \frac{\overline{v_{bn}^2}}{\Delta f} = 4kTR_b \tag{8.5}$$

$$\overline{v_{en}^2} = 4kTR_e\Delta f \Rightarrow S(v_{en}) = \frac{\overline{v_{en}^2}}{\Delta f} = 4kTR_e \tag{8.6}$$

RF noise performance is typically described through four noise parameters: the minimum noise figure $F_{\min}$, the noise resistance R_n and the real and imaginary components of the optimum noise impedance Z_{opt} ($Z_{opt} = G_{opt} + j\,B_{opt}$). The minimum noise factor $F_{\min}$ can be described by

$$F_{min} \cong 1 + \frac{n}{\beta} + \sqrt{\frac{2I_C}{v_T}(R_b + R_e)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta}\right) + \frac{n^2}{\beta}} \tag{8.7}$$

$$F_{min} \cong 1 + \sqrt{\frac{2I_C}{v_T}(R_b + R_e)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta}\right)} \tag{8.8}$$

where $v_T = \frac{kT}{q}$, $\beta \approx \frac{I_C}{I_B} > 100$, $R_b > R_e$, and $n \cong 1$.

From Equation (8.6), $F_{min} \cong 1 + \sqrt{\frac{2I_C}{v_T\beta}R_b}$; $\quad for \quad f << \frac{f_T}{\sqrt{\beta}}$ (8.9)

$$[F_{min}]_{opt} \cong \frac{1}{[\beta]^{1/4}} \sqrt{4\pi f R_b C_{be}}; \quad for \quad f << \frac{f_T}{\sqrt{\beta}} \tag{8.10}$$

$$F_{min} \cong 1 + f \sqrt{\frac{2}{v_T} R_b \left(\frac{I_C}{f_T^2} \right)}; \quad for \quad f >> \frac{f_T}{\sqrt{\beta}} \tag{8.11}$$

$$[F_{min}]_{opt} \cong \sqrt{32\pi^2 f^2 R_b C_{be} \tau_f}; \quad for \quad f >> \frac{f_T}{\sqrt{\beta}} \tag{8.12}$$

$$\tau_f \cong \tau_b + \tau_e + \tau_{bc} \tag{8.13}$$

The noise resistance R_n and the corresponding optimum noise resistance R_{opt} is given by

$$R_n \cong \left[\frac{kT}{2qI_C} + R_b \right] \tag{8.14}$$

$$[R]_{opt} \cong \left(R_b + \frac{kT}{2qI_C} \right) \left(\frac{2}{F_{min} - 1} \right) = R_n \left(\frac{2}{F_{min} - 1} \right) \tag{8.15}$$

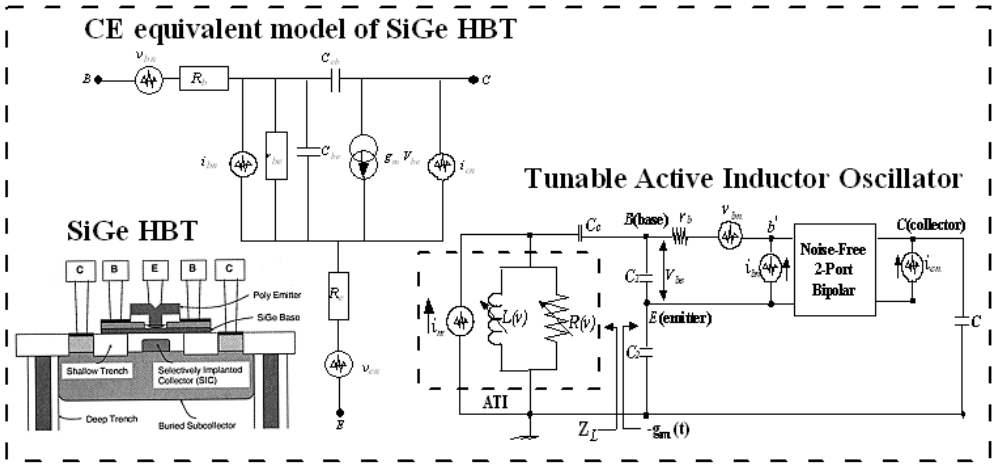


Figure 8-3 A typical CE simplified model of the SiGe HBT and TAIO

As shown in Figure 8-3, the parasitic base-emitter junction capacitance C_{be} and the parasitic base resistance R_b vary linearly with the emitter width w_e. This allows f_{min} to scale down linearly with w_e for low and high frequency regions.

From Equation (8.9), f_{min} for low frequency can be minimized by increasing the value of current gain β and reducing the values of R_b at a given device bias (I_C=I_{C1}). Although increasing the value of β will minimize f_{min}, this comes at the cost of reducing the breakdown voltage (BV_{CEO}).

From Equation (8.11) for high frequencies, f_{min} can be minimized by decreasing the value of R_B, and increasing f_T at given device bias (I_C =I_{C2}). The thermal noise generated due to the base resistance R_b in SiGe HBT can be minimized by increasing the doping profile of the base and reducing the emitter width. From Equation (8.10) and Equation (8.12), for the low frequency regime, maximizing β is important, while for high frequency regime, minimizing τ_f becomes

important. The parasitic base-emitter junction capacitance C_{be} and the parasitic base resistance R_b vary reciprocally with the emitter strip length L_e, whereas, C_{be} and R_b increasing proportionally with the emitter width w_e.

From Equation (8.14) and Equation (8.15), R_n *and* R_{opt} can be optimized based on the scaling for the related device parameters. For tunable active inductor oscillator applications (TAIOs), the transistor geometric profile needs to be properly scaled and optimized to the minimum noise figure for low phase noise VCO applications.

8.2.2 Low Frequency Noise (1/*f* Noise)

The low frequency noise ($1/f$) noise plays an important role to determine the close in carrier phase noise, which is unconverted to the carrier frequency, resulting in a $1/f^3$ region.

The major contribution of low frequency noise is flicker noise ($1/f$ noise), which is dependent on the base current of the SiGe HBTs and can be described by [4]

$$S_{I_b,1/f} = \left[\frac{\overline{i^2_{1/f}}}{\Delta f}\right] = \left[\frac{K}{A_e}\right]\left[\frac{I_B^a}{f^b}\right] \tag{8.16}$$

where Δf is a narrow frequency bandwidth at frequency f, I_B is the base current, K is a constant for a particular device and technology, A_e is the emitter area, a is flicker noise exponent ($\cong 2$ for SiGe HBTs), and b is flicker noise frequency shaping factor with the value of about unity.

8.2.3 Impact of Scaling on Oscillator Phase Noise $£(f_m)$

The modified Leeson phase noise eq. is given by Rohde [6]

$$£(f_m) = 10\log\left\{\left[1+\frac{{f_0}^2}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^2}{f_m^2}\right\} \tag{8.17}$$

Where,
m is the ratio of the loaded and unloaded Q
Q_0 is the unloaded Q
f_0 is the oscillation frequency
f_c is the flicker corner frequency
f_m is the offset frequency from the carrier
F is the noise factor
K_0 is the oscillator voltage gain
R is the noise resistance of the tuning diode
k is the Boltzmann's constant and T is the temperature in degrees Kelvin.

The noise factor F as given in Equation (8.9) and Equation (8.11) is a sensitive scaling parameter. It can be optimized with respect to the geometric profile of the SiGe HBTs to obtain the minimum noise figure for low noise oscillator applications.

From Equation (8.19), the minimum phase noise at far frequency offsets can be obtained by minimizing the noise factor F for a given TAIOs topology, operating frequency and tuning range. However, the close-in phase noise is related to the 1/f noise up-conversion and can be suppressed by optimizing symmetry of the active inductor oscillator RF signal waveforms. From [5],

$$\pounds(f_m) = \begin{cases} 10\log\left[\left(\frac{C_0{}^2}{q_{max}^2}\right)\left(\frac{i_n{}^2/\Delta f}{8f_m^2}\right)\left(\frac{\omega_{1/f}}{f_m}\right)\right]; & \frac{1}{f^3} \rightarrow region \\ 10\log\left[10\log\left[\left(\frac{\Gamma_{rms}{}^2}{q_{max}^2}\right)\left(\frac{i_n{}^2/\Delta f}{4f_m^2}\right)\right]\right]; & \frac{1}{f^2} \rightarrow region \end{cases} \tag{8.18}$$

$$\Gamma_{rms}^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = \sum_{n=0}^{\infty} C_n^2 \tag{8.19}$$

$$\Gamma(x) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n Cos(nx + \theta_n); \quad x = \omega_0 t \tag{8.20}$$

$$\omega_{1/f^3} = \omega_{1/f}\left[\frac{C_0^2}{\Gamma_{rms}^2}\right] \tag{8.21}$$

Where
$(i_n^2/\Delta f)$ is the noise power spectral density,
Δf is the noise bandwidth,
Γ_{rms}^2 is the root mean square value of $\Gamma(x)$ the impulse sensitivity function (ISF),
C_n is the Fourier series coefficient, $x = \omega_0 t$, C_0 is zeroth order of the ISF (Fourier series coefficient), θ_n is the phase of the nth harmonic,
f_m is the offset frequency from the carrier,
$\omega_{1/f}$ is the flicker corner frequency of the device,
q_{max} is the maximum charge stored across the energy storing capacitor in the resonator network.

From Equation (8.20) and Equation (8.21), the 1/f noise up-conversion can be reduced by minimizing the value of C_0, which is a function of the slope of the rise and fall time of the waveform across the active inductor resonator. The active inductor oscillator approach using scaled device discussed in this work shows the impact of device scaling (Area 1: 0.5) on the phase noise at close-in and far frequency offsets from the carrier.

8.2.4 Design Examples and Validation

The steady-state oscillation condition for a typical series feedback active inductor oscillator shown in Figure 8-4 is given by

$$Z_{osc}(I_L, \omega) + Z_L(\omega) = 0 \tag{8.22}$$

$$Z_{osc}(I_L, \omega) = R_{osc}(I_L, \omega) + jX_{osc}(I_L, \omega) \tag{8.23}$$

$$R_{osc} = \left(\frac{\frac{1}{R_2}}{\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{R_2}\right)^2} \right) - \left(\frac{-\mathrm{gm}\left((1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)\left(\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{R_2}\right)^2\right) - \frac{\omega^2 C_{b'e} C_{ce}}{R_2}\left(2(1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)}{\omega C_{ce}\left(\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{R_2}\right)^2\right)\left(\left((1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)^2 + \left(\frac{1-\omega^2 C_{b'e} L_1}{R_2}\right)^2\right)} \right) \quad (8.24)$$

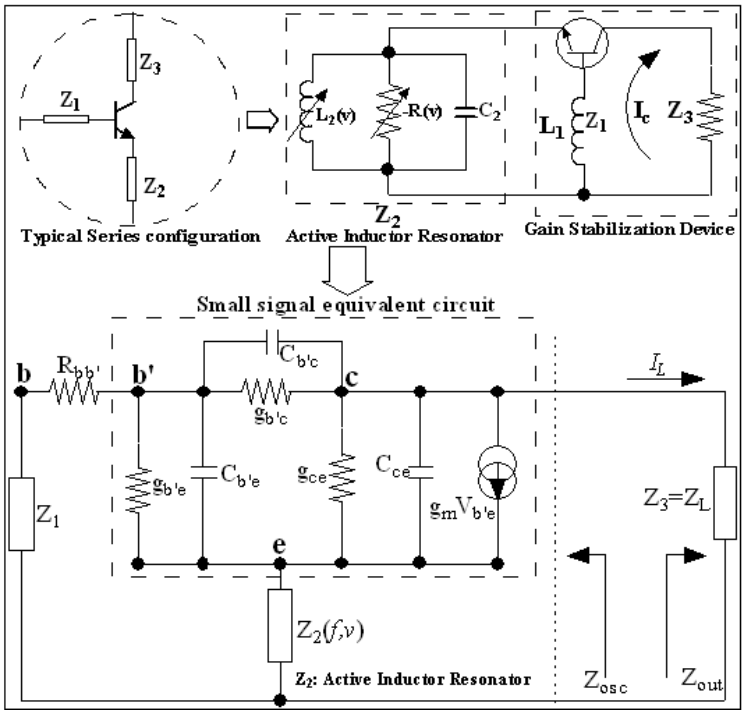


Figure 8-4 A typical series feedback active inductor oscillator topology

$$X_{osc} = \left(\frac{\left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{\omega L_2} - \omega C_2\right) - \frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)^2 + \left(\frac{1-\omega^2 C_{b'e} L_1}{R_2}\right)^2\right]}{\left[\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)^2 + \left(\frac{1-\omega^2 C_{b'e} L_1}{R_2}\right)^2\right]} \right) + \left(\frac{\omega C_{b'e}\left(\frac{1}{\omega L_2} - \omega C_2\right)\left[(1-\omega^2 C_{b'e} L_1)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right] + \frac{(1-\omega^2 C_{b'e} L_1)}{\omega R_2 C_{ce}} g_m\left[\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 - \left(\frac{1}{R_2}\right)^2\right] - \frac{(1-\omega^2 C_{b'e} L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}}{\left[\left(\frac{1}{\omega L_2} - \omega C_2\right)^2 + \left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e} L)\left(\frac{1}{\omega L_2} - \omega C_2\right) - \omega C_{b'e}\right)^2 + \left(\frac{(1-\omega^2 C_{b'e} L_1)}{R_2}\right)^2\right]} \right) \quad (8.25)$$

For sustained oscillation $X_{osc} = 0$, (25) reduces to

$$\left.\begin{aligned} X_{osc} = &\left[\frac{-1}{\omega C_{ce}}\left(\frac{1}{\omega L_2}-\omega C_2\right)^2+\left(\frac{1}{\omega L_2}-\omega C_2\right)-\frac{1}{\omega C_{ce}}\left(\frac{1}{R_2}\right)^2\right]\left[\left((1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right)^2+\left(\frac{1-\omega^2 C_{b'e}L_1}{R_2}\right)^2\right]+ \\ &\omega C_{b'e}\left(\frac{1}{\omega L_2}-\omega C_2\right)\left[(1-\omega^2 C_{b'e}L_1)\left(\frac{1}{\omega L_2}-\omega C_2\right)-\omega C_{b'e}\right]+\frac{(1-\omega^2 C_{b'e}L_1)}{\omega R_2 C_{ce}}g_m\left[\left(\frac{1}{\omega L_2}-\omega C_2\right)^2-\left(\frac{1}{R_2}\right)^2\right]-\left[\frac{(1-\omega^2 C_{b'e}L_1)}{R_2}\frac{\omega C_{b'e}}{R_2}\right] \end{aligned}\right\} = 0 \quad (8.26)$$

From Equation (8.26), the possible modes of oscillations are:

$$\omega_1 = \left[\frac{1}{L_2C_2}\right]^{1/2},\ \omega_2 = \left[\frac{1}{L_1C_{b'e}}\right]^{1/2},\ \omega_3 = \frac{1}{C_{b'e}C_{ce}}\left[2C_{b'e}C_{ce}\left(\frac{g_m}{R_2}\right)-\left(\frac{g_m}{R_2}\right)^2-8C_{b'e}^2\left(\frac{1}{R_2}\right)^2\right]^{1/2} \quad (8.27)$$

For the dominant mode oscillation condition, the negative resistance associated with R_{osc} can be described by solving Equation (8.24) through Equation (8.28), and the value of R_{osc} can be optimized in such a way that only desired mode (ω_1) of oscillation is sustained. The other modes (ω_2 and ω_3) must meet the constraints of insufficient gain of R_{osc} to be quenched:

$$R_{osc} = \left[\frac{(g_m+\varphi\gamma)+\omega C_{be}R_3(\omega C_{be}-\varphi\delta))}{(g_m+\varphi\gamma)^2+(\omega C_{be}-\varphi\delta)^2}\right]^{-\left[\frac{g_m}{\omega_1^2 C_2 C_{ce}(1-\omega_1^2 L_2 C_{b'e})}\right]} \quad (8.28)$$

$$L_2 = \frac{1}{\omega_1}\left\{\frac{\omega_1 C_{be}R_3(g_m+\varphi\gamma)-(\omega_1 C_{be}-\varphi\delta)}{(g_m+\varphi\gamma)^2+(\omega_1 C_{be}-\varphi\delta)^2}\right\} \quad (8.29)$$

Where

$$\gamma = g_m - (\omega_1 C_{be})^2(R_{cs}+R_T)$$

$$\delta = \omega_1[g_m C_{be}(R_{cs}+R_T)+C_{be}]$$

$$\varphi = \frac{g_m{}^3 R_{CS}}{\gamma^2+\delta^2}$$

From Equation (8.29), the voltage tunable inductor (L_2), which is a part of the resonator network, is realized using an active inductor topology.

The noise dynamics of active tunable oscillator can be described in terms of total noise voltage power, $\left|\overline{e_n^2(\omega)}\right|$, within 1Hz bandwidth as

$$\left|\overline{e_n^2(\omega)}\right|_{\omega=\omega_1} = \overline{[e_R^2(\omega_1)]_{+R}} + \overline{[e_{NR}^2(\omega_1)]_{-R}} \quad (8.30)$$

The first term in Equation (8.30) is related to the thermal noise due to the loss resistance (+R) associated with the oscillator circuit and load (R_L), and the second term is related to the effective negative resistance (-R) for compensating the net losses. The noise voltage associated with the +R and –R can be described by

$$\left|\overline{e_n^2(\omega_1)}\right|_{+R_1} = 4kTRB \Rightarrow \left|\overline{e_n^2(\omega_1)}\right|_R = [4kTR]_{B=1Hz} \tag{8.31}$$

$$\overline{[e_{NR}^2(\omega_1)]_{-R}} \approx \left[\frac{4qI_c g_m^2}{\omega_1^4\beta^2 C_{ce}^2(C_2 + C_{b'e} - L_2C_2C_{be}\omega_1^2)^2 + \left|g_m^2(t)\right|\omega_1^2(C_2 + C_{b'e} - L_2C_2C_{b'e}\omega_1^2)^2}\right] \tag{8.32}$$

After approximations, adding shot noise, flicker noise and the loss resistor, the equivalent expression of the phase noise can be given by

$$\pounds(\omega) = \left[4kTR + \frac{\left|g_m^2(t)\right|(4qI_c) + \left|g_m^2(t)\right|\left(\frac{K_f I_b^{AF}}{\omega}\right)}{\omega_1^4\beta^2 C_{ce}^2(C_2 + C_{b'e} - L_2C_2C_{be}\omega_1^2)^2 + \left|g_m^2(t)\right|\omega_1^2(C_2 + C_{b'e} - L_2C_2C_{b'e}\omega_1^2)^2}\right] \times \frac{\omega_1^2}{4\omega^2 V_{ce}^2}\left[\frac{Q_0^2}{Q_L^2} + \left(1 - \frac{1}{\omega_1^2 L_2}\left(\frac{[(C_2 + C_{b'e} - L_2C_2C_{b'e}\omega_1^2) + C_{ce}]}{C_{ce}[(C_2 + C_{b'e} - L_2C_2C_{b'e}\omega_1^2)]}\right)\right)^2\right] \tag{8.33}$$

where K_f is the flicker noise coefficient and AF is the flicker noise exponent.

Although Equation (8.1) through Equation (8.33) had to be much simplified for illustrative results, the multi-mode oscillation and noise studies have revealed the key factors affecting the performance. It has been made clear that the multi-mode oscillation associated with active inductor based resonators is usually insufficient for traditional purposes, which is often ignored in published papers. Nevertheless, by keeping the limitations in mind one can find new feasible applications for the circuits described. As described in Equation (8.27), the theoretical evaluations are in a reasonable agreement with experimental results. The deflection of theoretical results from measured data is explained by the insufficiency of the scaled device model associated with synthesized inductors. In addition to this, characterization of oscillator noise dynamics should be linked with synthesized inductor on realization of a convenient and practical circuit for tunable oscillators.

A wide tuning range voltage controlled oscillator using an active inductor has been described. For the validation of the impact of the device scaling on phase noise, tunable oscillator using an active inductor using SiGe HBTs technology has been described for a broadband frequency generation. Apart from the inherent advantages of using lower cost SiGe technology as compared to GaAs technology, the technique enables higher integration, lower area and lower power consumption. The absence of on chip inductors makes this circuit appropriate for on-chip applications. Simulations and measurements have confirmed the performances of this topology: wide tuning-range, low power operation, and acceptable phase-noise.

Figure 8-5 shows a schematic of an active inductor oscillator at 18 GHz with 20% tuning range and the device scaled (1:0.5) using SiGe HBTs transistors. As shown in Figure 8-6 device scaling increases the contribution from 1/*f* noise (near carrier), whereas, it decreases the contribution from base current shot noise and base resistance thermal noise (far carrier).

Figure 8-6 shows a typical 8dB degradation in the phase noise at close-in (at 1 kHz offset from carrier), whereas, 5dB improvement at far-offset (10 MHz offset from the carrier) when the device is scaled to half the size.

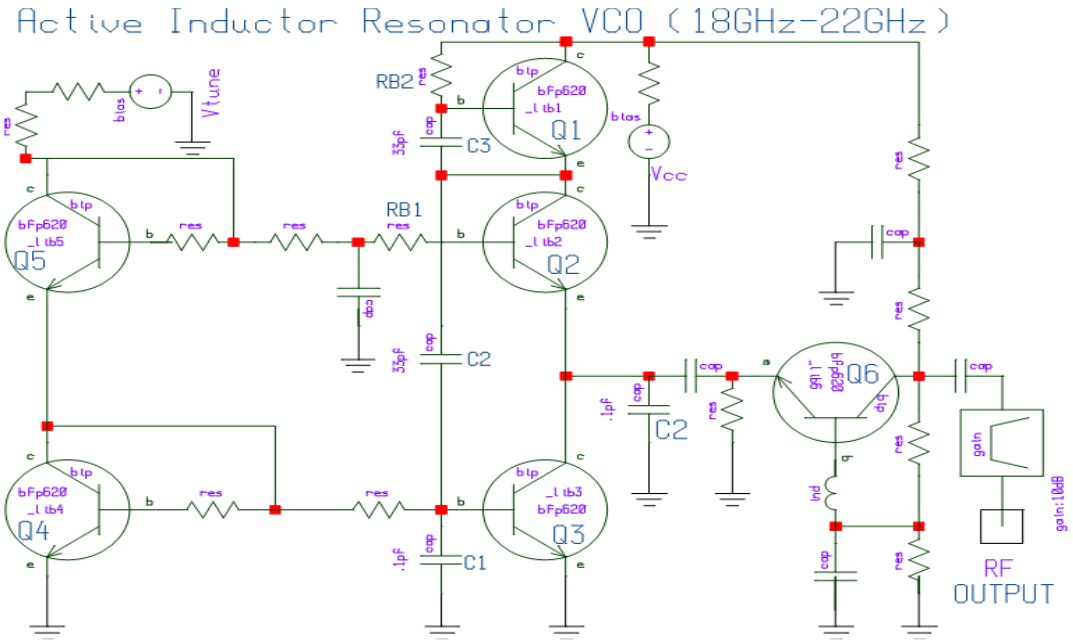


Figure 8-5 Schematic of TAIO (18 GHz-22 GHz) (Scaling 1: 0.5)

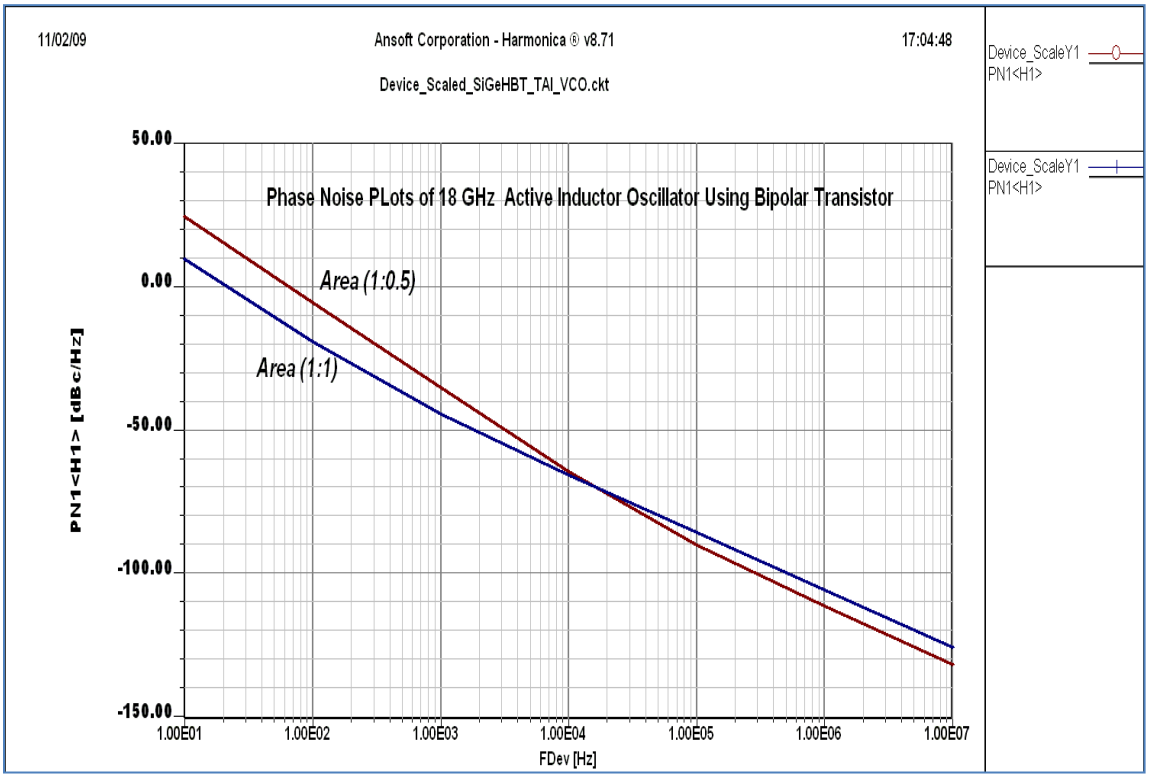


Figure 8-6 Simulated phase noise plot of TAI VCO (Scaling 1: 0.5)

From Equation (8.21), the $1/f$ noise up-conversion can be reduced by minimizing the value of C_0, which is a function of the slope of the rise and fall times of the waveform across the active devices that simulate the voltage tunable inductor circuits. The goal for improving $1/f$ noise characteristics is paramount for enabling a seamless transition from varactor-tuned LC resonator oscillator topologies to inductor-tuned oscillator topologies for wireless applications. Nevertheless, the advantages of integration in a small chip-area make inductor-tuned VCO technology a cost-effective alternative for RFIC/MMIC VCO solutions.

An oscillator designed with active inductor resonator is presented. From the theoretical analysis and simulations, it is obvious that TAIO circuit as shown in Figure 8-7 has the advantages of wider tuning range and integrable solution in smaller chip area. The main disadvantage of noise performance in scaled device is mainly due to more component noise associated with synthesized inductor and smaller voltage swing across the realized indictor-tuned resonator network. The design techniques of TAIOs to obtain a larger voltage swing and better phase noise performance are discussed. With the trend of device scaling, the maximum obtainable oscillation frequency and phase noise performance can be improved.

Underlying the physical mechanism controlling the noise dynamics and the impact of device scaling, the designer can minimize the noise contributions (broadband and $1/f$ noise) of the scaled active inductor in tunable oscillator circuits. This novel approach incorporates a dynamic phase-injection mechanism that minimizes the noise figure and current consumption while providing the designer an option of trading phase noise and tuning range for a given power consumption.

Figure 8-7 shows the schematic of the self-injection-locked scaled active inductor oscillator using SiGe HBTs for the minimization of noise for low cost and low phase noise signal source applications.

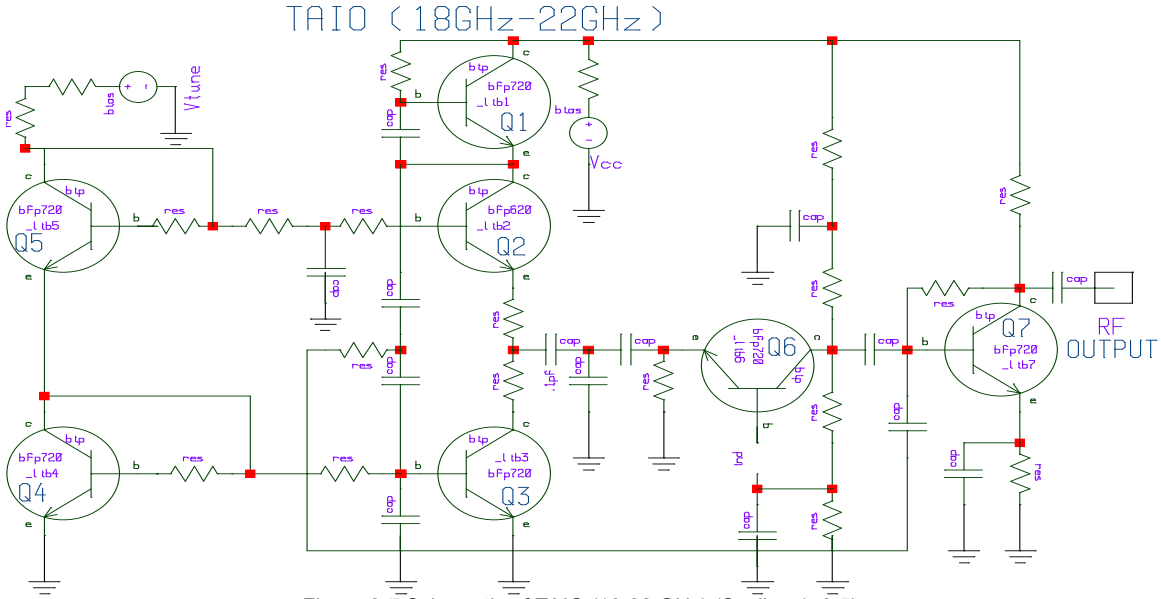


Figure 8-7 Schematic of TAIO (18-22 GHz) (Scaling 1: 0.5)

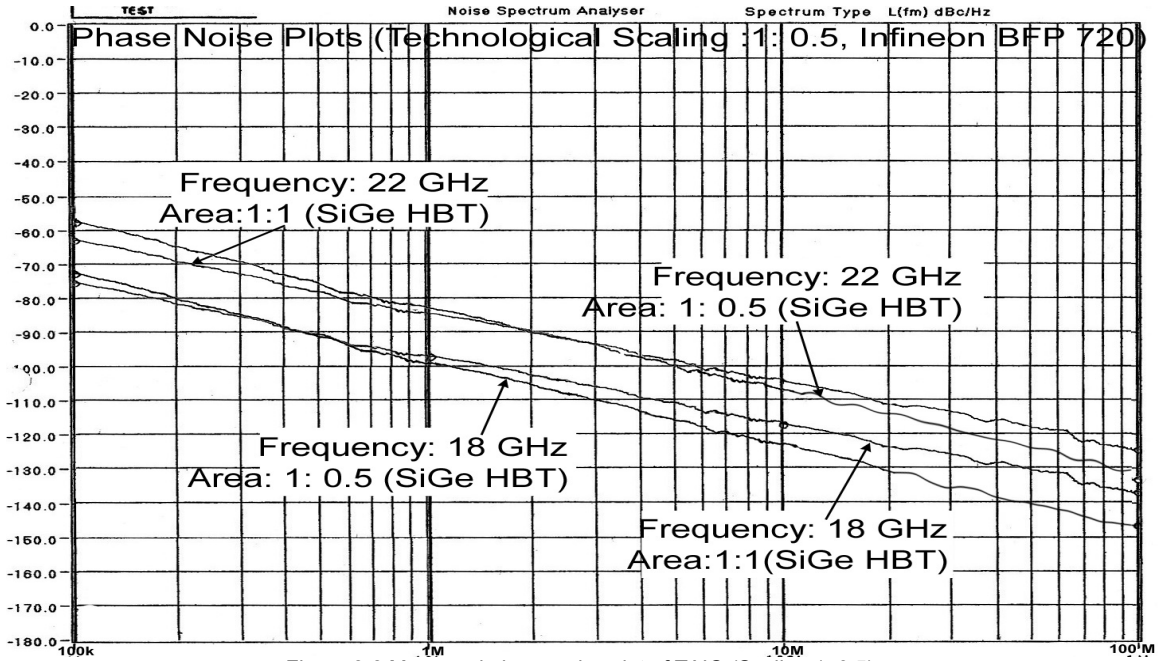


Figure 8-8 Measured phase noise plot of TAIO (Scaling 1: 0.5)

Figure 8-8 shows the measured phase noise plots of the oscillator with a 4000 MHz tuning range and a bias of 3V, 30mA. The device scaling increases the contribution of 1/*f* noise (near carrier) and it decreases the contribution from base current shot noise and base resistance thermal noise (far carrier). Note that the phase noise plot shows typically 4-8dB degradation at close-in (1 kHz offset from carrier) and 5-10dB improvement at far-offset (10 MHz offset from the carrier) when device is scaled to half the size.

Although the CAD simulated phase noise at 100 kHz offset for a 20 GHz carrier frequency is -75dBc/Hz which is inferior by 10-15dB in comparison to commercially available discrete passive LC resonator based varactor-tuned oscillator topology for a given DC power consumption. In addition to this 1/*f* noise associated with the active device (SiGe HBT BFP 620F, Infineon) that forms active inductor under large signal drive level can become a limiting factor and restricts the applications. But the advantages of integration in a small chip area make this technology as a promising candidate for RFIC/MMIC VCOs solutions. By incorporating noise-feedback and dynamic-phase-injection mechanism, it is shown that user can have an option of trade-in phase noise versus tuning range for a given power consumption.

However, the far out phase noise is degraded by 8-10dB, which can be minimized by noise-feedback network that controls the average noise factor of the active inductor oscillators. From the theoretical analysis and simulations, it is obvious that TAIO circuit has the advantages of wider tuning range and integrable solution in a smaller chip area.

Using a discrete SiGe HBTs, a prototype VCO is implemented for demonstration. The fabricated circuit exhibits a wide frequency tuning range from 18 GHz to 22 GHz while maintaining excellent circuit performance in terms of close-in phase noise and output power within the entire frequency range. It is suitable for the implementation of fully integrated RF transceiver for multi-standard applications. The emerging applications of tunable active inductor topology continue to

unfold along with the inception of new design techniques for improving phase noise and dynamic range. In spite of these drawbacks active inductors have a significant advantage over passive inductors in terms of die-area, Q-factor, and issues regarding EMI and floor planning.

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9. Design Challenges, Conclusion and Futuristic Work

Where do we go from here ?
The number of discrete components has shrunk into integrated circuits in the base-band and IF-sections, the same applying to many parts in the RF section. Passive tunable inductors, however, have not been among those preferred components, and are expensive and bulky individual components in the RF section, including cumbersome in automated manufacturing processes. Although, a synthesized tunable inductor using active devices would rectify all these drawbacks but no commercially significant progress has been made in realizing them before this thesis because of poor phase noise performance, tuning linearity and dynamic range. Unlike their passive counterparts such as tuning diodes and switched capacitors, synthesized tunable inductors have noise contribution and distortion; they consume power and need constant fine tuning for maintaining thermal drift and accuracy. However, realization with tuning diodes and switched capacitors at high frequencies for tunable oscillator applications become challenging due to package parasitic that limits the tunability.

Tunable Active Inductor Oscillators (TAIOs) have shown seem to offer the best possibilities for monolithic high-frequency signal sources realizations. The objective of this study was to investigate the possibilities offered by synthesized active inductors in tunable oscillator design, recognize their limitations and find potential applications in the field of portables and test equipments. Different active inductor topologies have been probed in order to find the suitability and optimal performance for each technique with respect to tuning element in oscillators and filters.

9.1 Design Challenges

There is a misconception found in many papers is to regard synthesized inductor-tuned resonators as direct alternatives to varactor-tuned resonators. This is the result of neglecting noise and distortion contributions associated with active devices that comprises the synthesized inductors. Although the absolute theoretical results give an optimistic view, their relative accuracy is good and useful for practical applications, if permitted by the chosen process and practical issues. Several active inductors configuration have been briefly discussed, with the emphasis on low noise, low power consumption and small size. Different process technologies are experimented, and their suitability for tunable oscillator has been evaluated. Understanding the theoretical limitations, the performance figures have been on a par with other published works, but generally, somewhat lower noise figures and power consumptions have been acquired. An in-depth investigation of the active inductor, implemented in discrete version process, has been the primary motivator driving this research work. Literature surveys and comparisons to other published works, focused on active inductors (AIs), have been made within this thesis. Different design topologies and strategies to realize AIs have been offered. The shortcoming of the AI, over statistical process skew, has been uncovered and the obligation to tune as an essential strategy to avoid instability, inductance variation and low quality has been stressed.

9.2 Conclusion

In this research work, Tunable Active Inductor Oscillators (TAIOs) are realized using discrete SiGe HBTs for the demonstration of a cost-effective alternative of Varactor-Tuned Oscillators at

microwave frequencies. In the present study, a different configuration of a tunable inductor is shown derived from active devices for comparison in terms of performance and feasibility. The emphasis is put on noise, power consumptions, and tuning characteristics, as they are the main concern in tunable oscillator's applications. A method for understanding active inductor noise dynamics and its partial or eventual cancellation with appropriate injection and noise filtering techniques is presented. The theoretical and practical design issues related to TAIO circuits have been discussed and tackled in this thesis as follows:

- Investigation of the potentials and challenges of using active inductors to provide area-efficient and wide-tuning in oscillator circuits and compensation for noise and power consumptions
- This thesis explores the use of active inductors as a compact alternative to the bulky passive spiral structures in varactor-tuned oscillator circuits.
- Develop the novel techniques and design methods to enhance the performance of active inductors when applied to tuning element in resonator tank and filter circuits
- Design and implementation of the prototype circuits using discrete components and verification of the performance improvement, if at all, brought by the use of active inductor as a cost-effective alternative of varactor-tuned oscillator circuits.
- Investigation of possibility of the tunable oscillator using the variable inductor is a quite useful for reconfigurable RF circuits for multi-band/mode ratio.

Although the active inductor is noisy and has limited dynamic range compared to spiral inductors, in this thesis we show that by utilizing injection-locking mechanism, the noise contribution from the active inductor can be reduced to a minimum level.

9.3 Futuristic Work

Although important, the fabrication of integrated TAIOs is out of the scope of this research work. As a partial fulfillment of Dr.-Ing-Habil and relying on my dissertation (A New and Efficient Method of Designing Low Noise Microwave Oscillators"), this research work was focused on finding cost-effective alternative of Varctor-tuned tunable filter and oscillator technology. As a matter of fact, this thesis is divided in 9-chapters with the projections that future research work following this project could be directed. First and foremost, realization of integratable multi-band VCO, as a user-defined signal sources is the most obvious possibility for future work. Incorporation of automatic active tuning to this design would further fulfill the "hands off" classification of this design tuning strategy.

The future of monolithic TAIOs design will be promising if the development of high-Q TAIs provides new possibilities for tuning features realizations. At some point, however, it will be questionable to use varactor diodes at all, and the topologies will revert to integrated TAIOs. Research on these subjects will be of great interest, given the motivation of this work. For active inductors to be reliably deployed in tunable oscillator circuits, the robustness of such circuits in the presence of process variations has to be more thoroughly investigated, especially when implemented in MMIC technologies in which process variations are getting much worse. It is thus one of the most important follow-up works to be considered. It is thus expected to be more challenging to use active-inductor topology where phase noise and dynamic range are key

factors. Further improvements are still in progress, which aim to reduce the active inductor's noise contribution, power dissipation, and increase its frequency tuning range to compensate PVT variations; suggested as follows:

- Low power active inductor that is able to reach lower inductance value with high f_0. Existing design shows that higher power consumption is needed to reach lower inductance value and high f_0. This study should also enhance inductance range for better tuning capability.

- Use suitable MMIC technologies that will work with lower voltage supply, this will help to reduce power consumption.

- Better understanding of noise cancellation of noise generated by active inductor. This will improve noise performance, including the figure of merit (FOM) of design.

- Layout optimization to ensure active inductor performance is not degraded due to electromagnetic interference and cross-coupling.

- A floating active inductor can be connected to any source. Existing design required DC blocks to ensure that active inductor internal nodes will not be impacted due to DC introduce by the system.

- The hybrid approach (combination of the active variable inductor and the switched capacitors) can provide wider tuning range.

The possibility of oscillator design based on problems associated with the active inductor topology was demonstrated. Because of the design challenges pointed out above, this type of VCO still lacks the acceptability as a commercial solutions, continuous research is needed for overcoming the limiting factors above 30 GHz linked with active inductor-tuned VCOs.

Symbol	Description
LTV	Linear time variant
$NLTV$	Nonlinear time variant
$LTIV$	Linear time invariant
ATI	Active tunable inductor
AI	Active Inductor
$TI\ or\ TAI$	Tunable inductor or Tunable active inductor
$TAIO$	Tunable Active Inductor Oscillator
$ATIO$	Active tunable inductor oscillator
AIO	Active inductor oscillator
VCO	Voltage controlled oscillator
G_m	Large-signal transconductance
g_m	Small-signal transconductance
$a_n(x)$	Fourier coefficient
$I_n(x)$	Modified Bessel function of order n
$I_e(t)$	Emitter current
$I_c(t)$	Collector current
I_{cob}	Collector reverse current
$V_{n(total)}$	Total noise voltage
V_{sn}	Noise due to source
$V_{n(network)}$	Noise due to network
Y_g	Generator admittance
Y_{opt}	Optimum noise admittance
F_{min}	Minimum achievable noise figure
R_n	Noise resistance
$[C_Y]$	Y-parameter noise correlation matrix
$[C_A]$	ABCD Correlation Matrix
Y_{cor}	Correlation factor
$\overline{i_{bn}^2} = 2qI_b\Delta f$	Mean square value of noise due to base current

$\overline{i_{cn}^2} = 2qI_c\Delta f$	Mean square value of noise due to collector current
$\overline{i_{con}^2} = 2qI_{cob}\Delta f$	Mean square value of noise due to reverse collector current
$\overline{v_{bn}^2} = 4kTR_b\Delta f$	Mean square value of noise voltage due to base resistance
$S(i_{cn}) = 2kTg_m$	Noise power spectral densities due to collector current
$S(i_{bn}) = \frac{2kTg_m}{\beta}$	Noise power spectral densities due to base current
$S(v_{bn}) = 4kTR_b$	Noise power spectral densities due to base resistance
$S(v_{sn}) = 4kTR_s$	Noise power spectral densities due to source resistance
$\overline{i_d^2} = 4kTg_mP\Delta f$	Mean square value of noise due to drain current
$\overline{i_g^2} = \frac{4kT(\omega C_{gs})^2 R}{g_m}\Delta f$	Mean square value of noise due to gate current
$P = \left[\frac{1}{4kTg_m}\right]\overline{i_d^2}/Hz$	FET noise coefficient
$R = \left[\frac{g_m}{4kT(\omega C_{gs})^2}\right]\overline{i_g^2}/Hz$	FET noise coefficient
$C = -j\left[\frac{\overline{i_g i_d^*}}{\sqrt{\left[\overline{i_d^2}\,\overline{i_g^2}\right]}}\right]$	FET noise coefficient
P	0.67 for JFETs and 1.2 for MESFETs
R	0.2 for JFETs and 0.4 for MESFETs
C	0.4 for JFETs and 0.6-0.9 for MESFETs
Z_s	Complex source impedance
$a = \left[1 + \frac{f^2}{f_b^2} - \alpha_\theta\right]\frac{1}{\alpha_\theta}$	Modified factor
X	Drive-Level
$\left(\frac{kT}{q}\right)x$	Drive-Voltage
$2\left[\frac{I_1(x)}{I_0(x)}\right]$	Fundamental component of current

$\left[\frac{I_2(x)}{I_1(x)}\right]$	Second harmonic component of current
φ	Conduction angle
n	Transformation factor
n_{opt}	Optimum transformation ratio
R_P	Parallel loss resistance
Q_L	Loaded quality factor
f_0	Center frequency
f_c	Flicker corner frequency
f_m	Frequency offset
P_{sav}	Average power at oscillator output
K_0	Oscillator voltage gain
$F = \frac{\overline{i_L^2}}{i_{LO}^2}$	Noise factor
NF	Noise Figure
$\mathcal{L}(f_m)$	Ratio of sideband power in a 1 Hz bandwidth at f_m
E_B, E_H	Vector of harmonic-balance (HB) errors
E	Vector of real and imaginary parts of all HB errors
X_B, X_H	Vector of state variable (SV) harmonics
J_B, J_H	Vector of forcing terms
$\delta X_B, \delta X_H$	Perturbation of the circuit state
M	Jacobian matrix of the HB errors
$\delta\omega_0(\omega)$	Phasor of the pseudo-sinusoidal components
$N_k(\omega)$	Noise power spectral density
$C_k(\omega)$	Normalized correlation coefficient
$J_p(\omega)$	Side-band noise sources
$U_p(\omega)$	Side-band noise sources
I_k^{SS}	Noise power spectral density
$S_{\Delta\theta}(\omega)$	Power spectral density of the input phase error

$\boldsymbol{\theta_d}$	Peak phase deviation
$\boldsymbol{e_N(t)}$	Noise signal voltage
$\boldsymbol{R_N(t)}$	Time variant negative resistance
$\boldsymbol{k}$	Boltzmann's constant (1.38E-23 J/K)
$\boldsymbol{kT}$	4.1×10^{-21} at 300 K_0 (room temperature)
$\boldsymbol{R}$	Equivalent noise resistance of tuning diode
$\boldsymbol{G}$	Compressed power gain of the loop amplifier
$\boldsymbol{TF(j\omega)}$	Closed loop transfer function
$\boldsymbol{H(j\omega)}$	Open loop transfer function
$\boldsymbol{\langle\lvert\delta\varphi_{ck}(\omega)\rvert^2\rangle}$	PM noise at k^{th} harmonic
$\boldsymbol{\langle\lvert\delta\varphi_{mk}(\omega)\rvert^2\rangle}$	PM noise due to contribution of modulation
$\boldsymbol{\langle\lvert\delta A_{ck}(\omega)\rvert^2\rangle}$	AM noise to carrier ratio at k^{th} harmonic
$\boldsymbol{\langle\delta\varphi_{ck}(\omega)\delta A_k(\omega)^*\rangle}$	PM-AM correlation coefficient for the k^{th} harmonic
$\boldsymbol{\langle\lvert J_H(\omega)J_H^{\otimes}(\omega)\rvert\rangle}$	Correlation matrix
$\boldsymbol{T_F^{\otimes}}$	Conjugate-transpose
$\boldsymbol{T_{Ak}}$	Row-matrix
$\boldsymbol{T_F}$	Frequency transfer matrix
$\boldsymbol{Y_R(k\omega_\theta)}$	Trans-admittance matrix
$\boldsymbol{\lvert I_k^{SS}\rvert\, exp(j2\varphi_k^{SS})}$	k^{th} harmonic of the steady-state current through the load
$\boldsymbol{C_{k,-k}^*(\omega)}$	Correlation coefficient of the upper and lower sidebands
$\boldsymbol{m(t)}$	Modulating signal
$\boldsymbol{K_p}$	Phase sensitivity
$\boldsymbol{\beta = \frac{\Delta f}{f_m}}$	Modulation index of the modulating signal
$\boldsymbol{SNR}$	Signal to noise ratio
$\boldsymbol{A_{SSB}}$	Sideband amplitude of a phase modulation
$\boldsymbol{C_0}$	Coefficient of Fourier series, 0^{th} order of the ISF
$\boldsymbol{\Delta f}$	Noise bandwidth
$\boldsymbol{\omega_{1/f}}$	1/f noise corner frequency of the device/transistor

q_{max}	Maximum charge on the capacitors in the resonator
$NFT_{inr(\omega)}$	Noise transfer function due to resonator loss resistance
$NFT_{vbn(\omega)}$	Noise transfer function due to transistor base resistance
$NFT_{ibn(\omega)}$	Noise transfer function due to the transistor base current
$NFT_{ifn(\omega)}$	Noise transfer function due to flicker noise
$NFT_{icn(\omega)}$	Noise transfer function due to collector current
K_f	Flicker noise constant
AF	Flicker noise exponent
$\sigma(t)$	Complex envelope of the frequency modulated signal
Γ_{rms}	Impulse sensitivity function
EMF	Electromotive force
β^+	Large-signal current gain
Y_{11}^+	Large-signal input admittance
Y_{21}^+	Large-signal transconductance